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The AXIOM software layers

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ABSTRACT

People and objects will soon share the same digital network for information exchange in a world named as the age of the cyber-physical systems. The general expectation is that people and systems will interact in real-time. This poses pressure onto systems design to support increasing demands on computational power, while keeping a low power envelop. Additionally, modular scaling and easy programmability are also important to ensure these systems to become widespread. The whole set of expectations impose scientific and technological challenges that need to be properly addressed.

The AXIOM project (Agile, eXtensible, fast I/O Module) will research new hardware/software architectures for cyber-physical systems to meet such expectations. The technical approach aims at solving fundamental problems to enable easy programmability of heterogeneous multi-core multi-board systems. AXIOM proposes the use of the task-based OmpSs programming model, leveraging low-level communication interfaces provided by the hardware. Modular scalability will be possible thanks to a fast interconnect embedded into each module. To this aim, an innovative ARM and FPGA-based board will be designed, with enhanced capabilities for interfacing with the physical world. Its effectiveness will be demonstrated with key scenarios such as Smart Video-Surveillance and Smart Living/Home (domotics).

1. Introduction

We are entering the Cyber-Physical age, in which both objects and people will become nodes of the same digital network for exchanging information. Therefore, the expectation is that "things" or systems will become somewhat smart as people, having to permit a rapid and close interaction not only human-human and system-system, but also human-system, and system-human. More scientifically, we expect that such Cyber-Physical Systems (CPS) will at

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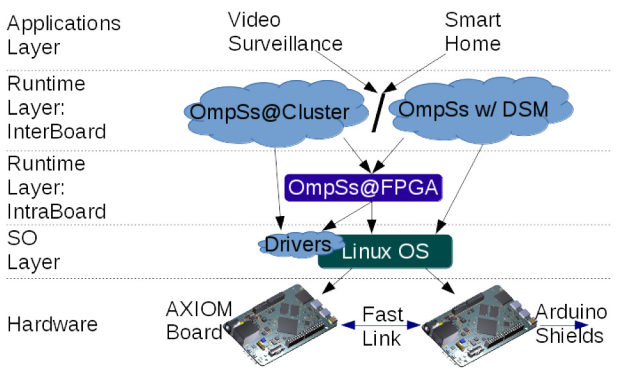

Fig. 1. The AXIOM Software Layers.

least react in real time, provide enough computational power for the assigned tasks, consume the least possible energy for such tasks (energy efficiency), allow for an easy programmability, scaling through modularity and exploit at best existing standards at minimal costs.

The AXIOM project (Agile, eXtensible, fast I/O Module) aims at researching new hardware/software architectures for CPSs in which the above expectations are realized. The project, started on February 2015, will span over 3 years. The coordination of the project is carried out by the University of Siena (UNISI). UNISI also takes the evaluation part of the project. Foundation for Research and Technology - Hellas (FORTH) develops the interconnection between boards. Barcelona Supercomputing Center (BSC) is responsible of the OmpSs (OpenMP+StarSs) programming model and software toolchain. Partner EVIDENCE takes the lead on the development of the runtime systems. Partner SECO designs and builds the prototype board. Partner HERTA Security provides a video-surveillance use case. Partner VIMAR provides a smart-building use case.

Fig. 1 shows the software layers used in this project. As it can be seen the project addresses all the levels of the system, from the application level, that includes two key application domains, to the hardware level. That includes developing a specific runtime software manager (OmpSs@FPGA), a fast interconnection link (Fast Link) and even the AXIOM board itself. As can also be seen in Fig. 1 the project aims to develop a board that can work well both alone or as part of a larger system (i.e. a group of boards interconnected by the AXIOM link). This modular capabilities are addressed from both the hardware side (the implementation of the AXIOM link) and the software side (the development of inter-node execution capabilities using the OmpSs programming model). From the hardware point of view is one of the aims of the project to make the board accessible in terms of cost (as cheap as possible, even around one hundred euros) while making it powerful enough to deal with the envisioned use cases. This holistic development is what we call the AXIOM platform.

The specific objectives of the AXIOM project are:

- Realizing a small board that is flexible (suitable for a wide range of applications), energy efficient and modularly scalable (AXIOM Board in Fig. 1). We will use an ARM- and FPGA-based chip with custom high-speed interconnects to build the AXIOM prototype board.
- Easy programmability of multi-core, multi-board, FPGA node, with the OmpSs programming model (OmpSs@Cluster/OmpSs over DSM, and OmpSs@FPGA in Fig. 1), and improved thread management and real-time support from the operating system. The software will be Open-Source.
- Easy interfacing with the Cyber-Physical world, based on the Arduino shields [1,2], pluggable onto the board. This shields are going allow the developed board to be extended with sensors (e.g. a camera). They will provide new functionalities to the developed board to widen the scope of its applications.
- Contribute to standards, in the context of the Standardization Group for Embedded Systems (SGET) and OpenMP.

The rest of the paper is organized as follows. Section 2 explains the AXIOM software layers. Section 3 explains the AXIOM link development. Section 4 explains the applications evaluated and the expected scenarios. Section 5 explains the experimental setup followed by Section 6 that presents the first results obtained by the project. Section 7 explains the related work. Finally, Section 8 summarizes the conclusions and the envisioned future work.

2. The AXIOM software

One of the problems when building a complex ecosystem like the one described in Fig. 1 is how to easily program applications that should take advantage at the same time of both on-chip resources (i.e. the FPGA and the multiple cores) and multiple board resources (through fast link multiple board connection).

Several solutions have been proposed during the last decades to parallelize computations on multi-core systems. However, no unanimous consensus on the best solution has been achieved. On one hand, some solutions are based on message-passing mechanisms (e.g., MPI), which are usually considered too difficult to use for developers not accustomed to parallel programming. For example, parallelizing existing legacy serial codes, like face detection, audio processing or search algorithms, with MPI need a large code rewriting to add the communication primitives and synchronization needed. Usually this means to rewrite the full application at once to take advantage of the cluster. Instead, models targeting SMPs, are usually based on code annotations, that allow introducing less changes in the original code, and also incrementally work on the different parts of the applications, that can be tested much earlier than when using message passing.

Another possibility that is going to be explored in this project is the use of a DSM system. Distributed shared memory (DSM) is a form of memory architecture where actually physically separate memories can be addressed as one logically shared address space. The main advantage of this memory organization is that it can be easily programmed as the program can access all the available memory despite its real physical location being the DSM support (probably integrated with the OS) the one responsible of managing the communication. On the other hand, this management when not properly handled can lead to unnecessary or inefficient communication patterns.

AXIOM will leverage OmpSs, a task dataflow programming model that includes heterogeneous execution support as well as data and task dependency management [3] and has significantly influenced the recently appeared OpenMP 4.0 specification.

2.1. The OmpSs programming model

In OmpSs, tasks are generated in the context of a team of threads that run in parallel. OmpSs provides an initial team of threads as specified by the user upon starting the application.

Tasks are defined as portions of code enclosed in the *task directive*, or as user-defined functions, also annotated as tasks, as follows:

```
#pragma omp task [clause − list]
  {structured − work|
  function − declaration|
  function − definition}
```

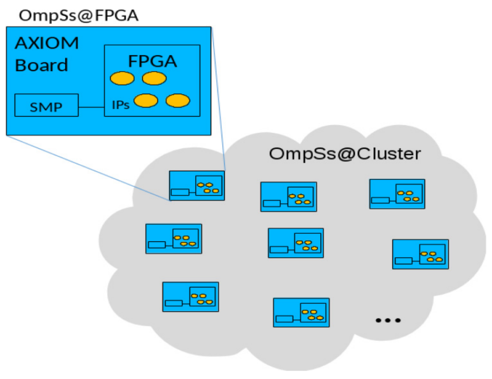

Fig. 2. General view of OmpSs@FPGA and OmpSs@Cluster execution context.

A task is created when the code reaches the task construct, or a call is made to a function annotated as a task. The task construct allows to specify, among others, the clauses *in, out* and *inout*. Their syntax is:

$$\texttt{in}\ (\texttt{data}-\texttt{reference}-\texttt{list})$$
$$\texttt{out}\ (\texttt{data}-\texttt{reference}-\texttt{list})$$
$$\texttt{inout}\ (\texttt{data}-\texttt{reference}-\texttt{list})$$

The information provided is used to derive dependencies among tasks at runtime, and schedule/fire a task. Tasks are fired when their inputs are ready and their outputs can be generated.

Dependencies are expressed by means of data-reference-lists. A data-reference in such a list can contain either a single variable identifier, or also references to subobjects. References to subobjects include array element references (e.g., *a[4]*), array sections (*a[3:6]*), field references (*a.b*), and elaborated shaping expressions (*[10][20] p*). The latter means the rectangular area starting at address *p*, with a shape of 10 rows and 20 columns.

OmpSs is based on two main components: i) The Mercurium compiler gets C/C++ and FORTRAN code, annotated with the task directives presented above, and transforms the sequential code into parallel code with calls to the Nanos++ runtime system; and ii) The Nanos++ runtime system gets the information generated by the compiler about the parallel tasks to be run, manages the task dependences and schedules them on the available resources, when those tasks are ready. Nanos++ supports the execution of tasks in remote nodes, and heterogeneous accelerators.

At the lower level, the AXIOM project will investigate and implement the OmpSs programming model on top of the following intra- and inter-node technologies:

- **Intra-node:** The most important target here is FPGA programmability support.
  - OmpSs@FPGA, for easy exploiting of the FPGA acceleration;
- **Inter-node:** In this case two different approaches can be addressed based on the performance requirement, although they can be integrated in the same scenarios, to work with different memory address spaces.
  - OmpSs@cluster, for efficient parallel programming hiding message-passing complexities;
  - OmpSs on a DSM-like paradigm, for easy parallelization of legacy code.

Fig. 2 shows the overall view of OmpSs@FPGA and OmpSs@cluster execution context in a multi-board system. Each FPGA-based node will be addressed by the OmpSs@FPGA support meanwhile the OmpSs@cluster will help to transparently program all the multi-node system.

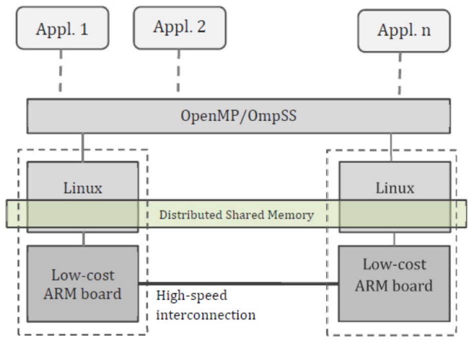

Fig. 3. General view of OmpSs over a DSM system.

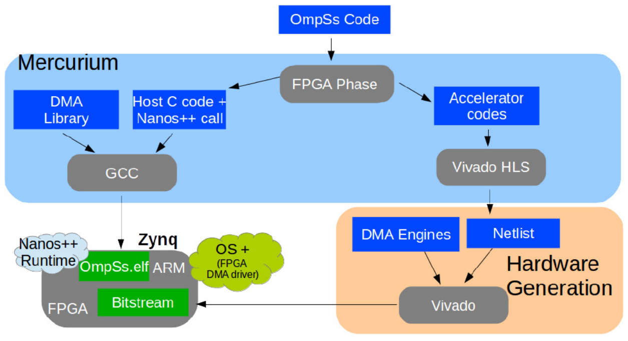

Fig. 4. OmpSs@FPGA ecosystem compilation flow.

Fig. 3 shows the overall view of a DSM system where OmpSs@FPGA would have the same intra-node influence and OmpSs@cluster will appear like a single intra-node OmpSs running over a transparent DSM system.

2.2. OmpSs@FPGA

The OmpSs@FPGA ecosystem consists of the infrastructure for compilation instrumentation and execution from source code written in C/C++ to ARM binary and FPGA bitstream for Zynq. The compilation infrastructure provides support to (1) generate ARM binary code from OmpSs code, that can run in the ARM-based SMP of the Zynq SoC, (2) extract the kernel of the part of the application to be accelerated into the FPGA and (3) automatically generate a bitstream that includes the IP cores of the accelerator(s), the DMA engine IPs, and the necessary interconnection. In addition, the ARM binary can be instrumented to generate traces to be analyzed offline with the Paraver tool [4].

The runtime infrastructure should allow heterogeneous tasking on any combination of SMPs and accelerators, depending on the availability of the resources and the target devices.

Fig. 4 shows the high level compilation flow using our OmpSs@FPGA ecosystem. The OmpSs code is passed through the source-to-source compiler Mercurium [5], that includes a specialized `FPGA` compilation phase to process annotated `FPGA` tasks. For each of those tasks, it generates two C codes. One of them is a `Vivado HLS` (source to HDL Xilinx tool) annotated code for the bitstream generation branch ("accelerator codes" box in Fig. 4). The other is an intermediate host source code with OmpSs runtime (Nanos++) calls that is generated for the software generation branch ("Host C code + Nanos++ runtime call" box in Fig. 4). Both the hardware and the software generation branches are transparent to the programmer.

Fig. 5 shows a matrix multiply example that has been annotated with OmpSs directives. This code shows a parallel tiled matrix multiply where each of the tiles is a task. Each of those tasks

```
#pragma omp target device(fpga, smp) copy_deps
#pragma omp task in(a[0:BS*BS-1], b[0:BS*BS-1]) \
                 inout(c[0:BS*BS-1])
void matrix_multiply(int BS, float a[BS][BS],
                     float b[BS][BS],
                     float c[BS][BS]) {
    for (int ia = 0; ia < BS; ++ia)
        for (int ib = 0; ib < BS; ++ib) {
            float sum = 0;
            for (int id = 0; id < BS; ++id)
                sum += a[ia][id] * b[id][ib];
            c[ia][ib] = sum;
        }
}

int main( int argc, char * argv[] ){
 int BS = ...
 ...
 for (i=0; i < NB; i++)
   for (j=0; j < NB; j++)
     for (k=0; k < NB; k++)
       matrix_multiply(BS, A[i][k], B[k][j], C[i][j]);
 #pragma omp taskwait
 ...
}
```

Fig. 5. OmpSs directives on matrix multiplication.

has two input dependences and an inout dependence that will be managed at runtime by Nanos++. Those tasks will be able to be scheduled/fired to an SMP or FPGA, as it is annontated in the target device directive, depending on the resource availability. The `copy_deps` clause associated to the `target` directive hints the Nanos++ runtime to copy the data associated with the input and output dependences to/from the device when necessary.

2.3. OmpSs@cluster

OmpSs@cluster is the OmpSs flavor that provides support for a single address space over a cluster of SMP nodes with accelerators. In this environment, the Nanos++ runtime system supports a master-worker execution scheme. One of the nodes of the cluster acts as the master node, where the application starts. In the rest of nodes where the application is executed, worker processes just wait for work to be provided by the master.

In this environment, the data copies generated either by the `in`, `out`, `inout` task clauses are executed over the network connection across nodes, to bring data to the appropriated node where the tasks are to be executed.

Following the Nanos++ design, *cluster threads* are the components that allow the execution of tasks on worker nodes. These threads do not execute tasks themselves. They are in charge of sending work descriptors to their associated nodes and notifying when these have completed their execution. One cluster thread can take care of providing work to several worker nodes. In the current implementation, cluster threads are created only on the master node of the execution. Slave nodes cannot issue tasks for remote execution and thus they do not need to spawn cluster threads.

In Nanos++, the device specific code has to provide specific methods to be able to transfer data from the host address space to the device address space, and the other way around. The memory coherence model required by OmpSs is implemented by two generic subsystems, the *data directory* and the *data cache*, explained below.

Fig. 6 shows how the different Nanos++ subsystems are organized to manage the memory of the whole cluster. The master node is the responsible for keeping the memory coherent with the OmpSs memory coherence model, and also for offering the OmpSs single address space view. The master node memory is what OmpSs considers the *host memory* or *host address space*, and

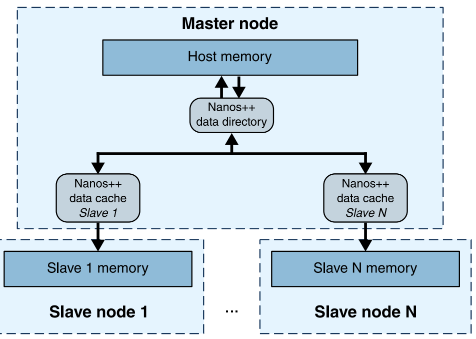

Fig. 6. Nanos++ distributed memory management organization.

it is the only address space exposed to the application. The memory of each worker node is treated as a private device memory and is managed by the master node.

The *data cache* component manages the operations needed at the master node to transfer data to and from worker memories. There is one data cache for each address space present on the system. Operations performed in a data cache include allocating memory chunks, freeing them and transferring data from their managed address spaces to the host address space and the other way around. Data caches also keep the mapping of host memory addresses to their private memory addresses. Memory transfer operations are implemented using network transfers. Allocation and free operations are handled locally at the master node.

A memory reference may have several copies of its contents on different address spaces of the system. To maintain the coherence of the memory, the master node uses the *data directory*. It contains the information of where the last produced values of a memory reference are located. With it, the system can determine which transfer operations must perform to execute a task in any node of the system. Also, each task execution updates the information of the data directory to reflect the newly produced data.

The implementation of the network subsystem is currently based on the active messages provided by the GASNet communications library. In the context of AXIOM, we will adapt the networking on the communications library provided for the Zynq platform.

2.4. OmpSs on DSM-like systems

DSM is a well-known research topic, and it can be implemented either at software or at hardware level (with a full range of hybrid approaches).

We will work on the performance analysis of current DSM implementations. After that the project will decide upon the design and development of a proper, reliable and efficient mechanism to implement a DSM-like paradigm integrated in the Linux OS. The mechanism will run on the reference platform. It will allow to leverage the simplicity and scalability of the OmpSs framework on top of the AXIOM platform. It will be released as Open-Source software, and it is expected to bring benefits to both the ICT and the embedded industries.

2.5. Operating system support

The operating system used in the project will be Linux. One of the advantages of using a SoC like the Zynq is that Linux can be run on the ARM cores of the platform off-the-shelf. This kind of system has the advantage of the easiness to program a standard processor like the ARM along with the raw performance power of the FPGA fabric that will be used through the OmpSs programming model.

We will investigate the possibility of integrating features in the OS to load balance the work across the nodes through the high-speed interconnection. Finding an efficient solution is an aimed outcome of the project since current solutions for load balancing in distributed systems may be expensive, too specific, or difficult to program (with paradigms such as MPI).

Particular attention will be given to scalability and latency issues, by implementing lock-free data structures. Another relevant aspect will be the necessity of properly managing events in real-time.

The OS scheduler will be extended to enable it distributing threads across the different nodes. The low-level thread scheduler (LLTS [6–10], discussed in Section 7) may be accelerated in hardware, by mapping its structure in the FPGA cards composing the evaluation platform. This will avoid bottlenecks from the scheduler, thus increasing the performance of parallel applications.

3. The AXIOM link

The AXIOM platform will be built around FPGA-based SoC, as exemplified by the Zynq platform by Xilinx. Zynq devices feature a dual- or quad-core ARM Cortex A9 processor closely connected to an FPGA fabric. The closeness of the connection (and hence the low latency) and the flexibility of the reconfigurable FPGA logic make the combination very powerful in terms of customization. In addition, Zynq devices feature gigabit-rate transceivers that will be used to provide ample communication bandwidth between AXIOM nodes.

In terms of connectivity, AXIOM -besides including classical connectivity (e.g., Internet)- will also bring modularity at the next level, allowing the construction of more compute intensive and performance systems through low-cost but scalable high-speed interconnect. This interconnect, subject of research and design during the project, will utilize relatively low cost SATA connectors to interconnect multiple boards. Such connectivity will allow to build (or upgrade at a later moment) flexible and low-cost systems with simplicity by re-using the same basic (small) module without the need of costly connectors and cables.

We will provide three bi-directional links per board, so that the nodes can be connected in many different ways, ranging from ring, to the well-established 2D-mesh/torus, and up to arbitrary 3-D topologies such as mesh/torus. The AXIOM interconnect will have customizable parameters (such as packet size, formats, etc) if needed by applications, further improving the efficiency and performance.

In AXIOM we will provide a powerful network interface (NI) -implemented in the FPGA region- that will efficiently support the communication protocols needed by the applications. Besides implementing a MPI-like communication library, we will support a (distributed) Shared Memory model with support from the OmpSs programming model, the Operating System, and the Run-time. One such optimization is the efficient implementation of remote direct memory access (RDMA) and remote-write operations as basic communication primitives visible at the application level.

The AXIOM interconnection library will support two main packet types, (a) RDMA, and (b) short messages. RDMA packets will be used to (a) request large data from a remote node (RDMA requests), and (b) transmit large data (RDMA writes). Short messages will be used to exchange short data between nodes that will contain either raw data or acknowledgement packets (ACKs). Towards a balanced and efficient bandwidth network utilization, we employ a packet priority transmission scheme; ACKs, RDMA writes / messages, and RDMA requests are classified with the highest, middle and lowest transmission priority respectively.

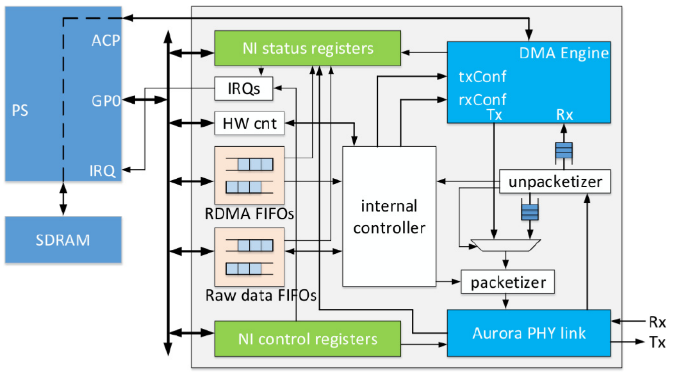

Fig. 7. The Network Interface controller structure.

Fig. 7 illustrates the NI internal structure for inter-node communication. The “RDMA FIFOs” will be used to store descriptors for sending / receiving RDMA packets to / from remote nodes. RDMA descriptors contain the local and remote node id, source and destination data address, and finally the payload size. The “Raw data FIFOs” will be used to store descriptors for exchanging either short data messages or ACKs. Such descriptors will contain the source and destination node id, and also encapsulate the payload data (raw data or an ACK).

The “NI control registers” are memory mapped registers that allow the local Zynq processing system (PS) to configure the NI PHY loopback mode or toggle local notifications when data are successfully transmitted. The “NI Status registers” are also memory mapped registers that allow the PS to monitor certain NI internal states, such as the DMA engine progress, queues status (empty, full, etc.), PHY channel and link states. In addition, when a FIFO state moves from empty to not empty the “IRQ” module raises an interrupt to inform the PS.

The hardware counters module (“HW cnt”) provides a set of counters to monitor the progress of RDMA requests and RDMA writes. Every new RDMA request / RDMA write that reads / writes a large set of data from / to a remote node, is essentially served by multiple short RDMA responses (packets that fetch subsets of the requested data). Moreover, each RDMA request / RDMA write gets a unique id that is assigned to a HW counter. The latter is set to the number of RDMA responses required to transmit all data; its value is decremented each time an RDMA response is finished. The PS can access all HW counters for debugging purposes via software.

The “DMA engine” is responsible for storing incoming payload / loading requested data to / from the required SDRAM address via the PS coherency port (ACP). The “Aurora PHY link” utilizes the Zynq MGT transceivers to serially send / receive data to / from remote nodes.

The “packetizer” assembles a complete packet that will be sent to a remote node; short messages and RDMA requests / RDMA writes are forwarded to the Aurora PHY link, while RDMA response headers are appended with the requested payload provided by the DMA engine. In contrast, the “unpacketizer” caches incoming packets. Simple messages / ACKs and RDMA response headers are eventually stored to the “Raw data FIFOs”. Trailing payload data from RDMA responses are forwarded to the DMA engine and stored to the SDRAM via the ACP, ensuring the PS data coherency.

Finally, the NI “internal controller” (NIC) orchestrates the overall module functionality.

4. Application domains and examples of use

AXIOM will be applied in two real life application domains: Video-surveillance and Smart-home. They will operate as benchmarks for assessing the potentialities and the limits of the proposed architecture. The two application domains have been chosen for the different kind of challenges to process capabilities they pose.

4.1. Video-surveillance

Intelligent multi-camera video surveillance is a multidisciplinary field related to computer vision, pattern recognition, signal processing, communication, embedded computing and image sensors. Smart video-surveillance has a wide variety of applications both in public and private environments, such as homeland security, crime prevention, facial marketing and traffic control, among others.

These applications are generally very computationally demanding, since they require monitoring very diverse indoor and outdoor scenes including airports, hotels or shopping malls, which usually involve highly varying environments. In many cases it is also necessary to analyze multiple camera video streams, particularly when object re-identification or tracking of individuals across cameras is required. For instance, a scenario where runners may be observed and recognized with different objectives: statistics, real-time detection of people that want to be video recorded during the race, TV reportage where the TV officer only has to say the name of a runner and the corresponding camera becomes operative, etc. Another crowded scenario may be the case of a large company with hundreds of employees that work in several different places/buildings: an employee A in any room requests videoconference with a person (in any place, any building) and AXIOM, in real-time, detects where this person is and requests permission to begin videoconference room-to-room by telling that person: “A is requesting a videoconference”. Real-time recognition may also help to track emergency vehicles to skip traffic jams by analyzing the traffic camera images in real-time.

The modular approach explored by AXIOM is particularly well-suited for tackling such challenging scenarios as it addresses the issues derived from their computational complexity, distributed nature, and need for synchronization among processes. Furthermore, the AXIOM platform makes it possible to execute compute intensive tasks on ARM with FPGA processing nodes. This will enable companies such as Herta Security to deploy their real-time face recognition technology in crowded and changeable environments using multiple cameras simultaneously.

4.2. Smart-home

Smart home means buildings empowered by ICT in the context of the merging Ubiquitous Computing and the Internet of Things: the generalization in instrumenting buildings with sensors, actuators, cyber-physical systems allow to collect, filter and produce more and more information locally, to be further consolidated and managed globally according to business functions and services. A smart home is one that uses operational and IT technologies and processes to make it a better performing building - one that delivers lower operating costs, uses less energy, maximizes system and equipment lifetime value, is cyber-secured and produces measurable value for multiple stake holders.

Major challenges in such environments concern cryptography, self-testing and first of all sensor-networks management. Sensor data brings numerous computational challenges in the context of data collection, storage, and mining. In particular, learning from data produced from a sensor network poses several issues: sensors are distributed; they produce a continuous flow of data, eventually at high speeds; they act in dynamic, time-changing environments; the number of sensors can be very large and dynamic. These issues require the design of efficient solutions for processing data produced by sensor-networks.

AXIOM can help with preventive and interactive maintenance of infrastructures, climate and temperature management. This management can be remotely controlled helping to improve the energy efficiency at home, apartments and company office buildings. For instance, AXIOM may detect patterns of behavior in a company office building to adapt climate and light switching to the working way of life of the workers.

The two application domains pose also common challenges such as, board-to-board communication and easy programmability. Furthermore, the two scenarios shown can easily converge, offering opportunities for synergies and emerging services in the respective domains.

4.3. Examples of use

We are currently considering a wide range of potential uses both for Video-surveillance and for Smart-home. They range from dynamic retail demand forecasting in train/bus station to Smart Marketing in shopping malls for Video-surveillance; and from Smart home comfort to Autonomous drone for infrastructure and smart-home control. Here a taste of the scenarios, where the goals are expressed in terms of the final users of the enabling technology is showed. A discussion of another scenario, part of our scenario exploration, related to vehicle detection can also be found in another paper [11]. At the same time, these goals should match with the challenges to AXIOM processing capabilities:

- Dynamic retail demand forecasting. Due to the high fluctuation of passengers departing and arriving at train stations, demand for station retailers varies strongly over time. By forecasting such demand through video analysis, better services can be provided through more efficient staff utilization. The purpose of this scenario is to provide retailers with a real-time forecast of potential customers arriving at their outlets, to allow for better task allocation and to increase business efficiency.
- Smart marketing in shopping mall. Consumer behavior in a shopping mall can be very eclectic yet the awareness of patterns of behavior can be of help both to services providers and to clients to meet their respective goals. Demographic analyses is carried out over the captured facial snapshots, helping to identify interesting facts such as the demographic profiles of the customers, or how do they distribute into gender and age segments. The visitors are tracked from one camera to another, so as to discover the main paths they take through the mall and how long they stay at different locations. The goal is to collect statistical information about the visitors in order to define marketing strategies both for service providers and for clients.
- Smart home comfort. Comfort perception and necessities can be different in respect of time of the day/week and to the characteristics of the people actually living that space in that moment. The smart home is required to identify and manage the different situations, and to react at the people indications in an easy and smooth way. Networked sensors and actuators are distributed in each room embedded in ordinary appliances. The appliances perform their primary normal function, but also collect different kinds of information, ranging from presence detection, temperature, humidity, window and door opening, air quality, audio. The objective of the smart home comfort autopilot is to minimize power consumption and to guarantee people’s comfort and well being, without giving the impression of reducing people freedom and capacity of control.
- Autonomous rover/drone for infrastructure control. Preventive maintenance is performed on equipment to keep it running smoothly and efficiently and to help extend its life. Many types

of equipment should be put on a preventive maintenance program: HVAC systems, pumps and air compressors, air conditioning, chillers and absorption equipment, elevators, safety showers, back-flow preventers, building exteriors, roofs, windows, fire doors and generators. Autonomous rovers and drone furnished with thermo camera and ambient sensors can move inside and outside a building monitoring the energy flow, providing data for a multi-level energy flow models that can be used for preventive maintenance. The goal is maintaining building infrastructure efficient, manage operating costs, and minimizing potential downtime. It also ensures these components perform within their originally designed operating parameters, allowing data center managers the opportunity to replace components before they fail.

The software approach explored by AXIOM is particularly well-suited for tackling such challenging scenarios, as it addresses the issues derived from their computational complexity, distributed nature, and need for synchronization among processes. Moreover, we are considering some representative benchmarks to test drive the design of the software stack that two partners already explored in the ERA project [12,13].

Finally, it is worth mentioning that this project doesn't address the problem of maintaining or securing "sensible" data. In principle AXIOM is not collecting sensitive information, as per the definition of sensitive information provided by EU Directive 95/46/EC. However, according to the approved Commission Proposals on the data protection reform, biometric data has to be considered sensitive by default. This Regulation shall apply from 25 May 2018 but the project considers since the beginning that biometric data collected deserve that highest protection, at the same level of data revealing racial or ethnic origin, political opinions, religious or philosophical beliefs. Accordingly, procedures compliant with national and EU legislation are followed to deal with data collection, storage, protection, retention and destruction and confirmation.

Regarding the software developed in the presented scenarios, it will rely on the Linux OS security layers already developed. As a full Linux compliant architecture, the AXIOM architecture supports the technical means to guarantee different privacy levels to protect the access to "sensible" plain data. Of course, it will also be archived and distributed following national and EU legislation.

5. Experimental setup

In the first year of the AXIOM project we want to properly evaluate the potential of the proposed hardware/software platform to achieve the following goals:

- Easy programmability of multi-core, multi-board, FPGA nodes using the OmpSs programming model.
- Reasonable performance and improved energy efficiency compared against state-of-the-art systems.

5.1. Benchmarks description

Three benchmarks have been used for the analysis of easy programmability when using the OmpSs@FPGA infrastructure: (1) Cholesky matrix decomposition, working on a dense matrix of 64x64 double-precision complex numbers; (2) Covariance, working on arrays of 32-bit integer complex numbers; and (3) Matrix multiplication, working on a matrix of single precision floating point values (32×32 and 64×64 sizes). On the order hand, for performance results the same matrix multiplication has been used with a larger matrix 2048×2048, and different block sizes.

Table 1
Total number of *additional* lines of code compared to a baseline C implementation.

Application	*Pthread*	*Accel*	*OmpSs*
`Cholesky`	26	71	3
`Covariance`	29	94	3
`MxM 64x64`	39	95	3
`MxM 32x32`	39	95	3

5.2. Hardware and software

To perform the FPGA experiments showed in this article we have used a Zynq 706 board. The board includes a Zynq 7045 with 2 ARM cores running at 800MHz and an FPGA that run at 200MHz and features 350K logic cells, 19.1Mb of block RAM and 900 DSP slices. The SoC was released at 2012 and used 28nm technology. Timing of the applications has been obtained by instrumenting with `gettimeofday` the part of the code that calls several times the kernel code while the power consumption was computed using the tools provided by Xilinx.

The OmpSs implementation is based on Mercurium 1.99.4 and Nanos++ 0.8. For the hardware compilation branch we have used the Xilinx ISE Design 14.7 and the Vivado HLS 2013.2 tools. The `#pragma HLS pipeline II=1` was used to parallelize the second loop of the matrix multiplication. All OmpSs codes have been compiled with the arm-xilinx-linux-gnueabi-g++ (Sourcery CodeBench Lite 2011.09–50) 4.6.1 and arm-xilinx-linux-gnueabi-gcc (Sourcery CodeBench Lite 2011.09–50) 4.6.1 compilers, with `-O3` optimization flag. OmpSs runtime used an AXIOM premilinary prototype of the NI interface. Results show the average elapsed execution time of 3 application executions.

The machine used to obtain the GPP reference results was an i5-3470 with 4 cores running at 3.20GHz. The processor was selected as it was released in Q2'12, close to the releasing time of the Zynq 7045, and uses a 22nm technology. As with the ARM codes, timing was measured with `gettimeofday` and power was measured reading directly the processor hardware registers. Codes were compiled with gcc version 5.2.1 using `-O3` optimization flag and MKL version 11.2.3.

6. Results

We have done some experiments for coding a set of benchmarks in the Zynq platform and an initial evaluation of programmability cost in terms of number of lines of code, as a measure of programmability complexity.

6.1. Programmability analysis

In order to have a good programmability analysis we have implemented four different versions of each benchmark code: sequential code, pthread code, FPGA-accelerated code and OmpSs code. All versions of the codes consider the full Matrix Multiply, the full Cholesky, and the full Covariance as tasks.

We want to remark the programmability facilities of our proposal. With this objective, Table 1 shows the total number of *additional* lines of code for each of the different versions of the applications, compared to the sequential version: a pthread version *only* running tasks in one or two ARM cores (`Pthread`), a sequential version using one or two hardware accelerators (`Accel`), and the OmpSs version (`OmpSs`).

The Pthread and Accel versions require more *additional* lines than the OmpSs version. This is especially high in the sequential versions using the hardware accelerators. For the Pthread version this is due to the additional calls to the Pthreads library, in order

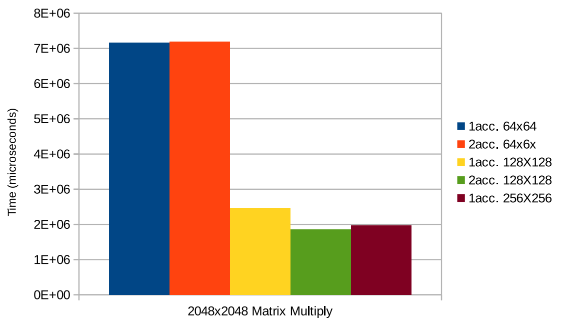

Fig. 8. Elapsed-time: 1/2 FPGA accelerators, up to 256 × 256.

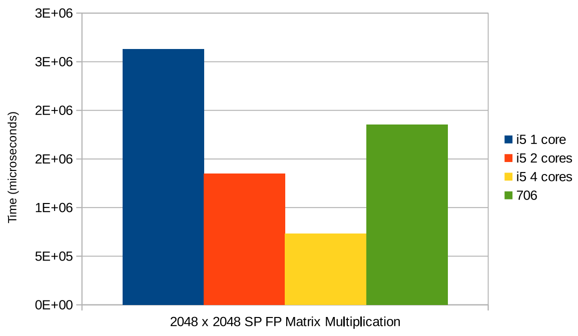

Fig. 9. Elapsed-time: FPGA MxM versus SMP MxM (MKL).

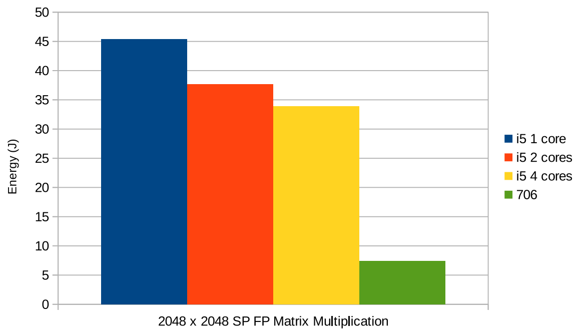

Fig. 10. Energy consumption: FPGA MxM versus SMP MxM (MKL).

to create, manage and join the pthreads. For the Accel version, this is because the application needs to call the low-level infrastructure to setup the communications layer with the FPGA and perform the actual data transfers back and forth to the FPGA hardware.

On the other hand, in the case of the OmpSs version, the thread management, the setup of the communications and data transfers to and from the FPGA are all done internally by the Nanos++ runtime. This way, the programmer does not need to write any line of code related to low level management, but only the directives triggering the communications.

Indeed, the current compilation and runtime infrastructure of the OmpSs programming model allows to exploit the heterogeneous characteristics of the Zynq All-Programmable SoC with the only effort of two directive lines. Note however that Table 1 indicates that the OmpSs version needs an additional third line. This line is a `taskwait` before the program ends, as it can be observed in Fig. 5. Actually, the code showed in Fig. 5 is used to generate both the 32 × 32 and the 64 × 64 versions of the matrix multiplication, using all the available resources (ARM cores and FPGA), simply by redefining the BS variable as 32 or 64 elements.

For the Pthreads and Accel versions however, different block sizes need new scheduling schemes, adding more complexity to the transformation of the code. Indeed, implementing a fourth version of the code managing heterogeneous executions would require more development time and additional lines that the ones showed in Table 1.

6.2. Performance results

In order to study the suitability of our approach to the High Performance Computing (HPC) environment, it is necessary to demonstrate that our systems is not only able to be easily programmed but also that it can achieve a reasonable performance when compared to other current state-of-the-art approaches.

First, an evaluation of the best accelerator size for the selected FPGA was performed. Fig. 8 shows the elapsed time for a 2048 × 2048 matrix multiplication using 1/2 accelerators of sizes (blocks) 64 × 64, 128 × 128 and 256 × 256. Results show that using 1/2 64 × 64 accelerators are the worst choice. This accelerator size is too small for the problem since the data transfer to/from the FPGA overcomes the computational benefits of using the FPGA. Indeed, as the communication channel is shared, using two accelerators does not improve the performance that is bounded by the DMA. On the other hand, there is a significant improvement when moving to 128 × 128 accelerators. Those bigger accelerators compute blocks of four times the size of 64 × 64 accelerators and consequently the data movements are divided by four. Therefore, 128 × 128 accelerators are also 8 times more time consuming than 64 × 64 accelerators since doubling the block size means eight times more multiplications, and then, using two accelerators can help to improve the performance. However, due to FPGA limited resources, the compiler is not able to make the two accelerators, sharing resources, as fast as only one, using all the resources. This limit explains why the largest accelerator (blocks of 256 × 256) is not able to be as fast as two 128 × 128 ones. Although the data transfers are again divided by four the accelerator is six times slower than one 128 × 128 due to the limited resources and this results in a worse overall performance. One not so obious, but nevertheless important result of Fig. 8 is that all the accelerators were compiled and executed using the same source code (listed in Fig. 5) changing only the block size (BS). Both the compiler and the runtime take care of all the details.

Fig. 9 shows the time in microseconds that takes to compute a 2048 × 2048 matrix multiplication, using the best block size, in two different systems. Columns named i5 show the time used by the Corei5 machine described in Section 5.2 when using 1, 2 and 4 cores respectively with the `sgemm` function of the MKL library. Column 706 shows the time used by the same computation when it is performed in a Zynq 706 board using the code showed in Fig. 5 and the OmpSs compilation and execution framework. As it can be seen the FPGA board is competitive with the conventional SMP with a result between 1 and 2 Corei5 cores in performance terms. Fig. 10 shows the energy consumption of the same computation in the same machines. As it shows the FPGA system clearly outperforms the conventional SMPs in terms of energy consumption which shows that our approach is promising for future computing systems.

What is more important from the results showed in Figs. 9 and 10 is not that an FPGA of an older technology process can clearly outperform in terms of energy a conventional processor but the fact that writing the code for the FPGA was actually simpler than writing the code for the SMP. Indeed, as mentioned above the FPGA code was directly the one showed in Fig. 5 while the SMP code was changed to call the parallel `sgemm` version of the MKL library instead of the original matrix multiply function. So, OmpSs was not used for the Core i5 version. Arguably, the change was not cumbersome neither extensive but the fact is that the naive original version of the MxM code, although compiled with the `-O3` optimization flag, performed much (36 × slowdown) worse than the MKL `sgemm` implementation forcing us to change the code to provide a fair evaluation. In our opinion this highlights the potential of using the OmpSs programming model for heterogeneous systems.

7. Related work

The AXIOM project will exploit the OmpSs dataflow features in the AXIOM heterogeneous architecture. OmpSs is the result of the integration of StarSs [14] and OpenMP.

In this section we discuss some work that has been fundamental for the development of this project and provided the necessary inspiration and vision to develop some basic concepts related to the dataflow execution model. Dataflow execution model had been studied since long time ago [15] as they provide a simple an elegant way to efficiently move data from one computational thread to another one [16,17]. In the context of the TERAFLUX project [9,18] such dataflow model had been extended to multiple nodes executing seamlessly thanks to the support of an appropriate memory model [7,10]. In such memory model a combination of consumer-producer patterns [8,19] and transactional memory [20,21] permits a novel combination of dataflow concepts and transactions in order to address the consistency across nodes, where each node is assumed to be cache-coherent, i.e., like in a classical multi-core. Dataflow models also allow the system to take care in a distributed way of faults that may compromise a node [22,23].

In order to integrate heterogeneous execution of the same applications over processors and FPGA fabric, OmpSs@FPGA is a key point in the project. Although to the best of our knowledge OmpSs@FPGA [24, 25] is the first successful attempt to implement hardware accelerators from high-level directives in a total transparent way, other approaches have been used in the past. Some tools try to reduce the FPGA programmability problem by offering the possibility of generating HDL code from C or C-like languages like ROCCC [26,27] or generating systems with an embedded soft processor connected to the generated hardware accelerators like LegUp [28] and C2H tool [29]. However, with the new SMP/FPGA SoCs, new strategies are required in order to exploit those current heterogeneous *and* parallel platforms. Our ecosystem also covers runtime support for parallel execution of heterogeneous tasks on those SoCs, unlike other.

PGI [30] and HMPP [31] programming models are two other approaches quite related to OmpSs. PGI uses compiler technology to offload the execution of loops to the accelerators. HMPP also annotates functions as tasks to be offloaded to the accelerators. We think that OmpSs has higher potential in that it shifts part of the intelligence that HMPP and PGI delegate in the compiler to the OmpSs runtime system. Although these alternatives do support a fair amount of asynchronous computations expressed as futures or continuations, the level of lookahead they support is limited in practice.

To execute over several nodes, OmpSs@cluster [32] is one of the alternatives explored in the project. As alternatives, Partitioned Global Address Space (PGAS) programming models expose an abstracted shared address space to the programmer simplifying its task, while data and thread locality awareness is kept to enhance performance. Representative PGAS languages are UPC [33], and X10 [34]; and Chapel [35], which implement Asynchronous PGAS model, offering asynchronous parallelism. An alternative way to provide asynchronous parallelism on clusters is a hybrid programming model that composes SMPSs [36], that inspired OmpSs, with MPI. The main idea is to encapsulate the communications in tasks so they are executed when the data is ready. This technique achieves an asynchronous dataflow execution of both communication and computation.

OpenCL [37] attempts to unify the programming models for general-purpose multi-core architectures and the different types of hardware accelerators (Cell B.E., GPUs, FPGAs, DSPs, etc.). The participation of silicon vendors (e.g., Intel, IBM, NVIDIA, and AMD) in the definition of this open standard ensures portability, low-level access to the hardware, and supposedly high performance. We believe, however, that OpenCL still exposes much of the low-level details (i.e. explicit platform and context management, kernel special intrinsic functions, explicit program, kernel and data transfer management, etc.), making it cumbersome to use by non-experts.

Another alternative for mutli-node programming is DSM. DSM is a recently revived topic [38]. Some attempts for creating Software DSM implementations for Linux have been carried out during the last decades. Examples are Treadmarks (TMK), JIAJIA [39], Omni/SCASH [40,41], Jump [42,43], Parade [44,45], NanosDSM [46]. Some of these projects only supported very specific hardware, and none of them has been maintained during the last decade.

Regarding applications, state-of-the-art implementations of video-surveillance or voice-identification scenarios currently rely on machine learning techniques based on deep neural networks (DNNs). As recent studies have pointed out, DNNs are particularly good for addressing computer vision image classification and recognition problems exhibiting highly non-linear properties. Applications ranging from face recognition [47] and age/gender estimation [48] to pedestrian detection [49] have experienced dramatic improvements in terms of accuracy just by training DNNs with huge amounts of data. Due to the architectural properties of these models and the advances in HPC, it is now cost-effective to massively scale the infrastructure to train such networks with millions of sample images that have been previously manually tagged by humans on the widely-available social networking services.

The proliferation of frameworks and libraries such as Caffe [50] and cuDNN [51] have democratized the usage of parallelized DNN-based solutions on GPU architectures. However, there is a lack of ready-to-deploy implementations of DNN inference engines for embedded platforms powered by FPGA accelerators. Since DNN evaluation is highly parallel in nature, it is feasible to offload all the required SGEMM matrix multiply operations to FPGAs, and also to execute forward propagation in an efficient manner through the OmpSs programming model.

Once DNN models are trained as a result of a process that usually takes several days on a GPU cluster, it is then possible to evaluate them on the AXIOM board. With this idea in mind, we aim to produce a generic easy-to-use, low-power hardware/software stack to cheaply deploy machine learning solutions based on DNNs interacting with the Cyber-Physical world. This ecosystem powered by the AXIOM platform is expected to solve a myriad of computer vision problems, and thus dramatically improve productivity on a wide range of industries.

8. Conclusions and future work

In this paper, we have presented the software layers that we are developing on the AXIOM H2020 European Project. The main objective of the project is to bring to reality a novel small board which aims at becoming a very powerful basic brick of future interconnected and scalable embedded Cyber-physical systems, and specifically we focus on the application domains of Video-surveillance, deep learning and Smart-home. The module consists of both hardware and software that will be designed and demonstrated in the project.

On one hand, the target board architecture will be a board based on a SoC with several ARM cores and an FPGA, like the Xilinx Zynq, and with the Arduino interface to be extensible. The AX-

IOM system will comprise several of such boards linked through custom communication links, and providing application memory coherence at software level. On the other hand, we will research ways to easy programmability of the system, based on the OmpSs programming model and DSM-like techniques to achieve a global system image for applications. Currently, we are in the process of designing a high-speed communications layer between boards. These communication will be implemented using the transceivers available in the Zynq SoC. We have also started looking at the application requirements to ensure that our platform fits with their needs.

The expected impacts obtained from the AXIOM project include a platform interfacing with the physical world through compatibility with Arduino shields. This platform will be aimed to become the hardware and software platform for large scale production. In this sense we want to develop an autonomous technology that is able to break the Embedded Systems energy efficiency and programmability barriers. The same set of technologies are expected to represent the base for future European industrial exploitation in the HPC and Embedded Computing markets. Finally, it is expected to provide the basis for a new European-level research at the forefront of the development of extreme-performance system software and tools.

Our preliminary experiments have shown that the OmpSs programming model increases the expressiveness of serial or pthreads programming, thus allowing developers to focus on solving the issues related to the algorithms, instead of dealing with the low-level details of the communications among boards or data transfers between the cores and the embedded FPGA. Also we show that this easiness in programmability is joined by competitive performance and lower energy consumption when compared to standard processors.

The key features of the project presented in this paper are the possibility to modularly enhance the capabilities of the board, improve its interface with the physical world, flexibly reconfiguring it for accelerating specific functions, while providing energy efficiency and easy programmability.

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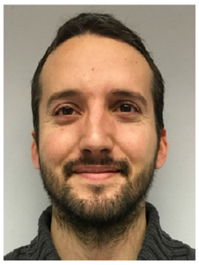

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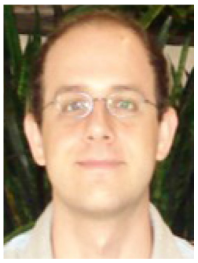

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