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Gate Stability of GaN-Based HEMTs with P-Type Gate

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Abstract: This paper reports on an extensive investigation of the gate stability of GaN-based High Electron Mobility Transistors with p-type gate submitted to forward gate stress. Based on combined electrical and electroluminescence measurements, we demonstrate the following results: (i) the catastrophic breakdown voltage of the gate diode is higher than 11 V at room temperature; (ii) in a step-stress experiment, the devices show a stable behavior up to V_{GS} = 10 V, and a catastrophic failure happened for higher voltages; (iii) failure consists in the creation of shunt paths under the gate, of which the position can be identified by electroluminescence (EL) measurements; (iv) the EL spectra emitted by the devices consists of a broad emission band, centered around 500–550 nm, related to the yellow-luminescence of GaN; and (v) when submitted to a constant voltage stress tests, the p-GaN gate can show a time-dependent failure, and the time to failure follows a Weibull distribution.

Keywords: gallium nitride; high electron mobility transistor; degradation; step stress

1. Introduction

Gallium nitride transistors have recently been demonstrated to be excellent devices for application in the power electronics field. Thanks to the high breakdown voltage of GaN (3.3 MV/cm), high electron mobility transistors (HEMTs) can reach breakdown voltages in excess of 1 kV; in addition, the high mobility of the electrons in the channel results in a low on-resistance. With regard to this last aspect, recent on-resistance values reported in the literature are 100 mΩ for a 20 A/650 V transistors [1], 70 mΩ for 600 V AlGaN/GaN devices with a 214 mm gate width [2], and a specific on-resistance of 2.3 mΩ cm^2 for normally-off devices with a gate-drain distance of 12 μm [3]. Finally, the wide bandgap of the semiconductor (3.4 eV) allows for high temperature operation.

The high electron density in the two-dimensional electron gas (2DEG) is obtained thanks to the spontaneous and piezoelectric polarization of GaN, without the need for any doping; typically, GaN-based transistors are normally-on devices, with a negative threshold voltage. Several methods have been recently proposed for the fabrication of normally-off GaN-based transistors: the use of a deep gate recess, in combination with a metal-insulator-semiconductor (MIS) stack [4]; the implantation of fluorine ions under the gate [5], that results in a significant depletion of the channel; the use of a p-type gate material, such as p-AlGaN [6] or p-GaN [7], which shifts the conduction band upwards, thus resulting in the depletion of the channel for negative gate voltages. As an alternative to these strategies,

it has been also proposed to develop special E-mode devices, integrating a normally-on GaN HEMT connected in cascode configuration to a normally-off silicon MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in the same package [8]. In this last approach, the on/off state of the low-voltage silicon MOSFET controls the on/off state of the GaN-based high voltage HEMT; the cascoded device behaves then as an enhancement device, which is compatible with commercial drivers. All of these approaches have advantages and drawbacks: the use of a gate recess with gate insulator leads to a very low gate leakage current, but can favor trapping at the interfaces and/or in the insulator, as well as time-dependent dielectric breakdown; fluorine implantation allows to obtain high (positive) threshold voltages (>2 V, [9]), but the fluorine ions (and the threshold voltage) can be unstable if the devices are submitted to long-term stress [10]); the use of a p-type gate requires the optimization and activation of the p-type dopant (magnesium), *i.e.*, an additional growth step; finally, cascoded HEMTs are rather complex structures, having two devices mounted on the same package. This can generate reliability problems, due to the use of extra bonding wires, and to the fact that a silicon-based transistor is used in proximity of a GaN HEMT that—in principle—can operate at high temperatures.

Several reports on the reliability of MIS-based devices and normally-on HEMTs have already been published in the literature (see, for instance, [11,12] and references therein). On the other hand, only little information on the stability of HEMTs with a p-gate is currently available [13,14].

The aim of this paper is to contribute to the understanding of the physical mechanisms responsible for the failure of GaN-based HEMTs with p-GaN gate submitted to positive bias stress. We present our recent results on the degradation of transistors with a p-GaN gate submitted to stress with positive gate voltage. The results of our investigation indicate that the analyzed devices have a (positive) breakdown voltage higher than 11 V at room temperature, and can show a catastrophic failure when they are submitted to a step-stress experiment. Information on the nature of the failure mechanism is provided based on spatially- and spectrally-resolved electroluminescence (EL) measurements and on optical characterization. Finally, we demonstrate the existence of a time-dependent breakdown process in positively-biased devices with p-GaN gate.

2. Materials and Methods

The analysis was carried out on HEMTs with p-GaN gate, whose structure is schematically represented in Figure 1. The devices were grown by metal-organic chemical vapour deposition on a 200 mm silicon substrate; the epitaxial structure consists of a 200 nm AlN nucleation layer, a 1 μm AlGaN backbarrier, a 2 μm AlGaN buffer layer, a 300 nm GaN channel layer, a 15 nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 70 nm p-GaN layer. This study is aimed at investigating the stability and degradation of the p-GaN gate under positive bias conditions. All the measurements were carried out on symmetric tests structures without field plate, that allow to observe the gate from the top during the execution of the electroluminescence measurements. The gate width is W_G = 100 μm, and the gate length is L_G = 0.8 μm. The electrical measurements were carried out in a probe station equipped with a semiconductor parameter analyzer (Keysight B1505). The electroluminescence characterization was carried out by means of a high-sensitivity Si-based camera (Luca Andor, UK), mounted on an optical microscope with visible-ultraviolet lenses (Mitutoyo, Japan); the synchronization between the electrical stimulus and the camera was obtained through a customized LabView® software (LabView 2009, National Instruments, USA).

The electrical characteristics measured on a representative device are plotted in Figure 2; the threshold voltage is V_{TH} = 1.7 V (at 100 μA/mm, V_{DS} = 1 V), and at higher drain voltages remains well above 1 V (V_{TH} = 1.32 V at 100 μA/mm, V_{DS} = 10 V).

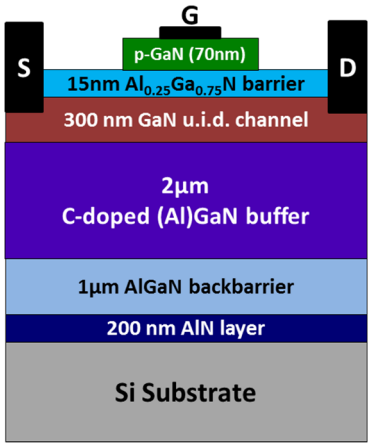

Figure 1. Schematic structure of the samples analyzed within this paper.

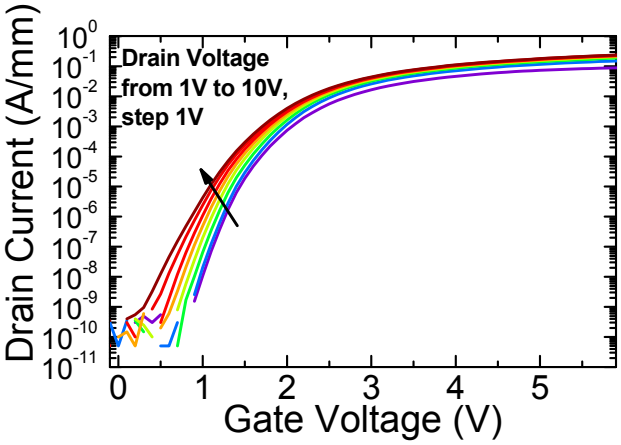

Figure 2. Drain current vs gate voltage curves measured on one of the analyzed devices for different drain voltages.

3. Results

Before starting with the stress experiments, the devices were preliminary submitted to a breakdown stress. The gate voltage was rapidly swept from 0 V to 15 V, and the corresponding gate current was monitored. During the measurement, the drain, source and chuck were grounded. Representative results obtained on four identical samples are reported in Figure 3. As can be noticed, the gate current is negligible and below instrument sensitivity (around 100 pA/mm) up to a gate voltage of 8 V (the gate voltage swing of these devices is 6 V). For gate voltages between 8 V and 11 V, gate current shows an exponential increase, reaching values in the order of 100 nA/mm. For higher voltages, the devices reach the forward gate breakdown, that corresponds to a rapid increase in gate leakage. This degradation is permanent (*i.e.*, not recoverable), and—once the devices have reached the breakdown—the gate current is around 10–100 mA/mm for voltages higher than 12 V.

In a dc breakdown test, the device fails rapidly, so it is impossible to investigate the physical origin of the degradation. To obtain a better description of the degradation process, we carried out a series of step-stress experiments: the stress voltage applied to the gate was increased by 0.5 V every 120 s, with source, drain and chuck grounded. The gate current was constantly monitored during stress, together with the electroluminescence signal emitted by the devices.

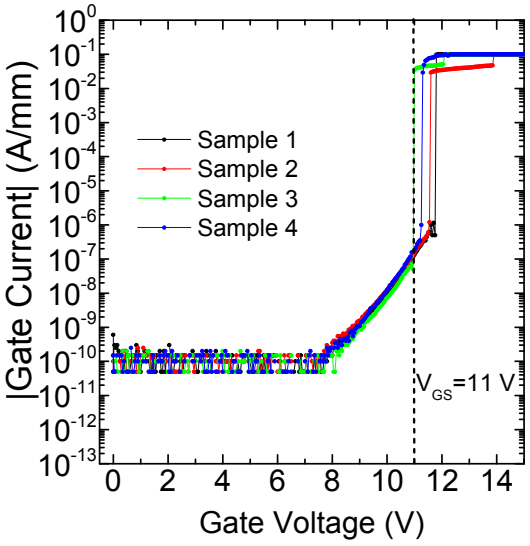

Figure 3. Forward-voltage breakdown curves measured on 4 representative devices.

The results obtained on one of the analyzed samples are reported in Figure 4. Gate current remains below the instrumentation limit up to a stress voltage of V_{GS} = 7.0 V. During the subsequent steps (for 7.5 V < V_{GS} < 9.5 V), the gate current slightly increases during each stage of the step-stress experiment. The failure is reached during the step at V_{GS} = 10 V; after an initial phase in which current increases slowly with time, gate leakage shows a rapid increase and reaches the compliance limit.

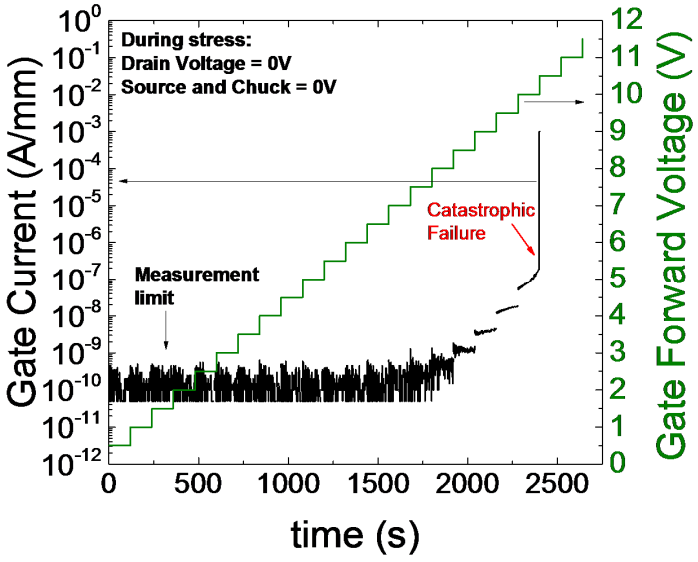

Figure 4. Results of a step-stress experiment carried out on one of the analyzed devices. With drain and source grounded, the gate voltage is increased by 0.5 V every 120 s. The corresponding gate current is sampled every second.

The spatially-resolved electroluminescence measurements carried out before and during the step-stress experiment showed negligible light emission up to V_{GS} = 9 V (Figure 5a); this result is consistent with the very low gate leakage detected in this voltage range. Remarkably, during the step at V_{GS} = 10 V a weak luminescence signal was detected (Figure 5b). Under these conditions light emission is focused in proximity of three localized regions, and stronger in the area indicated by the white arrow in Figure 5b. After failure (and after the corresponding increase in gate leakage), forward

current flows mostly in a localized area located in proximity of the dominant emission spot identified before failure (compare Figure 5b,c).

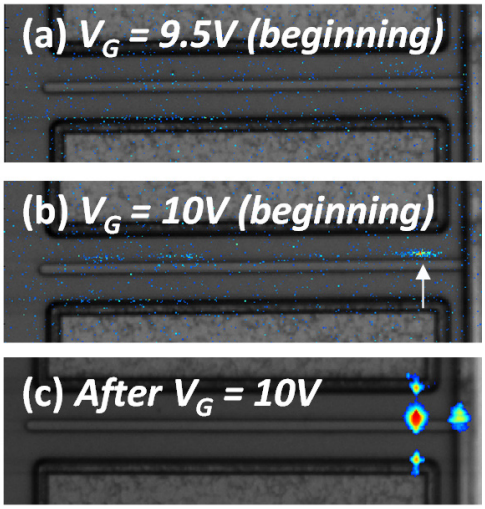

Figure 5. Spatially-resolved electroluminescence measurements carried out along the gate of the analyzed devices (**a**) at the beginning of the stress at V_{GS} = 9.5 V, (**b**) at the beginning of the stress at V_{GS} = 10 V and (**c**) after the catastrophic failure**.**

More detailed data on the origin of the luminescence signal were collected by means of spectrally-resolved electroluminescence measurements. The EL spectra were measured on the same sample of Figure 5 (after stress) by applying a constant gate current of 1 mA to the gate of the devices. The measurements were carried out by means of a high sensitivity cooled CCD (charge-coupled device) camera equipped with a monochromator. Figure 6 reports the EL spectra emitted by the same sample as in Figure 5. The device emits a broad luminescence peak centered around 500–550 nm. The origin of luminescence can be explained by considering that—under high forward bias—a high current of energetic electrons flows through the p-GaN/i-AlGaN junction. The flow of highly energetic electrons can induce the ionization of the deep levels responsible for the yellow luminescence of GaN (consistently with [13,15,16]). It is worth noticing that the gate voltage of the devices remains stable during the whole duration of the EL spectral measurements (see Figure 6), demonstrating that the spectral measurement does not induce any further degradation.

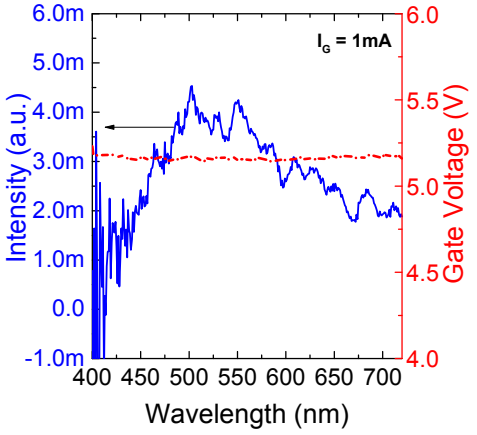

Figure 6. EL (electroluminescence) spectra evaluated from λ = 400 nm to λ = 720 nm on the same device as Figure 5 after the stepstress. The gate voltage measured during the acquisition of each wavelength is also reported.

The results collected during the last stage of the stress step experiment in Figure 4 indicate that the catastrophic degradation does not occur immediately after the stress is applied, but after several seconds of operation at V_{GS} = 10 V. This result suggests that the devices show a time-dependent failure. To better investigate this aspect, we carried out a set of constant voltage stress tests at voltages close to (but smaller than) the dc breakdown voltage. Figure 7 reports the results obtained by stressing identical samples with a gate voltage of 9.75 V, and source, drain, and chuck grounded. As can be noticed, in the initial phase of the stress experiment the gate current is very low and stable; this phase is followed by a gradual increase in gate leakage, that—for most of the samples—changes of 2–3 orders of magnitude. Failure occurs as a sudden increase in gate leakage (reaching the compliance value of 10 mA/mm).

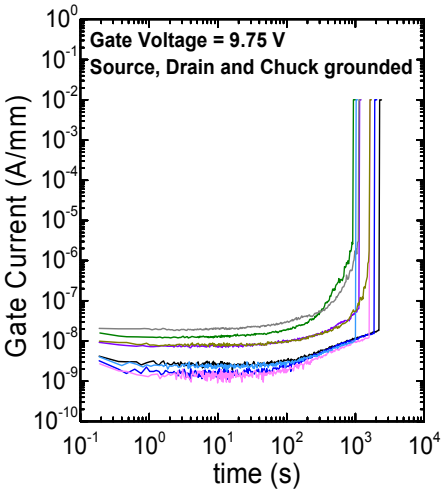

Figure 7. Results of constant voltage stress tests carried out on eight identical devices with a gate bias of 9.75 V, source, drain and substrate connected to ground.

The time-to-failure was found to follow a Weibull distribution (Figure 8), with a shape factor β of 2.25 (indicating that the failure rate increases with time) and a scale parameter (time at which 63.2% of samples failed) η of 1454 s. The time to failure is supposed to become shorter with increasing stress voltages. By analyzing the mean time to failure during stress at different voltage levels, we estimated that the devices have a twenty-years lifetime for a gate voltage of 7.2 V; this value is significantly higher than the typical gate operating voltage (5 V).

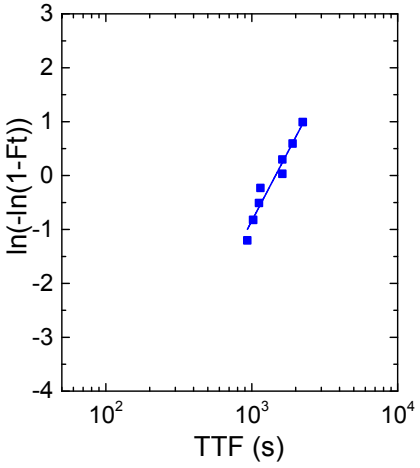

Figure 8. Weibull distribution of time-to-failure for the analyzed devices. β = 2.25, η = 1454 s.

The time-dependent failure process described above can be interpreted based on the following considerations. In reverse-biased Schottky junctions, the time-dependent failure has been ascribed to the degradation of the AlGaN layer, that is subject to a high electric field [15,17]. However, the devices analyzed within this paper are submitted to a positive gate bias, and 2D simulations [13] demonstrate that the absolute value of the electric field in the AlGaN decreases significantly during stress, with respect to rest conditions. The observed failure can therefore not be ascribed to the degradation of the AlGaN barrier.

Two other mechanisms can therefore be considered:

(i) at high (positive) gate bias, the electric field in the p-GaN can significantly increase (see the simulations in [13]), since the Schottky metal/p-GaN diode is reversely biased and the p-GaN is partly depleted. The high electric field can favor the generation of defects in the p-GaN, similarly to what observed in the AlGaN barrier under negative bias [15,18,19]. This may lead the generation of leakage paths and to the consequent failure of the gate junction. Avalanche effects (proposed in [13]) can further accelerate the defect generation process.

(ii) during positive voltage stress the SiN passivation may be exposed to a high electric field, especially in proximity of the gate edge. This may lead to a time-dependent (and geometry-dependent) dielectric failure of SiN, with consequent increase in gate leakage.

4. Conclusions

In summary, in this paper we have described an analysis of the degradation mechanisms of GaN-HEMTs with p-type gate submitted to positive bias stress. The results demonstrate that in the operating voltage range (up to 7 V) the devices have an high robustness towards stress. In addition, based on the results of dc breakdown measurements, step-stress experiment and constant voltage tests, we demonstrated that the transistors can show a time-dependent failure when submitted to forward gate stress at higher voltages (V_{GS} > 9 V). The failure corresponds to an increase in gate leakage, that is well correlated to the generation of hot-spots, identified by means of EL measurements. Possible mechanisms responsible for this failure have been discussed based on the experimental evidence collected within this paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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