Design Techniques of Energy Efficient PLL for Enhanced Noise and Lock Performance

Dissertation submitted in partial fulfillment of

the requirements for the award of

Doctor of Philosophy

by

Umakanta Nanda

Under the supervision of

Prof. (Dr.) D. P. Acharya

Prof. (Dr.) S. K. Patra

Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela - 769008, India

April 2016

Design Techniques of Energy Efficient PLL for Enhanced Noise and Lock Performance

A dissertation submitted to the department of

Electronics and Communication Engineering

of

National Institute of Technology Rourkela

in partial fulfilment of the requirements

for the degree of

Doctor of Philosophy

by

Umakanta Nanda

(Roll No- 511EC101)

under the supervision of

Prof. (Dr.) Debiprasad Priyabrata Acharya

and

Prof. (Dr.) Sarat Kumar Patra

Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela - 769008, India
April 2016

Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela - 769 008, India. www.nitrkl.ac.in

Certificate of Approval

Certified that the thesis entitled ***"Design Techniques of Energy Efficient PLL for Enhanced Noise and Lock Performance "*** submitted by ***Umakanta Nanda***, bearing **Roll No: 511EC101** to National Institute of Technology, Rourkela, for award of the degree of Doctor of Philosophy has been accepted by the external examiners and that the student has successfully defended the thesis in the viva-voce examination held today.

Prof. K K Mahapatra Member DSC	Prof. P M Khilar Member DSC	Prof. S. Das Member DSC
Prof. S K Patra Co-Supervisor		Prof. D P Acharya Supervisor
External Examiner		Prof. S Meher Chairman DSC

Department of Electronics and Communication Engineering
National Institute of Technology Rourkela
Rourkela - 769 008, India. www.nitrkl.ac.in

Dr. Debiprasad Priyabrata Acharya
Associate Professor
Dr. Sarat Kumar Patra
Professor

May 12, 2016

Certificate

This is to certify that this work in the thesis entitled ***"Design Techniques of Energy Efficient PLL for Enhanced Noise and Lock Performance"*** by ***Umakanta Nanda***, bearing **Roll No: 511EC101**, is a record of original research work carried out by him under our supervision and guidance in partial fulfillment of the requirements for the award of the degree of *Doctor of Philosophy* in *Electronics and Communication Engineering*. Neither this thesis nor any part of it has been submitted for any degree or academic award elsewhere.

(Sarat Kumar Patra) ***(Debiprasad Priyabrata Acharya)***

Declaration

I certify that,

a) The work contained in the thesis is original and has been done by myself under the general supervision of my supervisor and cosupervisor.

b) The work has not been submitted to any other Institute for any degree or diploma.

c) I have followed the guidelines provided by the Institute in writing the thesis.

d) I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.

e) Whenever I have used materials (data, theoretical analysis, and text) from other sources, I have given due credit to them by citing them in the text of the thesis and giving their details in the references.

f) Whenever I have quoted written materials from other sources, I have put them under quotation marks and given due credit to the sources by citing them and giving required details in the references

Signature of the student

Dedicated to my parents

Acknowledgment

I take the opportunity to express my reverence to my supervisors Prof.(Dr.) D. P. Acharya and Prof.(Dr.) S. K. Patra for their guidance, inspiration and innovative technical discussions all during the course of this work. I find words inadequate to thank them for enabling me to complete this work in spite of all obstacles. I am also thankful to all faculty members and research students of ECE Department, NIT Rourkela. Special thanks go to Prof.(Dr.) S. Meher, and Prof.(Dr.) K. K. Mohapatra for their constructive criticism and motivation during the course of my work. I am also thankful to Prof. (Dr.) Susmita Das and Prof (Dr.) P. M. Khilar for their valuable suggestions throughout my research time.

I am thankful to Prof.A.K.Swain, Prof. (Dr.) A.K.Sahoo and Prof. (Dr.) S. K. Das for their support and help at times of need. Its my pleasure to show my indebtedness to my friends at NIT like Prakash, Debashis, Pallab, Nihar, Sanand, Jagannath, Tom, Sudheendra, Srinivas, for their help during the course of this work. I find words inadequate to express any form of acknowledgment to my wife, brother and sisters who have been supporting me throughout my PhD career.

Umakanta Nanda

Abstract

Phase locked loops (PLLs) are vital building blocks of communication systems whose performance dictates the quality of communication. The design of PLL to offer superior performance is the prime objective of this research. It is desirable for the PLL to have fast locking, low noise, low reference spur, wide lock range, low power consumption consuming less silicon area. To achieve these performance parameters simultaneously in a PLL being a challenging task is taken up as a scope of the present work. A comprehensive study of the performance linked PLL components along with their design challenges is made in this report.

The phase noise which is directly related to the dead zone of the PLL is minimized using an efficient phase frequency detector (PFD) in this thesis. Here a voltage variable delay element is inserted in the reset path of the PFD to reduce the dead zone.

An adaptive PFD architecture is also proposed to have a low noise and fast PLL simultaneously. In this work, before locking a fast PFD and in the locked state a low noise PFD operates to dictate the phase difference of the reference and feedback signals.

To reduce the reference spur, a novel charge pump architecture is proposed which eventually reduces the lock time up to a great extent. In this charge pump a single current source is employed to reduce the output current mismatch and transmission gates are used to reduce the non ideal effects.

Besides this, the fabrication process variations have a predominant effect on the PLL performance, which is directly linked to the locking capability. This necessitates a manufacturing process variation tolerant design of the PLL. In this work an efficient multi-objective optimization method is also applied to attain multiple optimal performance objectives. The major performances under consideration are lock time, phase noise, lock range and power consumption.

Keywords: Phase locked loop (PLL), phase frequency detector, charge pump, loop filter, voltage controlled oscillator (VCO), frequency divider, lock in time, lock range, phase noise, power consumption, reference spur, dead zone, delay element, dual PFD, adaptive frequency calibration technique.

Contents

List of Acronyms/Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
PLL	Phase Locked Loop
CSVCO	Current Starved Voltage Controlled Oscillator
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
IDEA	Infeasibility Driven Evolusionary Algorithm
VCO	Voltage Controlled Oscillator
PFD	Phase Frequency Detector
LPF	Low Pass Filter
CP	Charge Pump
VVDE	Variable Voltage Delay Element
ADCC	Adaptive Duty Cycle Control
PED	Phase Error Detector
AFC	Adaptive Frequency Calibration
FED	Frequency Error Detector
CPPLL	Charge Pump Phase Locked Loop
RF	Radio Frequency
FOM	Figure Of Merit
TGCP	Transmission Gate Charge Pump
Op-Amp	Operational Amplifier

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

Phase locked loops (PLLs) are widely used in communication systems. With the continuous rise in demand for high performance, portable communication devices, CMOS integrated circuit designs of PLL for different applications is a challenge for circuit designers in industry. Areas for use of PLLs include line synchronization and color sub-carrier recovery in TV receivers, local oscillators, FM and PM demodulators in radio receivers, frequency synthesizers in transceivers and signal generators. The basic PLL operation is simple, however a detailed design of PLL circuit for a required application often needs a great level of understanding of the underlying principles of circuit properties, operation, and associated limitations. Besides this, the mixed signal behavior of the PLL puts further criticality for design in view of noise, locking capability and power consumption.

A clock signal, mostly derived from PLL is required in most of the electronic systems. With the clock speed in communication systems pushing into the GHz range, the key issues in analog designs, phase noise and jitter are becoming

increasingly critical. Besides this, PLLs are desired to lock faster over a wide range of frequencies consuming minimum power.

Power dissipated by PLLs is often a small fraction of total active power. However, during sleep modes where the PLL must remain in lock, this can be a significant fraction of dissipated power. For some applications such as high speed, parallel links and distributed synchronous clocking, where multiple PLLs are employed to minimize the timing uncertainty, makes the low-power and low jitter PLL even more challenging. The emerging internet of things (IOT) applications also demand the power consumption of PLL device to be substantially low.

In sub-micron CMOS manufacturing, process uncertainties play a vital role. This brings about the performance variations to such an extent that the yield of the process is greatly affected. There has been continuous efforts to build circuits that are immune to such uncertainties. Such fabrication process tolerant designs are of high interest to integrated circuit (IC) designers in industry.

In general analog integrated circuit design requires many performance parameters to be improved. These performances are competing in nature calling for multi objective optimization to yield a PLL circuit with enhanced characteristics.

1.2 Objective and scope of the thesis

In this thesis, phase noise, lock time and jitter properties along with the power performance of the PLL and its building blocks are investigated. The research objectives of this thesis can be outlined below.

i. to carry out a state of the art overview of the techniques for PLL designs where proficiency is achieved by deploying different methods or architectural modifications for different building blocks. The performance linked architectures of PLL are also to be reviewed by summarizing different parameters. The challenges pertaining to the PLL design are to be enumerated.

ii. to develop techniques that minimize the dead zone problem, a critical performance parameter, occurring when the phase error between the two input signals to the phase frequency detector (PFD) approaches zero. Due to dead zone phenomenon there exists an offset phase difference between the input and feedback signals of the PLL though their frequencies are same after locking.

iii. to improve the phase noise performance and locking ability of PLL so as to cater to most of the modern high frequency applications. This is to be achieved by addressing the design of PFD architectures.

iv. to design a charge pump with enhanced current matching, reduced clock feed-through and charge sharing effects so as to minimize the reference spur and lock time. This is to be achieved using high performance current source and transmission gates in the charge pump circuit.

v. to reduce the effect of fabrication process variations by proposing novel process variation tolerant PLL. The proposed design minimizes the shift in duty cycle of the divider output signal fed to PFD, preventing the lock failure. It improves lock time and phase noise performance of the PLL.

vi. to achieve simultaneous optimization of the PLL performances using an effective multi objective optimization technique there by saving the designer's time and providing near best performance. All the performance parameters like phase noise, lock time and power consumption for a CPPLL are modeled and optimized subject to the practical design constraints.

1.3 Thesis organization and chapter wise contribution

This thesis is organized into eight chapters. Each of the chapters along with contribution of each chapter is presented below.

Chapter 1: Introduction

The motivation behind the work embodied in the thesis is outlined. The

objective of the thesis along with its scopes is also presented. The contribution of the thesis in terms of different characteristics of PLL performance, are also described.

Chapter 2: Phase Locked Loop Design: Recent Developments

In this chapter the basic PLL performance parameters are discussed. To improve these parameters the role and abilities of architectures of various building block are outlined. A detailed investigation of the available literature is carried out to provide a review on the current performance related PLL architectures and scopes for research. A comparative summary of the performance parameters of selected recent designs are also presented. The challenges involved in the PLL design are briefly discussed.

Chapter 3: Efficient Technique for Low Power Fast Locking PLL Operating in Minimized Dead Zone Condition

This chapter focuses on phase frequency detector (PFD), the first building block of PLL. Dead zone being one of the limitations of PFD which affects the phase noise and locking capability of the PLL is addressed. The design of a dead zone free PLL with low phase noise and fast locking capability is proposed in this chapter. The design is achieved by using a voltage variable delay element (VVDE) in the reset path of the phase frequency detector (PFD). A feedback from one of the inputs of charge pump circuit is used to maintain the overall PFD delay at a small positive value to avoid dead zone at lower phase noise. The lock time of the PLL is reduced along with the eventual reduction of power consumption.

Chapter 4: Adaptive PFD Selection Technique for Low Noise and Fast PLL

In this chapter an analytical model of phase noise and settling time for the overall charge pump PLL is presented. A dual PFD architecture is proposed where the PFD is adaptively selected to offer low noise and fast locking ca-

pability. The lock range of the PLL is also markedly enhanced which enables the PLL to be used over a wide range of communication standards making it available for many applications. The PLL consumes less power in comparison to other multi-PFD architectures and the peak to peak jitter does not vary much over a wide range of temperature and in all fabrication process corners.

Chapter 5: A New Transmission Gate Cascode Current Mirror Charge Pump For Fast Locking Low Noise PLL

This chapter represents a novel transmission gate cascode current mirror (TGCCM) Charge pump circuit. In the design, one supply independent reference current source is used leading to minimum current mismatch. The transmission gate (TG) switching is used to reduce different switching errors. After the PLL locks, the control voltage obtained is ripple free which reduces the reference spur. The lock time of the PLL is very less using this proposed charge pump.

Chapter 6: Process Variation Tolerant Wide-band Fast PLL with Reduced Phase Noise using Adaptive Duty Cycle Control Strategy

In this chapter process variation related locking and phase noise performance of the PLL is enumerated. A design strategy for frequency divider in PLL is proposed, which adaptively controls the shift in the duty cycle due to process variations and hence the PLL to lock at high frequencies. The proposed process variation tolerant design is demonstrated to assist the PLL to lock faster in normal operating conditions too. It achieves reduction of the phase noise at a given operating frequency under similar operating conditions. This PLL is demonstrated to provide a wider temperature range of application in comparison to normal PLL.

Chapter 7: Multi objective optimization of PLL performances using IDEA

This chapter reports the modeling of PLL performances, like phase noise

and power consumption. These two performances along with the lock time of PLL is optimized by an efficient multi-objective optimization technique, infeasibility driven evolutionary algorithm (IDEA) in a real time constrained environment. The simulation study reveal significantly superior performance of the optimized PLL.

Chapter 8: Conclusions and scope for future work

This chapter presents the general conclusions drawn from the proposed work with much emphasis on the work done. The limitations and scope for further research work has been discussed at the end.

1.4 Outcomes of the thesis in terms of results

The performance of the phase locked loop (PLL) dictates the quality of the communication systems where it is used. It is desirable for the PLL to have fast locking, low noise, wide lock range, low power consumption and less silicon area. However to achieve these performances simultaneously for the PLL is challenging. Invention of various techniques for the basic building blocks of the PLL have made them efficient by minimizing the above constraints and vital for almost all communication systems where it is used as frequency synthesizers or clock generators. It is further expected that these types of modifications will help in performance and reliability of the future communication systems. These will also ensure for higher accuracy for a wide lock range fast locking PLL that can be employed for several frequency bands of GSM and WiMAX technologies. A concise survey of the latest PLL techniques where proficiency is achieved by deploying different methods or architectural modifications for various building blocks and the resulting performance of the PLLs are comprehensively presented.

A novel technique to minimize the blind zone which reduces the phase noise is presented. In this work, a variable delay element is incorporated in the Reset

path of the PFD. The overall PFD delay is maintained at a small positive value to avoid blind zone at lower phase noise. The performance analysis carried out in Cadence design environment and compared with the performance of a PFD using a fixed delay element in its reset path. The designed PLL achieves a phase noise of -109.5 dBc/ Hz at 1 MHz of offset frequency. With this phase noise enhancement of 6 dB, the power consumption is also reported to be 1.73 mW.

Charge Pump in a phase locked loop (PLL) generates non-ideal effects such as current mismatches at the output node and switching errors at the pull up and pull down networks. A novel transmission gate cascode current mirror charge pump circuit is presented. The switches incorporated in this work are transmission gates which help to reduce various switching errors, and only one supply independent reference current source is used to have a minimum current mismatch of only 7%. It is observed that the loop locks in 25 ns which is 50% faster than the conventional charge pump. The control voltage has almost no ripple in it after locking bringing down the reference spur. This PLL operates at 2.5 GHz having a wide lock range of 0.5 to 2.8 GHz with an average power consumption is 1.74 mW. Due to the use of cascade current mirror circuits, the obtainable output voltage swing is 1.79 V.

Selecting the fast phase frequency detector (PFD) before the loop locks and the low noise PFD after locking, a fast and ultra-low noise phase locked loop (PLL) design is achieved. A comprehensive phase noise and settling time formulation for the charge pump PLL is presented. A dual PFD architecture of a PLL which combines the benefits of both the PFDs and heavily shrinks the trade-offs among phase noise, power consumption and lock time of the PLL is presented. This is made feasible by adaptively selecting the PFD at suitable instants of operation of the PLL. The PLL locks within 120 ns consuming an average power of 1.2 mW for an input reference frequency of 1.25 GHz. The proposed technique is energy efficient with consistent jitter performance over a wide range of temperatures. It also operates over a wide lock range of

0.7-2.8 GHz so that it can be used in cellular handsets for multiple radio standards like Global System for Mobile communications (GSM) and Worldwide Interoperability for Microwave Access (WiMAX).

The effects of manufacturing process variations on the phase locked loop (PLL) performances like lock time, lock range and phase noise are studied. At higher operating frequencies, due to process variations, there is a shift in duty cycle of the divider output to phase frequency detector, leading to lock failure. To alleviate this problem an adaptive duty cycle control (ADCC) strategy is proposed and used in the frequency divider present in the feedback path of PLL. The proposed technique makes the PLL process variation tolerant and lock at higher frequencies where otherwise PLL goes out of lock. It assists the PLL to lock faster and achieve low phase noise at all frequencies under nominal conditions. The operating temperature range is also enhanced to -100^0 to 100^0C. Simulation studies on a 3.5 GHz PLL reveals the lock range improvement of 40% and phase noise improvement of 15% over a normal PLL.

The PLL performances like phase noise and power consumption are modeled. Along with these two performances the lock time of PLL is subjected to optimization in a real time constrained environment. An efficient multi-objective optimization technique infeasibility driven evolutionary algorithm (IDEA) is used. With the optimized design parameters the PLL is simulated in cadence analog design environment for model validation. This is demonstrated to achieve significantly superior performance of PLL. Compared to a recently published article where analytical method is adopted, the values of filter components are very less. This design methodology benefits the designer in industry to deliver a product with near optimal performance in significantly less time.

1.5 Publications out of the thesis

Published/Accepted:

Journals:

[**P1**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, Design of an efficient Phase Frequency Detector to reduce Blind Zone in a PLL, Microsystem Technologies, Springer. (In Press)

[**P2**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "Low Noise and Fast Locking Phase Locked Loop Using a Variable Delay Element in the Phase Frequency Detector", *Journal of Low power Electronics, American Scientific Publishers*, Vol.10, no.1, pp. 53-57, 2014.

[**P3**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "A New Transmission Gate Cascode Current Mirror Charge Pump for Fast Locking Low Noise PLL", *Circuits, Systems and Signal Processing, Springer*, Vol.33, no.9, pp. 2709-2718, 2014.

Communicated:

Journals:

[**C1**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "Phase Locked Loop Design: Recent Developments", *IETE Journal of Research, Taylor and Francis*

[**C2**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "Adaptive PFD Selection for Low Noise and Fast PLL in Multi-standard Radios", *Microprocessors and Microsystems, Elsevier*

[**C3**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "Process Variation Tolerant Wide-band Fast PLL with Reduced Phase Noise using Adaptive Duty Cycle Control Strategy", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*

[**C4**] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "Multi-performance Optimization of a PLL for Fast Locking Energy Utilization and Low Noise", *Circuits, Systems and Signal Processing, Springer*

Chapter 2

Phase Locked Loop Design: Recent Developments

2.1 Introduction

Phase locked loops (PLLs) [1–5] are integral parts of all communication systems mostly as synchronizers, clock and data recovery circuits, frequency synthesizers and clock generators. PLL is expected to perform over a wide range of frequencies starting from audio to radio systems. Besides this, the topologies of PLL vary depending on it's application beginning from purely analog through mixed signal circuits to all digital circuits. Owing to this diversity, PLL has been an active area of research and product development over the years. Sometimes the PLL itself is deliberated as a unique system and its design is one of the most challenging tasks, requiring dedicated efforts. A major challenge in the design of high-performance PLLs, containing combination of several components of different features and covering the entire field of circuit design is to optimize among the trade off parameters like lock time, power consumption, phase noise, and bandwidth [6, 7].

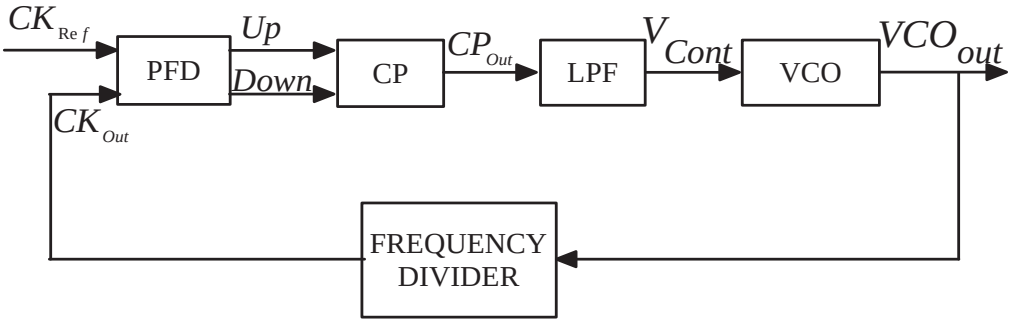

Figure 2.1: Simple block diagram of CP-PLL [1]

The techniques and strategies essential for implementing each constituent block of charge pump PLL (CP-PLL) (Figure 2.1) differs to cater the varying requirements. Each block needs a specific methodology and is driven by an appropriate design flow which ensures that the final design meets its specification requirements.

CP-PLL is one of the most commonly used topology for PLL. It consists of subsystems like Phase frequency detector (PFD), charge pump (CP), loop filter, voltage controlled oscillator (VCO), and a frequency divider. The PFD compares the input reference signal (CK_{Ref}) and the feedback signal (CK_{Out}) with respect to their phase and frequency and generates two signals, Up and Down in response [8]. The charge pump takes these two signals as its input and generates a constant current into the loop filter. The loop filter can be a R-C network that filters the error voltage produced due to the phase difference between CK_{Ref} and CK_{Out}. The filtered output voltage is the control voltage of the VCO that shifts it's output frequency in a direction to reduce the phase difference between the CK_{Ref} and CK_{Out} signals. When the control voltage matches the average frequencies of the CK_{Ref} and CK_{Out}, the loop is said to be locked. If the CK_{Ref} and VCO_{Out} are of different frequencies then a frequency divider is used in the feedback path taking the signal from VCO and feeding to PFD. Even though the CK_{Ref} and CK_{Out} signals do not exactly match with respect to their phase, and have a constant or offset phase difference, the PLL is said to be lock if the frequency of the above two signals match.

2.2 Performance Indices of PLL

A PLL consists of multiple sections. Design error in any of the sections can lead to anomalies in operation. Similarly each stage also controls certain properties of the signal. The performance dependency of a PLL with respect to each of its components is illustrated in Figure 2.2.

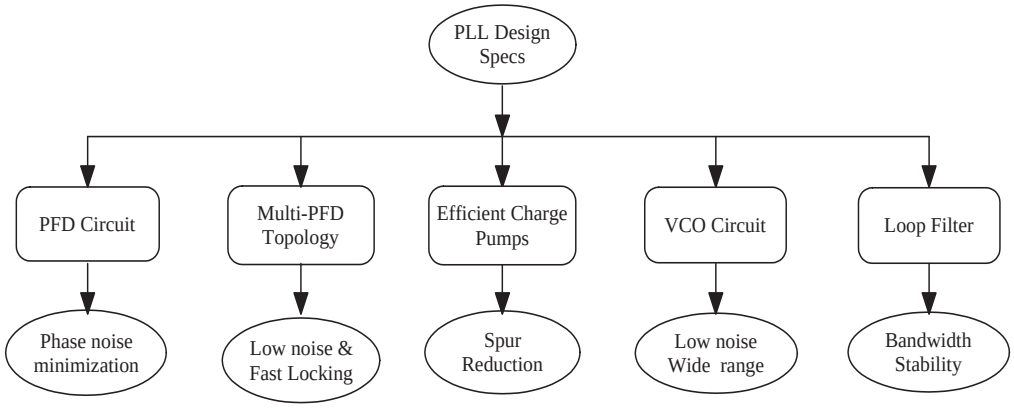

Figure 2.2: Performance mapping to major contributing PLL block

2.2.1 Phase Noise

Phase noise plays a very important role in PLL as it affects the spectral purity of the output signal. Theoretically it is desired that the signal spectrum at the output should be a single line at the desired frequency of operation. But usually PLL output is observed to contain a band of other frequencies which can be considered as spectral impurities. These signals appear as phase noise which is attributed to the random phase and frequency variation of the propagating signal.

PLL is a type of oscillator, and in any oscillator design, frequency stability is an critical criteria. The most significant source of phase noise in a PLL is the VCO, though random noise is also available in the reference input, PFD, loop filter and dividers. Thermal, shot and flicker noise are examples of the sources for which fluctuations in the frequency occurs. One of the sources of

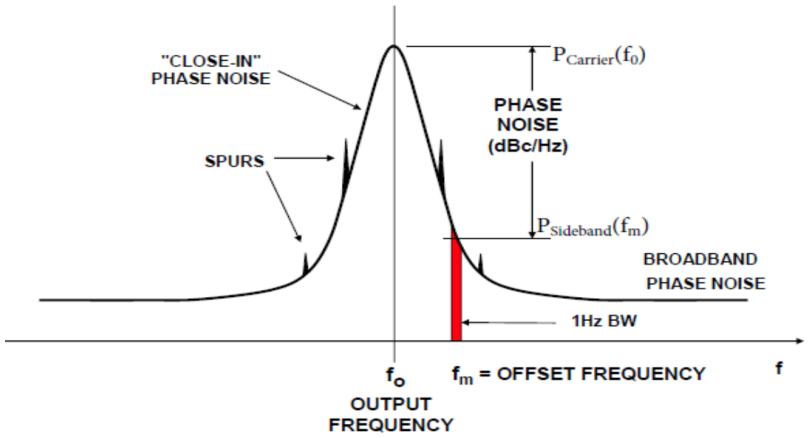

Figure 2.3: Oscillators phase noise and spurs [9]

noise is the additive Gaussian noise. Here the probability distribution of the signal noise amplitude is distributed in the form of a Gaussian curve. Two types of amplitude and power density spectra of the signals are considered, those are single sided and double sided.

Short term instabilities in an oscillator can be characterized in the frequency domain in terms of the single sideband noise spectral density. Figure 2.3 demonstrates a typical spectrum, with random and discrete frequency components causing broad skirt and spurious peaks [9]. The phase noise spectrum of an oscillator shows the noise power in a 1 Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1 Hz bandwidth at a specified frequency offset, f_m, to the oscillator signal amplitude at frequency f_o.

Generally an oscillator is characterized in terms of its single-sideband phase noise [9] as shown in Figure 2.4, where the phase noise in dBc/Hz is plotted as a function of frequency offset, f_m, with the frequency axis on a log scale. It can be observed here that the actual curve is approximated by a number of regions, each having a slope of $1/f_k$, where k = 0 corresponds to the *white* phase noise region (slope = 0 dB/decade), and k = 1, corresponds to the *flicker* phase noise region (slope = 20 dB/decade). There are also regions where k = 2, 3, 4, and these regions occur progressively closer to the carrier frequency.

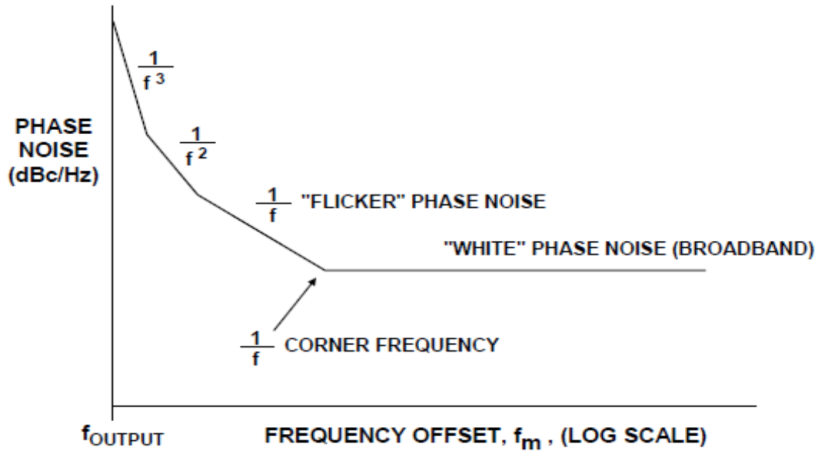

Figure 2.4: Phase noise in dBc/Hz versus frequency offset at PLL output [9]

2.2.2 Jitter

Jitters constitute the short term variation of signals with respect to their ideal position in time domain. This adversely affects the quality of information transmitted. Deviation of the signal from the ideal position can occur on either leading edge or trailing edge of signal. Some of the usual sources of jitter are internal PLL components, thermal noise generated randomly from crystal, crystal vibration causing random mechanical noise etc. Jitter increases with the time delay between the reference and the observed transition as shown in Figure 2.5. The variance, σ_t^2, increases as the time between reference and the observed transition increases. This is popularly known as jitter accumulation. Phase noise can be converted into time jitter [9] by integrating the phase noise plot over the desired frequency range.

2.2.3 Reference spurs

In the architecture of the PLL, the Up and Down outputs of the phase frequency detector produce narrow pulse at every phase comparison, though the input phase difference is zero, which drives the charge pump. There can be even an ac component that is sub harmonic of the reference frequency. Even

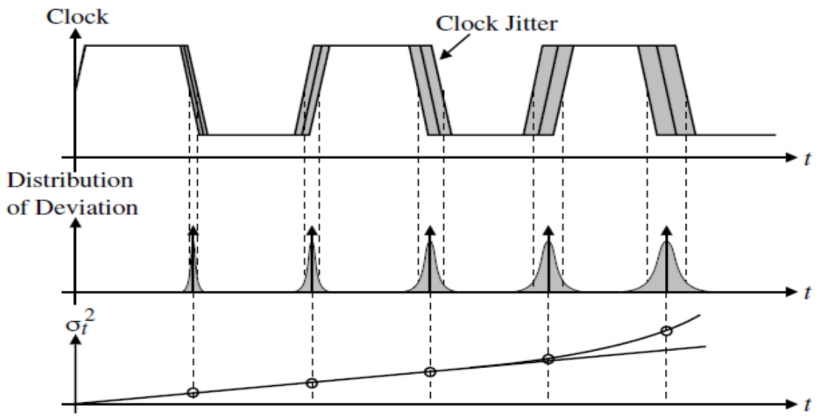

Figure 2.5: Jitter accumulation

though these are very narrow in nature, their existence indicates that the dc control voltage which drives the VCO is fluctuated by a signal that is equal or multiple of input reference frequency ($f_{CK_{Ref}}$). This results in reference spurs [10] in the output which occurs at offset from the center frequency that are multiples of reference frequency (Figure 2.3) like the offset values of $\pm f_{CK_{Ref}}$, $\pm 2f_{CK_{Ref}}$ etc. The signals causing these spurs are called as feed-through.

2.2.4 Lock time

In many critical applications, it is very vital for the PLL output to lock to the input signal as soon as possible. Lock time is the time taken by the PLL to establish the lock (or capture the signal). Fast locking is a desirable characteristic of the PLL.

2.2.5 Lock range

The range of frequencies over which PLL will track the input frequency signal and remains locked is referred as PLL Lock range.The lock range is usually band of frequencies above and below the PLL free running frequency or operating frequency.

2.2.6 Bandwidth

Loop bandwidth is mainly controlled by the filter present next to the charge pump in a PLL. Normally this filter is a low-pass filter, and the lower the cutoff frequency of this filter the lower is the loop bandwidth. Other factors also can affect loop bandwidth, such as the speed at which the VCO can change the output frequency in response to its input. Also, any frequency dividers in the PLL can potentially change the loop bandwidth. But the overwhelming factor in loop bandwidth is the filter. Bandwidth can also be defined as the frequency where the PLL starts to lose the lock with reference signal. There are a lot of non ideal effects which produce high amount of ripple on the biasing voltage and modulate the output frequency of VCO. Hence the waveform becomes non periodic. Lower values of loop bandwidth lead to reduced levels of phase noise and reference spurs, but at the expense of longer lock times. Hence the loop bandwidth can be estimated depending on the specifications. Generally the loop bandwidth is taken to be $1/20^{th}$ of the reference frequency.

2.2.7 Stability

A system which remains in a constant or defined state unless affected by an external action and returns to the constant state when the external action is removed can be defined to be stable. A PLL being a type of oscillator, frequency stability is of critical importance. PLL stability is analyzed using the measures like phase and gain margin in a linear PLL model. As long as the loop-filter bandwidth is low enough for the linear PLL model to be valid, a second order loop-filter is always stable. However, parasitic components may introduce higher order poles, and the phase shift from these poles may decrease the phase margin and consequently affect the stability. Variation in loop-gain due to changes in PLL division ratio and non-linear oscillator tuning curve may also degrade phase margin under certain operating conditions. Changing the loop gain affect the position of the poles and zeros. The phase of the open-loop

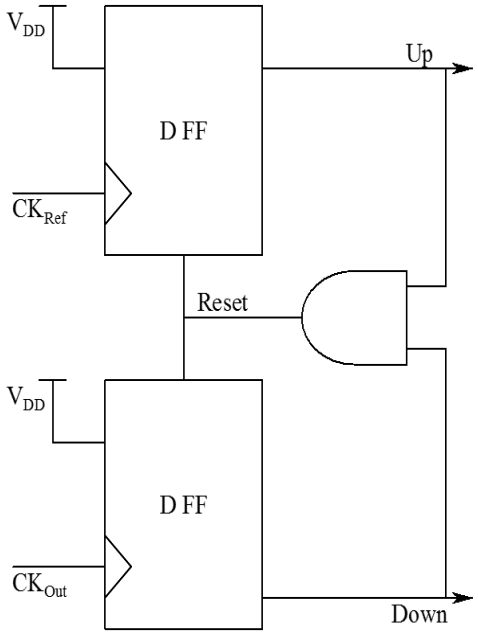

Figure 2.6: Conventional PFD

transfer function is identical for both loop gain settings. However real PLL implementation should of course be designed to be stable for all loop-gains.

2.3 Architecture of PLL components linked with performance

Figure 2.2 shows the dependencies of overall PLL performances on various PLL components. Each of the PLL components with respect to their individual performance contribution to the overall PLL design are discussed.

2.3.1 Phase frequency detector

Analysing the generic PLL Figure 2.1 [4], a simple phase frequency detector (PFD) generates two signals, namely Up and Down in response to the CK_{Ref} and CK_{Out}. A simple phase frequency detector architecture is shown in Figure 2.6 [11] which consists of two resettable D flip-flops used to detect the phase

difference between the reference signal and the feedback signal. Depending on the relative phase of the CK_{Ref} and CK_{Out} signals, the PFD generates an Up and a Down signal that switches the current of the charge pump. Initially, both outputs Up and Down are low. At the rising edge of one of the PFD inputs, the corresponding output becomes high. This state is continued until the second input goes high. When both the outputs are high the circuit resets. Ideally the characteristic of PFD is linear for the entire range of input phase differences from -2π to 2π. When the inputs differ in frequency, the phase difference changes each cycle by $2\pi[(T_{CK_{Ref}} - T_{CK_{Out}})/\max(T_{CK_{Ref}}, T_{CK_{Out}})]$. Here $T_{CK_{Ref}}$ and $T_{CK_{Out}}$ are the time periods of CK_{Ref} and CK_{Out} respectively.

The incoming reference and feedback signals decide whether the PFD will set or reset. When the PLL is locked the phase difference between the two input signals (CK_{Ref} and CK_{Out}) is very small. In this case if one rising edge from any of the two signals is detected at one of the flip flops (FFs) then that FF will set and the output (Up or Down) will take finite amount of time to reach at the charge pump due to propagation delay of the FF. During this period if the second FF detects rising edge of another input signal then that FF will set and give output as high. Now both the output signals of the PFD will be high which causes a reset signal to be generated for both the FFs and disable the PFD for phase difference detection. This minimum phase difference region where no phase difference can be detected by PFD is called as Dead Zone phenomenon [12, 13]. In other words, it is the minimum pulse width of the PFD output that is needed to turn on the charge pump completely.

Due to this, the PFD can not detect the phase difference that is smaller than the dead zone and the output of the PLL varies within this range causing further increase in phase noise and jitter [14]. The transfer function of the PFD illustrating the dead zone region is shown in Figure 2.7 in phase difference axis.

Blind zone is another issue with PFD where the actual leading phase from one of the inputs will not be detected at the output. When the phase difference between the two inputs of the PFD is close to 2π, the rising edge of the leading

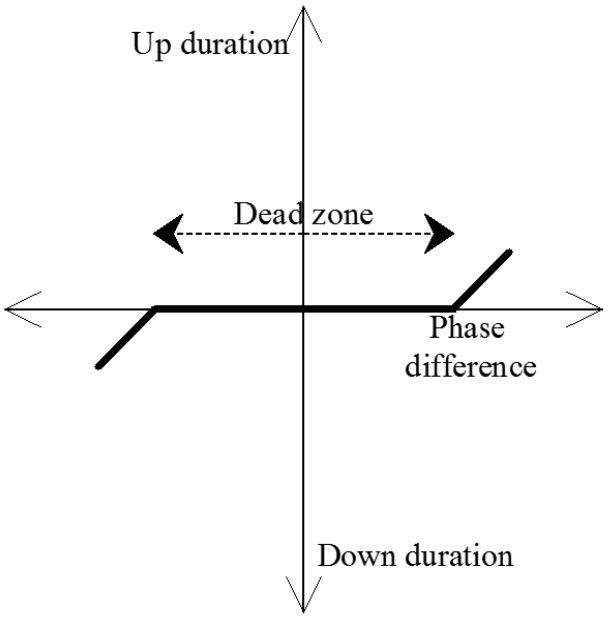

Figure 2.7: Dead zone illustration in the transfer characteristics of PFD

phase may fall in to the reset region, due to which the leading phase can not be detected leading to a wrong measurement at the output. This reset zone is called blind zone.

2.3.2 Charge pump

Charge pump is a switching circuit that pumps charge in to the loop filter under the control of the phase frequency detector. Usually charge pump circuit paired with PFD (Figure 2.8), generates a constant control voltage for the VCO [15]. The DC level of this voltage is controlled by the Up and Down signals of the PFD [11]. Hence it depends on the phase difference between the two inputs of the PFD. Typically charge pump has two current switches denoted as Up and Down. The Up switch delivers a pump current I_{Up} into the loop filter when Up signal of the PFD is active and the Down switch extracts a pump current I_{Down} from the loop filter when Down signal of PFD

is active. Due to this switching action a charge pump behaves like a time varying network. Ideally $I_{Up} = I_{Down} = I_{Cp}$. Where I_{Cp} is the net charge pump current.

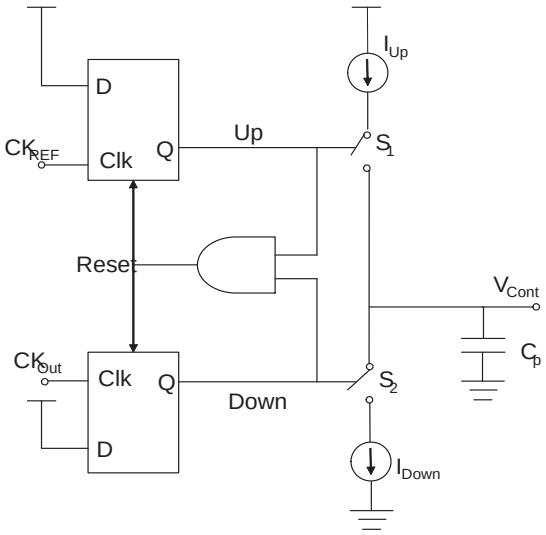

Figure 2.8: Conventional PFD with charge pump

Charge pump PLLs (CP-PLLS) are widely deployed in modern communication systems for their large gain, wide frequency acquisition range and fast locking capability. However charge pump in a PLL generates non ideal effects such as current mismatch at the output node and switching errors at the pull up and pull down networks. The charge pump should generate a constant current into the loop filter having the capacitor. But the current mismatch between Up and Down network of the charge pump increases the glitches in it resulting in the static phase offset and dynamic jitter which are also known as reference spur in PLL. The reference spur [16] is expressed as,

$$S_r = 20log\left(\frac{\sqrt{2}\frac{I_{CP}R}{2\pi}\varphi_e K_{VCO}}{2f_{CK_{Ref}}}\right) - 20log\frac{f_{CK_{Ref}}}{f_{P_{LPF}}}\,(dBc) \tag{2.1}$$

where R is the resistor in the loop filter, I_{CP} is the charge pump output current, ϕ_e is the phase offset, $f_{CK_{Ref}}$ is the frequency of the reference signal, $f_{P_{LPF}}$ is the frequency of the pole of the loop filter.

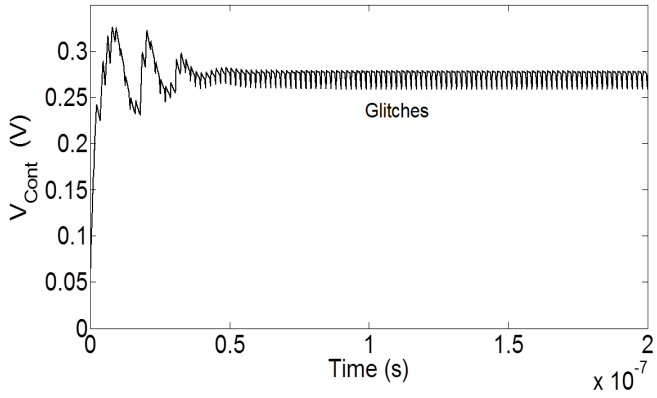

Figure 2.9: Conventional charge pump non ideal effects

Leakage current, current mismatch and timing mismatch are some other dominant reasons for non ideal characteristics of charge pump [16] on which the level of reference spurs of the PLL depends. Switching errors due to leakage current, including charge injection, clock feed through and charge sharing are other non-ideal effects in charge pump [17]. In ON state, the MOS switch S_1 holds charge in its channel. But when they are switched off partially, some charge will flow towards the drain terminal, causing the load capacitor at the output of the charge pump to be charged to some extent. This gives rise to charge injection that enhances the spikes in the control voltage. When the switch transistors are in OFF state the output of the charge pump floats. When these transistors transit from OFF to ON, charge sharing occurs between the parasitic capacitance and the output node of the charge pump resulting in a deviation in the control voltage. Clock feed through is a result of the fast rise and fall of the clock signal coupled into the signal node through the gate to source and gate to drain parasitic capacitances. It raises the level of signal which could forward bias the PN junction of the MOSFET, resulting in electron injection into the body of the MOS causing faulty operation as it propagates through a nearby high impedance node [17].

The non-idealities of the charge pump described above give rise to the glitches indicated in Figure 2.9. Even after the PLL is locked, the glitches are

usually observed, which can introduce a formidable amount of reference spur.

2.3.3 Loop filter

During the locked state in PLL, the output of the PFD is a contribution of number of factors. Out of these, the first one is a dc component which is roughly proportional to the difference in the phase between the two inputs of the PFD. The remaining factors are the ac components referred as the sub harmonics (multiples) of the reference frequency. These unwanted high frequencies are filtered out by the loop filter acting as a low pass filter. The loop filter determines the stability of a CP-PLL. Loop filters are classified into active and passive types. Active loop filters are complex and generate more noise. Hence a passive filter is preferred for PLL design.

A charge pump PLL using a phase frequency detector with charge pump is of type-II [18]. The loop filter as presented in Figure 2.10 has a resistor R that is in series with a capacitor C_1 and another capacitor C_2 is in parallel with R and C_1. When the PLL is in the locked state the output node of the charge pump is in the high impedance state as none of the transistors at the output stage of CP is active. In this state the capacitor C_1 can not discharge. Hence the passive filter behaves like an integrator when driven from three state source. This can adjust control voltage. In this filter R is used to improve the stability of the loop. But adding a resistor in series, the loop filter experiences a larger control voltage jump and hence a frequency jump in the output of VCO. C_2 is deployed to keep the voltage drop on R from causing jumps on the control voltage of VCO and consequently jumps in frequency of the VCO output. Adding C_2 the filter becomes a 2^{nd} order one and the PLL a third order one. This creates the stability problem again as the order of the PLL increases. But if the C_2 is of $1/10^{th}$ of the C_1, the close loop time and frequency responses remain unchanged making the PLL stable [4].

Evaluation of proper loop filter component values, depends on filter topol-

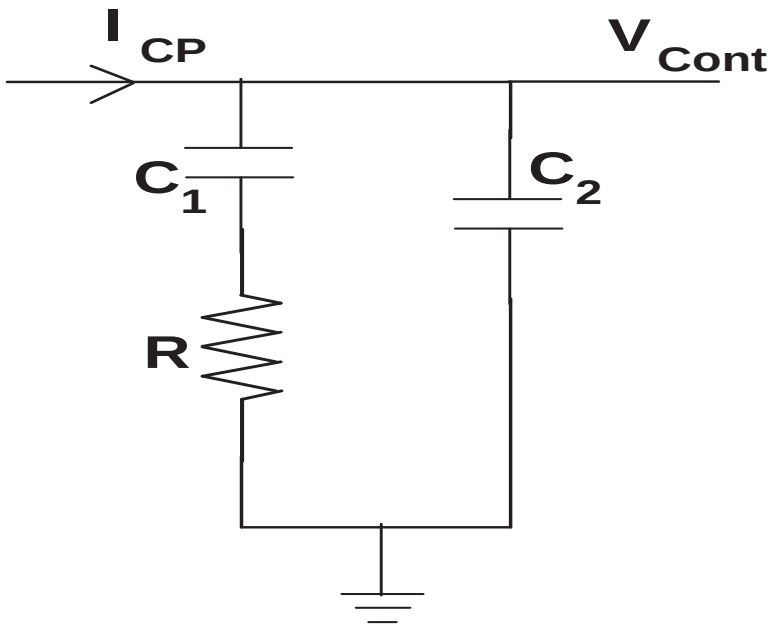

Figure 2.10: Second order passive lead lag filter for PFD with current output

ogy, order, bandwidth, phase margin, and pole ratios. The stability is related to the phase margin of the PLL. Higher phase margin may decrease peaking response of the loop filter at the expense of degraded lock time. Choosing a very small loop bandwidth improves the reference spur but increases the lock time, whereas choosing a loop bandwidth of too wide, the lock time is decreased but the reference spur becomes worse.

2.3.4 Voltage controlled oscillator

A wide tuning range voltage controlled oscillator is used in PLL so that the entire frequency range is covered. Also the phase noise requirement of the VCO can be loosened due to that when the loop is locked, the noise generated by the VCO at the center of oscillation frequency will be filtered out by the loop bandwidth. But when it comes to be used in noise sensitive applications, especially at high frequency of operation, the employment of LC-VCO [19] finds preference over other VCO types. Another type of VCO which provide good control over delay and high dynamic supply noise rejection is differential

VCO (DVCO) [20] [21].

An N stage Current Starved VCO (CS-VCO) shown in Figure 2.11 is similar to a ring oscillator. Here the ring oscillator is composed of five inverter stages where each stage constitutes one PMOS and one NMOS present at the middle of each stage of the CS-VCO. The PMOS connected to V_{DD} and NMOS connected to ground operate as current sources. The current sources limit the current available to the inverter, in other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. The input control voltage set the currents at the drain terminals of the PMOS and NMOS.

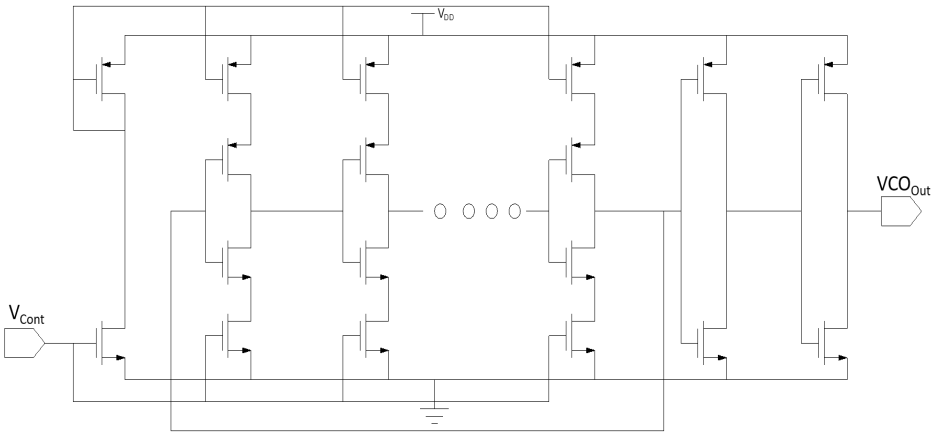

Figure 2.11: Current Starved Voltage controlled oscillator

2.3.5 Frequency divider

The output of the VCO is normally fed to the input of PFD through the frequency divider circuit to scale down the frequency. A simple D flip flop as shown in Figure 2.12 acts as a frequency divider network. Here the $Q^{'}$ output is fed back to the D input. The VCO_{Out} works as a clock for the D-FF.

At the first rising edge, the state of D input is passed to Q. As the $Q^{'}$ is the inverted state of Q and fed back to D, this state will be transfered to Q in the second rising edge of VCO_{Out}. In other words in the first cycle of VCO_{Out},

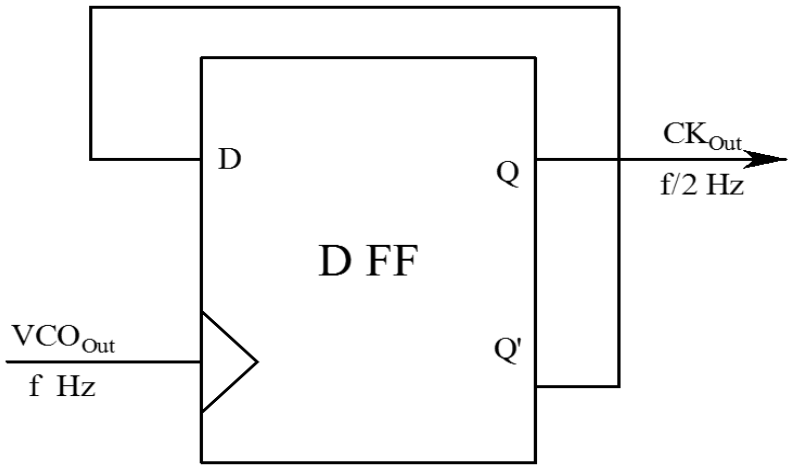

Figure 2.12: Frequency divider circuit using D-flipflop

Q will be in one state and in the second cycle of the VCO_{Out}, Q will be in another state. Thus the frequency of the VCO_{Out} signal is halved.

2.4 Architectures of PLL components

A large number of architectures are available for different components of PLL. However some of the recent architectures of the PLL components are discussed here in relation with their performances. The review of the architectures is restricted only to most seemingly efficient ones.

2.4.1 PFD Architectures in PLL

The noise contributed from the PFD modulates the Up and Down pulse widths [8] which generates a random component in the charge pump output current. The phase noise can modulate both the widths of Up and Down pulses by same amount so that charge pump produces no net output. The phase noise can also modulate the position of Up only with respect to Down. But the most interesting case is when the phase noise modulates both the widths of Up and Down signals simultaneously. The random difference between the widths of Up and Down pulses raises the phase noise of the PFD. The phase noise can be

related to the timing jitter [22]. Recently a number of tri-state PFDs have been designed in literature, which include precharge-type PFD [22, 23], and latch-based PFD [24] as presented in Figure 2.13. Out of these PFD topologies, the latch-based PFD is frequently employed for its high operating speed, wide input range and low power consumption. The design of a dead zone free PLL with low phase noise and fast locking capability [12, 25–30] are also reported in literature.

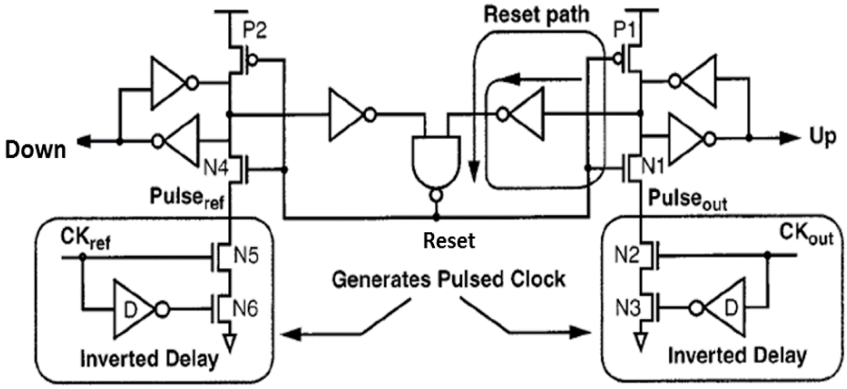

Figure 2.13: Latch based PFD [24]

For clock generators in high-performance microprocessors and high-speed digital communication systems as clock generators, a fast locking phase locked loop (PLL) [16, 24, 31] is generally adopted. These types of applications can sustain a certain amount of phase noise, but need to be fast. On the other hand frequency synthesizers for RF applications need to have ultra-low phase noise. In many systems, fast frequency acquisition, low phase noise and wide lock range are the desirable features.

To reduce phase noise by preventing dead zone, a delay element block having delay of T_D is usually inserted in the reset path of the PFD. A variable delay element based technique as shown in Figure 2.14 is deployed by Charles et al. [12], to minimize the reference spur by maintaining the dead zone free operation of the PFD. Initial experimentation was done with fixed delay elements comprising of two and eight inverters and afterwards the delay length

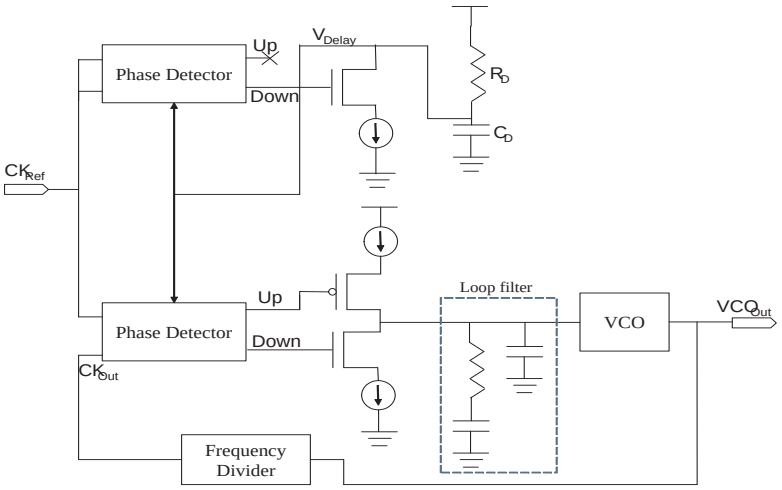

Figure 2.14: PFD with variable delay element [12]

was controlled by the feedback from the charge pump by a variable delay element. The reference spurs reported here are reduced by 16 dB and 12 dB which are better than their conventional counter parts. In comparison to design by Maneatis [32], the reference spur is reduced by around 20 dB and 24 dB at 50 MHz and 100 MHz frequencies respectively. In order to reduce the ripple present in V_{Delay}, a low pass filter having resistor and capacitor is used which in turn increases the chip area.

In a very simple design [33], two inverters acting as a buffer are used to overcome the dead zone. Juang [34] injected a pre-delay element in the reference clock and the local signals, respectively, before they are alternatively provided to the reset inputs of the S-R latches. In this work the dead zone is removed and merged into the intervals of π or -π. Inserting this delay of 1.2 ns, a reduced dead zone of 0.42 ns is achieved. A delayed version of the two inputs is generated in the PFD by Zhang et al. [35]. The delay must be greater than the reset pulse width or the blind zone which ensures that the PFD does not miss any rising edge of any input. Another technique used by Zhang et al. [35] delays the rising edge of the inputs to minimize the blind zone of the PLL.

The pre-charging time for the internal parasitic capacitances is very often

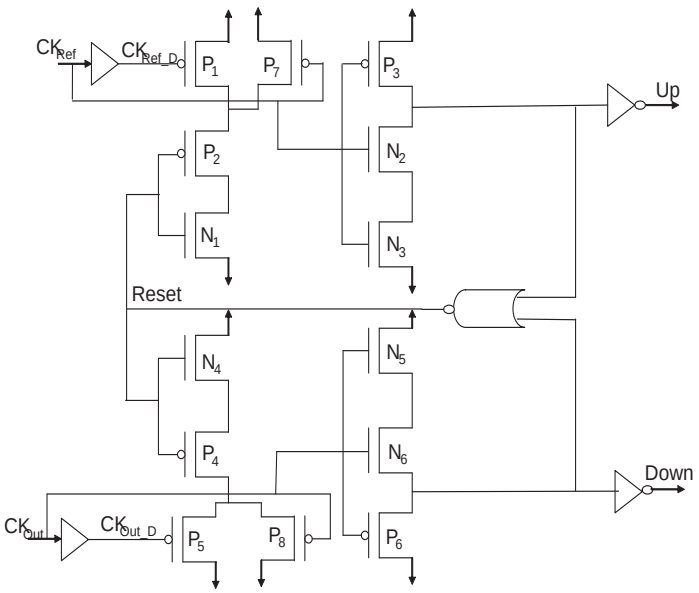

Figure 2.15: PFD with minimal blind zone [26]

responsible for the blind zone. A PFD shown in Figure 2.15 can lessen the pre-charging issue [26]. This approach reduces the blind zone close to the theoretical limit imposed by process voltage temperature (PVT) variations. This PFD is similar to the high speed PFD reported by Lee et al. [36] and combined with a delay cell and two additional transistors. Keeping the operating frequency almost same, the blind zone here is reported to be 61 ps where as in [37] and [36], the blind zone is reported to be 156 and 221 ps respectively. Though the blind zone is very much reduced by Chen et al. [26], the lock time and phase noise information of the PLL needs investigation.

A modified dynamic logic style PFD [27] is used for a delay locked loop (DLL) design. In this case only one of the outputs of PFD is made high at a time, even for a small input phase difference. The dead zone of the PLL at 84 MHz and 800 MHz frequency is limited to 127.3 ps and 10.25 ps respectively. It is also limited in the aforesaid PLL and there exists a scope of power consumption improvement. Two types of PFDs have been developed by Majeed et al. [28], where the operation of the PFDs does not depend on any reset process, thereby completely eliminating the dead zone concept.

The dead zone in PLL can be reduced by making the pulse widths of Up and Down half of their actual size [38]. A difference PFD operating at high frequency uses an edge detector circuit to avoid dead-zone between two input signals [39]. In complementary PFD [40], a phase detector and a frequency detector operate in parallel, where for phase difference below 1800 ps, the frequency detector is turned off. Furthermore, for a dead zone free operation at 4 GHz frequency, the AND gates between the inputs of the phase detector are replaced by transmission gates. The reset path and the delay path are separated in the PFD block [41] ensuring no erroneous condition at the rising edge of the input when the delay is active. A double edge checking PFD is implemented [42] to avoid Up and Down signals to rise at the same time which helps in reducing the dead zone. This PFD can achieve a dead zone of 3 ps at 4.78 GHz frequency when simulated in 0.35 μm CMOS technology with 3-V supply.

A falling-edge PFD using 12 transistors [43], does not depend on the reset signal but the duty cycle of the input signals affects the output. In this PFD the dead zone occur when both the inputs have same duty cycle. A conventional PFD with two more OR gates, an extra NAND gate and an additional "*Start*" signal as shown in Figure 2.16 is implemented [44]. Here the reset signal does not appear when the phase error goes beyond $-\pi$ to π, there by making the PFD dead zone free.

Laha et al. [29] have considered a double gate MOSFET (DG-MOSFET) for the NOR gate of the charge pump PFD making it more area efficient than a conventional one. The reduced transistor count lowers the parasitic capacitance which increases the speed of the PFD. More importantly, for a phase difference of 60 and 80 ps, this PFD generates the output to initiate the charge pump which reaches a required threshold level of logic high in 32 and 45 nm technologies respectively. Hence this faster rise time at a very small phase error makes PFD to avoid dead zone in a superior manner than the PFD having conventional NOR gate. However the above designs lack in a proper

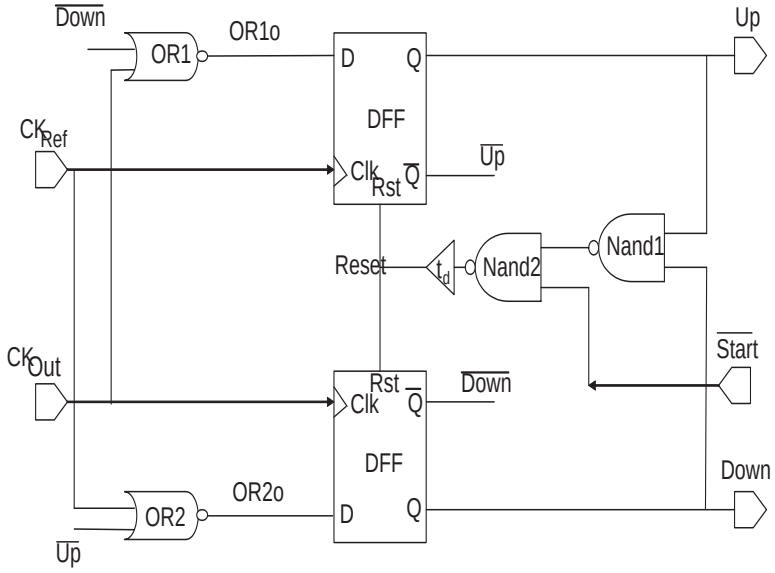

Figure 2.16: Dead zone free PFD [44]

analysis of PLL performance parameters and their simulated performance.

In the fast PFD [25], blind zone appears when the input phase difference goes near 2π. As shown in Figure 2.17, by using only sixteen transistors, this PFD not only eliminates the blind zone, but also speeds up the acquisition process achieving high operating frequency. This has been achieved by avoiding the reset process when the phase difference varies between π to 2π. In 0.5 μm technology with 5 V power supply, the PLL using this PFD has been reported to operate at 800 MHz. Table 2.1 provides a comparative summary of performances of selected architectures discussed in this section.

Table 2.1: Summary of the literature reporting dead zone minimization in PFD

Reference	Performance parameters						
	Reported Result type	Technology (nm)	V_{DD} (V)	Lock time (ns)	Max. freq. (GHz)	Dead zone (ps)	Power consumption (mW)
Hu [25]	Simulated	500	5	150	0.8	Nil	-
Ismail [43]	Simulated	180	1.8	-	2.5	Nil	0.006 at 50 MHz
Chen [26]	Measured	130	1.2	-	2.9	52	0.496 at 128 MHz
Lan [44]	Simulated	130	1.2	2800	1.25	Nil	0.062
Zhang [35]	Simulated	130	1.2	90	1.5	Nil	0.01
Raghav [27]	Simulated	180	1.8	265	0.8	10.25	5
Majeed [28]	Simulated	180	1.8	4500	4	Nil	12.1
Kailuke [30]	Simulated	180	1.8	-	1	Nil	0.381

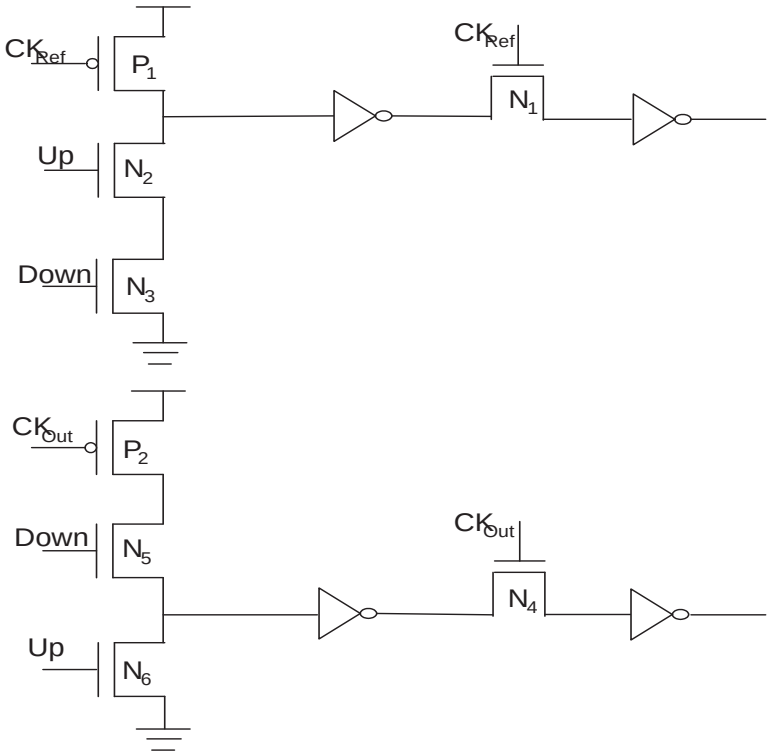

Figure 2.17: Fast PFD with zero blind zone [25]

2.4.2 Multi PFD Architectures

There has always been a trade off among the PLL performance in terms of phase noise, lock time and power consumption based on design. Designers minimize the loop band width [17, 45] to achieve better phase noise performance. On the other hand to minimize the lock time, the band width is enhanced. Hence there exists a tight tradeoff between the frequency acquisition time and phase noise of the PLL. Sometimes improvement of both the acquisition time and phase noise is achieved using hybrid analog/digital PLLs with loop bandwidth stepping ability [32, 46], at the cost of an escalation of power consumption. Another feasible solution to this problem is the adaptive PLL using a wide bandwidth when the loop is in out-of-lock state and switching to a narrow bandwidth as the loop locks. For these adaptive PLLs [17,45,47], the boost in loop bandwidth is accomplished by increasing the charge pump current and loop gain which also increases the power consumption. However if the

loop stability is considered, the reference frequency will be a major constraint in loop bandwidth enhancement technique. Hence to get rid of these trade offs and to achieve simultaneously fast and low noise capability, dual/multi PFD architectures [48–50] are reported.

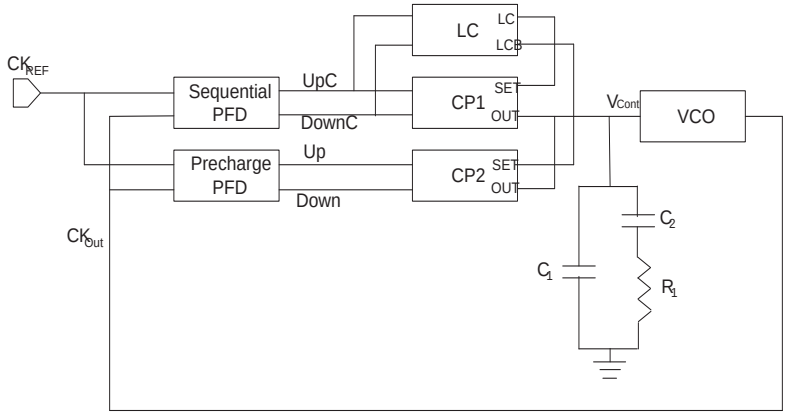

Figure 2.18: Multi-PFD PLL architecture [49]

A phase detector and a frequency detector can be incorporated [51], based on the required applications. A multiplying phase detector is suitable for locking of a data pulse stream, whereas a phase-frequency detector (PFD) is suitable for frequency synthesis since the input signal does not have missing transitions. Frequency detection is generally required to improve the lock time.

Another multi PFD PLL [49] improves the acquisition time and lock range using a sequential PFD and a pre charged PFD as shown in Figure 2.18. A lock detection circuit (LC) is used here to selectively enable the respective charge pump of the PFD to be operated for a particular span of time.

A fast locking PLL with phase error detector (PED) circuit was proposed by Kuo et al. [50].The design reduces both power consumption and acquisition time. The PED circuit here delivers a dual-slope PFD characteristic and charge pump which effectively shrinks the power consumption. A coarse-tuning current is activated to track the large phase difference for fast locking and a fine-tuning current is initiated to complete the fine adjustment near small phase difference.

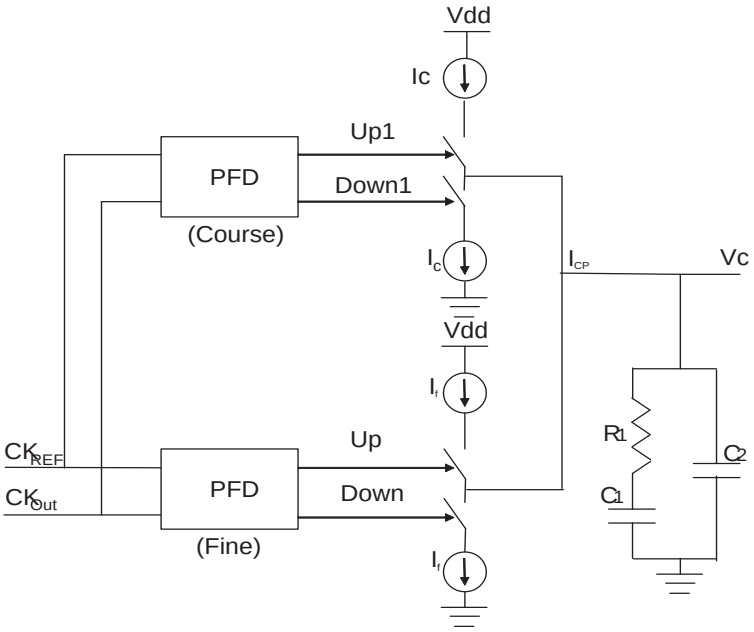

Figure 2.19: Dual slope PFD with charge pump and loop filter [52]

Similarly in another design [52], a dual-slope PFD and charge pump architecture shown in Figure 2.19, accomplishes fast locking of phase-locked loop. The periodic ripples on the control voltage of the VCO are randomized by a novel random clock generator [48] where random selection of the phase frequency detectors is performed to reduce the reference spur at the output of the PLL in locked state. The performance parameters of the reported multi PFD architectures are summarized in Table 2.2. However in most of the reported multi PFD architectures discussed above, the power consumption is very high and lock range is also limited.

Table 2.2: Summary of performances of PLL using multi-PFD architectures

Multi-PFD Architectures	Performance parameters							
	Reported Result type	Technology (nm)	Frequency (GHz)	Phase noise (dBc/Hz)	Lock range (GHz)	Lock time (ns)	Power (mW)	Area (mm^2)
Liao [48]	Measured	180	2.5	-105	2.5-2.7	-	20	1.56
Woo [49]	Measured	1500	0.16	-	0.12-0.25	4500	18.68	845
Kuo [50]	Simulated	350	2.4	-	1.8-2.5	150	18.5	-
Cheng [52]	Measured	350	0.8	-	0.36-1.44	3000	23.1	87.1

2.4.3 Charge pump circuits

The non ideal effects due to the charge pump output current mismatch motivated the designers to design charge pump with low current mismatch between Up and Down network of the charge pump enabling faster locking and to have very low or extremely low glitch in the control voltage of the VCO [53–59]. To reduce the current mismatch, only one current source is used from which both the charging and discharging current is derived. As the Up and Down switches are responsible for charge injection, transmission gates (TGs) have been used to reduce the non-ideal effects like charge injection and clock feed through to reduce glitches in control voltage of the VCO. Charge sharing [58–63] is another non-ideal effect which leads to current mismatch.

To improve the performance, charge pumps are broadly categorized into two types viz. differential charge pumps and single ended charge pumps. Differential charge pumps have specific advantages over single ended charge pumps [16]. The overall performance of differential charge pumps is not affected by the switch mismatch between the NMOS and PMOS transistors. Since the switches are made up of only NMOS transistors, and has fully symmetric operation, the inverter delays between Up and Down signals do not generate offset. Compared to the single ended ones, this charge pump doubles the range of output compliance. Since the leakage current is a result of common mode offset, this configuration is not affected by leakage current. Better immunity is provided by two on chip loop filters. Differential charge pumps also suffer from some critical drawbacks like requirement of multiple loop filters consuming large area and common mode feedback circuitry. As many transistors and multiple current sources are required, a large silicon area is occupied which also leads to enhanced power consumption.

Some modifications have been reported in single ended charge pump to overcome their limitations. To control the current mismatch, gain boosting circuits [54, 55] are used which are shown in Figure 2.20. When the Down

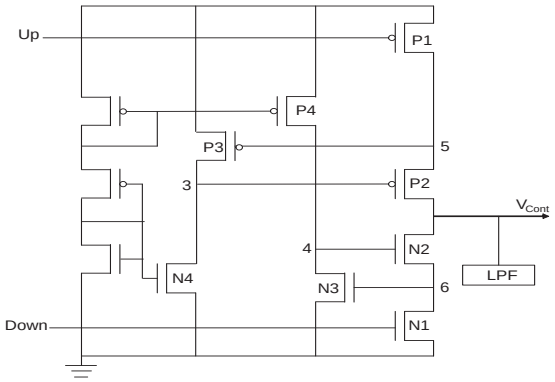

Figure 2.20: Gain boosting charge pump [54, 55]

signal is active, N_2 and N_3 operate in conjunction with N_1 to provide a gain boosting circuit. It increases the output resistance of the charge pump and enhances the current matching characteristics, but the other switching errors have not been considered to improve reference spur.

To minimize these switching errors and also the current mismatch, transmission gate charge pump (TGCP) can be used, where the switches can be realized by transmission gates. Only one current source can be used to reduce current mismatch. Though TGCP removes most of the non-ideal effects in charge pump, use of operational amplifier and a large bypass capacitor makes the circuit consume more power and silicon area. The level of reference spur is also higher than the source charge pump.

To minimize the reference spur level, the phase offset can be reduced as these are directly proportional to each other (Eq. 2.1). To reduce the phase offset, the turn on time of the PFD can be reduced. Perfect current matching characteristics can be achieved by using an error amplifier and reference current sources [57]. To reduce the current mismatch, a second compensation circuit is deployed in a charge pump making it to have two push-pull charge pumps and two replica-feedback biasing circuits working as compensators [59]. A static phase error suppression technique is used by Hassani et al. [64] where reset pulse of phase detector (PD) is used to steer charge pump currents to a dummy branch during idle interval of PD and eliminate charge pump current mismatch

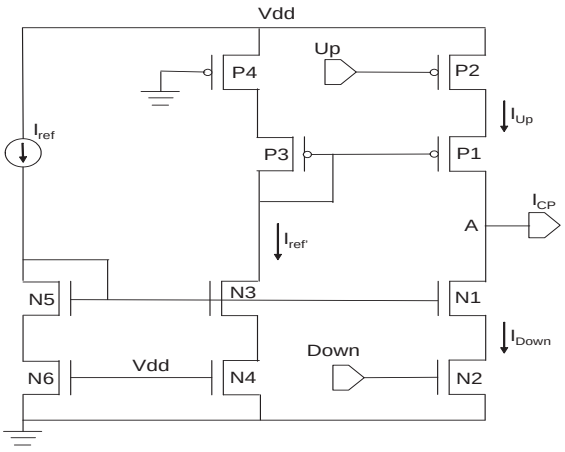

Figure 2.21: Ratioed current charge pump [63]

effect.The charge pump having a rail to rail error operational amplifier with reference circuit and cascode current mirror [60], matches the current over a wide range of output voltage. This operational amplifier can be realized by a rail to rail bulk-driven amplifier designed by Khateb et al. [65], which provides large common mode input voltage range and voltage swing at low power supply. It also provides superior linearity.

An enhanced charge pump design with reduced charge injection and current mismatch [61] has been presented. By changing the position of the switching transistor and adding extra compensation transistors the charge injection has been reduced. A trans-conductance amplifier is added to overcome the current mismatch of the basic charge pump. To enhance the output resistance and to match the output current, two high swing cascode current mirrors each for Up and Down network were proposed by Zhang et al. [62]. A ratioed current charge pump [63] has been seen to suppress the magnitude of the reference spur. This charge pump, depicted in Figure 2.21, is implemented by properly sizing the source and drain network. The sizing can be achieved by using the relation between the ratioed current and the size of the transistors.

Considering the aspect ratios of P_1, P_2 and N_1, N_2 to be same, the Down

and Up current ratio can be written as,

$$\frac{I_{Down}}{I_{Up}} = \frac{\left(|V_{GS_{P3}}| - |V_{T_P}|\right)^2 \left(1 + \lambda_P \left|V_{DS_{P3}}\right|\right)}{\left(|V_{GS_{P1}}| - |V_{T_P}|\right)^2 \left(1 + \lambda_P \left|V_{DS_{P1}}\right|\right)} \cdot \frac{W_{N_1}(V_{GS_{N1}} V_{T_N})^2 \left(1 + \lambda_N V_{DS_{N1}}\right)}{W_{N_3}(V_{GS_{N3}} V_{T_N})^2 \left(1 + \lambda_N V_{DS_{N3}}\right)} \tag{2.2}$$

where, I_{Down} , I_{Up} are the current due to Down and Up networks respectively, V_{GSP_3} , V_{GSP_1}, V_{DSP_3}, V_{DSP_1} are the gate to source voltages and drain to source voltages of P_3 and P_1 respectively. λ_P, λ_N are the channel length modulation co-efficients of PMOS and NMOS devices respectively, V_{T_P}, V_{T_N} are the threshold voltages of PMOS and NMOS devices respectively, W_{N_1}, W_{N_3} are the width of N_1 and N_3 respectively. As the glitches in the charge pump output current are mostly responsible in the reference spur, an additional buffer stage having a delay element, a delay capacitor and a MOSFET is introduced so that the glitches will appear with some time delay [66]. Moreover the capacitance offered by the delay capacitor and the transistor (parasitic) also attenuate the magnitude of the glitches.

Termelez et al. [67] proposed a differential charge pump design technique, that accomplishes low charge sharing and charge injection. Incorporating a sampled data common-mode feedback circuit, the output voltage range of the charge pump is increased and lowering of the mismatch between charging and discharging current is realized. A dynamic current follow technology can be implemented [68] to match the Up and Down currents and two differential pair inverters are incorporated to make the charge pump faster. Alternatively both the currents from Up and Down networks can be fed from a common reference [69], and as long as the aspect ratios of the transistors are same, there will not be any mismatch between Up and Down currents. In another charge pump [70], to reduce charge sharing, current mismatch, and charge injection problems, using differential current-steering switches with DC reference voltage biasing at one side, feed-through of the input pulses is eliminated. The feedback stability issue associated with this design was resolved by deploying differential current-steering switches with one side connected to a DC reference voltage [71]. This

modification minimizes the charge sharing, timing mismatch and feed-through of the input pulses thus Presenting a replica biasing using feedback. It reduces the current mismatch between the Up and Down modules of the charge pump.

Current mismatch compensator circuits can be introduced so that the charge pump will not be influenced by process variations and power supply noise [72] which are also responsible for current mismatch and consequently phase offset. Similarly a beta-multiplier circuit with a differential amplifier [73] can be used to create the reference current independent of the supply voltage. Further to achieve high output impedance and improve the current matching characteristics, the folded cascade structure with a diode-connected PMOS is used.

A PLL with digital calibrated charge pump was designed by Liang et al [74]. Here the static phase difference of the PFD input is measured. This amount of phase difference is associated with current mismatch and was used for calibration. Self-calibrated charge pumps with a voltage scaler [75] are deployed to reduce the static phase error, there by minimizing the reference spur, and jitter of an low temperature polysilicon thin-film transistor (LTPS-TFT) PLL. However, the techniques employed there are difficult to be applied where the phase error is not static. A dynamic auxiliary path in the charge pump is adopted to overcome these limitations [76] . In each reference cycle interval, this path is utilized to detect and correct the current mismatch between Up and Down path. By getting a mirrored controlled voltage a timing control unit determines the time to activate the current mismatch detection module, where a comparator is used to detect the current difference. The difference from the comparator is used in a finite state machine (FSM) to update the Up current to match with Down current. Unlike most existing calibration techniques where the calibration is performed only once at the beginning of the locking process of the PLL, this technique dynamically adjusts the Up current to achieve a better matching performance.

A wide input ranged rail-to-rail Op Amp and self-biasing cascode current

Table 2.3: Summary of the literature reporting spur reduction using new charge pump circuits

Reference	Performance parameters						
	Result type	Technology (nm)	V_{DD} (V)	Reference spur (dBc/Hz)	Current mismatch (%)	Area (mm^2)	Power consumption (mW)
Choi [54]	Simulation	350	3.3	-150	0.1	-	-
Mekky [55]	Simulation	90	2.5	NA	0.6	0.289	-
Zhou [56]	Simulation	180	1.8	-	0.01	15	-
Lee [57]	Simulation	250	2.5	-75	1	40	-
Hwang [59]	Simulation	130	1.2	-	3.2	-	-
Hou [60]	Simulation	180	1.8	-	0.1	0.036	3
Jung [61]	Measured	130	1.5	-	1	3.96	1
Yu [69]	Simulation	180	1	-	Nil	-	0.028
Sun [71]	Simulation	180	1.2	-	0.5	-	0.85
Zhiqun [77]	Measured	180	1.8	-	0.4	0.036	0.9

mirror can be used to reduce the charge pump current mismatch in a large output voltage range [77]. Hence additionally, a pre-charging current source is deployed to enhance the initial charge current that will speed up the settling time of the PLL. A lock detector (LD), a high-resolution phase detector (HRPD), and a 5-bit successive approximation register (SAR) controller are included in a charge pump current mismatch calibration scheme [78] to reduce the reference spurs.

Selected charge pump based PLL performance parameters used in PLL are summarized in Table 2.3. The performance requirements like reference spur reduction, lock time reduction and minimization of the phase noise have also a wide scope for further study.

2.4.4 Voltage controlled oscillator circuits

Due to the increasing demand for high frequency multi band and multi standard transceiver specification in modern wireline, wireless communication wide-band fast locking PLL achieving low phase noise has gained applicability [79]. Therefore requirement of a voltage controlled oscillator (VCO) with wide tuning range, low phase noise is of paramount need [80, 81]. The leakage current due to the device mismatch gives rise to reference spur in a CP-PLL by affecting the common mode voltage [82] of a current starved VCO (CS-

VCO) over a large frequency range. However, with implementation of a high tuning range VCO having large gain, the phase noise can degrade, threatening the stability of the PLL further. Hence a solution to design a wide range PLL without sacrificing the phase noise is required.

A popular technique for lowering the phase noise is to employ a complementary cross-coupled pair with a symmetric rise and fall time [83]. This technique effectively modifies the impulse sensitivity function (ISF) coefficient lowering the phase noise conversion gain. Low phase noise LC-VCOs are generally adopted for PLL design. A LC-VCO design topology using capacitive feedback to provide switched current source implemented at 5.36 GHz frequency was proposed by Liu et al. [84]. The noise shaping effect and the reduction of drain current duty cycle for low phase noise performance of -121.36 dBc/Hz at 1 MHz offset frequency is implemented in the design. Two different 1.8-GHz CMOS VCOs [85] are tuned by an inversion-mode MOS varactor and an accumulation-mode MOS varactor, respectively in 0.6 μm CMOS process for low power consumption and a low phase noise. To minimize tail current output noise, a noise-cancellation technique can be adopted [86] to limit the phase noise of the overall LC VCO. Though the phase noise performance is better in LC VCOs, the tuning range degrades in it which will reduce the lock range of the PLL. An optimal LC-VCO design through evolutionary algorithms is reported by Pereira et al. [87].

Various adaptive frequency calibration (AFC) techniques [88–94] can be realized to design wide range PLLs. To enhance the frequency range, both the discrete and continuous tuning mechanisms can be adopted [89]. An AFC technique is used where an auxiliary digital loop to select a particular band of VCO is incorporated. The lock time achieved with this design was 1.7 μs. To improve the locking process, lock range, lock time, and to reduce the number of comparisons a code optimization along with a binary search algorithm was adopted by Lee et al. [88]. This process achieved frequency range more than 400 MHz and the lock time is less than 65 μs when measured in 180 nm

technology.

At 900 MHz, an automatic switched-capacitor (SC) discrete-tuning loop is deployed [92] to provide 20 percent more tuning range than the conventional one with a calibration time of 2 ms when measured in 0.6 μm technology. However, this calibration time is in a little higher side. A superior design was proposed by Lee et al. [93] where both the switched capacitor bank LC VCO along with the AFC technique to get a tuning range of 600 MHz which is as wide as 40 percent of the highest frequency. However, this technique also suffers from high calibration time of the order of tens of μs. A VCO with a 5-bit differential switched capacitor array to build a tuning range from 2-3.2 GHz was proposed by Zhang [90], which achieved a calibration time of less than 6 μs.

Another AFC technique is implemented by Yadong et al. [91] which works in two different modes namely frequency calibration mode and store/load mode. In the first mode, an efficient frequency detector is employed to reduce the lock time to 16 μs. In second mode of operation, by loading the calibration results, stored after frequency calibration, the AFC makes the VCO come back to the calibrated frequency in about 1 μs.

Yet in a different design [94], a fast and high-precision search for an optimal discrete tuning curve of a VCO in a fractional-N PLL is executed. A high-speed frequency error detector (FED) converts the VCO frequency to a digital value and computes the exact frequency difference from a target frequency. A minimum error code finder finds an optimal code closest to the target frequency achieving the tuning range of 2.3 to 3.9 GHz when implemented in 0.13 μm technology. In spite of all the studies, the current starved voltage controlled oscillator still remains a standard choice in PLL design for many acceptable high frequency applications.

2.5 Design challenges

A number of PLL architectures along with their merits and drawbacks by linking them with the vital performance parameters were presented in the previous sections. Synchronizing the phase and frequency of a signal is a tedious job, because performing algebraic operations on frequencies is more challenging than on other electrical parameters such as voltages or currents. This challenge has taken different directions throughout the years, encouraging the invention of numerous architectures and circuit techniques. This section depicts some of the challenges in the design of PLLs at both architecture and circuit level. Some of these design challenges are enumerated here.

2.5.1 Dead zone

As discussed in the previous section, though dead zone is minimized by adopting various circuit techniques, it cannot be made zero. The phase offset will always remain between the reference and feedback signals leading to increased jitter. Therefore there has been a continuous strive among the designers to achieve incremental dead zone minimization.

2.5.2 Charge-pump Current Mismatch

Charge pump circuits in the PLL frequently use current mirror to match the output currents due to the variation of Up and Down signals generated for the PFD. But the current mirrors also have threshold voltage mismatch in their MOSFETs and finite output impedance due to which the charge pump current mismatch can not be reduced to null though it is under control in several architectures discussed in the previous section.

2.5.3 Leakage Current

The high impedance nodes of the loop filter are responsible for the leakage current that discharges the integrator capacitor. It occurs due to the reverse current of drain/source diffusion diodes and gate leakage in deep submicron CMOS FETs. As we design circuits near 100 nm technologies, the leakage current surfaces to a non-ignorable extent.

2.5.4 Delay in feedback loop

In mixed signal PLL circuits, the delay introduced due to the digital blocks in the feedback loop like buffer, divider and PFD produces a linear varying phase shift as a function of frequency where the phase shift is directly proportional to the operating frequency. Due to this the phase margin also degrades leading to unknown condition on the stability of the PLL. Further for large bandwidth PLL the feedback loop is always troublesome.

2.5.5 PLL sampling effect

PFD does not compare the phases of the reference and feedback signal continuously. Practically it is done only based on their edge position which makes the PFD a sampled data system. A hold process is thought of during the inactive time of the PFD when there is no signals to compare. A PLL phase sample and hold process introduces a phase lag in the feedback loop which degrades the PLL phase margin and again makes the stability questionable.

2.5.6 Failure of frequency divider during transient locking

In many PLLs operating in GHz range, the frequency divider operates around the maximum frequency allowed by the particular CMOS process, which leaves very little margin for peaking during the transient locking process.

It happens due to the damping factor less than unity and large phase difference between reference and feedback signal at the time when the frequency locking is achieved and the phase locking starts. Further if during the transient locking the maximum operating frequency of the divider is exceeded and it fails to provide an output edge, the PLL fails to lock and can not recover.

2.6 Conclusion

PLLs are well established and very widely used circuits in modern communication electronic systems. In this chapter recent PLL architectures have been discussed and their performances are analyzed. Various performance parameters have been compared for each category of design. It is observed that the faster locking capability along with low noise performance is significant which calls for innovations in design. Besides this, other performances like enhancement of lock range and power consumption minimization need to be carefully addressed. The important issues like dead zone minimization and simultaneous achievement of multiple performances have a wide scope of research. The designers in industry would immensely be benefited with the development of process variation tolerant circuit topologies. Finally a near optimal PLL can be designed by simultaneously optimizing the performances through computationally intelligent multi-objective optimization techniques.

Chapter 3

Efficient Technique for Low Power Fast Locking PLL Operating in Minimized Dead Zone Condition

---

3.1 Introduction

In the generic phase locked loop (PLL) [1], the phase frequency detector (PFD) generates two Up and Down signals in response to the input reference CK_{Ref} and feedback signal CK_{Out} as shown in Figure2.6. The noise contributed from the PFD modulates the Up and Down pulse widths [7] which creates a random component in the Charge Pump (CP) output current.

Three possibilities are considered here. The phase noise can modulate both the widths of both Up and Down pulses in same amount where CP produces no net output. The phase noise can also modulate the position of Up only, with respect to Down. But the most interesting part is when the phase noise

modulates the width of both Up and Down signals simultaneously. The random difference between the widths of Up and Down pulses raises the phase noise of the PFD. The phase noise is also related to the power supply noise in all the building blocks [95].

An ideal PFD should posses minimized dead zone [12,25,26], high frequency of operation and fast locking [25, 26] capabilities. As discussed earlier, the dead zone phenomenon severely affects the phase noise property, hence, it is very essential to minimize the dead zone in a PLL. This can be achieved by simultaneously activating the Up and Down outputs of the PFD for a fixed duration in each cycle when the PLL is locked. To achieve this, a fixed delay element in the reset path of the PFD is manually used. But it causes a periodic disturbance on the control voltage of the VCO leading to reference spurs in the PLL output spectrum. This is caused due to the mismatches in the pulse arrival time between the Up and Down signals to the charge pump.

In this work a novel voltage variable delay element (VVDE) [96] is incorporated in the PFD to minimize dead zone and hence the PLL phase noise. Use of this technique is seen to reduce the power consumption and the lock time to a great extent.

Following this introduction remaining part of this chapter is organized as follows. Section 3.2 describes the function of a simple PFD architecture and analyzes the effect of dead zone in PFD on phase noise of the PLL. The proposed technique to minimize the dead zone and yet offering fast locking is described in section 3.3. The post layout performance analysis is carried out in section 3.4 and section 3.5 draws the conclusion on the performance of the proposed PLL design.

3.2 The Phase Frequency Detector and Dead Zone in PLL

The flip flops in the simple PFD [11] generates Up and Down signals which switch the current of the charge pump as shown in Figure 2.8. Initially, both the outputs are low. At the rising edge of one of the PFD inputs, the corresponding output becomes high. This state is continued until the second input goes high. When both the outputs are high the circuit resets. Ideally the PFD characteristic is linear for the entire range of input phase differences from -2π to 2π. When the inputs differ in frequency [24], the phase difference changes each cycle by,

$$\Delta\varphi = 2\pi \left[\frac{\left(T_{CK_{Ref}} - T_{CK_{Out}}\right)}{max\left(T_{CK_{Ref}}, T_{CK_{Out}}\right)} \right] \tag{3.1}$$

Where $T_{CK_{Ref}}$ and $T_{CK_{Out}}$ are the time periods of the input reference signal and the output feedback signal from the divider circuit respectively.

The incoming reference and feedback signals decide whether the PFD will set or reset. When the PLL is near locked, the phase difference between the two input signals (reference and feedback)to the PFD is very small. In this condition if a rising edge from any of the signals is detected at the input of one of the flip flops (FFs) then the corresponding FF will set and the output (Up or Down) will take a finite amount of time to reach and switch on the current source of the charge pump. During this period if the second FF detects rising edge of the other input signal then that FF will set and makes the output high. Now both the output signals of the PFD will be high which causes a reset signal to be generated for both the FFs and disable the PFD for phase difference detection. This is the dead zone phenomenon due to which the PFD cannot detect the phase differences smaller than the dead zone and the PLL output fluctuates in this range causing a further increase in the overall phase noise [12].

For a conventional PLL having a divider in its feedback path, the phase

noise spectral density [8] is related to the divider ratio gain N as,

$$S_{\theta_{Out}}(f) = 8\pi^2 f_{CK_{Ref}} \Delta t^2 N^2 \frac{rad^2}{Hz} \tag{3.2}$$

where $N = f_{VCO}/f_{CK_{Ref}}$, f_{VCO} is the VCO output frequency and $f_{CK_{Ref}}$ is the PFD operating frequency, Δt is the phase offset between the two input signals of the PFD referred to as dead zone. Further the gain attenuation factor [26] of the PFD is, $\alpha = 1 - 2(\Delta t - T_D) - T_D^2$.

Thus,

$$\Delta t = \frac{1 - \alpha - T_D^2 + 2T_D}{2} \tag{3.3}$$

where T_D is the delay of the delay element normalized to one clock cycle. Now solving (3.2) and (3.3),

$$S_{\theta_{Out}}(f) = 8\pi^2 f_{CK_{Ref}} \left(\frac{1 - \alpha - T_D^2 + 2T_D}{2} N \right)^2 \frac{rad^2}{Hz} \tag{3.4}$$

The above expression for $S_{\theta_{Out}}$ reveals that there is a strong relationship between phase noise and the delay width of the delay element. Hence the dead zone poses to be a physical limit on the phase noise performance of the PLL. Alternatively speaking, one cannot reduce the phase noise below a certain limiting value without reducing the dead zone.

The dead zone reduction can be accomplished by inserting a fixed delay element with T_D delay in the reset path of the PFD [88]. But within this delay interval T_D, if the next rising edge of CK_{Ref} arrives, it will have no effect on Up signal, which results in an erratic behaviour, as the Up signal has already been activated. This is presented in Figure 3.1(a).

Furthermore if any rising edge of CK_{Ref} is detected within the high period of Reset signal as shown in Figure 3.1(b), it will also not have any effect on Up signal. In both the cases due to the absence of the rising edge of Up signal, the Down signal leads, causing a negative output, which increases the difference in CK_{Ref} and CK_{Out} in the form of phase and frequency, for phase difference

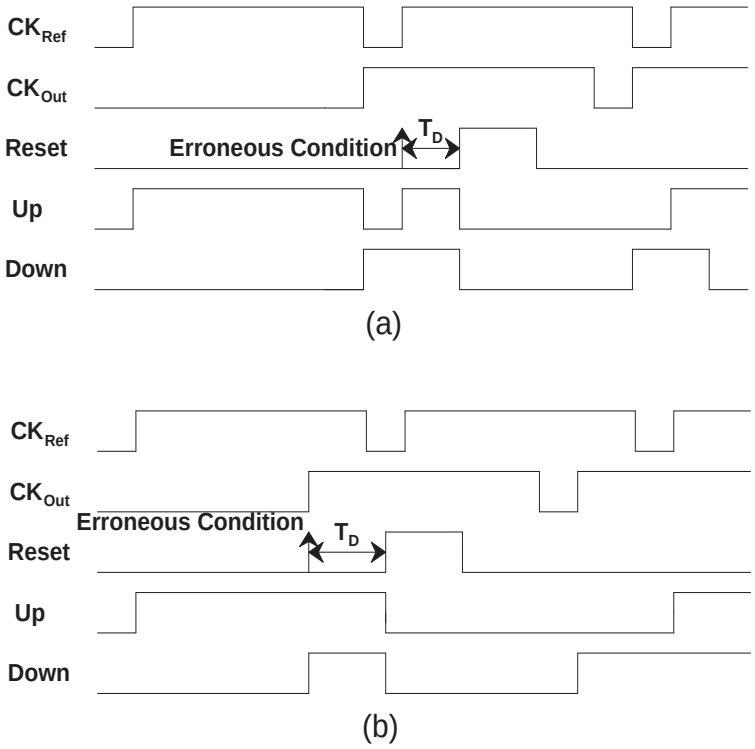

Figure 3.1: (a) Error during Reset delay (b) Error when Reset is active

higher than $2\pi - 2\delta$, where δ=$2\pi T_D/T_{CK_{Ref}}$ [88]. These erroneous effects yield wrong information about the phase or frequency difference thereby significantly reduce the performance of the PFD leading to performance degradation of PLL in turn. Another vital concern is that, in different applications of PLL, the input signals vary. With these variations in input signals a fixed delay element will not work effectively to minimize dead zone. If the fixed delay is larger than necessary, the reference spurs will be boosted. At the other extreme if the delay is less than the required value for the corresponding PLL, then it will initiate dead zone problem again. To alleviate this problem a variable delay in the Reset path is inserted which ensures the overall delay to be adequate satisfying the simultaneous requirement of low reference spur and minimum dead zone. The variable delay is controlled by one of the output signals of the PFD which makes it adaptive for the PLLs operating at different frequencies [12].

3.3 Variable delay element based PFD

A novel technique is proposed here to reduce the dead zone in PFD as well as phase noise of PLL. A novel structure having transistors $M_1 - M_6$, working as a Voltage Variable Delay Element (VVDE) shown in Figure 3.2, is incorporated in the PFD circuit which is similar to a dynamic two phase master slave pass transistor FF [24].

The cascaded inverting stages using MOSFETs $M_1 - M_4$ along with transistors M_5 and M_6 act as a variable delay element. The total delay can be modeled as equal to the combined propagation delays of the two inverting stages and the additional transistor delays. The propagation delay of an inverting stage depends on the time taken to charge or discharge the output node. Because of the nonlinear dependence of the charging or discharging current an exact computation of this delay is nontrivial. So an approximate mathematical expression is derived by considering average value of this current which is equal to the saturation current of the PMOS or NMOS transistor of the second inverting stage.

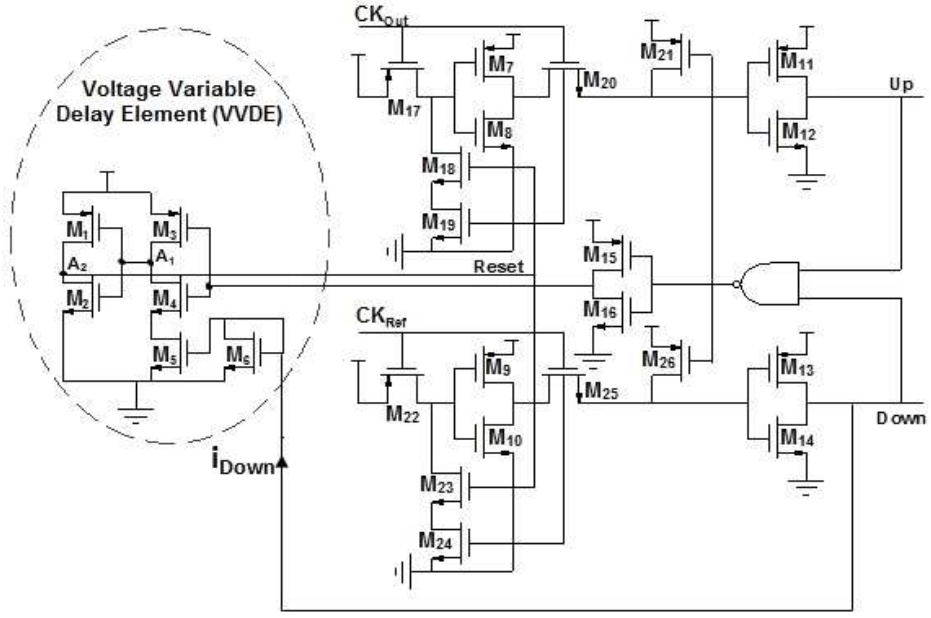

Figure 3.2: Proposed modified PFD with voltage variable delay element

Considering the short channel effect and assuming $V_{DD} \gg \left|V_{T_p}\right|$ *or* $|V_{T_n}|$ for the second stage, the average current can be expressed as,

$$\begin{aligned} I_{av} &= \tfrac{k_p}{2}\left(V_{GS} - \left|V_{T_p}\right|\right)^2 (1 + \lambda V_{DS}) \\ &= \tfrac{k_p}{2}\left(V_{DD} - \left|V_{T_p}\right|\right)^2 (1 + \lambda V_{DS}) \\ &\approx \tfrac{k_p}{2}(V_{DD})^2 (1 + \lambda V_{DS}) \end{aligned} \tag{3.5}$$

where λ is the channel length modulation coefficient. The high to low transition time t_{pHL} (similar analysis holds for low to high, t_{pLH}) can be derived as

$$\begin{aligned} t_{pHL} &= 0.69\tfrac{3}{4}\tfrac{C_L V_{DD}}{I_{DSat}} \\ &\approx 0.52\tfrac{C_L V_{DD}}{\frac{k_p}{2}(V_{DD})^2(1+\lambda V_{DS})} \\ &\approx \tfrac{C_L}{k_p V_{DD}(1+\lambda V_{DS})} \end{aligned} \tag{3.6}$$

Similarly estimating the propagation delay for the second inverter stage,

$$\begin{aligned} t_{p2} &= \tfrac{1}{2}\left(t_{pLH} + t_{pHL}\right) \\ &= \tfrac{1}{2}\left(\tfrac{C_L}{k_p V_{DD}(1+\lambda V_{DS})} + \tfrac{C_L}{k_n V_{DD}(1+\lambda V_{DS})}\right) \\ &= \tfrac{C_L}{2V_{DD}(1+\lambda V_{DS})}\left(\tfrac{1}{k_p} + \tfrac{1}{k_n}\right) \end{aligned} \tag{3.7}$$

Hence using (3.5) and (3.6), propagation delay of the second stage could be expressed as,

$$\begin{aligned} t_{p_2} &= \tfrac{1}{2}\left(t_{pLH} + t_{pHL}\right) \\ &= \tfrac{C_L}{2V_{DD}(1+\lambda V_{DS})}\left(\tfrac{1}{k_p} + \tfrac{1}{k_n}\right) \end{aligned} \tag{3.8}$$

This expression for t_{p_2} is subjected to an abrupt transition from V_{DD} to ground or vice versa.

However in the first stage of the delay element the current is controlled by a current mirror composed of M_5 and M_6. Here, when the voltage at Down node V_{Down} varies, the delay of the delay element changes. During the low to high transition of the input signal to the first stage, current at A_1 will be discharged through M_4 and the controlled transistor M_5 and the point A_2 of

the second stage will be charged through M_1. Therefore the total delay of the Reset signal is sum of the normal second stage delay and the controlled first inverter delay. The former delay is inversely proportional to the discharging drain current of M_4 or M_5. So the average current, referring to (3.5) can be approximated as the saturation current of the controlled NMOS transistor. The propagation delay of the first stage delay element becomes,

$$\begin{aligned} t_{p_1} &= \tfrac{1}{2}\left(t_{pLH} + t_{pHL}\right) \\ &= \tfrac{C_L}{2(1+\lambda V_{DS})}\left(\tfrac{1}{k_p V_{DD}} + \tfrac{V_{DD}}{k_n V_{Down}^2}\right) \end{aligned} \tag{3.9}$$

The typical value of channel length modulation coefficient (λ) is 0.02/V. As the power supply in this circuit is as low as 1.8 V the effect of channel length reduction will not be appreciable on overall performance of the circuit. Hence it can be neglected. Thus the total delay of the variable delay element can be expressed as,

$$\begin{aligned} t_{p,total} &= t_{p1} + t_{p2} \\ &= \left[\tfrac{C_L}{2(1+\lambda V_{DS})}\left(\tfrac{1}{k_p V_{DD}} + \tfrac{V_{DD}}{k_n V_{Down}^2}\right)\right] + \left[\tfrac{C_L}{2V_{DD}(1+\lambda V_{DS})}\left(\tfrac{1}{k_p} + \tfrac{1}{k_n}\right)\right] \\ &= \tfrac{C_L}{2}\left[\tfrac{\frac{1}{k_p}+\frac{1}{k_n}}{V_{DD}} + \left(\tfrac{1}{k_p V_{DD}} + \tfrac{V_{DD}}{k_n V_{Down}^2}\right)\right] \\ &= \tfrac{C_L}{2}\left[\tfrac{k_p k_n}{V_{DD}(k_p+k_n)} + \tfrac{1}{k_p V_{DD}} + \tfrac{V_{DD}}{k_n V_{Down}^2}\right] \end{aligned} \tag{3.10}$$

In the above relationships, $k_n = \mu_n C_{Ox}\left(\frac{W}{L}\right)_n$ and $k_p = \mu_p C_{Ox}\left(\frac{W}{L}\right)_p$, where μ_n and μ_p are the mobility of the electrons and holes in NMOS and PMOS respectively, C_{ox} is the gate oxide capacitance per unit area. $(W/L)_n$ and $(W/L)_p$ are the ratio between the channel width to length of NMOS and PMOS transistors respectively.

Equation 3.10 shows that the total delay of the delay element, $t_{p,total}$ is inversely proportional to V_{Down}^2. So, ultimately the current is controlled by the Down signal. When the voltage at Down node i.e. V_{Down} is more, the discharging will be faster and vice versa. Faster discharging will have a lesser propagation delay which is satisfied in (3.10). The second stage of the buffer is

a simple inverter. So the voltage at node A_2 has its normal rise and fall time.

3.4 Performance Analysis of Proposed PFD

The transistor sizes of the proposed PFD have been mentioned in Table 3.1 and the simulation of the complete PLL using this PFD was performed with supply voltage of 1.8 V. Except the proposed PFD, the PLL was constructed

Table 3.1: Design parameter values

Transistors	W/L Ratio (μm/ μm)
M_1, M_3, M_5, M_6	0.12/0.1
M_4	1.5/0.1
M_2	1.5/0.12
$M_7 - M_{16}$	3.3/0.1
$M_{17} - M_{26}$	1.1/0.1
Transistors of NAND Gate	1.1/0.1

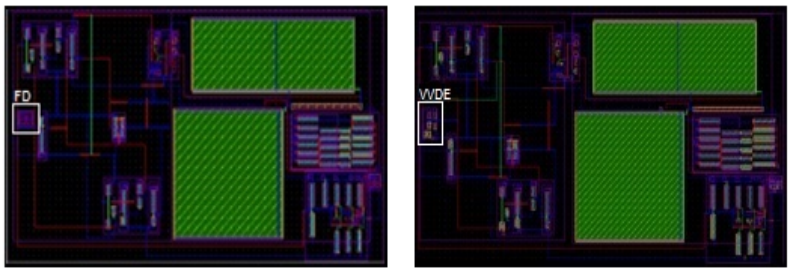

Figure 3.3: Layout of the PLL (a) with fixed delay element (b) with variable delay element

using charge pump [11] and CSVCO. The circuit was simulated in Cadence Specter RF using CMOS 90nm technology. The physical layout of the PLLs using the PFD with a fixed delay element and proposed PFD are shown in Figure 3.3(a) and 3.3(b) respectively. Transient analysis of the delay element is presented in Figure 3.4. Here the voltage transitions at each node of the

delay element are shown. The variation of the propagation delay with the voltage V_{Down} is shown in Figure 3.5. Here both the estimated and simulated total delay is seen to be increased with decrease in voltage levels of V_{Down}. The difference between the estimated and the simulated delay is around 10 ps which is due to the exclusion of delay of the transistor M_6 in (3.7) and (3.8). In Figure 3.6 the varying dead zone with the delay of the delay element is plotted. From this plot it is observed that lowering delay, the dead zone gets minimized. If the delay is decreased further then the PLL will not lock.

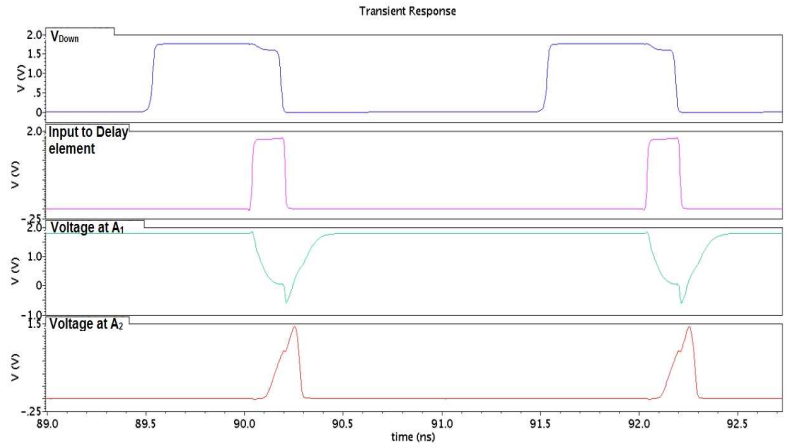

Figure 3.4: Voltage at different nodes of the delay element

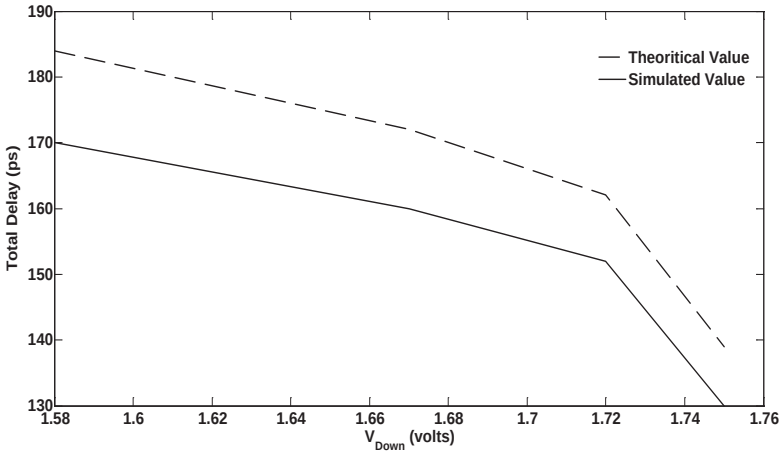

Figure 3.5: Variation of propagation delay with down signal

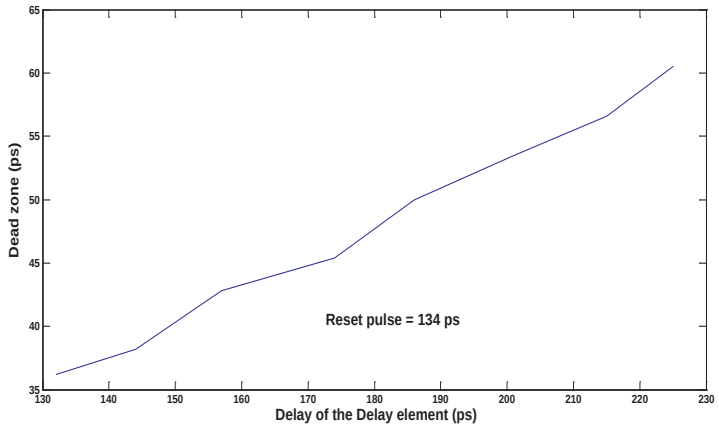

Figure 3.6: Variations of the dead zone with delay element

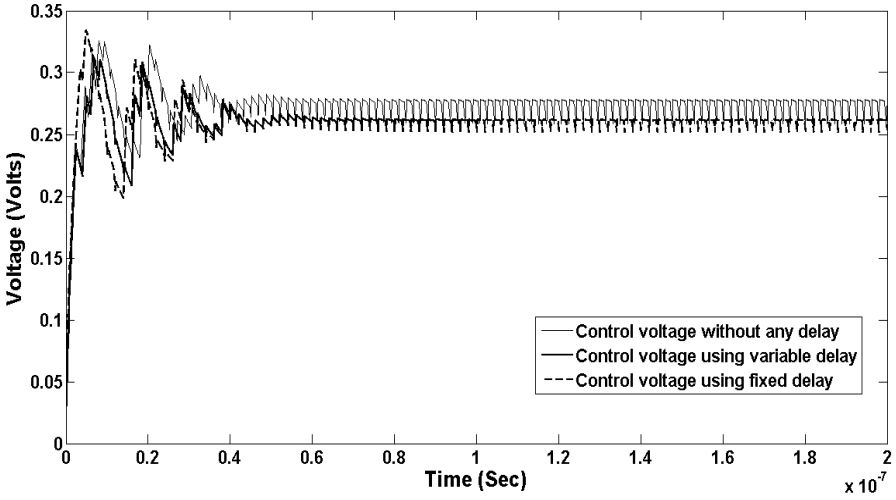

Figure 3.7: Transient variations of the control voltages

Since the passive elements like R and C [12] are not required in this technique, the PLL consumes lesser area. The transient variations in the control voltage of the VCO for the PLLs having no delay, fixed delay and variable delay PFDs are demonstrated in Figure 3.7. Further the transient response of the inputs of the PFD and VCO output are shown in Figure 3.8. In this case the perfect locking of the reference input and feedback signals of the PLL is observed. From the power consumption plot Figure (3.9), the average power of the PLL is estimated to be 1.74 mW.

Table 3.2: Summary of performance parameters of the PLL using different PFD architectures

Parameters	Fast Frequency acquisition PLL OF 1 GHz Range		
	Without delay element PFD [24]	With fixed delay PFD	With proposed VDE
Technology (nm)	90	90	90
Frequency (GHz)	1	1	1
V_{DD} (Volts)	1.8	1.8	1.8
Lock range(GHz)	0.5-1.9	0.4-3.2	0.8-2.5
Lock in time(ns)	220	55	50
Phase noise (dBc/Hz @1 MHz offset)	-91.74	-103.9	-110.5
Reference spur (dBc/Hz @500 MHz offset)	-73.0	-85.5	-92.9
Power consumption (mW)	3.43	1.39	1.74
Layout area(μm^2)	2720	2736	2862
Dead zone (ps)	330	80	36

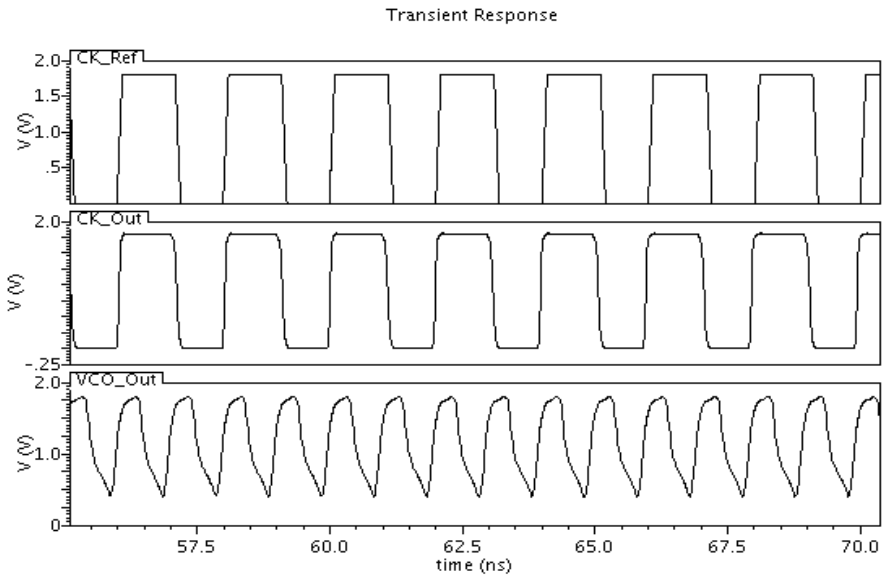

Figure 3.8: Transient response of the inputs of the PFD and VCO output

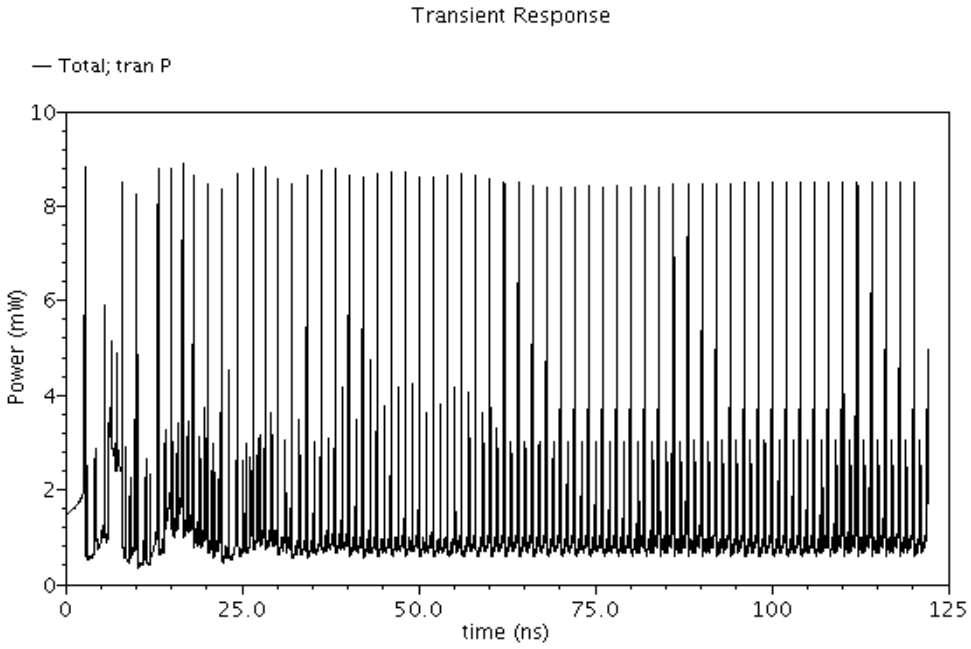

Figure 3.9: Total power consumption plot of the PLL

The phase noise at different offset frequencies has been plotted in Figure 3.10. It is observed that there is around 10% improvement in the phase noise of the PLL when the VVDE based PFD is used in place of the fixed delay based PFD.

Simulations studies are carried out on a PLL without delay in the reset path of the PFD proposed by Mansuri et. al [24] in 90 nm technology. Then fixed delay and variable delay elements are inserted in the reset path. The performance parameters are compared in Table 3.2. Apart from the phase noise improvement the proposed circuit is observed to lock faster and also consumes less power. The reference spur is also measured to be -92.9 dBc/Hz at 500 MHz of offset frequency which is around 10% better than the fixed delay PFD. This is achieved at the cost of silicon area and reduced lock range.

Figure 3.11 reveals that the dead zone using the proposed technique has been improved from others, including a conventional latch based PFD [24], with the use of a delay cell [25, 97] and with the use of two extra transistors [26]. Simulation of the proposed PFD and comparison of performance with other

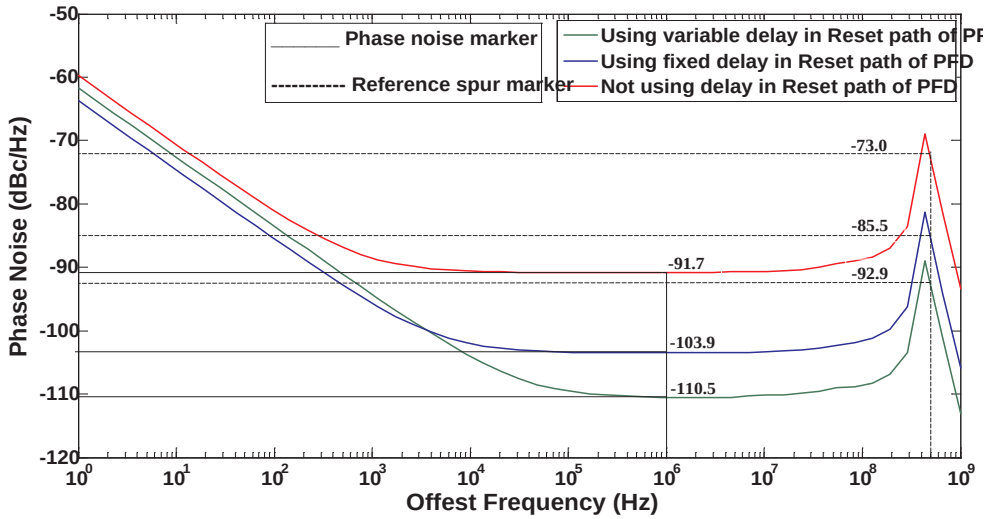

Figure 3.10: Phase noise of the PLL using different techniques in PFD

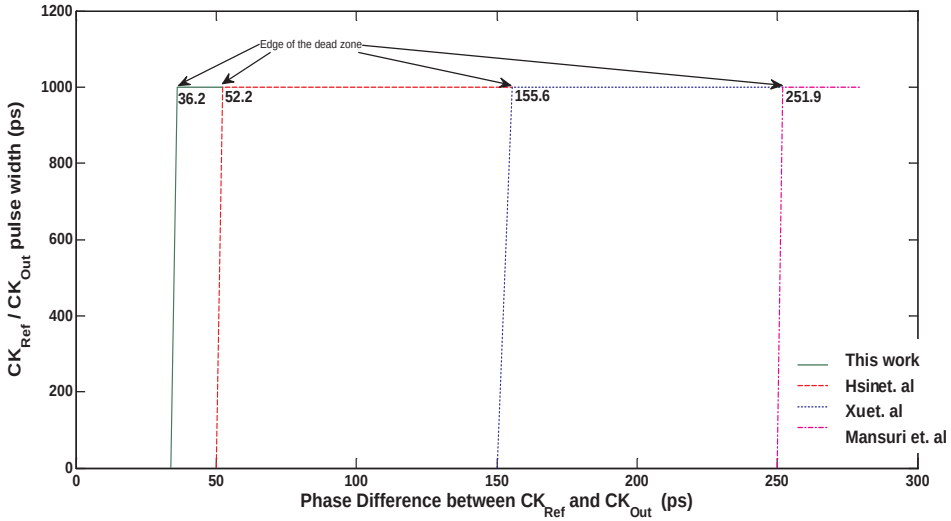

Figure 3.11: Simulated Dead zone of four different PFDs

Table 3.3: PLL performance comparison using different PFD architectures

Parameters	Chen [26]	Xiaoliang [97]	Hu [25]	This work
Technology (nm)	130	130	500	90
VDD (Volts)	1.2	1.2	5	1.8
Lock in time(ns)	-	2000	140	50
Max. Frequency (GHz)	2.9	1.5	0.8	2.5
Dead zone (ps)	52	-	-	36
Phase noise (dBc/Hz @ 1 MHz offset)	-	-96.2	-	-110.5
Power Consumption (μW)	0.496 @ 128 MHz	25 @ 1 GHz	-	1 @ 500 MHz

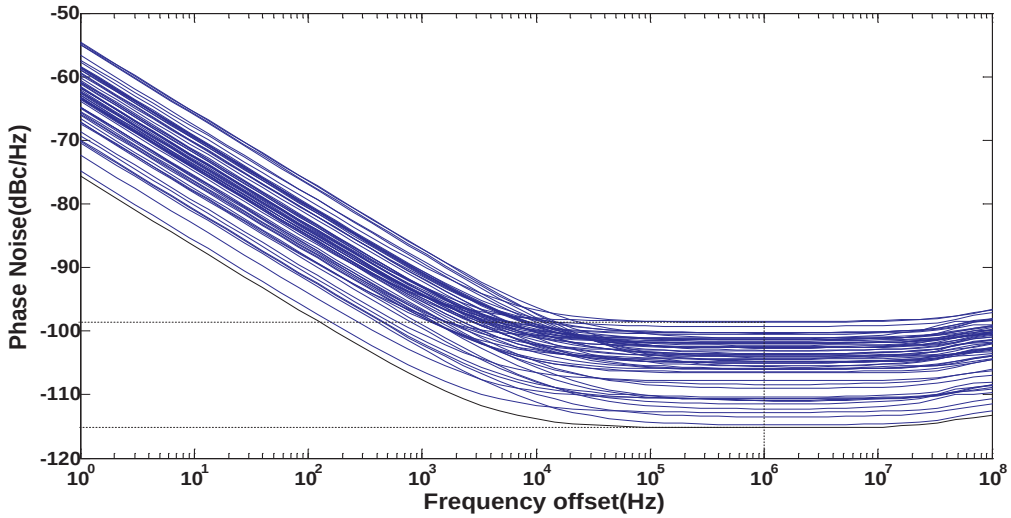

Figure 3.12: Monte Carlo simulation for Phase Noise

recent designs show that, with an acceptable value of power consumption the dead zone performance is better than the others which is presented in Table 3.3. As reported by Mahapatra et al. [98], the extra power consumption can be attributed to additional diffusion capacitance of the controlled transistor (M_5) that contributed to the total load capacitance.

To measure the phase noise in a worst case scenario the threshold voltage of the devices is subjected to a 10% variation. Based on this, the Monte Carlo simulation is performed for 100 iterations as (Figure 3.12) from which it is observed that the phase noise varies in the range -98.2 dBc/Hz to -116 dBc/Hz at 1 MHz offset confirming the variation of phase noise to be limited with threshold voltage variation.

3.5 Conclusion

A PLL incorporating a PFD having a voltage variable delay element in its reset path is proposed in this chapter. This technique reduces the dead zone, resulting in better phase noise performance. The lock in time and lock range are also reported for this design. The lock in time of the PLL is much less than

the PLL without using any delay whereas the lock range is found to be little less compared to the PLL using fixed delay PFD. The designed PLL having the proposed PFD achieves a phase noise of -110.5 dBc/ Hz at 1 MHz of offset frequency which is better as compared to the other similar designs. With this superior phase noise performance the power consumption is also found out to be 1.74 mW at the cost of 5% extra physical area. The PFD architecture and the parameters of the charge pump and loop filter mainly influence the lock time. So by proper selection of PFD and adjusting the charge pump current and the loop filter component values, a better lock time is achieved. The comparison between these parameters demonstrates that the proposed circuit can achieve better performance with an acceptable reduction in lock range and increase in physical area.

Chapter 4

Adaptive PFD Selection Technique for Low Noise and Fast PLL

4.1 Introduction

Integration of new generation mobile systems with the existing ones exemplifies the demand for multi standard radios on a single chip. This request brought a great challenge for the design of PLLs which are used as local oscillator and synchronizer in the mobile radio communication systems. PLL also finds applications in development of cellular handsets in different wireless communication standards. It is highly challenging to design PLL suitable for varied applications with difference in the specification requirement. In Global System for Mobile communication (GSM) applications, lock time is of paramount importance than the phase noise [24]. However in high frequency applications like Worldwide Interoperability for Microwave Access WiMAX, PLLs demand ultralow phase noise and jitter [99]. A comprehensive noise formulation of the overall PLL is highly desired for performance analysis.

Reduction of phase noise and jitter performance in individual PLL com-

ponents were analyzed by Lee et al. [100]. The timing jitter can be reduced adopting a disintegrated phase and frequency detection technique [101]. Initially during the locking process the frequency locking loop detects the frequency difference and drives the charge pump accordingly and the control signal is tuned so that the frequency of the divided signal will approach that of the reference. However the frequency detection loop is stopped when both the signals lock with respect to their frequencies. This helps to eliminate timing jitter due to the frequency detection loop. The PFDs are selected arbitrarily by a random clock generator to reduce the reference spur level of the PLL [48]. Using a sequential PFD and a pre-charge PFD an unlimited error detection range, high frequency of operation and fast frequency acquisition could be achieved in [49]. An additional phase error detector (PED) is designed in [50] to reduce both the power consumption and locking time of the PLL. To cater to the diversified requirements, multi PFD architectures are suitable. Some of the high performance multi PFD architectures were discussed in Chapter 2. A dynamically selected multi PFD architecture simultaneously offering maximal performance is always required to fit into multi standard communication applications.

The PLL design of this chapter has the following novel features.

i. An analytical model of phase noise and settling time for the overall CP-PLL is presented.

ii. A dual PFD architecture is proposed where the PFD is adaptively selected to offer low noise and fast locking capability.

iii. The proposed PLL can be used over a wide range of communication standards enabling variety of applications.

iv. The lock range of the PLL has been markedly enhanced.

v. The PLL consumes less power in comparison to other multi-PFD architectures [48–50].

vi. It is observed that the peak to peak jitter doesnt vary much over a wide range of temperature and in all fabrication process corners.

Following this in section 4.2, analytical modeling of phase noise and settling time of the charge pump PLL is carried out. Section 4.3 presents a comprehensive view of the low noise and fast PFD architectures. The architectural details of the proposed PLL is demonstrated in section 4.4. Performance analysis of the proposed PLL is carried out in section 4.5. Section 4.6 provides the concluding remarks of the chapter.

4.2 Phase noise and settling time analysis of a charge pump PLL

To explore the noise property of the complete PLL it is necessary to estimate the noise property of the PLL building blocks and take their combined effect. A simplified phase domain block diagram of the proposed PLL is exemplified in Figure 2.1 for the analysis of noise properties.

For a second order passive lead lag low pass filter [4] the closed loop transfer function of the PLL is given by,

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{K_{PFD}F(s)K_{VCO}}{N.s + K_{PFD}F(s)K_{VCO}} \tag{4.1}$$

where θ_{out} and θ_{in} are phase of the output and input signals of the PLL respectively, N is the divide ratio in the feedback path of the PLL, K_{PFD} is the gain of the PFD equated to $I_{CP}/2\pi$, where I_{CP} is the charge pump output current, K_{VCO} is gain of the VCO expressed as $\frac{\mu_n C_{Ox} W_n (V_{Cont} - V_{TH})}{n L_n C_L V_{DD}}$, where n is the number of inverter stages, V_{Cont} is the input control voltage, V_{TH} is the threshold voltage of the NMOS used, C_L is the effective load capacitance, W_n is the width of NMOS and L_n is the length of the NMOS in the VCO. The transfer function [102] of the second order low pass filter (LPF) Figure (2.10)used in the PLL can be expressed as,

$$F(s) = \frac{s + \frac{1}{\tau}}{sC_2\left(s + \frac{1}{\frac{\tau C_2}{C_1+C_2}}\right)} \tag{4.2}$$

where τ = R .C_1, where R is the resistor and C_1, C_2 are the capacitors used in the filter. Now the combined transfer function of the PFD and LPF can be written as,

$$K_{PFD}F(s) = \frac{I_{CP}}{2\pi C_1}\frac{s + \frac{1}{\tau}}{sC_2\left(s + \frac{1}{\frac{\tau C_2}{C_1+C_2}}\right)} \tag{4.3}$$

From (4.1) and (4.3), the transfer function of the PLL is,

$$H(s) = \frac{\left(s + \frac{1}{\tau}\right) I_{CP}K_{VCO}}{2\pi sC_2\left(s + \frac{1}{\frac{\tau C_2}{C_1+C_2}}\right) N.s} \tag{4.4}$$

For a large reference frequency most of the noise is contributed by the VCO and dominated by $1/f^2$ noise. So for a noisy VCO considering n_0(s) as the VCO input noise, the closed loop transfer function of the PLL is derived as,

$$H(s) = \frac{\theta_{out}(s)}{n_0(s)} = \frac{C_1N\left(s + \frac{1}{\tau}\right) K_{VCO}}{sC_2\left(s + \frac{1}{\frac{\tau C_2}{C_1+C_2}}\right) N.s} \tag{4.5}$$

Calculating the power spectrum density of θ_{out}(s),

$$S_{\theta_{Out}}(\omega) = |n_0(j\omega)|^2 \left|\frac{C_1N\left(j\omega + \frac{1}{\tau}\right) K_{VCO}}{j\omega C_2\left(j\omega + \frac{1}{\frac{\tau C_2}{C_1+C_2}}\right) N.j\omega}\right| \tag{4.6}$$

$$= \frac{N_0}{2}C_1^2N^2\left[\left(\omega^2 + \frac{1}{\tau^2}K_{VCO}^2\right)\Big/\omega^2C_2\left(\omega^2 + \frac{1}{\frac{\tau^2C_2^2}{(C_1+C_2)^2}}\right) N.\omega^2\right| \tag{4.7}$$

where ω is the offset frequency at which phase noise is to be estimated, $N_0/2$ is the power spectral density of the VCO input noise. N_0=FkT/P, where F is the

noise figure of the active device which is less than -130 dBc/Hz at 1 MHz offset, k is the Boltzmanns constant, T is the absolute room temperature and P is the power at the input of the VCO i.e. the product of charge pump output current and control voltage of the VCO. Further considering the damping constant $= I_{CP}K_{VCO}$R/2N, the settling time t_s [103] is approximated as,

$$t_s \approx \frac{10}{\gamma} = \frac{20N}{I_{CP}K_{VCO}R} \tag{4.8}$$

4.3 Low noise and fast PFD architectures

Noise effect is an important issue in high frequency applications especially in the gigahertz range. A calibrated PFD where a feedback from the charge pump controls the delay length of a variable delay element used in the reset path is designed Charles et al. [12]. In this design the feedback signal ensures the total PFD delay to be positive, eliminating the possibility of a dead zone while minimizing the phase noise. A 1 GHz PLL using this PFD generates a phase noise of -102.7 dBc/Hz at 1 MHz offset frequency when designed in 90 nm technology. Another PFD architecture described by Hu et al. [25] is reported to achieve zero blind zone at high operating frequency. The reset process is avoided when the phase difference is in the range of π to 2π. For a 1 GHz PLL using this PFD [25] a phase noise of -104.9 dBc/Hz at 1 MHz offset is estimated in 90 nm technology. For a carrier frequency of 7.92 GHz a pre-charge PFD is designed for the PLL [37] where the phase noise is reported to be -109.6 dBc/Hz at 1 MHz offset using 180 nm technology. Among the above discussed PFDs, PFD designed by Tak et al. [37] offers a very low phase noise performance.

Usually some delay is inserted in the reset path to reduce the dead zone of a PFD which decreases the overall phase noise of the PLL. However this technique reduces the effective range of phase comparison to less than 2π. The PFD will generate a false control signal when the phase error is larger than

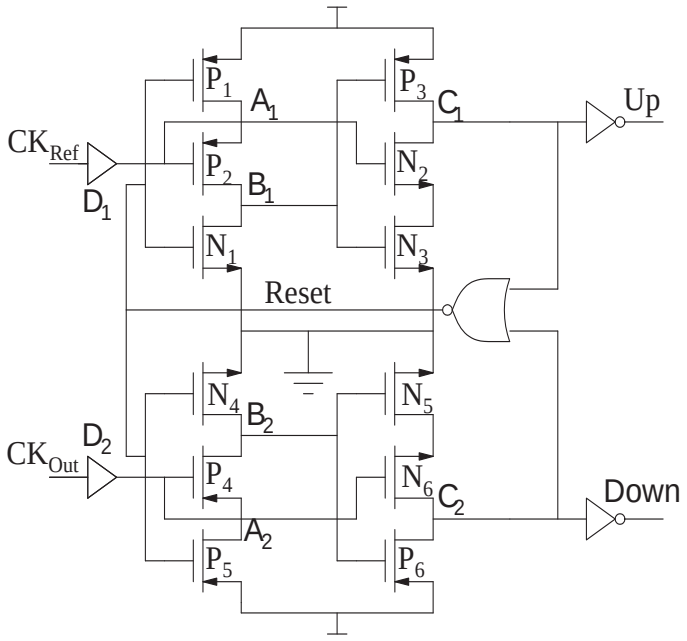

Figure 4.1: Low noise PFD architecture [37]

2π-Δ, where Δ=$2\pi t_{reset}/T_{CK_{Ref}}$. The t_{reset} refers to the reset path delay and $T_{CK_{Ref}}$ to the reference signal time period. The feedback signal frequency does not approach the lock range due to the above created error in the control signal. Increase in reference frequency enhances Δ to more than π, which increases the settling time and this does not guarantee phase lock.

To address this issue a modified pre-charge PFD [37] as shown in Figure 4.1, is considered for our PLL. In this case the phase noise reported is considerably low. To improve the phase noise performance, two buffers (delay stages) D_1 and D_2 are used in this PFD. Even when the phase difference of the two input signals is close to 2π this PFD generates the control signals effectively. It has the advantage of low power consumption and higher accuracy as compared to the design made by Mansuri et al. [24].

Rising edge of CK_{Ref} discharges C_1 through N_2 and N_3 making Up high. Similarly rising edge of CK_{Out} discharges C_2 through N_6 and N_5 which makes Down high. Now when both the input signals gets rising edge simultaneously, the reset signal will transit from low to high. A high reset discharges B_1 to

ground through N_1 which is the input of P_3. Now getting negative edge at input P_3 charges C_1 to high again which makes Up low. Similarly the reset signal discharges B_2 to ground making a high to low transition at the input of P_6. This consequently charges C_2 and makes Down signal low again.

Fast PFD architectures are necessary in modern communication systems for rapid frequency acquisition capability. The PFD designed by Mansuri et al. [24] is a dynamic two phase master slave pass transistor flip flop. The asynchronous and synchronous reset are generated for slave and master flip flop respectively which enhances the operating range. The reset signal propagates through one pass transistor, an inverter and a NAND gate. The smaller gates in reset path reduce the reset time to a great extent. When simulated in 90 nm technology this architecture provides a lock in time of 120 ns for 2.5 GHz operating frequency.

A novel multi state PFD with variable gain which can efficiently reduce the lock time is described by Yau et al. [104]. The architecture is decomposed into two sections. The first section has a conventional D flip flop based PFD and the second is included with two extra PFDs and six OR gates. At 400 MHz operating frequency this architecture provides a lock in time of 200 μs in 350 nm technology. Another fast PFD based on the conventional design using NAND gates is represented by Homayoun et al. [7]. This PFD has a very fast locking capability of 190 ns for 2.5 GHz operating frequency in 90 nm technology. Out of the above discussed fast PFDs, the PFD designed by Mansuri et al. [24] has been reported to have fastest locking property.

This PFD is presented in Figure 4.2 and is similar to a dynamic two phase master slave pass-transistor flip-flop [24]. When both up and down outputs become high, the slave is reset asynchronously while the master is reset synchronously, i.e. the reset is allowed only when the slave latch is transparent. The operating range is increased and the power consumption is reduced by synchronously resetting the master. While it is transparent, if the master latch is reset then there will be significant short-circuit current, resulting in more

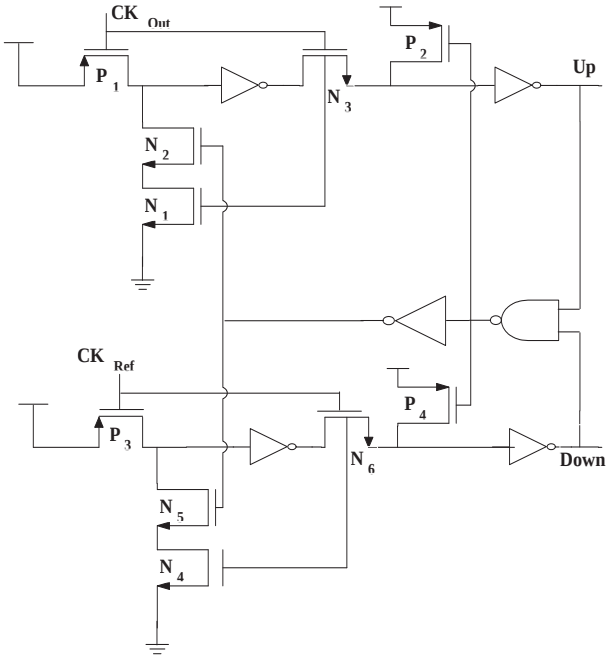

Figure 4.2: Fast PFD architecture [24]

power. One pass transistor, one inverter and one NAND gate are incorporated here in the reset path that effectively reduces the reset time.

4.4 Adaptive PFD selection for low noise and fast PLL

A novel PLL architecture with combined characteristics of low noise and fast acquisition is proposed which is shown in Figure 4.3. Two different PFDs (fast and low noise) are dynamically included in the PLL operation loop. At any instant of operation of the PLL, a PFD is adaptively selected by using a lock signal generated from the proposed PFD selector circuit. In the initial phase of operation when the PLL is not locked the PFD selector circuit selects the fast PFD and the low noise PFD remains out of the loop. In the locked phase of the PLL, the low noise PFD becomes active. This technique assists the PLL to achieve fast frequency acquisition and low phase noise. The reported

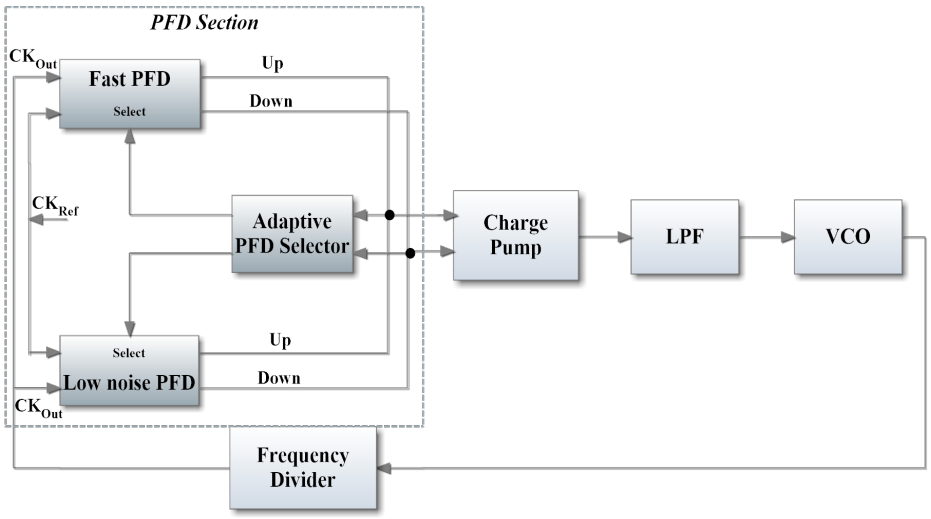

Figure 4.3: Adaptive PFD selection for PLL architecture

fast PFD [24] and low noise PFD [37] circuits discussed in previous section are considered for the proposed PLL design.

In the proposed PLL, unlike other dual PFD architectures [48,49], only one charge pump is used which help to improve the speed performance reducing the silicon area. The use of more than one charge pump, the Up and Down current mismatch increases which results in more reference spur generation at the output of the PLL. This issue has been resolved in the proposed single charge pump multi PFD PLL circuit. The primary contribution of the work lies in the inclusion of the adaptive PFD selection block. The proposed adaptive PFD selection block is depicted in Figure 4.4.

For making fast decision to select a PFD, a pre-amplifier (composed of $P_4 - P_7$ and $N_4 - N_5$ transistors) helps in the case of small differential input voltage and hence is a part of the comparator. A decision circuit (composed of $N_6 - N_10$ transistors) that produces proper 0 or 1 is necessary to select the PFD. A high speed comparator unlike the design by Woo et al. [49] is used to assist the fast selection of PFD. The proposed adaptive PFD selector takes nearly 64 ps to activate the desired PFD in contrast to the design by Woo et al. [49] that takes 200 ps for the same purpose. When the PLL is locked, the

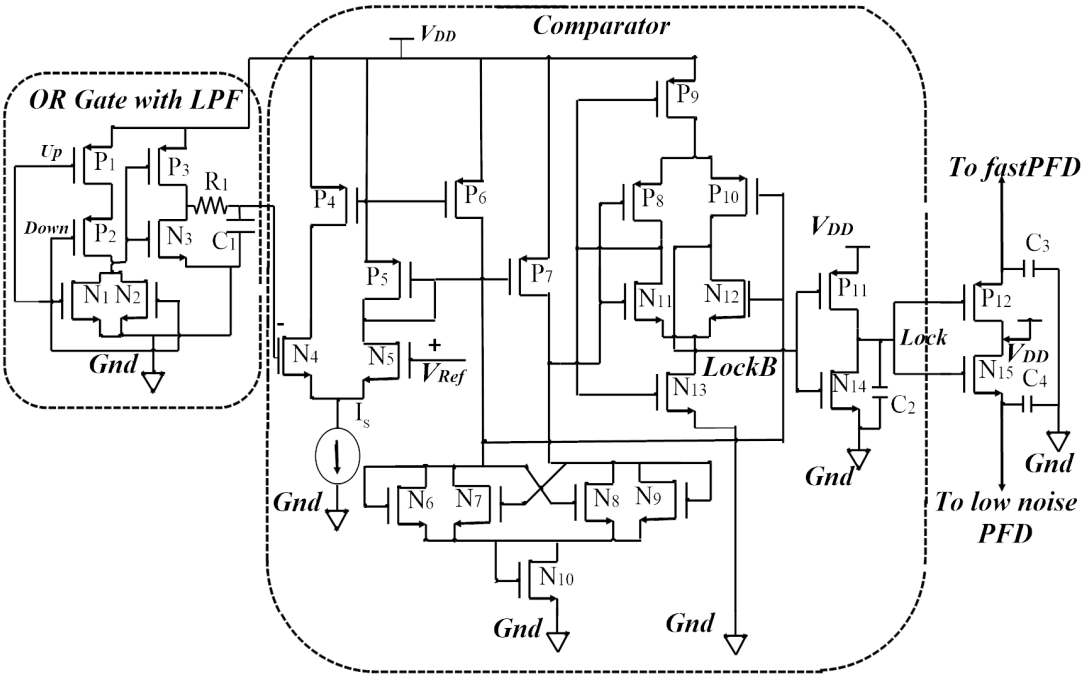

Figure 4.4: Proposed Adaptive PFD selector

Up and Down signals fed to the OR gate comprising of P_1-P_3 and N_1-N_3 are narrow pulses. These are rejected by suitably choosing the LPF components of C_1 and R_1 to be 0.377 pF and 210 Ω respectively. C_1 and R_1 values below this would be fail to suppress the ripples and beyond this simply increase the area. When the loop is unlocked the DC average values of the wider Up or Down pulses are fed to the negative input terminal of a comparator having P_4-P_{11} and N_4-N_{14} transistors. Monitoring the DC voltage at the output of LPF and setting the comparator with a reference trip point V_{Ref} of 50 mV (connected to positive input terminal of the comparator) the loop is determined to be whether in locked condition or not. Crossing the trip point to a higher voltage gives a low value 0 at the output of the comparator. This consequently detects the unlocked condition of the loop. Similarly crossing the trip point to a lower voltage detects the locked condition of the loop. Feeding the reference voltage to positive terminal of the comparator, reduces another inverter circuit which was used at the output of the lock detector in the design by Woo et al. [49]. When the PLL is out of lock condition during the initial phase of operation, the

Table 4.1: Geometrical aspect ratios of the transistors used in the proposed circuit

Transistors	**W/L (nm)**
P_1 - P_{12}	120/100
N_1-N_3, N_6-N_9, N_{11}-N_{15}	120/100
N_4 - N_{15}	500/100
N_{10}	1200/100

fast PFD is activated by receiving a low input Lock from the PFD selector to the PMOS P_{12}. In the second phase of the operation when the PLL is locked there will be a high Lock output making NMOS N_{15} ON and consequently activating the low noise PFD. Capacitors C_2 of 3.016 pF, C_3 and C_4 of 7.23 pF are used to minimize the fluctuations at corresponding branches and to make P_{12} and N_{15} work properly without contributing any noise to the system. The transistor aspect ratios taken in the design are mentioned in Table 4.1. Since the PFD selecting MOSFETS P_{12} and N_{15} are of very low aspect ratios, the voltage drop across these MOSFETs are observed to be negligible.

The circuit design parameters are R= 2.54 KΩ, C_1=3.2 pF, N=2, and K_{VCO}=2.5 GHz/V. The charge pump current I_{CP} are 66.6, 39.5 and 65.3 μA for PLLs having fast, low noise and dual PFD architecture respectively.

Considering the actual parameters of our design, the phase noise of the PLLs using Fast, low noise and dual PFD architectures are estimated from (4.7) and compared with the Cadence specter RF simulated values. It can be observed from Figure 4.5 that there is only difference of around 2 to 4 dB between the calculated and simulated phase noise of the PLLs. The lock time values among the different PLLs are compared in Figure 4.6.

4.5 Performance analysis of the proposed PLL

The PLL using the proposed technique is designed and simulated in Cadence Specter RF using 90nm technology. The physical layout of the proposed PLL is shown in Figure 4.7. The transient analysis of the complete PLL with

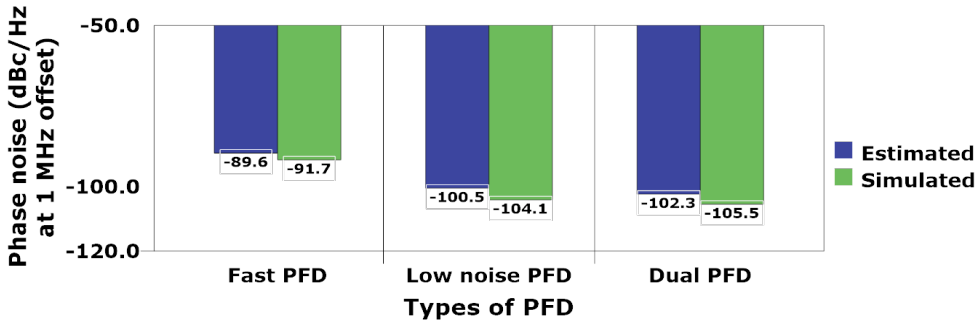

Figure 4.5: Estimated and simulated Phase noise of the PLL using different PFDs

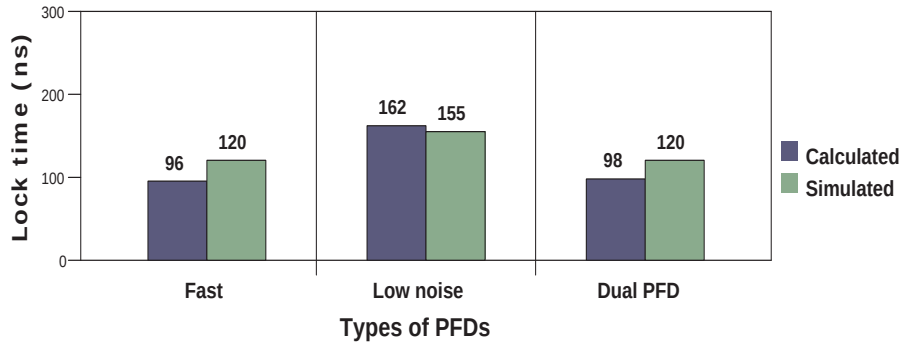

Figure 4.6: Estimated and simulated lock time of the PLL using different PFDs

the voltage at each node of interest is demonstrated in Figure 4.8. Here it is observed that the PLL is locking in 120 ns. Within this time, as the width of Up is relatively more, the *LockB* is high showing unlocked condition of the PLL. To enhance the locking speed before the PLL locks, power supply to the fast PFD is high. But in the second phase of the PLL operation after locking, when the control voltage (V_{Cont}) gets stabilized power supply for the fast PFD switches to low and for low noise PFD to high. This switching activity is possible due to the proposed adaptive PFD selector. Compared to the conventional PLL this design provides 50% less lock time.

The average power consumption of the PLL is estimated to be 1.2 mW from Figure 4.9. From the phase noise plot (Figure 4.10 and 4.12), the proposed design exhibits 15% better phase noise than the conventional design.

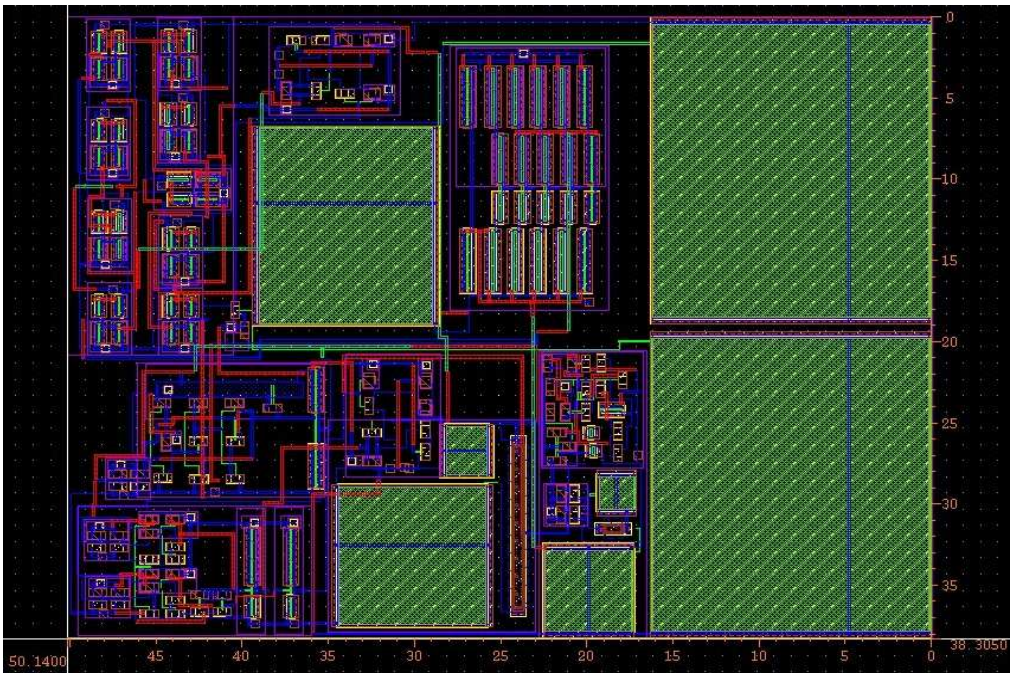

Figure 4.7: Complete layout of the PLL using adaptive multi PFD selection

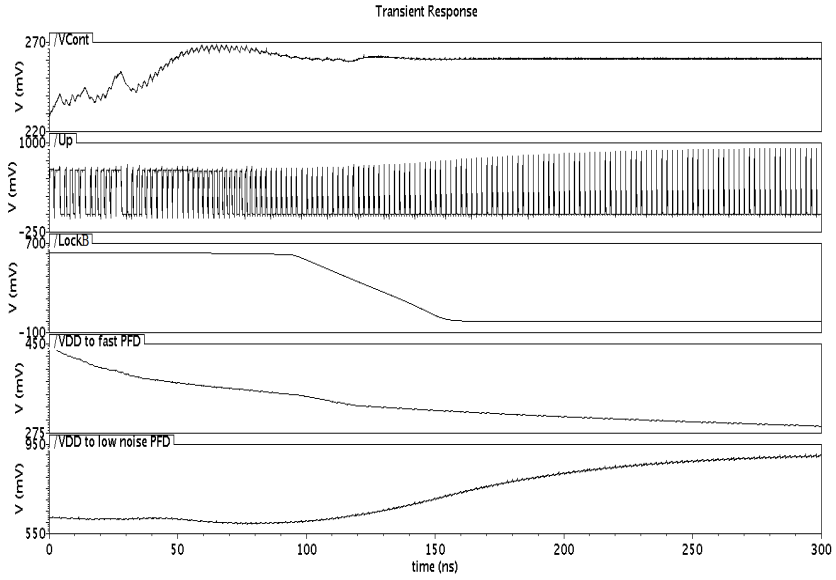

Figure 4.8: Transient analysis at different nodes of interest of the PLL

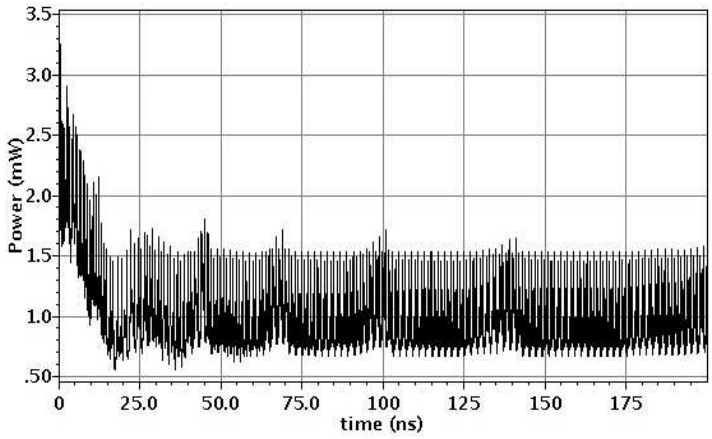

Figure 4.9: Power consumption plot of the PLL

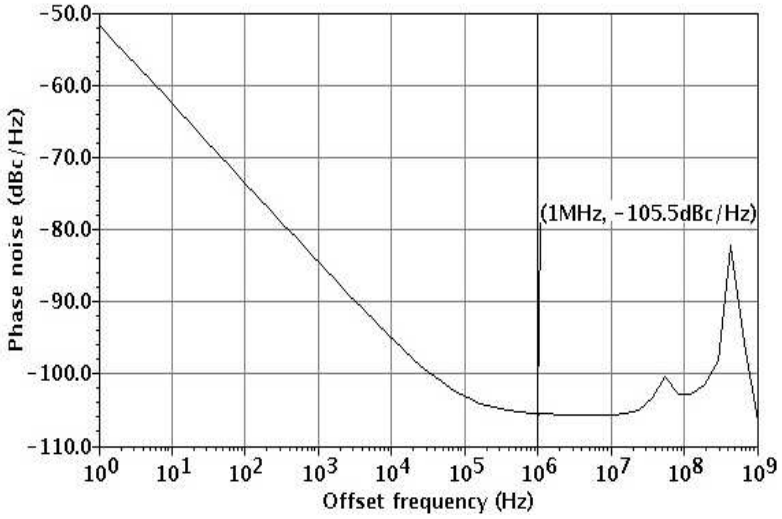

Figure 4.10: Phase noise variation plot of the PLL

Compared to the fast PFD [24] this dual PFD architecture has 15 dB improved phase noise. But if it is compared with the low noise PFD it has only 4 dB more phase noise. However this is affordable due to the fast locking capability of the PFD and in view of the objective of our design. To observe the impact of process and mismatch variations at four distinct temperatures, Monte Carlo simulations for 50 iterations showing phase noise variation when threshold voltage is varied by 5%, are demonstrated in Figure 4.11. Both the intra-die and inter-die process variation flags are set during the simulation. In-

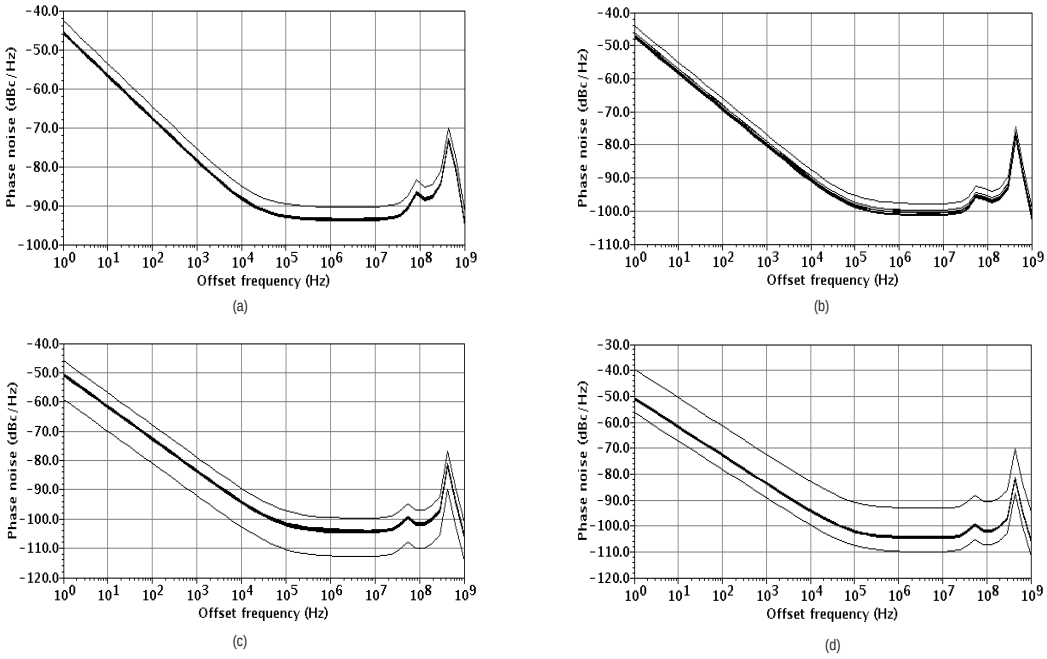

Figure 4.11: Monte Carlo simulation for phase noise at different temperatures. (a) -40^oC, (b) 0^oC, (27^oC, (d) 50^oC

dustry standard transistor and process variation foundry models are used for all simulations. For temperatures at -40^oC, 0^oC, 27^oC, 50^oC, the phase noise variations are estimated to be 4, 6, 13 and 18 dBc/Hz respectively at 1 MHz offset frequency. Consequently it is observed that with the rise in temperature the ranges of phase noise variation at different threshold voltages increases. However it is also observed that even at large temperature variation the phase noise doesnt go beyond -90 to -112 dBc/Hz at 1 MHz offset frequency.

The phase noise of the proposed PLL is compared with the conventional PLL and plotted in Figure 4.12. At different process corners NN, SS, SF, FS, FF, performance parameters of the PLL like phase noise, lock in time and power consumption are depicted in Table 4.2. The phase noise is measured to be best in FF and worst in SS corner. There is no significant variation in the power consumption across all the corners. However fast locking is achieved in SS corner.

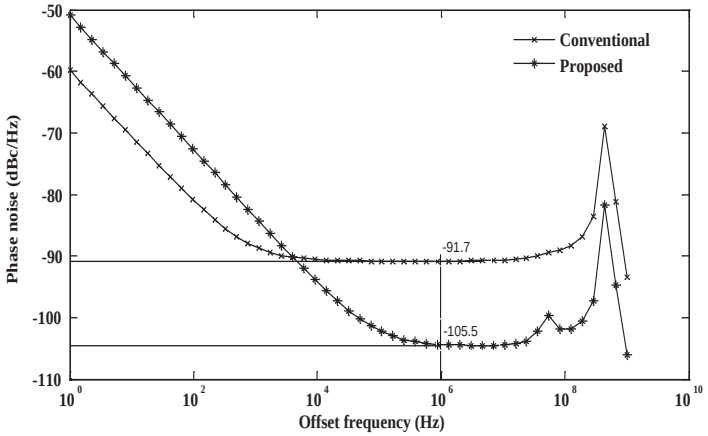

Figure 4.12: Phase noise comparison between the conventional and proposed PLL

Table 4.2: Performance summary of PLL at different process corners

Corner	Phase noise (dBc/Hz at 1 MHz offset)	Lock time (ns)	Power Consumption (mW)
NN	-105.5	120	1.2
SS	-98.4	80	0.9
SF	-101.1	90	1
FS	-103.7	100	1.1
FF	-110.1	90	1.6

Taking process variations into account all the performance parameters of the PLL are estimated at different temperatures ranging from -40^o to 50^o C and shown in Table 4.3. The power consumption has also a linear variation with temperature. With increase in temperature the average power consumption rises. Furthermore the lock time increases with increase in temperature.

At 2.5 GHz operating frequency, the output jitter is plotted in Figure 4.13. Here the peak to peak jitter is measured to be 24 ps which is only around 3% of one cycle of the output signal. Compared to that of conventional PLL (Figure 4.13a), the jitter produced in this work Figure (4.13b) is much improved. Due to this improved performance the finite transit time of the signal can be accepted. At different process corners and temperatures the jitter performance

Table 4.3: Performance summary of the PLL at different temperatures

Temperature (^{0}C)	Phase noise (dBc/Hz at 1 MHz offset)	Lock time (ns)	Power Consumption (mW)
-40	-93.8	60	0.9
0	-100.9	80	0.9
27	-105.5	120	1.2
50	-110.6	140	1.6

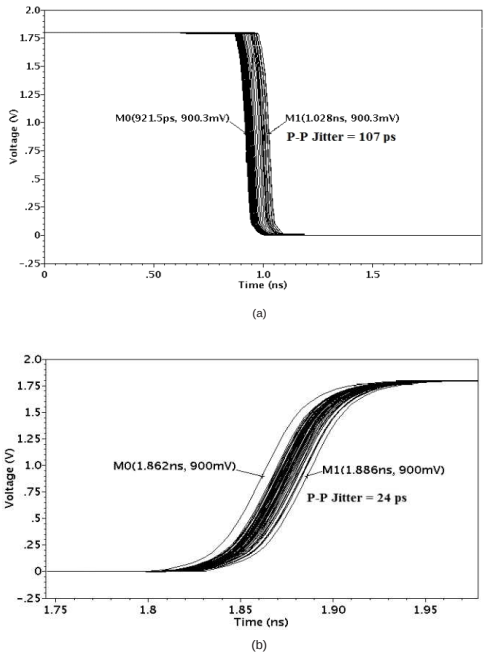

Figure 4.13: Jitter performance of the (a) conventional PLL, (b) proposed PLL

is measured and shown in Table 4.4 separately. It can be observed that the jitter of the PLL is very much consistent over a wide range of temperature in all process corners.

In Table 4.5 the simulated performance of this design is compared with the conventional PLL and other recent dual PFD architectures. It is observed that the tradeoff between power consumption and phase noise is reduced. All the performance indices achieved here are superior with 20 % physical area of the PLL.

Table 4.4: Jitter performance of the PLL at different process corners and temperatures

Temperature,(^{0}C)	P-P Jitter at different corners				
	NN	FF	FS	SF	SS
-40	33	29	34	37	45
0	27.5	26	28	30	42
27	24	25	23.5	24	39.5
50	18	20.5	21	23	37

Table 4.5: Post layout performance comparison of the PLLs

PARAMETERS	Conventional PLL [11]	PLL with multi PFD,architecture			
		Liao [48]	Woo [49]	Kuo [50]	Proposed
Technology (nm)	90	180	1500	350	90
Frequency (GHz)	2.5	2.5	0.16	2.4	2.5
Loop bandwidth (MHz)	-	0.05	-	-	32.5
Ref. frequency (MHz)	500	5	73.52	-	500
VCO Gain,(GHz/V)	2.5	0.336	0.02	-	2.5
Lock range(GHz)	0.5-2.6	2.5-2.7	0.12-0.25	1.8-2.5	0.7-2.8
Lock in time(ns)	220	-	4500	150	120
Phase noise (dBc/Hz), at 1 MHz offset)	-91.74	-105	-	-	-105.5
Power consumption (mw)	1	20	18.68	18.5	1.2
Layout area(mm^2)	1.6	1.56	845	-	1.94

4.6 Conclusion

This chapter proposed a novel dual PFD topology for a PLL by introducing an adaptive PFD selector which selects fast PFD before the loop locks and low noise PFD after locking. Phase noise analysis of the incorporated PFDs have been carried out and the comparison between the calculated and simulated results are presented. The process variation effects are observed by simulating

the performance of the PLL in all the five corners. The Monte Carlo simulations with 5% variation in threshold voltage are also carried out over a wide range of temperature from -40^o to 50^o C. The performance parameters have been compared with reported literatures and the proposed design is observed to offer superior performance with comparable physical area. This makes the proposed PLL to serve better in fast locking applications with improved phase noise performance and is suitable for multiple radio standards.

Chapter 5

A New Transmission Gate Cascode Current Mirror Charge Pump For Fast Locking Low Noise PLL

5.1 Introduction

Fast locking and low noise PLL being one of the driving factor of the current work can also be achieved by the charge pump (CP) block of the PLL. In due fact to their wide range of advantages charge pump phase locked loops (CP-PLLs) [3] are widely used in current communication systems. Today all wireless transceivers, disk read-write channels and other communication equipments are required to have a fast locking and low noise PLL.

A simple charge pump usually paired with a Phase Frequency Detector (PFD) [15] as shown in Figure 2.8 provides a wide lock range. The PFD generates either Up or Down signal which switches the current of the charge pump. The D flip flops make the PFD to generate Up and Down signal depending on the rising edge of the CK_{Ref} and CK_{Out} respectively. Now if both Up and

Down are low, then both the switches S_1 and S_2 will be off and V_{Cont} remains constant. If Up is high and Down is low, then I_{Up} (Up current) charges the capacitor CP through S_1. Conversely, if Up is low and Down is high, then I_{Down} (Down current) discharges the capacitor through S_2. Thus, if CK_{Ref} leads CK_{Out} the output voltage of the charge pump increases steadily and vice versa.

The charge pump is expected to generate a constant current and supply to the loop filter having the capacitor C_P. But the current mismatch between pull up and pull down network of the charge pump increases the glitches resulting in the static phase offset and dynamic jitter, known as reference spur [53] in PLL. This motivated the designers to have a charge pump which will have a less current mismatch between pull up and pull down network to lock faster and to have almost no glitch in the control voltage of the Voltage Controlled Oscillator (VCO).

To reduce the current mismatch only one current source is used [54, 55] from which both the charging and discharging current are derived. The Up and Down switches are responsible for charge injection. Transmission gates are also used [56] to reduce the non ideal effects like charge injection and clock feed through, and to get rid of the glitches in control voltage of the VCO. Charge sharing is another non ideal effect which leads to current mismatch. It occurs due to the parasitic capacitances of the charge pump. When the switches of the charge pump goes from OFF to ON state, charge sharing occurs between the parasitic capacitances of the charge pump and the output node due to which the control voltage of the VCO deviates from its required value.

In this chapter the non idealities of conventional charge pump are enumerated. A novel scheme for the design of charge pump to address some of the non idealities like current mismatch, charge sharing, and charge feed through is proposed and presented.

5.2 Conventional charge pump and its non-idealities

As has been discussed in Chapter 2, a simple charge pump consists of two current sources I_{Up} and I_{Down} and two switches as shown in the Figure 2.8. But in a conventional charge pump the current sources are realized by two MOSFETs (M_1, M_4) and the switches by NMOS M_2 and PMOS M_3, shown in Figure 5.1 by considering that a transistor biased with a constant voltage in saturation, can be implemented as constant current source to a good approximation. The inverter is inserted at the output of Up signal so that the M_3 will be switched on when Up is high. The insertion of inverter introduces a delay in path, thereby introducing a skew between Up and Down. To eliminate this effect, a transmission gate is inserted between Down and M_2. Hence both the Up and Down paths become balanced.

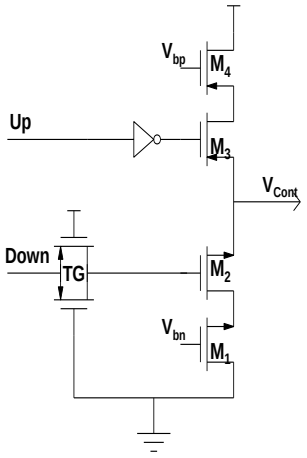

Figure 5.1: Conventional charge pump

The non idealities of charge pump (already discussed in Chapter 2) like leakage current, current mismatch and timing mismatch calls for a design to address these issues.

All the charge pump topologies reviewed in Chapter 2 the above mentioned

topologies did not mention about the output voltage swing. Considering all these effects, a novel charge pump topology is proposed which provides all the advantages and removes the limitations of TGCP.

5.3 Proposed transmission gate cascode current mirror charge pump

Current mirror is a primary component of a charge pump. An efficient current mirror should have high output impedance, high output voltage compliance, low power consumption and immune to power supply variation and noise. A self Biased High Swing Cascode Current Mirror is chosen here for its performance and circuit simplicity.

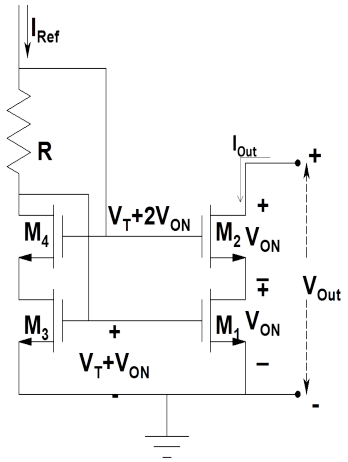

Figure 5.2: Self biased high swing cascode current mirror [15]

Considering all the transistors in saturation as shown in Figure 5.2, a resistor R is used to generate the bias by dividing the voltage across it. The aspect ratio values of M_1 and M_3 are estimated using the normal drain current characteristic of MOSFET in saturation.

Due to body bias the threshold voltages for M_2 and M_4 are expressed as,
$V_{T2,4} = V_{T0} + \gamma \left(\sqrt{|-2\phi_F| + V_{SB}} - \sqrt{|-2\phi_F|} \right)$

The gate voltage of M_2 and M_4 are,

$V_{G2,4} = V_{T2,4} + 2V_{ON}$

The gate voltage of M_1 and M_3 can be found to be,

$V_{G1,3} = V_{T0} + V_{ON}$

The simulated input output characteristics of self biased high swing cascode current mirror is shown in Figure 5.3.

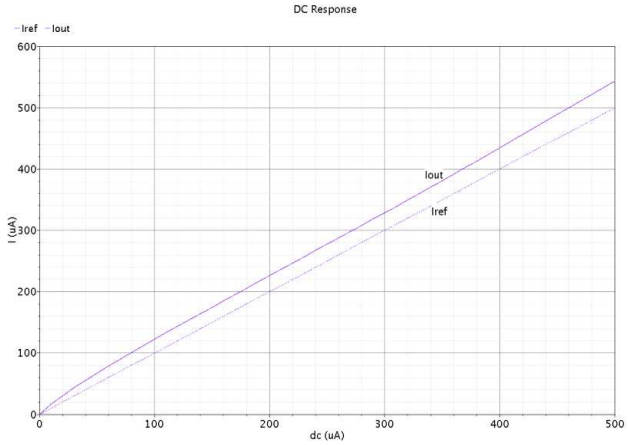

Figure 5.3: Input output response

The proposed charge pump topology using a self biased high swing cascode current mirror(5.2), threshold voltage reference circuit and transmission gate is shown in Figure 5.4. Transistors M_1 to M_6 with transmission gates T_1, T_2 and T_{Down} form the Down network of charge pump, where as transistors M_7-M_{10} with transmission gates T_3 and T_{Up} form the complementary Up part of the circuit. Switches are designed by transmission gates driven by complementary clock signals which removes the clock feed through effect.

The current mismatch is avoided by deriving charging and discharging currents from a single reference current source. Transmission Gates T_1, T_2 and T_3 are employed to reduce the mismatch caused due to insertion of T_{UP} and T_{DN}. The glitches at the drains of output transistors (M_5 and M_7) during switching T_{Up} or T_{Down} would not propagate to the output node due to the insertion of M_6 and M_9. Transistors M_5 and M_7 would be turned on softly, since the rise

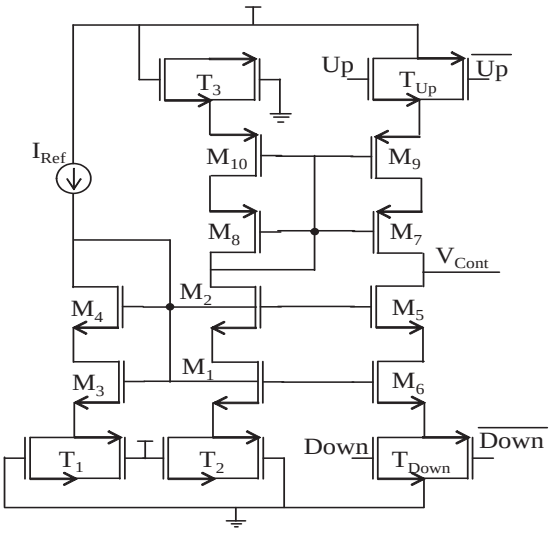

Figure 5.4: Proposed charge pump topology

Table 5.1: Aspect ratio of the circuit elements

Transistors	**W/L Ratio (nm/ nm)**
M_1, M_2, M_3, M_4, M_8, M_{10}	360/100
M_5, M_6, M_7, M_9	120/100
T_{UP}, T_{Down} (Both PMOS and NMOS)	120/100
T_1, T_2, T_3	360/100

and fall time of current pulses is controlled by the R-C time constants at their sources.

The sizing of the transistors and transmission gates of the charge pump is tabulated in Table 5.1. All this sizing has been done to maximize effective output voltage, remove current glitches and to reduce the turn on time of the charge pump. Value of bias current is chosen such that the charge pump helps to give optimum lock time for PLL. The Current I_{Ref} is drawn from a current reference circuit [56] shown in Figure 5.5. It is a current source which is very less affected by the fluctuation in the supply voltage and provides biasing current for the charge pump. The W/L value of the transistors M_{11} to M_{17} is (240/100) nm and M_{18} to M_{19} is (120/100) nm. The current drawn from the current reference is 40 μA.

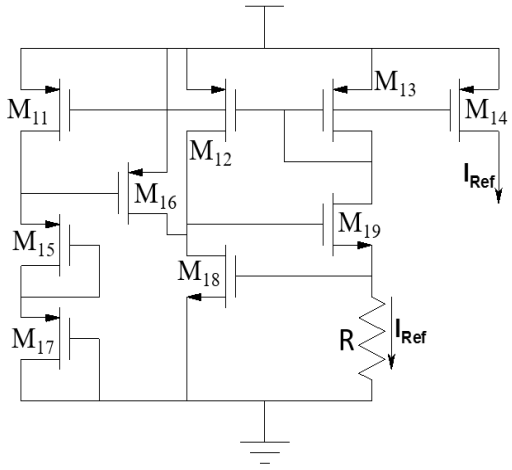

Figure 5.5: Current reference circuit

5.4 Post layout performance analysis

The proposed charge pump is designed using 90 nm CMOS technology and simulated with a 1.8 V power supply. The layout of the charge pump is shown in Figure 5.6. Use of high output impedance current mirror reduces the current mismatch between charging (I_{Up}) and discharging (I_{Down}) currents. The current mismatch is recorded as 7% for the proposed charge pump and 20 % for the conventional one.

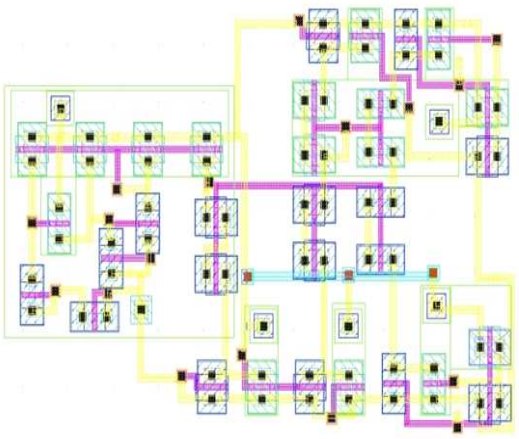

Figure 5.6: Physical design of the charge pump

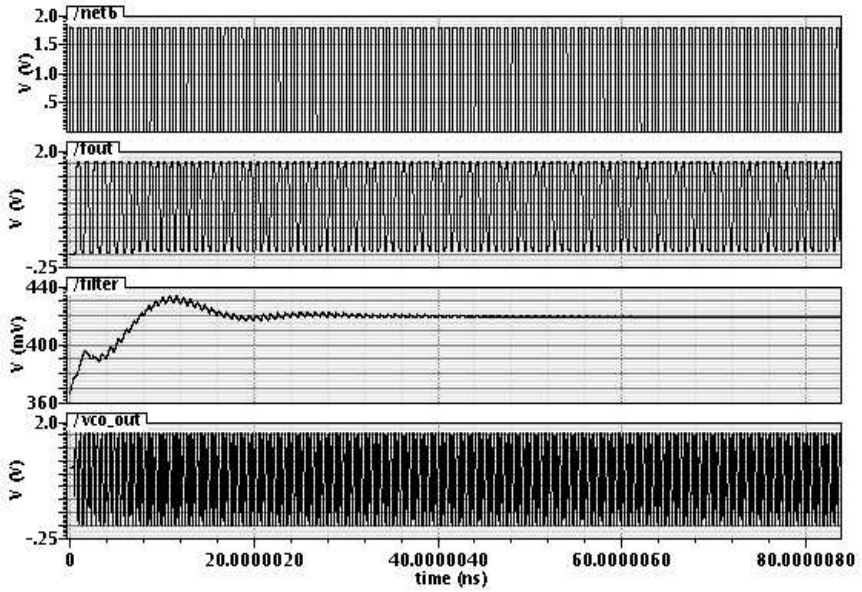

Figure 5.7: Transient analysis of the PLL using proposed charge pump

Using this charge pump the complete PLL is designed in Cadence. The transient analysis of the PLL is performed and presented in Figure 5.7. It is observed that the output voltage (VCO_{out}) swing is 0 to 1.79 V from a 1.8 V supply. The loop locks after 25 ns and the control voltage of the VCO has no ripple in it after 50 ns reveals the fact of reduced charge sharing and clock feed-through effect. To observe the superiority of control voltage variation of the modified charge pump, it is compared with the conventional one by connecting both of the charge pumps to the same PFD and the results of comparison between the control voltage variations of both the charge pumps plotted in Figure 5.8. Due to the ripple free characteristic after locking, the spur level also could be minimized. Hence the modified charge pump helps the PLL to lock faster with reduced reference spur. Instead of two as used in other charge pumps, only one current source is used in this proposed charge pump which results only 1.7 mW of average power consumption for the PLL. The power consumption plot is shown in Figure 5.9. The phase noise variation with different offset frequencies is plotted in figure 5.10. The phase noise is measured to be -87.1 dBc/Hz at 1 MHz offset and the reference spur is -57

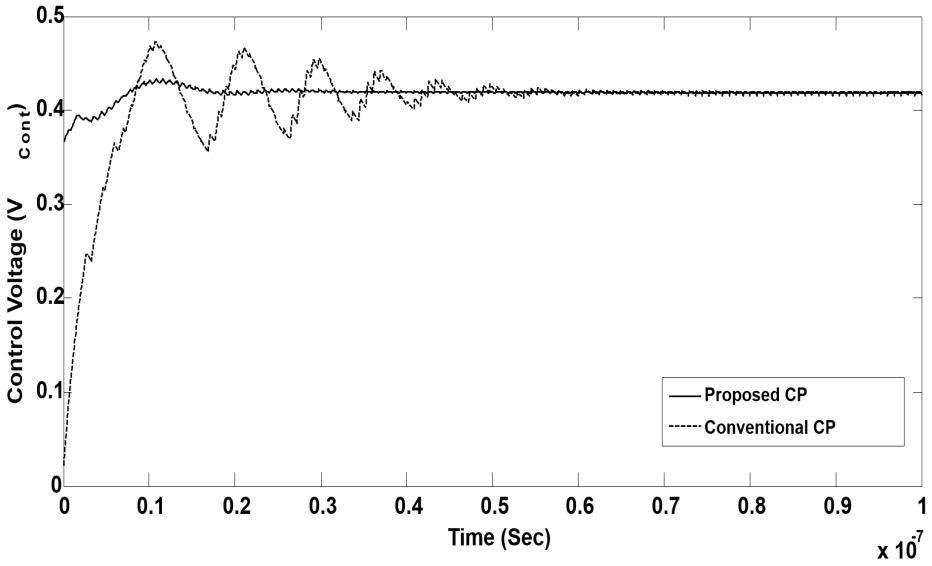

Figure 5.8: Comparison between the control voltage variation of proposed charge pump and conventional one

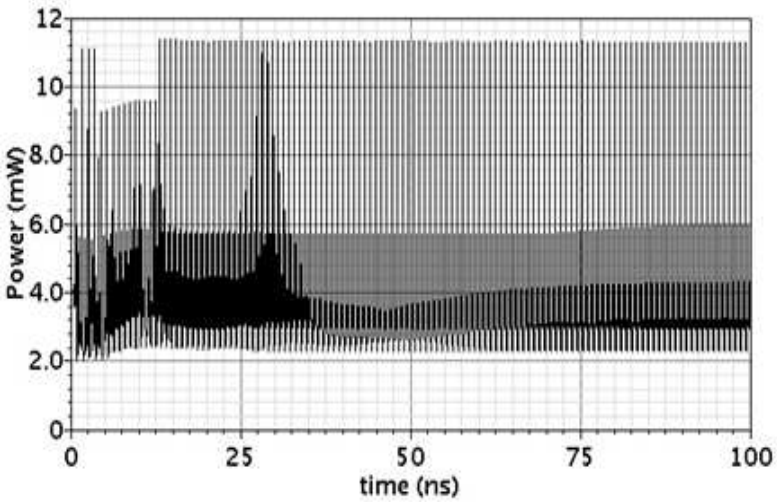

Figure 5.9: Power consumption plot of the PLL using proposed charge pump

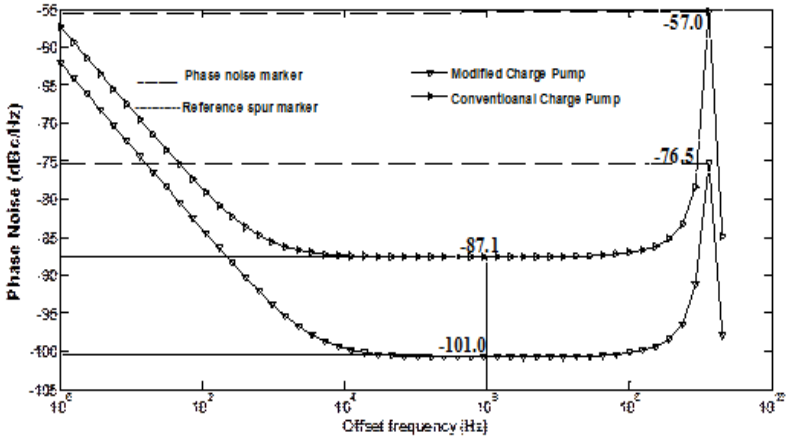

Figure 5.10: Phase noise variation plot of the PLL using proposed charge pump

dBc/Hz at 1.25 GHz offset frequency. The proposed charge pump is compared with the conventional one with respect to its phase noise performance and depicted in Figure 5.10. It is observed that the noise level is minimized by more than 10%. The performance comparison between the conventional and proposed charge pumps is summarized in Table 5.2.

Table 5.2: Performance comparison summary of proposed charge pump and conventional one

Parameters	**PLL of 2.5 GHz range**	
	Conventional CP	**Proposed CP**
Technology	CMOS 90 nm	
Frequency	2.5 GHz	2.5 GHz
Vdd	1.8V	1.8V
Current mismatch (%)	20	7
Lock range(GHz)	0.8-2.6	0.8-2.5
Lock in time(ns)	60	25
Phase noise (dBc/Hz @1 MHz offset)	-87.1	-101.0
Reference spur (dBc/Hz) @500 MHz offset)	-57.0	-76.5
Power consumption (mw)	3.43	1.74
Layout area(m2) of the CP	41.8	85.5

5.5 Conclusion

A high performance Transmission Gate Cascode Current Mirror charge pump is designed and implemented using CMOS 90 nm technology. Due to its reduced non ideal effects it can achieve fast locking with reduced reference spur. The power consumption also could be minimized due to the use of only one current source. A high swing cascode current mirror circuit is used which results the output voltage swing of the VCO to range from 0 to 1.7 V from 1.8 V supply. This improved performance could be achieved at the cost of more physical area of the charge pump.

Chapter 6

Process Variation Tolerant Wide-band Fast PLL with Reduced Phase Noise using Adaptive Duty Cycle Control Strategy

6.1 Introduction

Effects of variation in the manufacturing process and operating conditions on the performance of nanoscale CMOS integrated circuit are of paramount importance in semiconductor industry. Process variations lead to inter die and intra die devices geometry mismatch and hence other characteristic mismatches in circuits. It has been challenging for the engineers to address such unavoidable concerns in their designs.

Due to the increasing demand for high frequency multi band and multi standard transceivers in modern wireline, wireless communication and broadcasting systems, a wide-band fast locking phase locked loop (PLL) achieving

low phase noise is highly imperative [79]. This requires a voltage controlled oscillator (VCO) of high tuning range, and low phase noise [80]- [82]. To meet with the high frequency requirements, if we implement a high tuning range VCO having large gain, the phase noise will be degraded which threatens the stability of the PLL further. In this case we should come up with a solution to design a wide range PLL without sacrificing the phase noise.

To achieve an enhanced lock range performance of a PLL, various techniques have been reported [88]- [94]. In spite of all these efforts, non-idealities due to the process variations affect the lock range and hence lock time performance of the PLL considerably. PLL being a very sensitive mixed signal circuit, this issue becomes more prominent with increase in frequency of operation.

In this work, a novel adaptive duty cycle control strategy which makes the PLL process variation tolerant is proposed. The work presented here has following novel aspects.

i. The process variation related locking and phase noise performance of the PLL is enumerated.

ii. A design strategy for frequency divider in PLL is proposed which adaptively controls the shift in the duty cycle due to process variations and hence the PLL to lock at high frequencies. This PLL so designed is capable of working over a wider frequency range.

iii. The proposed design is demonstrated to assist the PLL to lock faster in normal operating conditions too.

iv. It achieves reduction of the phase noise at a given operating frequency under similar operating conditions.

v. This PLL finds a wider temperature range of operation in comparison to normal PLL.

6.2 Effects of process variation on PLL performance

The generic architecture of a charge pump PLL consisting of the phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO), and frequency divider is presented in Figure 6.1. The output signal from frequency divider is of high frequency which needs to be locked with the reference one without any disturbance. The PLL is a very sensitive circuit particularly at high frequencies. The small random variations in geometrical process parameters, supply voltage and temperature affect its performances like lock time, lock range and phase noise to a great extent.

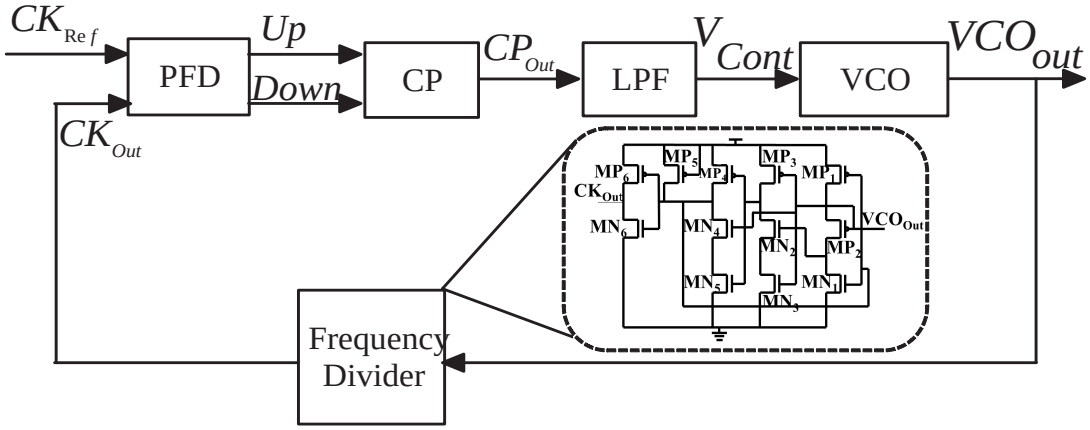

Figure 6.1: Proposed modification to PLL architecture

The CK_{Out}, the final output of the blocks of PLL including the divider, is fed to the PFD. A small fluctuation in CK_{Out} signal would result either in lock failure or in a large locking time. The voltage levels and duty cycle of the CK_{Out} signal are affected by the process variations particularly at extreme corners. Although all the devices in the PLL affect the performance, the fabrication process variation at the output devices of the divider more prominently affects the circuit performance. At high frequency, approximately above 2 GHz, the NMOS and PMOS devices fabricated at different process corners

cannot respond to the signal transitions in the normal expected way. Due to this, the lower level of the signal gets elevated from the ideal base line envelope (Figure 6.2) by an amount $\Delta V_{CK_{Out}}$. Under such conditions, the duty cycle variations progressively increase leading to large lock time and eventually lock failure. This significantly limits the operation of the circuit at high frequencies hence reducing the lock range of the PLL.

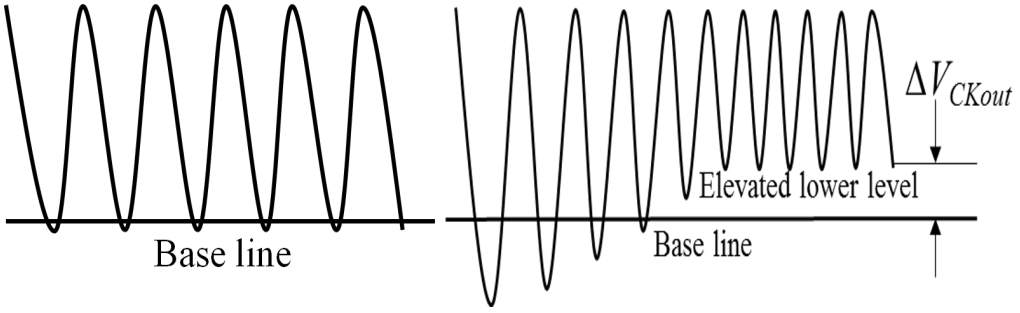

Figure 6.2: Output of the divider module at high frequency (a) ideal and (b) actual

Therefore though the circuit performs well under the nominal process conditions, it fails to lock at extreme process corners. This problem of locking of the PLL is substantiated by conducting extensive simulation analysis of the circuit under different process corners at different frequencies of operation. This poses to be a matter of concern for the designer and demands remedial measures. Besides the lock performances, the phase noise of the PLL system is considerably affected.

6.3 Adaptive duty cycle control strategy

To alleviate the above problem, an adaptive duty cycle control (ADCC) technique is proposed for the frequency divider circuit as shown in Figure 6.3. The maximum frequency to which the PLL can lock is enhanced by adaptively controlling the duty cycle of the divider output CK_{Out} .

In the PLL using the proposed strategy, a second order passive lead-lag low pass filter (LPF), five stage CS-VCO, and a frequency divider along with con-

ventional PFD and CP [11] are employed. The input reference signal (CK_{Ref}) and feedback signal (CK_{Out}) are fed to the PFD which generates the Up and Down Signals for the CP circuit depending upon the positions (lead/lag) of the input signals. The output node of the CP circuit charges if Up is high and discharges otherwise and will have ripples in it. Ripple free signal from LPF (V_{Cont}) controls the VCO output frequency. The CK_{Out} signal is the divided frequency version of VCO_{Out}. Due to the process variation effects, the output of the PLL gets disturbed as described in the previous section.

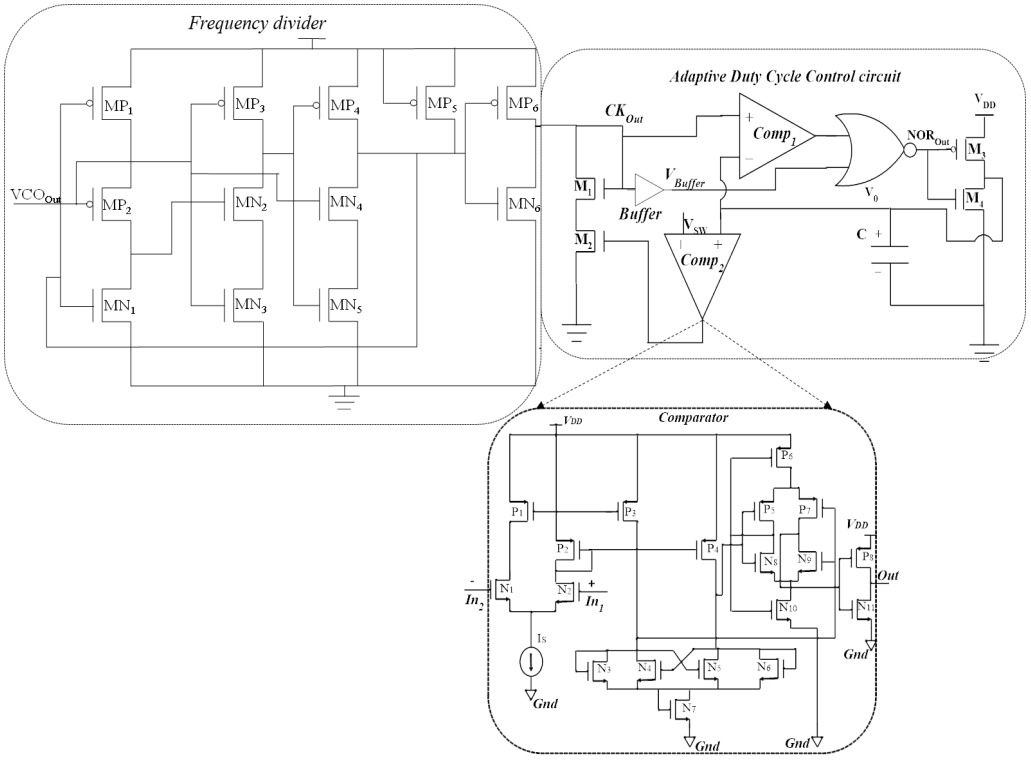

Figure 6.3: Adaptive duty cycle control (ADCC) in frequency divider

The proposed ADCC circuit and its operational flow diagram are depicted in Figure 6.3 and Figure 6.4 respectively. The $Comp_1$ and $Comp_2$ used here are high speed comparators [11] to process the high frequency signal CK_{Out}. The comparator $Comp_2$ is used to drag the CK_{Out} signal to the base line when it goes beyond a user defined threshold voltage V_{SW}. The capacitor C plays a vital role in design of the proposed circuit as it determines the value of V_O

which is input to both the comparators.

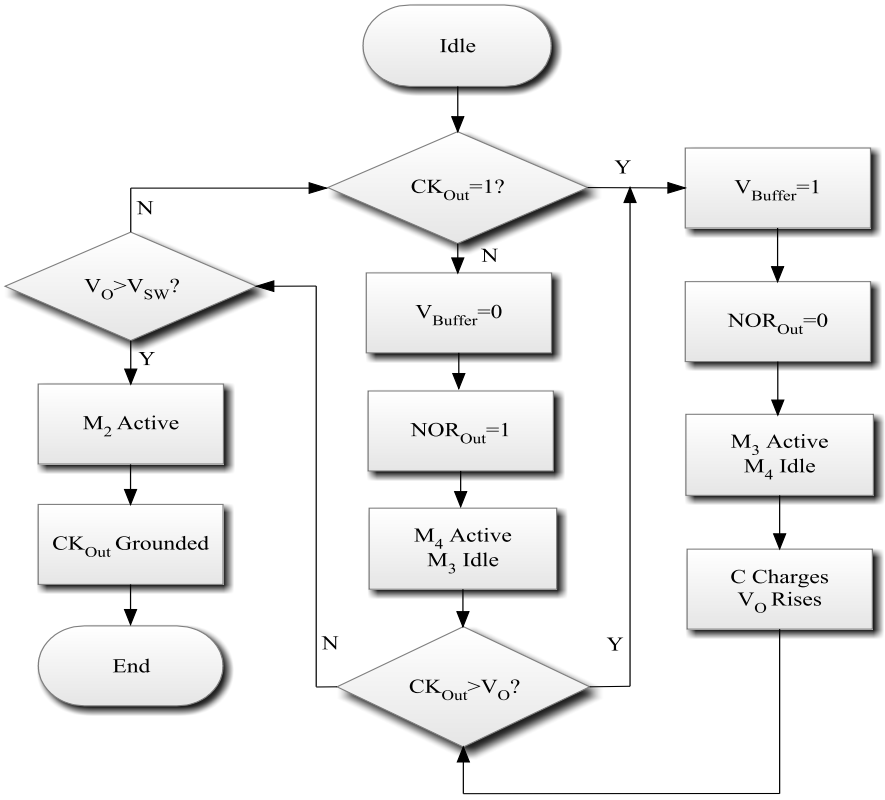

Figure 6.4: State diagram of the proposed ADCC frequency divider circuit

Suppose a change in control voltage, V_{Cont}, of the VCO (ΔV_{Cont}) changes the frequency of the VCO_{Out} to Δf_{VCO}. Here the Δf_{VCO} can be taken as Δf_{CKOut}. So for a transition in frequency of Δf_{CKOut} the change in control voltage is,

$$\Delta V_{Cont} = \frac{\Delta f_{CK_{Out}}}{N.K_{VCO}} \tag{6.1}$$

where, N is the divide ratio of the frequency divider, K_{VCO} is the gain of the VCO. The time required for a single shift of V_{Cont} is,

$$\Delta t = \frac{(C_1 + C_2)\,\Delta V_{Cont}}{I_{CP}} \tag{6.2}$$

where, C_1, C_2 are the loop filter capacitors, I_{CP} is the charge pump output current. In the ADCC circuit, capacitor C stores the voltage when the CK_{Out}

makes a transition to low. Considering M_3 as a MOS resistor, when $V_O \leq CK_{Out}$, transistor M_3 charges C to V_{DD}. Here the charging of V_O can be expressed as,

$$V_{O,Charge}(t) = V_{DD} + (V_{i1} - V_{DD})\, e^{-t/T_1} \tag{6.3}$$

where, charging time constant $T_1 = R_{M_3}.C$, R_{M_3} is the equivalent resistance offered by M_3, V_{i1} is the initial voltage in charging phase. Now when V_O is greater than CK_{Out}, at high to low transition of CK_{Out}, C discharges through M_4 making V_O as,

$$V_{O,Discharge}(t) = (V_{i2})\, e^{-t/T_2} \tag{6.4}$$

where, discharging time constant $T_2 = R_{M_4}.C$, $R_{M_4}$is the equivalent resistance offered by M_4, V_{i2} is the initial voltage in discharging phase. The charging and discharging voltage V_O ranges from 0 to V_{SW} as analytically discussed. Making $W_4 \gg W_3$, and subsequently $T_2 \ll T_1$, the required tracking time T_{Track} is estimated as,

$$T_{Tracking} = T_1 ln\left(\frac{1}{V_{DD} - V_{SW}}\right) \tag{6.5}$$

$$Hence, T_1 = \frac{T_{Tracking}}{ln\left(\frac{1}{V_{DD}-V_{SW}}\right)} \tag{6.6}$$

Now the value of capacitor can be expressed as,

$$C = \frac{T_{Tracking}}{ln\left(\frac{1}{V_{DD}-V_{SW}}\right) R_{M_3}} \tag{6.7}$$

As compared to the frequency acquisition time of the PLL, the time required to change in V_{Cont} for each transition of f_{CKout}, Δt is very small. Therefore required time $T_{Tracking}$ must be less than minimum pull-in time of the PLL ie.

$T_{Tracking} \leq \Delta$t. From 6.1, 6.2, and 6.7, the capacitor value is derived as,

$$C = \frac{(C_1 + C_2)\,\Delta f_{CK_{Out}}}{ln\left(\frac{1}{V_{DD}-V_{SW}}\right) R_{M_3} I_{CP}.N.K_{VCO}} \tag{6.8}$$

In the present case, V_{DD}=1.8 V, V_{SW} =1 mV which is very less than V_{DD}, C_1=4.65 pF, C_2=1.35 pF, Δf_{CKout}=50 MHz, K_{VCO}=1.9 GHz/V, R_{M3}=500 KΩ, N=2, I_{CP}=50 μA. This yields C to be 0.05 pF.

Algorithmic outline of the proposed ADCC circuit

$Condition-1$: At the rising edge of the CK_{Out},

1. V_{Buffer} changes from low to high making NOR_{Out} to be low.
2. M_3 becomes active and M_4 inactive. C charges to V_{DD} making V_O high.

$Condition-2$: At the falling edge of the CK_{Out},

1. V_{Buffer} changes from high to low making NOR_{Out} to be high.
2. M_4 becomes active and M_3 inactive. V_O discharges through M_4. Here again two cases arise.

$Case-1$: When CK_{Out} greater than V_O,

1. $Comp_1$ feeds a 1 to the NOR gate and the further operation will be same as Step 2 of Condition-1.

$Case-2$: When CK_{Out} less than V_O,

1. Getting both the inputs as high, NOR_{Out} becomes high, activating M_4 and deactivating M_3.
2. V_O reduces as the capacitor discharges. Hence, V_O tracks the lower level of CK_{Out}.
3. $Comp_2$ compares the inputs V_O and V_{SW}. V_{SW} is a reference voltage indicating the lowest level of the divided signal (CK_{Out}) swing which is considered to be 1 mV to ensure rail to rail swing of CK_{Out}.
4. Whenever V_O is greater than V_{SW}, $Comp_2$ feeds a high signal to the gate of M_2 which pulls CK_{Out} to ground ensuring rail to rail swing.

6.4 Performance analysis of the proposed PLL

The PLL designed using the proposed technique is simulated in Cadence Specter RF using UMC 180 nm technology. The physical layout of the PLL is shown in Figure 6.5. Simulations are carried out without and with the proposed strategy for PLL at different frequencies under the worst process variation condition. The shift of CK_{Out} from the base line, ΔV_{CKout} and locking time are reported in Table 6.1. At 2.25 GHz frequency when ΔV_{CKout} becomes 27 mV, the PLL goes out of lock. The PLL also goes out of lock for higher frequencies. By using the proposed strategy ΔV_{CKout} becomes bounded within 1 mV and the PLL locks at these frequencies. This ensures the PLL to become process variation tolerant. Besides this, the lock time reduces at all frequencies considerably by use of ADCC. The total silicon area with the ADCC circuit, reported by this design is 3.325 mm^2. The post layout transient analysis of the complete PLL for 3.5 GHz operating frequency with the voltage at CK_{Out} node is demonstrated in Figure 6.6. In the PLL, without the ADCC circuit, the upward shift of the voltage swing of CK_{Out} is depicted in it.

The problem of shifting is eliminated by the proposed technique. The proposed PLL locks at 40 ns whereas the lock range is improved by 40 %. The proposed design for the operating frequency 3.5 GHz exhibits a phase noise of -108.7 dBc/Hz at 1 MHz offset frequency. This is found to be 18 dB less than the conventional PLL [11] without ADCC where the phase noise is -90.5 dBc/Hz at 1 MHz offset frequency. The peak in the phase noise plot between 100 MHz and 1 GHz is the reference spur generated at that frequency. The phase noise of the proposed PLL is compared with the conventional PLL (Figure 6.8). It is observed that at 1 MHz offset frequency the proposed PLL exhibits 15% lesser phase noise than the conventional one.

Monte Carlo analysis is carried out to observe the impact of process and mismatch variations at different temperatures. Both the intra-die and inter-die process variation effects are observed. Industry standard transistor and

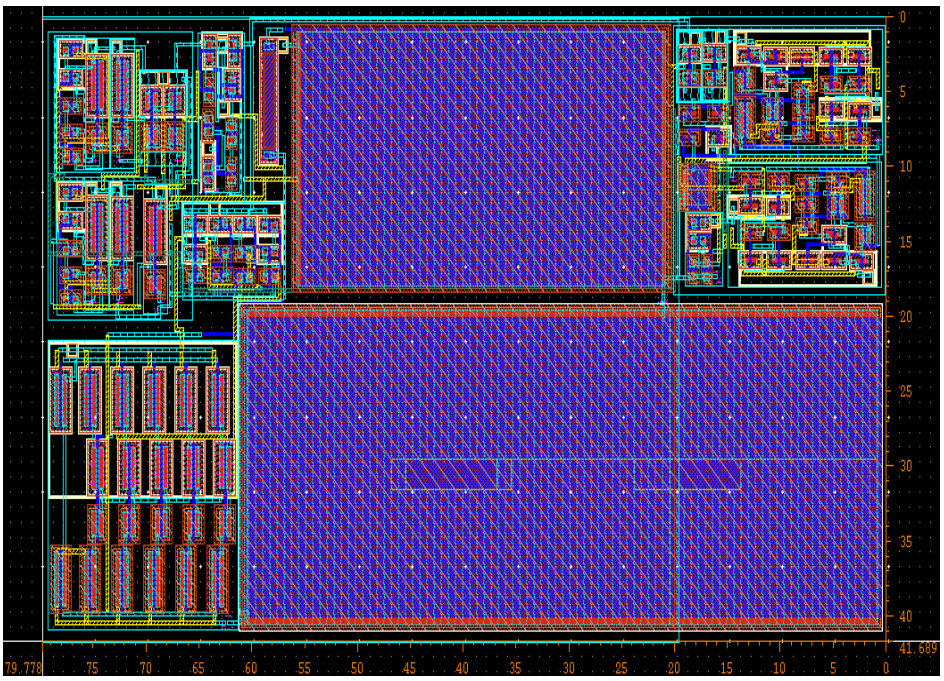

Figure 6.5: Physical layout of the proposed PLL

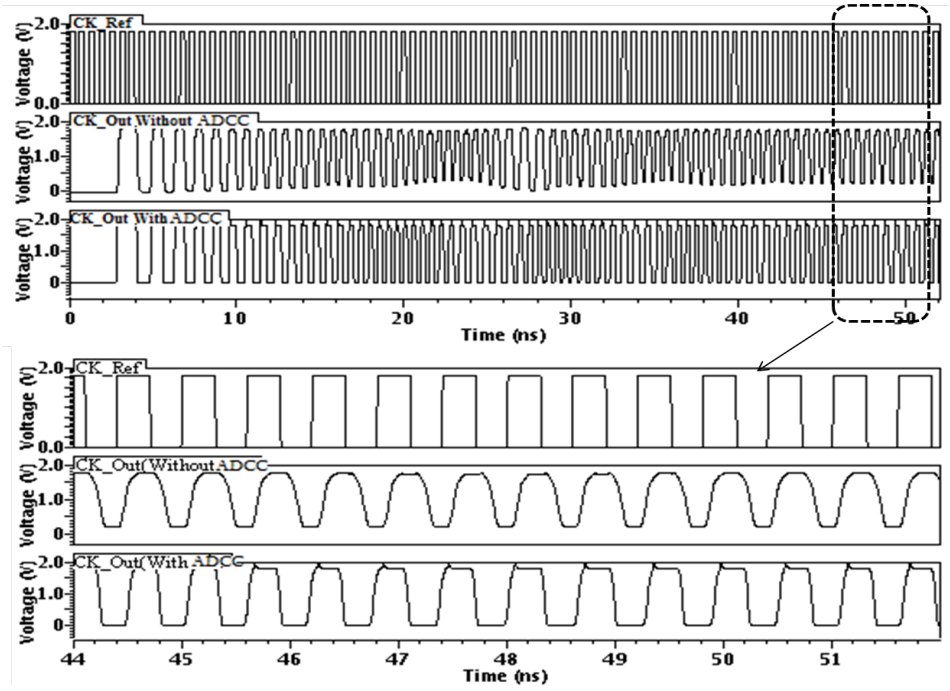

Figure 6.6: Transient analysis of the proposed PLL

Table 6.1: Performance summary of the PLL at different operating frequencies

Freq. (GHz)	Without ADCC			With ADCC		
	ΔCK_{Out} (mV)	Lock Time (ns)	Phase noise (dBc/Hz at 1Mhz offset)	ΔCK_{Out} (mV)	Lock Time (ns)	Phase noise (dBc/Hz at 1Mhz offset)
0.9	2.6	160	-102.3	0.16	35	-112.7
1.8	7.9	175	-98	0.27	40	-109.5
2.25	112	NL	-	0.45	40	-108
2.5	158	NL	-	0.59	50	-106.9
3.5	180	NL	-	0.75	55	-105.7

process variation models from UMC foundry are used for all simulations.

Table 6.1 also lights the phase noise of the PLL under worst case process variations and a reduction in phase noise is clearly observed there. Phase noise variations demonstrated in Figure 6.7 for temperatures at -100, -50, 0, 27, 50 and 100_o C are estimated to be 4, 1, 1, 2, 3 and 4 dBc/Hz respectively at 1 MHz offset frequency. Subsequently it is perceived that mostly with the rise in temperature the ranges of phase noise variation at different threshold voltages increases. However, it doesnt go beyond -102 to -109 dBc/Hz at 1 MHz offset frequency.

At different process corners, NN, SS, SF, FS, FF, performance parameters of the PLL like phase noise, lock in time and power consumption for different temperatures are estimated and shown in Table 6.2, 6.3 and 6.4 respectively. The phase noise is measured to be best in FF and worst in SS corner though there is no significant variation in the power consumption in all the corners. Fast locking capability is achieved in SF corner up to a good extent.

The power consumption has a linear variation with temperature. Furthermore, the lock time improves with decrease in temperature. The temperature based lock performance analysis reveals that the PLL with ADCC is capable of locking in the range of -100 to 100^0 C where the same PLL without the ADCC does not lock beyond -50 to 50^0 C range. This can again be attributed to the same control of CK_{Out} by the use of the proposed circuit.

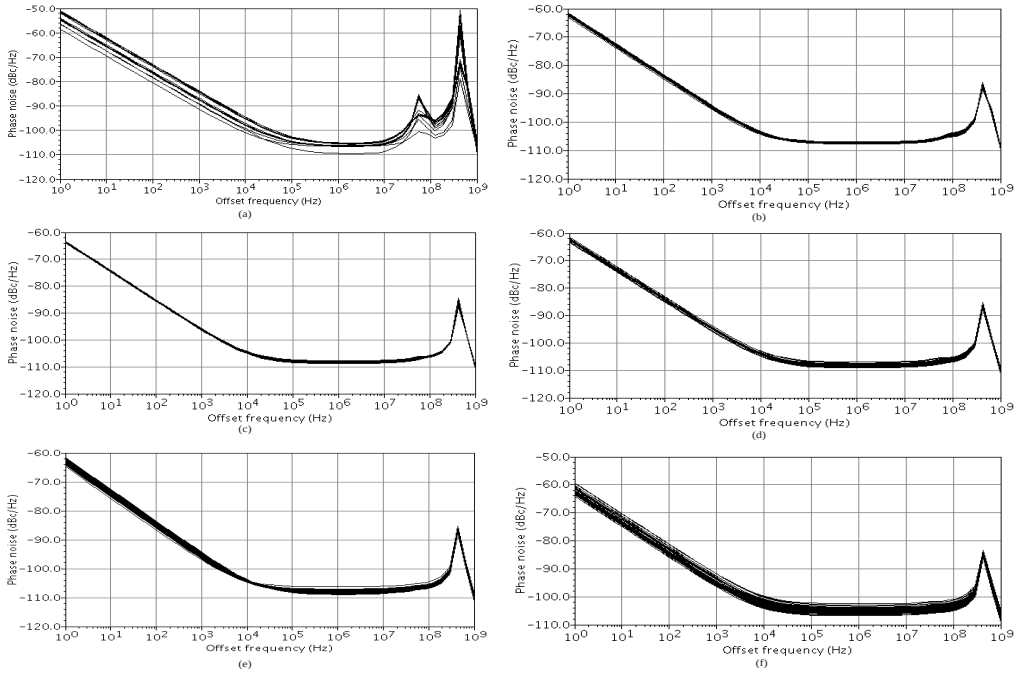

Figure 6.7: Monte Carlo simulations for phase noise variation at different temperatures (a) -100^o, (b) -50^o, (c) 0^o, (d) 27^o, (e) 50^o, and (f) 100^o C

Table 6.2: Phase noise of the PLL at different process corners and temperatures

Corner	Phase noise (dBc/Hz at 1 MHz offset frequency)				
	-100^0 C	-50^0 C	0^0 C	50^0 C	100^0 C
NN	-106.5	-107.8	-108.7	-108.9	-105.3
SS	-101.4	-102.6	-103.1	-103.7	-104.6
SF	-103.1	-104.7	-105.0	-105.9	-106.9
FS	-104.3	-107.9	-108.6	-109.0	-109.4
FF	-108	-109.5	-109.9	-110.1	-110.6

Table 6.3: Lock time of the PLL at different process corners and temperatures

Corner	Lock time (ns)				
	-100^0 C	-50^0 C	0^0 C	50^0 C	100^0 C
NN	25	35	45	60	75
SS	30	40	55	65	80
SF	25	35	45	50	60
FS	30	45	55	65	75
FF	15	30	40	60	70

Table 6.4: Power consumption of the PLL at different process corners and temperatures

Corner	Power consumption (mW)				
	-100^0 C	-50^0 C	0^0 C	50^0 C	100^0 C
NN	4.05	4.2	4.35	4.5	4.6
SS	3.5	3.6	3.8	4.1	4.25
SF	4.15	4.25	4.3	4.45	4.5
FS	3.95	4.0	4.15	4.3	4.4
FF	4.2	4.5	4.6	4.6	4.7

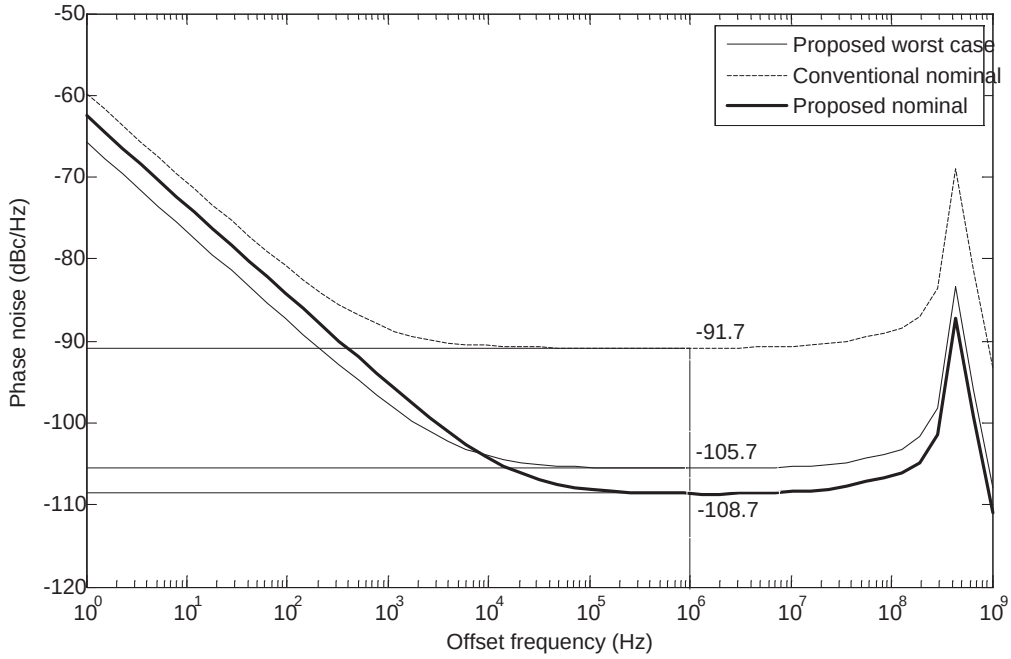

Figure 6.8: Phase noise comparison between the conventional and proposed PLL

Table 6.5: Performance comparison of the PLLs

Parameters	Conventional	PLL with enhanced lock range			
		Yadong [91]	Shin [94]	Song [106]	This work
Technology (nm)	180	180	130	180	180
Frequency (GHz)	2.2	0.9	2.5	0.9	3.5
Lock range (GHz)	0.5-2.2	0.62-0.92	2.3-3.9	0.8-1.0	0.7-4.2
Lock time (ms)	0.22	20	50	40	0.04
Phase noise (dBc/Hz) at 1 MHz offset)	-90.5	-130	-124.1	-114	-108.7
Power (mW)	3.6	21.6	18.96	64.8	3.6
Layout area (mm^2)	1.6	1.06	2.10	3	3.3
Jitter (ps)	127	-	-	-	20

In Table 6.5, the performance comparison of this design with the conventional and other recent PLL architectures having enhanced lock range is presented. All the performance indices achieved here are observed to be superior with an affordable physical area.

6.5 Conclusion

This chapter analyses the lock performance degradation of the PLL due to manufacturing process variations. To alleviate this problem, an adaptive duty cycle control (ADCC) strategy is proposed here for the divider circuit. Use of the proposed strategy makes the PLL to lock at higher frequencies and to be process variation tolerant. This strategy additionally helps the PLL circuit to lock faster. The circuit performance parameters are evaluated through extensive simulations using Cadence Spectre. The comparative analysis of performance of the proposed circuit relatively establishes its capability of fast locking yet producing wide band applicability. The process and mismatch vari-

ation effects in the modified PLL circuit are observed in all the five corners. The PLL with the proposed strategy is observed to work over a wide temperature range of -100 to 100^0C in comparison to normal case operating in range of -50 to 50^0C. The performance parameters like lock range, lock time, phase noise, and power consumption are compared with reported literatures and are observed to be superior. This is achieved at the cost of area due to the additional ADCC circuit. The proposed approach is expected to improve the yield performance of the PLL at higher frequencies.

Chapter 7

Multi objective optimization of PLL performances using Infeasibility Driven Evolutionary Algorithm

7.1 Introduction

Higher phase noise in PLL will cause reduced signal to noise ratio and increased adjacent channel power. Usually the contribution to the phase noise comes from all components of the PLL [95] with the major source of noise being the voltage controlled oscillator (VCO). To reduce the phase noise it is important to estimate how the noise affects each block of the PLL. Although dead zone of phase frequency detector (PFD), gain of VCO, frequency dividing ratio, etc. are the decisive factors for the phase noise in PLL, low pass filter (LPF) components cannot be neglected as they determine the PLL characteristics like loop bandwidth, lock time and output phase noise. The loop band-width should be fixed as high as possible to reduce the phase noise. But it is constrained to be well below the lowest operating frequency for stabil-

ity [3]. Now these constraints can cause the PLL to have undesirable phase noise performance and narrow operating frequency. Due to these dynamic loop settings, it is very complex to model the PLL at transistor level. For appropriate evaluation of LPF components with the preselected loop bandwidth and phase margin, the PLL is systematically modeled by numerous designers. Then typical behavioral approaches are performed to observe PLL specifications which include phase noise. If any of the specifications do not meet the required values, design modification is carried out again by approximating new LPF components. This iterative process consumes long design time to arrive at proper LPF component values with acceptable efficiency. However besides phase noise there are other performance parameters of PLL which also need to be optimized. These are lock time and power consumption with a specified operating frequency. Further there exists trade off among these parameters due to their interdependency. This interdependency is shown in Figure 7.1).

Optimization of nano-CMOS devices [107] and circuits [108, 109] are currently of great interest among the designers community. Various algorithms have been used for optimization. However optimizing multiple objectives in a constrained environment has proven to be a difficult task but is very useful. In this chapter a comprehensive model of phase noise, power consumption and lock time have been explicitly derived. These expressions are then subjected to multi-objective optimization algorithm. As deliberated by Ray et al. [110], Infeasibility Driven Evolutionary Algorithm (IDEA) is employed here to determine the passive components of LPF and aspect ratios of the devices which affect the performances like phase noise, lock in time and power consumption in a feasible range of constraints.

7.2 Performance modeling of PLL

In this section the performance models of PLL like phase noise, power consumption and lock time are analyzed.

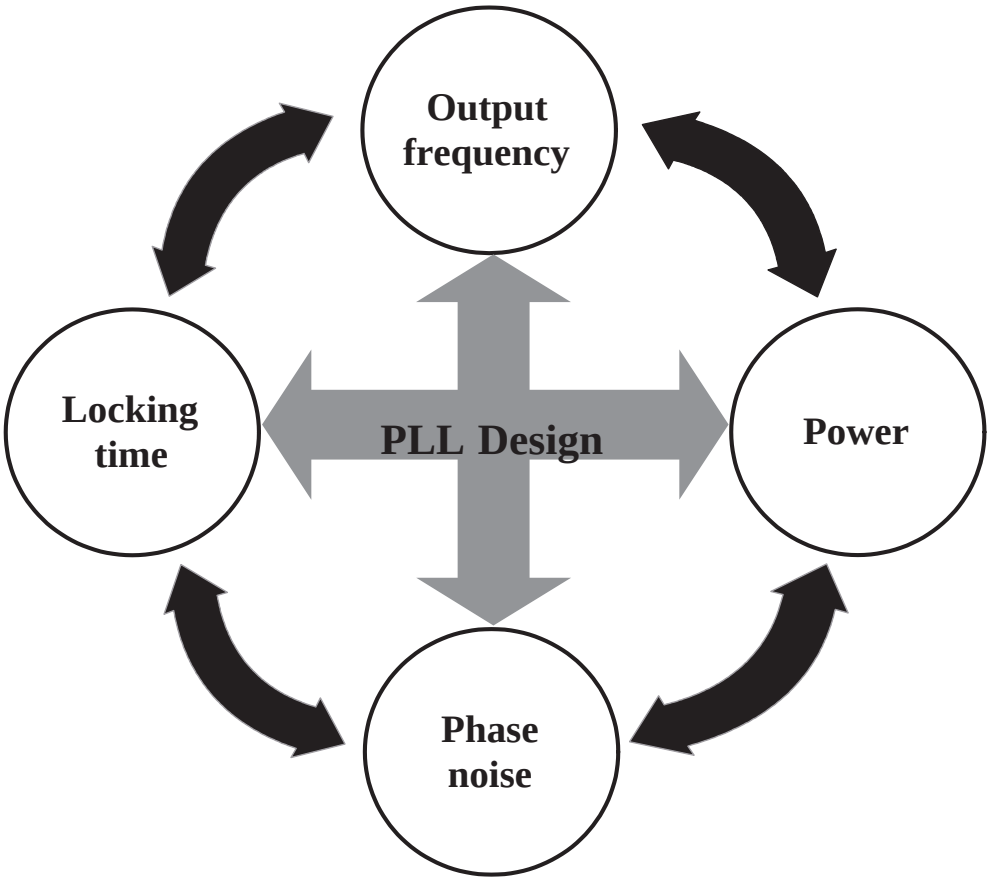

Figure 7.1: Characterization of PLL

7.2.1 A comprehensive model of Phase noise

To explore the noise property of the whole PLL it is obligatory to calculate the noise property of the PLL building blocks. A phase domain block diagram is exemplified in Figure 7.2 for the analysis of noise properties of the noise sources. For a second order passive lead lag low pass filter shown in Figure 2.10, the closed loop transfer function of the PLL is,

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{NK_{PFD}F(s)K_{VCO}}{N.s + K_{PFD}F(s)K_{VCO}} \tag{7.1}$$

where θ_{out} and θ_{in} are Phase of output and input signals of PLL, K_{PFD} is gain of the PFD $= I_{CP}/2\pi$, K_{VCO} is gain of the VCO$=\frac{\mu_n C_{Ox} W_n (V_{Cont} - V_{TH})}{nL_n C_L V_{DD}}$, F(s) is

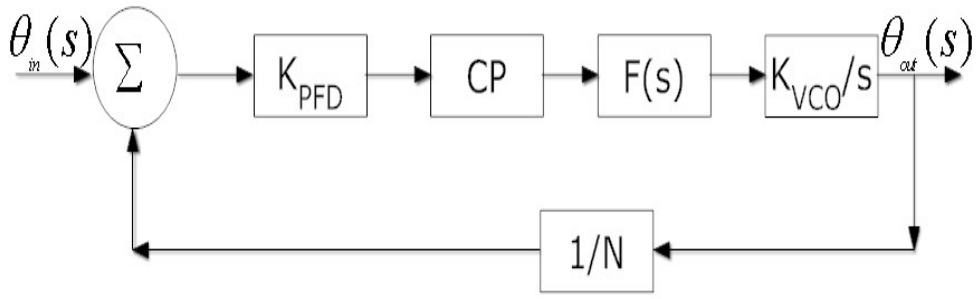

Figure 7.2: Phase domain block diagram of PLL

transfer function of the filter=$\frac{(1+s\tau)}{sC_1}$ (neglecting C_2 as it is $1/10^{th}$ of C_1), where τ=RC_1 N is divider ratio. The combined transfer function of the PFD and LPF can be written as,

$$K_{PFD}F(s) = \frac{I_{CP}}{2\pi C_1} \times \frac{1+s\tau}{s} \tag{7.2}$$

where I_{CP} is charge pump output current. Now (7.1) and (7.2) form the transfer function of the PLL as,

$$H(s) = \frac{N\left(\frac{I_{CP}}{2\pi C_1} * \frac{1+s\tau}{s}\right) K_{VCO}}{N.s + \left(\frac{I_{CP}}{2\pi C_1} * \frac{1+s\tau}{s}\right) K_{VCO}} \tag{7.3}$$

Taking K_{VCO} in Hz/V,

$$H(s) = \frac{N(1+s\tau)}{1+s\tau+\left[s^2 \Big/ \left(\frac{K_{VCO}I_{CP}}{NC_1}\right)\right]} \tag{7.4}$$

For a noisy VCO considering n_0(s) as the VCO input noise, the closed loop transfer function of the PLL is given as,

$$H(s) = \frac{\theta_{out}(s)}{n_0(s)} = \frac{2\pi C_1 N}{I_{CP}} \frac{s}{\left[s^2 \Big/ \left(\frac{K_{VCO}I_{CP}}{2\pi NC_1}\right)\right] + 1 + s\tau} \tag{7.5}$$

Expressing K_{VCO} in Hz/V,

$$\frac{\theta_{out}(s)}{n_0(s)} = \frac{2\pi C_1 N}{I_{CP}} \frac{s}{\left[s^2 \Big/ \left(\frac{K_{VCO} I_{CP}}{N C_1}\right)\right] + 1 + s\tau} \tag{7.6}$$

Now calculating the power spectrum density of θ_{out}(s),

$$\begin{aligned} S_{\theta_{Out}}(\omega) &= |n_0(j\omega)|^2 \left| \left(\frac{2\pi C_1 N}{I_{CP}}\right) \left[\frac{j\omega}{\left\{ \frac{-\omega^2}{\left(K_{VCO} I_{CP}/N C_1\right)} \right\} + j\omega\tau + 1} \right] \right|^2 \\ &= \frac{N_0}{2} \left(\frac{4\pi^2 C_1^2 N^2}{I_{CP}^2}\right) \left[\omega^2 \Big/ \left\{ 1 - \omega^2 \left(\frac{C_1 N}{K_{VCO} I_{CP}}\right) \right\}^2 + \omega^2 \tau^2 \right] \end{aligned} \tag{7.7}$$

where $N_0/2$ is the VCO input noise power, N_0=(F*k*T)/P, where F is the noise figure of the active device which is less than -130 dBc/Hz at 1 MHz offset, k is the Boltzmanns constant, T is the absolute room temperature and P is the power at the input of the VCO i.e. the product of charge pump output current and control voltage of the VCO.

7.2.2 Power consumption

The total power consumption of the PLL is contributed by each of its constituent blocks. Power consumed by each block and the total power consumed by all the blocks are also derived here.

The overall capacitance of the PFD is,

$$C_{PFD} = 24C_{Gate} + 11C_{P,Drain} + 13C_{n,Drain} \tag{7.8}$$

where C_{Gate} is the input or gate capacitance, $C_{p,Drain}$ is the drain capacitance at the output end of the PMOS, and $C_{n,Drain}$ is the drain capacitance at the output end of the NMOS. Now, considering this total capacitance and taking

N as the divider ratio, the power consumption by the PFD is estimated as,

$$P_{PFD} = C_{PFD}.V_{DD}^2 \frac{f_{VCO}}{N} \tag{7.9}$$

where f_{VCO}/N is the divided frequency of the VCO output signal as well as PFD feed back input signal.

At a particular instant the output current from CP (I_{CP}) either charges or discharges. The effective power consumption will be half of the total power. Hence the effective power consumption is,

$$P_{CP} = \frac{1}{2}\left(I_{CP} \times V_{DD}\right) \tag{7.10}$$

where,

$$I_{CP} = \frac{\left[\left|\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_n (V_{GS} - V_T)^2\right|\right]}{2} \tag{7.11}$$

The power dissipation in the CS-VCO has components of static power, short circuit power and dynamic power consumption. The static power dissipation in CMOS is due to leakage currents and is small in comparison to other components. In the operation of CMOS inverter current flow consists of two components, one due to output capacitor charging and discharging and the other due to current flowing straight from V_{DD} to ground. The power dissipated in charging and discharging the the load capacitances is known as the switching power. The component of the power dissipation due to the flow of current from V_{DD} to ground is called the short-circuit power dissipation.

The total power dissipated in a CMOS circuit is given by

$$P_{Total} = P_{Dynamic} + P_{ShortCircuit} + P_{Static} \tag{7.12}$$

The total capacitance of the VCO is,

$$\begin{aligned} C_{tot} &= C_{out} + C_{in} \\ &= C_{in} + C_{gd_p} + C_{db_p} + C_{gdov_n} + C_{db_n} + C_{gsov_n} + C_{gbov_n} \end{aligned} \tag{7.13}$$

where,

$$\begin{aligned} C_{in} &= \tfrac{2}{3} C_{ox} W_n L_n \\ C_{gd_p} &= C_{gdchannel_p} + C_{gdov_p} \\ C_{gdchannel_p} &= \tfrac{1}{2} C_{ox} W_p L_p \\ C_{db_n} &= \frac{Cj_n Ad_n}{\left(1+\frac{V_{DD}}{pb_n}\right)^{mj_n}} + \frac{Cjsw_n Pd_n}{\left(1+\frac{V_{DD}}{pbsw_n}\right)^{mjsw_n}} \\ C_{gdov_n} &= \left(1+\cos\left(\tfrac{\pi}{N}\right)\right) W_n C_{gdo_n} \\ C_{db_p} &= Cj_p Ad_p + Cjsw_p Pd_p \\ C_{gdov_p} &= W_p C_{gdo_p} \\ C_{gsov_n} &= W_n C_{gso} \\ C_{gbov_n} &= 2L_n C_{gbo} \\ C_{in} &= \tfrac{2}{3} C_{ox} W_n L_n \\ C_{gd_p} &= \tfrac{1}{2} C_{ox} W_p L_p \\ C_{db_n} &= \frac{Cj_n Ad_n}{\left(1+\frac{V_{dd}}{pb_n}\right)^{mj_n}} + \frac{Cjsw_n Pd_n}{\left(1+\frac{V_{dd}}{pbsw_n}\right)^{mjsw_n}} \\ C_{gdov_n} &= \left(1+\cos\left(\tfrac{\pi}{N}\right)\right) W_n C_{gdo_n} \\ C_{db_p} &= 2Cj_p Ad_p + 2Cjsw_p Pd_p \\ C_{gdov_p} &= W_p C_{gdo_p} \\ C_{gsov_n} &= W_n C_{gso} \\ C_{gbov_n} &= 2L_n C_{gbo} \end{aligned} \tag{7.14}$$

The parameters used above are C_j: zero-bias area junction capacitance, C_{jsw}: zero-bias sidewall junction capacitance, C_{gdo}: gate-drain overlap capacitance, pb: p-n junction potential, pbsw: p-n junction sidewall potential, m_j: area junction grading coefficient, mjsw: sidewall junction grading coefficient, A_d: drain area, P_d: drain perimeter, V_{DD}: the positive power supply voltage, and I_D: the drain current flowing through a single inverter stage.

Now the total power consumption of the VCO can be presented as

$$P_{VCO} = N \times C_{tot} \times V_{DD}^2 \times f_{VCO} \tag{7.15}$$

The power consumption of the divider having two D flip-flops is estimated as,

$$P_{Divider} = C_{Divider} \times V_{DD}^2 f_{VCO} \tag{7.16}$$

where,

$$C_{Divider} = \frac{1}{2}\left(12C_{Gate} + 6C_{Drain,n} + 6C_{Drain,p}\right) \tag{7.17}$$

$$\begin{aligned} P_{PLL} &= P_{PFD} + P_{VCO} + P_{CP} + P_{Div} + P_{LPF} \\ &= \left(\tfrac{C_{PFD}}{N} + nC_{VCO} + C_{Div}\right) V_{DD}^2 f_{VCO} + \tfrac{I_{CP}V_{DD}}{2} + I_{LPF}V_{Cont} \end{aligned} \tag{7.18}$$

where $P_{PFD}, P_{VCO}, P_{CP}, P_{Div}, P_{LPF}$ are the power consumptions by PFD, VCO, CP, divider and LPF circuits respectively. $C_{PFD}, C_{VCO}, andC_{Div}$ are the capacitances of PFD, VCO, and divider circuits respectively. V_{DD} and f_{VCO} are the power supply and operating frequency of the VCO respectively. I_{LPF} is the current through the loop filter. The power consumption of the LPF being less effective and small is not taken in to a count in the total power consumption expression.

7.2.3 Lock time

The lock in time of PLL is already discussed in 2. Considering the damping constant $\gamma = I_{CP}K_{VCO}\mathrm{R}/2\mathrm{N}$, the lock in time is approximately expressed as [103],

$$LT_{PLL} \approx \frac{10}{\gamma} = \frac{20N}{I_{CP}K_{VCO}R} \tag{7.19}$$

7.3 Optimizing the PLL performances

Though the designer can optimize the circuit in the netlist level, it is less effective and a time consuming iterative process and sometimes it is next to impossible for complex nanoscale circuits with large number of devices and

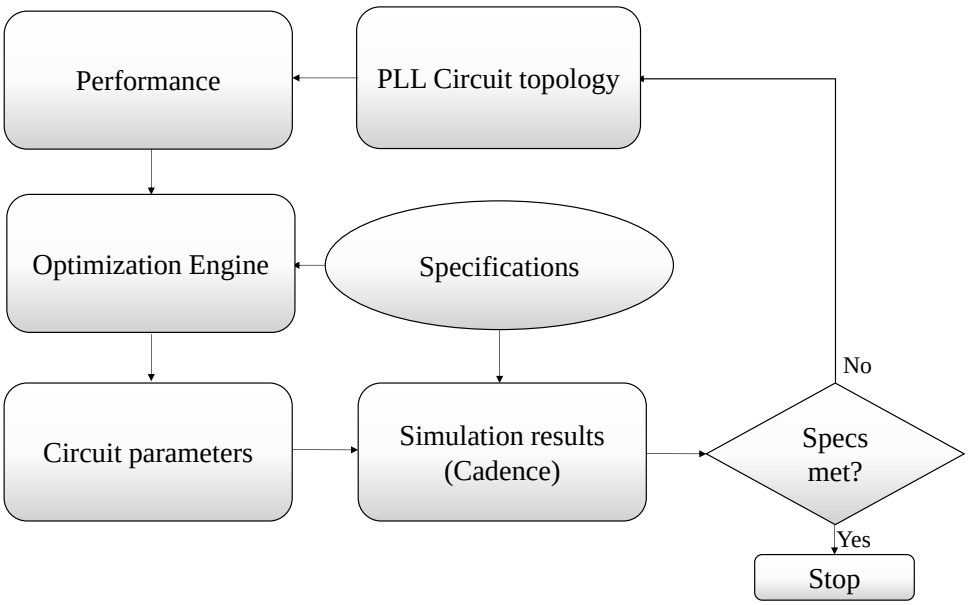

Figure 7.3: PLL design and optimization landscape

interconnects. Unlike traditional optimization methods, here the circuit parameters having trade-off among each other are mathematically modeled. Then a circuit optimization algorithm is developed by incorporating these models. This runs in a tool like MATLAB to provide the best result with the appropriate circuit parameters in a single run. Here the real advantage is that we do not need to change the parameters of the devices again and again. The near optimal performance parameters are obtained from the optimization tool. The complete process of PLL optimization is demonstrated in Figure 7.3.

There has been a ceaseless demand towards development of highly efficient computationally intelligent algorithms. Non-Dominated Sorting Genetic Algorithm-II (NSGA-II) [111] is a standard multi-objective optimization algorithm. However a better technique available would be an obvious choice among the designers.

Infeasibility driven evolutionary algorithm (IDEA) is a recently developed multiobjective optimization algorithm which has been reported in to offer superior performance [110], [112], [113].

Differing from others, IDEA is a proficient optimization technique in which the design parameters for optimal performance can be achieved for multiple objective functions. IDEA differs from NSGA-II mainly in the mechanism for elite preservation. In IDEA, a few infeasible solutions are retained in the population at every generation. Individual solutions in the population are evaluated as per the original problem definition with k objective and marked infeasible if any of the constraints are violated. To effectively search along the constraint boundary, the original k objective constrained optimization problem is reformulated as k + 1 objective unconstrained optimization problem. In IDEA, the first k objectives are the same as in the original constrained problem where as the additional objective is a measure of constraint violation, referred to as violation measure.

In NSGA-II, the elite preservation mechanism throws out the infeasible solutions from the population. To retain the infeasible solutions in the population, an alternate mechanism is required. In IDEA, the infeasible solutions are ranked higher than the feasible solutions, thus adding selection pressure to generate better infeasible solutions. Presence of infeasible solutions with higher ranks than the feasible solutions translates into an active search through the infeasible space.

This feature of IDEA accelerates the movement of solutions towards the constraint boundary. With the modified problem definition and ranking of the infeasible solutions higher than the feasible solutions, IDEA can find the solutions to the original problem more efficiently.

Algorithm for PLL performance optimization

If P is the Population Size
Customize Number of Generations: $P_G \geq 1$
Customize Proportion of infeasible solutions: $0 < \delta < 1$

1. Number of infeasible solutions, $P_{inf} = \delta * P$

2. Number of infeasible solutions, $P_f = P - P_{inf}$

3. while Parameter Constraints $PC = [W_{min} < W < W_{max}, L_{min} < L < L_{max}, R_{min} < R < R_{max}, C_{1min} < C_1 < C_{1max}, I_{CPmin} < I_{CP} < I_{CPmax}]\, do$

   4. Pop1 = Initialize () subject to PC

   5. Estimate $[S_{\theta_{Out}}(Pop1), P_{PLL}(Pop1), LT_{PLL}(Pop1)]$

   6. for $i = 2\, to\, P_G\, do$

      7. $childpop_{i-1} = evolve(pop_{i-1})$

      8. Estimate $[S_{\theta_{Out}}(childpop_{i-1}), P_{PLL}(childpop_{i-1}), LT_{PLL}(childpop_{i-1})]$

      9. Compute $T = |f_{PLL} - f_{desired}|$

      10. if Tolerance,T $\leq \delta$ *then* R_f *else* R_{inf} end if

      11. $(R_f, R_{inf}) = Split(pop_{i-1} + childpop_{i-1})$

      12. Rank(R_f)

      13. $Rank(R_{inf})$

      14. $pop_i = R_{inf}(1 : P_{inf}) + R_f(1 : P_f)$

   15. end for

16. end while

As our optimization is required for the PLL, the problem is stated as,

$$
\begin{aligned}
& Minimize\,[S_{\theta_{Out}}(f), P_{PLL}, LT_{PLL}] \\
& \left.\begin{aligned}
f_{PLL} &= f_{Specification} \\
W_{min} &< W < W_{max} \\
L_{min} &< L < L_{max} \\
R_{min} &< R < R_{max} \\
C_{1min} &< C_1 < C_{1max} \\
I_{CPmin} &< I_{CP} < I_{CPmax}
\end{aligned}\right\} Constraints
\end{aligned}
\quad subject\,to
$$

As shown in Figure 7.1 the PLL circuit is characterized for output frequency, power consumption, lock in time and phase noise, which are the major design objectives for any PLL. Here the mathematical model for phase noise (7.7) power consumption (7.18), and lock in time (7.19) of the PLL are considered as the objective functions for the optimization algorithm IDEA and the operating frequency, aspect ratios of different blocks, LPF components and charge pump current are taken as constraints. It is very important for the designer to know that the final design is accomplished by running IDEA engine only once and the physical layout has to be done for minimum number of times before the fabrication. Hence the design process is very fast.

7.4 Validation with the case of a PLL

The effectiveness of the proposed method is validated by simulating the PLL in Cadence Design Environment. Here the constraints of the LPF components, charge pump current and aspect ratios of transistors of VCO are satisfied Table 7.1 where the phase noise, lock in time and power consumption are optimized simultaneously.

In Table 7.2 the optimal design values predicted by IDEA and the values obtained by Cadence are demonstrated. The performance parameters are compared with the design by Jiang et al. [114].

Table 7.1: Design Parameters Constraints and values for Optimal Performance

Design Parameters	Lower Limit	Upper Limit	Optimal Value
W_n (nm)	120	2000	810
W_p (nm)	200	2000	1710
L (nm)	100	100	100
R (kΩ)	1	5	1.5
C_1 (pF)	1	6	1.05
I_{CP} (μA)	10	60	53

Table 7.2: Summary of performance parameters

Performance Indices	IDEA estimated	Cadence Validated	Jiang [114]
Output Frequency(GHz)	1	1.26	1.86
Phase Noise (dBc/Hz at 1 MHz offset)	-129.0	-126.3	-117.8
Lock time (ns)	44	50	20700
Lock range (GHz)	-	0.4-2.7	-
Referencespur (dBc/Hz)	-	-109	-88
Power Consumption (mW)	2.1	1.523	-

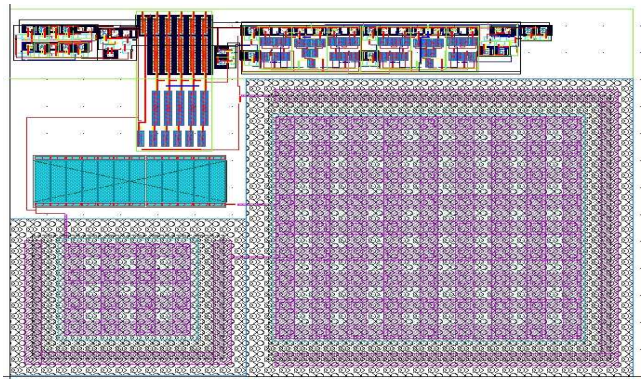

Figure 7.4: Chip layout of the complete 1.26 GHz PLL

The physical layout of the complete PLL designed to operate at 1.26 GHz is presented in Figure 7.4. The transient analysis is shown in Figure 7.5. It is observed that the PLL locks at 50 ns with an output frequency of 1 GHz. The lock range of the PLL is estimated to be 0.4 to 2.7 GHz.

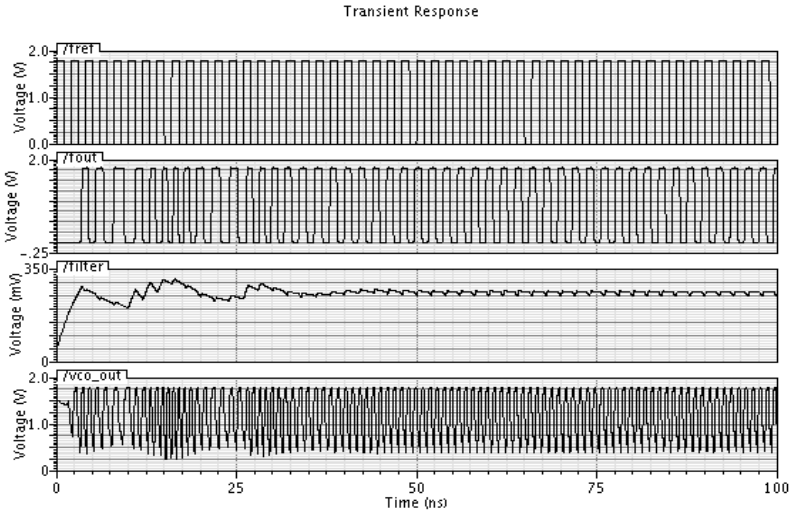

Figure 7.5: Transient analysis of the PLL

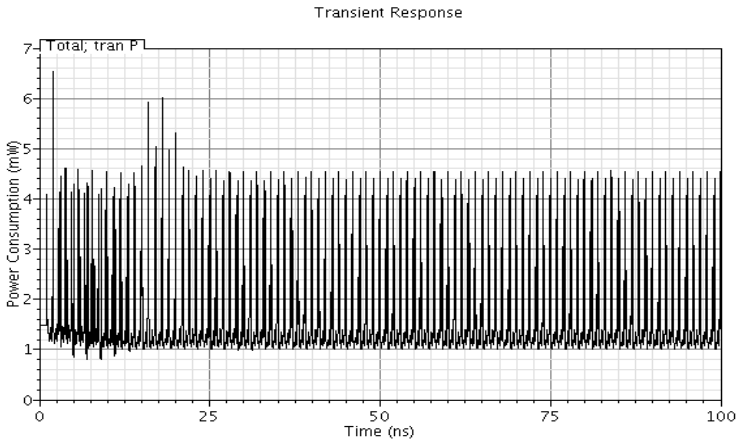

Figure 7.6: Power consumption of the PLL

The values of R and C of the LPF taken here for design are well within the limit and are very less in comparison to the design of Jiang et al. [114] which traditionally reduce the silicon area and improve the operating frequency. The phase noise and lock in time achieved here is also very less than that reported in the design by Jiang et al. [114]. Average power consumption and phase noise plots of the PLL are shown in Figure 7.6 and Figure 7.7 respectively.

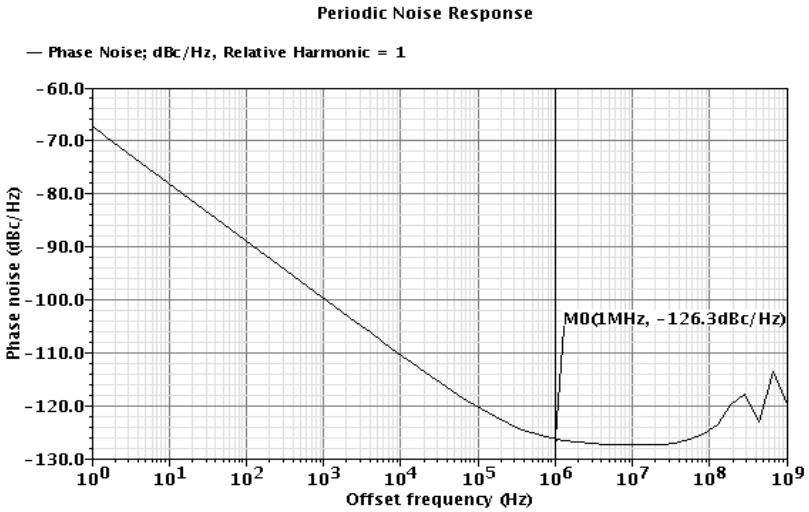

Figure 7.7: Phase noise variation with offset frequency of the PLL

7.5 Conclusion

Phase noise and power consumption of the CMOS PLL are modeled and then considered for optimization along with lock time to achieve a targeted frequency of oscillation in a technology constrained environment. The design parameters obtained from IDEA algorithm are used to perform a schematic and physical layout level CMOS PLL design in the Cadence Virtuoso Analog Design Environment. Subsequently, for the demonstration of the methodology, the PLL performance parameters are estimated from the transient and noise analysis in Cadence tool and are compared with their estimated optimal values. The R and C values of the filter are very less, hence the area of the designed PLL is appreciably less. So, this design methodology benefits the designer in industry to deliver a product with optimal performance in significantly less time.

Chapter 8

Conclusions and scope for future research

8.1 General Conclusions

The research studies of the performance linked PLL components along with their design challenges are addressed in this thesis. The phase locked loop (PLL) design has multiple challenges which provide trade offs among the performance parameters. Variety of techniques have been applied to have better PLL performance.

The investigations conducted in this research work contribute to the following outcomes.

i. A technique that reduces the dead zone, resulting in better phase noise performance has been proposed where a PLL incorporating a PFD with a voltage variable delay element in its reset path is designed. By proper parameter selection of the PFD and adjusting the charge pump current and the loop filter component values, a better lock time is achieved.

ii. An adaptive dual PFD architecture is proposed for the PLL to simultaneously achieve low phase noise and low lock time. In this work phase noise analysis of the incorporated PFDs have been carried out and the comparison

between the calculated and simulated results are presented. This PLL can be applied where both the noise and speed are of primary concern.

iii. A high performance transmission gate cascode current mirror charge pump is designed and implemented to reduce the non ideal effects which ultimately reduces the reference spur level of the PLL. To reduce the current mismatch a single current source is employed in this work.

iv. An adaptive duty cycle control (ADCC) strategy is proposed for the divider circuit in a PLL to alleviate the shift of the base line of the divider output signal which occurs due to the manufacturing process variation effects.

v. A multi objective optimization algorithm is applied to improve multiple performance parameters of a general charge pump PLL. This design procedure benefits the designer in industry to deliver a product in significantly less time with optimal performance .

8.2 Limitations and scope for future research

Though this thesis came up with some solutions to improve the overall performance of the PLL, there still exists some limitations and the research can further be extended in some other dimensions.

8.2.1 Limitations

i. The dead zone due to the PFD could not be made zero though it is under control up to a healthy extent.

ii. In dual PFD architecture 4, due to the inclusion of additional capacitors the layout area becomes larger.

iii. The power consumption of the PLL can further be reduced by using power reduction strategies.

iv. Parasitic aware multi performance optimization can be carried out for the PLL.

v. The measured results of the ADCC PLL have not been included in the thesis because the chip is yet to be fabricated.

8.2.2 Scope for future research

i. The proposed work can be implemented for performance verification in lower technologies like 65 nm or 45 nm.

ii. The leakage current can be included in analysis of PLL for near about 100 nm technology.

iii. Low power techniques can be proposed to reduce the power consumption further.

iv. To reduce the phase noise, other type of VCO circuits like LC-VCO can be employed in the PLL.

v. More number of fabrication process variation parameters can be included for PLL design optimization.

Bibliography

[1] F. M. Gardner, *Phaselock Techniques*. 3rd ed. New York: Wiley-Interscience, 2005.

[2] J. P. Frazier, "Phase-lock loop frequency acquisition study," *IRE Transactions on Space Electronics and Telemetry*, vol. 8, no. 3, pp. 210–227, September 1962.

[3] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Transactions on Communications*, vol. 28, no. 11, pp. 1849–1858, November 1980.

[4] R. E. Best, *Phase Locked Loops Design, Simulation and Applications*. McGraw-Hill Publication, 5th Edition, 2003.

[5] W. C. Lindsey and C. M. Chie, *Phase-Locked Loops*. New York. IEEE Press, 1986.

[6] C. Toumazou, G. S. Moschytz, and B. Gilbert, *Trade-Offs in Analog Circuit Design: The Designer's Companion*. New York: Springer- Verlag, 2004.

[7] A. Homayoun and B. Razavi, "Analysis of phase noise in phase/frequency detectors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 529–539, 2013.

[8] I. Thompson and P. Brennan, "Phase noise contribution of the phase/frequency detector in a digital PLL frequency synthesisers," *IEE Proceedings of Circuits, Devices and Systems*, vol. 150, no. 1, pp. 1–5, 2003.

[9] W. Kester, "Converting oscillator phase noise to time jitter," *Tutorial MT-008, Analog Devices*, 2009.

[10] D. Mandal, P. Mandal, and T. K. Bhattacharyya, "Prediction of reference spur in frequency synthesisers," *Circuits, Devices & Systems, IET*, vol. 9, no. 2, pp. 131–139, 2015.

[11] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation.* IEEE Press Series on Microelectronic Systems, 2002.

[12] C. T. Charles and D. J. Allstot, "A calibrated phase/frequency detector for reference spur reduction in charge-pump PLLs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 9, pp. 822–826, 2006.

[13] J. Strzelecki and S. Ren, "Near-zero dead zone phase frequency detector with wide input frequency difference," *Electronics Letters*, vol. 51, no. 14, pp. 1059–1061, 2015.

[14] G. S. Singh, D. Singh, and S. Moorthi, "Low power low jitter phase locked loop for high speed clock generation," in *2012 Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, 2012, pp. 192–196.

[15] B. Razavi, *Design of Analog CMOS Integrated Circuits.* McGraw-Hill Publication, 2000.

[16] Razavi, *Phase-Locking in High-Performance Systems: From Devices to Architectures.* Wiley-IEEE Press, 2003.

[17] Crowley, *Phase locked loop with variable gain and bandwidth.* U.S. Patent 4,156,855, 1979.

[18] M. Ugarte and A. Carlosena, "Performance Comparison and Design Guidelines for Type II and Type III PLLs," *Circuits, Systems, and Signal Processing*, vol. 34, no. 10, pp. 3395–3408, 2015.

[19] D. Mandal and T. Bhattacharyya, "Implementation of CMOS low-power integer-N frequency synthesizer for SOC design," *Journal of Computers*, vol. 3, no. 4, pp. 31–38, 2008.

[20] G. Villar, E. Alarcón, E. Vidal, J. Cosp, and J. Madrenas, "Synchronizable Compact CMOS Oscillator," *Analog Integrated Circuits and Signal Processing*, vol. 42, no. 2, pp. 179–183, 2005.

[21] M. Aqeeli, A. Alburaikan, X. Huang, and Z. Hu, "Wide tuning range voltage controlled oscillator (VCO) with minimized phase noise variation in nanoscale CMOS technology," in *15th International Conference on Nanotechnology (IEEE-NANO)*. IEEE, 2015, pp. 51–54.

[22] H. O. Johansson, "A simple precharged CMOS phase frequency detector," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 295–299, 1998.

[23] H. Kondoh, H. Notani, T. Yoshimura, H. Shibata, and Y. Matsuda, "A 1.5-V 250-MHz to 3.0-V 622-MHz operation CMOS phase-locked loop with precharge type phase-frequency detector," *IEICE transactions on electronics*, vol. 78, no. 4, pp. 381–388, 1995.

[24] M. Mansuri, D. Liu, and C.-K. Yang, "Fast frequency acquisition phase-frequency detectors for GSa/s phase-locked loops," in *Proceedings of the 27th European Solid-State Circuits Conference, ESSCIRC 2001*. IEEE, 2001, pp. 333–336.

[25] W. Hu, L. Chunglen, and X. Wang, "Fast frequency acquisition phase-frequency detector with zero blind zone in PLL," *Electronics Letters*, vol. 43, no. 19, pp. 1018–1020, 2007.

[26] W.-H. Chen, M. E. Inerowicz, and B. Jung, "Phase frequency detector with minimal blind zone for fast frequency acquisition," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 12, pp. 936–940, 2010.

[27] H. S. Raghav, S. Maheshwari, M. Srinivasarao, and B. P. Singh, "Design of low power, low jitter DLL tested at all five corners to avoid false locking," in *10th IEEE International Conference on Semiconductor Electronics (ICSE), 2012*, 2012, pp. 526–531.

[28] K. K. A. Majeed and B. J. Kailath, "Low power, high frequency, free dead zone PFD for a PLL design," in *2013 IEEE Faible Tension Faible Consommation (FTFC)*. IEEE, 2013, pp. 1–4.

[29] S. Laha and S. Kaya, "Dead zone free area efficient charge pump phase frequency detector in nanoscale DG-MOSFET," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2013, pp. 920–923.

[30] A. C. Kailuke, P. Agrawal, and R. V. Kshirsagar, "Design of phase frequency detector and charge pump for low voltage high frequency PLL," in *2014 International Conference on Electronic Systems, Signal Processing and Computing Technologies (ICESC)*. IEEE, 2014, pp. 74–78.

[31] I. A. Carlos Quemada, Guillermo Bistue, *Design Methodology for RF CMOS Phase Locked Loops*. Artech Publications, Boston, 2009.

[32] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 11, pp. 1723–1732, 1996.

[33] M. M. Kamal, E. W. El-Shewekh, and M. H. El-Saba, "Design and implementation of a low-phase-noise integrated CMOS Frequency Synthesizer for high-sensitivity narrow-band FM transceivers," in *Proceedings of*

the 15th International Conference on Microelectronics, 2003. ICM 2003. IEEE, 2003, pp. 167–175.

[34] D.-C. Juang, D.-S. Chen, J.-M. Shyu, and C.-Y. Wu, "A low-power 1.2 GHz 0.35 μm CMOS PLL," in *Proceedings of the Second IEEE Asia Pacific Conference on ASICs, 2000. AP-ASIC 2000.* IEEE, 2000, pp. 99–102.

[35] C. Zhang and M. Syrzycki, "Modifications of a Dynamic-Logic Phase Frequency Detector for extended detection range," in *53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS).* IEEE, 2010, pp. 105–108.

[36] W.-H. Lee, J.-D. Cho, and S.-D. Lee, "A high speed and low power phase-frequency detector and charge-pump," in *Proceedings of the ASP-DAC'99. Asia and South Pacific Design Automation Conference, 1999.* IEEE, 1999, pp. 269–272.

[37] G. Y. Tak, S. B. Hyun, T. Y. Kang, B. G. Choi, G. Byoung, and S. S. Park, "A 6.3-9-GHz CMOS fast settling PLL for MB-OFDM UWB applications," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 8, pp. 1671–1679, 2005.

[38] G. Lee, P. Chan, and L. Siek, "A CMOS phase frequency detector for charge pump phase-locked loop," in *42nd Midwest Symposium on Circuits and Systems, 1999*, vol. 2. IEEE, 1999, pp. 601–604.

[39] K.-H. Cheng, T.-H. Yao, S.-Y. Jiang, and W.-B. Yang, "A difference detector PFD for low jitter PLL," in *The 8th IEEE International Conference on Electronics, Circuits and Systems, 2001. ICECS 2001*, vol. 1. IEEE, 2001, pp. 43–46.

[40] M. Renaud and Y. Savaria, "A CMOS three-state frequency detector complementary to an enhanced linear phase detector for PLL, DLL or

high frequency clock skew measurement," in *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS'03*, vol. 3. IEEE, 2003, pp. III–148.

[41] K.-S. Lee, B.-H. Park, H.-i. Lee, and M. J. Yoh, "Phase frequency detectors for fast frequency acquisition in zero-dead-zone CPPLLs for mobile communication systems," in *Proceedings of the 29th European Solid-State Circuits Conference, 2003. ESSCIRC'03.* IEEE, 2003, pp. 525–528.

[42] C.-P. Chou, Z.-M. Lin, and J.-D. Chen, "A 3-ps dead-zone double-edge-checking phase-frequency-detector with 4.78 GHz operating frequencies," in *The 2004 IEEE Asia-Pacific Conference on Circuits and Systems, 2004. Proceedings*, vol. 2. IEEE, 2004, pp. 937–940.

[43] N. M. Ismail and M. Othman, "CMOS phase frequency detector for high speed applications," in *4th International Design and Test Workshop (IDT), 2009.* IEEE, 2009, pp. 1–5.

[44] J. Lan, Y. Wang, L. Liu, and R. Li, "A nonlinear phase frequency detector with zero blind zone for fast-locking phase-locked loops," in *International Conference on Anti-Counterfeiting, Security and Identification*, 2010, pp. 41–44.

[45] J. Lee and B. Kim, "A low-noise fast-lock phase-locked loop with adaptive bandwidth control," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1137–1145, 2000.

[46] C. S. Vaucher, "An adaptive PLL tuning system architecture combining high spectral purity and fast settling time," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 490–502, 2000.

[47] J. Kim, M. A. Horowitz, and G.-Y. Wei, "Design of CMOS adaptive-bandwidth PLL/DLLs: a general approach," *IEEE Transactions on*

Circuits and Systems II: Analog and Digital Signal Processing, vol. 50, no. 11, pp. 860–869, 2003.

[48] T.-W. Liao, J.-R. Su, and C.-C. Hung, "Spur-reduction frequency synthesizer exploiting randomly selected PFD," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 3, pp. 589–592, 2013.

[49] Y. Woo, Y. M. Jang, and M. Y. Sung, "Phase-locked loop with dual phase frequency detectors for high-frequency operation and fast acquisition," *Microelectronics journal*, vol. 33, no. 3, pp. 245–252, 2002.

[50] Y.-F. Kuo, R.-M. Weng, and C.-Y. Liu, "A fast locking PLL with phase error detector," in *2005 IEEE Conference on Electron Devices and Solid-State Circuits*. IEEE, 2005, pp. 423–426.

[51] K. M. Ware, H.-S. Lee, and C. G. Sodini, "A 200-MHz CMOS phase-locked loop with dual phase detectors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 6, pp. 1560–1568, 1989.

[52] K.-H. Cheng, W.-B. Yang, and C.-M. Ying, "A dual-slope phase frequency detector and charge pump architecture to achieve fast locking of phase-locked loop," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 11, pp. 892–896, 2003.

[53] W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," in *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, ISCAS'99*, vol. 2. IEEE, 1999, pp. 545–548.

[54] Y.-S. Choi and Dae-HyunHan, "Gain-boosting charge pump for current matching in phase-locked loop," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 10, pp. 1022–1025, 2006.

[55] R. H. Mekky and M. Dessouky, "Design of a low-mismatch gain-boosting charge pump for phase-locked loops," in *Internatonal Conference on Microelectronics, 2007. ICM 2007.* IEEE, 2007, pp. 321–324.

[56] J. Zhou and Z. Wang, "A high-performance CMOS charge-pump for phase-locked loops," in *International Conference on Microwave and Millimeter Wave Technology, 2008. ICMMT 2008*, vol. 2. IEEE, 2008, pp. 839–842.

[57] J.-S. Lee, M.-S. Keel, S.-I. Lim, and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," *Electronics Letters*, vol. 36, no. 23, pp. 1907–1908, 2000.

[58] M. El-Hage and F. Yuan, "Architectures and design considerations of CMOS charge pumps for phase-locked loops," in *Canadian Conference on Electrical and Computer Engineering, IEEE CCECE 2003*, vol. 1. IEEE, 2003, pp. 223–226.

[59] M.-S. Hwang, J. Kim, and D.-K. Jeong, "Reduction of pump current mismatch in charge-pump PLL," *Electronics letters*, vol. 45, no. 3, pp. 135–136, 2009.

[60] N. Hou and Z. Li, "Design of high performance CMOS charge pump for phase-locked loops synthesizer," in *15th Asia-Pacific Conference on Communications, 2009. APCC 2009.* IEEE, 2009, pp. 209–212.

[61] M. Jung, A. Ferizi, and R. Weigel, "A chargepump with enhanced current matching and reduced clock-feedthrough in wireless sensor nodes," in *2010 Asia-Pacific Microwave Conference Proceedings (APMC).* IEEE, 2010, pp. 2291–2294.

[62] C. Zhang, T. Au, and M. Syrzycki, "A high performance NMOS-switch high swing cascode charge pump for phase-locked loops," in *IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), 2012.* IEEE, 2012, pp. 554–557.

[63] N. Kamal, S. Al-Sarawi, and D. Abbott, "Reference spur suppression technique using ratioed current charge pump," *Electronics Letters*, vol. 49, no. 12, pp. 746–747, 2013.

[64] M. Hassani and S. Saeedi, "Edge-combining multi-phase DLL frequency multiplier with reduced static phase offset and linearized delay transfer curve," *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 3, pp. 705–718, 2015.

[65] A. Khateb, V. Musil, and R. Prokop, "Rail-to-rail bulk-driven amplifier," *Electronics, Sept*, 2005.

[66] R. A. Baki and M. N. El-Gamal, "A new CMOS charge pump for low-voltage (1V) high-speed PLL applications," in *Proceedings of the International Symposium on Circuits and Systems, ISCAS'03*, vol. 1. IEEE, 2003, pp. I–657.

[67] B. Terlemez and J. Uyemura, "The design of a differential CMOS charge pump for high performance phase-locked loops," in *Proceedings of the 2004 International Symposium on Circuits and Systems, ISCAS'04*, vol. 4. IEEE, 2004, pp. IV–561.

[68] Z. Tao, Z. Xuecheng, and S. Xubang, "A CMOS charge pump with a novel structure in PLL," in *Proceedings of 7th International Conference on Solid-State and Integrated Circuits Technology*, vol. 2, 2004, pp. 1555–1558.

[69] H. Yu, Y. Inoue, and Y. Han, "A new high-speed low-voltage charge pump for PLL applications," in *6th International Conference On ASIC, ASICON 2005*, vol. 1. IEEE, 2005, pp. 387–390.

[70] S. J. Byun, B. Kim, and C.-H. Park, "Charge pump circuit for a PLL," October 4 2005, US Patent 6,952,126.

[71] Y. Sun, L. Siek, and P. Song, "Design of a high performance charge pump circuit for low voltage phase-locked loops," in *International Symposium on Integrated Circuits, ISIC'07*. IEEE, 2007, pp. 271–274.

[72] K.-S. Ha and L.-S. Kim, "Charge-pump reducing current mismatch in DLLs and PLLs," in *ISCAS*, 2006.

[73] N. T. Hieu, T.-W. Lee, and H.-H. Park, "A perfectly current matched charge pump of CP-PLL for chip-to-chip optical link," in *Conference on Lasers and Electro-Optics/Pacific Rim*. Optical Society of America, 2007, pp. 1–2.

[74] C.-F. Liang, S.-H. Chen, and S.-I. Liu, "A digital calibration technique for charge pumps in phase-locked systems," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 390–398, 2008.

[75] W.-M. Lin, S.-I. Liu, C.-H. Kuo, C.-H. Li, Y.-J. Hsieh, and C.-T. Liu, "A Phase-Locked Loop With Self-Calibrated Charge Pumps in 3-LTPS-TFT Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 142–146, 2009.

[76] W.-H. Chiu, T.-S. Chang, and T.-H. Lin, "A charge pump current missmatch calibration technique for Δ-Σ fractional-N PLLs in 0.18-μm CMOS," in *IEEE Asian Solid-State Circuits Conference, A-SSCC 2009*. IEEE, 2009, pp. 73–76.

[77] L. Zhiqun, Z. Shuangshuang, and H. Ningbing, "Design of a high performance CMOS charge pump for phase-locked loop synthesizers," *Journal of Semiconductors*, vol. 32, no. 7, 2011.

[78] Y.-W. Chen, Y.-H. Yu, and Y.-J. Chen, "A 0.18-m CMOS Dual-Band Frequency Synthesizer With Spur Reduction Calibration," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 10, pp. 551–553, 2013.

[79] M. Brandolini, P. Rossi, D. Manstretta, and F. Svelto, "Toward multi-standard mobile terminals-fully integrated receivers requirements and architectures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 3, pp. 1026–1038, 2005.

[80] J. W. M. Rogers, F. F. Dai, M. S. Cavin, and D. G. Rahn, "A multiband Δ-Σ fractional-N frequency synthesizer for a MIMO WLAN transceiver RFIC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 678–689, 2005.

[81] N. H. W. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. F. Wagner, C. Plett, and N. G. Tarr, "Design of wide-band CMOS VCO for multi-band wireless LAN applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1333–1342, 2003.

[82] R. Holzer, "A 1 V CMOS PLL designed in high-leakage CMOS process operating at 10-700 MHz," in *IEEE International Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC 2002*, vol. 1. IEEE, 2002, pp. 272–466.

[83] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 5, pp. 717–724, 1999.

[84] P. Liu, P. Upadhyaya, J. Jung, D. Heo, J.-H. Kim, and B.-S. Kim, "Low phase noise LC VCO with reduced drain current duty cycle," *Electronics letters*, vol. 48, no. 2, pp. 77–78, 2012.

[85] P. Andreani and S. Mattisson, "On the use of MOS varactors in RF VCOs," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 6, pp. 905–910, 2000.

[86] C.-H. Heng, A. Bansal, and Y. Zheng, "Design of 1.94-GHz CMOS noise-cancellation VCO," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 59, no. 2, pp. 368–374, 2011.

[87] P. Pereira, M. H. Fino, and M. Ventim-Neves, "Optimal LC-VCO design through evolutionary algorithms," *Analog Integrated Circuits and Signal Processing*, vol. 78, no. 1, pp. 99–109, 2014.

[88] K.-S. Lee, E.-Y. Sung, I. C. Hwang, and B.-H. Park, "Fast AFC technique using a code estimation and binary search algorithm for wideband frequency synthesis," in *Proceedings of the 31st European Solid-State Circuits Conference, ESSCIRC 2005.* IEEE, 2005, pp. 181–184.

[89] M. Saadat, M. Momtazpour, and B. Alizadeh, "Simulation and improvement of two digital adaptive frequency calibration techniques for fast locking wide-band frequency synthesizers," in *Design & Technology of Integrated Systems in Nanoscale Era, 2007. DTIS. International Conference on.* IEEE, 2007, pp. 136–141.

[90] H. Zhang, "A broadband VCO with an adaptive frequency calibration circuit," *International Journal of Digital Content Technology and its Applications*, vol. 6, no. 17, 2012.

[91] Y. Yadong, Y. Yuepeng, L. Weiwei, and D. Zhankun, "A fast lock frequency synthesizer using an improved adaptive frequency calibration," *Journal of Semiconductors*, vol. 31, no. 6, pp. 5–11, 2010.

[92] T.-H. Lin and W. J. Kaiser, "A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 424–431, 2001.

[93] H. Lee, J.-K. Cho, K.-S. Lee, I. C. Hwang, T.-W. Ahn, K.-S. Nah, and Byeong-HaPark, "A Σ-Δ fractional-N frequency synthesizer using

a wide-band integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1164–1169, 2004.

[94] J. Shin and H. Shin, "A fast and high-precision VCO frequency calibration technique for wideband fractional-n frequency synthesizers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1573–1582, 2010.

[95] A. Arakali, S. Gondi, and P. K. Hanumolu, "Analysis and design techniques for supply-noise mitigation in phase-locked loops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 11, pp. 2880–2889, 2010.

[96] A. El Mourabit, G.-N. Lu, P. Pittet, Y. Birjali, and F. Lahjomri, "Low power, high resolution CMOS variable-delay element," *AEU-International Journal of Electronics and Communications*, vol. 66, no. 6, pp. 455–458, 2012.

[97] X. Xiaoliang, L. Huihua, and A. Siyan, "Design of low phase noise and fast locking PLL frequency synthesizer," in *International Conference on Electric Information and Control Engineering (ICEICE)*, 2011, pp. 4113–4116.

[98] N. R. Mahapatra, A. Tareen, and S. V. Garimella, "Comparison and analysis of delay elements," in *45th Midwest Symposium on Circuits and Systems*, vol. 2. IEEE, 2002, pp. II–473.

[99] W.-Y. Shin, M. Kim, G.-M. Hong, and S. Kim, "A fast-acquisition PLL using split half-duty sampled feedforward loop filter," *IEEE Transactions on Consumer Electronics*, vol. 56, no. 3, pp. 1856–1859, 2010.

[100] J. S. Lee, W. K. Jin, D. M. Choi, G. S. Lee, and S. Kim, "A wide range PLL for 64X speed CD-ROMs & 10X speed DVD-ROMs," *IEEE Transactions on Consumer Electronics*, vol. 46, no. 3, pp. 487–493, 2000.

[101] S.-J. Li, H.-H. Hsieh, and L.-H. Lu, "A 10 GHz Phase-Locked Loop With a Compact Low-Pass Filter in 180 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 10, pp. 659–661, 2009.

[102] P. K. Hanumolu, M. Brownlee, K. Mayaram, and U.-K. Moon, "Analysis of charge-pump phase-locked loops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 9, pp. 1665–1674, 2004.

[103] F. Herzel, A. Ergintav, and Y. Sun, "Phase Noise Modeling for Integrated PLLs in FMCW Radar," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 3, pp. 137–141, 2013.

[104] J. Yau and S. H.-L. Tu, "A high-speed frequency acquisition PLL using phase frequency detector with variable gain," in *53rd IEEE International Midwest Symposium on Circuits and Systems*. IEEE, 2010, pp. 101–104.

[105] D.-S. Lee, J.-H. Jang, H.-G. Park, Y. Pu, K. C. Hwang, Y. Yang, M.-K. Seo, and K.-Y. Lee, "A Wide-Locking-Range Dual Injection-Locked Frequency Divider With an Automatic Frequency Calibration Loop in 65-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 4, pp. 327–331, 2015.

[106] B. Song, J. Lee, K. Kim, and J. Burm, "A fast AFC technique with self-calibration for fast-locking PLLs," *International Journal of Electronics*, vol. 100, no. 8, pp. 1080–1091, 2013.

[107] R. Jain, H. Rucker, and N. R. Mohapatra, "Optimization of si mos transistors for thz detection using tcad simulation," in *Simulation of Semiconductor Processes and Devices (SISPAD), 2014 International Conference on*. IEEE, 2014, pp. 213–216.

[108] P. K. Rout, D. P. Acharya, and G. Panda, "A multiobjective optimization based fast and robust design methodology for low power and low phase noise current starved VCO," *IEEE Transactions on Semiconductor Manufacturing*, vol. 27, no. 1, pp. 43–50, 2014.

[109] O. Garitselov, S. P. Mohanty, and E. Kougianos, "A comparative study of metamodels for fast and accurate simulation of nano-CMOS circuits," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 1, pp. 26–36, 2012.

[110] T. Ray, H. K. Singh, A. Isaacs, and W. Smith, "Infeasibility driven evolutionary algorithm for constrained optimization," in *Constraint-handling in evolutionary optimization*. Springer, 2009, pp. 145–165.

[111] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A Fast and Elitist Multi-Objective Genetic Algorithm: NSGA-II," pp. 182–197, 2002.

[112] H. K. Singh, A. Isaacs, T. T. Nguyen, T. Ray, and X. Yao, "Performance of infeasibility driven evolutionary algorithm (IDEA) on constrained dynamic single objective optimization problems," in *IEEE Congress on Evolutionary Computation*. IEEE, 2009, pp. 3127–3134.

[113] A. Saha, T. Ray, and W. Smith, "Towards practical evolutionary robust multi-objective optimization," in *IEEE Congress on Evolutionary Computation*. IEEE, 2011, pp. 2123–2130.

[114] B. Jiang, T. Xia, and G. Wang, "PLL low pass filter design considering unified specification constraints," *Analog Integrated Circuits and Signal Processing*, vol. 80, no. 1, pp. 113–120, 2014.