# Power Integrity Analysis for Jitter Characterization

**Linson Thomas**


Department of Electronics and Communication Engineering
**National Institute of Technology Rourkela**

# Power Integrity Analysis for Jitter Characterization

*A thesis submitted in partial fulfillment*

*of the requirements of the degree of*

***Master of Technology***

*In*

***Electronics and Communication Engineering***

***(Specialization: VLSI Design and Embedded Systems)***

*by*


***Linson Thomas***

ROLL NO: 214EC2185


*based on the research carried out*

*under the supervision of*

***Prof. K. K. Mahapatra***


May 2016


Department of Electronics and Communication Engineering

**National Institute of Technology Rourkela**

Department of Electronics and Communication Engineering
**National Institute of Technology Rourkela**

**Prof. K. K. Mahapatra**
Professor

May 31, 2016

# Supervisors' Certificate

This is to certify that the work presented in the thesis entitled *Power Integrity Analysis for Jitter Characterization* submitted by *Linson Thomas*, Roll Number 214EC2185, is a record of original research carried out by him under our supervision and guidance in partial fulfillment of the requirements of the degree of *Master of Technology* in *VLSI Design and Embedded Systems.* Neither this thesis nor any part of it has been submitted earlier for any degree or diploma to any institute or university in India or abroad.

Prof. K. K. Mahapatra
Supervisor

*Dedicated to*

*My beloved family*

# Declaration of Originality

I, *Linson Thomas*, Roll Number *214EC2185* hereby declare that this thesis entitled *Power Integrity Analysis for Jitter Characterization* presents my original work carried out as a master student of NIT Rourkela and, to the best of my knowledge, contains no material previously published or written by another person, nor any material presented by me for the award of any degree or diploma of NIT Rourkela or any other institution. Any contribution made to this research by others, with whom I have worked at NIT Rourkela or elsewhere, is explicitly acknowledged in the thesis. Works of other authors cited in this thesis have been duly acknowledged under the section "Bibliography". I have also submitted my original research records to the scrutiny committee for evaluation of my thesis.

I am fully aware that in case of any non-compliance detected in future, the senate of NIT Rourkela may withdraw the degree awarded to me on the basis of present thesis.

May 31, 2016

*Linson Thomas*

NIT Rourkela

# Acknowledgement

The years I spent at the National Institute of Technology have been full of unforgettable memories. Thanks to many people who deserve my highest gratitude.

First of all, I am deeply grateful to my academic advisor, Prof. K. K. Mahapatra for the constant support at each step of the process.

I would also like to express my appreciation to the Department of Electronics and Communication Engineering, specifically the team of VLSI and Embedded Systems for providing such a friendly and encouraging environment with all the required tools to support high quality academic research. I express my genuine appreciation to Prof. A. K. Swain, Prof. D. P. Acharya and Prof. Nurul Islam, who had presented the universe of VLSI and Embedded System and helped me learning different areas of my specialization.

I am very grateful to Mr. Pratik Damle of S. T. Microelectronics for his mentorship and significant contribution to my academic research. I express my soulful gratitude to him for their invaluable guidance for my training and completion of thesis. I am truly appreciative to all my colleagues and different companions who had made my stay at NIT Rourkela and S.T. Microelectronics a charming experience.

Last, but not the least, I express my deepest appreciation to my parents, Mr. N. T. Thomas and Mrs. Lilly Thomas and sister Lincy Thomas to whom I owe not only my success but every step of my life. I thank them for the consistent backing and support.

May 31, 2016 *Linson Thomas*

NIT Rourkela Roll Number: 214EC2185

# Abstract

Continuous improvements in the VLSI domain have enabled the integration of billions of transistors on the same die operating at frequencies in the gigahertz range. These advancements have brought upon the era of system-on-chip (SoC). Traditionally, analog ICs has been prone to device noise while digital ICs have typically not been the prime concern being considered as relatively immune to noise. With faster transition times and denser integration, the scenario wherein digital ICs were considered to be immune to noise has changed significantly. Drastic changes in the physical design of an IC and increase in the operating frequencies has immensely changed the classical understanding of noise in the new age complex ICs. Switching noise specifically has become a dominating criteria for high performance digital and mixed signal ICs.
Voltage variations on the power/ground nodes of a circuit is a type of switching noise affecting digital and mixed-signal ICs.

Therefore, power integrity (PI) has become a critical challenge that must be addressed at the system level considering the parasitic effects of package and board. However, until recently, board designers have not considered PI from a system perspective. In contrast, various optimization techniques were focused separately on chip, package, and PCB design. Such a disjoint effort often resulted in circuits that even though meeting the design constraints before tape-out, they did not function correctly (or at all) once inserted on the PCB. PI and EMC have become critical objectives for first-silicon success. In fact, it is an interesting fact to note that even if all the traditional constraints related to area, timing, and power are met, but the chip does not satisfy the PI and EMC requirements, then the system will require some re-designing which results in a drastic increase in non-recurring costs as well as additional delays in the product chain, thereby missing critical time-to-market windows.

To cope up with the customer's ever increasing requirements and increasingly aggressive competition in the market, a proper understanding of the PI and EMC/EMI problem has become a must. Ironically, this is an era where though the clock frequencies are increasing and SI-PI problems are getting severe and severe, but the time to solve these problems and completing a proper working product is getting smaller and smaller. Inorder to handle the said challenges, so as to avoid costly design respins, what is required is

- the development of a PI/EMC-aware design methodology.
- a systematic methodology for efficient and reusable approach for a range of applications

An effective method to achieve PI and reduce electro-magnetic (EM) emissions considers the transient current profile generated on the power ground grid through accurate modeling approach of the system power delivery network (PDN) to estimate the PI and EMC behavior before implementation.
The simultaneous toggling of blocks within the logic blocks result in large current spikes on the power rails and ground rails. These power grids are localized in close proximity of the clock buffers and the current glitches may have a resulting effect on the clock signals being locally generated.

In this work, a die, package and board modeling and co-simulation methodology is presented which can be easily integrated into a standard VLSI design flow. This methodology involves breaking down the system in multiple components and generating models for each component to observe individual performance. System level response can be seen by combining them together. This approach has been successfully exploited to guarantee the power integrity on an industrial design. This approach becomes successful in providing a systematic and a widely reusable method to estimate integrity issues before fabrication, thus exhibiting its worthiness as a design step in avoiding failures and re-spins.

# Table of Contents

# List of Figures

# List of Table

# Chapter 1

# Introduction

## 1.1 Background

*"I would like to describe a field, in which little has been done, but in which an enormous amount can be done in principle. [...] Furthermore, a point that is most important is that it would have an enormous number of technical applications. What I want to talk about is the problem of manipulating and controlling things on a small scale. [...] For instance, wires should be 10 or 100 atoms in diameter, and the circuits should be a few thousand angstroms across. [...] There is nothing that I can see in the physical laws that says that the computer elements cannot be made enormously smaller than they are now. In fact, there may be certain advantages..."*

An excerpt from Richard P. Feynman's talk, "*There is Plenty of Room at the Bottom*," which apart from Moore's law, have been a source of enlightenment and inspiration for generations of engineers leading to the ever increasing growth of VLSI technology.

The journey of continuous advancements in the field of VLSI began with the discovery of a device called transistor (trans - resistor) at Bell Laboratories by John Bardeen, Walter Brattain, and William Shockley about a decade before Feynman gave this speech.

In 1959, Bob Noyce of Fairchild Semiconductor built the first monolithic IC using the planar process for manufacturing transistors [1].
From 1960 to now, microelectronic IC technology has progressed enormously with simultaneous advances in fabrication technology, devices, and design methodologies. Several billions of devices can now be integrated onto the same die, achieving 100,000 times more performance as compared to 1960 [2]. The primary design objectives driving this advancement have also evolved during this time frame. This evolution of the design objectives [3] is depicted in Figure 1.1

In the 1960's and 1970's, yield was the primary concern due to limited integration density, and consequently, area was the primary design objective [3]. A system contained a large number of interconnected ICs on a printed circuit board (PCB) where the system speed was primarily determined by the inter-chip communication. In the 1980's, the integration density significantly increased, and the speed bottleneck shifted from the inter-chip communication to the intra-chip communication. Circuit speed became an important design objective. In the meantime, a new class of handheld applications such as calculators and wrist watches emerged, making power consumption another primary parallel design objective [3]. During the 1990's, the design objectives could be categorized under three paths. Speed was the primary objective of the first path where additional power consumption could be tolerated for the sake of higher performance. The second path focused on consumer electronics where high speed was not required, and ultra-low power was the primary design objective. Finally, there were those applications where both speed and power had to be simultaneously considered. Speed and power became the primary design focus of this last design choice.

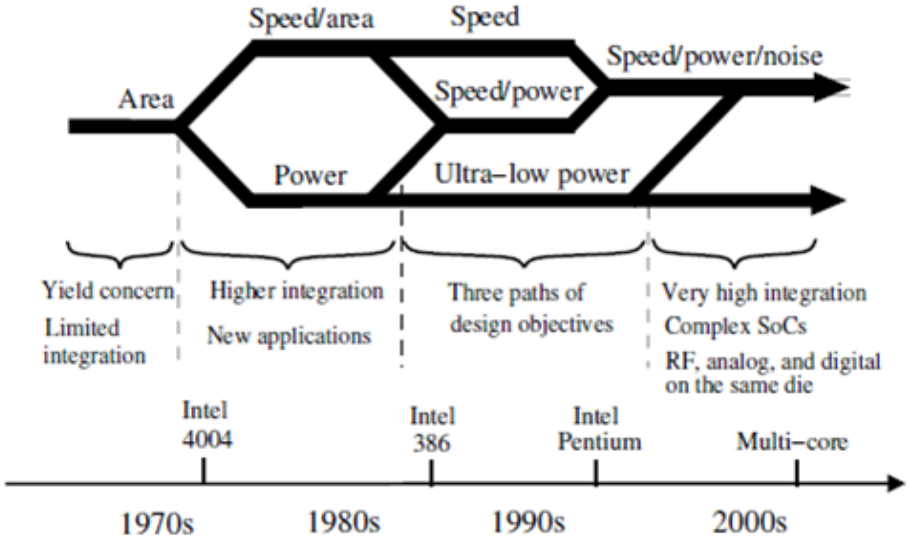


Figure 1.1 Design concern across decades

During the 2000's, the integration density has further increased, allowing complex system-on-chips (SoC) where analog, RF, and digital circuits are built on the same die. This highly dense integration of various functionalities, higher clock frequencies (faster signal transition times), and reduced power supply voltages caused another primary design objective, noise, to emerge.

Simultaneous optimization of speed, power, and noise has therefore become the primary focus in the IC design process. This co-optimization has enormously complicated the design process due to tradeoffs.

## 1.2 VLSI flow

A generalized ASIC design flow is pictorially represented in the figure above. Generally, the ASIC design flow is broadly classified into front-end processes and back-end processes. Above representation shows the verification stages too along with the fore mentioned processes.

The design stage starts with recognizing the specifications. All the technical aspects and details required are gathered extensively as this will have a huge impact on the future of the product. Once all the technicalities like architecture, interface etc. are decided, then a behavioral description is created to analyze the design in terms of functionality, performance and other specifications. RTL code is written in any hardware description language such as verilog or VHDL and the design is said to have made a front end design entry. At times, RTL code or netlist is automatically obtained from the schematic made from the specifications.

Once the RTL code is written, it is verified for functional correctness. Testbenches are generated or assertions are written to perform this functional verification. Along with this, power consumption as per the designed logic is predicted using test vectors representing the activity factors.

Next stage is the replacement of RTL description by actual gate descriptions. Using the RTL, technology library and help of first level floor planning, translation into gate level with speed, power and area optimization is carried out in the synthesis process.

Once synthesis is performed, there is an array of verification analysis (functional, timing and power) carried out. The synthesized gate level netlist is compared with the RTL for logic equivalence check along with the model checks. Gate level simulations are carried out formally and power analysis for the actual gate level representation for the logic is done. A very important step here is the timing analysis, commonly known as STA. Intrinsic gate delay information and route delay information are used for exhaustively evaluating all the timing paths. Set-up and hold violations, slack time are all reported and any changes in the synthesized circuit will be notified for improvement of timing. STA appears in the design flow after almost every step henceforth.

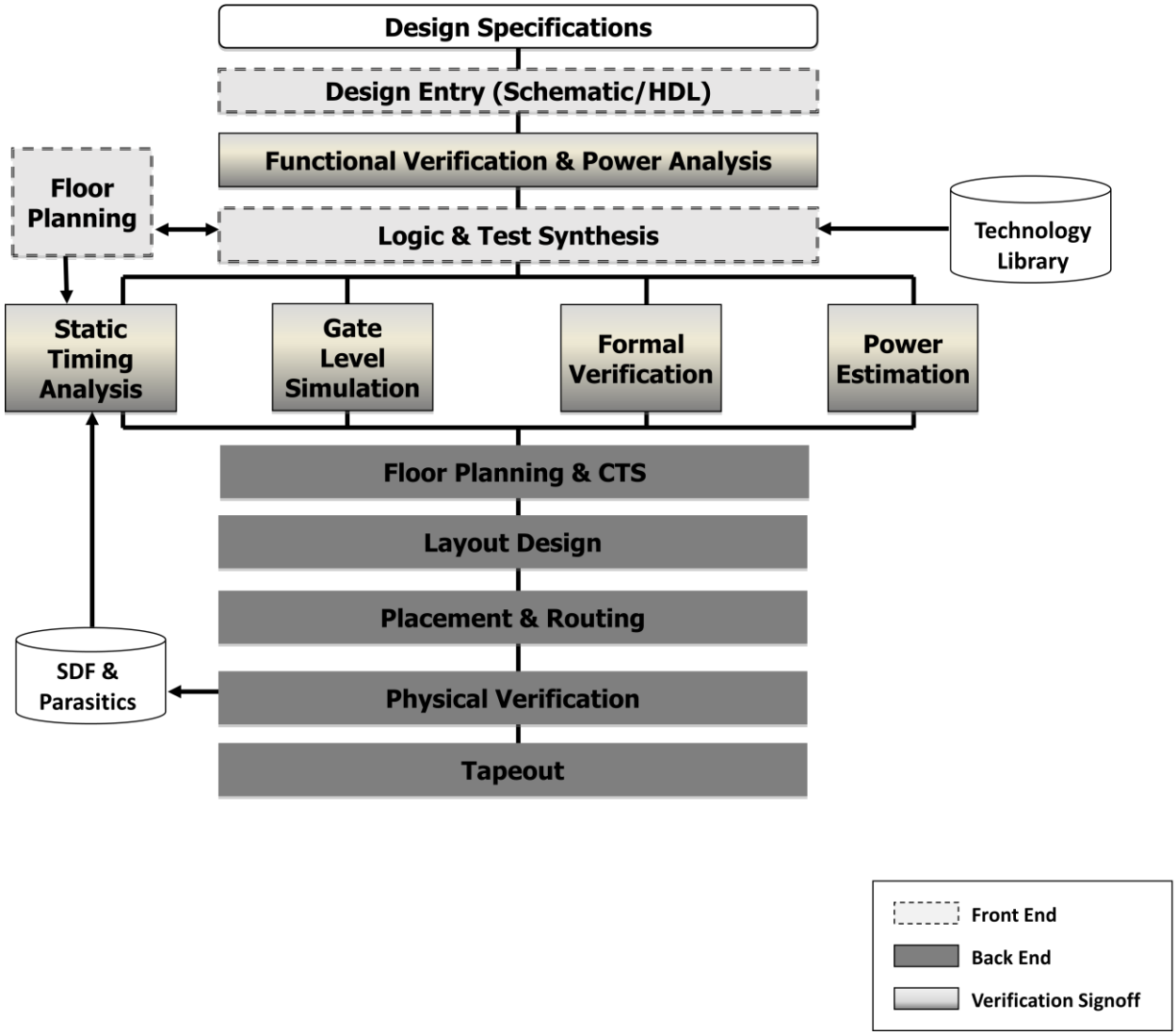


Figure 1.2 General VLSI design flow

After all the verification checks, the design enters the back-end. Floor-planning , placement and route consists of placing modules in the chip depending on various factors like interaction with other modules, noise immunity, path delay etc. Buffers are required in various paths of the synthesized clock tree to minimize skew. Routes are also done taking care of skew for clock circuits. Other specials nets like power and ground are also given special attention during routing.

Through these steps, the physical layout of the design is created. Once all the routes are done with then we can obtain a proper idea of the parasitic information in the design.

Parasitic extraction is performed on the physical layout and the information is obtained as a spef file.

Back annotation of the parasitic data is done on the pre layout design to check whether the design meets the timing requirements even after the inclusion of parasitic. Along with timing analysis, there are other factors too that are to be taken care of at this stage, collectively known as physical verification. Crosstalk, electromigration are some of the important aspects that are considered here.
Once all the stages are satisfactorily passed and there is a high probability of the design to be a success, then the design is sent to the fabrication lab for tape-out. The design chips thus obtained from the fab-lab are then rigorously tested and validated.

## 1.3 Where SI-PI comes in the flow

Signal and power integrity has never been a new phenomenon. However, in the good old days when the transition time was less and the clock frequencies were low, it did not have any significant effect on the system performance. With the advent of high-speed standards and interfaces, system designs are diving deep into the high speed regime. Under these conditions, where the interconnect properties are no more transparent to the signals [6], signal integrity (SI) analysis will have a huge role to play in guarantying a reliable functional operation of electronics products.

The flow chart as in figure 1.3 shows the SI and PI considerations that have now become an integral part of the design flow, considered at almost each stage of a high-speed design process flow. Based upon the stage where it is considered, SI guidelines can be classified as pre-layout SI guidelines and post-layout SI guidelines.

In the absence of proper pre-layout SI guidelines, prototypes may never leave the bench and without post-layout SI verifications, products may fail in the field [4].

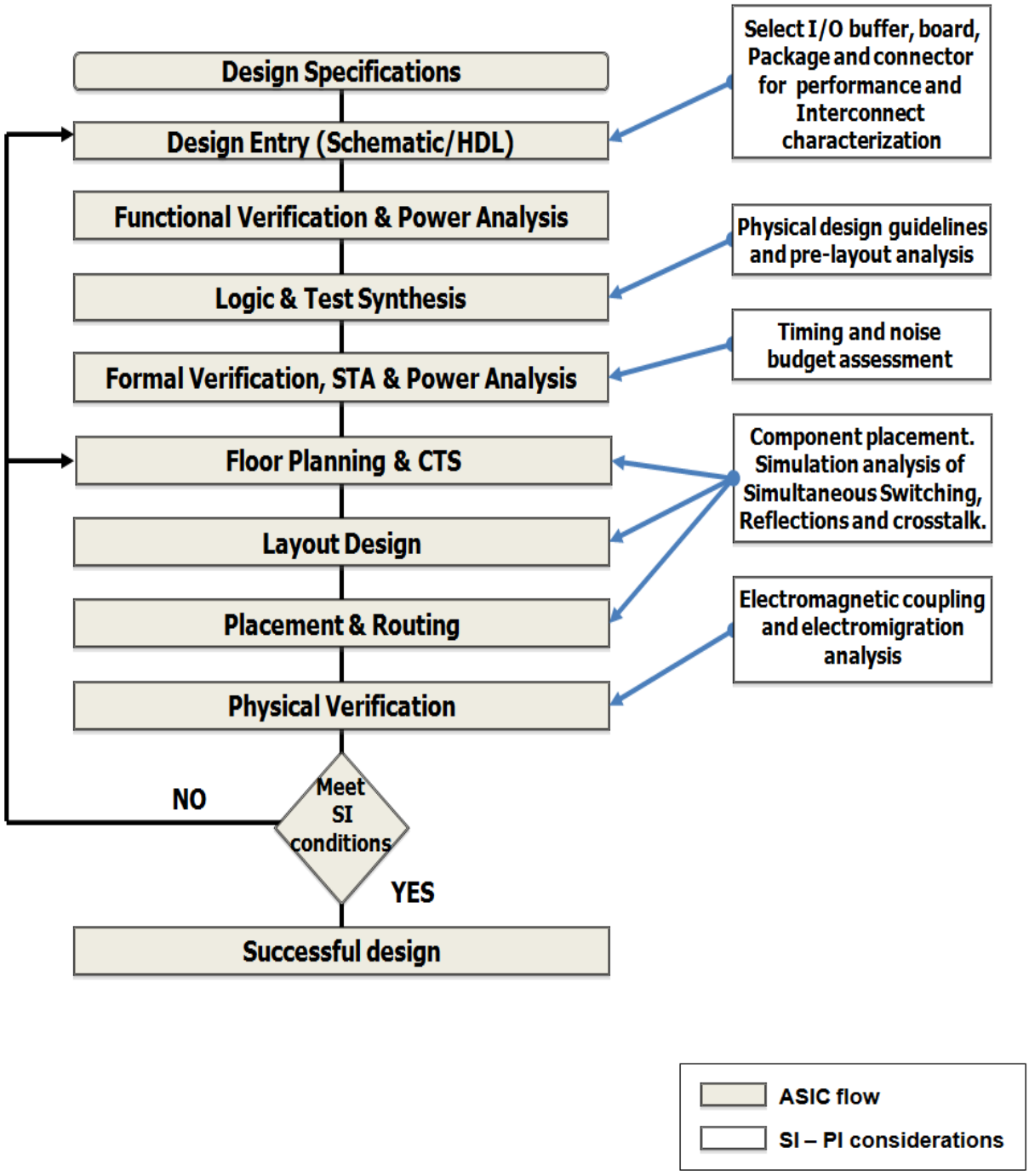


Figure 1.3 SI-PI considerations in a VLSI design flow

## 1.4 Importance of PI

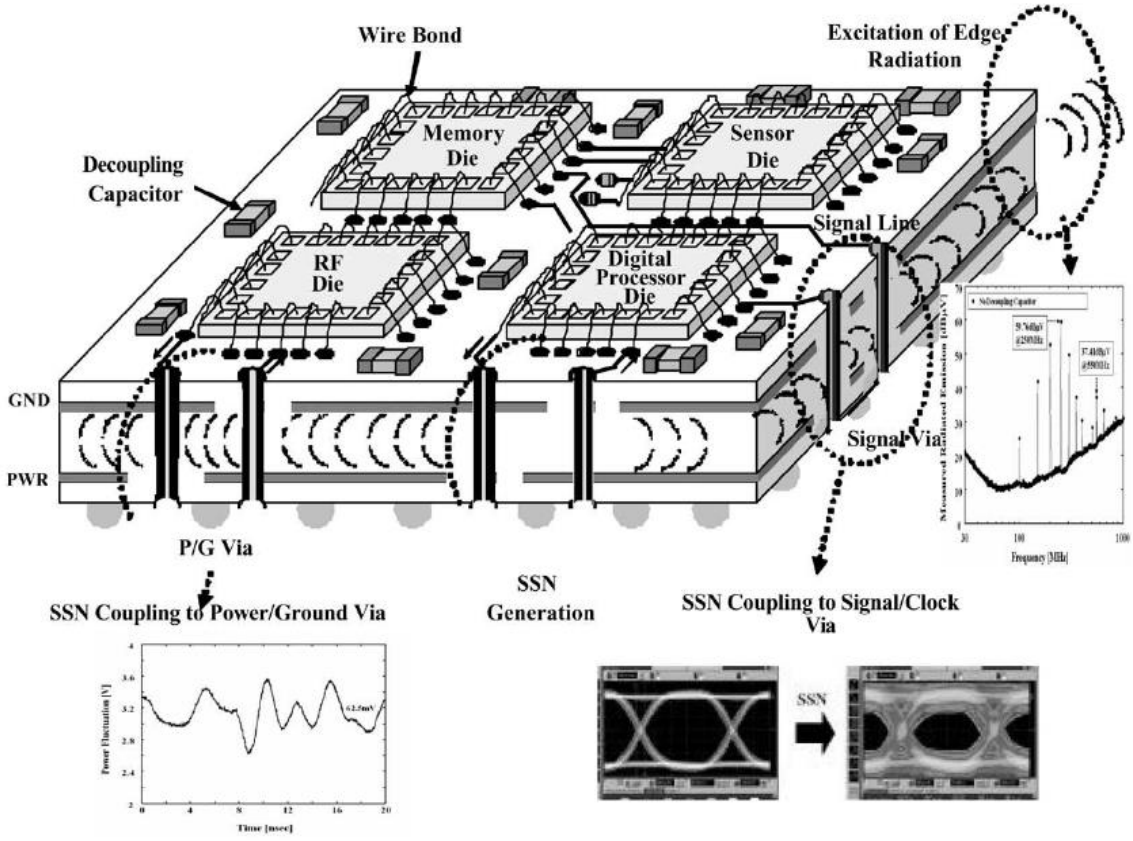


Figure 1.4 Noise coupling in a typical SoC [18]

As we know that the continuous progress in technology has changed the understanding related to noise immensely. Simultaneous switching noise (SSN) has specifically become a dominant aspect in digital blocks. Figure 1.4 shows a typical SoC and the possible coupling in the power and signal paths associated with it.

All these noise coupling in the power distribution network have the potential to become a major source of power integrity issues. Therefore, it becomes imperative to perform power integrity analysis and understand the system margins of the PDN so as to create successful and reliable designs

## 1.5 Literature Survey

Following the Moore's law, we know that the trend in VLSI technology is to increase the circuit densities every 18 months. Apart from the number of transistors being integrated, the design concerns have also seen a tremendous change in the past few decades. Therefore, along with high circuit density, we have designs with increased operating frequencies and lower operating voltages in-order to keep power low. Increased frequencies results in faster transitions or switching which further results in large glitches of currents. These high transients thereby cause large Ldi/dt drops in the power delivery network causing power supply fluctuations. With lower operating voltage, the noise margin gets decreased [10] [12] [13]. So, on one hand the variations are getting increased and on the other hand the noise margin is decreasing. This being a disastrous combination will lead to sure failures in any high performance low voltage design.
Inorder to keep up with the technology and the changing design parameters, immense growth in the understanding of new age complex designs to meet the timing, power and area budget is continuously being carried out. Novel ideas and methodologies to cope up with the failures are being inculcated in the design flow.

Early literature on power supply induced jitter consisted of considering various engineering solutions available in hand [15]. Once these solutions were implemented, the designs were rigorously tested. However, this methodology purely depended on trial and error and did not have any structured approach.

Further studies and advancements in this area led to 'power integrity' analysis to deal with the concerns due to the power supplied to the blocks within a design. Fairly recent literatures boast of a power integrity aware design methodology in the simulation stage of the design flow to help designers to efficiently evaluate the behavior of the die before tape-out. The methodology includes obtaining models for signal and power delivery network to make signal and power integrity simulations possible [14] [15].

With respect to PI analysis, recent literatures are focused on the modeling techniques. Power delivery network modeling starts with deciding the allowable noise in the power path and thus obtaining the target impedance, which when interacting with the current flowing through it will still be able to keep the functionality in control. Further modeling

methodologies involve obtaining behavior of power nets on PCB and package distribution planes, output drivers, power rails, solder bumps and hence on [14].

## 1.6 Outline of Thesis

The primary concepts required to have a firm understanding of this overall study are properly organized in Chapter 2. Herein, after explaining concepts of power integrity, the importance of jitter, especially clock jitter is mentioned. Methodology of obtaining the clock jitter due to power supply variations requires proper understanding of power delivery network. A detailed explanation of PDN and its elements are also covered in this chapter.

Once all the required concepts are explained, we go into the technical approach for dealing with clock jitter in chapter 3. The total clock paths are identified, preparing for jitter simulation

Modeling methodology of the power delivery network and simulation of individual components of the PDN is clearly shown in Chapter 4. Target impedance along with PCB and package planes, power/ground rail and chip power is evaluated in this chapter.

Obtaining the individual models was just the preparation of what the aim of this study requires. In Chapter 5, all the models are used together as a composite network, to analyze the total power supply variations. Obtaining this profile gives us the power to observe the jitter on the clock signal.

Jitter measurement results obtained from the approach mentioned in chapter 5 are all organized in chapter 6. Comparative analysis of optimized PDN is done with the default PDN to show the improvements in the jitter figures.

Finally in chapter 7 the inferences from the results are discussed and key points for better PDN design are noted down. The possible adaptation of this study is mentioned in the later section of this chapter.

# Chapter 2

# Basic Concepts

## 2.1 Signal and Power Integrity

### 2.1.1 Signal Integrity

Signal Integrity, as can be seen is made up of two words,

Signal, which refers to the electrical signal in this respective domain.
Integrity refers to fidelity or accuracy or lack of corruption.

Thus, Signal Integrity as a term stands for the accuracy with which the system deals with the signal in picture [4]. That is, by signal integrity we focus on the preservation of a signal's relevant information once it passes through a signal path [5]. In other words, Signal Integrity is a measure or an assessment of the quality of an electrical signal.
Dealing with signal integrity leads to encountering an avalanche of terms, describing the causes and manifestations of SI problems. Ringing, ground bounce, crosstalk, terminations, reflections, skin depth, gaps in planes, impedance discontinuities, rise-time degradation and much more are all terminologies related to signal integrity [4]. At first glance, the list of signal integrity effects seem like an endless random collection of terms, which makes it look a tiresome job to put them into perspective. A way to overcome this difficulty is to classify these innumerable terms into groups based upon a common relation. This makes it easier to isolate a problem, understand it efficiently and determine its cause. All the issues and concerns associated with signal integrity are related to one of the following four families of noise sources [4].

i. Signal quality of one net
ii. Crosstalk between two nets
iii. Rail collapse in power / ground grid
iv. Electromagnetic coupling

A thorough study of the origin of noise mentioned in above families will provide us with a generic solution to fix the SI-PI problems in the associated family.

*i. Signal quality of one net*

A net is made up of all the metal connected together in a system. The signal quality on a single net depends equally upon the physical features of the signal trace and the return path. The quality of a signal passing through a net depends upon the impedance the signal faces during its route to the other end of the net. If the impedance remains the same, the signal continues its journey undisturbed. On the other hand, if the impedance changes, reflection due to the change will be produced and a distorted signal is what remains. Any feature that changes the cross section or geometrical shape of the net, such as, a branch, trace width change, gap in return path plane will change the impedance the signal sees. Such a feature is technically known as an impedance discontinuity and every impedance discontinuity will add some extent of distortion in the signal that passes through it The way to minimize the problems associated with impedance changes is to keep the impedance the signal sees constant throughout the net.

*ii. Crosstalk between two nets*

Crosstalk simply can be related to the coupling between multiple signal nets. One net carrying a signal, can pass over some of its properties to an adjacent quiet net due to magnetic coupling between the two nets. Even though the signal quality on the first net (the active net) is perfect, some of the signal can couple over and appear as unwanted noise on the second, quiet net. In high speed devices, crosstalk is usually referred to as switching noise, ground bounce, dI-dt noise or simultaneous switching noise.

By understanding the nature of the capacitive and inductive coupling, it is possible to optimize the physical design of the adjacent signal traces to minimize the coupling. Spacing the traces farther apart, usage of lower dielectric constant material to decrease the cross talk for same characteristic impedance lines, keeping interconnects short are some of the steps that can be taken to minimize cross talk.

*iii. Rail collapse in power / ground grid*

Noise is a problem not for just the signal paths but it can also be a disaster in the power- and ground-distribution network which feeds power supply to each chip. When current through the power and ground path changes, as when a chip switches its outputs or core

gates switch, there will be a drop in the voltage across the power and ground rails. This voltage drop causes a decrease or collapse of the voltage between the power and ground rails which implies lesser voltage reaches the chip.

Larger the power delivery network impedance, larger is the voltage drop, and lesser the voltage gets sup[lied to the chip. Minimizing the impedance in the power delivery network is the remedy to deal with this problem.

*iv. Electromagnetic coupling*

With clock frequencies in the MHz range, the first few harmonics may fall within the common communication bands of FM radio, cell phone, and personal communications services. As a result of this, there is the possibility of such products interfering with these common communications unless their electromagnetic emissions are kept under acceptable levels.

It takes three things to have an EMI problem: a source of noise, a pathway to a radiator, and an antenna. Unfortunately, without special design considerations the radiated emissions level will inevitably increase with increasing clock frequencies.

Most of the voltage sources that drive radiated emissions come from the power and ground distribution networks. Often, the same physical designs that contribute to low rail-collapse noise will also contribute to lower emissions. Shielding is also used to minimize the leakage of noise to any antenna.

As mentioned previously, signal integrity depicts the preservation of relevant signal properties after passing through a signal path. It would be worthwhile to discuss about ‘relevant signal properties’ and ‘signal path’, as these terms form the cornerstone of understanding the above mentioned definition [5].

Relevant signal properties

- *voltage swing*

The voltage swing is the maximum peak to peak value of any signal. Voltage swing must be sufficiently high with respect to the ringing for proper discrimination between high and low levels.

- *ringing (overshoot/undershoot) and settling time*

Ringing is the fluctuating / unsettled part of the signal caused primarily due to mismatching or impedance discontinuities. A signal should be able to settle to its value in as less time as possible.

- *edge transition time*

The edge transition time is basically the time required for the signal to go from one level to another i.e., the rise and fall time. The transition time should be short enough to allow the signal to settle to their appropriate levels within the unit interval.

- *bit duration/data rate*

Data rate defines the number of data bits that can be transmitted in a second. The bit duration should be high enough to let the signal settle well before and be able to represent its proper data for enough duration.

- *jitter*

Jitter that is nothing but the short term deviation of signal edges from its nominal edge, becomes a critical factor for clock data recovery at the receiver end.

Signal path

In high speed applications, considering signal paths as uniform transmission lines having properties (characteristic impedances, propagation coefficient etc.) constant over their length is not practical. Signal paths typically consist of piecewise homogenous transmission lines, including PCB traces or cables and lumped elements like connectors or vias [5].

Signal paths such as these cause significant modifications of signal properties. As explained in the family classification of SI problems, signal paths could have discontinuities leading to reflections. Larger mutual inductive coupling could lead to crosstalk, modifying the characteristics of any signal while travelling through such a path

### 2.1.2 Power Integrity

As we entered the high speed regime, the effect of interconnects, which were earlier insignificant, started to become critical. Signal speeds have become high enough that the interconnect properties are no longer transparent to the signal being transmitter and therefore has become a contributing factor in a circuit's performance, leading to signal integrity problems. These added problems made the concept of 'pure digital' a trivial matter and from then on digital buses too had to analyzed with respect to their analog characteristics [6].

In the near past, the power supplied to the logic blocks have become a greater concern, resulting in "power integrity" analysis.

Modern packages make use of ball-grid arrays (BGAs) consisting of hundreds of power and ground pins with dedicated pins of different voltages ranging down to less than 1 V [20]. The total activity governed by the logic may result into sinking tens of amps of current. Such activity supported by large number of transitions may hamper the supply to the ICs. Providing "clean" power to these ICs is what is to be achieved through power integrity analysis. This has necessitated a proper understanding of how a signal propagates through the power delivery network, which includes many components like regulators, capacitors, vias, power/ground planes and so on [17] [18].

The first stage of power integrity analysis is to find the impedance of the power distribution network (PDN). To achieve good power integrity, we want the power supply network to offer as low impedance as possible. At DC, as low a resistance as possible is desired to keep the DC IR drops low and at AC, minimizing the impedance between power and ground at different locations throughout the frequency range is the key [18].

## 2.2 Jitter

As it has been said throughout this article, entering into the high speed regime has resulted into a humungous change in the way we deal with integrated circuit designs. Transmitting of data is not simply transferring 1s and 0s anymore. Designers have to more careful about the true nature of binary information carrying circuit, realizing that it is actually analog in nature.

One of the major issues that have sprung up due to faster transition rates is jitter. This section will deal with the fundamentals of jitter and its significance on a system's BER. Furthermore, jitter measurements will be discussed, which is more necessary as just knowing the concepts isn't enough if measurement aspects are not clear.

Jitter can be defined as "the deviation of the significant instances of a signal from their ideal location in time" [8]. In a digital signal the significant instances are the transition points. Simply, jitter is how early or late the signal transition occurs with reference to its nominal transition edge.

Before talking about anything, let's start with the types of jitter and their sources in the real world

### 2.2.1 Broad classification of sources of jitter

Depending on its causes, jitter on a signal has different behavior or characteristics. So, categorizing jitter on the basis of its sources would help us in dealing with it efficiently. The primary interactions [7] behind the reason for jitter are listed below:

*i. Random noise phenomena*

Random phenomena are those which randomly introduce noise in a system.
These sources include:

- Thermal noise — associated with the flow of electrons in conductors.
- Shot noise —fluctuations in current originating from the discrete nature of electric charge
- Pink noise — noise that is spectrally related to $1/f$

*ii. Data-dependent phenomena*

Data dependent sources of jitter are those that affect the signal being identified at the receiver side.
Examples of DDJ sources include:

- Inter-symbol interference
- Duty-cycle distortion

*iii. System phenomena*

System related jitter effects on a signal are because of the environment in which the digital signal is being carried.

Examples of such sources of jitter are:

- Crosstalk between signals
- Path discontinuities
- Impedance mismatch

The above mentioned phenomena are like the bank of jitter sources. Whatever be the type of jitter in the system will be because of one of the fore mentioned causes.

## 2.2.2 Jitter Family

Let us now get into the detailed explanation of the jitter family and the individual cause for the particular jitter.

Total jitter comprises of random jitter and deterministic jitter [8] as shown in figure 2.1.

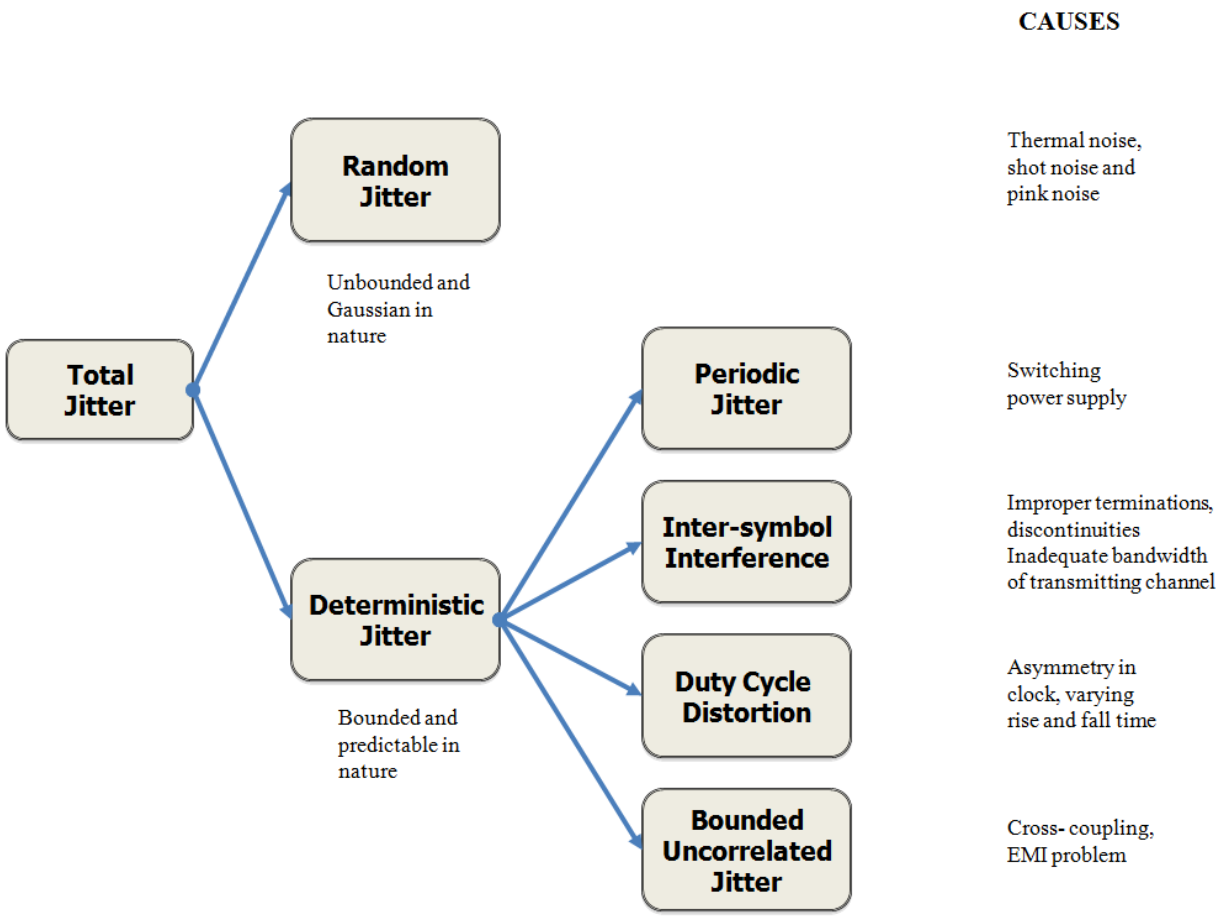


Figure 2.1 Jitter family tree

2.2.2a Random Jitter

Random jitter (RJ) results from the random noise phenomena explained in section 2.2.1. Random jitter is said to unbounded; unbounded as in it does not attain any maximum or minimum value of phase deviation within a given time interval. It is because that random jitter has unlimited (approaching to infinity) peak-to-peak, it is measured in terms of RMS value.

2.2.2b Deterministic Jitter

Deterministic jitter (DJ) is the result of system phenomena and data- dependent phenomena mentioned in section 2.2.1 DJ is bounded and is therefore measured as peak-to-peak value always. It is said to be bounded because DJ attains a maximum and minimum value of phase deviation within some specified time interval.

Deterministic Jitter further consists of sub-components Periodic Jitter, Duty Cycle Distortion (DCD), Inter-Symbol Interference (ISI), and Bounded Uncorrelated Jitter (BUJ) as shown in Figure 2.1.

Let us now take a look at each of the sub-components of deterministic jitter.

*i. Periodic Jitter*

Signals from a switching power supply coupling into the data or system clock signals would be a common example of PJ. PJ is said to be uncorrelated if the signal is based upon a different clock source, as it is uncorrelated with the clock or data signal. Also, if coupling is from an adjacent data signal based on the same clock or the same frequency clock then the PJ turns out to be correlated

PJ usually results in amplitude distortions on the data signal and if the amplitude distortions occur near or at the data signal transition, timing errors may occur.

*ii. Duty Cycle Distortion*

The prime causes of DCD jitter are threshold level offsets and rise and fall time asymmetry. An increase in threshold level results in an output signal with duty cycle less than 50% and if the threshold level is decreased, then a duty cycle greater than 50% is observed at the output signal. A second source of DCD is asymmetry in rise and fall time. A slower fall time compared to the rise time results in a duty cycle of more than 50% for a

repeating 1010... pattern, and slower rise time relative to the fall time results in a duty cycle of less than 50%.

*iii. Inter-Symbol Interference*

Bandwidth limitation problem in the channel is the man reason for ISI. A bandlimited channel passes only a certain frequency ranges, resulting in no response if the signal is below or above the frequency range that the receiver allows, rendering the signal incomplete. In addition, the receiver collects the pulse's shape differently, altering it in a way that the shape of the first symbol period has some interference with the subsequent symbols.

*iv. Bounded Uncorrelated Jitter*

Crosstalk is said to be prime cause for BUJ. Most of the literature terms BUJ as an immeasurable aspect of jitter. As the name says, BUJ is bounded but uncorrelated to the data sequence.

### 2.2.3 Jitter Measurement

Knowing the components of jitter and their causes is essential, but what is more important is to be able to measure jitter in a defined manner. Jitter measurements are classified into the following major categories 9[]

- Period Jitter
- Cycle to Cycle Period Jitter
- Long Term Jitter

Period jitter (PJ) is the difference between the period of a clock signal and period of an ideal clock signal over a number of randomly selected cycles. If a clock sequence is provided, the individual clock periods can be measured making it possible to obtain the average clock period, standard deviation and peak-to-peak value. The standard deviation is referred to as the RMS value of period jitter and the peak-to-peak value as the name suggests gives the peak to peak period jitter.

Cycle to cycle (C2C) jitter is the difference between the cycle duration adjacent cycles of a signal, over a random sample of adjacent cycle pairs, preferably keeping the sample size

greater than or equal to 1,000. The difference in cycle to cycle jitter is that it measures the difference in period between 2 consecutive cycles and does not involve any ideal clock

Long-term jitter measures the change in a clock's output from its nominal position, over several consecutive cycles. The difference in long-term jitter from period jitter and cycle-to-cycle jitter is that it represents the cumulative effect of jitter on a continuous stream of clock cycles over a long time interval, therefore also known as accumulated jitter.

## 2.3 Importance of Clock Jitter

Noise or other disturbances like power supply variations, loading conditions and interference coupled from nearby circuits in a system are the typical sources of jitter in clock signals

Clock being the most important signal in any system, discrepancies in the clock signal could lead to bit errors at the receiver end. To describe the significance of clock signal, let us have a look at the violations that could occur in a design due to excessive clock jitter.

The jittered clock could have its rising edge before the data is valid or it could be such that the effective hold time gets reduced, both leading to incorrect data being processed. Figures 2.2 and 2.3 shows setup and hold violations that could lead to data transaction failures of any design.

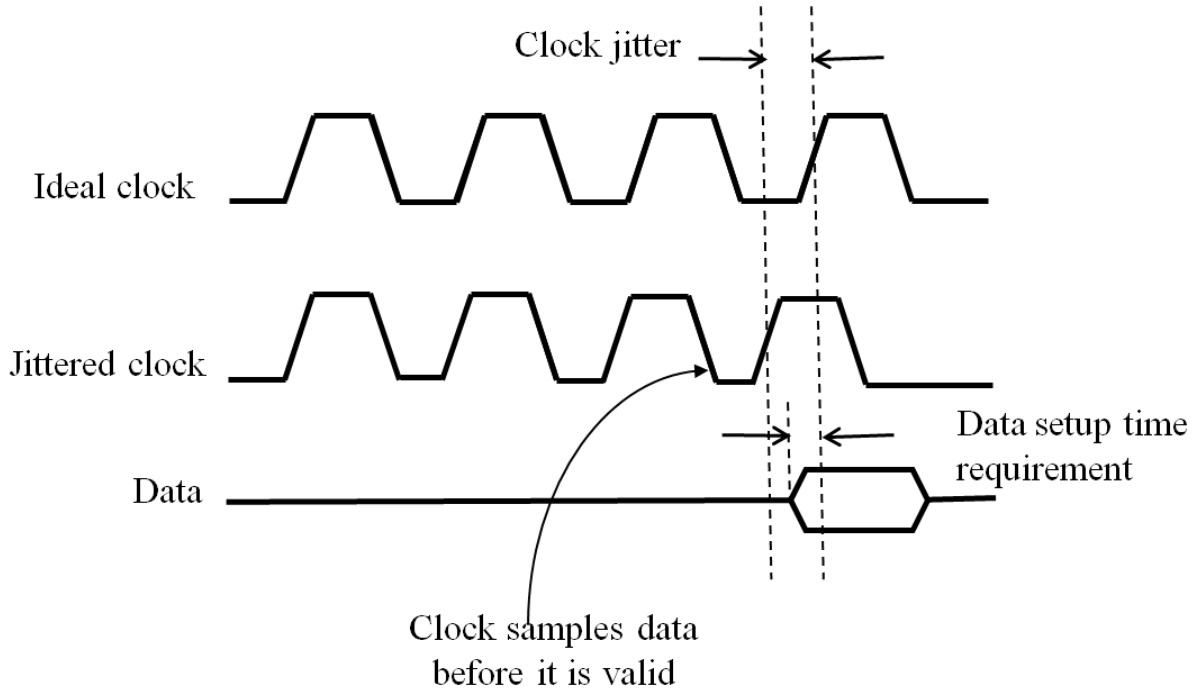


Figure 2.2 Setup violation due to clock jitter

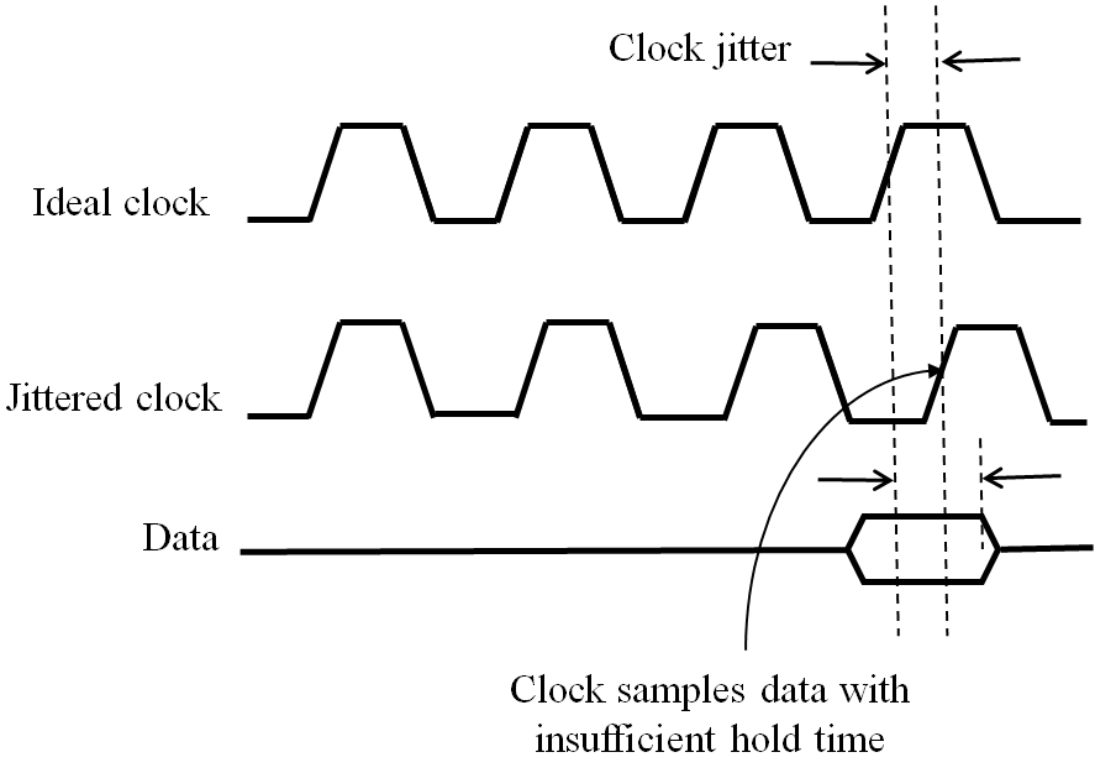


Figure 2.3 Hold violation due to clock jitter

## 2.4 Power Delivery Network

### 2.4.1 Elements of Power Delivery Network

Even before power integrity considerations were taken seriously, designing the power delivery network (PDN) for any system has been a critical task. With the growing age, this task is now becoming highly challenging. With technology scaling the trend is to lower the power supply voltage and increase in clock rates. These trends results into various consequences making the design of a PDN even more challenging.

Before jumping into the designing of a PDN, lets understand the proper definition and the various entities of a PDN.

A power delivery network is the network that provides clean power to the functional blocks of a system. The goal of the power delivery network (PDN) is to be able to sustain the load under all conditions without compromising on the voltage integrity [18]. When a functional unit turns on to perform a task, there is a transient current demand at this point which could be multiple times that of the nominal current. This places an enormous load

on the PDN. And the transient voltage noise on the PDN needs to be validated under these circumstances.

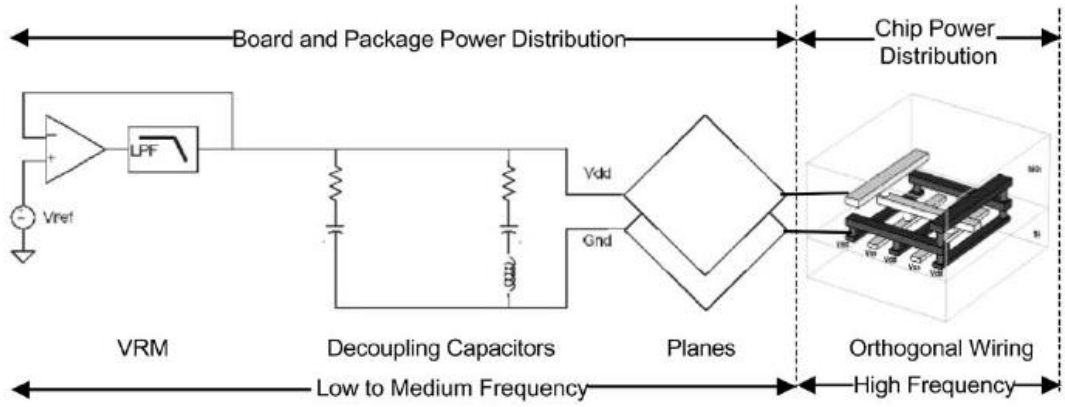


Figure 2.4 components of a power delivery network

PDN consists of multiple elements across the voltage regulator module, the board planes for power distribution, the package planes for power distribution and the chip level power distribution; along with decoupling capacitors at each level as shown in Figure 2.4.

The modeling architecture and challenges for the fore-mentioned blocks in the PDN are explained below.

*i. Voltage Regulator Module*

A voltage regulator module (VRM) is basically a converter that provides appropriate power supply to different sections in a PCB and package. As the VRM is capable of converting any voltage to what is required by the processing unit, multiple sections with different supply voltages can be mounted on the same chip.

A VRM model for simulation purpose can be obtained as a SPICE netlist from the manufacturer of the VRM. If not available, the VRM can simply be modeled as a voltage source with its internal series resistance and its pin inductance [18] [23], as shown in figure 2.5.

As per the behavior of a R-L circuit, at low frequencies, the VRM has low impedance which makes it capable of responding to the transient current requirements. As the frequency increases, the VRM impedance becomes more and more inductive and the consequent increase in the VRM impedance makes it incapable of meeting the instantaneous current requirement [4].

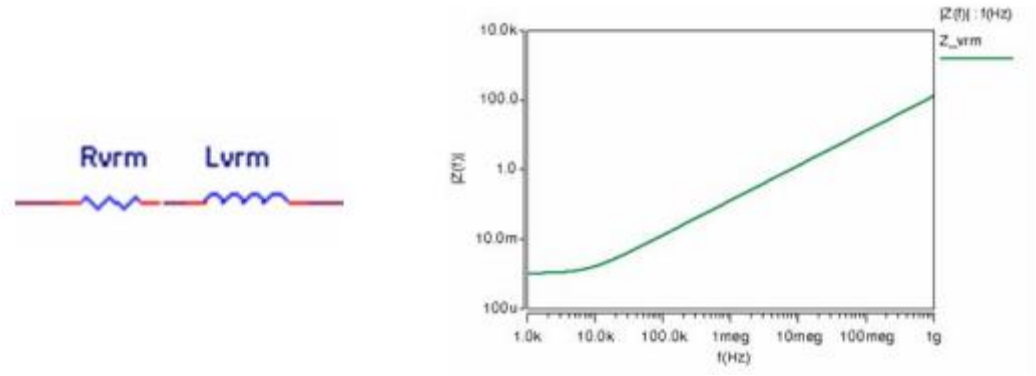


Figure 2.5 VRM schematic and frequency response

*ii. Decoupling Capacitors*

Decoupling capacitors, commonly known as de-caps, are used as an aid to the slow and lethargy VRMs. All the de-caps (VRM, PCB, PKG) have a significant role in the PDN network.

The effect of the individual family of de-caps [18] are shown in figure 2.6.

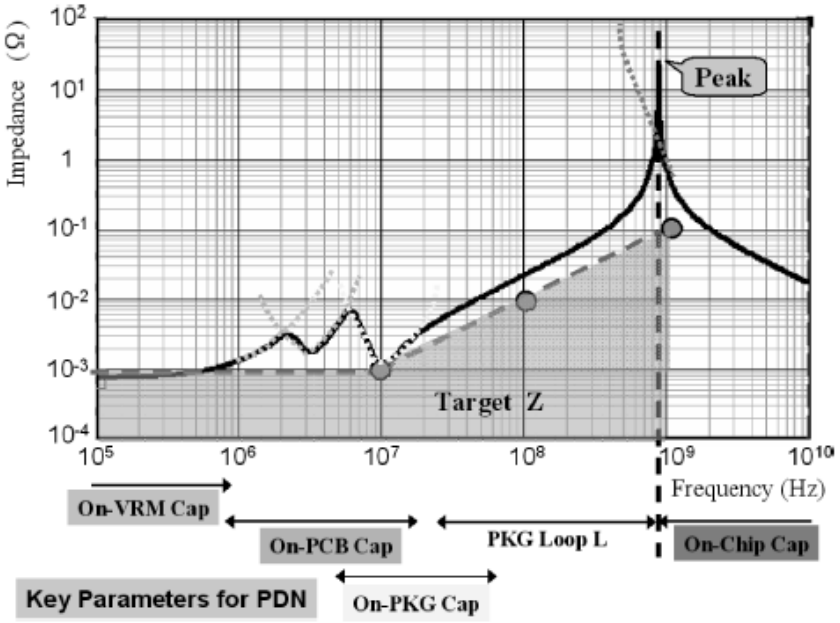


Figure 2.6 impedance profile of PDN with contribution of different L and C [18]

At low frequencies, the equivalent series resistance (ESR) associated with bulk capacitor of the VRM becomes influential in smoothing the output power supply voltage. At middle frequencies, the ground bounce is taken care by keeping the equivalent series inductance (ESL) of that capacitor low. At high frequencies, the on-chip capacitors become effective.

PCB de-caps are used to deal with the plane anti-resonant peaks. Therefore appropriate selection of the capacitors is essential to keep the PDN impedance under check.

Any capacitor mounting has an additional loop inductance associated with it [16]. Loop inductance depends upon the trace width and length that connects the vias, the via length that connects the capacitor to the appropriate power plane, the diameter of the vias and so forth. Therefore, this loop inductance value becomes design dependent and is a prime concern while designing a PCB. Inorder to reduce this loop inductance, while designing the PCB, place the vias in close proximity to the capacitor, to reduce the trace length between the via connecting the capacitor to the power/ground plane. Multiple power/ground via pairs should be preferably used to reduce the resistance provided to the current flow. To keep crosstalk at minimum, place the vias such that the vias with opposite current flowing through it are placed close together which will negate the magnetic lines produced by the currents thus reducing coupling. Also, same polarity vias should be placed away from one another, so that the coupling between them be as low as possible.

### *iii. Package and Board Planes*

Using planar layers in the PCB/ PKG stackup are an effective method for power distribution [23]. However, the power/ground planes behave as electromagnetic resonant structures and become a significant source of noise when excited at the resonance frequency [18].

The parameters that decide resonance frequency [16] include

- the effective series inductance (ESL) of the decoupling capacitors and vias.
- the number of the power/ground bonding pads

Models for board and package planes are obtained by extracting s-parameters from the brd files.

### *iv. Chip Power Distribution*

Continuous scaling of CMOS process technology has made it challenging to design the on-chip power delivery networks in high performance SoCs. Chip power distribution models the operation of the chip in a manner that causes additional stress particularly.

On-chip power delivery networks should provide a low impedance path over a wide frequency range.

On-chip decoupling capacitance, as mentioned earlier supports the VRM when it is unable to respond to the fast changing current requirements. To aid the VRM, the de-cap is used as a local power source, which can efficiently lower the PDN impedance [4]. The addition of decoupling capacitances effectively decouples the large switching currents from the inductance in the power delivery network, thereby reducing the switching noise [21] [22].

The inductance and the decoupling capacitance associated with the package and chip forms a parallel *RLC* circuit which will again form a resonant structure. At this resonant frequency, the functional blocks on the chip will face a high impedance. Looking at this trend, it will be imperative in the future generation chips to include large amounts of de-caps on the chip to control the switching noise and maintain the chip-package resonant frequency well below the operating frequency [17].

### 2.4.2 Power Delivery Network Design

Every time the VLSI technology is scaled, the resultant effect is a drastic increase in circuit densities, lower operating voltages and faster device switching speeds. These trends in turn lead to designs with increased current and transition rates; and reduced noise margins. The increased currents along with the large interconnect resistance results into significantly high IR drops; on the other hand the faster transition rates cause large inductive LdI/dt voltage drops in the power delivery networks. Along with the above mentioned consequences, Electro-migration (EM) is another critical interconnect failure reason in integrated circuits [18]. These effects brought about by the improvement in technology, in turn, create challenges from a power delivery standpoint as increasingly stringent noise requirements have to be met for proper device operation.

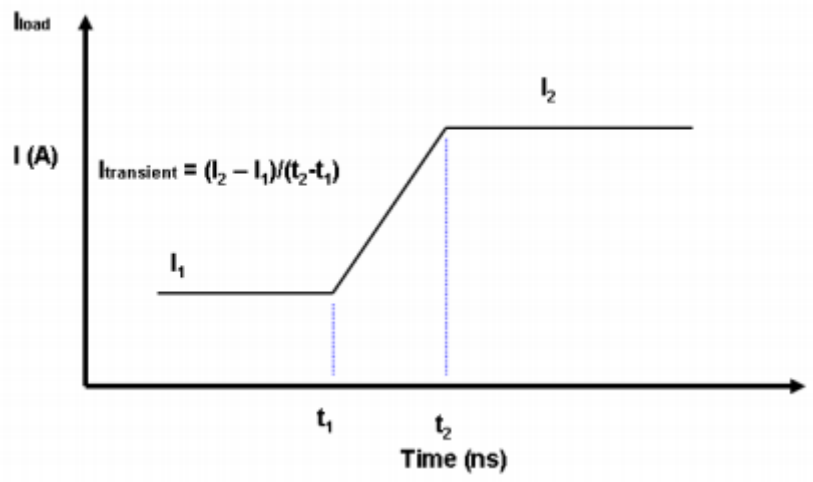


Figure 2.7 transient current definition

A power delivery network will provide a signal an impedance ($Z_{PDN}$) associated with the path the signal follows as it travels from the voltage regulator module (VRM) to the die. The noise magnitude, i.e. the voltage ripple that is observed on any given power/ground rail is directly related to this impedance (ZPDN) and the transient current (ITRANSIENT) drawn by that rail

Based on Ohms law: VRIPPLE = ITRANSIENT * ZPDN

The transient current produced in any system is application-specific, based upon the switching signal pattern. Therefore, without special knowledge of the behavior of the chips in each application, there cannot be a proper estimation of this parameter. What we can say is that the transient current would depend on the core logic. In other words, while designing the PDN, there is no control over the transient currents that would appear. However, the ZPDN is under our control and ZPDN can be optimized through good board design practices [16]. To maintain the voltage ripple noise within the constrained limits,. ZTARGET is used as the guideline, wherein the PDN impedance should always be lower than the target impedance.

So, let's now delve into the concepts of Target impedance and its significance while board designing.

### 2.4.3 Target Impedance

The first step in designing the PDN is to establish the target impedance.

As fluctuating currents with some spectrum, I(f), pass through the complex impedance of the PDN, there will be a voltage drop in the PDN:

$$V(f) = I(f) \times Z(f)$$

Where:

V(f) = the voltage amplitude as a function of frequency

I(f) = the current spectrum drawn by the chip

Z(f) = the impedance profile of the PDN as seen by the chip pads.

This voltage drop in the PDN means that the constant voltage of the regulator is not seen by the chip, but is changed. In order to keep the voltage drop on the chip pads less than the

voltage noise tolerance, usually referred to as the ripple, given the chip current fluctuations, the impedance of the PDN needs to be below some maximum allowable value [4]. This is referred to as the target impedance

$$\boldsymbol{V_{ripple} > V_{PDN} = I(f) \text{ x } Z_{PDN}(f)}$$

Where:

Vripple = the voltage noise tolerance for the chip, in Volts

VPDN = the voltage noise drop across the PDN interconnects, in Volts

I(f) = the current spectrum drawn by the chip, in Amps

ZPDN(f) = the impedance profile of the PDN as seen by the chip pads, in Ohms

The maximum impedance for the PDN, the target impedance, is established based on the highest impedance that will create a voltage drop still below the acceptable ripple spec. This is given by

$$\boldsymbol{Z_{PDN} \text{ x } I_{transient} = V_{noise} < V_{DD} \text{ x } ripple} \%$$

$$\boldsymbol{Z_{target}(f) < \frac{V_{ripple}}{I(f)}}$$

or

$$\boldsymbol{Z_{target}(f) < \frac{V_{DD} \text{ x } ripple \%}{I(f)}}$$

where:

$V_{DD}$ = the supply voltage for a specific rail

$I_{transient}$ = is the worst case transient current

$Z_{PDN}$ = the impedance of the PDN at some frequency

$Z_{target}$ = the target impedance, the maximum allowable impedance of the PDN

$V_{noise}$ = the worst case noise on the PDN

ripple% = the ripple allowed, assumed to be +/– 5% in this example

Minimizing the impedance associated with the complete path between the VRM and die, such that it meets the target impedance $Z_{TARGET}$ results in an efficient PDN design. However, designing a power delivery network over a wide band of frequency can be a tricky task under some scenarios. If $Z_{PDN}$is kept way too below the target impedance in the frequency range below the target impedance, it implies that the PDN was overdesigned and costs more than what is optimally required. But with such a PDN design one can be sure that the worst case voltage noise generated across it will seldom lead to failures. Hence, from a design standpoint, trade-offs have to be made to achieve a reasonable balance between cost and performance.

## 2.5 S-Parameter

At low frequencies simple voltage and current analysis can help us in analyzing and characterizing the system efficiently. But at high frequencies, where usage of general two port parameters becomes infeasible, S parameters play a dominant role.

Generation and use of S parameters is quite simple. Moreover for further analysis on parasitic like inductance and capacitance etc or any irregularities and discontinuities in the PCB S parameters can be easily converted to other parameters.

At sufficiently high frequency it is easy to measure signal properties in terms of transmission and reflection parameters rather than voltage, current, impedance and admittance etc. S parameters help us in treating the system as a black box and measuring its performance under any source or load conditions. We do not require an open or short test to generate these parameters as for Y, Z or H parameters. It is easier to measure the performance in terms of gain, loss and reflection coefficients and import the S parameter file in our advance SI simulation tools. S parameters can be easily cascaded and therefore we can fully characterize an interconnect path comprising of connector, cable and PCB traces.

S parameters can be defined for single port or multiple port system and are suitable for single ended as well as differential signal analysis

To have a quick glance at the S parameters let us consider PCB interconnect as two port network as shown in figure 2.8. Any PCB trace acts as a transmission line and may be single or differential in nature. Accordingly S parameters required for the traces could be single or differential in nature.

S parameters are defined as reflection and transmission coefficients. For a simple two port network as shown below in figure below the S parameters are defined as

$$B1 = S_{11}A1 + S_{12}A2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ 1$$
$$B2 = S_{21}A1 + S_{22}A2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ 2$$

The signal A1 which is incident on the PCB interconnect at port 1 is called the incident signal. Part of this signal is reflected as B1, and part of it is transmitted as B2 out of port 2.. Similarly for signal A2 incident on port 2, B2 is the reflected signal and B1 is the transmitted signal.

Assuming the wave travelling from port 1 to port2 to be in forward direction, port 1 is assumed as input and port 2 as output, we can define the S parameters S11, S12, S21 and S22.


Figure 2.8 interconnect as a 2 port network

The input reflection coefficient S11 is the signal reflecting from port 1 because of the signal incident on port 1. The signal coming out of port 2 as a result of the incident signal at port 1 defines S21, the forward transmission coefficient. Similarly S22 is the reverse reflection coefficient and S12 is the reverse transmission coefficient.

In the same manner, for differential signal PCB interconnects the S parameters can be defined as mixed mode S parameters. The differential channel or interconnect never remain purely differential due to asymmetry in length or width of traces or local dielectric constant hence the mixed mode S parameters come into picture. A brief insight of the generalized mixed mode S parameters for a coupled interconnect are defined as below:

In figure 2.9, $S_{CC}$ is the common s-parameters, $S_{DD}$ the differential s – parameters and $S_{DC}$ and $S_{CD}$ the mode – conversion or cross – mode s – parameters. In particular, $S_{CD}$ describes the conversion of differential mode signals into common-mode signals and $S_{DC}$ describes the conversion of common signals into differential signals.

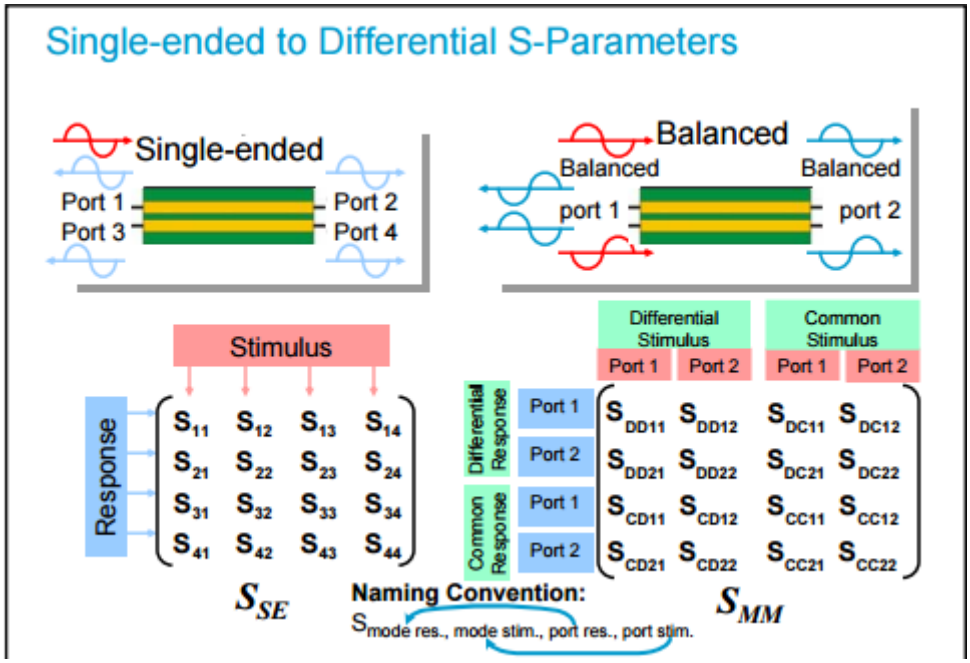


Figure 2.9 relationship between single-ended and differential s-parameter

For further analysis on capacitance and inductance S parameters are converted to Z or Y parameters. For analyzing the inductance offered by a trace if we convert S to Z then divide the imaginary part of Z by $2\pi f$ we get the inductance. For analyzing the capacitance similar process can be adopted by converting S to Z parameters. Sometimes during high speed analysis of PCBs or packages we want that the high impedance offered by the network should not fall in the desired frequency range. Every time we make modifications in the PCB or package design it might be difficult to directly generate Z or Y parameters at high frequencies. Therefore generating S parameters and then converting to other parameters and analyzing the board helps in quick analysis and correction of the design.

# Chapter 3

# Technical Approach

## 3.1 Objective

The functionality of any system is very sensitive to the clock signal. Literatures have shown that the major cause of designs failing in the high speed regime is power supply induced jitter on clock signals. Having understood the importance of clock and the disastrous effect of discrepancies in clock, it is necessary to be able to predict the accurate level of jitter on the clock signal as early as possible

The next sections in this chapter provide an idea of the approach taken to obtain clock jitter and predict the performance of a design well before fabrication, giving a higher probability in achieving the dream of any VLSI engineer, 'first silicon success'

## 3.2 Identifying Clock Paths

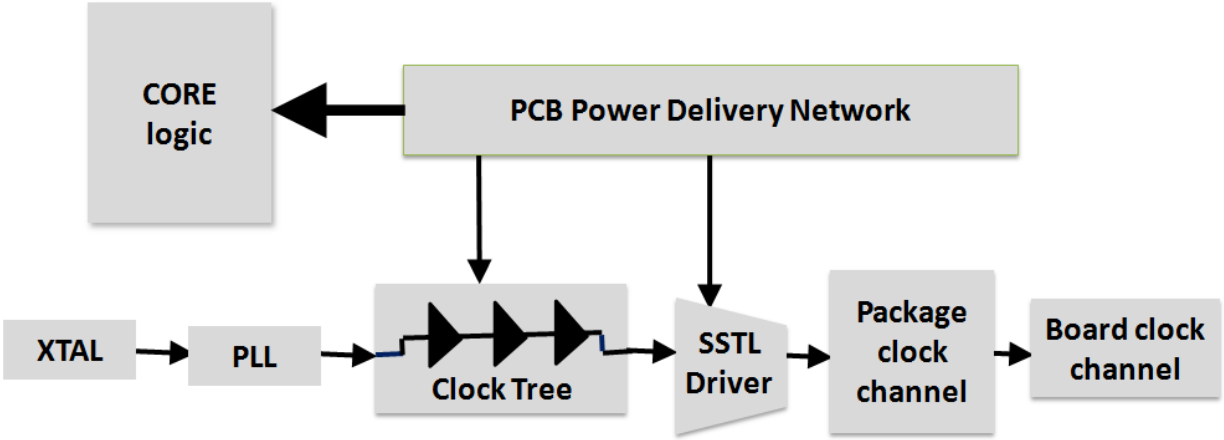


Figure 3.1 Clock paths within the system under consideration

Many diversified sources in a system exists which can cause jitter in the clock signal. Typically noise in power supply of a buffer is one of the main factors causing jitter in output of a buffer. There can be jitter introduced due to PLL architecture and clock tree.

Then characteristics of channel carrying signal also impact it significantly and can add jitter. Looking at the architecture and different components present in system under investigation, simplified block diagram with the blocks affecting clock is drawn in Figure 3.1 and possible suspects which could adversely affect the clock jitter [13] are identified as listed below:

- Quality of channel used for transmission of differential clock in package and board i.e. trace length mismatch and impedance variations in clock traces, which could result in clock skew.

- Violation of target impedance specifications for power delivery network over the frequency band of operation, which is a major reason for generation of power supply ripple at inputs of different blocks.

- Characteristics of SSTL drivers with ideal supply i.e. inherent jitter added due to buffer architecture.

- Susceptibility of SSTL driver to supply noise. SSTL driver contains level shifter, which operates on core supply and I/O supply both. An increase in core activity can degrade core supply. Noise in I/O supply can be introduced due to simultaneously switching buffers in I/O ring.

- Jitter added due to clock tree itself, which could further get worse due to core supply noise.

- Jitter inherently present in PLL output and degradation due to supply noise.

## Clock Jitter Simulation

It was important to evaluate the performance of individual blocks mentioned in Figure 3.1 to be able to predict their contribution in the overall clock jitter. Models for all the blocks need to be gathered and simulated individually to observe the response. Further, system level simulations should be performed to get the output jitter figures. The modeling

methodology employed and the individual analysis is contained in the next chapter. Chapter 5 and 6 consists of composite model setup and its simulation; and the jitter results obtained respectively.

This evaluation was done at CAD level using Cadence Sigrity Tool, POWERSI; Apache RedHawk suite from ANSYS, ADS suite from EEsof EDA, Keysight Technologies and Synopsys SPICE simulation environment, HSPICE [8].

## 3.3 System Level Modeling

Modeling and Simulation is a discipline of creating a prototype of a physical design to predict its performance in the real world, to evaluate the conditions under which the product could fail and to check whether the measures taken could really work or not. Integrity analysis is to verify before fabrication whether the power supply to each block and the signal are in good condition. For this analysis generation of proper models of the paths in the system under consideration, as we have mentioned above, is one of the earlier steps.

Therefore, let's have a proper understanding as to what modeling and simulation is.

Here, the various terms and aspects related are attended to and a detailed explanation of what system modeling and simulation means is provided.

*System*

A system is any set of things working together as part of a mechanism that exists and operates in time and space.

*Model*

A model is a simplified representation of a system using certain related concepts and idea to obtain a kind of understanding of the real system.

*Simulation*

A simulation often refers to a computerized version of the system under consideration that is simulated over time to study the interactions involved in the system. Simulations are generally iterative, as in one develops a model, simulates it, studies the implications from

the simulation, refines the model, and continues the iterations until an adequate level of understanding is developed as shown in figure 3.2.

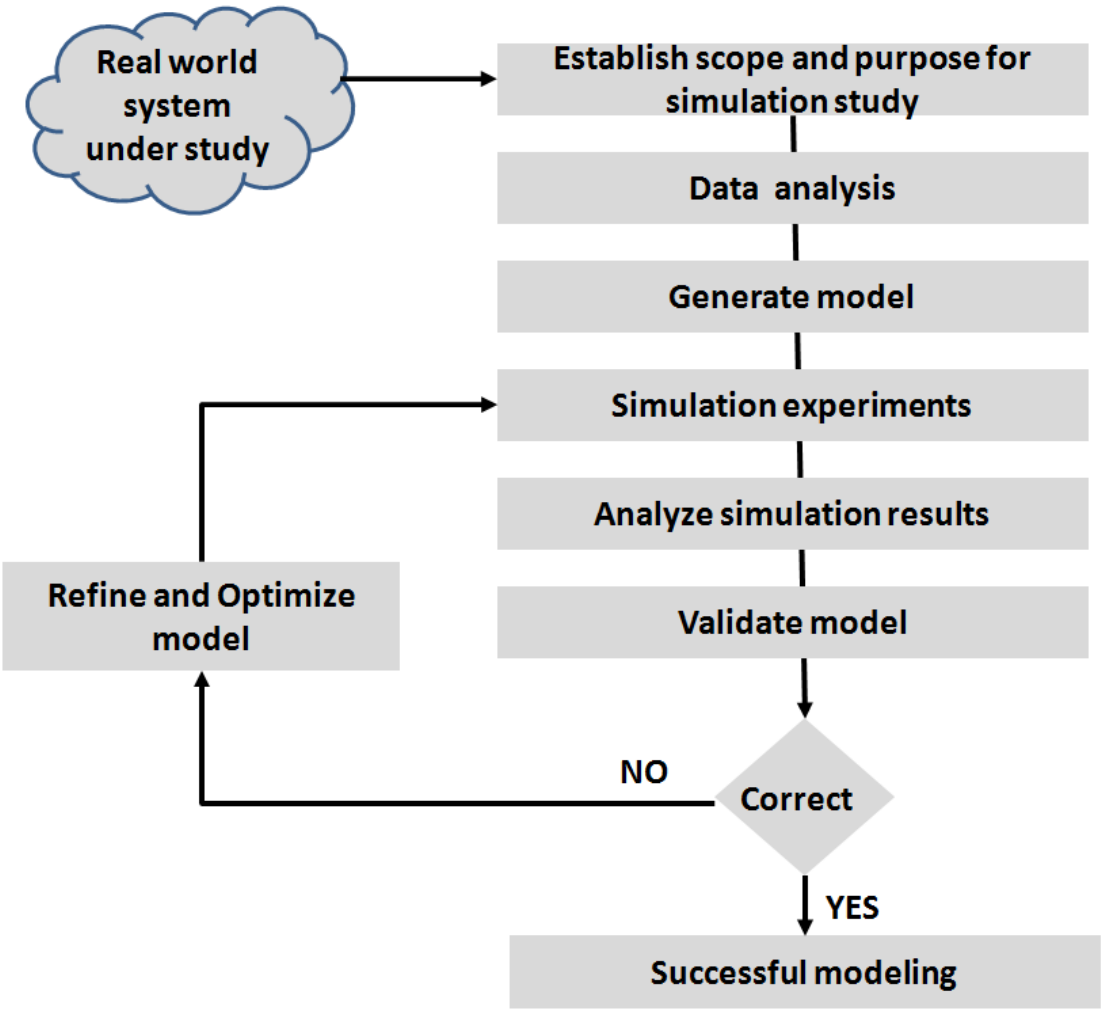


Figure 3.2 General flow of modeling and simulation study

Modeling and Simulation is a discipline for developing a level of understanding of the interaction of the parts of a system, and of the system as a whole.

Since models are nothing but simplification of reality, there will always be a tradeoff as to how well defined the model is to represent the real system and how simple it is to understand. Therefore, there are a few factors that need to kept in mind while generating a model,

- There should be adequate details to cover relevant interactions.
- Complexity should not be very high.
- Time consumption should be optimum.

Low resolution of details while generating the model carries the risk of missing important interactions in the system whereas large number of details would lead to increased complexity. An overly complex model promotes less understanding and may consume too much time.

However, with increasing complexity in the real world design, as is the case in the present generation of integrated circuits, it cannot be helped if their corresponding models turn out to be complex. To reduce the complexity, the system itself can be broken into smaller blocks and models of these small blocks can be created, which obviously would be less complex than modeling the complete system. In this case, validating the functionality of the models as they are connected together is an important issue. Validating any model includes simulating the model under known input conditions and comparing the simulation result with the real world system output.

# Chapter 4

# Power Delivery Network Modeling

Power delivery network in simple words is the network which facilitates the delivery of supply voltages from an external source right up to the supply nodes of various circuit blocks in a DIE.

PDN consists of multiple components sprawling across voltage regulator module (VRM), PCB, package and Die [17] [18] as described in section 2.3. Since the PDN consists of several elements, it cannot be confined in a single model. Models of different components need to be extracted and joined together so as to form a composite network model which depicts the whole PDN.

Modeling of power delivery networks is an integral part of the power integrity analysis process and the modeling methods employed should be evolved enough to model complex power distribution structures accurately with minimum CPU time.

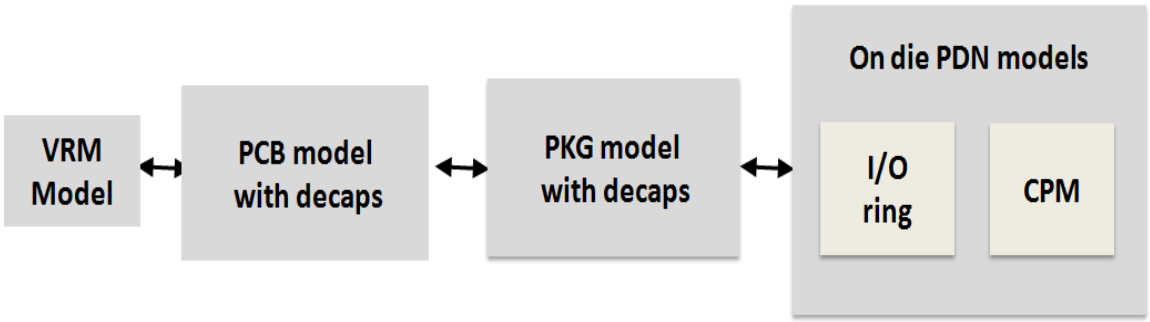


Figure 4.1 Primary parameters of PDN to be modeled

Reliable PDN models are a firm necessity for designers to efficiently evaluate the system PI and EMC performance prior to fabrication.

When we speak about modeling the multiple components making up the PDN, we precisely need to make the aspects of the voltage regulator module (VRM), the PCB and package planes, the package pads and bond wires, the power ground rail parasitics and the

chip's switching current to be available in an acceptable format for the simulation environment.

Power ground planes on the PCB are used to effectively supply the current to the package. The path used contributes some resistance and inductance and therefore several small capacitors are placed near the package critical pins. Some parasitic resistance and inductance are introduced through the package pins too. So for further coupling form these parasitic inductances high performance packages often contain small capacitors. These capacitors have an associated effective series resistance (ESR) and an effective series inductance (ESL), thereby considering the parasitics of the capacitor. The package then gets connected to the chip/die through the solder bumps or bond wires. These bumps also include some additional resistance and inductance. The contribution of the I/O pads and the power ground rail parasitic resistance are also taken into consideration. Finally, the current demands of the chip are modeled as a variable current source[15].

A detailed methodology is explained in the further sections of this chapter. However, the PDN modeling being done is to obtain the PDN impedance, which has to be compared with the target impedance profile. Therefore, obtaining the target impedance is the first priority and the next section covers the same.

## 4.1 Target Impedance Calculation

As explained in section 2.3.2, defining the target impedance is the first step for power network analysis.

The methodology adopted so as to obtain the $Z_{TARGET}$ is to estimate the current drawn by the chip. A worst case scenario is tried to be modeled wherein the maximum transient current would be generated that would affect the system the most.

Figure 4.2 shows the setup created to emulate the worst case condition for the concerned application the chip is to be used. All the I/O buffers, namely, data, data mask, clock, strobe, are all stimulated with a continuously switching pattern (clock like). As a result, all the buffers are simultaneously switching, creating a pressure on the regulator to cope up with the continuously changing current demands ($di/dt \rightarrow max$).

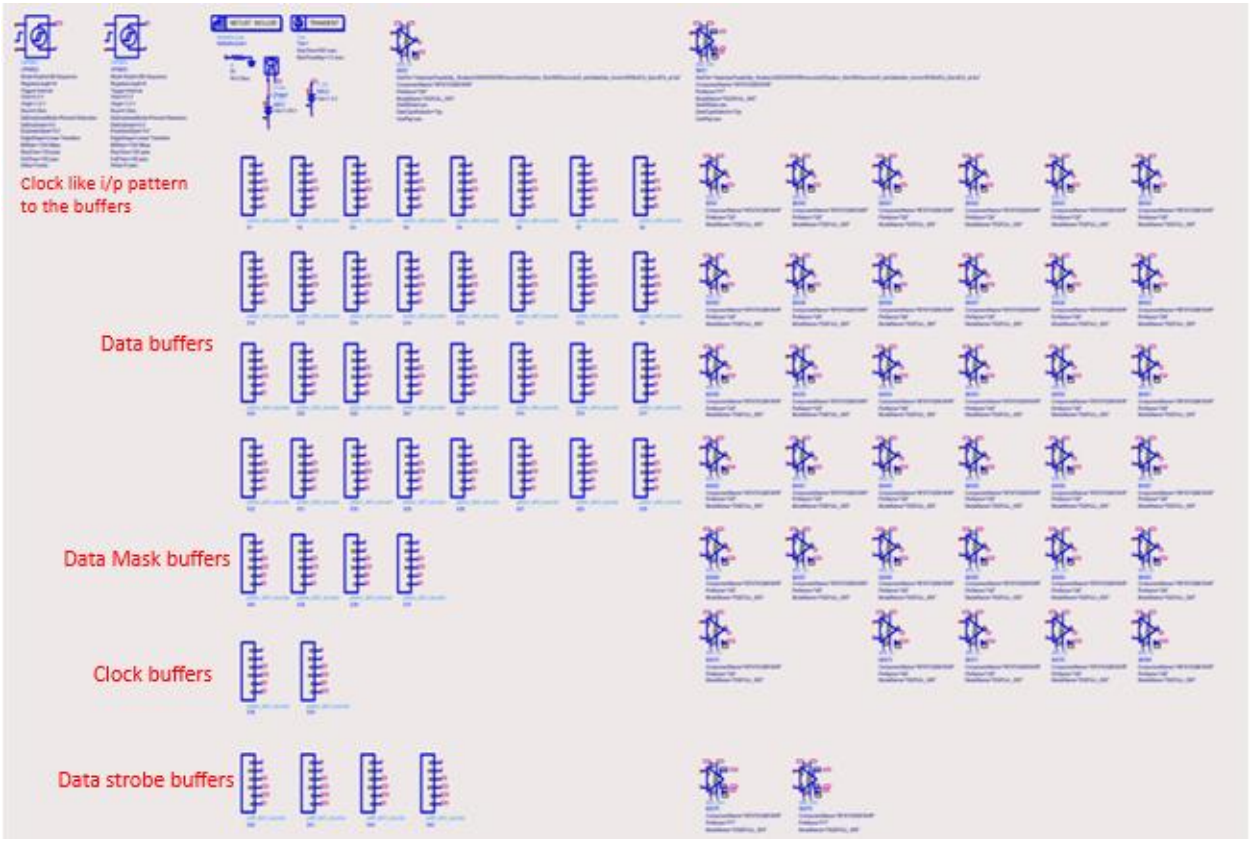


Figure 4.2 Target impedance calculation setup

$$Z_{target}(f) < \frac{V_{ripple}}{I(f)}$$

Keeping the above equation in mind, the spectrum of the transient current is obtained and with a maximum allowable ripple as 20 mV, the target impedance across the frequency range is obtained.

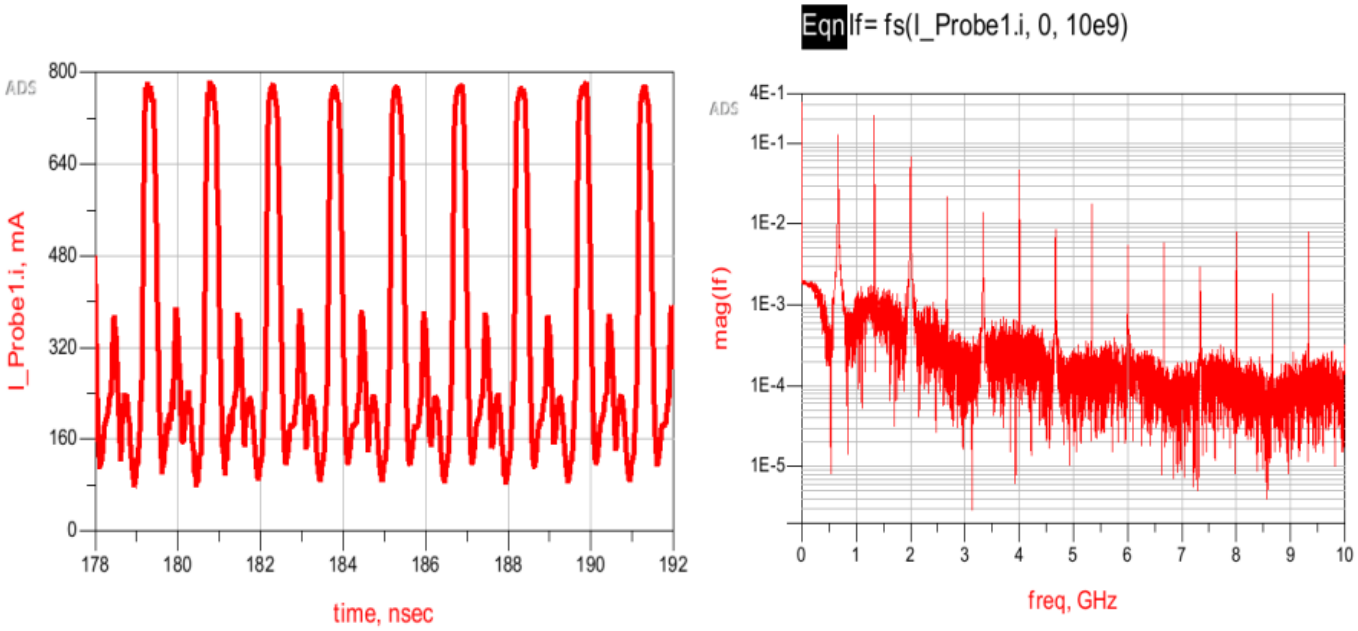


Figure 4.3 transient current profile due to switching in time and frequency domain

Figure 4.3 show the current profile under continuous transitions by all the blocks within the systems. FFT is performed on the time domain transient current so as to obtain the worst case transient current profile in the required frequency range. Since 20mV was decided as the maximum allowable drop, the target impedance profile was obtained for the required frequency range using equation mentioned above and the transient current profile as shown in figure 4.4

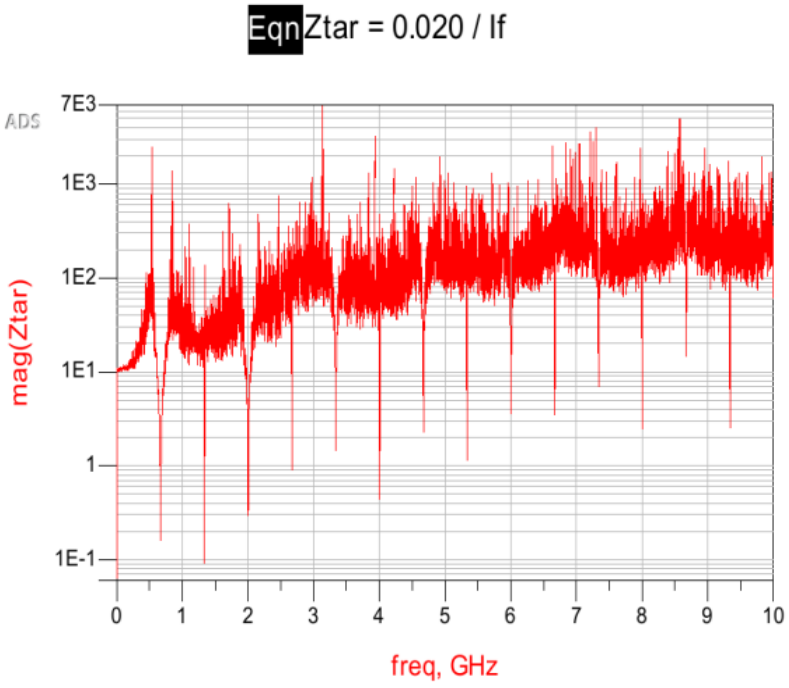


Figure 4.4 Target impedance profile

## 4.2 Board (PCB) and Package (PKG) Modeling and Analysis

### 4.2.1 PCB Modeling

Fast and accurate analysis of IC packages and PCBs is necessary for handling the increasingly challenging and interrelated power, signal, and electromagnetic interference (EMI) issues.

A broad range of studies to identify trace and via coupling issues, power/ground fluctuations caused by simultaneously switching outputs needs to be readily performed. Frequency-dependent s-parameters for board and package modeling for subsequent simulations is extracted using Cadence Sigrity Tool PowerSI [19].

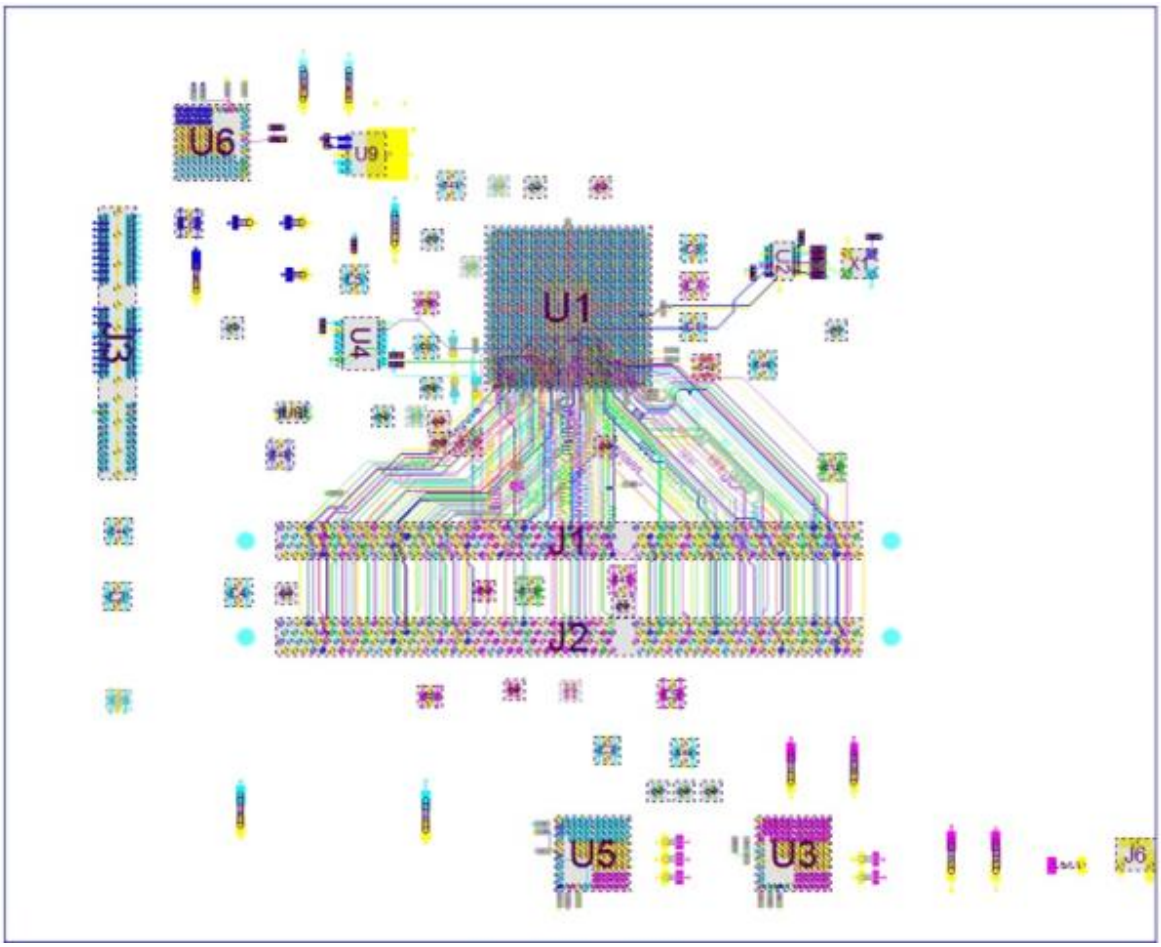


Figure 4.5 A view of the PCB file used

Figure 4.5 provide a visual idea of the PCB brd file. Precisely it represents the top layer of the PCB stackup. Modeling as per our requirements and the further analysis made over the modeled network is explained in the following sub-sections.

Modeling

S parameters play a dominant role in high speed PCB simulation and verification. For details about the basics of s-parameter refer to section 2.4

While generating S parameters for the PCB traces we verify the stack up, identify the ports, provide source and load terminations and select the frequency range. For this purpose, CADENCE Sigrity tool POWERSI is used.

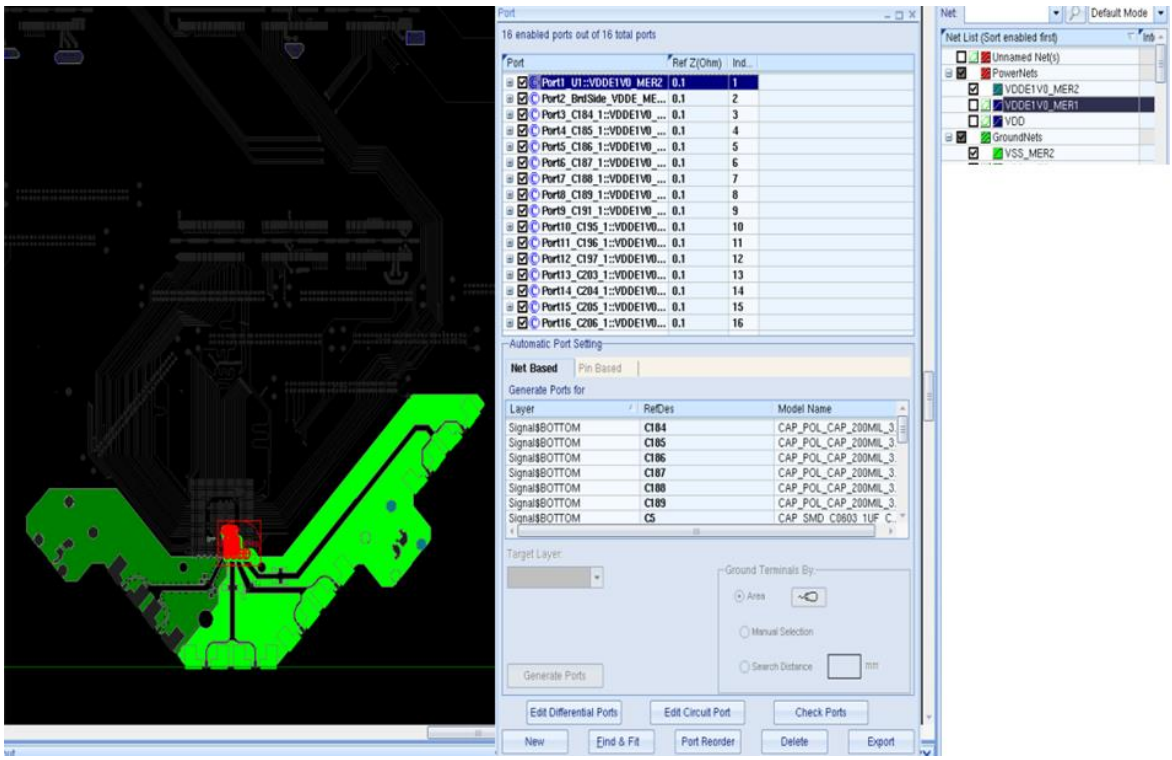


Figure 4.6 modeling stages carried out on the PCB in Sigrity tool POWERSI

First step after loading the brd file under consideration is to verify the stackup. Stackup data consists of the properties (thickness, conductivity, dielectric constant, loss tangent, etc.) of the individual layers that forms up the PCB.

Once this is taken care of, identify the power net on which analysis is to be done. Selected Power and ground net will be highlighted on the appropriate layers as shown in the left side of the figure 4.6.

Components corresponding to the selected net will be activated. Identify locations where ports are to be defined using which the s-parameters would be extracted. One would be the VRM port through which the input is to be applied, other being the chip and the remaining ports would be based upon the decoupling capacitor locations.

Once all the requisites are met, define the sampling technique and the frequency range till which the parameters are to be extracted.

A touchstone format file containing the s-parameters is obtained as the output and this file is used to do the further analysis of the PCB power delivery network.

PDN analysis

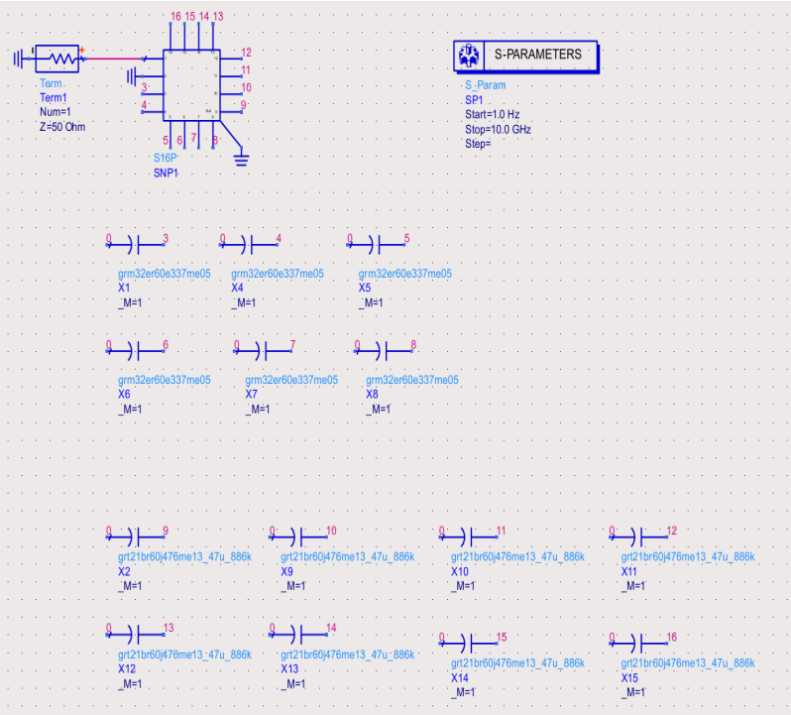


Figure 4.7 PCB PDN setup in ADS

The motive behind extracting the s-parameter, was to analyze and pass judgements over the network impedance.

The s-param file(SNP) is imported into ADS and appropriate decaps are placed as per the ports declared while extracting the s-params. Inorder to view the impedance, voltage sources are shorted and ‘term’ is placed to define from which location the impedance is to be plotted.

Figure 4.8 shows the impedance that the power net faces on the PCB. The maximum voltage drop on this power network would be based upon this impedance and the transient currents. Hence, it is imperative to keep the PDN impedance well below the target impedance. However, this basically forms only the PCB power delivery network for the respective net. The total PDN for the power net under consideration would have cumulative effects from that of PKG and die. Therefore, the next stage would be to model the PKG PDN

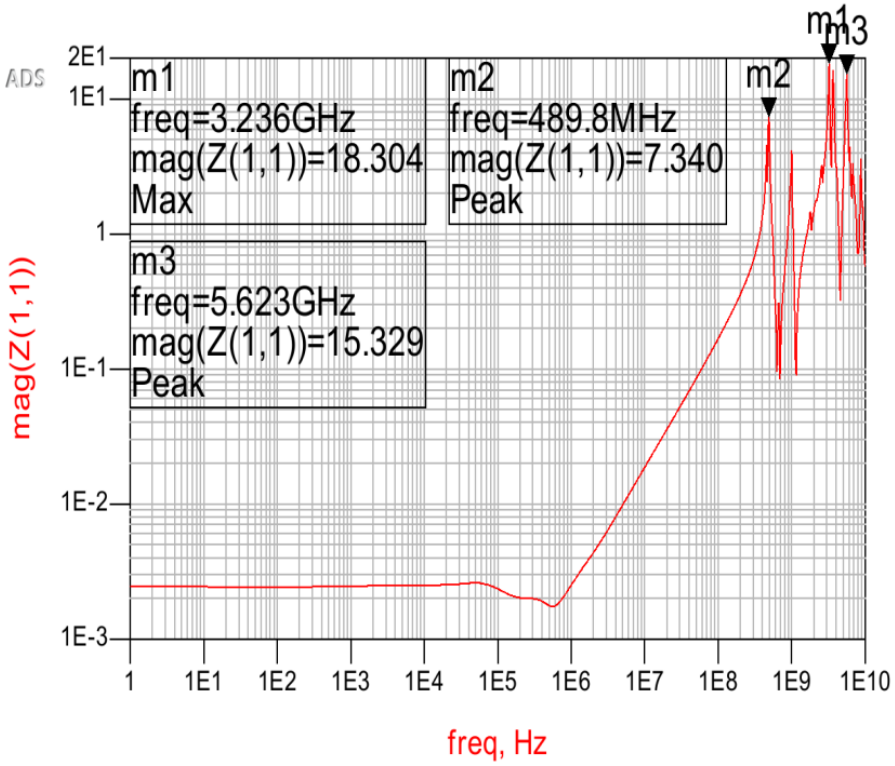


Figure 4.8 PDN impedance as observed on the power net

Optimization

The PDN impedance was observed for different combinations of de-caps. The existing de-caps were replaced by de-caps having SRF around the anti-resonance peaks and observed for any decrement in the impedance value. As we have discussed above, lower the PDN impedance better the power integrity would be. Here, the default de-caps are replaced with different value de-caps of the same dimension and the combination with better $Z_{PDN}$ is chosen for further analysis. In figure 4.9, red trace shows the $Z_{PDN}$ with default decaps and blue trace shows the optimized $Z_{PDN}$.

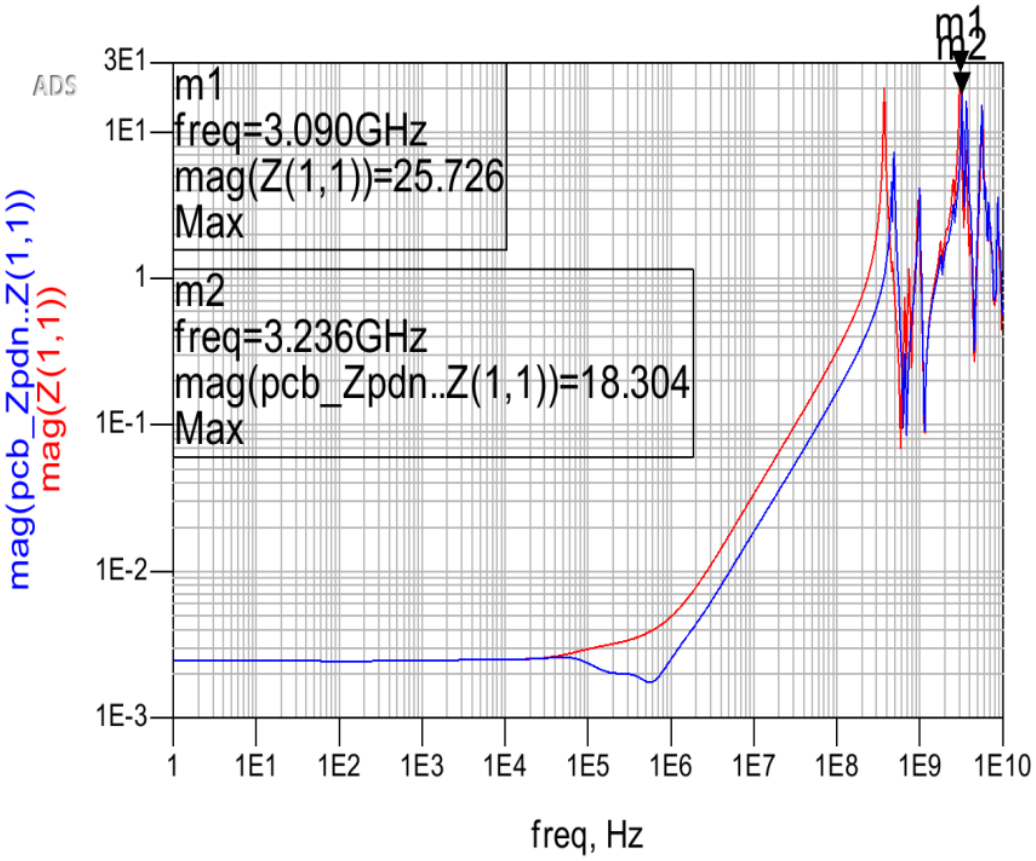


Figure 4.9 PDN optimization result comparision

As can be seen the blue trace which represents the optimized PDN has lesser impedance as compared to the default one

### 4.2.2 Package Modeling

Figure 4.10 shows the top and bottom layer of the package under consideration. Power delivery network for corresponding power net used in the PCB is to analysed. Modeling and analysis of the same is carried out in the subsequent sections.

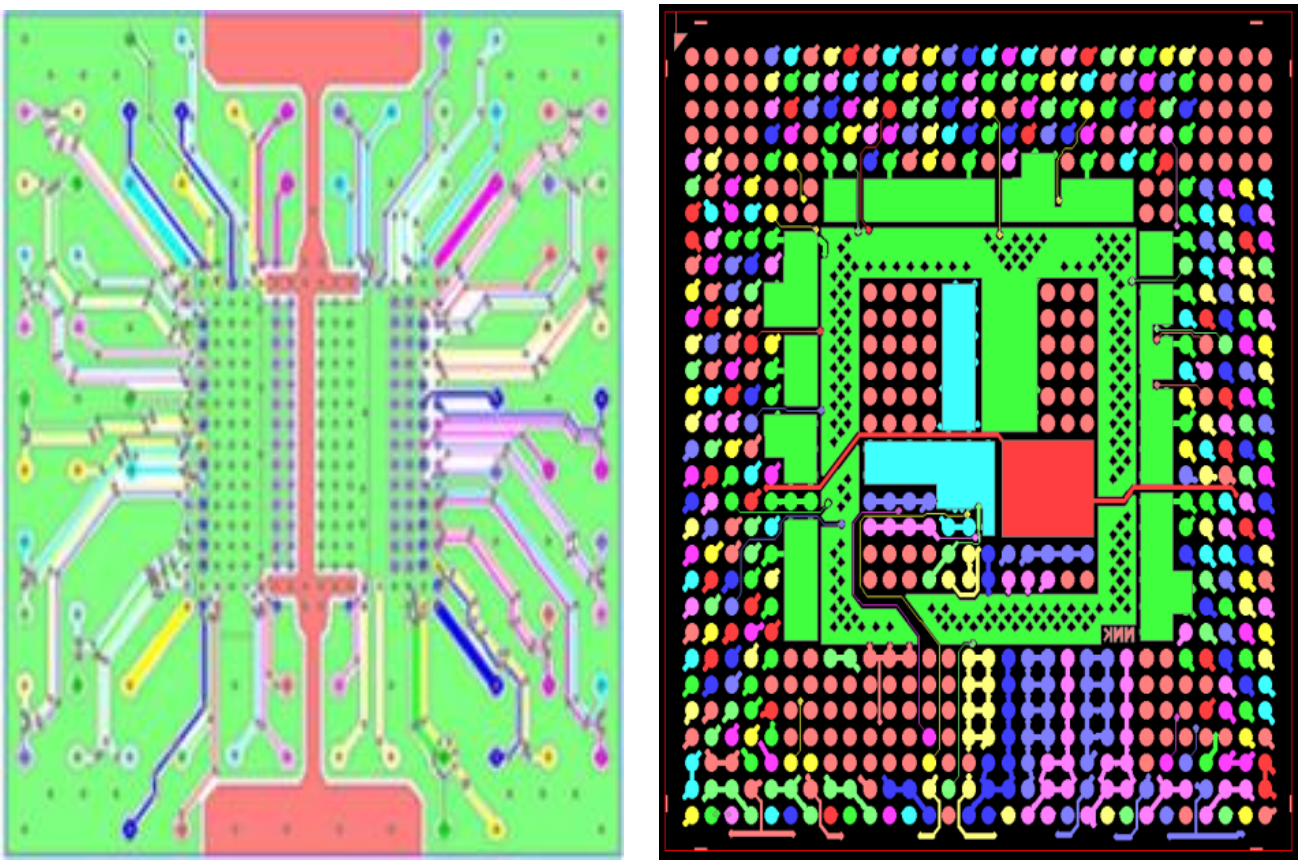

Figure 4.10 a view of the package under consideration

Modeling

Similar to PCB PDN modeling, corresponding power net on the PKG is identified and appropriate number of ports are set, so as to obtain the s-parameter file for the package power delivery network. Same methodology as explained in section 4.2.1 for extracting s-parameters of PCB power nets is followed with the package power net too. Again a

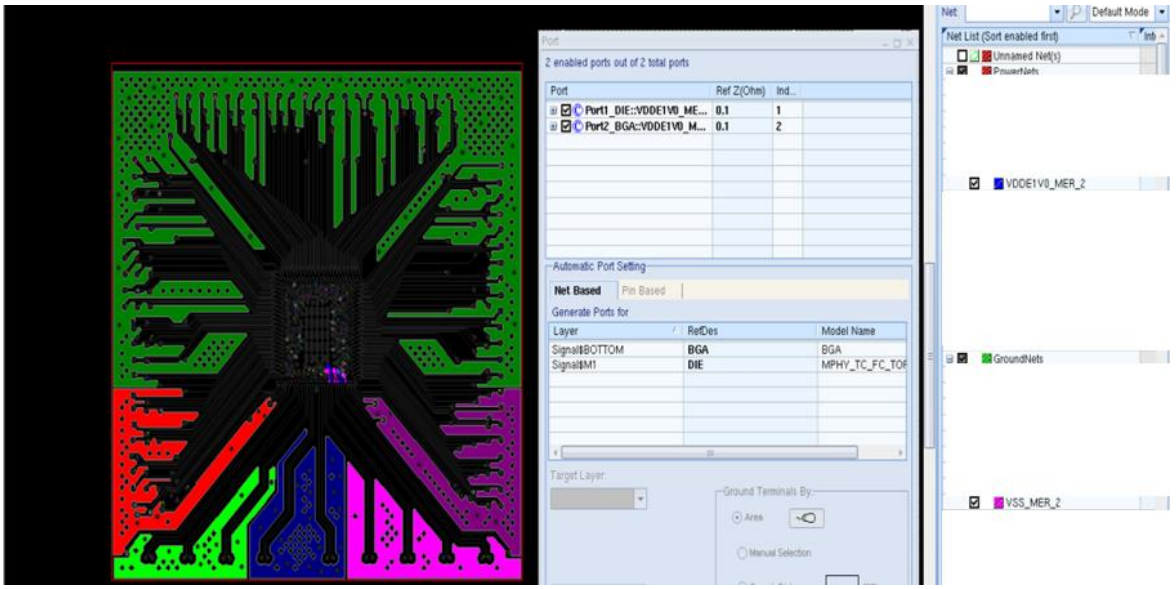


Figure 4.11 Modeling stages carried out on the package in Sigrity tool POWERSI

touchstone format s-parameter file is obtained after the extraction flow in POWERSI is completed.

PDN analysis

The same series of steps are taken once the s-parameter file is generated to obtain the package PDN impedance. The BGA through which the package connects to the PCB is shorted and the impedance is observed from the DIE side. Figure 4.13 shows the impedance that the power supply voltage faces as it travels from the DIE to BGA or vice-. versa

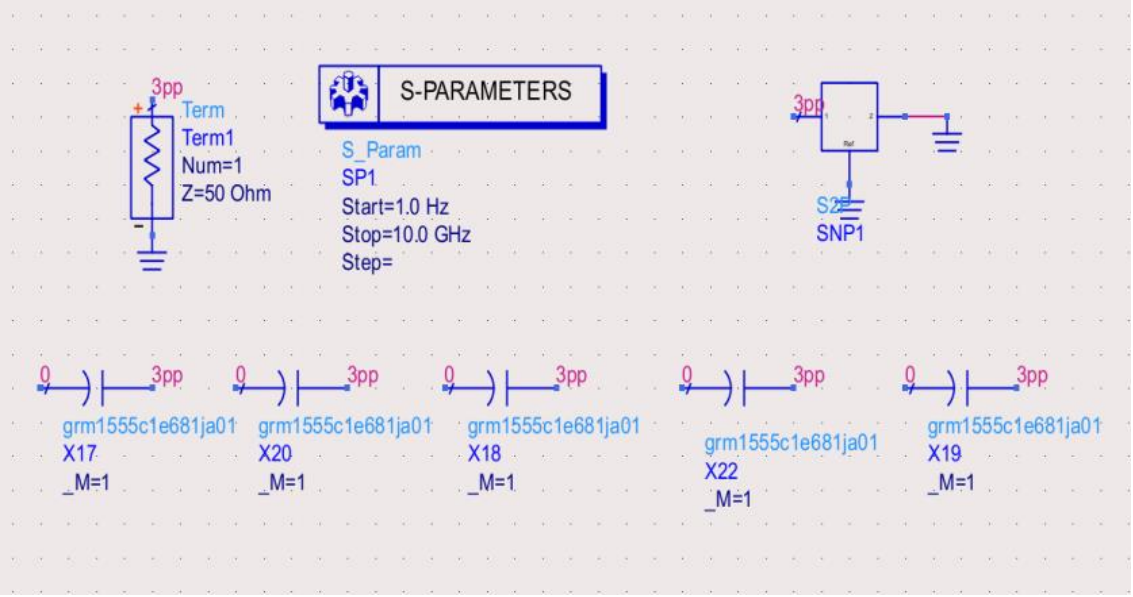


Figure 4.12 package PDN setup

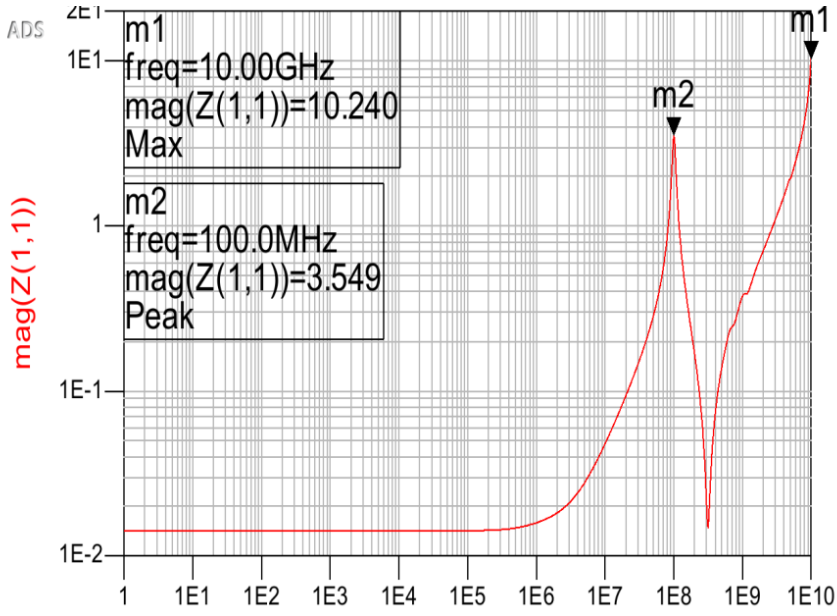


Figure 4.13 PDN plot of power net in the package

Optimization

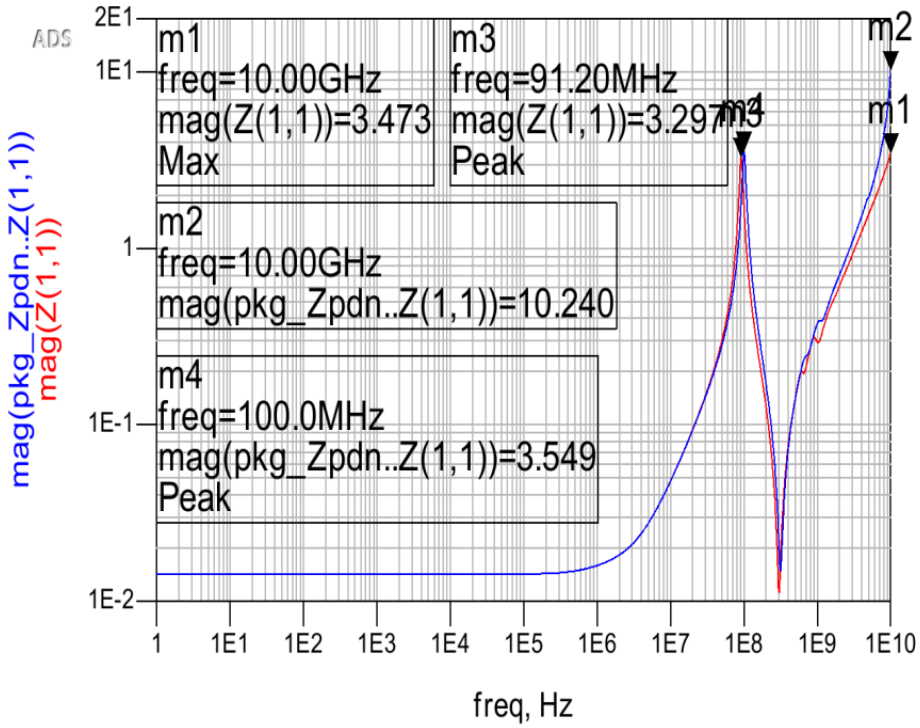


Figure 4.14 comparative analysis of optimized package PDN

Package capacitor values are changed for combinations that provide a better result. Figure 4.14 gives a comparative analysis between two combinations of de-cap values.

## 4.3 On-Die Modeling and Analysis

On-die modeling factors include the contribution of the I/O pads, the power grid rail parasitic resistance and capacitance; and the chip power model.

### 4.3.1 I/O ring modeling

I/O ring modeling is done by creating SPICE models for individual type of buffers taking into account the parasitic effects and the pad and bump connection. Following figure gives a generic idea about the I/O ring and the power grid rails.

Figure 4.15 shows a typical I/O ring formation with the varied colours of rectangular shapes representing different kinds of buffers and the resistances and capacitors represent the parasitic of the power rail.

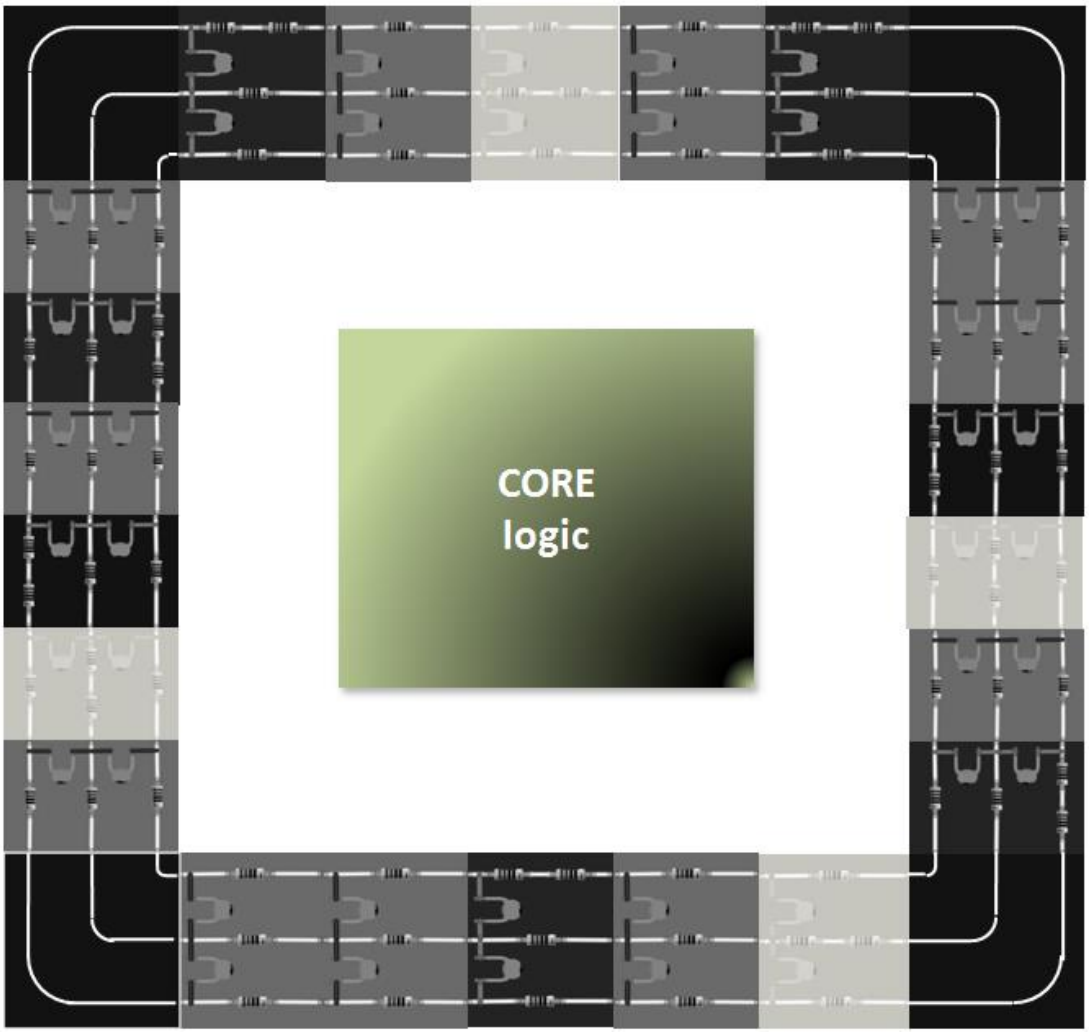


Figure 4.15 general structure of I/O ring and rail parasitics

SPICE models are created for individual type of buffers taking into account the width and length of each of them and the effective parasitic in the buffer area. Once all the SPICE models are generated, depending upon the order the buffers are placed in the I/O ring, their corresponding SPICE models are concatenated to make a complete model of the I/O ring. This created SPICE netlist can then be imported into any simulation environment to add the contribution of the I/O pads and the power ground rail parasitic resistance and capacitance

### 4.3.2 Chip Power Modeling

A second parameter of the on-die PDN model is the chip switching activity. In our PI/EMC-aware design flow ANSYS' tool suite Apache RedHawk [24] is used to generate a SPICE format chip power model (CPM) consisting of the die equivalent impedance network and current profile at a selected pin or group of pins.

Determining the current signature for each component accurately is one of the critical aspects of CPM generation. Particularly, for large complex blocks, it is essential to derive the current profile from a well defined characterization. The input transition time and output load capacitance of each library cell is taking into account to simulate the dynamic current behavior of the entire SoC.

In our approach, this current signature is determined using a vector-based set of stimuli (VCD file) obtained from the logic simulation.

However, VCD generation is just the beginning of this process. CPM generation is a tricky and tiring task. A GSR (global system requirement) file needs to be created consisting all the inputs required for CPM generation and certain simulation conditions. These inputs consists of the files that define the physical structure of each cell , for example the def, lef, lib files and so on associated with the used cells. Using these files as inputs the chip layout map is obtained

Once the layout map is obtained in RedHawk through the GSR, there are quite a few steps more to be considered till we reach the SPICE compatible chip power model. First the network extraction needs to be performed to obtain the RLGC model of the power net under consideration. The second step is to perform voltage drop analysis which will provide the voltage data based upon the switching information and current extracted from the VCD file.

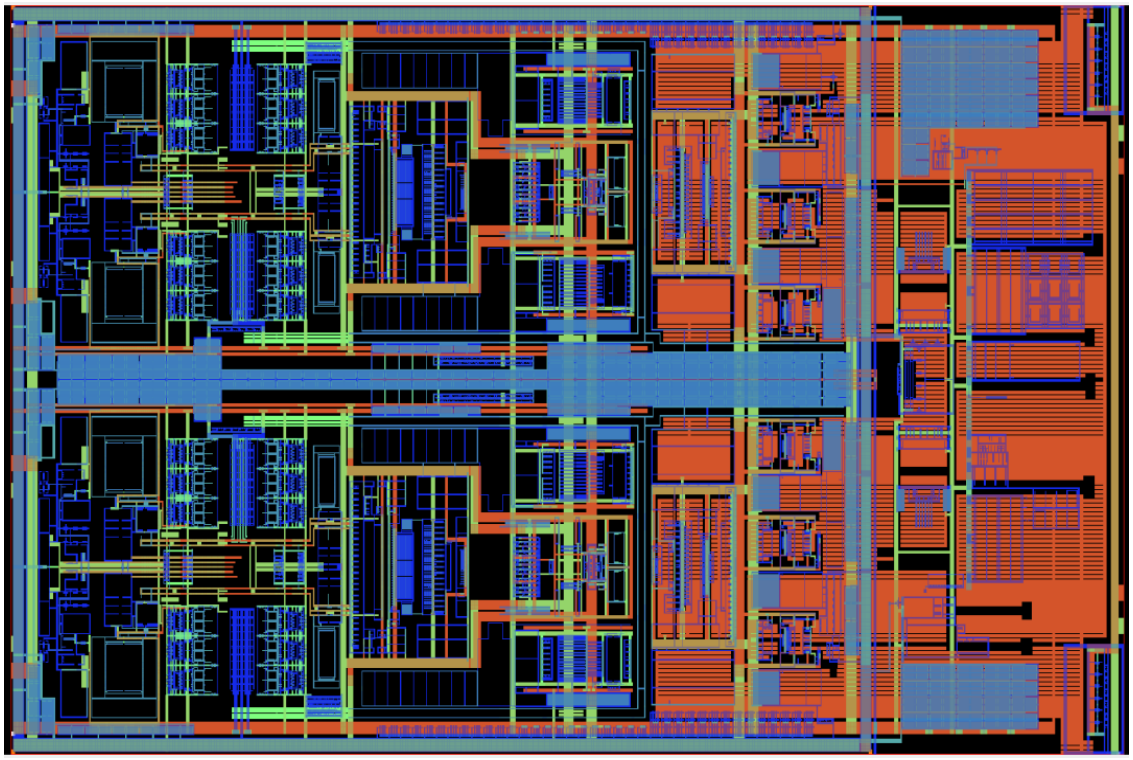

Figure 4.16 chip layout map

Once this is done, the chip power model can be generated which will provide the current profile for all the power ground pins mentioned in the pad location (.ploc) file provided.

## 4.4 Buffer Modeling

Knowing the output behavior of individual buffers to switching activity is the most important factor when SSN effect comes into picture. Using the SPICE models directly results into a time consuming, never ending simulation process.

To speed up the process, each type of buffer was run individually in HSPICE to obtain the current profile of every kind of buffer used [18]. The current profile as shown in figure 4.10 represents the switching behavior of the buffer and is stored as a piece-wise linear waveform to be used later in the jitter analysis.

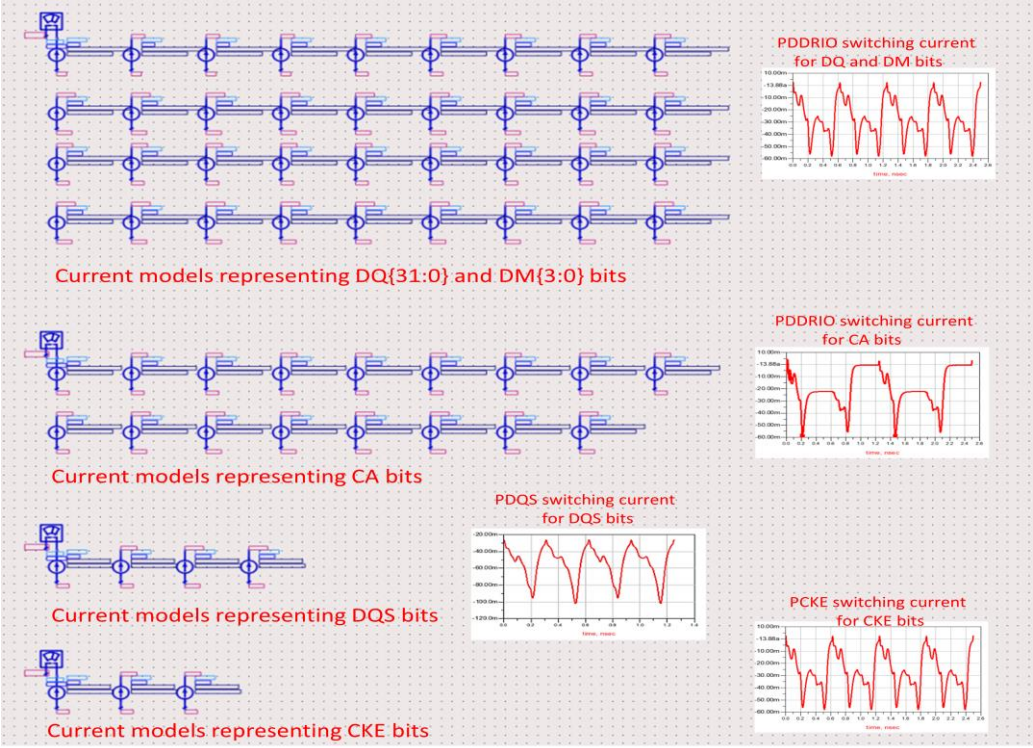


Figure 4.17 SSTL buffer switching profile

## Chapter 5

# Co-Simulation for Combined Effects and Analysis

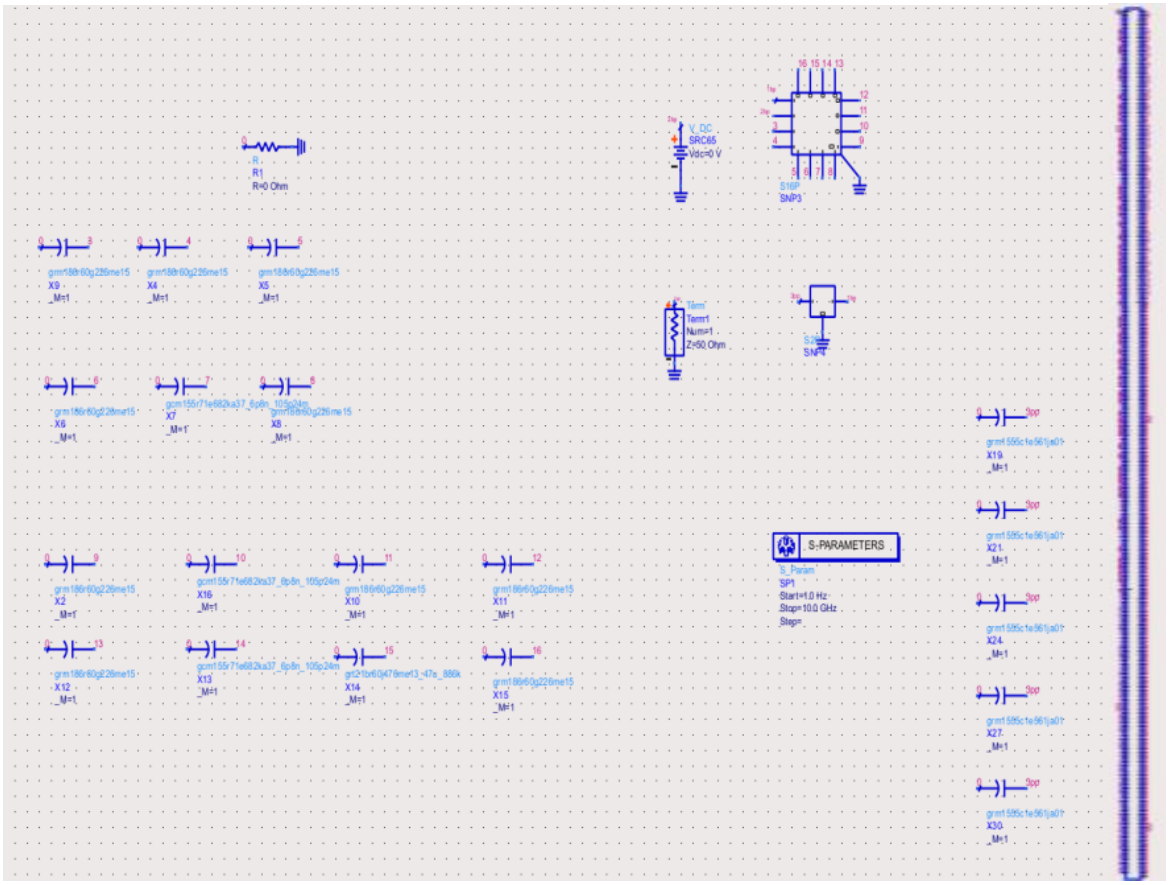


Figure 5.1 Composite PDN setup

Once all the individual models are readily available at hand, its time to combine them all together to analyze for any degenerative interaction which can cause the entire system to fail. The performance of the system can thus be predicted before even its physically implemented.

Since quantizing the power supply induced jitter has been the aim of our analysis, the individual models are connected in such a way that the power supply would pass from the VRM to the package via the PCB planes and routes, from the PCB to the BGA bumps of the package, from the BGA to the supply solder bumps of the chip, from the bumps to the buffer and the core logic via power ground rails. To emulate this route, the PCB and

package models are properly concatenated. I/O ring SPICE model is provided the supply that comes out of the package pin. CPM is appropriately applied and the total amount of power supply variation due to all the activity stored in the CPM is obtained. The section on jitter results will consist about the details of what is done with the discrepant power supply data. For now, let us analyze the impedance that this complete path provides for which the setup made in the simulation environment is shown in figure 5.1

## 5.1 Composite PDN

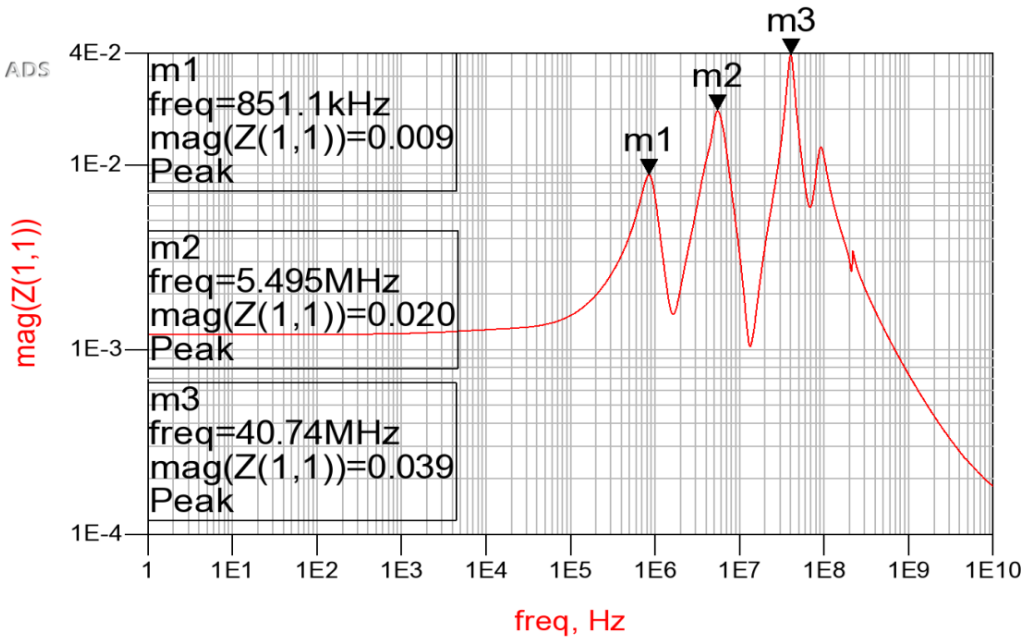


Figure 5.2 Total PDN plot

Figure 5.2 shows the composite PDN impedance obtained by considering all the individual models together in ADS simulation environment. The plot represents the total PDN impedance, the contributing factors being the PCB and package interconnect resistances, decoupling capacitance and its ESR and ESL, power rail parasitics, bump resistances.

## 5.2 Optimization

The PDN impedance was observed for different combinations of de-caps. The existing de-caps were replaced by de-caps having SRF around the anti-resonance peaks and observed for any decrement in the impedance value.

As we have discussed above, lower the PDN impedance better the power integrity would be. Here, the default de-caps are replaced with different value de-caps of the same dimension and the combination with better ZPDN is chosen for further analysis and comparative studies. Figure 5.3 shows the optimized ZPDN profile. As can be observed, the PDN impedance is well below the target throughout the frequency range which gives an assurance that the worst case transient current would lead to voltage drops not so high to create any dis-functionalities.

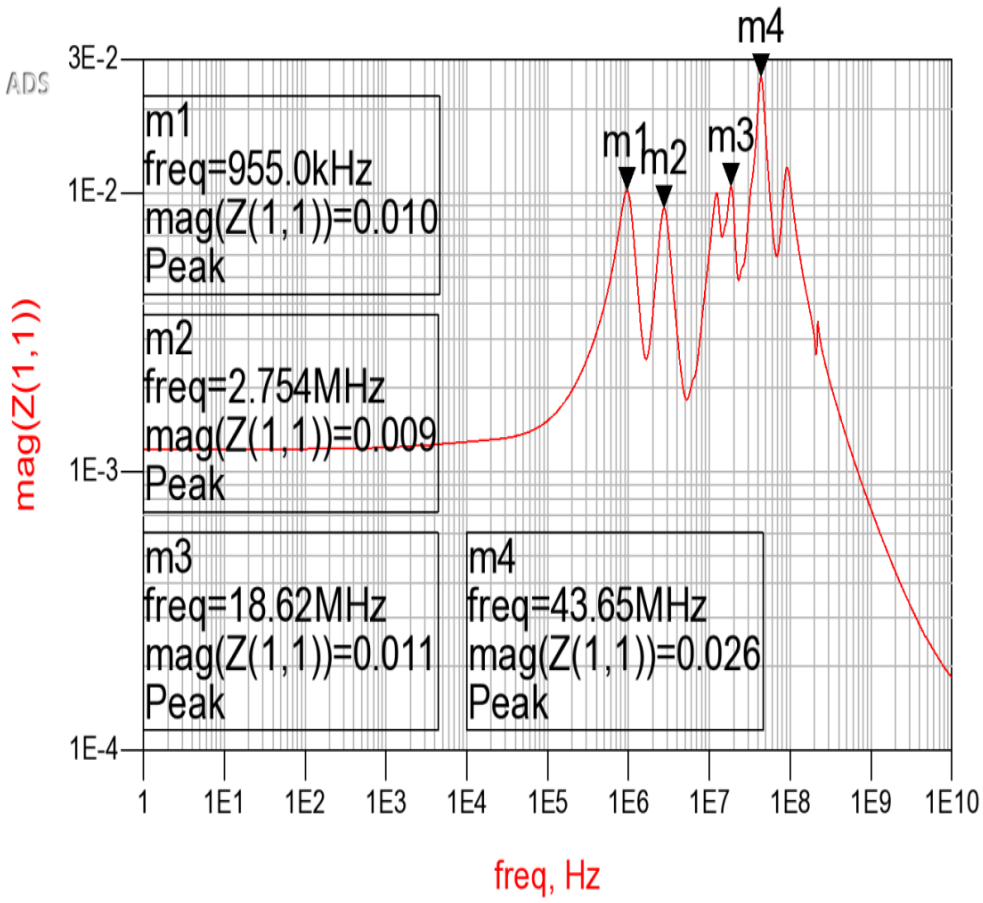


Figure 5.3 Optimized PDN impedance plot

# Chapter 6

# Jitter Measurement Results

Coming to jitter measurement, first the power supply variation caused due to the network and the logic switching is extracted.

Figure 6.1 shows the setup for obtaining the power supply variations. As clock is the

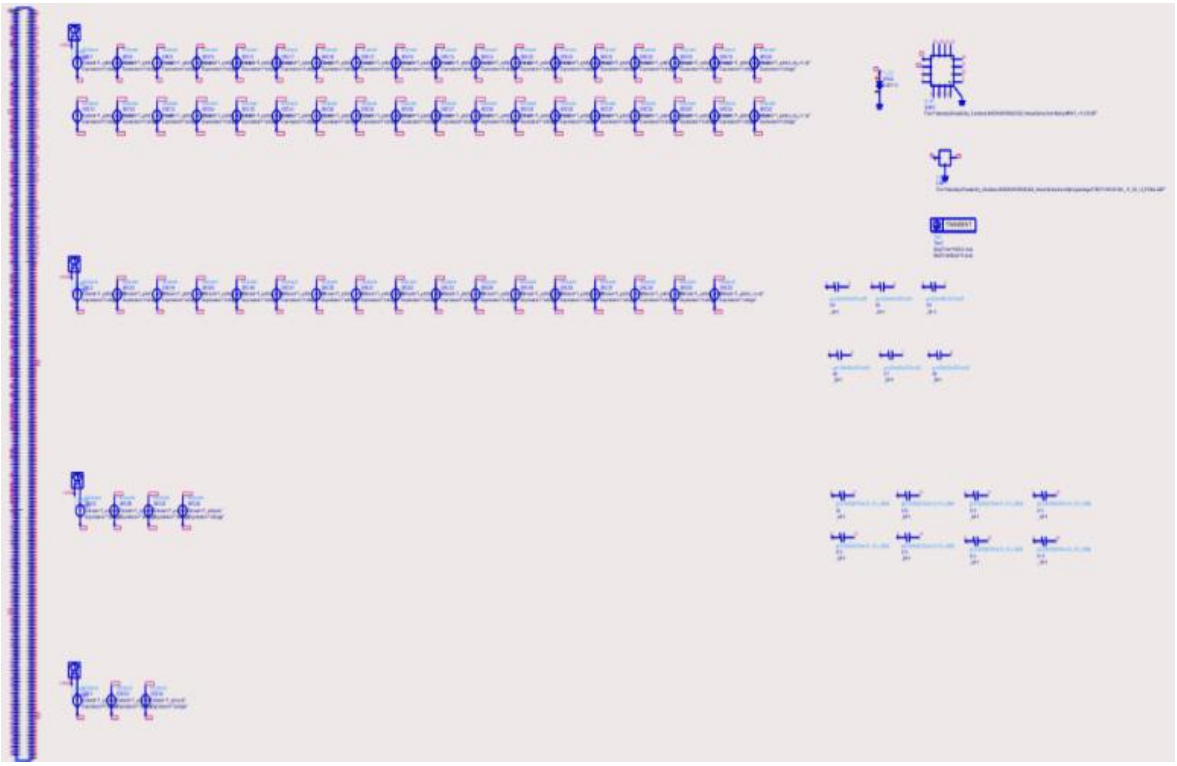

Figure 6.1 Jitter measurement setup

signal that switches most on any system and any discrepancy on the clock signal will lead to disastrous effect on the system integrity, jitter on the differential clock signal due to power supply variations is to be observed for performance analysis. For this, the deterioration of the power supply due to PCB and package interconnects is considered and all the current profile due to the switching activity is added to observe the effect of SSN as shown in the figure above.

The power supply variation is observed on the clock buffer and below shown are two cases of extracted clock jitter. First case shows the jitter under default condition and the other case displays jitter with optimized PCB and package PDN impedance.

## 6.1 Default PDN results

This section shows the results for the unoptimized PDN shown in figure 5.2. The power supply variation at the power supply pins of the clock buffer is extracted. Figure 6.2 shows the fluctuations induced in the power supply due to the switching action of the logic blocks.

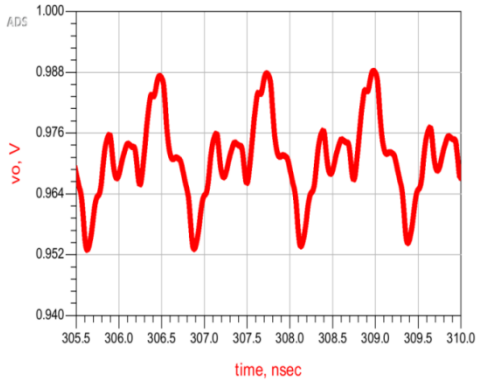


Figure 6.2 power supply variation profile due to switching

This extracted data was applied to the SPICE model of the clock buffer. The output signal (figure 6.3a) thus obtained from the clock buffer will contain the power supply induced jitter. Eye diagram is used as the representation of the digital signal for jitter measurement wherein the width of the intersection of falling and rising pulse in an unit interval is the measured peak- peak jitter.

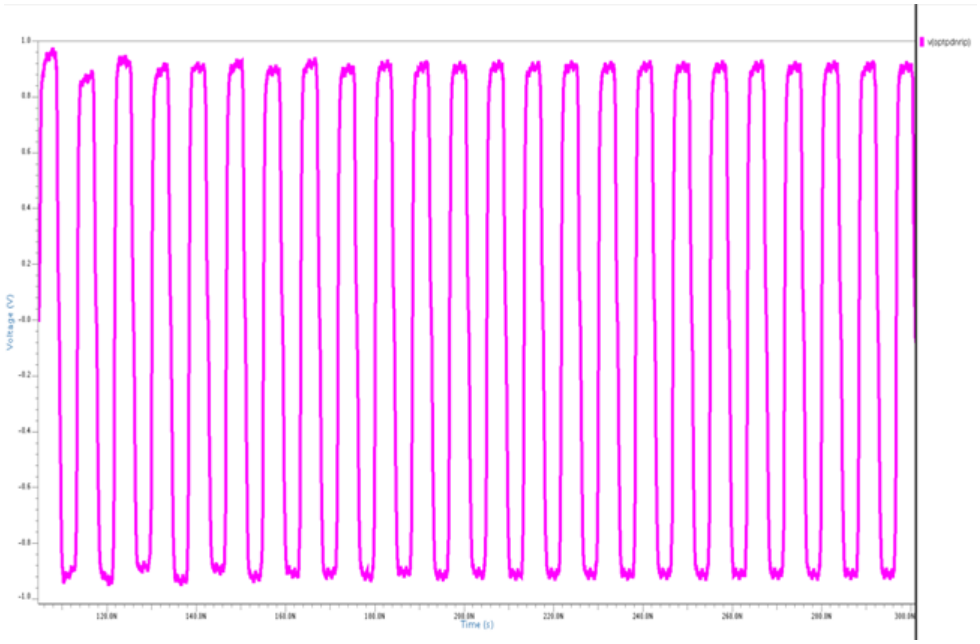

Figure 6.3a PSIJ in clock signal

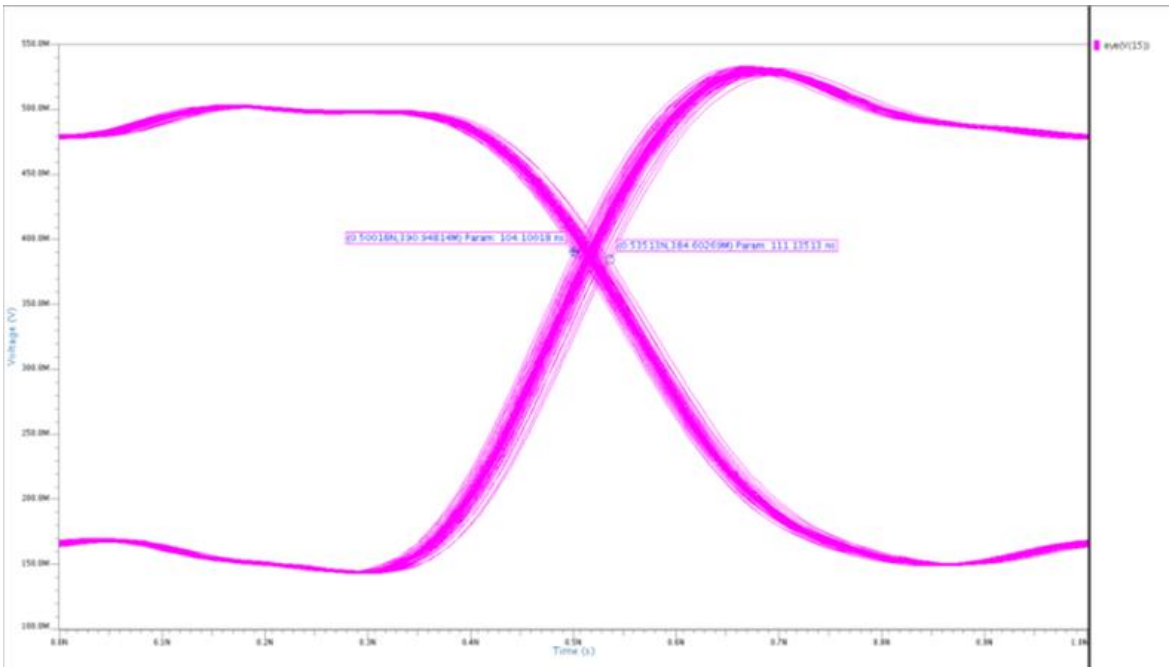

Figure 6.3b eye diagram of jittered clock signal

Figure 6.3a shows the jittered clock output and the corresponding eye diagram is shown in figure 6.3b. The jitter was measured to be 35ps peak-peak in this case.

## 6.2 Optimized PDN results

Similar steps as mention in section 6.1 were taken on the optimized PDN whose plot is shown in figure 5.3. Figure 6.4 shows the power supply variations due to SSN effect. These fluctuations were extracted and applied to the clock buffer for jitter measurement

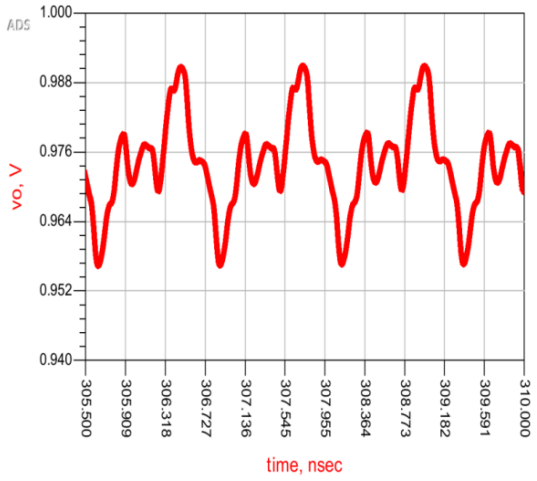


Figure 6.4 power supply variation profile due to switching

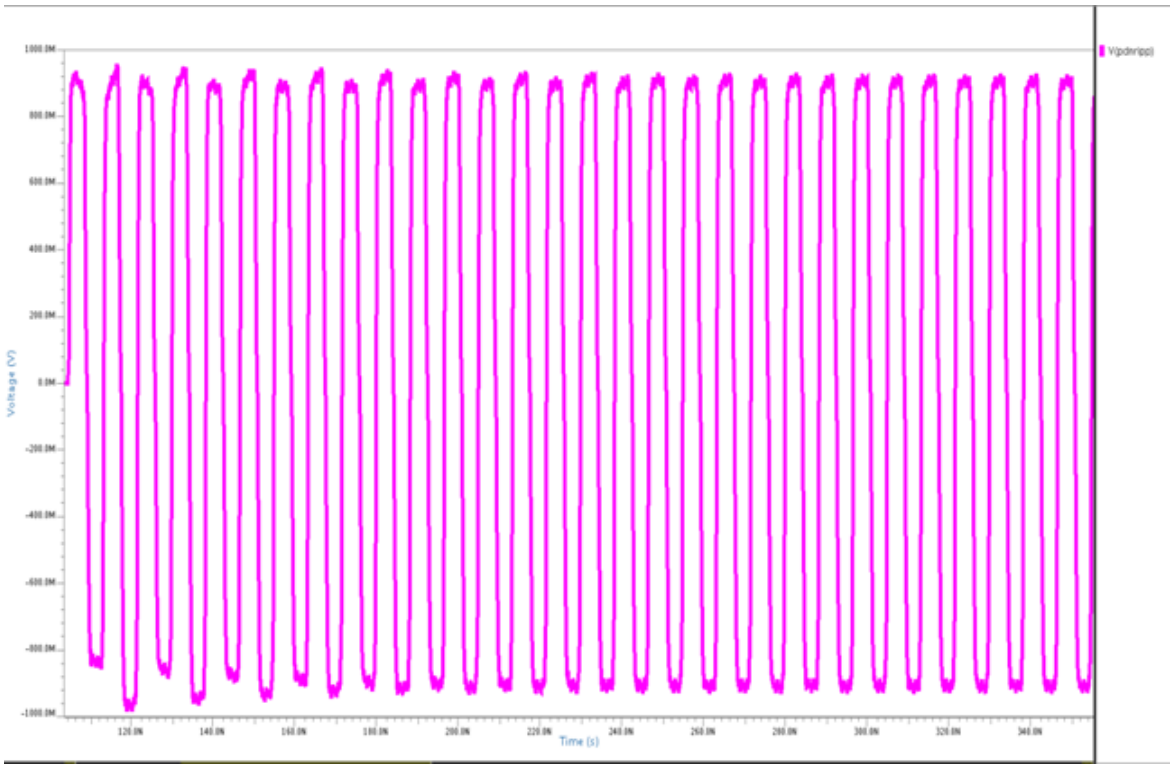

Figure 6.5a PSIJ in clock signal

Figure 6.5a shows the output from the clock buffer and figure 6.5b is the eye diagram of the output waveform. In the optimized case, the jitter was found out to be 20 ps. As predicted the jitter value is lower for better power delivery network design.

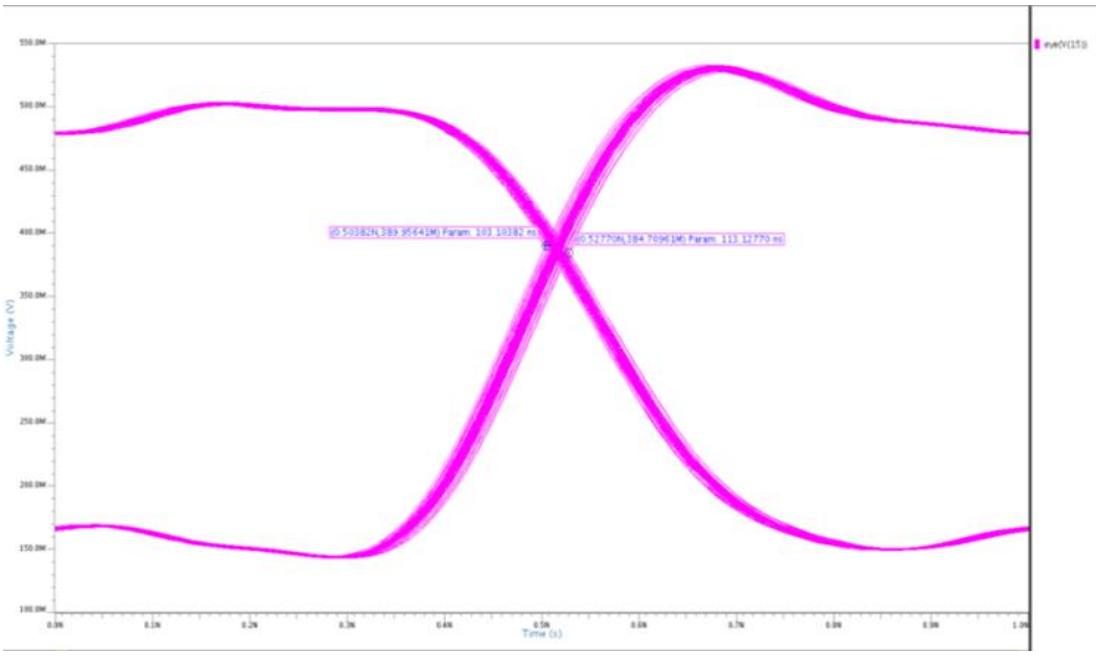

Figure 6.5b eye diagram of jittered clock signal

# Chapter 7

# Inferences and Possible Adaptations

## 7.1 Inferences

Chapter 5 shows the PDN impedance profile and its optimized version. The jitter measurements of both the cases done in chapter 6 shows that the optimized PDN generates lower clock jitter by approximately 16 ps. This is as expected since higher the supply fluctuation, higher is the amount of jitter induced.

| Power Delivery Network | Power supply variation | Power supply induced jitter |
|---|---|---|
| Default case | 0.951 – 0.994 V | 36 ps |
| Optimized PDN | 0.957 – 0.990 V | 20 ps |

Table 7.1 Comparative analysis of PSIJ

Therefore, in-order to keep PSIJ at minimum, PDN should be designed well enough to keep supply voltage as constant as possible.
To maintain the PDN impedance low, here decoupling capacitor network was optimized. Other points that can be considered for better PDN design are as follows [16].

- Place the vias as close as possible to the capacitor, so as to reduce the trace length between the via connecting the capacitor to the power/ ground plane.

- Place the capacitors on the top or bottom plane of the PCB stackup depending upon which plane would be closer to its corresponding power/ground planes, thereby minimizing the via length.

- If possible, use multiple power/ground via pairs to reduce the resistance provided to the current flow.
- Keep the power and ground vias coupled closely as much as possible. This will help reduce the loop inductance, therein keeping switching effects to a low level.

- To keep crosstalk at minimum, place the vias such that the opposite current polarity vias are close together which will negate the magnetic lines produced by the currents thus reducing coupling. Also, same polarity vias should be placed away from one another, so that the coupling between them be as low as possible.

- Length of the power traces on M1 layer should be kept short as much as possible

## 7.2 Possible Adaptations

As its been clear that integrity analysis is now a full-fledged part of the design flow and modeling of the design is required to make integrity analysis possible, we need to find novel ideas to make better accurate models within a short frame of time. With improvement of technology, the operating frequency and speed is increasing and the total time available to get through each stage of the design flow and get the product ready is decreasing. To cater to these needs and to meet the time to market, coming up with methodologies to complete the integrity analysis and giving thumbs up for fabrication, as far as this study is concerned, would only be helpful.

Keeping this mind, a method to deal with the PDN setup and optimization quickly is being proposed. Employing AEL (application extension language) used in Keysight technologies tool ADS (that we use for manual PDN optimization and analysis), some of the stages like PDN setup, de-cap optimization can be accelerated [25].

Scripts can be written to create a generic template of the PDN setup, wherein the user will be given the control to provide the input and simulation settings. The user can input the s-parameter file name for both board and package, number of de-caps, termination resistances, simulation parameters etc. in provided fields of an excel sheet. These parameters will be then parsed into ADS using AEL scripts which will place the components mentioned and run the simulation as required. Once the PDN impedance is plotted on the display window, then a script with the logic for PDN optimization is fired. The PDN impedance is compared with target impedance and the frequencies where the plot is not within the target is noted down. The frequencies where the PDN impedance is missing the target with a large difference is targeted first. De-caps having SRF near to those frequencies are chosen to replace some of the presently available de-caps, decided

on the basis of location effectiveness. The simulation is run with these changes and the impedance plot is now studied in the same manner. These bunch of steps are repeated till the best possible response of the current design can be obtained.

# Bibliography

[1] W. Brinkman, D. Haggan and W. Troutman, "A history of the invention of the transistor and where it will lead us", *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1858-1865, 1997.

[2] J. D. Meindl, "Retrospect and Prospect", *Proceedings of the IEEE International Conference on Very Large Scale Integration (keynote speech)*, October 2007.

[3] M. Popovich, A. V. Mezhiba, and E. G. Friedman, Power Distribution Networks with On-Chip Decoupling Capacitors. Springer Verlag

[4] E. Bogatin, *Signal integrity-- simplified*. Upper Saddle River, NJ: Prentice Hall, 2004.

[5] K. Helmreich, "Measuring Signal Integrity", *IEEE Microwave Magazine*, No. 1011092011941415, 2011.

[6] S. Bothra, B. Rogers, M. Kellam and C. Osburn, "Analysis of the effects of scaling on interconnect delay in ULSI circuits", *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 591-597, 1993.

[7] S. Corporation, "jitter and measurement", *www.sitime.com*, 2014. [Online]. Available: http://www.sitime.com/support2/documents/AN10007-Jitter-and-measurement.pdf

[8] Summit Technical Media, "Jitter—Understanding it, Measuring It, Eliminating It; Part 3: Causes of Jitter", June 2004.

[9] Summit Technical Media, "Jitter—Understanding it, Measuring It, Eliminating It Part 1: Jitter Fundamentals", June 2004.

[10] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 2001.

[11] M. Popovich, E. Friedman, M. Sotman and A. Kolodny, "On-Chip Power Distribution Grids With Multiple Supply Voltages for High-Performance Integrated Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 16, no. 7, pp. 908-921, 2008.

[12] P. Larsson, "Power Supply Noise in Future IC's: A Crystal Ball Reading", *IEEE custom integrated circuits conference*, 1999.

[13] Jim Monthie, Vineet Sreekumar and Ranjit Yashwante "Impact of Power Supply noise on Clock Jitter in High-Speed DDR Memory Interfaces" *VLSI Design and 2013 12th International Conference on Embedded Systems (VLSID)*, 2013, pp. 262-266

[14] June Feng, Bipin Dhavale, Janani Chandrasekhar, Yuri Tretiakov and Dan Oh “System Level Signal and Power Integrity Analysis for 3200Mbps DDR4 Interface” *2013 Electronic Components & Technology Conference,* pp. 1081-1086

[15] Giovanni Graziosi, Patrice Joubert Doriol, Yamarita Villavicencio, Cristiano Forzan, Mario Rotigni, and Davide Pandini “Advanced Modeling Techniques for System-level Power Integrity and EMC Analysis”, *Microelectronics and Packaging Conference,* 2009. EMPC 2009, pp. 1-6.

[16] Printed Circuit Board (PCB) Power Delivery Network (PDN) Design Methodology, 1st ed. San Jose: Altera, 2009.

[17] Narimasa Takahashi, Masahide Nose, Satoshi Kaeko and Yo Takahashi “Analysis of Complete Power-Distribution Network and Co-Design Optimization” *Transactions of The Japan Institute of Electronics Packaging Vol. 2,* No. 1, 2009. 19 \

[18] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, “Power distribution networks for system-on-package: Status and challenges,” *IEEE Trans. Advanced Packaging, 197 vol. 27,* pp. 286-300, 2004.

[19] "Cadence SI / PI Analysis - Sigrity", *Sigrity.com,* 2016. [Online]. Available: http://www.sigrity.com.

[20] I. Poole "What is a BGA | SMD Ball Grid Array Package | Tutorial", *Radio-electronics.com,* 2016. [Online]. Available: http://www.radio-electronics.com/info/data/smt/smd-bga-ball-grid-array-package.php.

[21] Xiang Zhang, , Yang Liu, Xiang Hu, and Chung- Kuan Cheng, "Ratio of the Worst Case Noise and the Impedance of Power Distribution Network", *IEEE Transactions on Components Packaging and Manufacturing Technology*, 2014.

[22] Kim, Jingook, Yuzo Takita, Kenji Araki, and Jun Fan, "Improved Target Impedance for Power Distribution Network Design with Power Traces Based on Rigorous Transient Analysis in a Handheld Device", IEEE *Transactions on Components Packaging and Manufacturing Technology*, 2013.

[23] Novak, L. M. Noujeim, V. St. Cyr, N. Biunno, A. Patel, G. Korony, and A. Ritter, “Distributed matched bypassing for board-level power distribution networks,” *IEEE Trans. Adv. Package.*, vol. 25, pp. 230–243, May 2002.

[24] *RedHawk*. San Jose: ANSYS Apache, 2016.

[25] ADS (Advanced Design System) documentation at Keysight knowledge center at http*://edadocs.software.keysight.com*