NANO SEMICONDUCTING DEVICE BASED DESIGN OF VOLTAGE CONTROLLED OSCILLATOR

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CERTIFICATE

This is to certify that the thesis titled, "NANO SEMICONDUCTING DEVICE BASED DESIGN OF VOLTAGE CONTROLLED OSCILLATOR" submitted by Vivek Kumar Chaturvedi in partial fulfillments for the requirements of Bachelor of Technology Degree in Electrical Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by them under my supervision and guidance. According to me, the matter present in the thesis has not been duplicated from any other sources/papers/thesis for the award of degree.

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I, Vivek Kumar Chaturvedi, student of Electrical Engineering is very thankful for the help and guidance of our esteemed professor P.K Sahu. His intellectuality helped me to focus on my project more and during this I learnt a great deal of project writing and how to implement ideas in a new direction. Further, my departmental colleagues were enough helpful to share their knowledge as we all know a project has to involvement of more domain knowledge and more diverse ideas on other subjects too. I was thankful for the Lab being provided for carrying out the project work.

Prof. A.K Panda, a source for inspiration of every other student has been very firm in making students learn and that's why I was able to carry my work with a zeal and enthusiasm. I am thankful to the NIT campus for such an environment which helped me persevere with calm and composed mind.

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CONTENTS

Contents

List of Figures

ABSTRACT

The fast advancement of the CMOS innovation has made conceivable the improvement of littler correspondence frameworks with expanding usefulness. Yet, as CMOS innovation approaches the Nano-scale, critical deviations in the framework execution may be found because of either interconnect or gadget between and intra-kick the bucket parameter varieties. For the most part, in Nano-CMOS innovation, blemishes in simple and computerized circuits are ordinarily alluded as process' parameter variability. The requirement for executing ease, completely incorporated RF remote handsets has spurred the broad utilization CMOS innovation. Nonetheless, in the specific case for voltage controlled oscillators (VCO) where steadily stringent particulars regarding stage commotion must be accomplished, the configuration of the on-chip LC tank is a testing undertaking, where completely playing point of the real advances qualities must be pushed to about its points of confinement. To overcome stage commotion impediments emerging from the low quality element of incorporated inductors, advancement outline strategies are generally utilized. Low power CMOS and LC Tank VCOs are demonstrated. Their basic and symmetric structure can give low power advertisement low clamor operation. The proposed VCOs can have distinctive focus frequencies.

CHAPTER-1

INTRODUCTION

Discovery of Transistor

In the period 1903-1948, the vacuum tubes was the interest for development. In 1903, the vacuum-tube diodes were developed by J.A. Fleming. It was in 1905 that Lee De Forest introduced a third element called the control grid in a vacuum diode which resulted for the first amplifier, the triode. On December 4, 1948, the electronics industry were experiencing the discovery of a completely new set of inventions and development.

Walter H. Brattain and John Bardeen showed the enhancer activity of the first customary transistors at Bell Telephone Laboratories. The upsides of these three terminal strong state gadgets over the tube were self-evident. Littler light weight had no radiator necessity for warmer misfortune, had unbending development and was more effective on the grounds that less influence was devoured by the gadget , it was then accessible for utilization ,obliged no period and lower working voltage were conceivable. This was the History of Development of transistor, how it came to capacity in the gadgets world.

Transistor model

A transistor is a semiconductor gadget which is used to enhance and switch electronic signs. It is made of a strong bit of semiconductor material with no less than three terminals for association with an outer circuit. A voltage or current connected to one sets of the transistor's terminals changes the present moving through another pair of terminals. Since the controlled (yield) force can be substantially more than the controlling (info) control, the transistor gives enhancement of a signal. A few transistors are bundled exclusively yet numerous more are discovered inserted in coordinated circuits.

The different types of transistors are BJT,MOSFET, IGBT, JFET ,THYRISTORS.

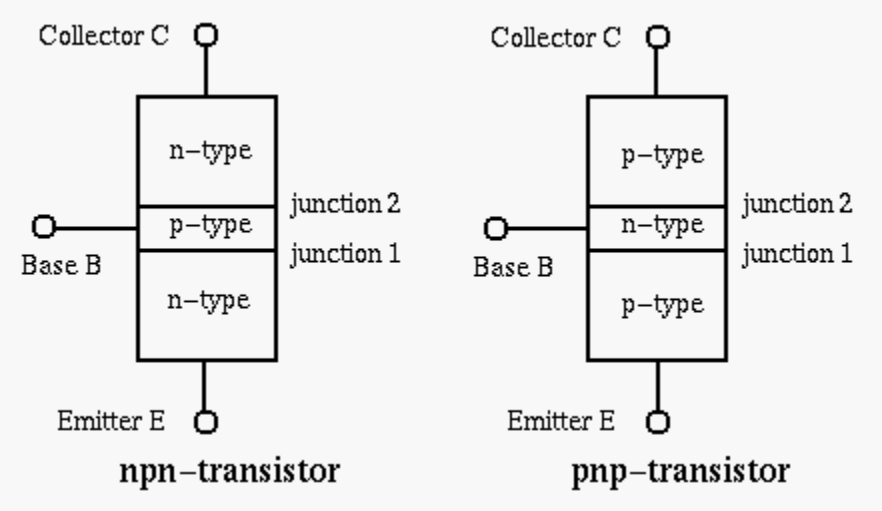
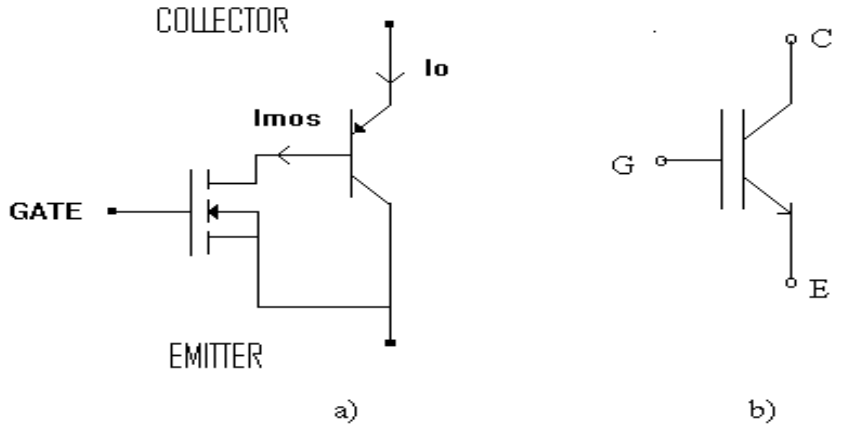


Figure 1: Types of transistor



.Figure 2: IGBT

In our work, we will be mainly concentrating on CMOS.

1.3 OBJECTIVE

The objective is to simulate the VCO circuit using CMOS through MATLAB, P-Spice and TSpice and comparing with the nano CMOS. Comparison with traditional MOS was studied.

1.4 FUTURE PROSPECTS

The future work is to replace the Bulk-CMOS with the nano-CMOS and make the system faster. This includes SD-RAM, Processor, logic circuits, and switches, and also where we can implement these applications.

CHAPTER-2

VOLTAGE CONTROLLED OSCILLATOR

VCO and its types:-

VCOs can be parted into two social occasions in light of the assignment variable of waveform made:

1) Harmonic oscillators, and 2) relaxation oscillators.

Straight or consonant oscillators give a sinusoidal waveform. Consonant oscillators in equipment contraptions regularly are involved a resonator with an "intensifier" that diminishes setbacks and partitions the resonator from the sign yield. Delineations:- symphonious oscillators are LC-tank oscillators and valuable stone oscillators. In a "VCO", the voltage information controls full repeat. A 'varactor diode's capacitance' is controlled by the voltage over the diode. Accordingly, a varactor can be used to change the capacitance (and hereafter the repeat) of a LC tank.

Relaxation oscillators give a sawtooth or triangular waveform. They are used as a piece of strong facilitated circuits (ICs). They usually give a broad mixture of operational frequencies with an irrelevant outside parts devices used. Loosening up oscillator "VCO" have three sorts:

1) grounded-capacitor 'VCO',

2) deferral based ring 'VCO'., and

3) emitter-coupled "VCO"

The beginning two representations work as a general rule with same qualities. The time taken in every state depends on upon how fast/direct charging or discharging of a capacitor. For this sort the expansion pieces are related in a ring. The yield repeat transforms into a component of the deferral in every stage.

Harmonic oscillator VCOs purposes of advantages over relaxation oscillators are:-

1) Frequency unfaltering quality on grounds to temperature, uproar, and power supply is suitable for consonant oscillator VCOs.

2) The precision for repeat control taking after the repeat is controlled by a tank circuit is more in Harmonic oscillator. Disadvantages of harmonic oscillator VCOs is that they are

difficult to implement in monolithic Integrated Circuits. Relaxation oscillator ‘VCOs’ are better for this technology. Relaxation VCOs can also be tuned for a wider range of frequencies.

CONTROLLING FREQUENCY IN VCOs

A voltage-controlled capacitor is utilized to roll out an LC oscillator for the improvement of its recurrence in response to control voltage. An opposite one-sided semiconductor diode is utilized to show how quite a bit of voltage-ward capacitance is utilized to change the recurrence of the oscillator by changing info control voltage being connected to the diode. "Voltage variable capacitance" varactor diodes are utilized with described wide-extend quantifiable estimations of capacitance. For low-recurrence 'VCOs', different routines for differing the recurrence is finished by changing the charging/releasing rate of a capacitor by method for a voltage controlled current source which are utilized.

Ring oscillator's recurrence is controlled by fluctuating either the supply voltage, the current accessible to each stages of an inverter circuit, or the capacitive stacking on every phase of the ring.

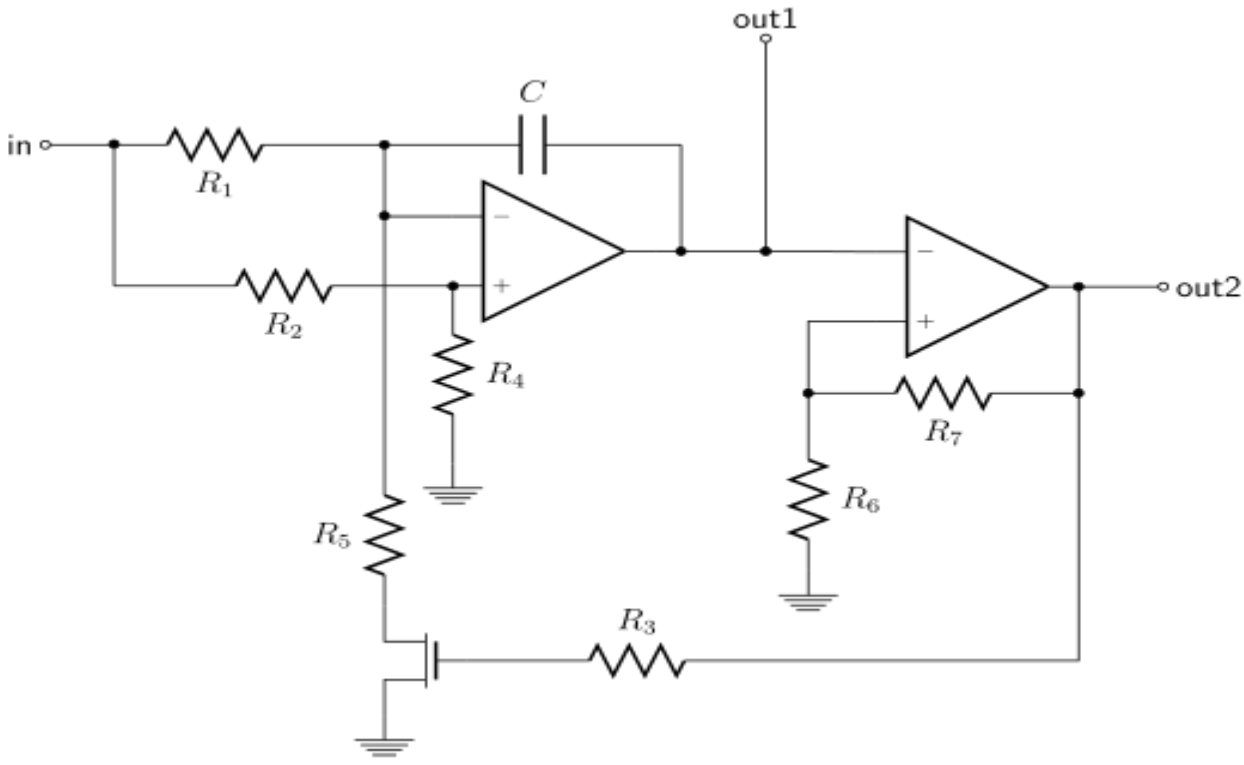


Figure 3: :- showing a typical opamp based VCO’s

Phase domain equations

Simple applications, for example, "recurrence adjustment" are utilized to control oscillator recurrence with a "voltage-controlled oscillator" (VCO). The 'relationship capacity' between the control voltage and the yield recurrence is non direct however for little ranges, the relationship is about straight, and along these lines straight control hypothesis can be utilized.

'Genuine VCOs' particularly those which are utilized at radio recurrence have non-straight relationship. There gadgets are known as voltage-to-recurrence converters (VFC). These gadgets are outlined in such a route, to the point that they are direct over an extensive variety of information voltages.

VCO Modeling is not related with the adequacy or shape "sine wave, triangle wave, sawtooth" yet rather on its prompt stage. Subsequently the fundamental point is not on the time-space flag. Asin (ωt+θ0) but rather typically on the contention of sine capacity. Consequently, demonstrating is generally done in the stage space.

The momentary recurrence of a "VCO" has a straight usefulness with a prompt control voltage. The yield period of an oscillator is characterized as the necessary of the prompt recurrence.

$$f(t) = f_0 + K_0 \cdot \ v_{\text{in}}(t)$$

$$\theta(t) = \int_{-\infty}^{t} f(\tau)\, d\tau$$

1. $f(t)$: - the instantaneous frequency of the 'VCO' at time *t*.
2. f_0 : - the quiescent frequency of the 'VCO'.
3. K_0:-is defined as the oscillator sensitivity, or gain. Its units is hertz per volt.
4. $f(t)$: - dependent on phase i.e. the 'VCO' frequency.
5. $\theta(t)$ The frequency of VCO depends on'VCO' output phase.
6. $v_{\text{in}}(t)$ The time-dependent control input or tuning voltage of 'VCO'.

For analyzing a control system, the Laplace transforms of the above signals are used in further analysis as shown below :-

$$F(s) = K_0 \cdot \ V_{\text{in}}(s)$$

$$\Theta(s) = \frac{F(s)}{s}$$

CHAPTER-3

Views about recent inventions of VCO's in nano-scale

The fast advancement of the CMOS innovation has made conceivable the improvement of littler correspondence frameworks with expanding usefulness. Yet, as CMOS innovation approaches the Nano-scale, critical deviations in the framework execution may be found because of either interconnect or gadget between and intra-kick the bucket parameter varieties. For the most part, in Nano-CMOS innovation, blemishes in simple and computerized circuits are ordinarily alluded as process' parameter variability. The requirement for executing ease, completely incorporated RF remote handsets has spurred the broad utilization CMOS innovation. Nonetheless, in the specific case for voltage controlled oscillators (VCO) where steadily stringent particulars regarding stage commotion must be accomplished, the configuration of the on-chip LC tank is a testing undertaking, where completely playing point of the real advances qualities must be pushed to about its points of confinement. To overcome stage commotion impediments emerging from the low quality element of incorporated inductors, advancement outline strategies are generally utilized. Low power CMOS and LC Tank VCOs are demonstrated. Their basic and symmetric structure can give low power advertisement low clamor operation. The proposed VCOs can have distinctive focus frequencies.

The most recent decade of this century has seen a dangerous development in the correspondences business. Individuals need to be associated all the time utilizing remote specialized gadgets. What's more, the interest for high transmission capacity correspondence channels has blasted with the appearance of the web. On account of the high thickness accessible on coordinated circuits, modern advanced adjustment plans can be utilized to augment the limit of these channels. This has changed the outline of remote and wireline handsets. We concentrate on the outline of a discriminating sub-hinder: the voltage controlled oscillator (VCO). We survey the prerequisites for VCOs and assess the points of interest and detriments of VCO reconciliation.

Fully monolithic Phase Locked Loops (PLL) in CMOS have been widely used many applications. Since the power consumption of the PLL mostly comes from the on-chip VCO, the demand of a low power CMOS VCO becomes high as the operating frequency increases.

Therefore, the outline of analog RF gadgets gets to be additionally difficult, as late advancements convey two noteworthy difficulties: firstly, because of the decrease of the oxide thickness, parasitic capacitances increment; furthermore, littler yield resistances are acquired, implemented by short channel-impacts. In this way, the test of simple RF configuration undertaking these days is to outline a circuit to meet the obliged specifications, at low supply voltage, (for low power utilization) and indicating low stage clamor, disregarding the way that transistors have more parasitic impacts and less inherent addition. In addition, the requirement for executing completely incorporated circuits renders imperious the configuration of uninvolved gadgets where the innovation attributes are pushed as far as possible.

CHAPTER-3

LITERATURE SURVEY

A -94 dBc/Hz@100 kHz, fully-integrated, 5-GHz, CMOS VCO with 20% tuning range for applications in Bluetooth.	A 5-GHz, fully monolithic voltage-controlled oscillator (VCO) for Bluetooth wireless transceivers is demonstrated in a 0.25 μm CMOS technology using accumulation mode varactors and spiral inductors. An 18% tuning range was measured for only 2.5 V tuning-voltage variation. The phase noise was -94 dBc/Hz at 100 kHz frequency offset with 40 kHz 1/f corner frequency.
60 GHz VCO with wideband tuning range fabricated on VLSI ,SOI, CMOS technology	A 60 GHz cross-coupled differential LC CMOS VCO is introduced in this paper, which is enhanced for an extensive recurrence tuning extent utilizing ordinary MOSFET varactors. The MMIC is manufactured on advanced 90 nm SOI innovation and obliges a circuit region of under 0.1 mm2 including the 50 Ω yield cushions. Inside a recurrence control range from 52.3 GHz to 60.6 GHz, a supply voltage of 1.5 V and a supply current of 15 mA.
A fully integrated spiral-LC CMOS VCO set with prescaler for GSM and DCS-2100 systems	An arrangement of two VCOs is produced in a 0.4 μm CMOS procedure, utilizing a completely incorporated winding inductor with symmetrical octagonal shape in the reverberation LC-tank. One VCO works at a 900 MHz focus recurrence, and the other at 1.8 GHz, both accomplishing the obliged stage commotion spec and tuning extent for the GSM and DCS-1800 framework. The stage commotion breaks even with -108 dBc/Hz at 100 kHz balance for the 900 MHz form and -113 dBc/Hz at 200 kHz for the 1.8 GHz rendition. The force utilization is 9 and 11 mW. An eight-modulus prescaler works together with both VCO.
A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator	A low voltage multiband all-pMOS VCO was created in a 0.18-μm CMOS process. By utilizing a mix of inductor and capacitor exchanging, four band (2.4, 2.5, 4.7, and 5 GHz) operation was acknowledged utilizing a solitary VCO. The VCO with a 1-V power supply has stage clamors at 1-MHz counterbalance from a 4.7-GHz bearer of -126 dBc/Hz and -134 dBc/Hz from a 2.4-GHz transporter. The VCO devours 4.6 mW at 2.4 and 2.5 GHz, and 6 mW at 4.7 and 5 GHz, separately. At 4.7 GHz, the VCO additionally attains to -80 dBc/Hz stage clamor at 10-kHz balance with 2 mW power utilization.

CHAPTER-4

PROBLEM STATEMENT

Outlining a Nano scale VCO utilizing CMOS innovation and watching its execution

Qualities as for that utilized with mass transistors. Explanations behind running with Nano scale CMOS:

The MOSFET is utilized as a part of computerized reciprocal metal–oxide–semiconductor (CMOS) rationale, which utilizes p- and n-channel MOSFETs as building pieces. Overheating is a real concern in coordinated circuits following always transistors are pressed into ever littler chips. CMOS rationale lessens power utilization on the grounds that no present streams (in a perfect world), and accordingly no force is devoured, aside from when the inputs to rationale doors are being exchanged. CMOS achieves this present decrease by supplementing each n-MOSFET with a p-MOSFET and associating both doors and both depletes together. A high voltage on the entryways will bring about the nMOSFET to lead and the p-MOSFET not to direct and a low voltage on the doors causes the opposite. Amid the exchanging time as the voltage goes starting with one state then onto the next, both MOSFETs will lead quickly. This course of action extraordinarily decreases power utilization and warmth era. Computerized and simple CMOS applications are depicted further.

SCALING OF MOSFET:

Over the earlier decades, the MOSFET has unendingly been scaled down in size; regular MOSFET channel lengths were beforehand a couple of micrometers, however current facilitated circuits are intertwining MOSFETs with channel lengths of numerous nanometers. Robert Dennard's work on scaling theory was vital in seeing that this consistent diminishment was possible. Intel began era of a philosophy including a 32 nm highlight size (with the channel being much shorter) in late 2009. The semiconductor business takes care of a "guide", the ITRS, which sets the pace for MOSFET change. Irrefutably, the issues with lessening the measure of the MOSFET have been joined with the semiconductor contraption assembling handle, the need to use low voltages, and with poorer electrical execution obliging circuit overhaul and improvement (little MOSFETs show higher spillage streams, and lower yield resistance, discussed underneath).

Designing an oscillator is based on the principle of the negative "trans-conductance" (-Gm) in an oscillator presented. A cross-coupled CMOS design was chosen as preferred to other owing to its low phase noise performance. The primary objective in the design of the oscillator is to size (design) the active devices to reduce the losses associated with the tank's "parallel resistance", Rp. The losses present in the inductor of tank (L = 8.41 nH) and capacitance of tank (C = 2.4 pF) can be represented by the "parallel resistance", Rp = 231 Ω 'obtained from inductor and varactor' design simulations.

The CMOS devices are scaled/sized, i.e., the W/L ratio of the nMOS (M1, M2) and pMOS (M3, M4) devices making the '-Gm' (negative trans-conductance) core are calculated using the relations.

The gate length was scaled down to the minimum dimension size of 1.6 μm as supported by the simulation in T-Spice. This resulting 'W/L' values of inductor and capacitor include: (W/ L) 481 μ 1.5 μ and (W L) 1481 μ 1.5 μ respectively. A current controlled device is added to the VCO circuit to have a greater/smoother control over the oscillator's output voltage swing.

$$G_{mn} = \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{th})$$

$$G_{mp} = \mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{th})$$

The gate length was scaled down to the minimum dimension size of 1.6 μm as supported by the simulation in T-Spice. This resulting 'W/L' values of inductor and capacitor include: (W/ L) 481 μ 1.5 μ and (W L) 1481 μ 1.5 μ respectively. A current controlled device is added to the VCO circuit to have a greater/smoother control over the oscillator's output voltage swing.

CHAPTER-5

EXPERIMENTATION

5.1 A low power CMOS VCO is presented

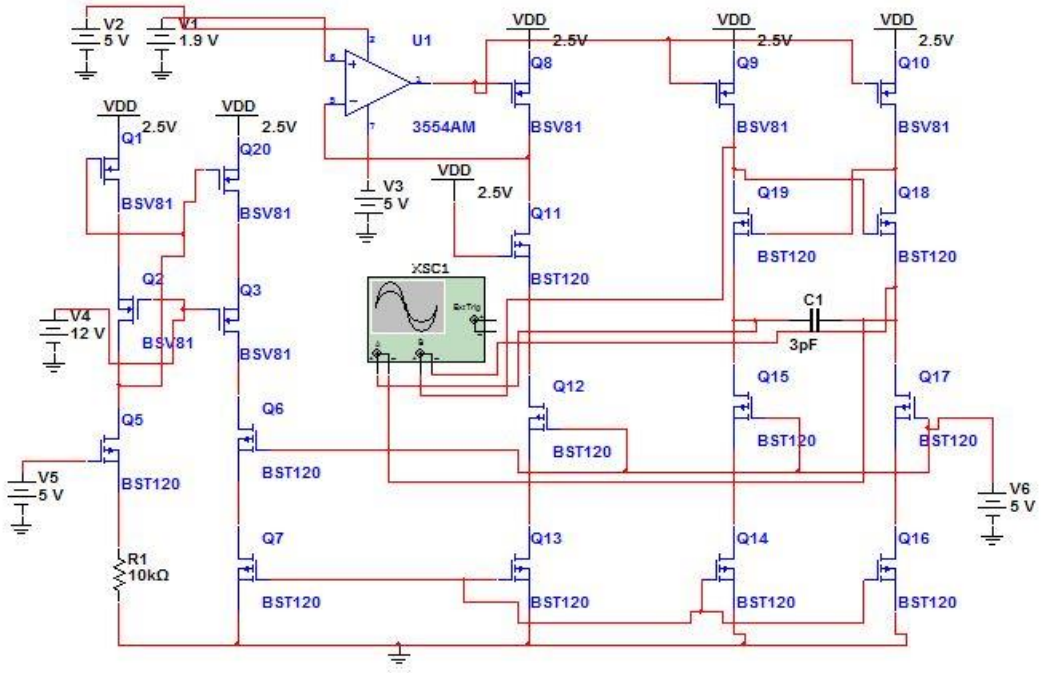


Figure 4 : VCO part 1

Output Waveform :

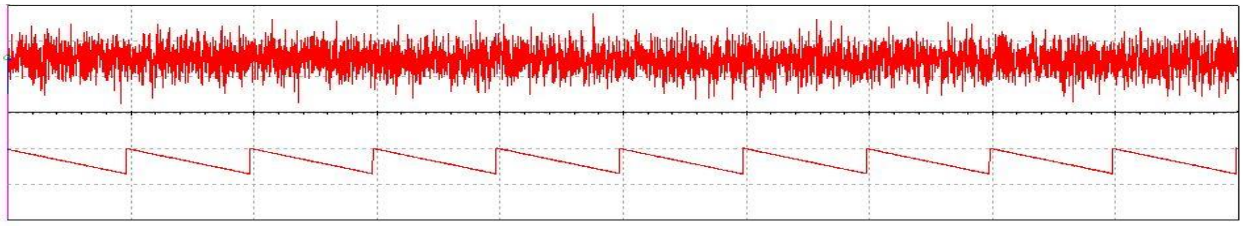


Figure 5 output waveform

Effect of change of capacitance:

Capacitance Value	Output frequency
2Pf	195MHz
3Pf	203.4MHz
5Pf	207.3MHz

5.2 LC Tank VCO

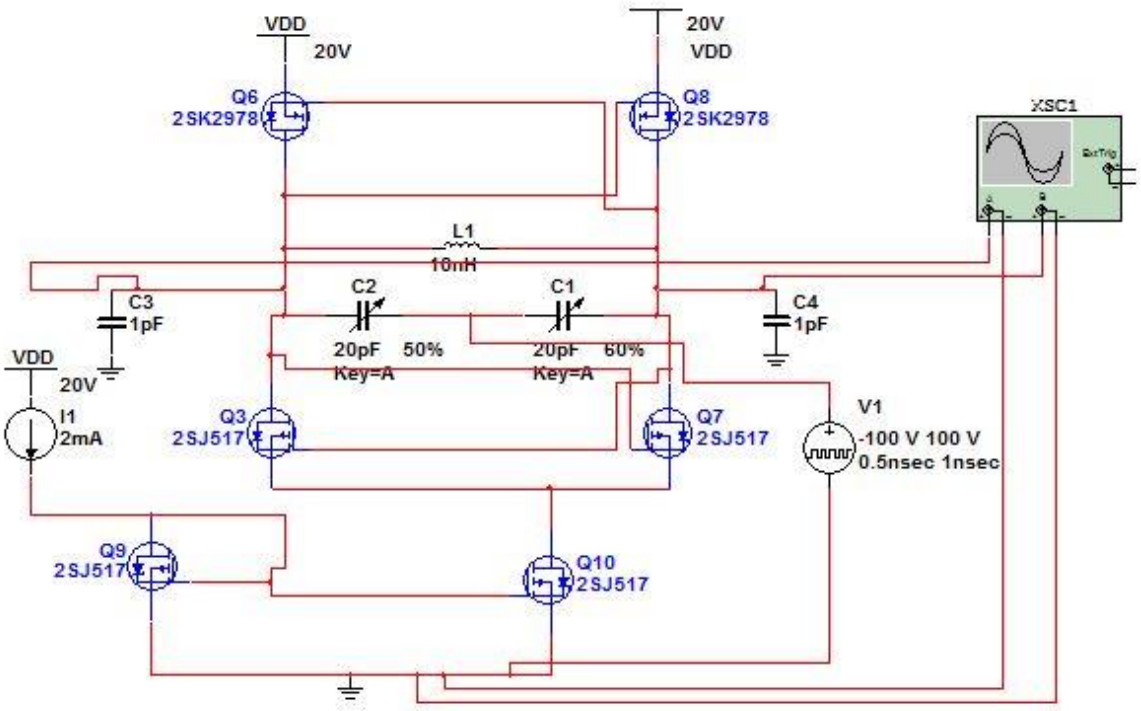


Figure 6: VCO part II

Output Waveform:

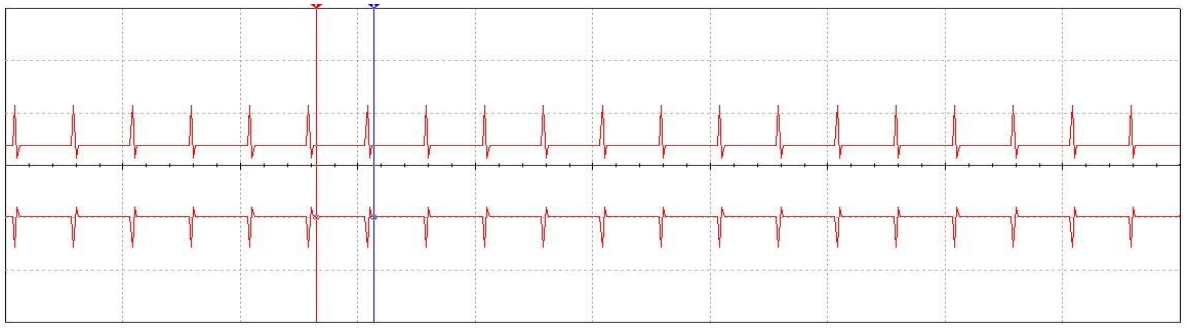


Figure 7: output signal

5.3 LC tank VCO design 2.

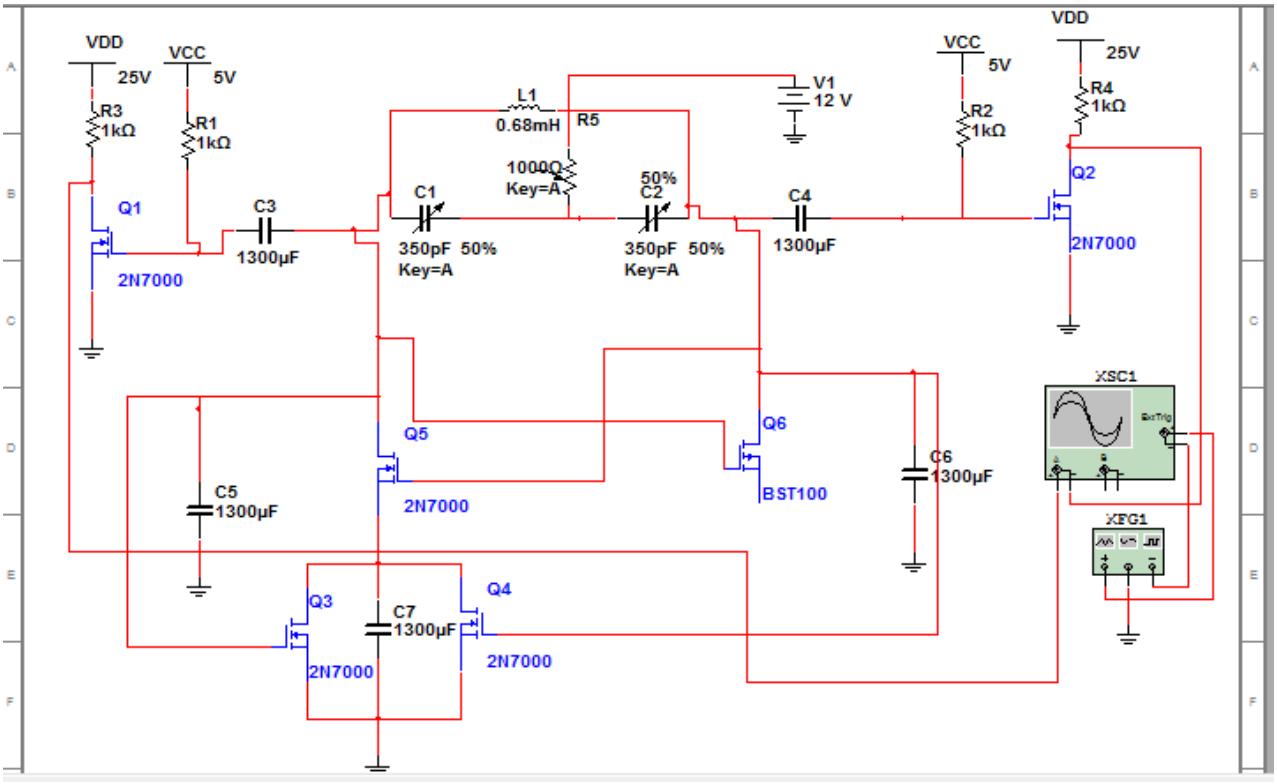


Figure 8: VCO part III

Output waveform:

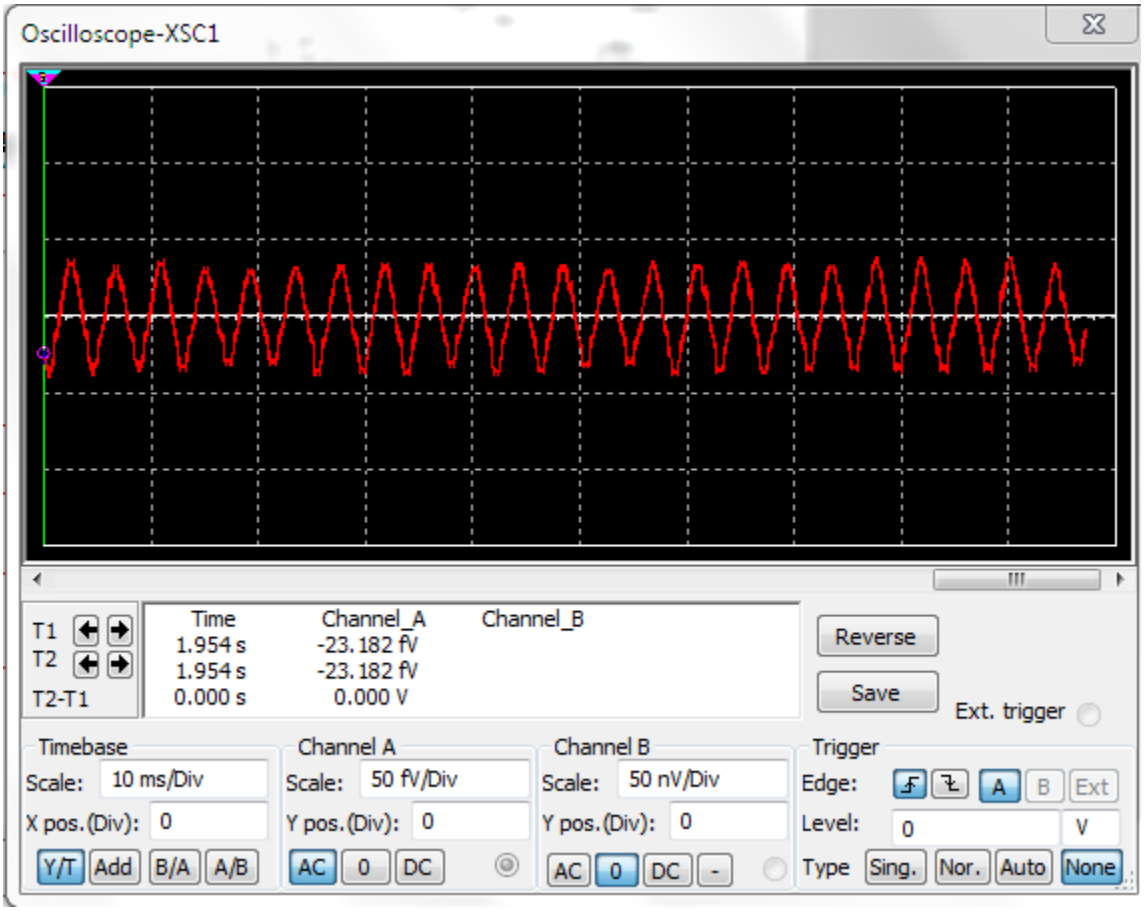


Figure 9: o/p in oscilloscope

Losses vs time graph:

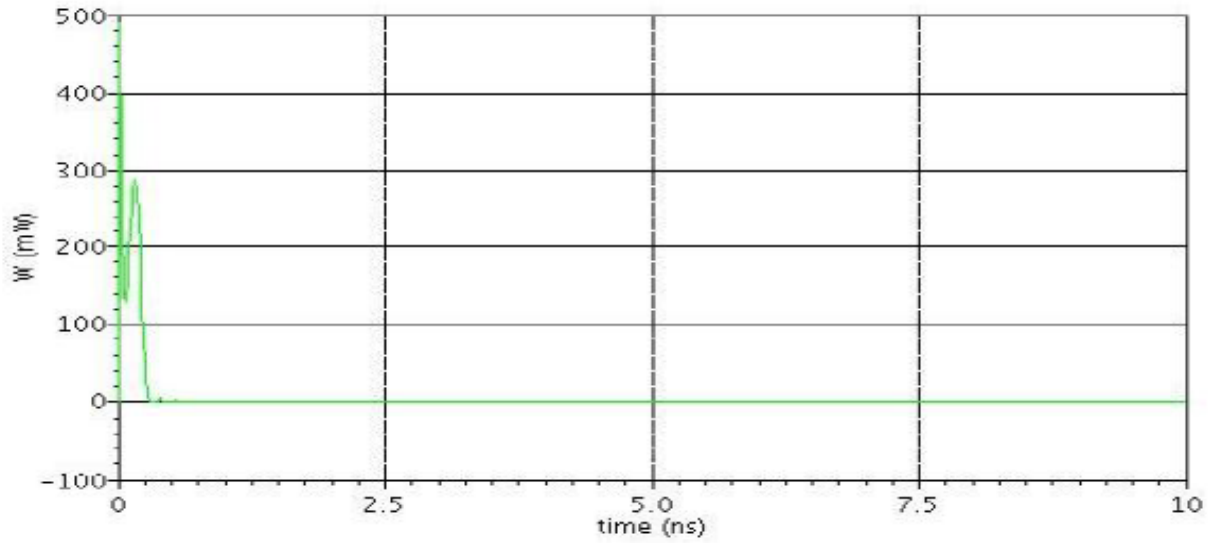


Figure 10: Losses vs time graph

Simulation of CMOS Inverter using P-Spice

The inverter circuit was also simulated using P-Spice and the MOSFET used were BSH107 (N-channel enhancement MOSFET) and BSH201 (P-channel enhancement MOSFET). In this simulation, we have observed the frequency of operation, time delay and also calculated the power dissipation of the MOSFET during the work.

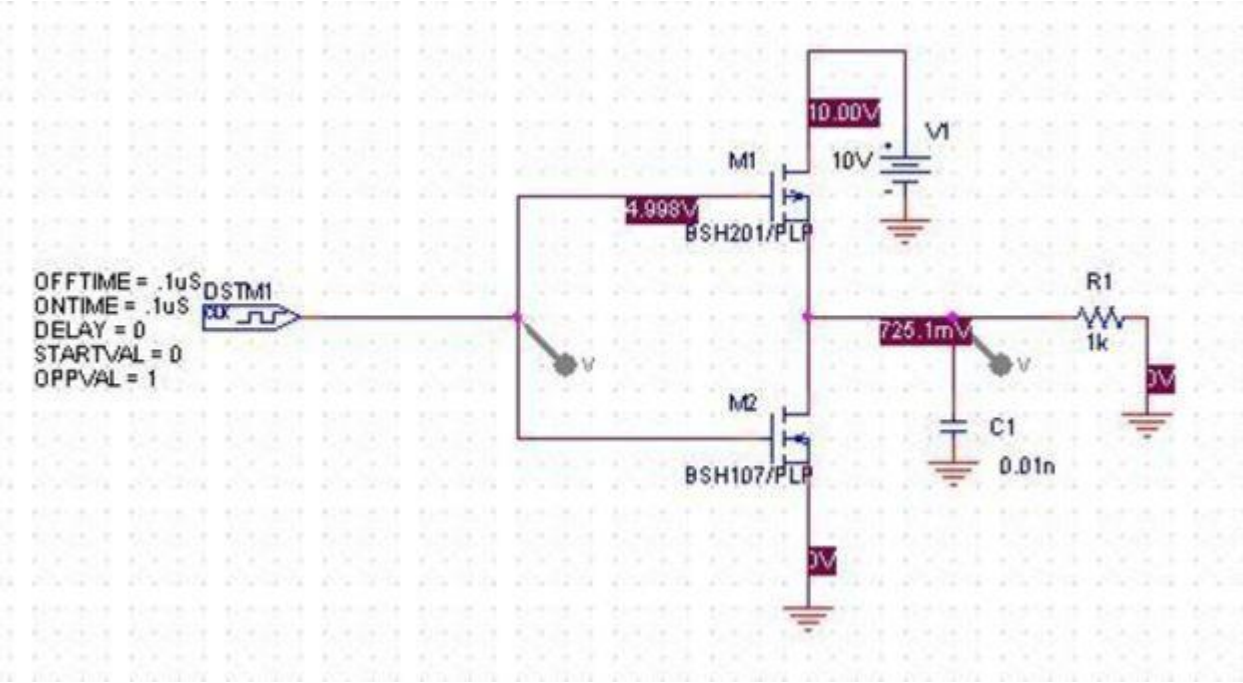


Figure 11: Inverter circuit

Output Waveform

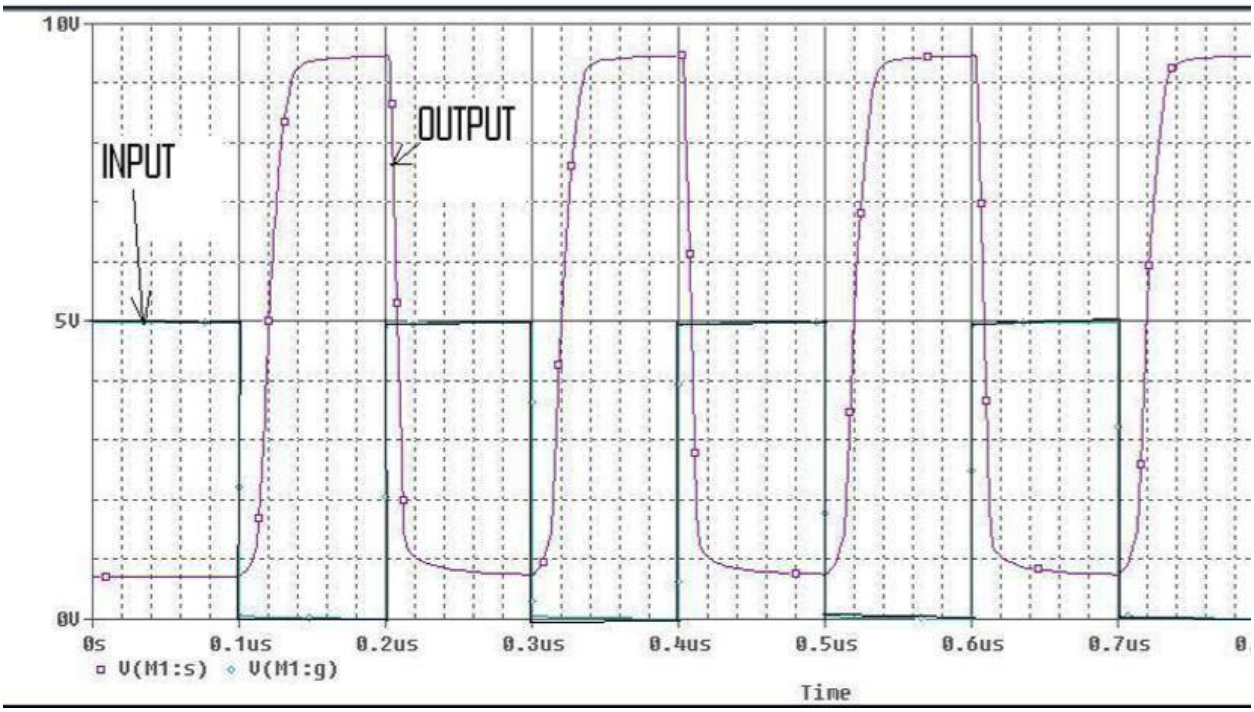


Figure 12: o.p waveform

Calculation: -

A standard MOSFET has a Width of 25 µm and Length of 16 µm. Frequency from the graph,

Hence,

Time Delay= 0.02 µs,

Frequency=5 MHz,

Vdd=10 V, Internal capacitance = 15pF

Power = $f*C*(Vdd)^2$

Applying the formula, we get Power Dissipation= **7.5mW**

Simulation of Nano-CMOS Inverter Logic Circuit using T-Spice

Program Code for Simulation of T-Spice:

```
.probe
.option probev

.option probei

.include "ml2_122.md"

m1n out in Gnd Gnd nmos L=5n W=10n

m1p out in Vdd Vdd pmos L=5n W=20n

c2 out Gnd 0.0000001F

vin in Gnd pwl (0ns 0V 100ns 0V 105ns 4V 200ns 4V 205ns 0V 300ns 0V 305ns 4V 400ns 4V
405ns 0V 500ns 0V 505ns 4V 600ns 4V)

vdd Vdd Gnd 3

.print tran v (in) v (out)

.tran 1n 600n
.end
```

Experimental values for MOS physical dimensions:

(NMOS L=40 nm W=60 nm),(PMOS L=40 nm W=80 µm)

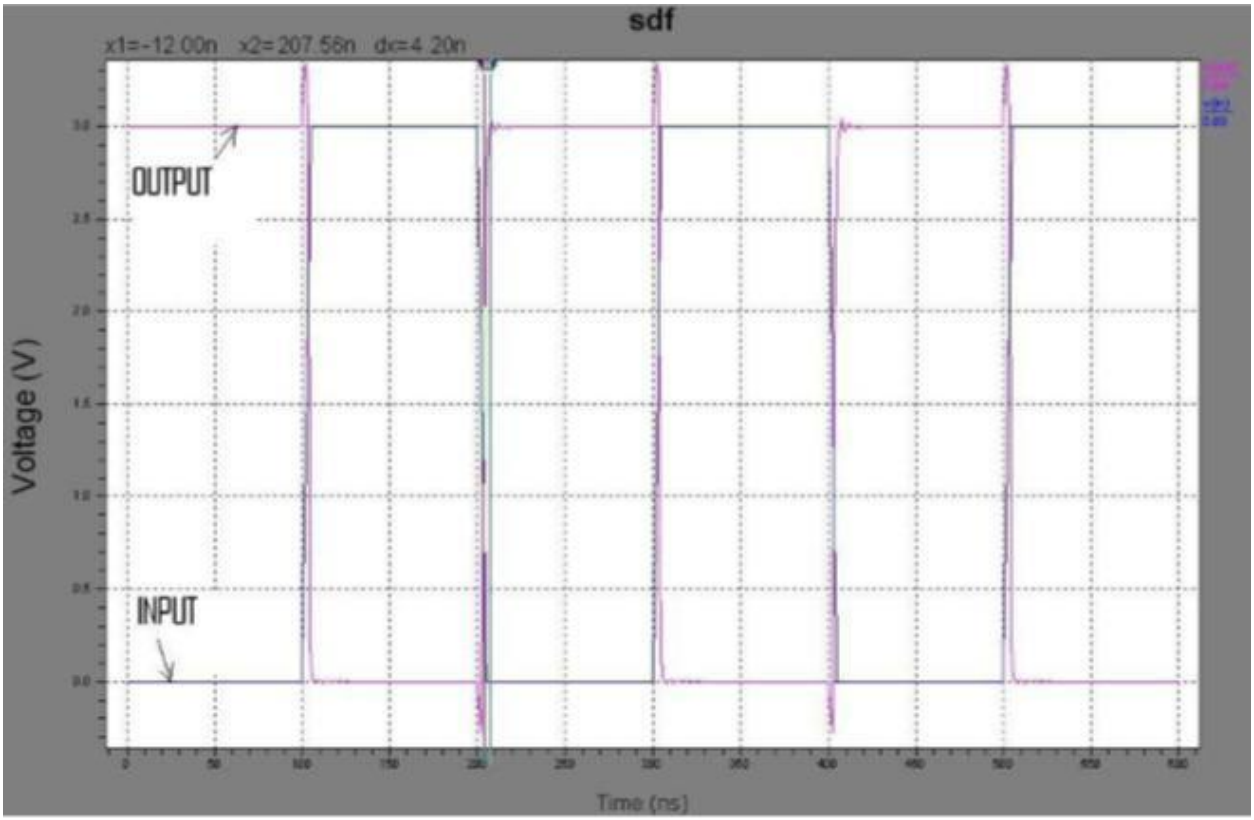


Figure 13: output waveform

Calculation:

T-Spice is reenactment programming, which gives flexibility to differ the physical parameters of any gadget. Through which we can fluctuate the physical parameters of MOSFET like Length, Width, Internal Capacitance, and so on. We lessen the length and width of the MOSFET taking the eq. beneath into thought.

And accordingly change the internal capacitance changes according to equation

Cgs=Cgd=0.5W*L*Cox ,

Where

W=Width of MOSFET,

L=Length of MOSFET,

tox=2nm, Cox= Capacitance per unit gate area.
Cox=εox/tox,

εox=3.9εo=3.45x10-11 F/m (εo=8.854x10^{-12} F/m)

Frequency obtained from the graph. The input frequency of clock is considered.

= 10 MHz

Taking W=60 nm, L=40 nm, Frequency= 10 MHz, Vdd=10 V,

We get C=18.84 x 10-18 F

$P=C*f*[(Vdd)]^2$

And calculating power $(VDD)^2$

Hence Power Dissipation= 18.84 x 10-9 W.

Propagation delay measured from the graph=4.2 ns.

Chapter 6

RESULTS/DISCUSSION

The initial two reenactment issues us a thought regarding the working of a VCO. The waveform demonstrates high stage clamor yet the settling time for the waveform is less.

It experiences damping and after that settles at a consistent voltage swing < Vdd.

The development of nano scale CMOS permits us to strive for the incorporated IC's for VLSI and ULSI outline.

As what's to come is advancing, the measure of transistors needed for a specific space is additionally multiplying at a pacing rate of at regular intervals, power utilization every unit range is likewise rising hugely.

Our next target is the creation of the configuration and for the present outline we have to reconstruct it utilizing CMOS based IC’s.

The dynamic scaling of CMOS innovation towards nanometer sizes has made conceivable the execution of completely coordinated frameworks for the remote correspondence applications. As aftereffect of the advancement in innovation improvement and the utilization of profound submicron CMOS forms, computerized circuits have gotten to be quicker, more exact, and with diminished of the usage region.

6.1 Comparison between traditional CMOS and nano-CMOS

Parameter	**CMOS**	**Nano-CMOS**
Vdd	9.81 V	9.81 V
Capacitance	13 Pf	8.3pF
Frequency	5 GHz	10 GHz
Power Dissipated	7.5 mW	0.83 μW
Width	25 μm	59 nm
Length	16 μm	38 nm
Time delay	0.02 μs	400 ns

Chapter 7

CONCLUSION

Every electronic devices being made now pronounce the use of low cost and small size transistor models for which CMOS makes an essential combination and if the size is in nano-scale ,then it is more justifiable and efficient as we are reducing the size of the whole board space. Single chip Si-based radio frequency electronic models are one of the most attractive and efficient of the innovations emerging in the wireless communication ranges. However the quality factor of the integrated circuits are still performance limiting criteria for every Si – based radio implementations. The quality factor of the LC-VCO tank has a significant influence on the performance, phase noise and power consumption of the *VCO*. The work in this thesis is based on reducing phase noise and tuning performance at the oscillation frequency of 1.1 GHz by optimizing the design characteristics. The optimization process of the LC-tank was done through a high quality inductor's perspective. But the inductor's quality factor continues to be the performance degradation, it will be justifiable and essentially beneficial to channel efforts that will help in improving the varactor tuning range in the presence of fixed parasitic capacitances. The absence of a library files to simulate phase noise in P-Spice is notably a short coming in itself. The impact of scaling of mosfets on phase noise will be an interesting innovative task. The device should scale down its integrated circuit transistors of the minimum dimension to 0.25μm or 0.18 μm, and efficiently by using multi-layer inductor structures brought about by an increase in frequency levels to design high quality inductors will significantly result in high performance VCOs and PLLs.

Reference

- Agere Syst., Lucent Technol., Murray HIll, NJ, USA, Custom Integrated Circuits, 2001, IEEE Conference
- Electron. Lab., Swiss Fed. Inst. of Technol., Zurich, Switzerland, Microwave Symposium Digest, 2004 IEEE MTT-S International
- ESAT, Katholieke Univ., Leuven, Heverlee, Belgium ; Steyaert, M. ; Miyakawa, H., Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997
- Zhenbiao Li ; Silicon Microwave Integrated Circuits & Syst. Res. Group, Univ. of Florida, Gainesville, FL, USA ; O, K.K., Solid-State Circuits, IEEE Journal of (Volume:40 , Issue: 6) RFIC Virtual Journal, IEEE
- Hsieh-Hung Hsieh ; Dept. of Electr. Eng., Nat. Taiwan Univ., Taipei ; Liang-Hung Lu, Microwave Theory and Techniques, IEEE Transactions on (Volume:55 , Issue: 3) RFIC Virtual Journal, IEEE
- P. Pereira, M. Helena Fino, Optimization of LC-VCO, Springer.
- M. Ventim-Neves, Springer Science+Business Media New York.