MODELLING AND ADAPTIVE CONTROL OF A DC-DC BUCK CONVERTER

A thesis submitted for the degree of

Bachelor and Master of Technology (Dual Degree)

In

Electrical Engineering

(Control and Automation)

By

Vishnu Dev

Roll No: 710EE3124

Under the Supervision of

Prof. Bidyadhar Subudhi

Department of Electrical Engineering

National Institute of Technology, Rourkela

Rourkela-769008

2015

MODELLING AND ADAPTIVE CONTROL OF A DC-DC BUCK CONVERTER

A thesis submitted for the degree of

Bachelor and Master of Technology (Dual Degree)

In

Electrical Engineering

(Control and Automation)

By

Vishnu Dev

Roll No: 710EE3124

Under the Supervision of

Prof. Bidyadhar Subudhi

Department of Electrical Engineering

National Institute of Technology, Rourkela

Rourkela-769008

2015

Department of Electrical Engineering

National Institute of Technology

Rourkela

CERTIFICATE

This is to certify that the thesis entitled "**Modelling and Adaptive Control Of a DC-DC Buck Converter**" being submitted by Vishnu Dev **(710EE3124)**, for the award of the degree of **Bachelor of Technology and Master of Technology (Dual Degree)** in **Electrical Engineering**, is a bonafide research work carried out by him in the Department of Electrical Engineering, National Institute of Technology, Rourkela under my supervision and guidance

The research reports and the results embodied in this thesis have not been submitted in parts or full to any other University or Institute for award of any other degree.

Prof. Bidyadhar Subudhi
Department of Electrical Engineering
NIT Rourkela, Odisha

Date:
Place: Rourkela

ABSTRACT

With the advancement of electronic industry the requirement of low power supply is essential as numerous industrial and commercial devices rely on power converters for regulated and reliable DC power source. The demands of DC-DC converters are increasing exponentially because of their high efficiency, small size as well as simple architecture. The complexity in modelling of DC –DC converter mainly depends on its usage and its sophistication as it ranges from simple analogue design for low cost application to digital and self-adaptive model for better performance. This paper comprises of method for obtaining the small signal model of DC-DC buck converter by linearizing it using state space averaging technique. Both state space as well as non- linear model of Buck converter is the simulated in MATLAB and desired response is observed. This paper also discuss the methods of design and implementation of controller for Buck converter .The purpose of the compensation is to modify the dynamic characteristics of the converter in order to satisfy the performance specifications of the Buck converter. The performance specifications of the converter are maximum peak overshoot, settling time and steady state requirements and should be stated precisely so that the optimal control of the converter can be obtained. In this research we are interested in two approaches that are commonly used in the digitally controlled design of buck converter, the pole-zero matching approach, which provides a simple discrete time difference equation, and the systematic pole placement method. This thesis also focuses on a new alternative adaptive schemes that do not depend entirely on estimating the plant parameters is embedded with LMS algorithm. The proposed technique is based on a simple adaptive filter method and uses a one-tap finite impulse response (FIR) prediction error filter (PEF). Simulation results clearly show the LMS technique can be optimized to achieve comparable performance to classic algorithms. However, it is computationally superior; thus making it an ideal candidate technique for low cost microprocessor based applications

ACKNOWLEDGEMENT

First of all I like to thanks from deep of my heart to my supervisors Prof. Bidyadhar Subudhi for the confidence that they accorded to me by accepting to supervise this thesis. I express my warm Gratitude for their precious support, valuable guidance and consistent encouragement throughout The course of my M. Tech. My heartiest thanks to Prof. Sandip Ghosh, an inspiring faculty and Prof. A. K. Panda, Head of Dept. of Electrical Engineering Department, NIT, Rourkela.
Special thanks to Sarada, Aakash, Nilkanth , Sumit for their support, care and love. I would like to extend special gratitude to my friends in NIT Rourkela, without whom, this journey would not have been this enjoyable.
Finally, I dedicate this thesis to my family: my dear father, my dearest mother and my brother who supported me morally despite the distance that separates us. I thank them from the bottom of my heart for their motivation, inspiration, love they always give me. Without their support Nothing would have been possible. I am greatly indebted to them for everything that I am.

TABLE OF CONTENT

LIST OF FIGURES

LIST OF SYMBOLS

μ	Step size
C	capacitor
d(n)	Control signal
e_P	Prediction error
f_o	Corner frequency
f_s	Sampling frequency
i_L	Inductor current
i_o	Load current
K_D	Derivative gain
K_I	Internal gain
K_P	Proportional gain
L	Inductor
M_P	Maximum overshoot
Q	Quality factor
t_r	Time rise
T_{sw}	Switching time
v_C	Capacitor voltage
V_{in}	Input voltage
v_L	Inductor voltage
v_o	Output voltage
V_{ref}	Reference voltage
$\widehat{W}$	Estimated filter weight
$\hat{v}$	Estimated output
θ	Parameters vector

Chapter 1

INTRODUCTION

1.1 Introduction

In power system accurate and precise power regulation is a desirable factor , It is needed to solve the problem of time varying parameters such as component tolerance , unpredictable load changes, effect due to aging of components, changes in ambient conditions , unexpected external disturbance and improper knowledge of load characteristic . For the design and control of DC-DC converters, the use of digital controllers have been increased tremendously, as it helps us several ways to improve the performance and dynamic characteristics of DC-DC converter. In comparison to the analog controllers digital controllers are flexible design and require less passive component thus reducing the size and cost of design. Unlike analog controllers digital controllers are less sensitive toward system parameter variation as well as external disturbances. It is easy to change or modify the control algorithms in digital controllers as well as advance control algorithms such as adaptive control, non-linear control and system identification algorithms can be implements easily.

For the closed loop control design of DC-DC converter mainly two control structure can be applied namely current mode control and voltage mod control. Since an additional signal conditioning circuit having high speed current sensor is required in current control mode it makes the system costly. Hence the digital voltage preferred as it is easier and simple to design. The digital PID controller is commonly used in control loop design of converters. This is because the PID control parameters are easy to tune and the designed controller is easy to implement.

In this thesis buck converter is chosen for modelling and design .The control method chosen to maintain the output voltage from the buck converter was PID controller. For tuning the gains of PID controller many topologies can be implemented like pole zero cancellation, pole placement etc. Pole placement as well as pole zero cancellation technique compares the actual output voltage with the reference voltage. The difference between both voltages will drive the control element to adjust the output voltage to the fixed reference voltage level. The classical PID controller having fix gain do not give satisfactory result due to uncertain parameters and load variation hence, there

is need arises of self- tuning or adaptive controller which can be reliable and give accurate response. Adaptive digital controllers offer a robust control solution and can rapidly adjust to system parameter variations.

1.2 Motivation

With the growing need of electronic industries, the need of accurate and having less ripples is also increasing tremendously. In current era, where fast processing micro-controllers are taking the place of analogue parts the need of describing the system became inevitable. In practical implementation there are many uncertain parameters which needs to be taken care of hence advance control technique are required. The switched-mode DC-DC converters are most widely used power electronic circuit because of its high conversion efficiency and performance. These are non-linear and variable structures whose structure change with time due to switching action.

1.3 Objective of thesis

The present thesis is focused on following objectives:-

- To develop the mathematical model of dc-dc buck converter
- To design small signal model of buck converter using state space averaging
- To study the response of open loop buck converter using MATLAB.
- To design the PID controller based on pole zero cancellation using FIR filter.
- To use pole placement approach to get the desired tuning gains of PID controller using IIR filter.
- To design an adaptive controller for buck converter based on one tap LMS predictor error filter.
- To simulate and compare the dynamics of all the above mentioned controllers using MATLAB.

1.4 Layout of the Thesis

This thesis is divided into mainly 6 chapters which is as follows:

Chapter 2 is literature review and the previous work done by other authors in the field of power converter design modelling and control is discussed. This chapter gives a brief information about

how the technological advancement has led to the growth of power converters from analog age to the age of microprocessor with in implementation of advanced adaptive algorithms.

Chapter 3 focuses on the design and modelling of buck converter. In this chapter the working and operation of buck converter is discussed as well as mathematical model along with state space structure of buck converter is obtained. The non – linear model of the converter is converted into small signal linear model by using state space averaging technique. The discrete model of buck converter is also obtained in this chapter.

Chapter 4 presents the digital control architecture of the DC-Dc buck converter .In this chapter the digital voltage mode control is achieved by using the PID controller.

The PID controller used here are based on two topologies to tune its gain first pole zero cancellation technique and the other is pole placement method.

Chapter 5 discusses an adaptive controller to minimize the error and give required voltage regulation. In this chapter a one tap FIR predictor error filter is realized based on LMS adaptive algorithm. The detailed discussion is done on linear predictors and predictor error filter along with the derivation of various search algorithms. At last the LMS algorithm is derived and result and simulations were obtained to show its effectiveness.

In chapter 6 conclusions are drawn from the work done and throw some light of the future scope of the research topic.

Chapter 2

LITERATURE REVIEW ON ADAPTIVE CONTROL OF DC-DC BUCK CONVERTER

The flexible operation and control of DC-DC converters have been key interest of the researchers from last decades. With the emerging sophisticated technology in power electronics, different problems were encountered on the pathway. There are numerous novel methods for the modelling and design as well as control schemes for DC-DC converter are available in literature. In last few decades with the evolution of microprocessors much emphasis is being given on the discretization of system as it reduces the complexity and increases the speed of operation of the controllers. Recently lots of research work was specified on self - tuning control methods for DC-DC converter applications in order to deal with the varying parameter and sudden load change adaptively.

In [12] the state-space averaged technique is used to develop the state space averaged small-signal model of the Buck DC-DC converter. In order to get good voltage regulation based on voltage mode control he designed the digital self-tuning PID controllers centered on recursive least-squares estimation algorithm. In order to see the response of both the converters under varying load or input voltage a comparative study was done in between the two self-adapting controllers. It is found that the first digital self-tuning PID controller gives the better performance and is more robust for model inaccuracies and disturbances in comparison with the other PID controller.
These self-tuning and adaptive control techniques are most effective during the steady-state and the parameters are tuned using pre-determined rules, such as phase margin and gain margin requirements [2]. Therefore, these categories of controller are generally unsuitable for time varying systems where on-line compensation is desirable.

In the field of adaptive control, model reference of adaptive control has drawn considerable attention, has been applied in [31]. This work is mainly centered on minimizing the error between the output voltage of the system and that of the reference model output and make it converge to zero. In this thesis it is shown that s the Buck-Boost converter has one zero in right half of s plane and hence is a non-minimum phase system. The author has focused on designing an adaptive

MRAC controller for the system based recursive least square method for the estimation of uncertain parameters of the Pole placement controller.

A digital control scheme using state feedback is proposed by the author in[5]. Three different algorithms were established centered on the state feedback control along with the combination of PID controller as well as decomposed fuzzy PID controller. The overshoot and steady state error is significantly decreased by the state controller as suggested by the author which in return improves the performance of the converter. However this approach does not deal with the state estimation for checking the robustness of the state feedback control and does not verify the dynamic performance of the converter.

In [18], the author has designed a digital control algorithm based on small signal model of buck converter. The designed controller is able to explicitly specify the preferred output voltage and transient response for a buck converter in voltage mode control. This algorithms is realized to minimize the error between the output voltage and required response. A zero steady-state error in the output voltage can be accomplished with the help of further dynamics to help the controller in order to follow the load variation and adapt the reference voltage according to changed load. The pole placement controller using state feedback is realized in order to find the weights of the adaptive algorithm.

In [9] focuses on the realization of an adaptive control for DC-DC Converter Operating in continuous conduction mode .In this paper the author have discussed the Buck-Boost converter with parasitic and varying load .The nonlinear structure of the system is converted into linear system by using state space averaging which is used for the on-line identification of the converter parameters. The pole placement controller is implemented here for the control structure and the uncertain parameters are estimated by using RLS adaptive filter.

An inventive, topology for online system identification is discussed in [4]. Author has paid attention on estimating the parameters of pulse width modulated dc–dc power converters. The suggested method can be implemented for different applications where effective and precise estimation of parameter is mandatory. The proposed technique which is based on DCD algorithm is computationally efficient and uses an IIR adaptive filter as the plant model. The system identification technique decreases the computational difficulty of existing RLS algorithms. Importantly, the proposed method is also capable of recognizing the parameters rapidly and precisely.

In [10] the author proposed a control technique which cancel the transfer function of the converter by mean of pole zero cancellation technique. The different approaches are considered in [3] which used polynomial controller and compared its dynamics with PID and PD Controllers, A full state-space feedback digital control scheme for the voltage-mode switching power supply was developed. The control scheme is based on superimposing a small control signal to the reference value of the control variable at each switching cycle to cancel out the perturbations. The main difference between this method and the traditional saw-tooth and threshold method is that it is possible to separately specify the desired output voltage and the type of transient response that the regulator would exhibit due to perturbations or a set-point variation. Also, with the aid of additional dynamics, zero steady-state error on the output voltage can be guaranteed. The specification is done by pole assignment on a discrete-time state-variable model.
In [13] Kelly and Rinne introduced a pole placement control strategy for the design and control of buck DC–DC Converter. In order to eliminate the steady state error a feedforward component is involved in the control strategy. The value of the feedforward gain which completely eliminates steady-state error, is dependent upon the gain of the plant, which may not be known exactly. In this design the feedforward gain is determined adaptively, so as to drive the steady state error to zero.

Kelly and Rinne proposed an adaptive, self-learning, digital regulator, based on a one-tap LMS prediction error filter (PEF) for on-line system identification [13]. The presented technique is simpler than many other methods and a prior knowledge of system parameters is not required in the adaptation process. However, there appears to be two limitations to this system. Firstly, the scheme involves subjecting the system to a repetitive disturbance to excite the FIR filter and improve the convergence of filter tap-weights, which after many iterations the controller begins to learn [7]. Furthermore, in this scheme only a PD controller is considered and this can yield a non-zero steady-state error, thus a feed-forward loop should be introduced to ensure system stability and achieve regulation.

Hence, it can be seen that lots of work has been done in the area of modelling and adaptive control of buck converter.

Chapter 3

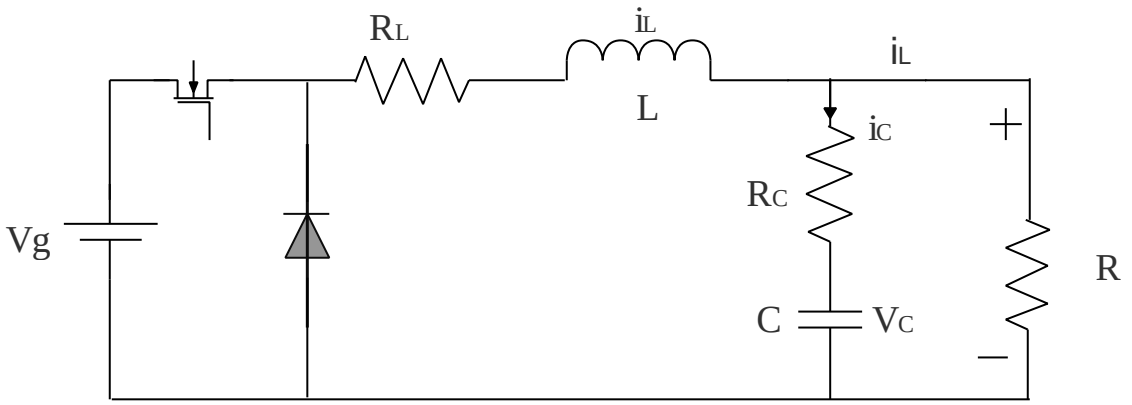
MODELLING OF DC-DC BUCK CONVERTER

3.1 Introduction

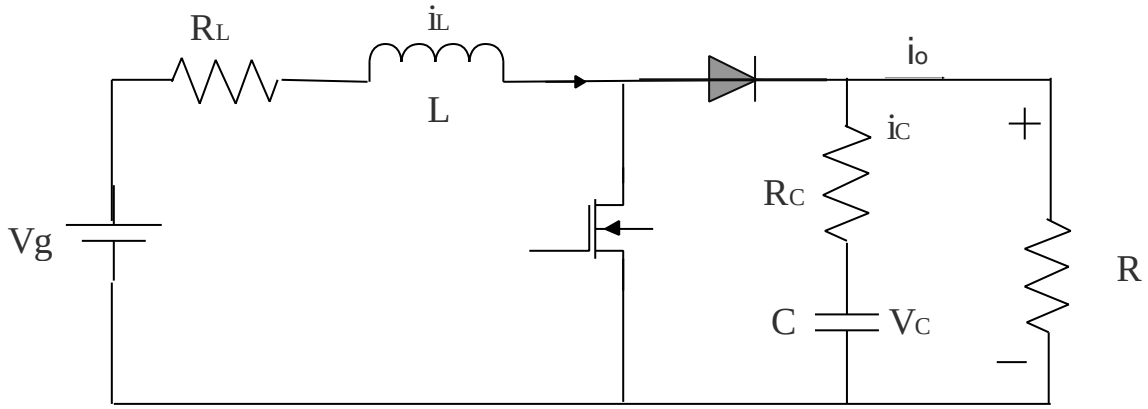
DC-DC converters are widely used in vast range of electrical and electronic systems, with changing power levels. Some examples are power supplies in Telecommunication devices, Computers/Laptops, Motor drives and Aerospace systems. Converters with a high performance voltage regulation during static and dynamic operations, high efficiency, low cost, small size/lightweight, and reliability is essential in these applications. The main role of DC-DC converters is to convert the unregulated input voltage into a different controlled level of dc output voltage. In general, a DC-DC converter can be described as an analogue power processing device that contains a number of passive components combined with semiconductor devices (diodes and electronics switches) to produce a regulated DC output voltage that has a different magnitude from the DC input voltage [18].

3.2 DC-DC Circuit Topologies

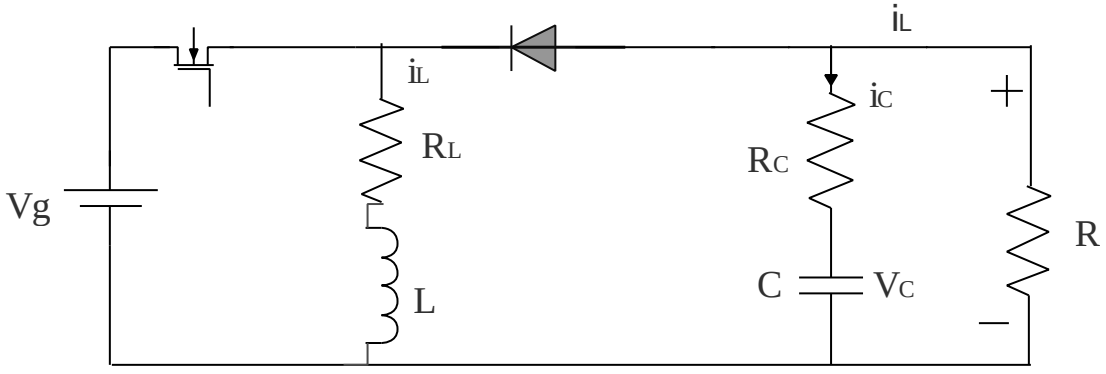
Configuration of the components of dc-dc converters in different ways leads to the formation of various power circuit structures having same types of components which include inductor *L*, capacitor *C*, load resistor R and the lossless semiconductor components like diodes and MOSFETs. The selection of the topology is mainly dependent on the desired level of regulated voltage, since the PWM DC-DC converters are applied to produce a regulated voltage in DC with different level that of the input voltage. This level can either higher or lower than given input voltage. Buck converter, Boost converter and Buck-boost converter are the most extensively used converters. A dc-dc buck converter as shown in Fig 3.1(a) is designed to generate a DC output voltage lower than the input voltage, On the other hand, a DC-DC Boost Converter (Fig 3.1(b)) is used to deliver a DC output higher than the applied input voltage. And finally the Buck – Boost converter (Fig 3.1 c) perform the task of both the Buck and Boost Converter that is it can either step down the input voltage or step up the voltage depending on its duty cycle.



(a)



(b)



(c)

Fig 3.1 Circuit diagram of a ; Buck converter, b ; Boost converter , c ; Buck-Boost converter

3.3 DC-DC Buck Converter Principle of Operation

The Buck converter is used to step down the input voltage V_{in} into a lower output voltage V_o .This can be accomplished by controlling the operation of the power switches, generally by using a PWM signal. Accordingly the states of the switch (*On*/*Off*) are changed periodically with a time period of T_{sw} (switching period) conversion ratio equal to D . The duty ratio D can be defined as the ratio of time for which the switch is in ON state i.e. Ton and total switching time take T_{sw} or it can also be defined as the ratio of output voltage to its input voltage during the steady state operation of converters. Then in order to removes the switching harmonics from the applied input signal the L-C low pass filter is implemented. A lower corner frequency is selected to provide smooth output DC voltage [18]. The corner frequency f_c should be much lower that the switching frequency f_{sw} which is defined as:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad 3.1$$

There are generally, two modes of operation in buck converter depending upon the switching period. The first mode is when the switch is ON and the diode is OFF. During this period the input voltage is delivered to the load resister directly while charging the inductor and capacitor which act as low pass filter. The second state is when the switch is OFF and the diode is ON, then the stored energy in capacitor and inductor will be discharged through the diode as the load get cuts off from the input voltage source. The operation comprising these two modes where the inductor current never falls to zero is known as continuous conduction mode or CCM. Apart from CCM there is one another mode of operation of Buck converter known as Discontinuous conduction mode or DCM .In this mode the inductor current of the converter falls to zero thus there are three states of operation in DCM, two as same as CCM and one where the inductor current remain zero as both the switch and the diode is in their OFF state during operation [19].

3.4 DC-DC Buck Converter Modelling

To design an appropriate feedback controller, it is necessary to define the model of the system. In synchronous dc-dc buck converter the free- wheel diode is replaced by another MOSFET device. Since there are two intervals per switching cycle. The switching period is defined as the sum of the on and off intervals$T_{sw} = T_{on} + T_{off}$. The ratio of the Ton interval to the switch period is known as the duty ratio or duty cycle $D = T_{on}/T_{sw}$ the output voltage can be computed in terms of duty cycle during its operation in steady state. The output voltage produced by the DC-Dc buck converter is always lower as compared with the input voltage owing to its configuration. The required out voltage is controlled by varying the on time of the witch that is Ton or by varying the duty cycle .Thus the output voltage level is controlled by the PWM signal which is used as its duty cycle [19].

$$V_o = \frac{V_{out}}{T_{sw}} V_{in} = DV_{in} \qquad 3.2$$

The differential equation of the converter in both the modes can be obtained by using KVL and KCL on the circuit shown in Fig 3.2.

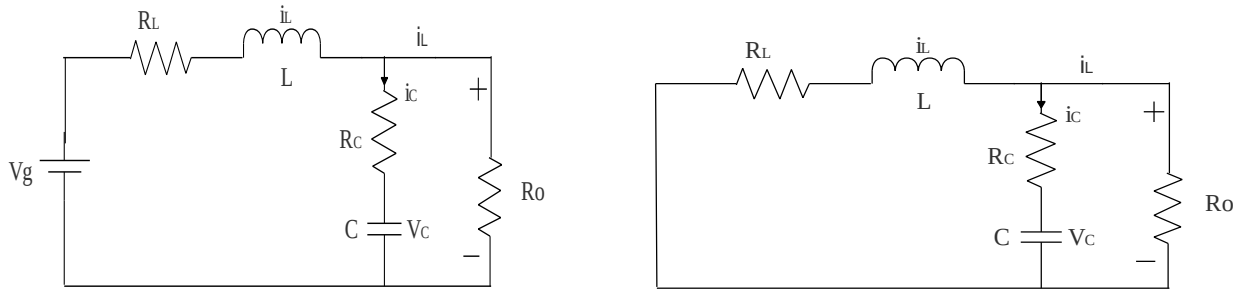


Fig 3.2 Circuit diagram of buck converter (a) when switch is ON (b) when switch is OFF

The output equations of the converter can be obtained as follows:

$$\frac{d\,i_L}{dt} = g\left(i_L, v_c\,, v_{in,}, L\,, R, C\,\right)$$

$$\frac{d\,v_c}{dt} = h\left(i_L, v_c\,, v_{in,}, L\,, R, C\,\right) \qquad 3.3$$

$$V_o\ = h\left(i_{L\,,}\,v_c\right)$$

Hence for the mode 1 when the switch is ON and diode is OFF the dynamic and output equations are as follows:

$$\frac{di_L}{dt} = \frac{V_{in}}{L} - \frac{(R_C+R_L)i_L}{L} - \frac{v_C}{L} + \frac{R_C i_o}{L} \qquad 3.4$$

$$\frac{dv_c}{dt}\ = \frac{i_L}{C}\ -\ \frac{i_o}{C} = \frac{i_L}{C} - \frac{v_o}{RC} \qquad 3.5$$

$$V_o = \ V_c + R_C(i_L - i_o) = R_C C\,\frac{dv_c}{dt} + V_c \qquad 3.6$$

On modifying the above equation and converting it in state space it can be represented in matrix form as [21]:

$$\dot{x} = A_1 x + B_1\,V_{in} \qquad 3.7$$

$$y = \ C_1 x$$

Which can be written as:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-1}{L}\left(R_2\ +\ \frac{RR_c}{R+R_c}\right) & \frac{-R}{L(R+R_c)} \\ \frac{R}{c(R+R_c)} & \frac{-1}{c(R+R_c)} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} \ \ + \begin{bmatrix} 1/L \\ 0 \end{bmatrix}\ V_{in} \qquad 3.8$$

$$V_o = \ \begin{bmatrix} \frac{RR_c}{R+R_c} & \frac{R}{R+R_c} \end{bmatrix}\ \begin{bmatrix} i_l \\ v_c \end{bmatrix} \qquad 3.9$$

Now for mode 2 applying KCL in circuit (b) of Fig 3.2 we can get the differential equation as:

$$\frac{di_L}{dt} = \frac{-1}{L}\left(R_2\ +\ \frac{RR_c}{R+R_c}\right) i_l - \frac{R}{L(R+R_c)}\,v_c \qquad 3.10$$

$$\frac{dv_c}{dt} = \frac{R}{C(R+R_c)}\,i_l - \frac{1}{C(R+R_c)}\,v_c \qquad 3.11$$

On modifying the above equation and converting it in state space it can be represented as:

$$\dot{x} = A_2 x + B_2 V_{in} \quad 3.12$$

$$y = C_2 x$$

Which can be written as:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-1}{L}\left(R_2 + \frac{RR_c}{R+R_c}\right) & \frac{-R}{L(R+R_c)} \\ \frac{R}{c(R+R_c)} & \frac{-1}{c(R+R_c)} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} \quad 3.13$$

$$V_o = \begin{bmatrix} \frac{RR_c}{R+R_c} & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} \quad 3.14$$

Hence from above equations:

$$A_1 = A_2 = \begin{bmatrix} \frac{-1}{L}\left(R_2 + \frac{RR_c}{R+R_c}\right) & \frac{-R}{L(R+R_c)} \\ \frac{R}{c(R+R_c)} & \frac{-1}{c(R+R_c)} \end{bmatrix} \quad 3.15$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}, \; B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$C_1 = C_2 = \begin{bmatrix} \frac{RR_c}{R+R_c} & \frac{R}{R+R_c} \end{bmatrix}$$

Here A_1, A_2, B_1, B_2, C_1 *and* C_2 are defined as state matrix, input coefficient vector and output coefficient respectively.

3.5 Buck State Space Average Model

The state space average model is most commonly used to obtain the linear time invariant (LTI) and system of SMPC. The converter's waveforms (inductor current and capacitor voltage) over one switching period is averaged to produce the equivalent state space model. In this way, the switching ripples in the inductor current and capacitor voltage waveforms will be removed [18].

Procedure for State-Space Averaging

Linearization of the power stage including the output filter using state- space averaging Our aim is to find a small signal transfer function $\widehat{V_o}(s)/\hat{d}(s)$, where $\widehat{V_o}$ and $\hat{d}$ are small perturbation in

the output voltage Vo and d, respectively, around their steady state dc operating values Vo and D (CCM).

STEP:-1

State-variable description for each circuit state (parasite element i.e . R_L and R_c)

$\dot{x} = A_1 x + B_1 x$ During on time that is dTs

$\dot{x} = A_2 x + B_2 x$ During on time that is (1-d) Ts

Output can be described by

$V_o = C_1 x$ During dTs

$V_o = C_2 x$ During (1-d) Ts

STEP:-2

Averaging of the state space equations of both modes using the duty ratio d.

The equation are time weighted and average resulting in.

$\dot{x} = [A_1 d + A_2(1-d)]x + [B_1 d + B_2(1-d)]Vin$ 3.16

$V_o = [C_1 d + C_2(1-d)]x$

STEP;-3

Introduction of small AC perturbation and separation into AC and DC component.

$x = x + \hat{x}$

$V_o = V_o + \hat{V}_o$

$d = D + \hat{d}$

In general $V_{in} = v_{in} + \hat{v}_{in}$, however, in view of our goal to obtain the transfer function between voltage $\hat{V}_o$ and control input $\hat{d}$ the perturbation is assumed to be zero in the input voltage to simplify the calculation. Using above equations and making $\dot{x} = 0$ at steady state,

$\dot{\hat{x}} = Ax + BVin + A\hat{x} + [(A_1 - A_2)x + (B_1 - B_2)Vin\,]\hat{d}$ + Term combining products of $\hat{x}$ and d.

Where,

A = $A_1D + A_2(1 - D)$

B = $B_1D + B_2(1 - D)$

The steady state equation formed by setting all perturbation terms and their time derivation to zero i.e

Ax + BV_{in} = 0

And hence,

$\hat{x} = [(A_1 - A_2)x + (B_1 - B_2)Vin\,]\hat{d}$ 3.17

And,

$V_o - \hat{V}_o = Cx + C\hat{x} + [(C_1 - C_2)x\,]\hat{d}$

Where,

C = $C_1D + C_2(1 - D)$

Now for steady state,

$V_o = Cx$

$\hat{V}_o = C\hat{x} + [(C_1 - C_2)x\,]\hat{d}$

We have x =$C^{-1}V_o$

$BV_{in} = -AX$

$\frac{V_o}{V_{in}} = -CA^{-1}B$

STEP:-4

Transformation of the AC equation into S-domain to solve for the transfer function. On converting the equation in S-domain, we have

$$s\hat{x}(s) = A\hat{x}(s) + [(A_1 - A_2)x + (B_1 - B_2)Vin]\hat{d}(s)$$

Or

$$\hat{x}(s) = (sI - A)^{-1} [(A_1 - A_2)x + (B_1 - B_2)Vin]\hat{d}(s) \quad 3.18$$

Now using the Laplace transform of

$$\hat{V_o} = C\hat{x} + [(C_1 - C_2)x]\hat{d}$$

We have

$$\hat{V_o} = C\left[(sI - A)^{-1} [(A_1 - A_2)x + (B_1 - B_2)Vin]\right] + [(C_1 - C_2)x]\hat{d}(s)$$

$$\frac{\hat{V_o}}{\hat{d}(s)} = c(sI - A)^{-1} [(A_1 - A_2)x + (B_1 - B_2)Vin] + (C_1 - C_2)x \quad 3.19$$

Small signal model for buck and buck-boost converter without parasite element I.e R_C and R_L.

For a buck converter.

$$\frac{\hat{i}(s)}{V_{in}(s)} = \frac{D}{R} \frac{(1+sCR)}{\left(1+\frac{sL}{R}+s^2Lc\right)}$$

$$\frac{\hat{i}(s)}{\hat{d}(s)} = \frac{V_{in}}{R} \frac{(1+sCR)}{\left(1+\frac{sL}{R}+s^2Lc\right)}$$

$$\frac{\widehat{V_o}(s)}{V_{in}(s)} = \frac{D}{\left(1+\frac{sL}{R}+s^2Lc\right)}$$

$$\frac{\widehat{V_o}(s)}{\hat{d}(s)} = \frac{V_{in}}{\left(1+\frac{sL}{R}+s^2Lc\right)} \quad 3.20$$

Once the average state space model of the buck converter is defined, it is possible to implement the Laplace transform for obtaining the frequency domain linear time model. This model is important in the linear feedback control design. In voltage mode of the converters, the control to

output voltage transfer function (3.21) plays a significant role in locating the positions of poles/zeros for optimal voltage regulation [24] . The control to output transfer function can be calculated by implementing the Laplace transform to the small signal average model of DC-DC Buck converter in equation and then solving the system with respect to DC output voltage.

$$G_b(s) = \frac{V_{in}(CR_c s+1)}{s^2 LC\left(\frac{R+R_c}{R+R_L}\right)+s\left(R_c C+C\left(\frac{RR_L}{R+R_L}\right)+\frac{L}{R+R_L}\right)+1} \quad 3.21$$

The equation (3.21) clearly shows that the control to input transfer function of DC-DC buck converter is of second order hence making the system a second order system [1, 18]. The transfer function can be modified as:

$$G_b(s) = G_o \frac{1+\frac{s}{W_r}}{1+\frac{s}{Qw_o}+\left(\frac{s}{w_o}\right)^2} \quad 3.22$$

Here quality factor Q , the corner frequency w_o , zero frequency W_r and the DC gain G_o can be defined as [26]:

$$w_o = \sqrt{\frac{R_+R_L}{LC(R+R_{c)}}} \quad 3.23$$

$$Q = {}^{1}\Big/ w_o\left(R_c C + \frac{L}{R+R_L} + \frac{RR_L C}{R+R_L}\right)$$

$$G_o = V_{in} = \frac{V_o}{D}$$

$$W_r = \frac{1}{CR_c}$$

The control to output voltage transfer function of buck converter contains two poles and one pole (3.22). The quality factor (Q) and angular resonant frequency (w_o) basically governs the location as well as dynamic behavior of dc-dc converter. The quality factor indicates the amount of overshoot that occurs during transient response in respect of time. This factor is inversely related to damping ratio of the system [27, 28].

$$M_p \approx e^{\frac{\pi}{2Q}\Big/\sqrt{1-\frac{1}{4Q^2}}} \quad , \quad Q = \frac{1}{2\varepsilon} \quad 3.24$$

Also, since the output (R_C) of the dc-dc converter has a non-negligible resistance which introduce a zero value to the control to output function of the buck converter (3.22). This has a negative impact on the dynamic behavior of the SMPC. To cancel this effect, a constant pole in the control loop may be added and this is placed at the same value as the ESR zero.

3.6 Discrete Time Modelling of Buck SMPC

A discrete time model of DC-DC converters are essential for digital implementation of the control algorithms. The continuous time dynamic model is defined in order to derive this discrete model. Then, by sampling the states of the converter at each time instant, the continuous time differential equations are transformed into a discrete time model. In theory, different techniques have been proposed. These techniques including the direct transformation methods (Bilinear transformation, Zero-order-hold transformation, pole-zero matching transformation etc.) from s-to-z domain are generally describe the buck converter as a second order IIR filter [1, 5, 21, 30-33].

$$G_b(z) = \frac{b_1 z^{-1} + b_2 z^{-2} + \cdots + b_N z^{-N}}{1 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_M z^{-M}}, N = M = 2 \qquad 3.25$$

However zero-order-hold (ZOH) transformation approach is more preferable for discrete time modelling of the control to output function. The sample data signals are acquired based on sample and hold process followed by A/D process. In addition, the control signal remains constant during the sampling intervals and is modified at the beginning of each updated cycle. Therefore, both the control and output signals are based on ZOH operation.

$$G_b(z) = (1 - z^{-1}) Z\left\{\frac{G_b(s)}{s}\right\} \qquad 3.26$$

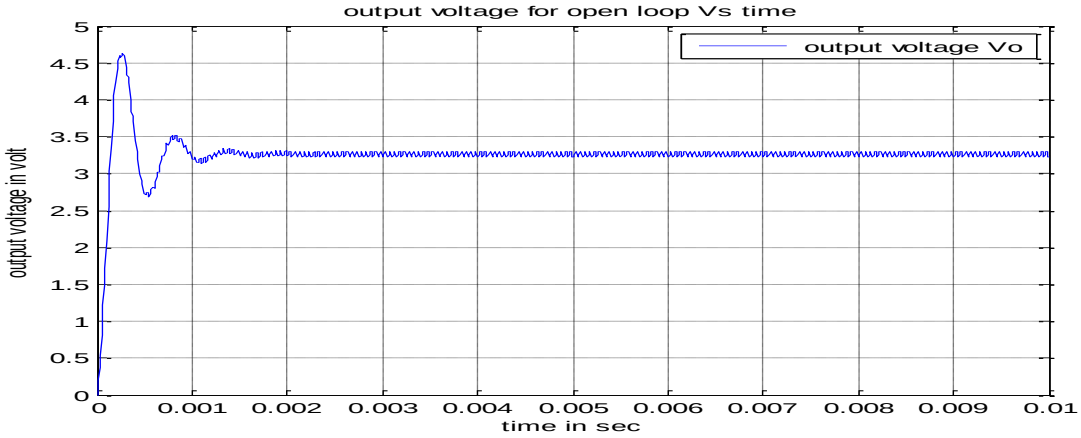
3.6 Simulation and Result of Open Loop Buck Converter

In order to find the output response of the open loop buck converter both non- linear as well as state space model have been simulated in Simulink MATLAB. Here the buck converter is designed for operating in the power supply of 5 Watt. The critical values of the inductor L and capacitor C are calculated by using the formulae

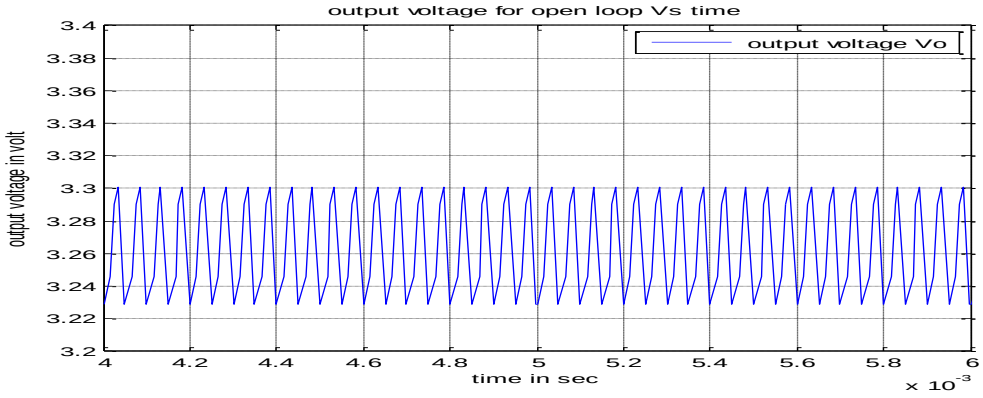
$$L_c = \frac{1-D}{2Rf} \quad , \quad C_c = \frac{1-D}{16Lf^2}$$

Hence the approximately found parameters are Inductor and capacitor value of L-C low pass filter is $L = 225\ \mu H$, $C = 330\ \mu F$ respectively. The value of parasitic taken are, $R_L = 65\ m\Omega$, $R_C = 25\ m\Omega$. Here the input voltage is 10 volt $V_{in} = 10\ V$ having a load $R = 5\Omega$. The switching frequency of the PWM is f = 20 kHz. The duty cycle of the PWM is chosen to be 33%.

The simulation and results are as follows:

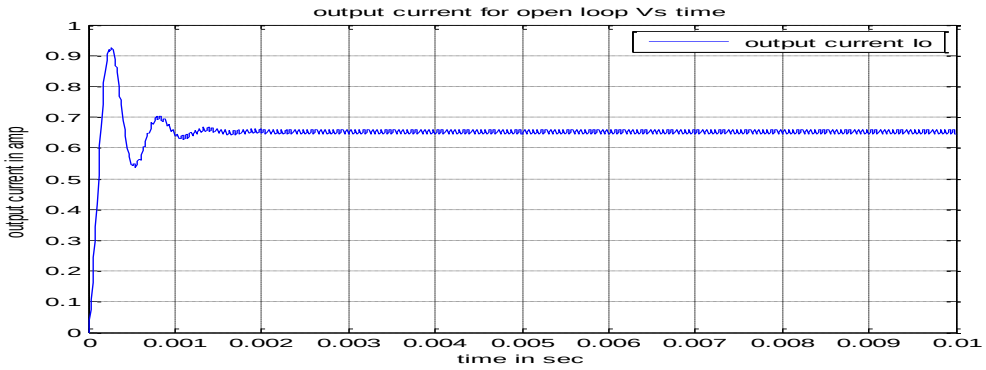


(a)

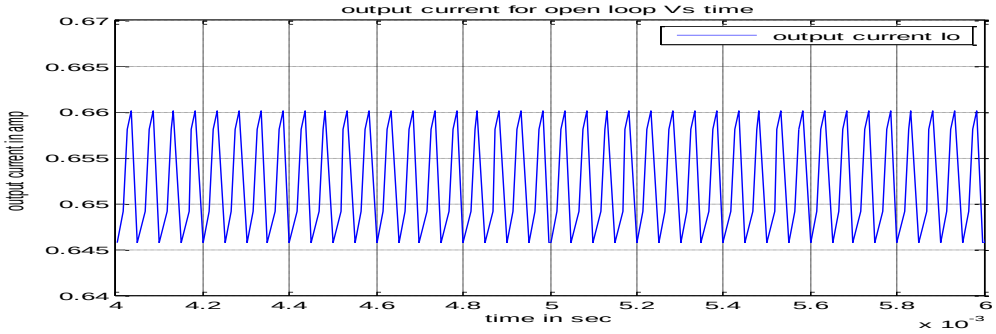


(b)

Fig 3.3 output voltage of buck converter

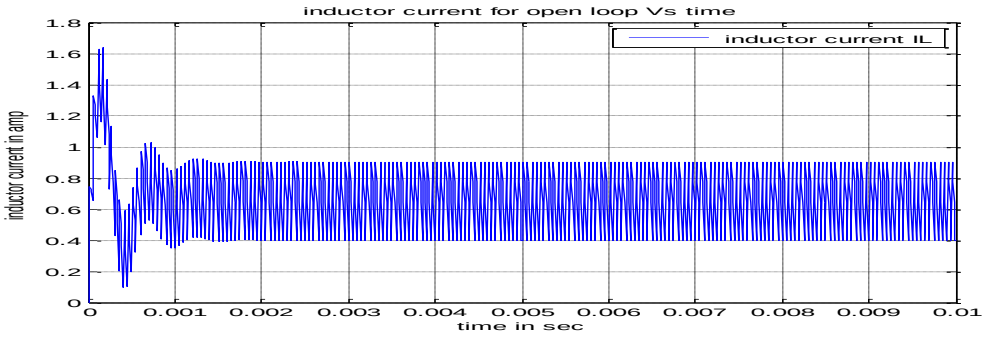


(a)

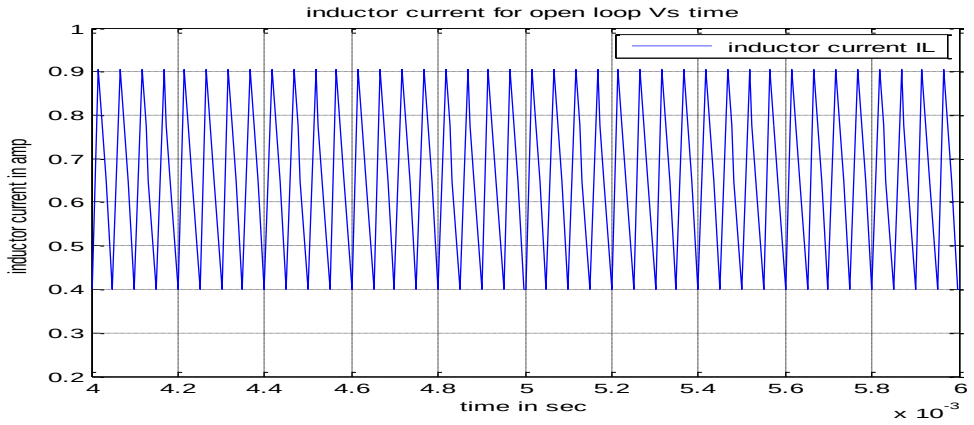


(b)

Fig 3.4 output current of buck converter



(a)



(b)

Fig 3.5 Inductor current of buck converter

Fig 3.3 shows the output voltage of the converter for the duty cycle of 33 %, the output voltage is found to be 3.298 volt which is approximately equal to the required voltage of 3.3 volt. The output current from Fig 3.4 is found to be about 0.6 ampere and Fig 3.5 shows the variation in inductor current over each switching period.

Chapter 4

DIGITAL CONTROL OF PWM BUCK CONVERTER

4.1 Introduction

Digital controllers are widely used in the control design of buck converters. Their use can significantly improve the performance of dc-dc converters. Digital controllers provide more flexibility in the design compared to the analog controllers and also they can be implemented with a small number of passive components, which reduce the size and cost of design. Moreover, digital controllers have low sensitivity on external disturbances and system parameter variation. In addition, they are easy and fast to design as well as modify or change the control structures or algorithms and it also enables advance control algorithms to be implemented. It can also be very easily reprogrammed. On the other hand, the analog system has faster power processing speed than digital controllers and also they have higher system bandwidth. Furthermore, no quantization effects are considered in analog systems.

There are two common control structures applied to closed loop design of the dc-dc power converters. They are Voltage mode control and Current mode control [10]. Digital Voltage mode controller are more preferred in the industry as current mode controllers require an additional signal condition circuit, consisting a high speed current sensor, thus increasing the cost. In addition, Voltage mode controllers are easier to design.

4.2 Digital Voltage Mode Control

As showed in Fig 4.1, there are six sub circuit blocks in a digitally controlled voltage mode scheme of buck converter. These circuits are categorized into two parts. The 1st part is defined as an Analog system. It includes dc-dc power processor stage, the gate drive and the sensing/signal conditioning circuit. The 2nd part is classified as the digital system including the digital controller and DPWM. The ADC block can be described as a mixed signal device.

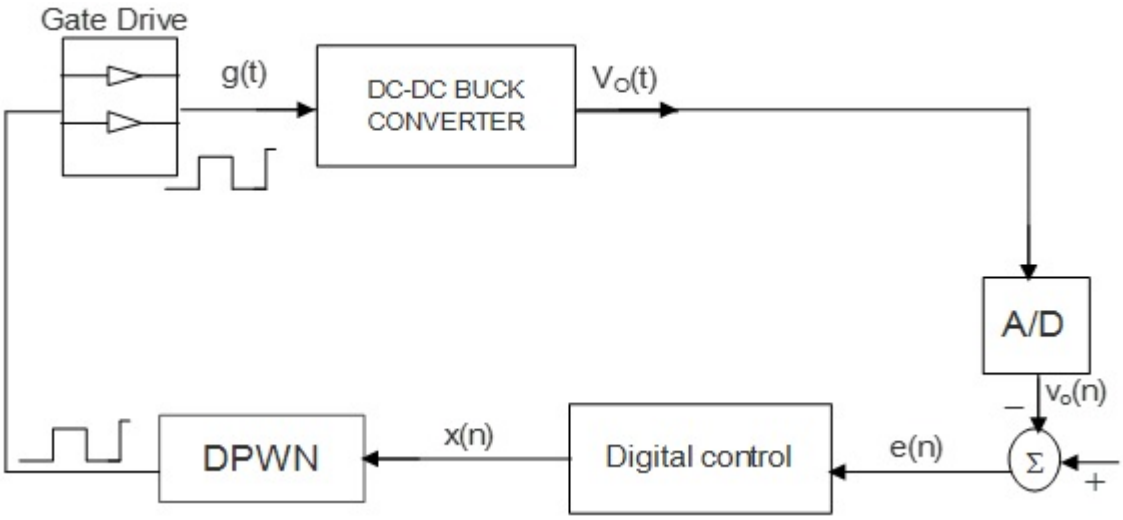


Fig.4.1 Digital voltage mode control architecture of DC-DC buck converter

The output voltage generated from the dc-dc power converter is firstly sensed and scaled by a commonly used resistive circuit voltage divider circuit with a gain factor equal to H_s. Therefore, Any sensed voltage higher than ADC full dynamic scale is attenuated by a factor to be processed b within the desired range, Other signal conditioning circuits are also used for suitable interfacing with ADCs like Analog buffer circuits with wide bandwidth operation and anti-aliasing filter to filter the frequency contend in the output voltage that is above the ADC sampling criteria [11].

The sensed output voltage (Vo) is digitized by ADC. Two factors must be considered for suitable selection of the ADC, they are:

1) The A/D number of bits or A/D resolution. This is important to the static and dynamic response of the controlled voltage of buck converter. The A/D must be less than the allowed variation in the sensed output voltage.
2) The conversion time is also an important factor in the selection of ADC as it indicates the maximum sampling rate of the ADC. In digitally controlled buck converters, small conversion time is required to achieve a fast response and high dynamic performance.

Generally, the sampling time equal to switching frequency of the buck converter is chosen to ensure that the control signal is updated at each switching cycle.

The digital reference scale is compared with the scaled sampled output voltage, v_o (n). The resultant error voltage signal is then processed by the digital controller via its signal algorithm. A second order IIR filter is used as a linear controller that governs the output voltage of the buck converter. Generally this IIR filter acts as a digital PID compensator as a central controller in the feedback loop.

$$G_c(z) = \frac{\sum_{i-0}^{N} q_i z^{-1}}{1-\sum_{K-1}^{M} s_k z^{-k}} \qquad 4.1$$

Both non-linear control and intelligent control techniques can also be applied for the digital control of buck converter. However, the control signal is then computed on cycle by cycle basis. The desired duty ratio of the PWM is produced by comparing the discrete control signal with the discrete ramp signal.

Here, the DPWM performs as an interface circuit between the digital and analog domains of the digitally controlled architecture within the buck converter simulating the purpose of the digital to analogue converter (DAC). The gate drive of the circuit is used to amplify the *On/Off* command signals generated across the DPWM. The output if the ate signal is then used to activate the power switches of the buck converter.

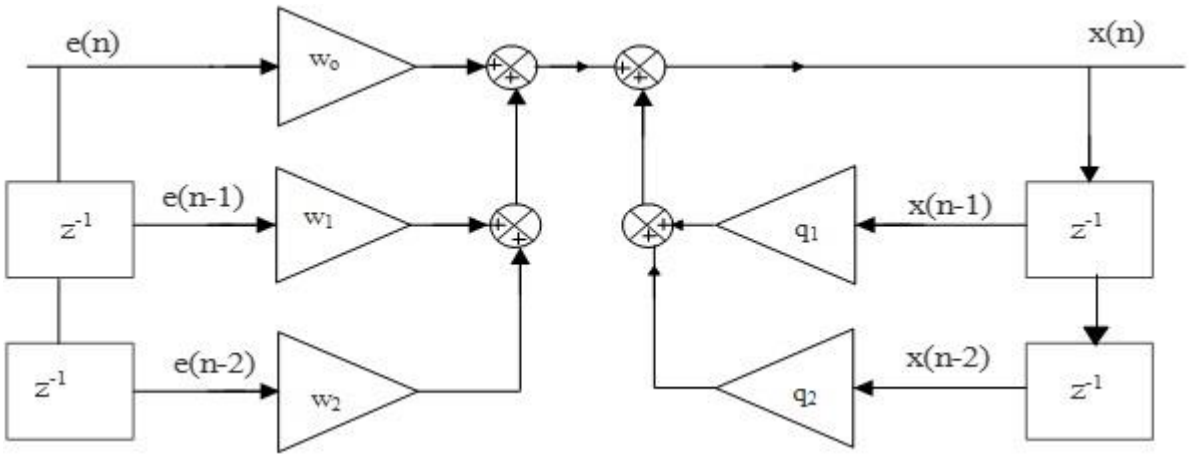


Fig.4.2 Two-poles /Two-zeros IIR digital controller

High resolution DPWM is necessary for the digital control of buck converters as it leads to accurate regulation of the voltage and avoid the limit cycle oscillation phenomenon. Limit cycles are defined as non-linear phenomenon that occurs in digital control of the dc-dc converters during steady state periods. These can be avoided if DPWM resolution is higher than ADC resolution [29]. Also, care is taken in selection of the integrated gain in PID controllers, as extensively high values of integrated gain can cause limit cycle oscillations around the steady state value.

4.3 Digital Proportional-Integral-Derivative Control

The digital PID controller is very commonly used in control loop design of buck converters as the PID control parameters are easy to tune and the designed controllers are easy to realize [31].

$$G_c(z) = \frac{D(z)}{E(z)} = K_p + K_I \frac{1}{1-z^{-1}} + K_D(1 - z^{-1}) \quad 4.2$$

$$d(n) = d_p(n) + d_1(n) + d_D(n) \quad 4.3$$

Where:

$$d_p(n) = K_p e(n)$$

$$d_I(n) = K_I e(n) + d_1(n-1) \quad 4.4$$

$$d_D(n) = K_D[e(n) - e(n-1)]$$

The variables K_P, K_I, and K_D, are the proportional-integral-derivative gains of PID controller, $e(n)$ is the error signal $[e(n) = V_{ref}(n) - v_O(n)]$, and $d(n)$ is the control action.

$$d(n) = d(n-1) + q_0 e(n) + q_1 e(n-1) + q_2 e(n-2) \quad 4.5$$

$$q_0 = K_p + K_I + K_D$$

$$q_1 = -(K_p + 2K_D) \quad 4.6$$

$$q_2 = K_D$$

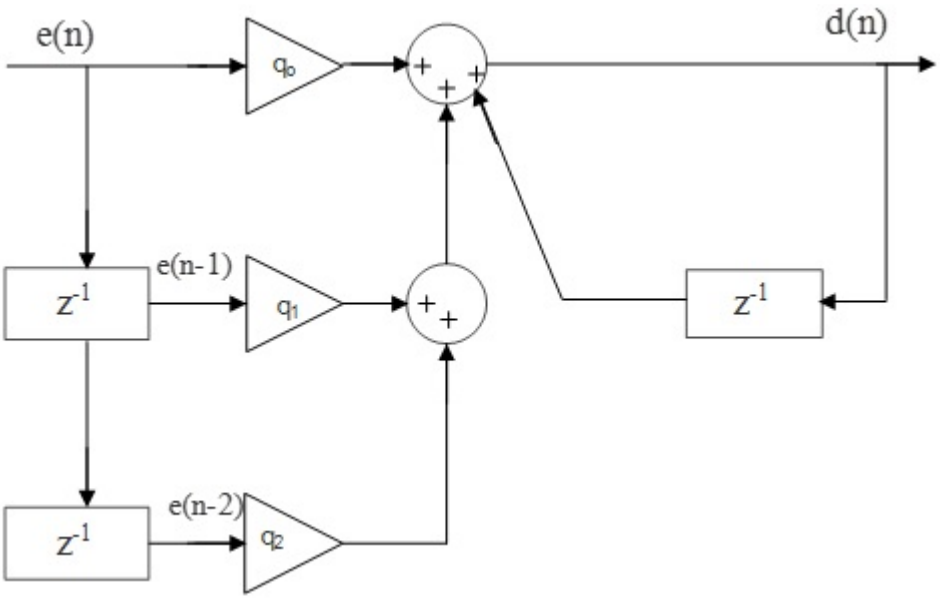


Fig.4.3 Digital PID compensator

System performance, loop bandwidth, gain margin and phase margin are determined based in PID coefficients. For instance, decrement in steady state error is achieved by the integral gain. However the integral part will add a pole at the origin to the open loop transfer function of the system. To ensure the system stability, this pole needs more consideration. In frequency domain, the integral part acts as a low pass filter making the system less susceptible to noise. Tough it adds phase lag to the system which reduces the phase margin of the control loop, thus more oscillations can be observed in the output response. Therefore to improve the stability of the system and enhance the dynamic performance, a derivative part should be introduced in the control loop to increase the phase margin (phase lead). The derivative controller is responsible for the rate of change of the error signal. For example, if the sensed output voltage of buck converter reaches the desired set point quickly then the derivative part slows the rate of change in the output control action. Therefore the derivative part is considered as intelligent part of the controller. However, the derivative part is more sensitive to the noise in the system [34], hence the derivation of error signal will amplify the noise in the control loop. The proportional gain makes the output of the PID controller respond to any change of the error signal. The PID controller has the same scheme functionality of the phase lead-lag compensator.

The parameters of the PID controllers can be determined indirectly or directly. In the indirect method, the discrete model of SMPC and the PID controllers are used, therefore all the calculations are obtained in the z domain. In this method a more accurate control loop can be achieved, where the errors related to the transformation approximation from s to z domains are avoided [17]. Whereas in the indirect approach, a continuous time domain of buck converter is used and the PID controller is designed in the s domain. Different transformation methods like bilinear transform method, backward Euler method and pole zero cancellation method can be used to transfer the PID controller from the continuous domain to the discrete domain. However this technique will increase the inaccuracy in the system performance due to the transformation approximation from s to z domain. Here we will discuss the two most common approach used in the digitally controlled design of buck converters: the pole-zero approach and the systematic pole placement method.

4.4 Digital Control for Buck converter based on PID Pole-Zero Cancellation

The design method presented here follows the same procedure as established in [23]. The design starts from the continuous model of the buck dc-dc converter, In order to cancel the two poles of power converter in (3.22), the two zeros should be placed exactly at the same frequency defined by w_o of the dc-dc power converter as given in equation (3.22). For simplicity of design, let's assume $R_C = 0$;

$$G_c(s) = G_{co}\frac{1+\frac{s}{Qw_o}+\left(\frac{s}{W_o}\right)^2}{s} \quad 4.7$$

Therefore, the overall loop gain is reduced to only one pole at origin together with the dc gain:

$$L(s) = \frac{G_o G_{co}}{s} \quad 4.8$$

It can be seen that in this technique precise knowledge of the power converter parameters such as quality factor and converter corner frequency, is required [27]. This is one of the drawbacks of this method, where the effect of any change in the dc-dc converter parameter directly influence the PID coefficients and in turn to the overall control loop. Therefore, an accurate parameter estimation is required for adequate control design. So, a fixed value of the quality factor is chosen. Since, quality factor is related to the damping factor. For an effective damping response, the damping factor is varied between 0.6 and 1.0 [21]. The resonant frequency of PID zeros are

approximated to be at the same value of power converter corner frequency. As a result, the compensator zeros are assigned close to the converter poles; this will ensure the system robustness. As a result, the overall loop gain can be written as:

$$L(s) = G_o G_{co} \frac{\left(1+\frac{2\xi s}{Qw_o}+\frac{s^2}{w_z^2}\right)}{\left(1+\frac{s}{Qw_o}+\frac{s^2}{w_z^2}\right)} \quad 4.9$$

Here, G_{co} is the dc gain. This gain is selected to satisfy design requirement such as phase margin and gain margin. The root-locus method can be used to find G_{co}.

$$G_{co} = \frac{2\pi f_b}{G_o} \quad 4.10$$

Finally, by using the pole-zero matching transformation method the discrete PID gains described in (4.6) can be determined.

4.5 Pole Placement PID Controller for DC-DC Buck Converter.

In pole placement approach for digital control of the buck DC-DC converter, a discrete PID control is used having two zero and two poles.

The transfer function is as follow;-

$$G_b(z) = \frac{b_1 z^{-1}+b_2 z^{-2}}{1+ a_1 z^{-1}+ a_2 z^{-2}} \quad 4.11$$

$$G_c(z) = \frac{\beta_0+\beta_1 z^{-1}+\beta_2 z^{-2}}{(1-z^{-1})(1+ az^{-1})} \quad 4.12$$

$$d(n) = \beta_0 e(n) + \beta_1 e(n-1) + \beta_2 e(n-2) + (1-\alpha)d(n-1) + \alpha d(n-2) \quad 4.13$$

The loop control transfer function of controller and plant is as follow[37] :

$$G_L(z) = \frac{B(z)\beta(z)}{A(z)\alpha(z)+B(z)\beta(z)} \quad 4.14$$

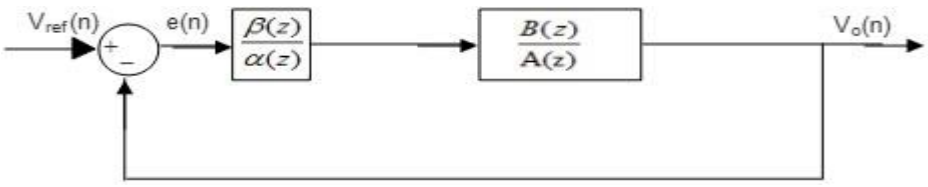


Fig 4.4 Closed loop control of Buck converter

To solve the relation of parameter in the dominator polynomial. The desired closed loop dynamic of the system can be used. Hence , in order to get required response the location of the closed loop poles are set according to the desired value instead of turning the conductor, coefficients in other techniques [37].

The characteristic equation can be formulated as:-

$$D(z) = A(z)\alpha(z) + B(z)\beta(z)$$

$$= 1 - \sum_{K-1}^{N_d} d_k z^{-k} = 1 + d_1 z^{-1} + d_2 z^{-2} + \cdots + d_{N_d} z^{-N_d}, \quad N_d \leq 4 \qquad 4.15$$

To describe the dived closed loop dynamics of the system of second order model, second order characteristic equations is used.

i.e $$G(s) = s^2 + 2\xi w_n s + w_n^2 = 0 \qquad 4.16$$

For better performance and proper damping response the damping factor and the natural frequency should be selected properly.

$$d_1 = -2e^{-\xi w_n T_s} \cos\left(w_n T_s \sqrt{1-\xi^2}\right)$$

$$d_2 = e^{-2\xi w_n T_s} \qquad 4.17$$

Rewriting the equation in matrix form we get ,

$$\begin{bmatrix} b_1 & 0 & 0 & 1 \\ b_2 & b_1 & 0 & a_1 - 1 \\ 0 & b_2 & b_1 & a_2 - a_1 \\ 0 & 0 & b_2 & -a_2 \end{bmatrix} \begin{bmatrix} \beta_0 \\ \beta_1 \\ \beta_2 \\ \alpha \end{bmatrix} = \begin{bmatrix} d_1 + 1 - a_1 \\ d_2 + a_1 - a_2 \\ a_2 \\ 0 \end{bmatrix}, N_d = 2 \qquad 4.18$$

$$\beta_0 = \frac{1}{b_1}(d_1 + 1 - a_1 - \alpha)$$

$$\beta_1 = \frac{a_2}{b_2} - \beta_2 \left(\frac{b_2}{b_2} - \frac{a_1}{a_2} + 1\right) \qquad 4.19$$

$$\beta_2 = \frac{s}{r}$$

$$\alpha = \beta_2 \frac{b_2}{a_2}$$

$$s = a_2([b_1 + b_2][a_1 b_2 - a_2 b_1] + b_2[b_1 d_2 - b_2 d_1 - b_2]$$

$$r = [b_1 + b_2]\left[a_1 b_1 b_2 + a_2 {b_1}^2 - {b_2}^2\right]$$

From the equation (4.18), it can be deducted that the solution of equation needs matrix inversion in order to find the control variables hence on –line updating is computationally heavy process which makes the pole placement method more suitable for Off-line control applications.

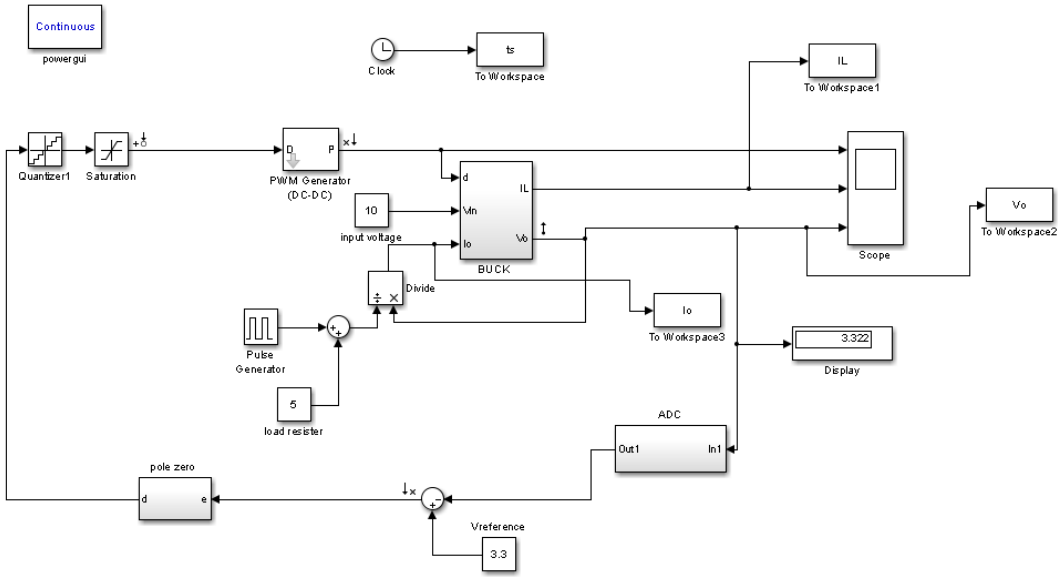
4.6 Simulation Results and Discussion

4.6.1 Simulation of a Buck converter based on PID pole-zero Cancellation

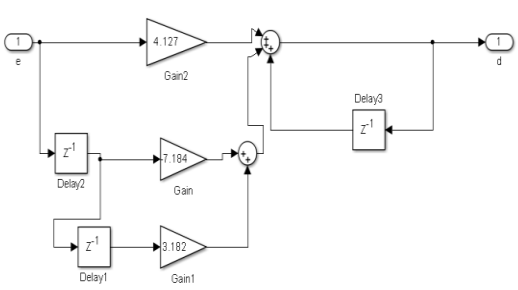
In order to see the response of PID controller based on pole zero cancellation approach, the voltage mode control topology of buck converter is simulated in Simulink. Inductor and capacitor value of L-C low pass filter is $L = 225\ \mu H$, $C = 330\ \mu F$ respectively. The value of parasitic taken are, $R_L = 65\ m\Omega$, $R_C = 25\ m\Omega$. Here the input voltage is 10 volt $V_{in} = 10\ V$ having a load $R = 5\Omega$. The switching frequency of the PWM is f = 20 kHz and the sampling time Ts is 50μs . Here the damping factor is chosen to be 0.7 with the corner frequency w_0 as 3722.5 rad/sec from calculations. After substituting the value of these in the equation (4.7) the control transfer function is obtained. In order to obtain the coefficients of digital PID controller the s to z based MATLAB pole zero matching method is used and then written in the form of equation 4.20. Hence the PID controller gains are finally tuned for optimal value and found as q_0 =4.125, q_1= -7.185 and q_2= 3.182.

$$d(n) = d(n-1) + 4.127e(n) - 7.184e(n-1) + 3.182e(n-2) \qquad 4.20$$

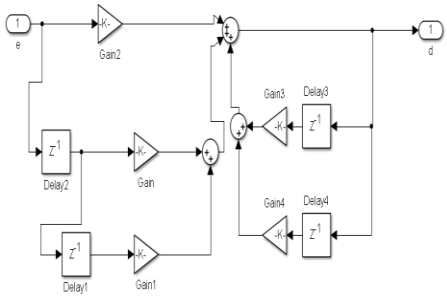
Simulink model of PWM buck converter with PID controller



(a)



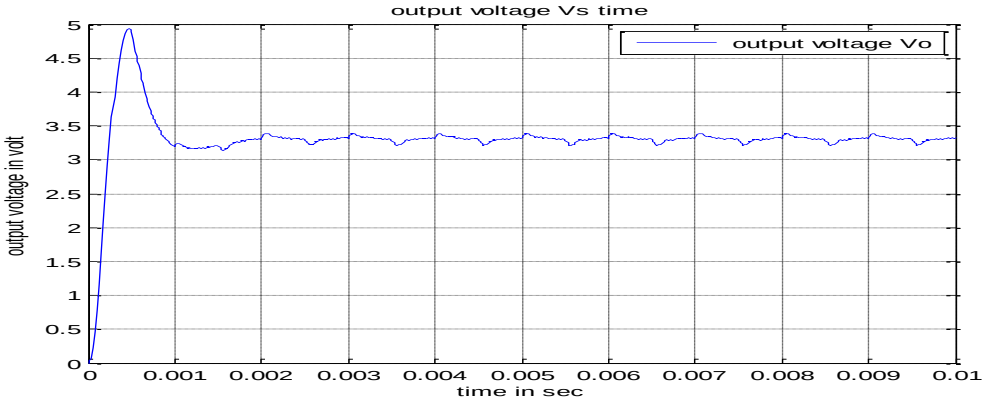
(b)



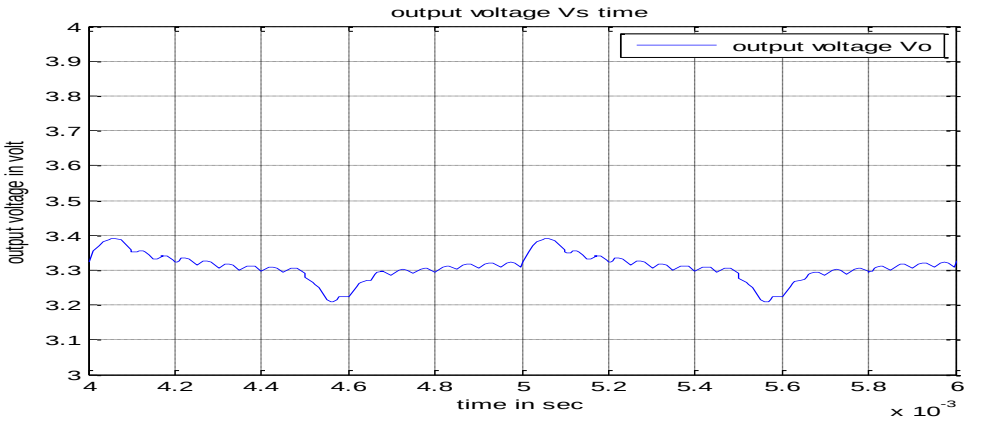
(c)

Fig 4.6 a; Simulink model of buck converter with PID, b; FIR filter as PID based on pole zero cancellation, c; IIR filter as PID based on pole placement controller

Simulation results for DC-DC buck converter using pole zero cancellation approach:

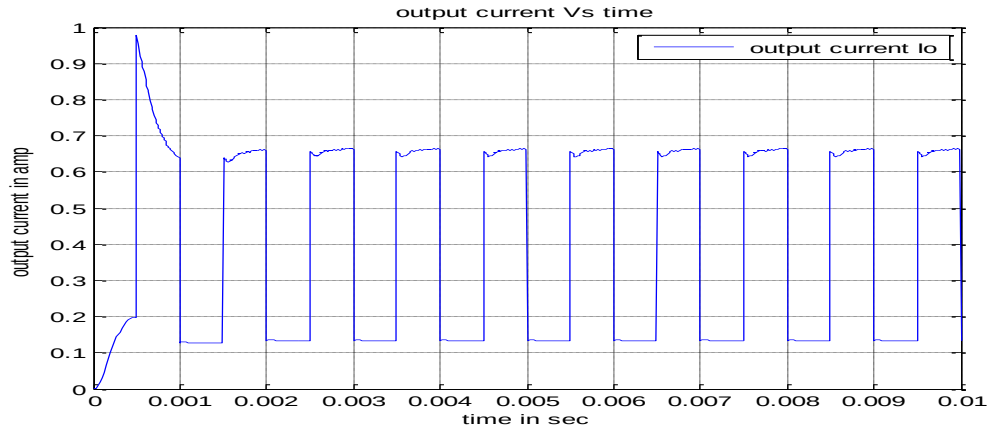


(a)

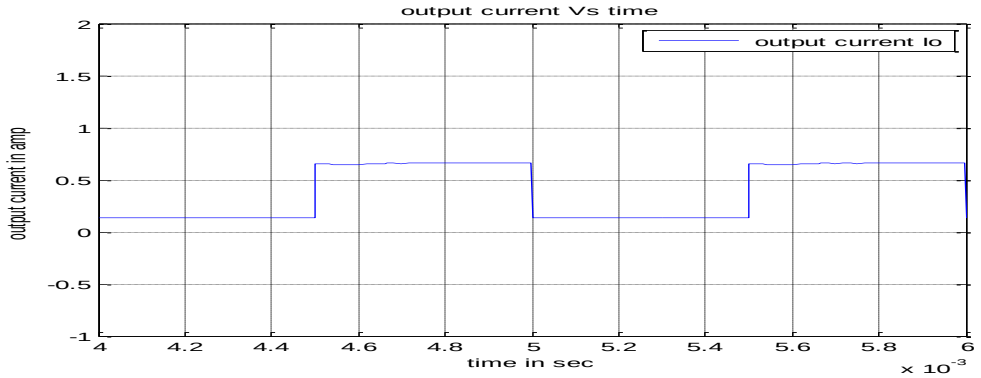


(b)

Fig 4.5 output voltage of buck converter for varying load using pole zero controller

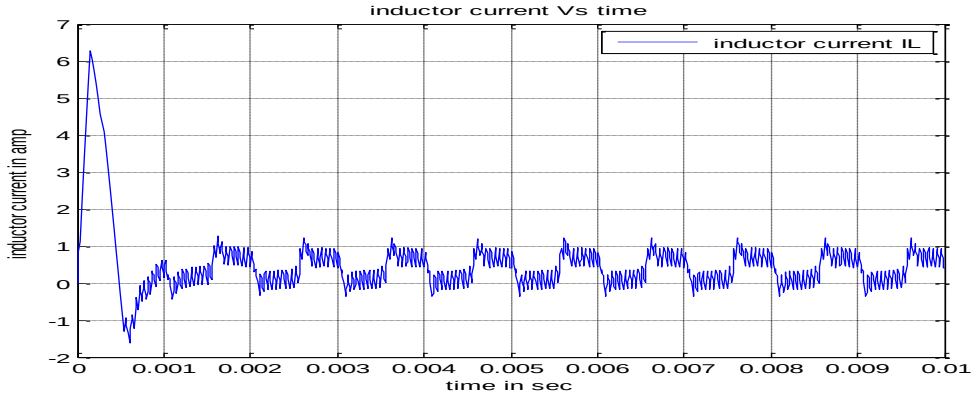


(a)

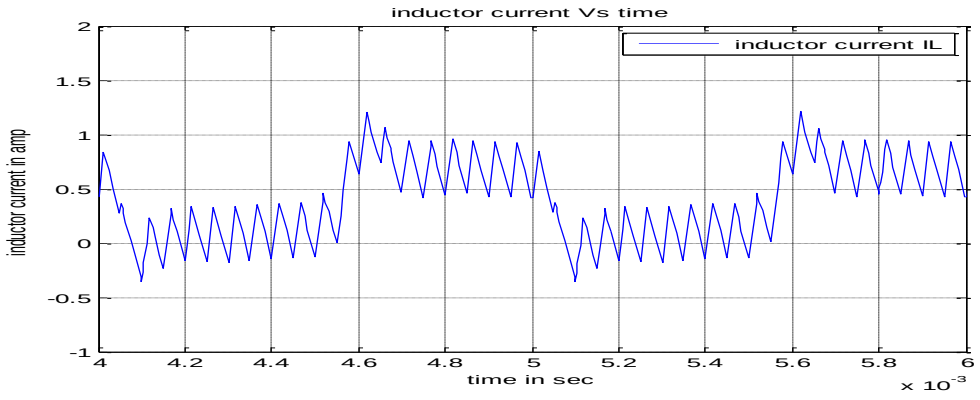


(b)

Fig 4.7 Output current of buck converter for pole zero PID controller



(a)



(b)

Fig 4.8 a; b; Inductor current for pole zero PID controller

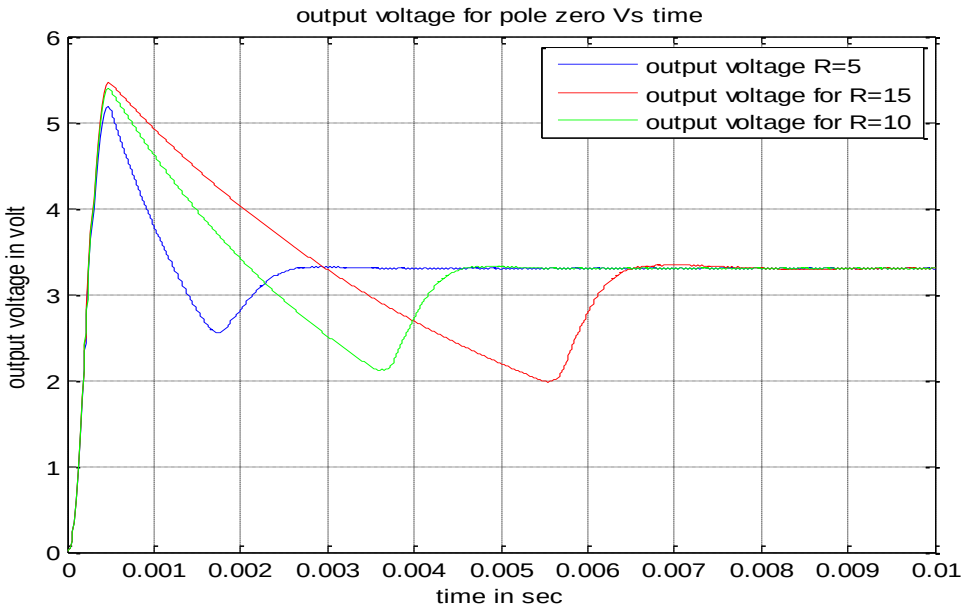


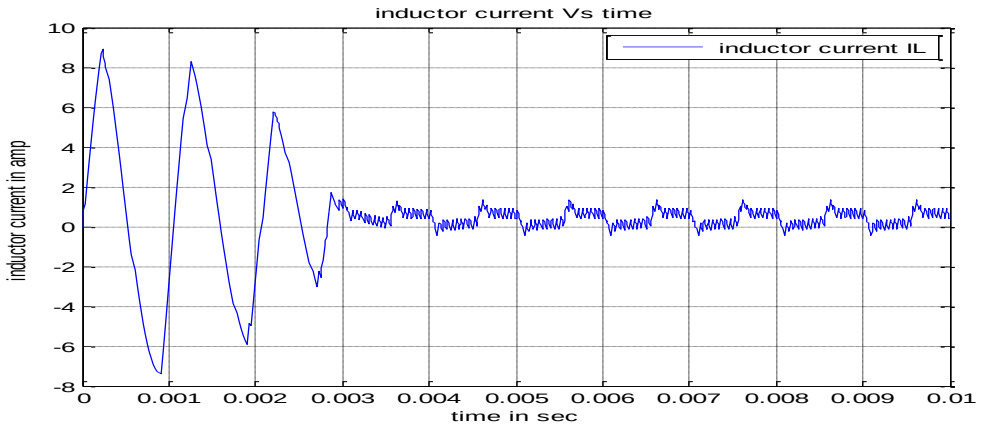
Fig 4.9 Response of output voltage on load variation for PID based on Pole zero cancellation

4.6.2 Simulation design of a Buck converter based on PID pole placement approach

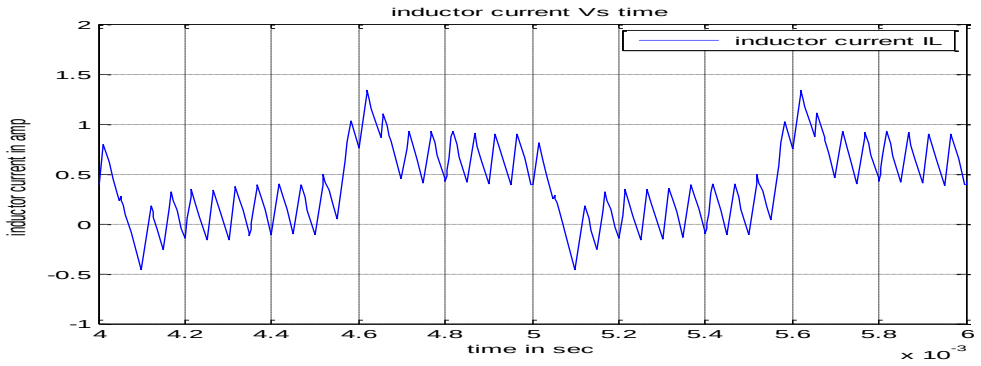
The parameters of Buck converter are selected as same as that are taken in pole zero approach. Here the natural frequency is chosen to be the twice of corner frequency that is $w_n = 2w_0$ = 7445 rad / sec , along with the damping factor of 0.7 . Putting these parameters in equations 4.17 and 4.19 , the coefficient of PID gains are found to be $\beta_0 = 4.672$, $\beta_1 = -7.54$, $\beta_2 = 3.185$ and $\alpha = 0.3747$ hence the digital PID controller can be represented by equation :

$$d(n) = 4.672e(n) - 7.539e(n-1) + 3.184e(n-2) + 0.6253d(n-1) + 0.3747d(n-2)$$

Simulation results of buck converter using PID controller based on pole placement approach

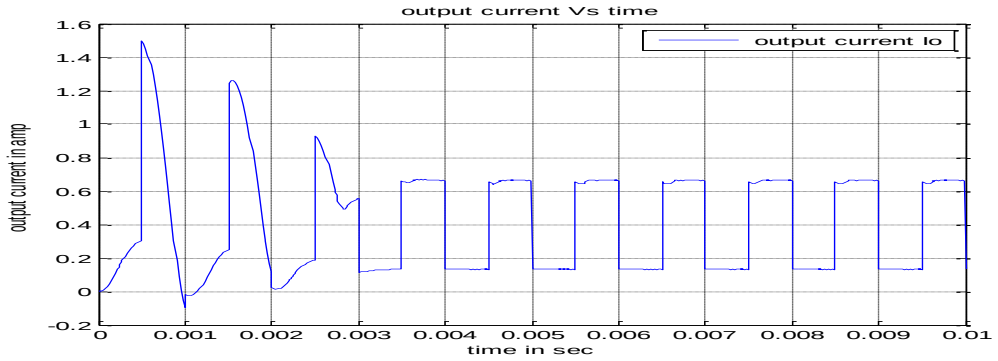


(a)



(b)

Fig 4.10 a; b; Inductor current for pole placement PID controller



(a)

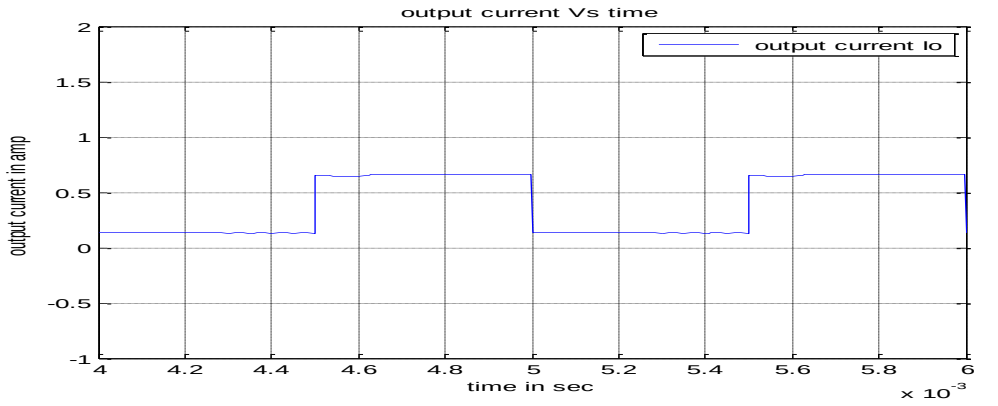
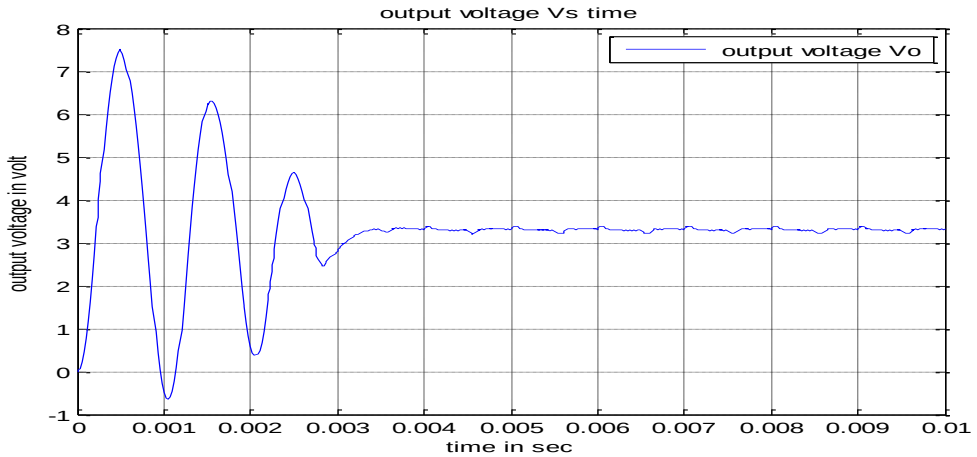
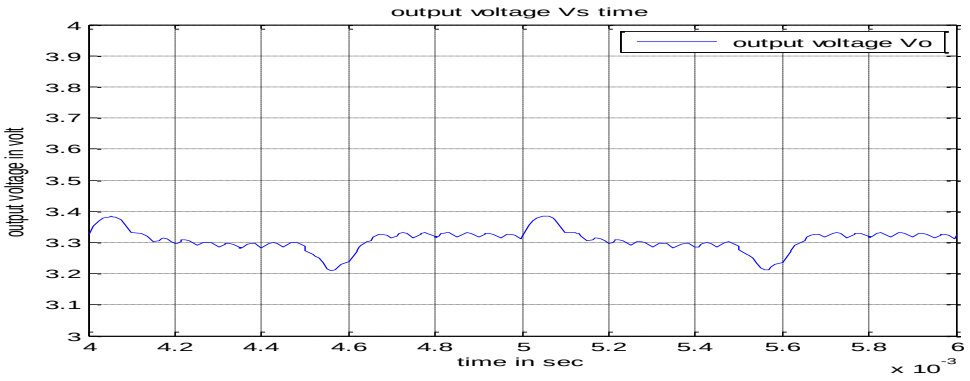


Fig 4.11 Output current of buck converter for pole placement PID controller



(a)



(b)

Fig 4.12 Output voltage of buck converter based on pole placement approach

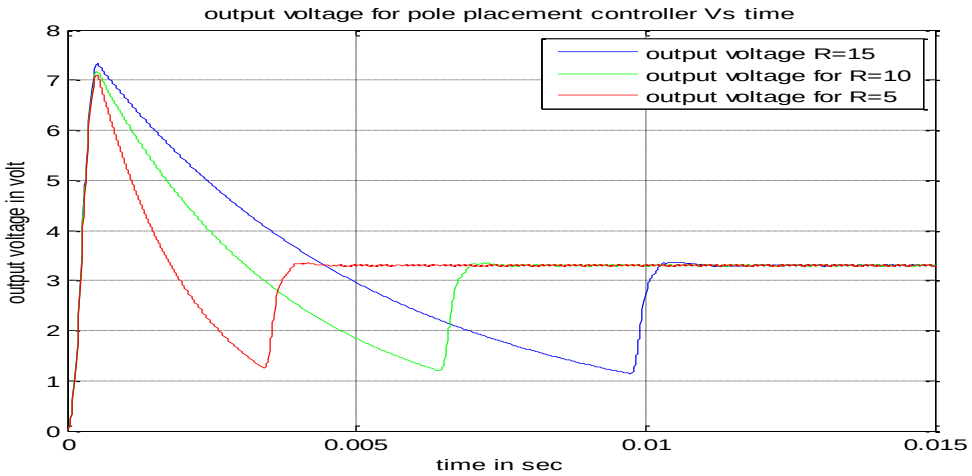
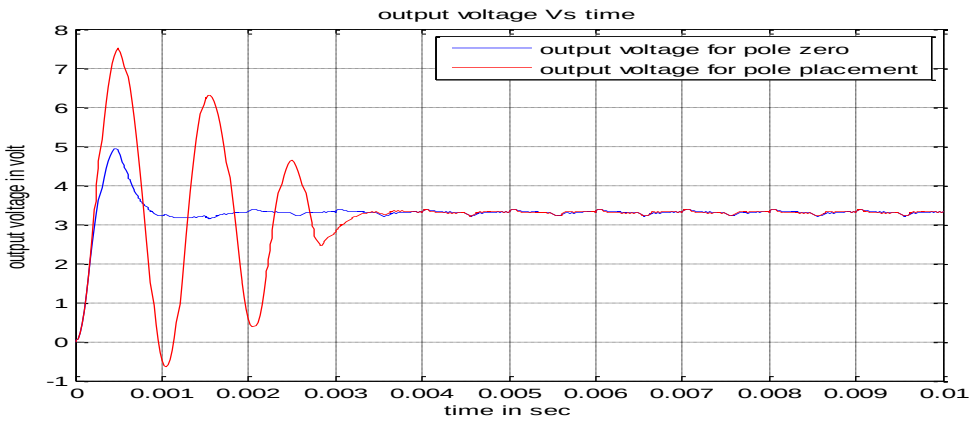


Fig 4.13 Response of output voltage on load variation for PID based on Pole zero cancellation



(a)

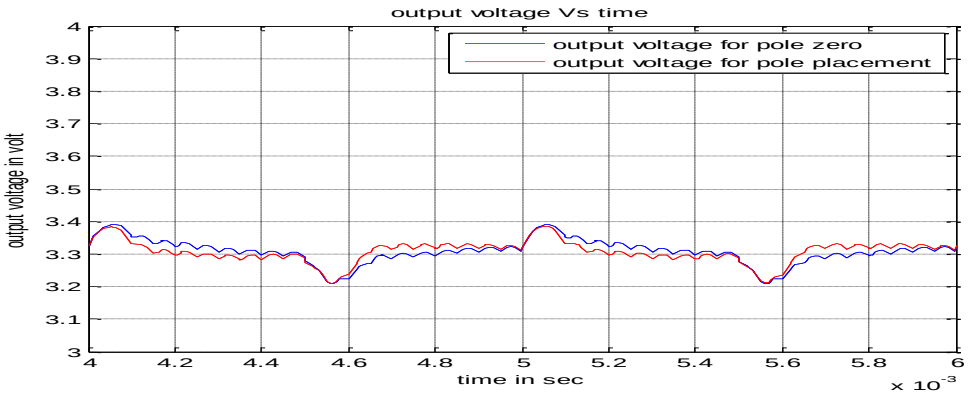


Fig 4.14 comparison of output voltage between pole zero and pole placement PID controller

Discussion

In the simulation results shown in above, it can be clearly seen that both the PID controller approach gives satisfactorily voltage regulation with some ripples when the load is varied in certain interval. Fig 4.5, 4.8, 4.11, 4.12 shows the response of output voltage of the buck converter with PID controller based on pole zero cancellation as well as pole placement approach respectively, it can clearly see that when the load current varies from one level to another Fig 4.6, 4.10 there is a fluctuation in the output voltage which dies out as the controller makes the output voltage to track the desired voltage level. Fig 4.6, 4.7, 4.9, 4.10 describe the variation in inductor current as well as output current of both the topologies. Fig 4.8 , 4.12 shows the variation of output voltage with different load , and the result suggest that with the increase in load the time taken to achieve the steady state also increases as well as small increase in peak overshoot the . There is a comparative study between the voltage regulation of the two approaches and it is found that the pole zero cancellation approach gives better performance than that of the pole placement controller as it takes less time to achieve the desired voltage level with less over shoot .

.

Chapter 5

ADAPTIVE CONTROL SCHEME USING ONE TAP FIR PREDICTOR ERROR FILTER

5.1 Introduction

According to Astrom and Wittenmark, to adapt means "to adjust a behavior to conform to new environment ". Adaptive or self -tuning controller cannot be realized without taking into the consideration of adaptive signal processing, as it is necessary to identify the system first for the design of self-tuning controllers. An adaptive inverse filter approach is used by Plett and Widrow for tuning the parameters of the adaptive controller successfully. In order to adjust the parameters of an unknown system, it is needed to minimize the error function of the system and update the coefficients which can be done by using Least Mean Square (LMS) algorithm.

For the design of any controller, the control of varying parameters need to be taken care of as it can leads to inaccurate results. With the variation of load and because of uncertain parameter the classical digit control schemes fails to provide accurate response because of inaccuracy's in this design. The uncertain parameter needs to be self-adjusted adaptively according to desire response. Hence, there is need to design an adaptive and self-turning digit controller which can provide a robust control solution and can quickly adapt to the varying parameter. This section highlights a new topology based on a simple adaptive filter methods which uses a one tap FIR prediction error filter. Here, the least mean square algorithms is implemented as the adaptive predictor error filter. It can be seen from stimulation that the dynamic response and convergence rate of the adaptive gains within the controller is improved using LMS algorithms. This result in a significant improvement in the overall dynamic performance of the closed loop control system of the converter, especially in the case of sudden changes in parameter. It is evident from result that the adaptive controller using one tap FIR predictor gives better voltage regulation and dynamic performance as compared to classical PID controller. In this controller an adaptive proportional derivative along internal compensator is used with LMS algorithms which proves to be more effective than convectional PID controller. The purpose of adding a non-adaptive integral controller in the feedback loop is to ensure better voltage regulation and increase in filter tap weight

excitation. This methods gives a self-compensating controller with fast adaptation. Which is needed to minimize the predicted error signed. Which leads to minimizing the voltage signal by finding the optimal positions of the pole automatically. In order to ensure that the adaptive gains converges to their optimal position value a second stage FIR filter i.e. adaptive gain stage is implemented to further minimize the predicted error signal.

5.2 Adaptive Filters and Linear Predictor

Adaptive filters as well as adaptive controllers are time varying systems as in order to obtain the required performance their parameters need to be updated repetitively. An adaptive filter can be defined as a self- designing filter , as its coefficient keep updating frequently until the desired signal is found. The adaptive filter mainly comprise of two components that is , a digital filter and an adaptation algorithm , used for varying the tap weight coefficients to get desired signal. For minimizing the estimated error most common adaptive algorithms used are least square algorithms such as LMS algorithm and RLS algorithm. They complete the task by iteratively updating the Filter parameters.

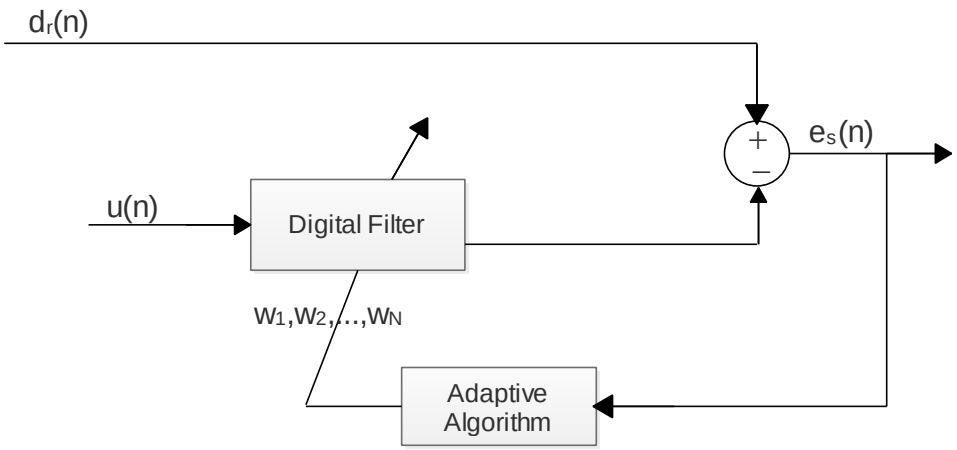


Fig. 5.1 Structure of an adaptive filter

5.3 Adaptive control of a buck converter using a predictive FIR

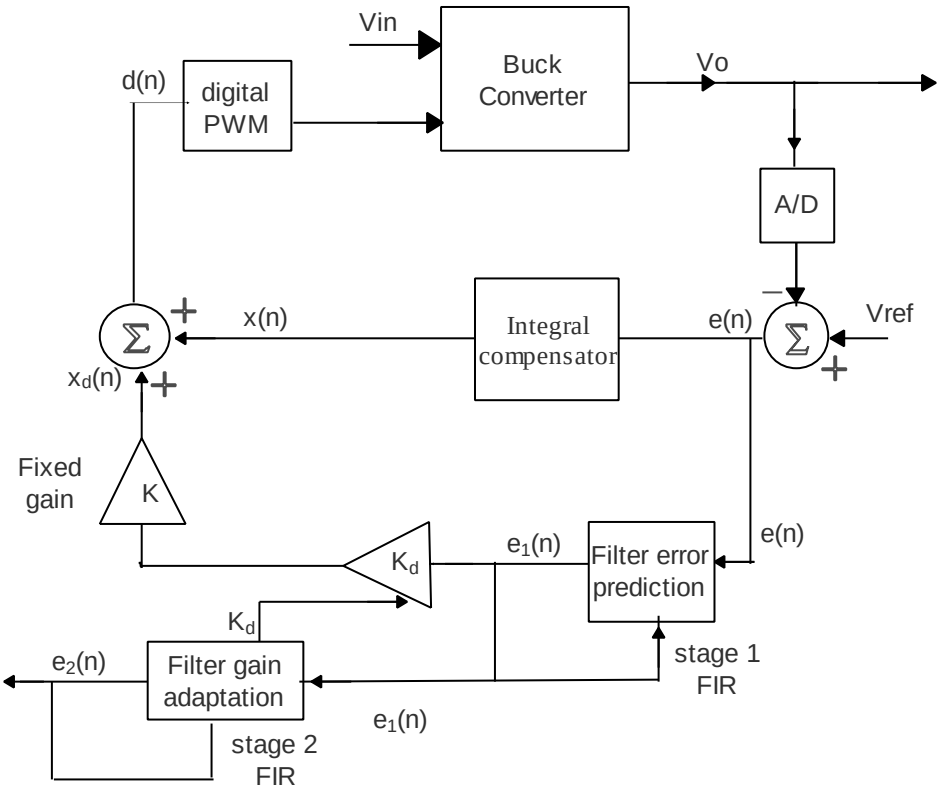


Fig 5.2 Adaptive PD+I controller using one tap LMS PEF

In the figure 5.2 there are two feedback loops one having a non- adaptive integral compensator and other having an adaptive PD Controller. By using these scheme we intend to get a PD + I controller which can be adaptive [36, 37]. The non -adaptive integral compensator have many purpose in this scheme. It is used to excite the system during the initial convergence of time for the filter tap weights. A transient is introduced by the compensator which commence an oscillation in the control error signal. The convergence time that is time required for optimal taps weight parameters get improved by the excitation signal , which then allows the controller to perform well and self-adjust continuously while operation .

This adaptive predictor error filter recognize the nature of oscillations generated by the integral controller and discards it from feedback loop , which in turn results in better voltage regulation. There is small fluctuation in voltage dynamics only when the loads get changed as it rapidly adapts the variation in voltage and return back to desired response. It also ensure that the steady-state

error becomes zero in the system. In order to increase the excitation until the optimal values of adaptive filter weight is achieved, a fixed gain is included at the output of PD compensator in closed loop (Fig 5.2) . The value of gain for buck converter is chosen to be equal to K'= L/T, here L is the value of inductor and T is the switching period [36].

5.4 Auto Regressive Process Generation and Analysis

An auto regressive process generator along with auto regressive analyzer that is moving average FIR filter is required in order to implement a predictor error filter in the closed feedback loop as central controller. The system H (z) generates the signal x(n) by introducing dependence in the white noise input w(n) and is known as the synthesis or coloring filter. In contrast, the inverse H(z) can be used to recover the input w(n) and is known as the analysis or whitening filter (Fig 5.3). In this sense the innovation sequence and the output process are completely equivalent.

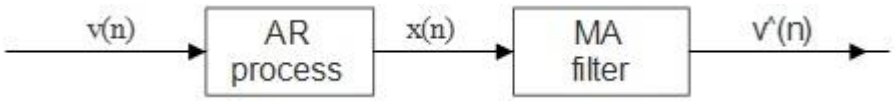


Fig 5.3 Reconstruction of white noise

Parametric pole-zero signal model.

Consider a system described by the following liner constant-coefficient difference equation.

$$x(n) + \sum_{i=1}^{P} a_i x(n-i) = \sum_{i=0}^{Q} d_i v(n-i) \quad 5.1$$

$$H(z) = \frac{X(z)}{V(z)} = \frac{\sum_{i=0}^{Q} d_i z^{-i}}{1+\sum_{i=1}^{P} a_i z^{-i}} \quad 5.2$$

We can express $H(z)$ in terms of poles and zeros after system as follows.

$$H(z) = d_o \frac{\prod_{i=1}^{Q}(1-a_i z^{-1})}{\prod_{i=1}^{P}(1-b_i z^{-1})} \quad 5.3$$

We have p=0 we have all-zero model AZ(Q) known as the moving-average model denoted by MA(Q), the difference equation is as follows.

$$x(n) = \sum_{i=0}^{Q} d_i v(n-i) \qquad 5.4$$

For Q=0 we have all pole model, denoted by AP(P) and is known as auto regressive model and input-output difference equation is as.

$$x(n) = -\sum_{i=1}^{P} a_i x(n-i) + d_o v(n) \qquad 5.5$$

For the stabilization of auto regressive filter, all the roots of the characteristic equation should be inside the unit circle in the Z domain (Fig 5.6. Hence the equation of AR process generator is as.

$$1 + a_i z^{-1} + a_2 z^{-2} + a_3 z^{-3} \ldots\ldots a_N z^{-M} = 0 \qquad 5.6$$

In order to analyze this unknown auto regressive process and to regenerate the input of the auto regressive filter, the inverse $H_1(z)$ filter need to be designed, known as analysis or whitening filter. Here all zero filter is used as whitening filter also known as moving average filter or FIR filter.

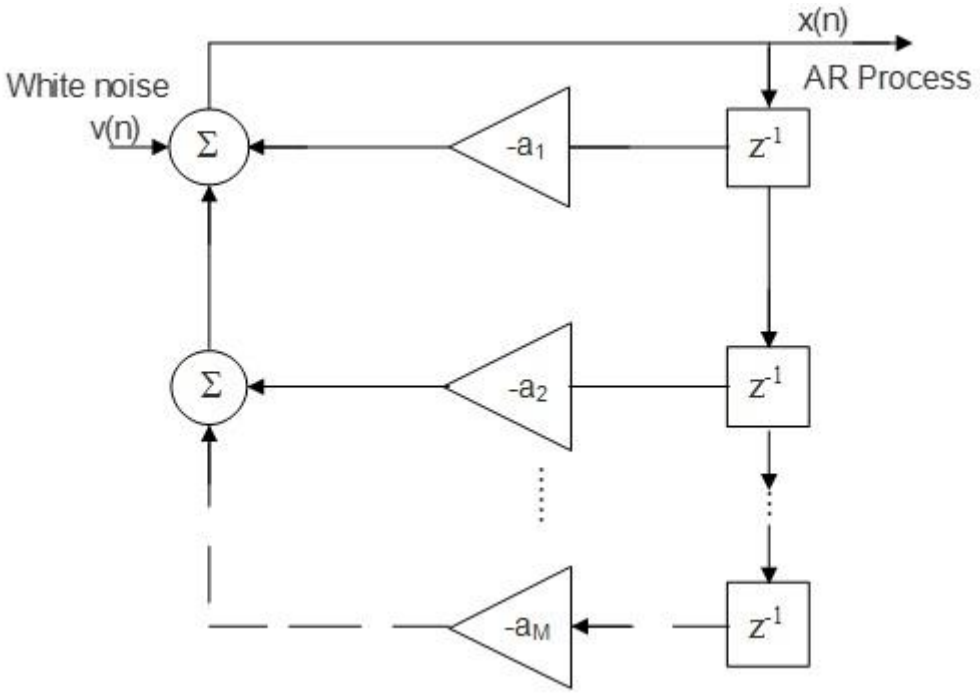


Fig 5.4 AR synthesizer or coloring filter

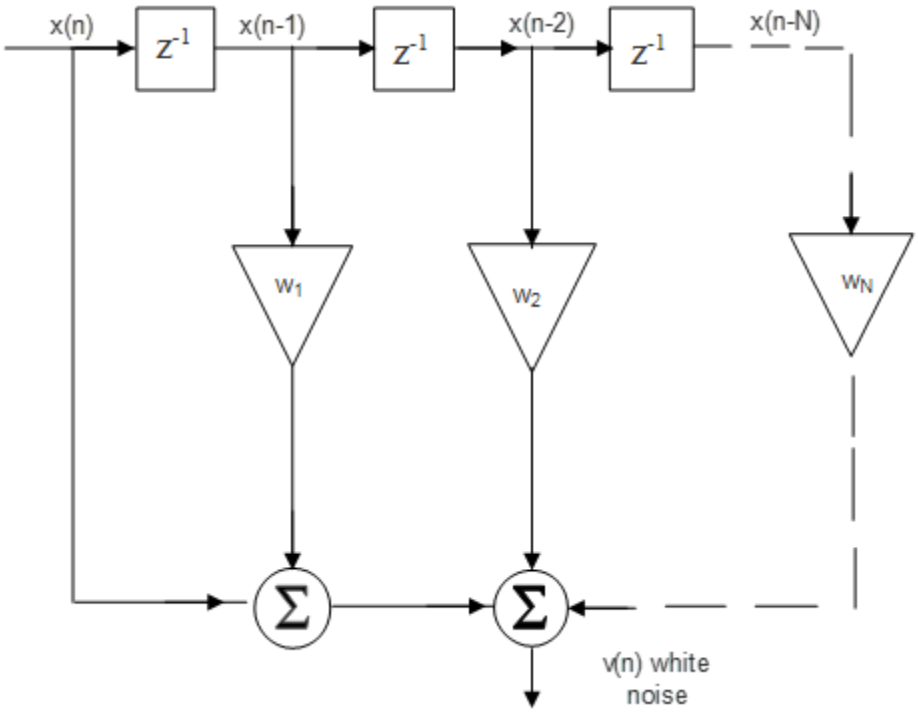


Fig 5.5 AR analyzer / MA filter

5.5 Relationship between moving average filter and forward prediction error filter.

A forward predictor filter can be defined as predictor that represents the linear combination

Of the part sample of input signal i.e. (x (n-1), x (n-2)… x (n-M)) it can be seen as the realization of MA filter having M unit delays as well as top weight. In which the estimated output $\hat{y}(n)$ of the forward predictor is shown as the prediction of all input signal x (n) i.e.

$$\hat{y}(n) = \sum_{1=1}^{M} w_i x(n-i) = W^T X \qquad 5.7$$

Here,

$$W = [\, w_1 \;\; w_2 \;\; \dots\dots\dots w_M \,]^T \qquad 5.8$$

$$X = [\, x(n-1) \;\; x(n-2) \dots\dots\dots x(n-M)]^T$$

The difference between the estimated output-signal $\hat{y}(n)$ and required signal x (n) can be defined as the predictor error e (n).

Hence

$$e(n) = x(n) - \hat{y}(n) \quad 5.9$$

The predictor error filter can be expressed as

$$e(n) = x(n) - \sum_{1=1}^{M} w_i x(n-i) \quad 5.10$$

$$e(n) = \sum_{1=0}^{M} w_{fi} x(n-i) \quad 5.11$$

$$w_{fi} = 1 \ , for \ i = 0$$

$$w_{fi} = w_i \ \ , for \ i \geq 1 \quad 5.12$$

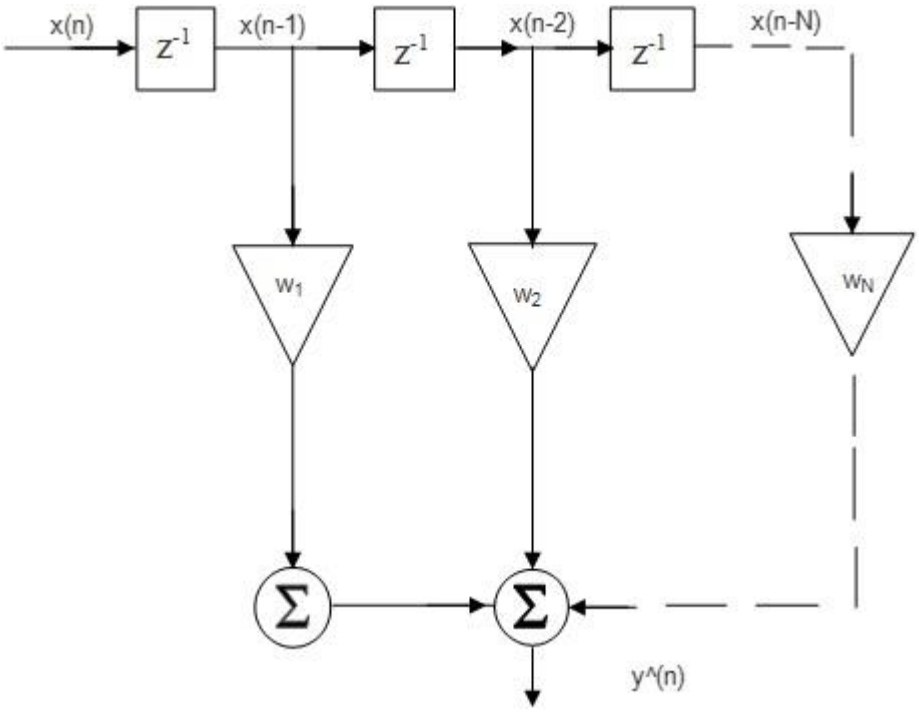


Fig 5.6 One step ahead forward predictor

It is shown in fig that the size of the PEF is one more than the size of the one step ahead forward prediction filter. While having equal no of delay elements and having same order. Hence, the relationship between forward predictor and moving average filter is illustrated. After getting the model of prediction error filter we need to find the tap weight of the filter and for getting that we need an analytical calculation of the linear system equation. For the optimal calculation of the filter top weight adaptive algorithms like least mean square (LMS) can be used. Which also reduces the

complexity in computation. Hence, the actual signal can be regenerated by applying an adaptive prediction error filter to predict the auto regressive process. The output to input difference equation of AR process is found to be of same form as that of the difference equation of a prediction error filter. Hence, the AR identifies can be realized using the forward prediction filter.

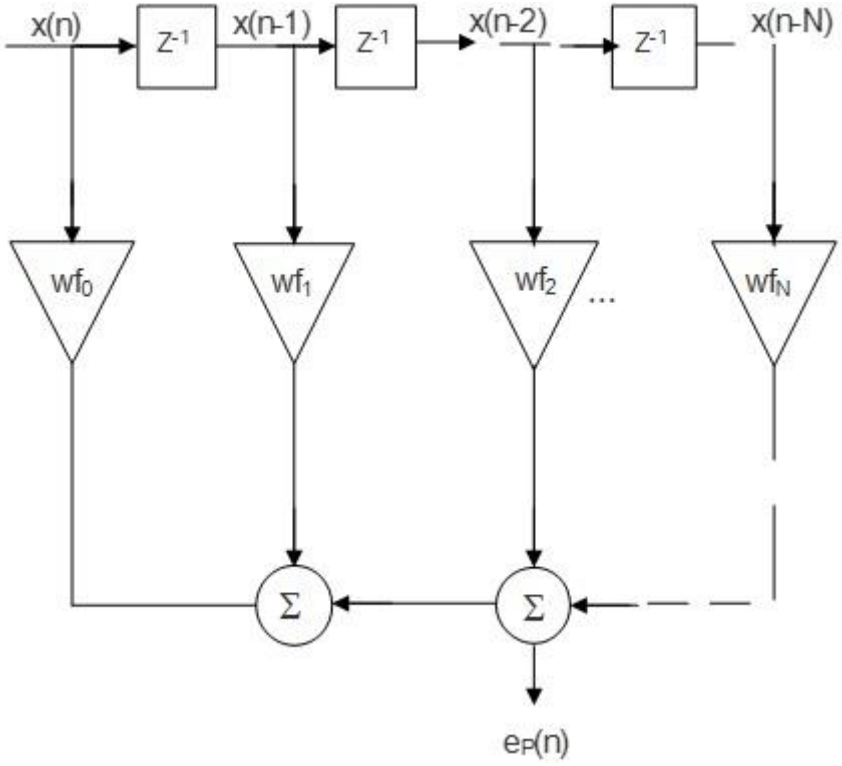


Fig 5.7 Forward predictor error filter

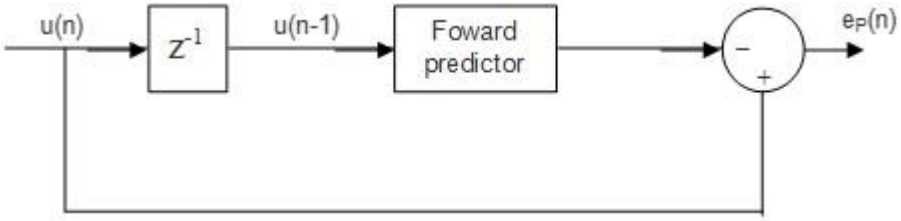


Fig 5.8 Prediction error filter

5.6 One tap linear FIR Predictor for PD compensation

Equation 5.1 represents the difference equation of a digital FIR filter or moving average filter. On writing that difference equation in z domain we get the equation of digital filter as

$$\hat{Y}(z) = X(z)(w_1 z^{-1} + w_2 z^{-2} + \cdots + w_N z^{-N}) \quad 5.13$$

By using the predicted error equation as given in 5.6, the FIR prediction error filter can be realized in z domain by equation.

$$\frac{E_p(z)}{X(z)} = (1 + w_1 z^{-1} + w_2 z^{-2} + \cdots + w_N z^{-N}) \quad 5.14$$

A second order digital filter can compensate the DC –DC converter systems satisfactorily, but in case of buck converter which is a second order minimum phase system, a classical moving average filter just by using the β parameters of the Pole placement controller as:

$$G_c(z) = \frac{\beta_0+\beta_1 z^{-1}+\beta_2 z^{-2}}{(1-z^{-1})(1-az^{-2})} = \frac{D(z)}{E(z)} = \beta_0 + \beta_1 z^{-1} + \beta_2 z^{-2} \quad 5.15$$

The Predictor error filter presented by Kelly and Rinne is made equivalent to the pole placement controller topology by making the order of the Predictor error filter one les that that of the buck converter. On comparing the two equation given in a FIR predictor error filter of lower order can be approximated and realized as a fain controlled controller.

$$\beta_0 + \beta_1 z^{-1} = K_d(1 + w_1 z^{-1}) \quad 5.16$$

The above equation is similar to a proportional derivative compensator and require one extra multiplication and addition operation. For a better regulation and stability the poles should be placed optimally inside the unit circle of z - domain. The two stage adaptive error filter have two different purpose. In the first stage the fir tries to minimize the error between the output and desired voltage by putting a zero close to the dominant pole of the AR model by using adaptive algorithm such as LMS while the second stage FIR filter, the proportional derivative gain Kd is estimated by the adaptive LMS algorithm such that the prediction error get minimized in the adaptive filter. The approach used for adaptation of signals is same in both the stages the only difference is that in the first stage voltage error signal act as an input signal while in case of stage 2 FIR the predicted error signal $e_1(n)$ is used as input signal . At last because of the adaptive tuning of derivative gain K_d and filter weight w_1 the prediction error variation is decreased which effects the output duty cycle. Ab

integral compensator is implemented along with this adaptive PD compensator forming a PD I configuration which results in a less complex adaptive controller. the controller gives a better voltage regulation by getting the optimal values of control parameters without having an exact knowledge of actual circuit parameters .

5.7 Least Mean Square algorithm

In order to estimate the parameter of a system optimally, the adaptive filter algorithm needs to find the solutions of equation given by $W = R^{-1}P$. We can solve the equation by using the gradient descent method in which a line search topology is performed in the direction which is negative to the gradient vector of minimizing function.

$$p = -g = -\nabla f(w) = -\frac{\partial f(w)}{\partial w} \quad 5.17$$

Hence the recursive equation for updating filter weights becomes as follows:

$$w(n+1) = w(n) + \frac{1}{2}\mu P_n, \quad n = 0,1,\cdots, \quad 5.18$$

Here, μ , w and p are step size tap weights of filter vector and direction vector respectively. So upon substituting (5.17) in (5.18) , the recursive update of tap weights can be seen as:

$$w(n+1) = w(n) + \frac{1}{2}\mu g_n, n = 0,1,\cdots, \quad 5.19$$

$$E[e^2(n)] = E[d_r(n)[-w^T u(n)]^2 = E[d_r^2(n)] - 2w^T E[u(n)u^T(n)]w \quad 5.20$$

The above equation can be further written as:

$$E[e^2(n)] = E[d_r^2(n)] - 2w^T\beta + w^T Rw \quad 5.21$$

Here

$$R = E[u(n)u^T(n)] \quad \text{Autocorrelation matrix} \quad 5.22$$

$$\beta = E[d_r(n)u(n)] \quad \text{Cross correlation matrix} \quad 5.23$$

From the equation (5.20), it is clear that there can only be one solution fir minimizing the mean square error as it is a quadratic function of tap weights which can only be found at its optimal value. By making the gradient of w equals to zero the optimal value of tap weights are calculated

$$g_n = \frac{\partial E[e_P{}^2(n)]}{\partial w} = -2\beta + 2Rw \quad 5.24$$

$$g_n = 2(Rw - \beta) = 0 \Rightarrow w_{opt} = R^{-1}\beta \quad 5.25$$

Where, the optimal solution of above equation is w_{opt} and is called as wiener solution. The updated filter coefficients can be found by substituting eqn (5.25) in eqn (5.19) and can be written as:

$$w(n+1) = w(n) - \mu R w(n) + \mu\beta \quad 5.26$$

Hence in order to find the optimal value of tap weights, the gradient vector need to be computed after each iteration and after that it is updated using equation (5.26) . But, the solution of R and is not available for the practical realization hence, the actual values of R and β can be replaced by their instantaneous values:

$$\hat{R} = u(n)u^T(n) \quad 5.27$$

$$\hat{\beta} = d_r(n)u(n)$$

By using the above in equation (5.25), it can be written as

$$\begin{aligned} g_n &= 2(-d_r(n)u(n) + u(n)u^T(n)w(n) \\ &= 2u(n)u^T(n)w(n) - d_r(n) \quad 5.28 \\ &= -2e(n)u(n) \end{aligned}$$

On substitution (5.27) in equation (5.26) the updated filter coefficients can be realized as:

$$w(n+1) = w(n) + \mu e(n)u(n) \quad 5.29$$

It is understood that the Least Mean Square is a simple and less complex algorithm. But, the major disadvantage of the LMS algorithm is its speed of convergence because the rate of convergence of this algorithm is controlled only by its step size μ. It is seen that the convergence rate have inverse relation with the step size which suggest that if the step size if greater there would be fast convergence but of the cost of less stability whereas on the other side the system will be more stable with low convergence rate when the step size is small .

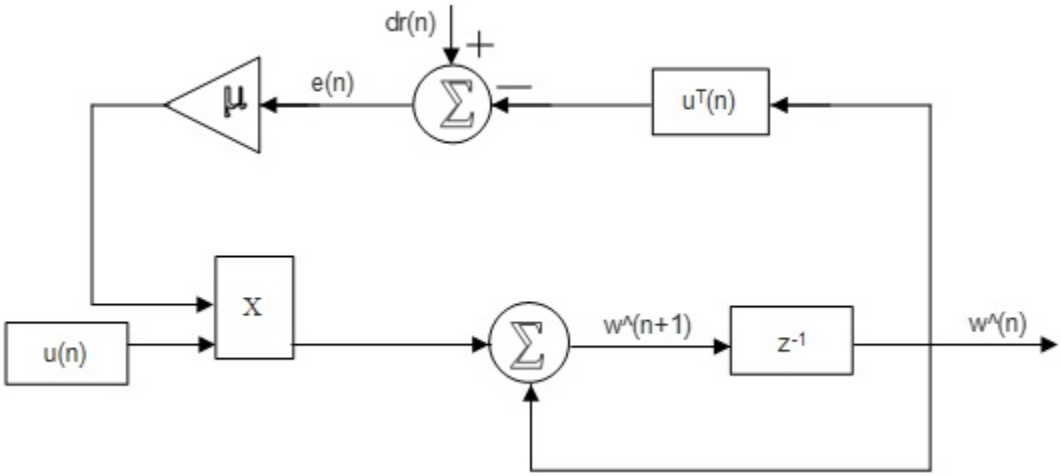


Fig 5.9 closed loop diagram of LMS algorithm

5.8 Simulation results

For voltage controlled buck converter the discussed adaptive controller with one tap predictor error filter using LMS adaptive algorithm is simulated to see the response is varying load conditions. The parameters of buck converters are as follows:

Inductor and capacitor value of L-C low pass filter is $L = 225\ \mu H$, $C = 330\ \mu F$ respectively. The value of parasitic taken are, $R_L = 65\ m\Omega$, $R_C = 25\ m\Omega$. Here the input voltage is 10 volt $V_{in} = 10\ V$ having a load $R = 5\Omega$.

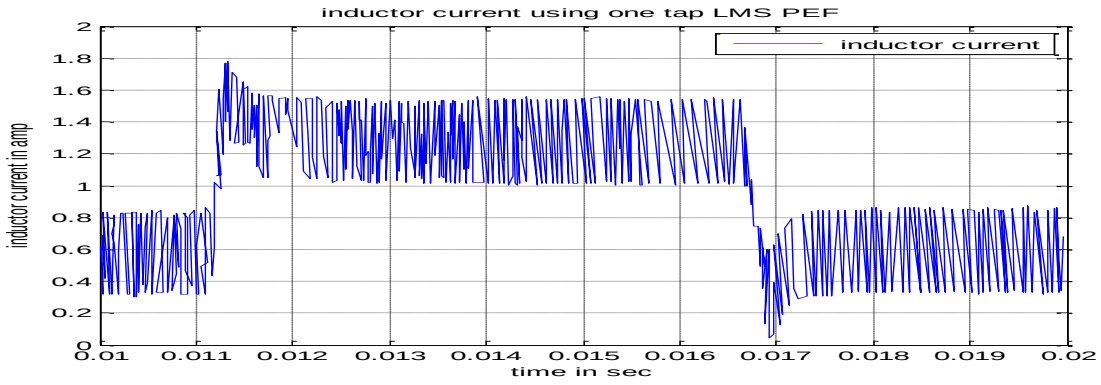


Fig5.10 Inductor current of buck converter with adaptive controller

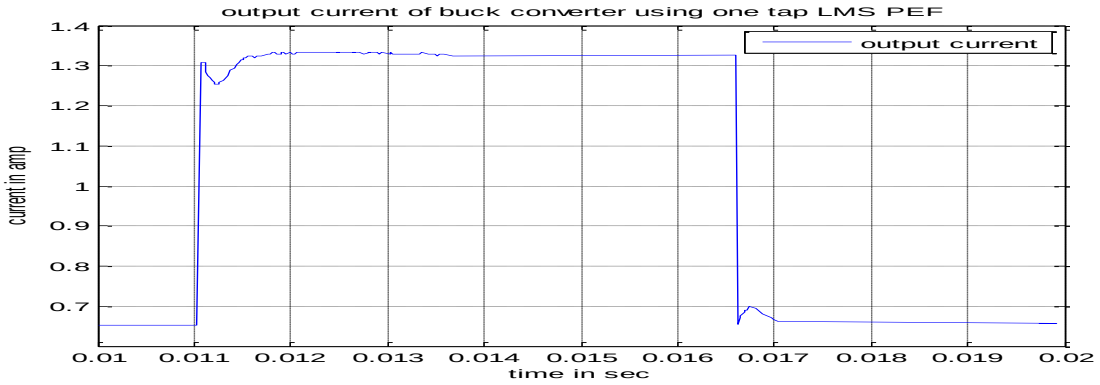


Fig 5.11 Load current of buck converter with adaptive controller

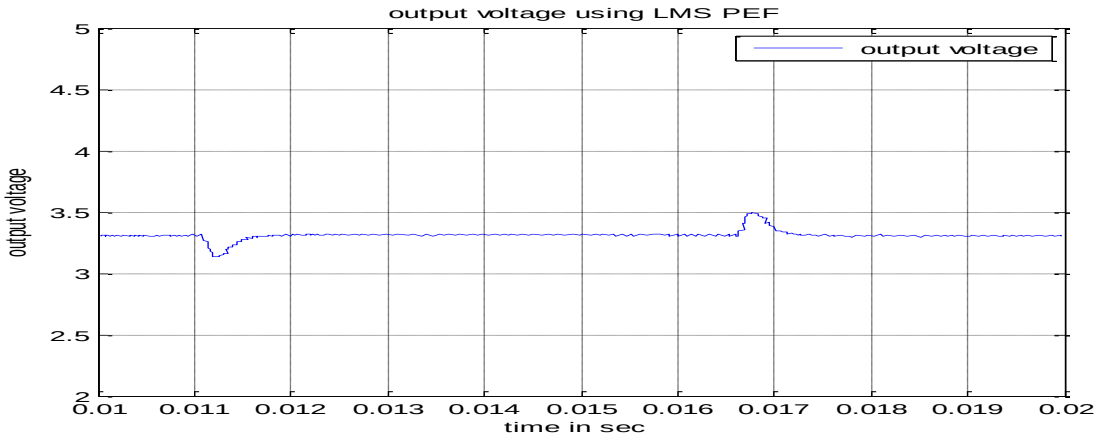


Fig 5.12 Output voltage of buck converter with adaptive controller

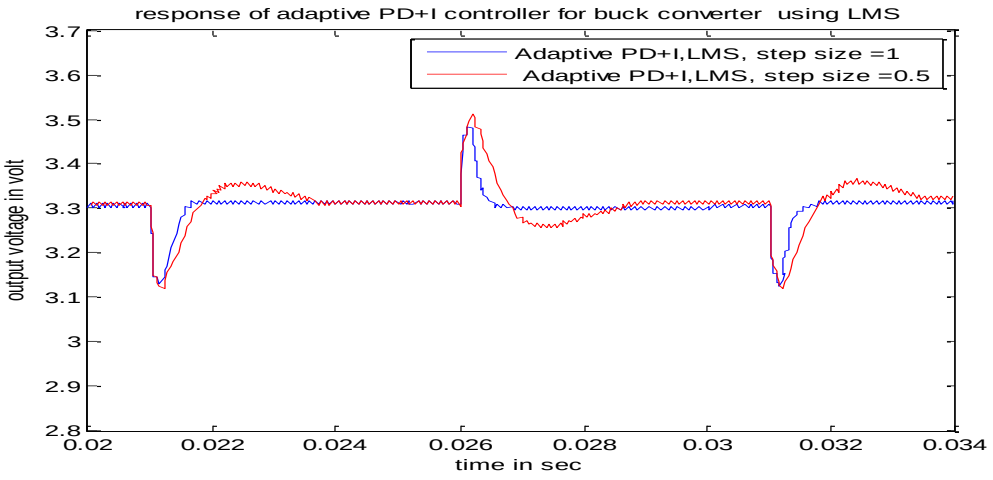


Fig 5.13 output voltage for different step size having reference voltage of 3.3 volt

Discussion

As mentioned in above sections, in the LMS algorithm the step size can account for some problem, as it compromises between fast convergence rate and the accuracy of estimation and it is also necessary to ensure that the step size should always be in the range where the Filter tap weights attain their optimal value as the tap weights or adaptive gain of LMS filter, the tap gradient noise, stability of the adaptation as well as the convergence rate mainly depend on the step size. Lower values of step size decreases the gradient size but increases the convergence time while the large value of step size improves the dynamic performance by decreasing convergence rate and vice versa. Fig 5.10, 5.11 shows the variation of inductor current as well as load current. It can be seen from the Fig 5.12 that the adaptive controller using LMS algorithm provide better voltage regulation than that of the PID based on pole placement and pole zero cancellation approaches with very less ripple . Fig 5.13 shows the effect of step size on the output voltage response and as said above the higher value of step size gives better dynamics.

Chapter 6

CONCLUSION

Common circuit topologies of dc-dc converters with focus on the buck dc-dc converter configuration and circuit operation were demonstrated. The mathematical modelling in continuous and discrete time domain of the buck converter was explained. In addition, this paper provided information on the actual linear state space and linear average model of buck dc-dc converters, with most of the emphasis on the modelling of the control-to-output voltage transfer function of dc-dc buck converter. Therefore, the digital voltage mode control architecture of the buck dc-dc converter was demonstrated and an overview of each block in this structure was highlighted. For the digital control of the buck converter, two techniques of control loop design were explained, the pole-zero cancellation method and the pole-placement approach. From the MATLAB simulation results it can be understood that both the digital control perform satisfactorily with the load variation and track the reference voltage instead of varying load it is also observed that the pole zero cancellation approach gives better dynamic performance with less settling time and less overshoot as compared to that of pole placement approach . Furthermore and adaptive control technique using one tap LMS predictor error filter is implemented. Finally, the proof of concepts for the most important aspects were analyzed and simulated.

REFERENCES

[1] R. W. Erickson, fundamentals of power electronics, fifth edition, U.SA, Kluwer Academic Pub, 2004

[2] M. Shirazi, R. Zane, and D. Maksimovic, "An Auto tuning Digital controller for DC-Dc power converter based on online frequency- response measurement," *IEEE Transaction on power electronics*, vol. 24 pp. 2578-2588, 2009.

[3] B. Miao, R. Zane, and D. Maksimovic, " Automated Digital controller design for switching converter," in *IEEE power electronics specialist conference (PESC 2005*), 2005,pp. 2729-2735.

[4] M. Algreer, M. Armstrong,, and D. Giaouris," Active on-line system identification of switch mode DC-DC power converter based on efficient recursive DCD-IIR adaptive filter," *IEEE transaction on power electronics, 2012.*

[5] M. Algreer, M. Armstrong, and D. Glaouris," System identification of PWM DC-DC converter during abrupt load changes," in *IEEE industrial electronics conference (IECON, 2009), 2009.*

[6] M. Aigreer, M. Armstrong,, and D. Glaouris," Adaptive control of a switch mode DC-DC power converter using a recursive FIR predictor," in *5th IET international conference on power electronics, machines and drives (PEMD 2010), 2010.*

[7] M. Aigreer, M. Armstrong,, and D. Glaouris," Adaptive PD+I control of a switch mode DC-DC power converter using a recursive FIR predictor*," IEEE transaction on industry application*, vol 47, pp. 2135-2144 , 2011.

[8] M. Aigreer, M. Armstrong, and D. Glaouris," Predictive PID Controller for DC-DC converter using an adaptive prediction error filter." In *7th IET international conference on power electronics, machines and drives (PEMD 2012), 2012*.

[9] D. Maksimovi and R. Zane," Small-signal discrete-time modelling of digitally controlled PWM converters*," IEEE transactions on power electronics*, vol. 22, pp 2552-2556, 2007.

[10] A. J. Frosyth and S. V. Mollow," Modelling and control of DC-DC converter," *power engineering journal*, vol. 12, pp. 229-236, 1998 .

[11] M. M. Peretz and S. Ben- Yaakov, "time domain design of digital compensators for PWM DC-DC converter," *IEEE transaction on power electronics.* vol.27, pp. 284-293.

[12] A. Kiam Heong, G. Chong and L. Yun," PID control system analysis, design, and technology," *IEEE transaction on control system technology.*

[13] A. Kelly and K. Rinne." Control of DC-DC converters by direct pole placement and adaptive feedforward gain adjustment," *in IEEE applied power electronics conference and exposition (APEC 2005*), 2005.

[14] K. J. A. and B. Wittenmark, adaptive control: Addison- Wesley publishing company, 2000.

[15] S. S. Haykin, adaptive filter theory, 4th ed. Upper saddle river, NJ: prentice hall, 2006.

[16] A. Kelly and K. Rinne." A self-compensating adaptive digital regulator for switching converters based on linear prediction," *in IEEE applied power electronics conference and exposition (APEC 2006),* 2006.

[17] M. M. Peretz and S. Ben-Yaakov, "Time-domain identification of pulse-width modulation converter," *IET power electronics, vol. 5, pp*. 166-172, 2012.

[18] M. Shirazi, R. Zane, and D. Maksimovic," An autotuning digital controller for DC-DC converter based on online frequency-response measurement," *IEEE transactions on power electronics, vol. 24, pp. 2578-2588, 2009.*

[19] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni," Autotuning of digitally controlled DC-DC converters based on relay feedback*," IEEE transactions on power electronics, vol. 22, pp. 199-207, 2007.*

[20] M. Ned, T. M. Undeland, and W. P. Robbins, power electronics: converters, applications and design, 3rd Edison.: john wiley & sons, Inc., 2003.

[21] D. Maksimovic and R. Zane," Small-signal discrete-time modelling of digitally controlled PWM converters," *IEEE transactions on power electronics*. Vol. 22, pp. 2552-2556, 2007.

[22] A. J. Foryth and S. V. Mollov," Modelling and control of DC-DC converter," power engineering journal. Vol. 12, pp. 229-236, 1998.x

[23] S. Abe, M. Ogawa, T. Zaitsu, S. Obata, M. Shoyama, and T. Ninomiya," Power stage frequency response cancellation of DC-DC converter with digital control," in *International symposium on power electronics electrical drives automated and motion (SPEEDAM)*, 2010, pp. 44-49.

[24] M. M. Peretz and S. Ben-Yaakov, "Time-domain design of digital compensators for PWM DC-DC converter*," IEEE transactions on power electronics, vol. 27*, pp. 284-293.

[25] D. M. Van de Sype, K. De. Gusseme, F. M. L. L. De Belie, A. P. Van den Bossche, and J. A Melkebeek,"small-signal z-domain analysis of digitally controlled converter," *IEEE transactions on power electronics, vol. 21, pp*. 470-478, 2006.

[26] M. M. Peretz and S. Ben-Yaakov, "Time-domain identification of PWM converter for digitally controllers design," *in IEEE power electronics specialists conference (PESC 2007), 2007*, pp. 809-813.

[27] Z. Zhao, "Design and practical implementation of digital auto-tuning and fast response controllers for low-power switch mode power supplies," PhD thesis, University of Toronto, 2008.

[28] Y. Duan and H. Jin," Digital controller design for switch mode power converters," *in IEEE applied power electronics conference and exposition (APEC 1999*), 1999, pp. 967-973, vol. 2.

[29] T. W. Martin and S. S. Ang," Digital controls for switching converters," in *IEEE International symposium on industrial electronics (ISIE 1995)*, 1995, pp.480-484, vol. 2.

[30] A. Kelly and K. Rinne," Sensorless current-mode control of a digital dead-beat DC-DC converters," in *IEEE applied power electronics conference and exposition (APEC 2004) 2004*, pp. 1790-1795, vol. 3.

[31] L. Corradini, P. Mattavelli, W. Stefanutti, and S. Saggini,"Simplified model reference-based autotuning for digitally controlled SMPS,"*IEEE transactions on power electronics, vol. 23, pp. 1956-1963,* 2008.

[32] V. P. Arikatla and J. A. Abu Qahouq,"Adaptive digital-proportional-integral-derivative controller for power converters," *IET power electronics, vol. 5,* pp. 341-348, 2012.

[33] A. Kiam Heong, G. Chong, and L. Yun," PID control system analysis, design, and technology*," IEEE transactions on control system technology*, vol. 13, pp. 559-576, 2005.

[34] V. Yousefzadeh and S. Choudhary," nonlinear digital PID controller for DC-DC converters," *in IEEE applied power electronics conference and exposition (APEC 2008),* 2008, pp. 1704-1709.

[35] Y. F. Liu, E. Meyer, and X. Liu," Recent developments in digital control strategies for DC-DC switching power converters," *IEEE transactions on power electronics, vol. 24, pp*. 2567-2577, 2009.

[36] H. Al-Atrash and I. Batarseh," Digital controller design for a practicing power electronics engineer," in *IEEE applied power electronics conference (APEC 2007),* 2007, pp. 34-41.

[37] A. Kelly and K. Rinne." Control of DC-DC converters by direct pole placement and adaptive feedforward gain adjustment," in *IEEE applied power electronics conference and exposition (APEC 2005), 2005, pp*. 1970-1975, vol. 3.

[38] L. S. Xuefang, F. Morel, B. Allard, D. Tournier, J. M. Retif, and G. Shuibao," A digital-controller parameter-turning approach, application to a switch-mode power supply," in *IEEE international symposium on industrial electronics (ISIE),* 2007, pp. 3356-3361.

[39] B. Widrow and G. L. Piett," Adaptive inverse control based on linear and nonlinear adaptive filtering," in international workshop on neural network for identification, control, robotics, and signal/image processing, 1996, pp. 30-38.

[40] S.S Haykin, Adaptive filter theory, 4th edition. Upper saddle river, NJ: prentice hall, 2002.