DESIGN OF LOW POWER FULL ADDER USING DIFFERENT HYBRID LOGIC STYLES

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Bachelor of Technology in Electronics and Instrumentation

And

Master of Technology

in

VLSI Design and Embedded Systems

Submitted By

Sompary Srinivas Kumar

Department of Electronics and Communication Engineering

National Institute of Technology Rourkela, India.

2016

DESIGN OF LOW POWER FULL ADDER USING DIFFERENT HYBRID LOGIC STYLES

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Bachelor of Technology in Electronics and

Instrumentation

And

Master of Technology

in

VLSI Design and Embedded Systems

Submitted By

Sompary Srinivas Kumar

(710EC2107)

Under the guidance of

Prof. A.K Swain

Department of Electronics and communication engineering

National institute of technology Rourkela, India.

Department of Electronics and Communication Engineering, National Institute of Technology, Rourkela

Certificate

This is to certify that the thesis entitled "Design of low power full adder using different hybrid logic styles" being submitted by Sompary Srinivas Kumar bearing Roll No. 710EC2107 to the National Institute of Technology, Rourkela, in the Department of Electronics and Communication Engineering is a bonafide work carried out by him under my supervision and guidance. The research reports and the results presented in this dissertation have not been submitted in parts or in full to any other University or Institute.

Place: Rourkela

Date: 31-05-2016

Prof. A.K Swain
Dept. of ECE
National Institute of Technology
Rourkela-769008

ACKNOWLEDGEMENT

I would like to express my gratitude to my thesis guide **Assistant Prof. A.K Swain** for his guidance, advice and support throughout my thesis work. I would like to thank him for being my advisor here at National Institute of Technology, Rourkela.

Next, I want to express my respects to **Prof. K. K Mahapatra, Prof. Pramod Kumar Tiwari, Prof. Sarkar** for teaching me and also helping me how to learn. They have been great sources of inspiration to me and I thank them from the bottom of my heart.

I would like to thank to all my faculty members, Phd Scholar **Ramakrishna** and staff of the Department of Electronics and Communication Engineering, N.I.T. Rourkela, for their generous help for the completion of this thesis.

I would like to thank all my friends and especially my classmates for thoughtful and mind stimulating discussions we had, which prompted to think beyond the obvious. I've enjoyed their companionship so much during my stay at NIT, Rourkela.

I am especially indebted to my parents for their love, sacrifice, and support. They are my first teachers, after I came to this world and I have set of great examples for me about how to live, study and work.

Sompary Srinivas Kumar

Abstract

Full adder is a basic and most important digital component. To improve the full adder architecture many improvements has been made. Here we present Hybrid CMOS full adder, ULP (Ultra low power) full adder and two new design full adders that is Hybrid logic style and GDI(gate diffusion input) Structure. These two new full adders consists less number of transistors (i.e.12 transistors) compared to previously designed full adders. The motive of adder cell is to provide high speed, low power consumption and also to give high voltage swing.

The Hybrid CMOS logic full adder and ULP full adder uses CPL logic, transmission gates and Static CMOS logic styles. New hybrid full adder uses semi XOR-XNOR gates and GDI-MUX full adder with a new design which eliminates the use XOR-XNOR gates and also uses GDI (gate diffusion input) cell with 12 transistors provides low power, high speed and also full voltage swing.

Theses design are implemented in Cadence virtuoso software using 90nm technology GPDK tool kit and comparison of Power, Delay and Power delay product (PDP) is done.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

MOTIVATION

THESIS ORGANIZATION

1. Introduction

Addition is one of the common and widely used fundamental arithmetic operation in many VLSI systems. Other similar arithmetic operations are subtraction, multiplication, division, address calculation etc. Using binary adders the full adder is designed and improving 1-bit full adder performance plays an important role in VLSI. Different varieties of full adders exploit completely different logic designs and technologies, which are reported in [1-4], and they unremarkably aim at increasing speed and reducing power dissipation.

To improve the performance of adder there we have two methods. One is 'System Level viewpoint' method and second method is critical Style view point'. In system level viewpoint it consists of finding the longest signal path in the ripple adders and reduce the trail so as to scale back the full signal path delay. The longest signal path is where the carry out bit of the most significant bit has to be calculated in most things. The second method is 'Circuit Style Viewpoint' in transistor level, that is, semiconductor device level design skills are supported by designing of high performance full adder. An optimized design is required to prevent any decrease in signal magnitude, provide small delays, consume less power in critical paths and even at low supply voltage maintain consistency while moving headed for smaller designs such as in nanometer range. Driving capability for different loads, outputs without glitches, layout regularity and interconnection quality should also be looked after.

Nanometer range devices face the problem of hot carrier effects and other short-channel effects. In order to maintain speed, threshold voltage must be scaled down, but doing so standby current increases, which in turn implies that static power is the main contributor to total power and thus should be taken care of properly.

1.2 Motivation:

Power consumption may be a key limitation in several electronic systems, starting from mobile telecommunication to transportable and desktop computing systems. Power is additionally a show stopper for several rising applications like close intelligence and detector networks. Consequently, new design methodologies and techniques are needed to regulate and control power dissipation. From refined handheld devices to bio-electronic circuits and Nano-satellites, all need

low power style. Due to scaling, circuits have become a lot of capable, use a lot of transistors to implement difficult functions and supply new applications to customers. However this implies a lot of power consumption. In some cases, low power style is needed to avoid overheating. There are alternative applications like bio-electronics wherever the circuit would be constituted within the body and has got to work either with small battery or victimization power harvest home techniques. Kind of like that, RFID and growing detector networking circuits even have to consume terribly low power owing to out there power limitation.

In some cases we have a tendency to could contemplate low-power style a second priority, however in those applications lower-power style is important. Thus either supply power limitation or, over heating concern and battery life thought, low power style is that the answer.

To own low power digital processing, a low-power full adder is desired. In terms of power dissipation techniques and also comparison there are few papers and references available. At the design level, some solutions like adiabatic circuits are introduced to reduce power consumption. However, a number of these solutions, like adiabatic, may not be practical as a result of the quantity of transistors they need. A number of these techniques like pipeline structures or asynchronous temporal order turning into additional engaging and obtaining additional attention than other solutions. This is often beside the first and main resolution to cut back the availability voltage. The aim of this analysis is to explore completely different solutions together with circuit techniques and to achieve a sensible low-power design.

1.3 Thesis organization:

This thesis provides design of full adder with new different techniques for lower power consumption, delay and but also increasing speed. Simulation results gives High Speed, low power dissipation, less delay. Thesis can be organized in the following manner. Chapter 2 focuses on C-CMOS and CPL full adder.Chapter3 focuses on hybrid CMOS full adder design and ULPFA full adder design. Chapter 4 focuses on Design of hybrid full adder and GDI-MUX full adder, which are newly proposed. Chapter 5 focuses on Comparison of results .The experimental values of all the results are shown in table.

CHAPTER 2

THEORY OF DIFFERENT STATIC LOGIC STYLES

Full adder circuit is intended for addition binary logics. Sum signal (SUM) and carry out signal (COUT) are the output of I-bit full adder. Each of them are generated by input A, B and CIN following mathematician equation as:

$$Sum=A \oplus B \oplus C_{in}$$

$$C_{out}=AB + BC_{in} + AC_{in}$$

Several completely different static CMOS logic designs are planned to design adder cells with Low power [7, 8].

2.1 C-CMOS

Complementary CMOS structure is constructed using regular CMOS design consists of PMOS pull-up and NMOS pull-down transistors [5-8]shown in figure-1. At the output stage transistors are present in series, which decrease the driving capability of the circuit. Therefore, extra buffers are required for suitable compensation. The benefit of C-CMOS style is improved quality of output in spite of transistor sizing and voltage scaling. It also gives a full voltage swing, which is needed in complex designs. More on, the layout of this design is area efficient and simple attributing to the PMOS NMOS transistor pairs and little variety of interconnecting wires.

2.1.1 Block diagram of C-CMOS full adder

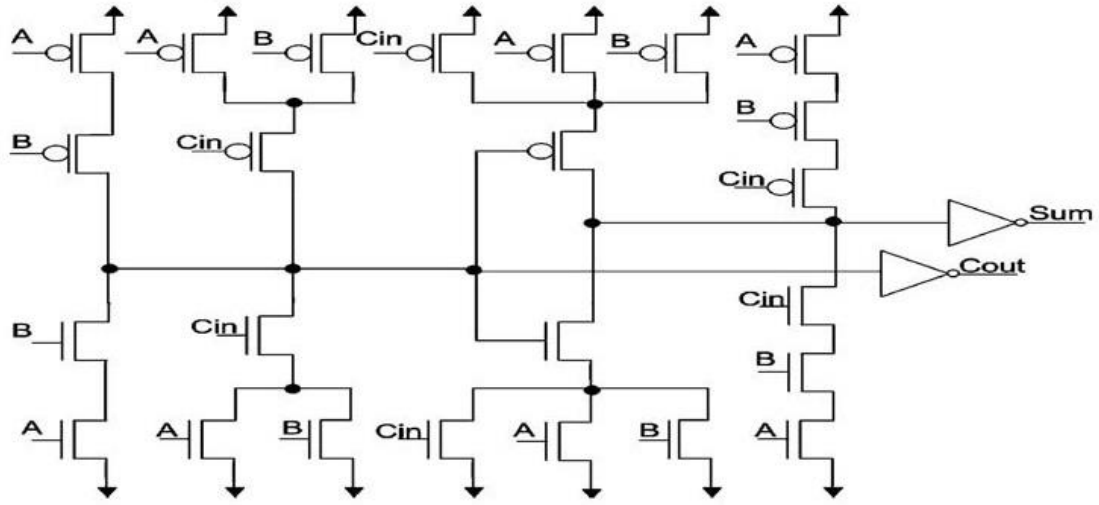

Figure-1 C-CMOS full adder [5]

Schematic diagram of C-CMOS full adder in 90nm technology using Cadence

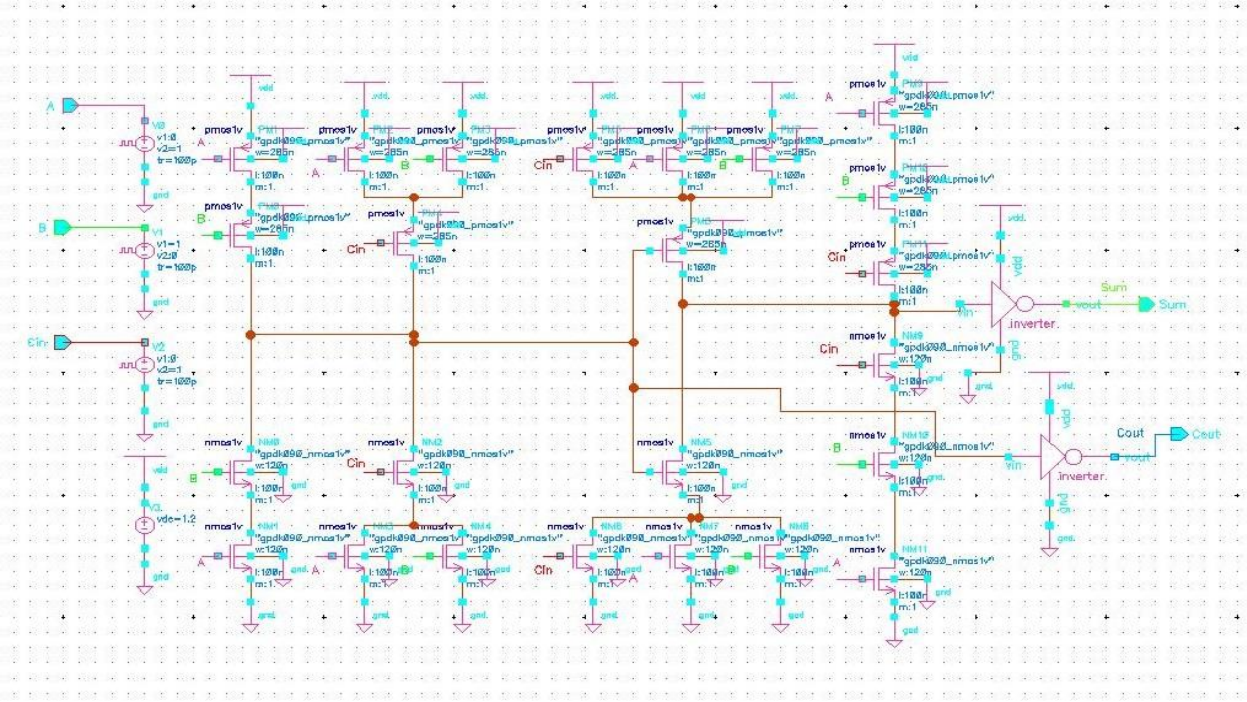

Figure-2 C-CMOS full adder Schematic diagram

2.2 Complementary pass transistor logic

The complementary pass transistor logic (CPL) full adder with swing restoration [5, 6, 8, 9] shown in figure-3 and it consists of 32 transistors with dual rail structure. The complementary transistor and pass transistor logic have some basic difference between them that is source terminal of pass transistor logic is not connected to power, instead it is connected to some input signals. Anyone of the pass transistor either PMOS or NMOS is enough to implement logic function and therefore which results in using of small input load and less number of transistors. The pass transistor logic has weak driving capability because of that output inverters are used for control driving capability.

2.2.1 Block diagram of CPL

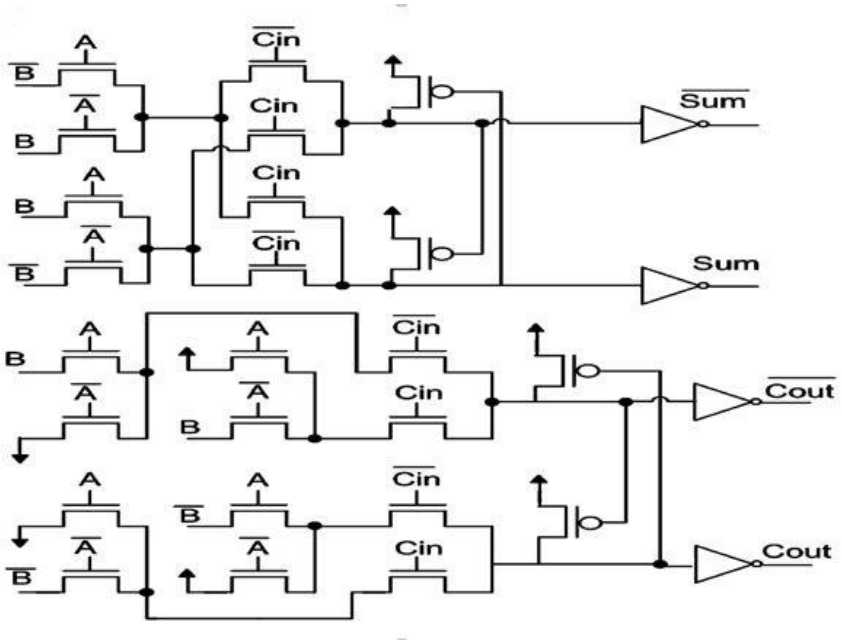

Figure-3 CPL full adder [5]

CPL full adder Schematic diagram in 90m using Cadence

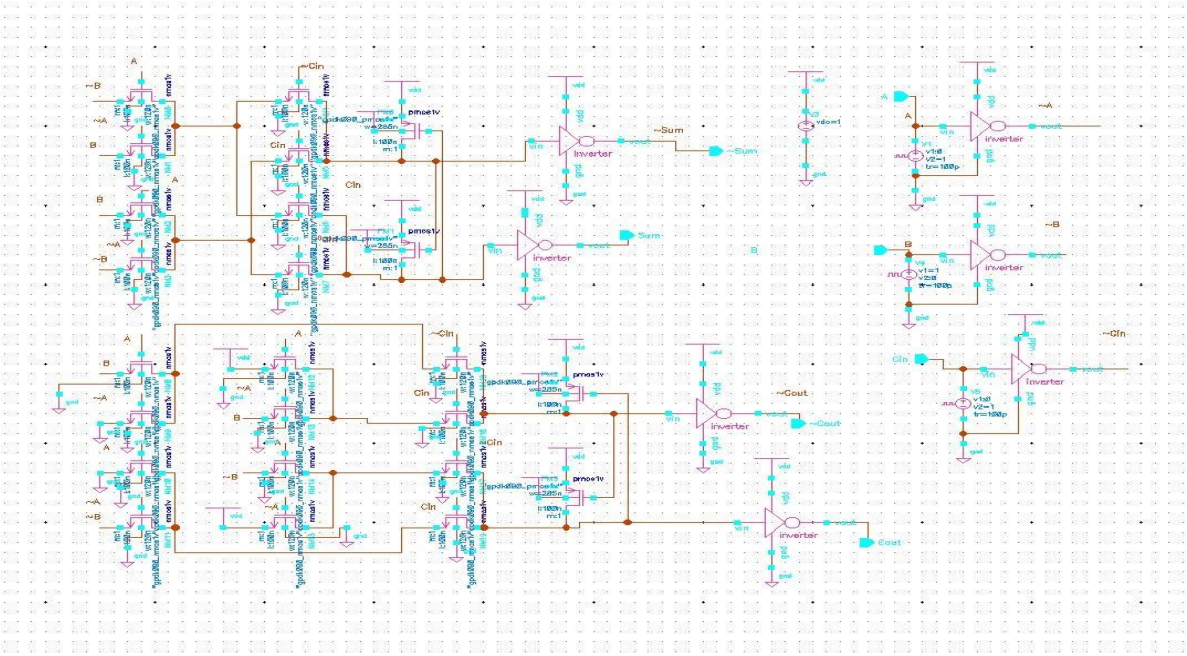

Figure-4 CPL full adder schematic diagram

CHAPTER 3

Theory of Hybrid CMOS and ULPFA full adders

The hybrid logic style uses completely different logic designs so as to make new full adders which gives good desired performance.

3.1 Hybrid CMOS full adder

The design utilizes several types of CMOS logic styles to generate a design of higher efficiency shown in Fig. 5. Module 1 gives fast response due to employment of only NMOS pass transistors, owing to their high mobility, for complementary pass transistor logic (CPL). However, a drawback exists to this design which is that it consumes more power due to employment of CPL designs [5, 8] and inverter. Inverter forms a sole reason for excess power consumption in static CMOS designs.

Module 3 uses an inverter and 4-transistors XOR gate. The design has been realized using pass transistor logic [11] and thus is inherently less power consuming, but decreases the driving capability [10] and hence an inverter is provided at the end to increase the drivability. But introducing an inverter implies that more power has be consumed for the working of this stage.

Module 2 gives out the sum of inputs. This module utilizes 10 transistors both in static CMOS style as well as transmission gate style, and this implies using large PMOS MOSFETs and thus consume large area. Also the input capacitance increases because of PMOS transistors. Moreover, presence of series transistors decreases the drivability and hence an inverter has been introduced to counter this effect. But, it also increase the static power consumption.

3.1.1 Block diagram of Hybrid CMOS full adder

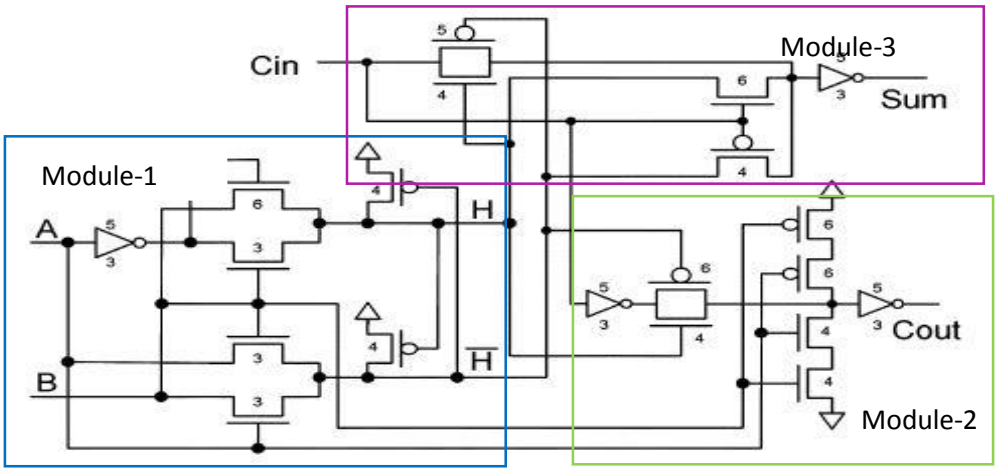

Figure-5 Hybrid CMOS full adder [15]

Schematic diagram of hybrid CMOS full adder in 90nm using Cadence

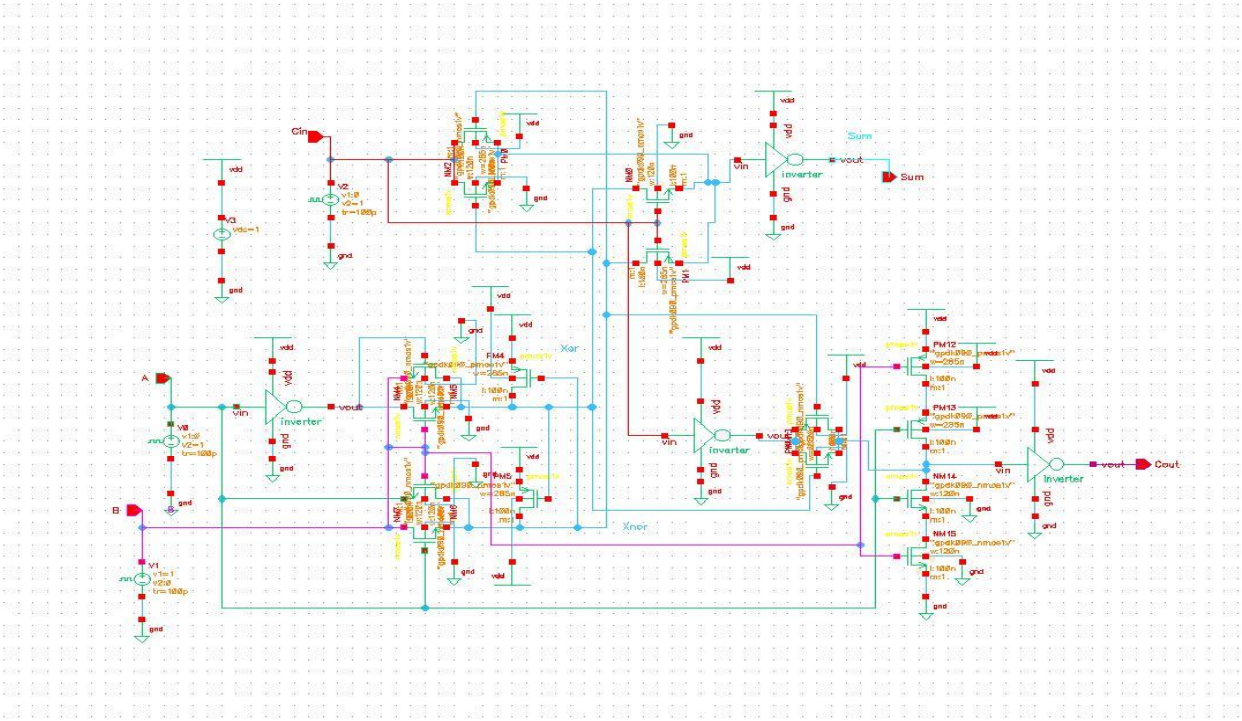

Figure-6 Schematic diagram of hybrid CMOS full adder

3.2 ULPFA

ULPFA design using CMOS logic style and pass transistor logic shown in figure-8. A unique voltage restorer ULPD has been employed in this full adder, which eliminates the need for speed compensations for full swing at outputs, provided in previous designs. Such a setup has been shown in Fig.7.

ULP diode is designed using one PMOS and one NMOS transistors, this diode provides a low leakage current when operated in reverse direction [13].

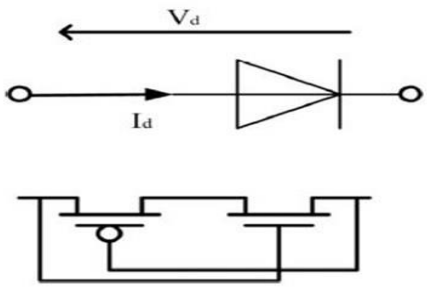

Figure-7 ULP diode [13]

UPLD works as a voltage restorer due to the fact that when a large reverse bias is provided, the reverse current increases due to increased VDS, but again when a maximum value is reached, current decreases due to increased negative value of VGS. Thus, a negative resistance region is formed that can be used for level restoration. Depletion mode PMOS and NMOS transistors have to be used to ensure that in negative resistance region it give high opposite current peaks [12]. For implementation of this paper, depletion mode MOSFETs with threshold voltages of 0.23 V and 0.18 V have been considered for 0.13 um and 90 nm technologies respectively.

For designing a ULP full adder we need low power XOR and XNOR gates [14]. These two gates are used for implementing Sum output with pass transistor logic style and ULP diode voltage level restorer because of this the problems of delay, power dissipation and noise are eliminated. Static CMOS logic style is used for designing Cout circuit .This circuit design is robust against voltage scaling and sizing of transistors. Due to existence of large number of PMOS transistors it uses large space and has high input capacitance. And also at the output series transistors create a weak driver. Moreover to eliminate the extra inverters the inputs of the design to be inverted. This is one drawback of this design due to the combination of two different logics we get non symmetrical and irregular layout for constructing the Sum and Cout.

3.2.1 Block diagram of ULPFA

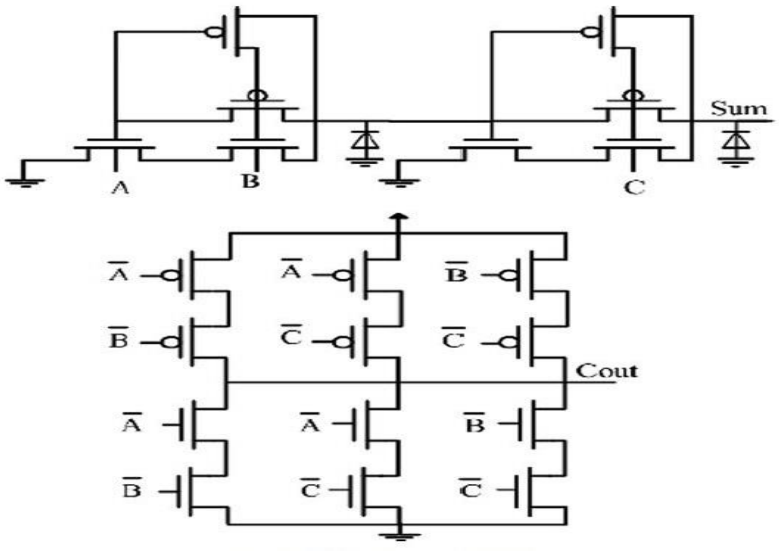

Figure-8 ULP full adder [12]

ULP full adder Schematic diagram inn 90nm using Cadence

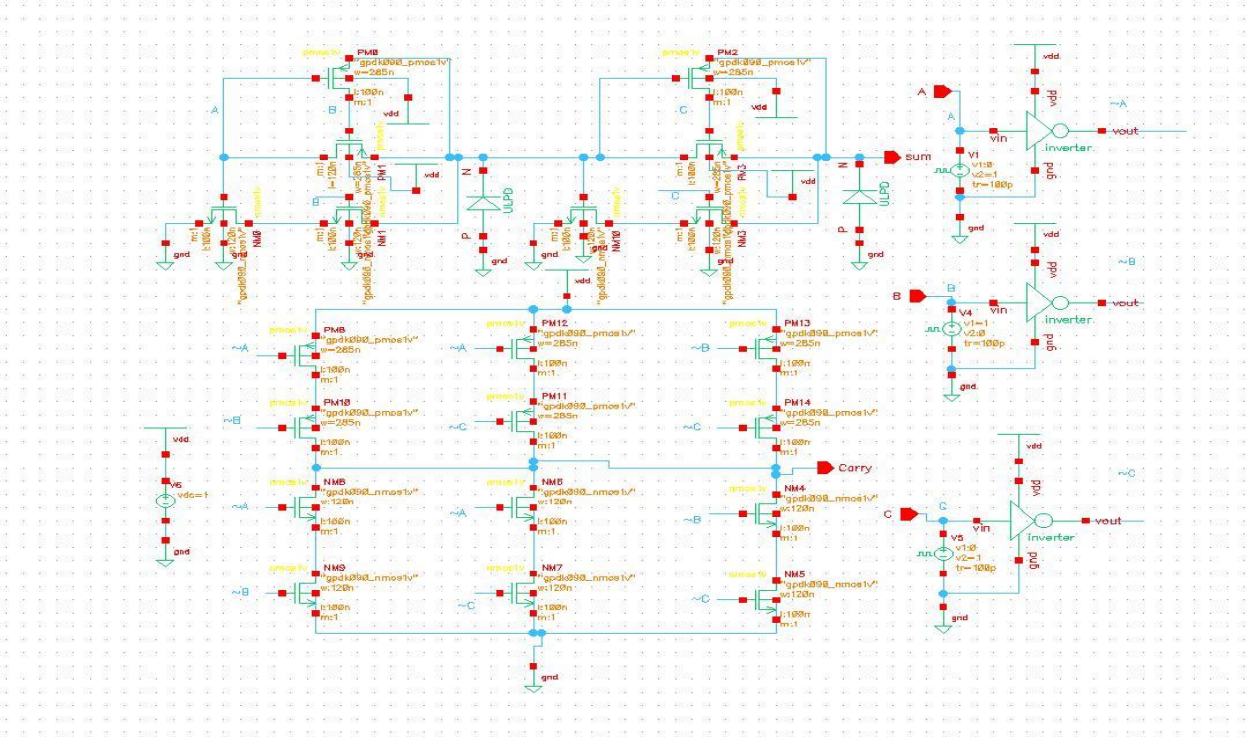

Figure-9 schematic of ULP full adder

Chapter 4

Proposed hybrid full adder circuits

4.1 Hybrid full adder using Semi XOR and Semi $XNOR$

This low power hybrid full adder utilizes a unique approach using Semi XOR-$XNOR$ gates[15], our design shows that Semi-XOR and Semi-$XNOR$ lacks to give possible outputs of normal XOR and $XNOR$. Whose characteristics are provided below in table.

4.1.1 Semi XOR-$XNOR$ gates

Here, a different circuit has been employed for Cout, unlike the Semi XOR-$XNOR$ structure in [2] shown in figure-10, which results in a robust and flexible low power full adder. These two gates Truth table has shown in Table-1.

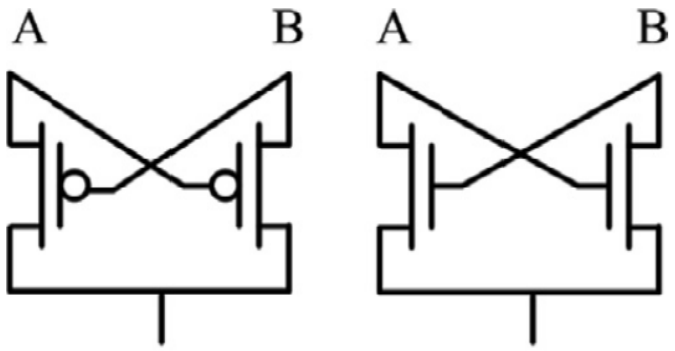

Figure-10 (a) Semi (b) Semi XNOR

Table 1:

Truth table of Semi XOR and Semi XNOR

A	B	Semi XOR	Semi XNOR
0	0	0	HZ
0	1	1	0
1	0	1	0
1	1	HZ	1

Table 2:

Truth table of Sum and C_{out}

A	B	C_{in}	Sum	C_{out}	Semi-XOR	Semi-XNOR
0	0	0	0	0	0	HZ
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	HZ	1
1	0	0	1	0	0	HZ
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	HZ	1

The above mentioned Table-2 shows that the first 4 states can be achieved by using Semi XOR gate and the remaining states can be obtained using Semi XNOR gate. Thus, using a selector, such that for Cin as 0, Semi XOR gate is chosen and for Cin as 1, Semi XNOR gate is chosen, a low power full adder using these gates can be realized.

The circuit shown in Fig. 11 based on the explanation above works fine as long as the output does not tend towards either of the two high impedance cases. One such high impedance output can be prevented by adding an extra NMOS transistor whose source/drain is connected with input Cin and drain/source connected with SUM. This NMOS is switched on in the two situations when Semi XNOR gate gives an output 1, where value of SUM, in these states, becomes equal to Cin. Another high impedance can be removed by introducing a PMOS with its source/drain connected to SUM and drain/source to Cin. The final design for SUM is shown in Fig. 12.

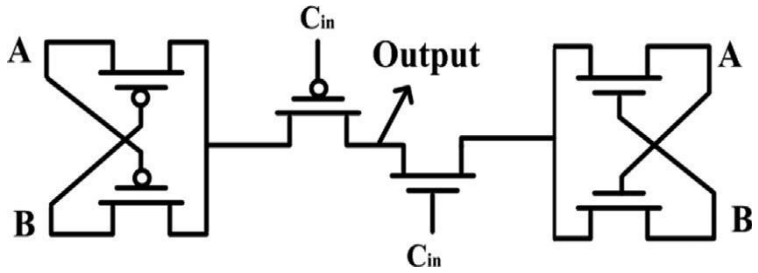

Figure-11 Sum generator cell with incomplete output [15]

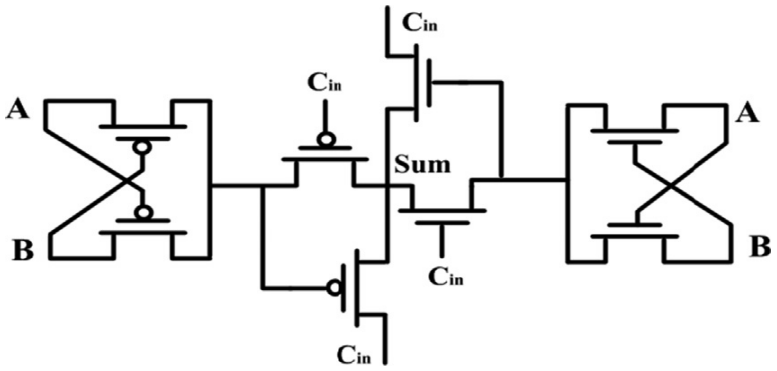

Figure-12 Sum generator with complete output [15]

Now, for designing a circuit for determining Cout, Table 2 shows that first 4 states can be realized through Semi XNOR gate and the rest through Semi XOR gate, except for the two high impedance situations that arise when either both the inputs are 1s or both 0s. First high impedance case, when both inputs are 1s can be rectified by introducing an extra NMOS with its source connected to Cout, drain to Vdd and gate to Semi XNOR output. The second high impedance case, where both inputs are 0s, can be eliminated by connecting a PMOS such that its gate is connected to Semi XOR output, source to Cout and drain to Cin. Fig. 13 shows the adder circuit without compensation for high impedance cases and the final schematic for the above explanation is shown in Fig. 16 as complete full adder [15].

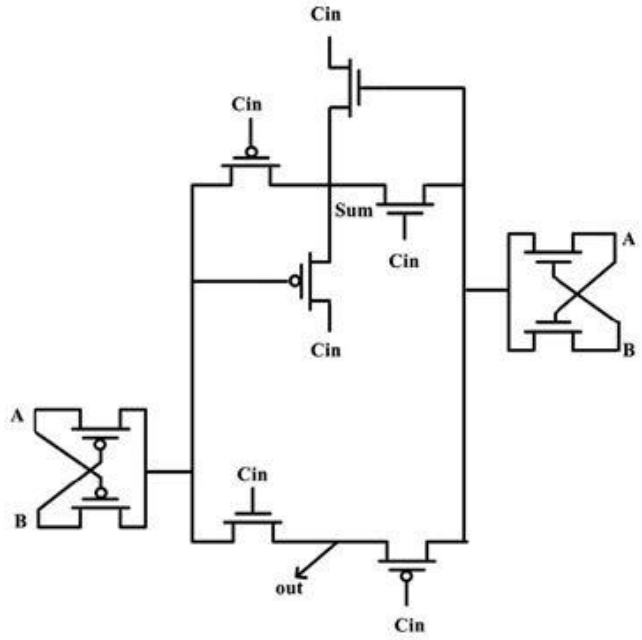

Figure-13 Incomplete full adder cell [15]

Fig. 14 shows the utilization of ULPD at the input terminals [12,13]. This causes a full swing at the output without the requirement of output buffers, which form a main reason for static power consumption. Also ULPD prevents any short-circuit currents owing to the fact that one part of the circuit remains off when the other part starts conducting, thereby removing any chance of direct path between Vdd and ground. ULPD not only prevents leakage currents but also provides good drivability which is essential in cascaded designs and other complex situations.

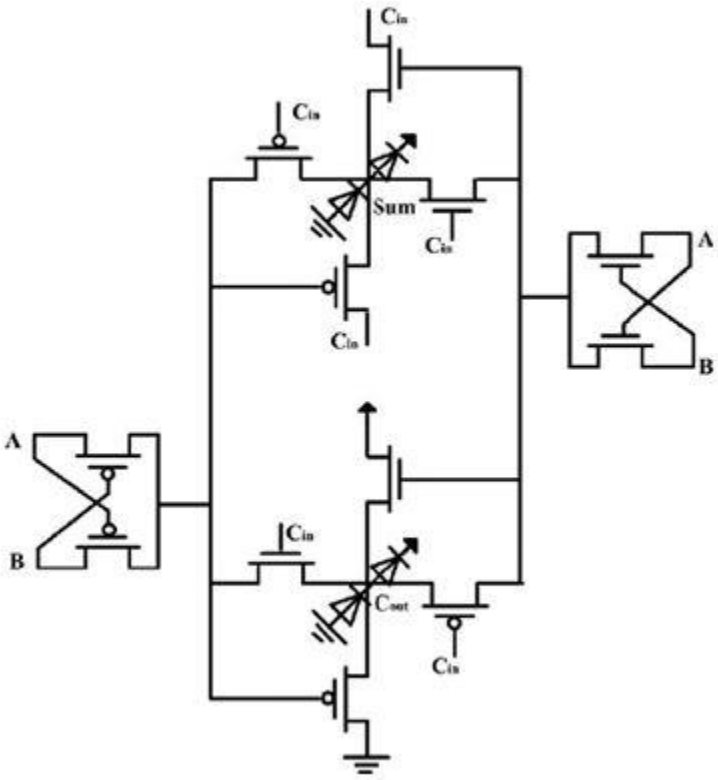

Figure-14 Proposed hybrid full adder [15]

This circuit is made of less number of transistor that is 20 transistor comparing to other circuits, this design provides low dynamic power dissipation. This is because, lower number of transistors implies that there is less amount of switching capacitance and hence low power assimilation. Moreover, this circuit is way faster than its counterparts, because, here, the critical path contains only two transistors which drive the output.

4.1.2 Schematic diagram of hybrid full adder in 90nm using Cadence

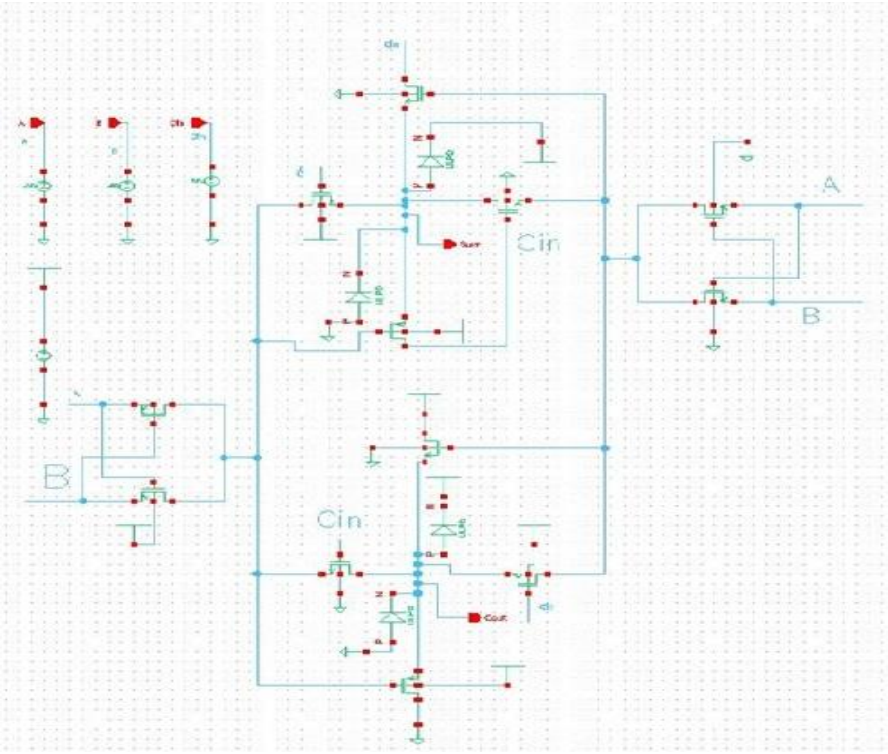

Figure-15 Schematic of hybrid full adder

4.2 GDI-MUX full adder

It is an ultra-low power circuit my using GDI method[15] is implemented and briefly discussed shown in figure-16 .GDI-MUX design is a new approach by eliminating the use of XOR and XNOR gates. Some alternate logic blocks like AND, OR and MUX are used to build a full adder. From Truth Table of a full adder, we can consider that when $C_{in} = 0$, C_{out} is same as the output of (A AND B) and both are equal, when $C_{in} = 1$, C_{out} is same as the output of (A OR B) and both are equal. Therefore to get C_{out} output, multiplexer is used. By following the same method when $C_{out} = 0$ the Sum is same as output of (A OR B OR C_{in}) and both are equal, when $C_{out} = 1$ the Sum is same as the output of (A AND B AND C_{in}) and both are equal. For required condition to select the following particular value C_{out} is used, to driving a multiplexer.

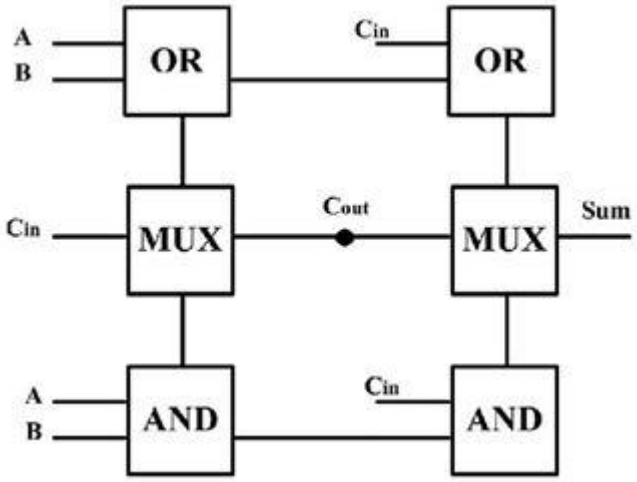

Figure-16 another logical scheme for designing full adder cell [15]

4.2.1 GDI cell

The GDI cell is displayed in figure-17 which consists of one PMOS and one NMOS transistors [16], and Table-3 shows the Truth Table of cell. It has two extra input pins which will used. The cell contains total three inputs P(input to source/drain of PMOS),G(combined gate input of PMOS and NMOS) and N(input to source/drain of NMOS).Both PMOS and NMOS bulks are linked to P or N, so it based on the CMOS inverter. In order to implement GDI design SOI processor is required[16]. It uses less number of transistors as compared to CMOS and pass transistor logic designs.

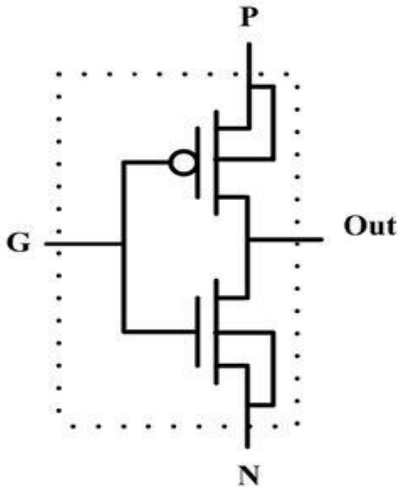

Figure-17 Basic GDI cell [15]

Table-3:

Truth table of basic GDI cell.

N	P	G	Out	Function
0	B	A	$\bar{A}$B	F1
B	1	A	$\bar{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
0	1	A	$\bar{A}$	NOT

The GDI-MUX full adder implementation is shown in figure-18.In Modudule1 (A OR B) implemented by connecting N input to Vdd, G input A and P input to B. Second step is module-2, In this (A AND B) is implemented by connecting N to B, G to A and P to GND. Cin acts as selector which connected to input G of GDI for getting Cout and P is connected to (A AND B) and N is connected to (A OR B) .Module-3 shows the designing of multiplexer, the above mentioned processor is followed here to implement (A OR B OR Cin) .Module-4 is implemented by connecting P to Cin,N to Vdd and G to (A OR B).Module-5 is implemented by connecting P to GND,G to (A AND B) and N to Cin. Finally for getting Sum output G input is connected to Cout and P is connected to (A OR B OR Cin) and N is connected to (A AND B AND Cin) respectively.

This approach minimizes the Power dissipation (both static and Dynamic) because of using UPLD level restorer it removes the current leakage problems and In cascaded series circuits provides good driving capability . GDI-MUX design uses 20 transistors which give low switching capacitance and low dynamic power consumption.

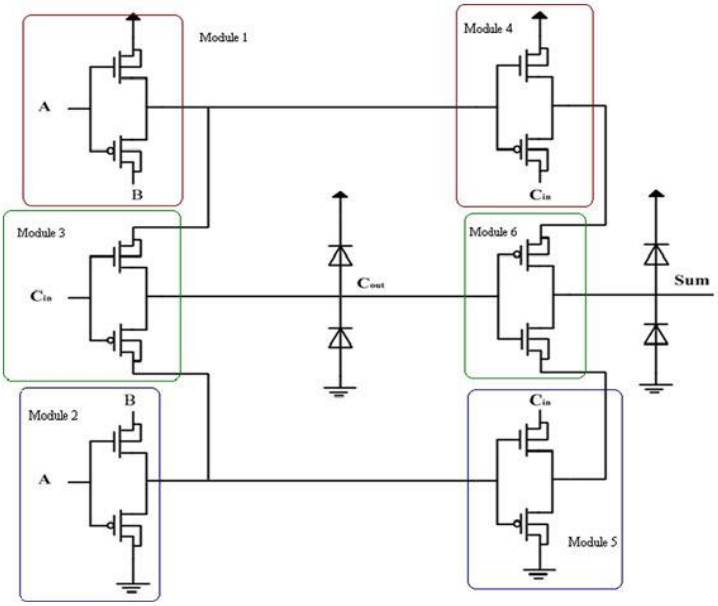

Figure-18 GDI-MUX full adder [15]

4.2.2 Schematic diagram of GDI-MUX full adder in 90nm using Cadence

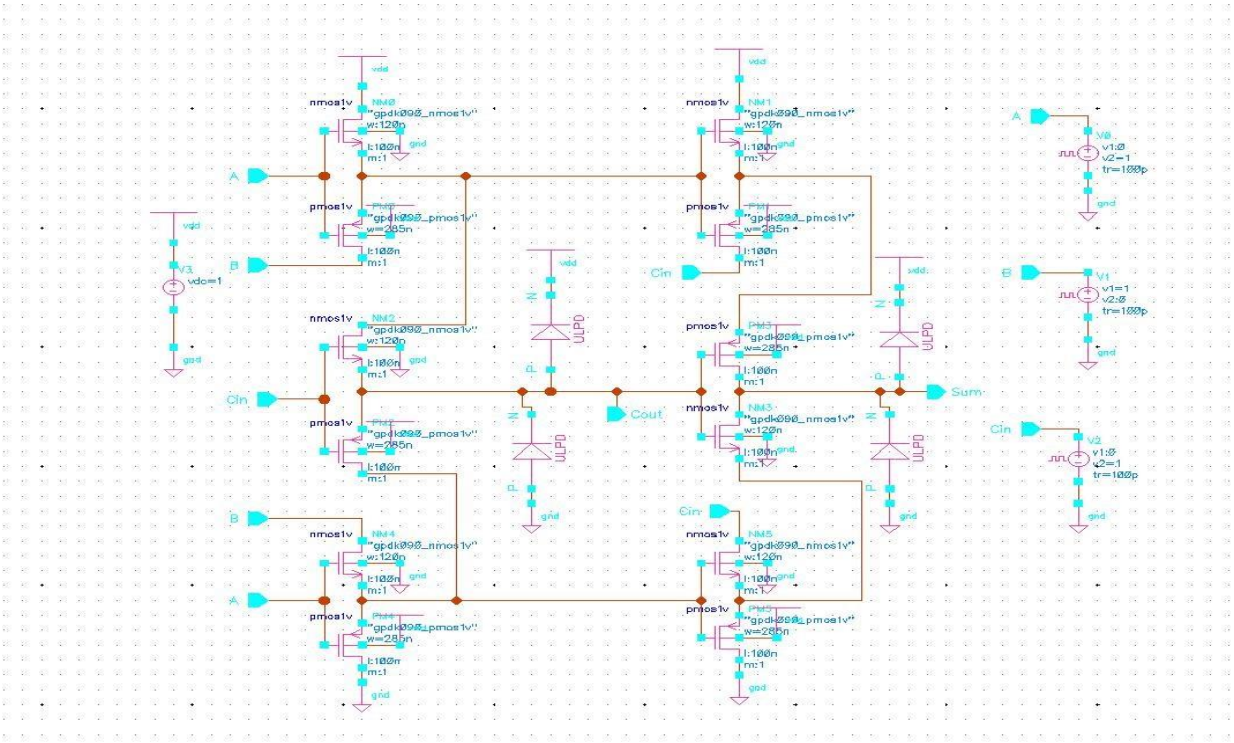

Figure-19 GDI-MUX schematic diagram

Chapter 5

Simulations and results

5.1 Simulation and results

All the full adders' simulations are done using Cadence Virtuoso in 90nm gpdk CMOS technology with supply voltage varying from 0.9 to 1.2V.Power dissipation, delay and Power delay product (PDP) are measured for different design techniques.Figure-20 to Figure-22 shows the transient response of different full adders. Figure-23 to Figure-25 shows the Power, Delay and PDP Comparison outputs.Table-4 shows the power dissipation results, Table-5 shows the Delay results and Table-6 shows the PDP results.

Transient response of C-CMOS full adder (fig.20a) and CPL full adder (fig.20b):

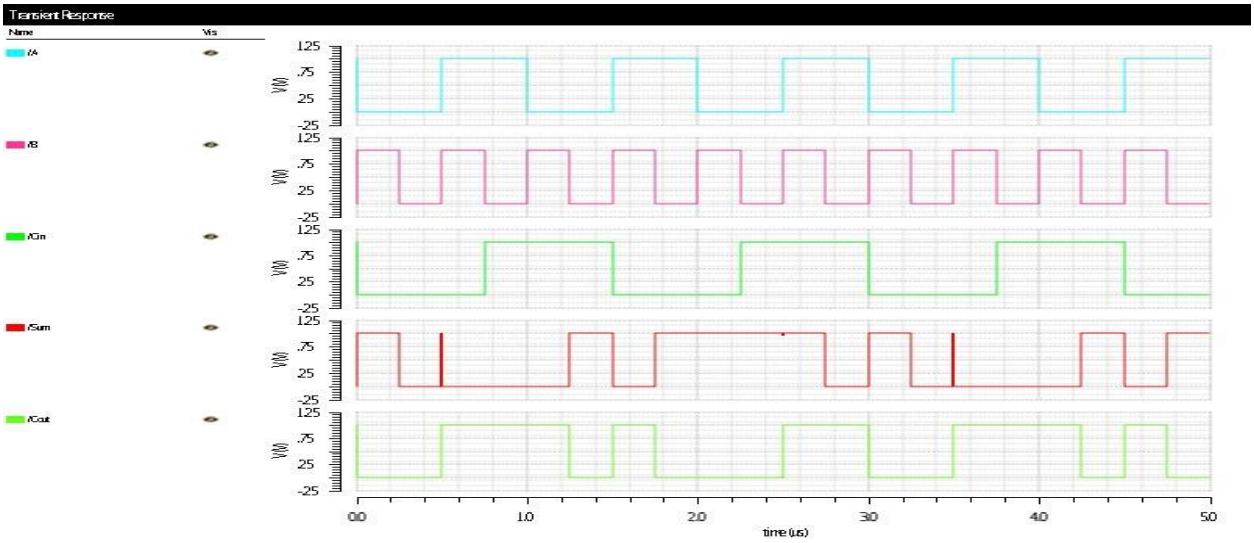

Figure-20 (a) transient response of C-CMOS full adder

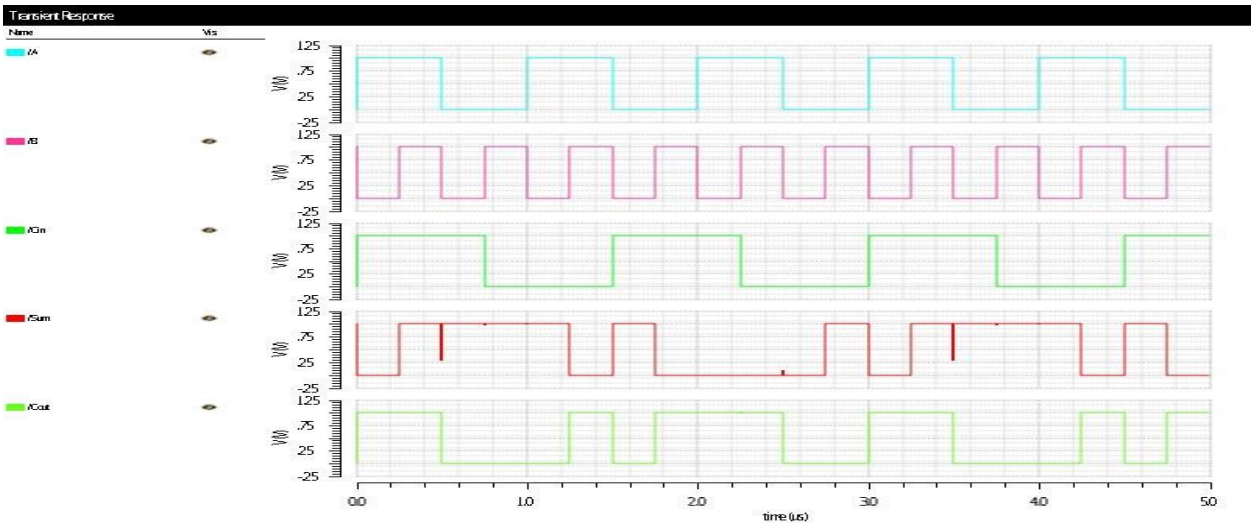

Figure-20 (b) transient response of CPL full adder

Transient response of hybrid CMOS full adder and ULP full adder

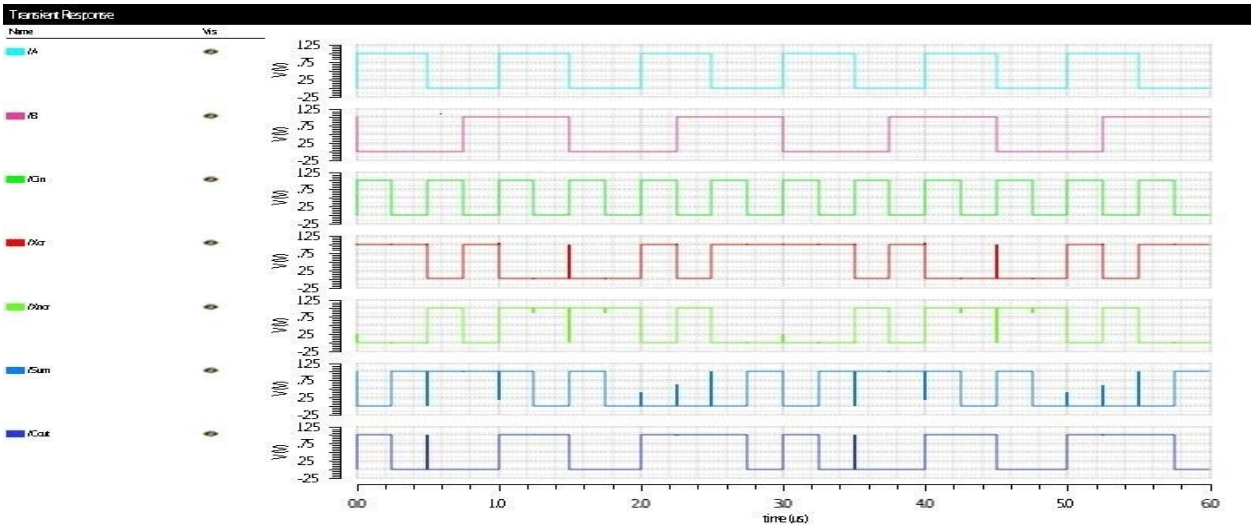

Figure-21 (a) Transient response of Hybrid CMOS full adder

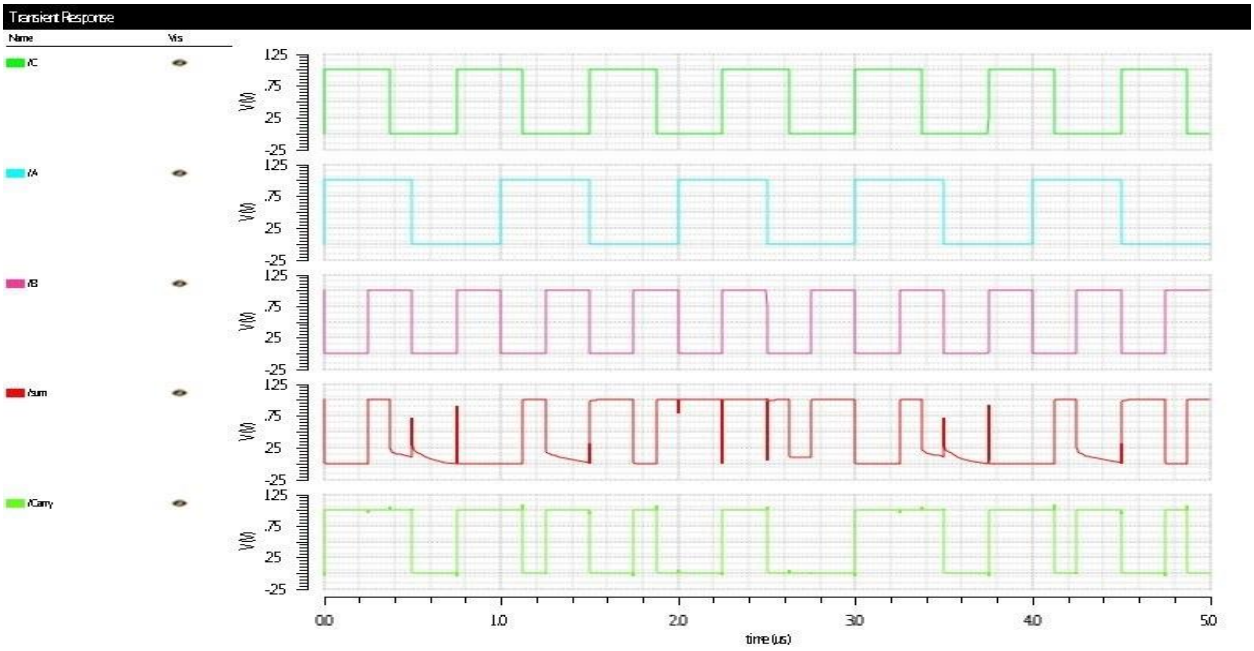

Figure-21 (b) Transient response of ULP full adder

Transient response of Hybrid full adder and GDI-MUX full adder

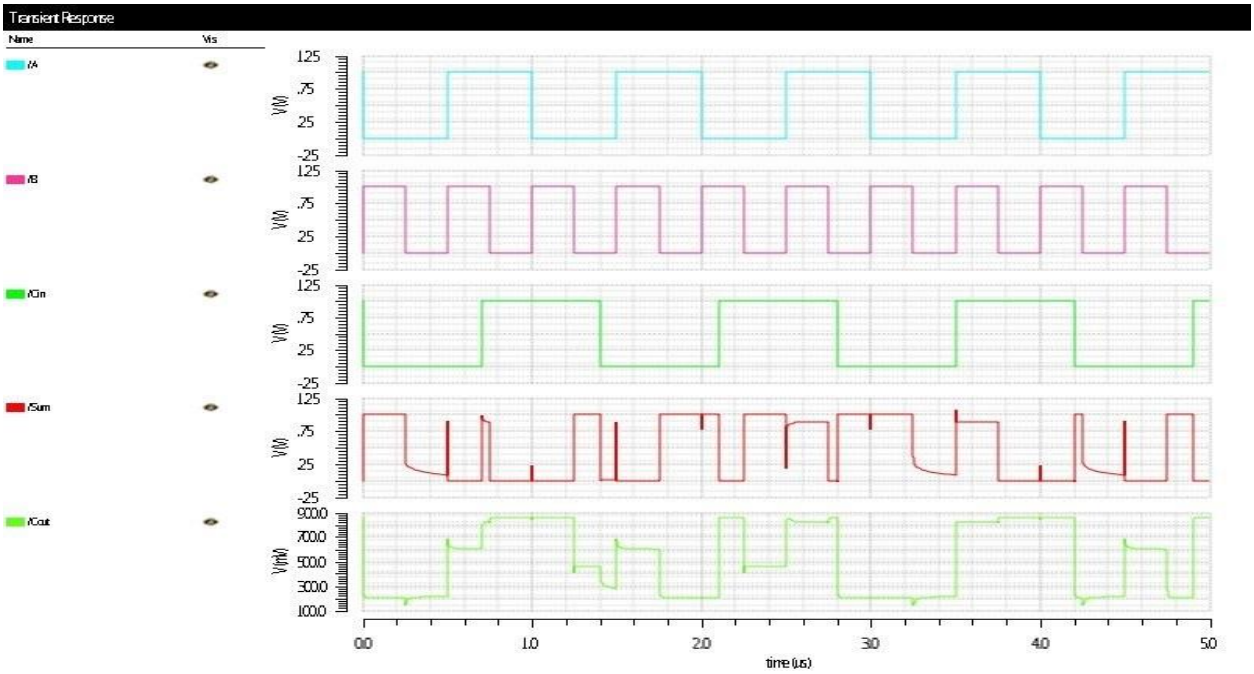

Figure-22 (a) hybrid full adder transient response

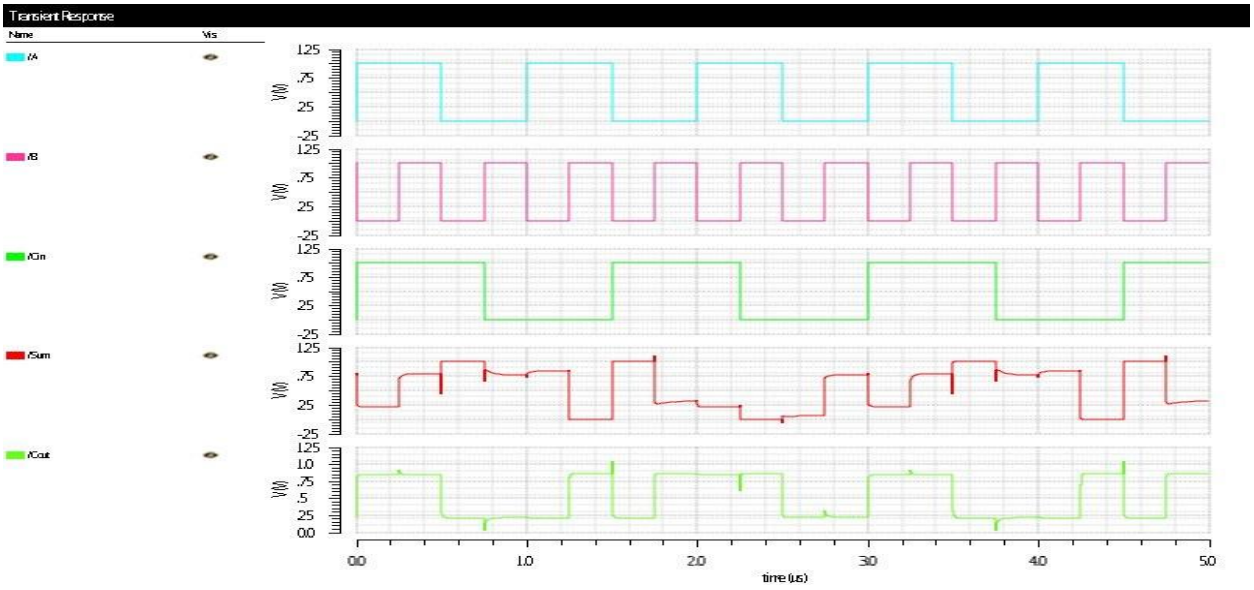

Figure-22 (b) GDI-MUX full adder transient response

5.2 Observations:

5.2.1 Power dissipations outputs for supply voltages varying for 0.9 to 1.2V in 90nm

Table-4

Supply voltage(V)	Design in (um)					
	C-CMOS	**CPL**	**Hybrid CMOS-1**	**ULPFA**	**Hybrid-2**	**GDI-MUX**
0.9	0.05387	0.2120	0.1249	0.2762	1.915	0.04892
1	0.07602	0.2948	0.1620	0.3057	2.038	0.07984
1.1	0.1273	0.4447	0.2578	0.3744	2.454	0.2331
1.2	0.6655	1.391	1.237	1.198	4.088	0.8299

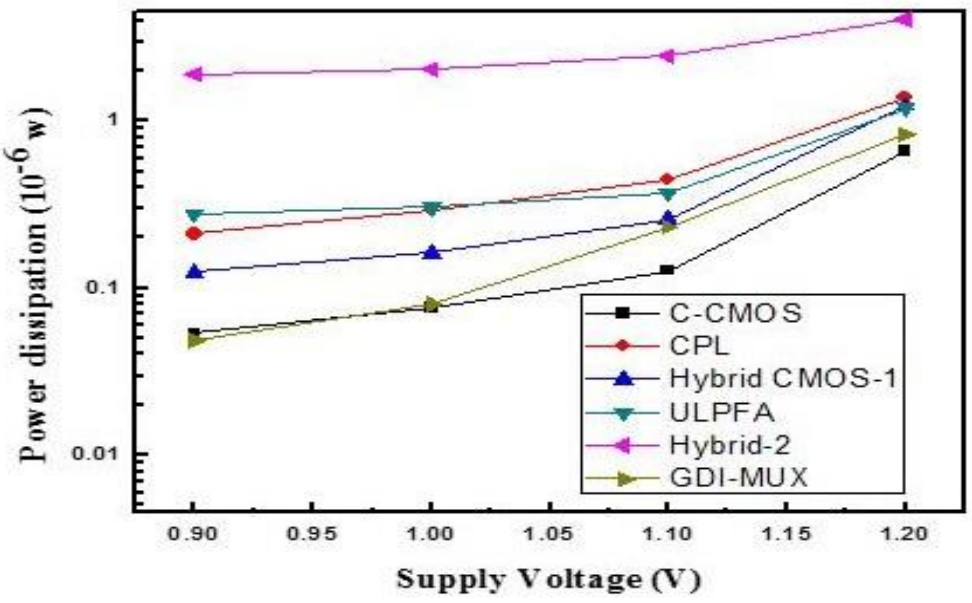

Figure-23 Power dissipation graph

5.2.2 Delay outputs for supply voltages varying for 0.9 to 1.2V in 90nm

Table-5

Supply voltage(V)	Design in (ps)					
	C-CMOS	**CPL**	**Hybrid CMOS-1**	**ULPFA**	**Hybrid-2**	**GDI-MUX**
0.9	124.5	132	104.8	110	100.45	102.65
1	119.5	107.7	104.1	104.2	97.45	99.4
1.1	107.9	86.9	99.9	100.1	97.15	99.05
1.2	108.9	85.1	96.8	97.45	99.3	102.45

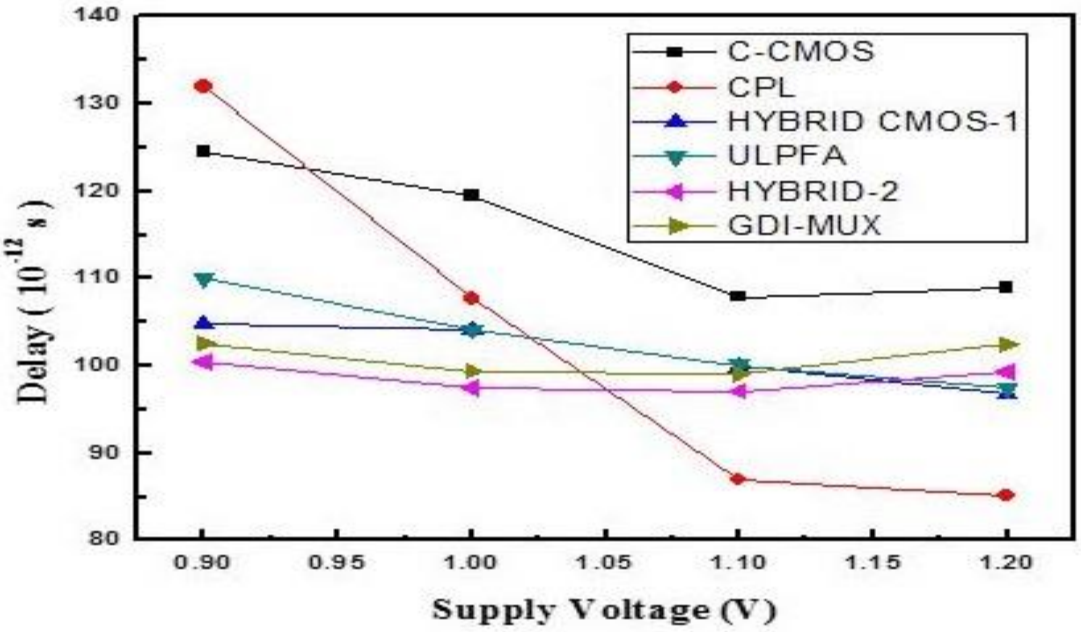

Figure-24 Delay Graph

5.2.3 Power Delay product outputs for supply voltages varying for 0.9 to 1.2V in 90nm

Table-6

Supply voltage(V)	Design in ($\times 10^{-18}$)					
	C-CMOS	**CPL**	**Hybrid CMOS-1**	**ULPFA**	**Hybrid-2**	**GDI-MUX**
0.9	6.706815	27.984	13.08952	30.382	119.36175	5.021638
1	9.08439	31.74996	16.8642	31.85394	198.6031	7.936096
1.1	13.73567	38.64443	25.75422	37.47744	238.4061	23.088555
1.2	72.47295	118.3741	119.7416	116.7451	405.9384	85.023255

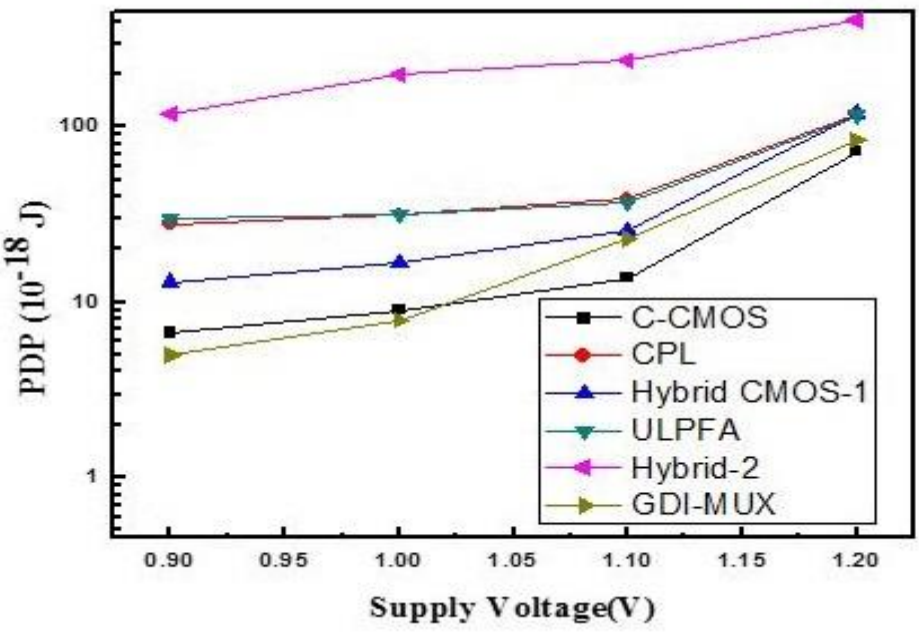

Figure-25 Power delay product graph

5.3 Conclusion:

Various types of full adders with different logic styles have been implemented. These C-CMOS, CPL, Hybrid CMOS, ULPFA full adders are compared with new hybrid full adder and GDI-MUX full adder. The two new full adders consists of less number of transistors, because of less number of transistors results in less switching activity and area. A broad comparison of all the designs will shows the gradual improvement in power dissipation, delay and Power delay product (PDP). The considered reduction in power by minimizing static and dynamic power dissipation as well as some techniques to enhance the speed of the design leads to the best PDP.

References:

[1] K. Navi, M.H. Moaiyeri, R. FaghihMirzaee, O. Hashemipour, B. MazloomNezhad, Two new low-power full adders based on majority-not gates, Microelectronics Journal (Elsevier), 40, 126–130.

[2] M.H. Moaiyeri, R. FaghihMirzaee, K. Navi, T. Nikoubin, O. Kavehei, Novel direct designs for 3-input XOR function for low power and high-speed applications, International Journal of Electronics (Taylor and Francis) 97 (6) (2010) 647–662.

[3] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, O. Kavehei, A novel low power full-adder cell for low voltage, Integration the VLSI Journal (Elsevier) 42 (4) (2009) 457–467.

[4] M. Alioto, G. Palumbo, Analysis and comparison of the full adder block, IEEE Transactions on VLSI 10 (6) (2002) 806–823.

[5] C.H. Chang, J. Gu, M. Zhang, A review of 0.18 um full-adder performances for tree structure arithmetic circuits, IEEE Transactions on Very Large Scale Integration(VLSI)Systems 13 (6) (2005).

[6] A.M. Shams, T.K. Darwish, M.A. Bayoumi, Performance analysis of low-power 1-bit CMOS full adder cells, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 10 (1) (2002) 20–29.

[7] Y. Jiang, A. Al-Sheraidah, Y. Wang, E. Sha, J. Chung, A novel multiplexer-based low-power full adder, IEEE Transactions on Circuits and Systems II: Express Briefs 51 (7) (2004).

[8] R. Zimmermann, W. Fichtner, Low-power logic styles: CMOS versus pass-transistor logic, IEEE Journal of Solid-State Circuits 32 (1997) 1079–1090.

[9] S. Issam, A. Khater, A. Bellaouar, M.I. Elmasry, Circuit techniques for CMOS low-power high performance multipliers, IEEE Journal of Solid-State Circuits 31 (1996) 1535–1544.

[10] S. Goel, A. Kumar, M.-A. Bayoumi, Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style, IEEE Transac-tions on Very Large Scale Integration (VLSI) Systems 14 (12) (2006) 1309–1321.

[11] H.T. Bui, A.K. Al-Sheraidah, Y. Wang, New 4-transistor XOR and XNOR designs, in: Proceedings of the 2nd IEEE Asia Pacific Conference ASICs, 2000, pp. 25–28.

[12] D. Hassoune, I.O Flandre, Connor, J.D. Legat, ULPFA: a new efficient design of a power-aware full adder, IEEE Transactions on Circuits and Systems—I: Regular Papers 57 (8) (2010).

[13] V. Dessard, SOI Specific Analog Techniques for Low-noise, High-temperature or Ultra-low Power Circuits, Ph.D. Thesis, UCL, Louvain, Belgium, 2001.

[14] J.-M. Wang, S.-C. Fang, W.-S. Feng, New efficient designs for XOR and XNOR functions on the transistor level, IEEE Journal of Solid-State Circuits 29 (7) (1994) 780–786.

[15] Foroutan, Vahid, MohammadReza Taheri,Keivan Navi, and Arash Azizi Mazreah. "Designof two Low-Power full adder cells using GDI structure and hybrid CMOS logic style",Integration the VLSI Journal, 2013.

[16] Arkadiy Morgenshtein, A. Fish, Israel A. Wagner, Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits, IEEE Transactions on VLSI Systems (2002) 566–581.