Performance Enhancement of Shunt APFs Using Various Topologies, Control Schemes and Optimization Techniques

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Performance Enhancement of Shunt APFs Using Various Topologies, Control Schemes and Optimization Techniques

DISSERTATION

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By

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CERTIFICATE

This is to certify that the thesis titled ***"Performance Enhancement of Shunt APFs Using Various Topologies, Control Schemes and Optimization Techniques"***, submitted by ***Ms. Sushree Sangita Patnaik*** to the National Institute of Technology Rourkela, for the award of the degree of ***Doctor of Philosophy*** in ***Electrical Engineering***, is a bona fide record of research work carried out by her under my supervision and guidance.

The matter embodied in the thesis is candidate's original work and has not been submitted elsewhere for the award of any degree or diploma.

In my opinion, the thesis is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy in Electrical Engineering.

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Acronyms

ABC	Artificial bee colony
AC	Alternating current
ACO	Ant colony optimization
ADALINE	Adaptive linear neuron
ANN	Artificial neural network
APF	Active power filter
APOD	Alternative phase opposite disposition
BFO	Bacterial foraging optimization
CSI	Current-source inverter
CSNL	Current source nonlinear load
DC	Direct current
DSO	Digital storage oscilloscope
DVR	Dynamic voltage restorer
EMI	Electro-magnetic interference
FFT	Fast Fourier transform
GA	Genetic algorithm
GTO	Gate turn-off thyristor
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-gate bipolar transistor
IPD	In-phase disposition
ISE	Integral square error
LPF	Low-pass filter
MLI	Multilevel inverter
PCC	Point of common coupling

PHC	Perfect harmonic cancellation
POD	Phase opposite disposition
PI	Proportional-integral
PLL	Phase-locked loop
PSO	Particle swarm optimization
PWM	Pulse-width modulation
RDFT	Recursive discrete Fourier transform
RMS	Root mean square
RT-Lab	Real-time Laboratory
SHE	Selective harmonic elimination
SVM	Space vector modulation
TDD	Total demand distortion
THD	Total harmonic distortion
UPQC	Unified power quality conditioner
VSI	Voltage-source inverter
VSNL	Voltage source nonlinear load
2C	Split capacitor VSI
3HB	Three H-bridges VSI
3L-HB	Three-level H-bridge VSI
4L	Four leg VSI

Notations

Notations for parameters used in APF

f	Operating frequency of supply
R	Resistance
L	Inductance
C	Capacitance
R_s, L_s	Source resistance and inductance
R_c, L_c	Filter resistance and inductance
R_F, C_F	RC high-pass filter on AC-side of APF
R_L, L_L	Load resistance and inductance
i_s	Source current
i_L	Load current
i_c	Compensation filter current
i_1, i_n	Fundamental and n^{th} order harmonic components of current
V_1, V_n	Fundamental and n^{th} order harmonic components of voltage
K_p, K_i	Proportional and Integral gains of PI controller
C_{dc}	DC-link capacitance
e_{dc}	Actual average energy stored on DC bus
$e_{dc}{}^*$	Nominal energy stored on DC bus
Δe_{dc}	Energy loss of DC bus
V_{dc}	Actual DC-link voltage
$V_{dc}{}^*$	Reference DC-link voltage
V_{dca}	Average value of actual DC-link voltage
ΔV_{dc}	Deviation in DC-link voltage from its reference value
V_c, I_c	AC-side voltage and current of VSI
I_{c0}, V_{dc0}	Steady-state operating points of I_c and V_{dc}

$I_{c,rated}$	Rated filter current
$V_{dc,\max\ \_rip(p-p)}$	Peak-to-peak ripple in DC-link voltage
J	Objective/cost/fitness function
HB	Hysteresis bandwidth
ω	Rotational speed of synchronously rotating $d-q$ axes
v_{sa}, v_{sb}, v_{sc}	Supply voltage in three phases
v_α, v_β, v_0	Supply voltage in $\alpha-\beta-0$ coordinates
v_d, v_q	Supply voltage in $d-q$ coordinates
$\overline{v_d}, \overline{v_q}$	Fundamental components of voltages v_d and v_q
i_{La}, i_{Lb}, i_{Lc}	Load currents in three phases
i_n	Neutral current in three-phase four-wire systems
i_α, i_β, i_0	Load current in $\alpha-\beta-0$ coordinates
i_{Ld}, i_{Lq}, i_0	Load current in $d-q-0$ coordinates
$i_{ca}, i_{cb}, i_{cc}, i_{cn}$	Actual compensation filter currents in four wires
${i_{ca}}^*, {i_{cb}}^*, {i_{cc}}^*, {i_{cn}}^*$	Reference compensation filter currents in four wires
${i_{c\alpha}}^*, {i_{c\beta}}^*, {i_{c0}}^*$	Reference compensation filter currents in $\alpha-\beta-0$ coordinates
${i_{cd}}^*, {i_{cq}}^*, {i_{c0}}^*$	Reference compensation filter currents in $d-q-0$ coordinates
p, q, p_0	Instantaneous active, reactive and zero-sequence powers
$\overline{p_0}, \widetilde{p_0}$	Average/mean/DC and oscillating/AC components of power p_0
$\bar{p}, \tilde{p}$	Average/mean/DC and oscillating/AC components of power p
$\bar{q}, \tilde{q}$	Average/mean/DC and oscillating/AC components of power q
$\overline{P_{loss}}$	Average value of loss occurring inside VSI
i_d, i_q	Instantaneous d-axis and q-axis current components
i_{d1h}	Active current required to maintain a constant DC-link voltage
i_{Ld1h}, i_{Lq1h}	Fundamental frequency components of i_{Ld} and i_{Lq}
i_{Ldnh}, i_{Lqnh}	Oscillating components of i_{Ld} and i_{Lq}
m	Level of MLI
$\theta_1, \theta_2, \ldots\ \theta_s$	Switching angles for cascaded MLI with s number of DC sources

v_{ref}	Reference signal for multicarrier PWM
$v_{cr1}, v_{cr2}, v_{cr3}, v_{cr4}$	Triangular carrier signals for multicarrier PWM
f_c, f_m	Frequencies of carrier and modulating signals
A_c, A_m	Amplitude of carrier and modulating signals
m_f, m_a	Frequency and amplitude modulation indices
f_{dev}	Device switching frequency
f_{inv}	Inverter switching frequency

Notations for parameters used in optimization techniques

x	Position of a particle in the search space
v	Velocity of the particle
i, j, k, l, m	Pointers for particle index, chemotaxis, reproduction, elimination dispersal event and swimming
x^i_{Lbest}	Position corresponding to best fitness attained by i^{th} particle
x^i_{Gbest}	Position corresponding to global best fitness
r_1, r_2	Random numbers in the interval $[-1,1]$
c_1, c_2	Cognitive and social acceleration constants
w	Inertia constant
w_{max}, w_{min}	Maximum and minimum values of w
G, g	Maximum and current values of number of generation
$\theta^i(j,k,l)$	i^{th} bacterium at j^{th} chemotactic, k^{th} reproductive and l^{th} elimination-dispersal step
$C(i)$	Step size
$\Delta(i)$	Vector in arbitrary direction whose elements lie in $[-1,1]$
J_{cc}	Cost function accounting for cell-to-cell communication
d_{att}, w_{att}	Quantity and diffusion rate of attractant signal
h_{rep}, w_{rep}	Quantity and diffusion rate of repellent effect magnitude
P	Number of parameters to be optimized

S	Population size
N_s	Swimming length
N_c	Number of chemotactic steps
N_{re}	Number of reproduction steps
N_{ed}	Number of elimination-dispersal steps
P_{ed}	Probability at which elimination-dispersal occurs
J_{health}^{i}	Fitness of i^{th} bacterium

Abstract

Following the advent of solid-state power electronics technology, extensive usage of nonlinear loads has lead to severe disturbances like harmonics, unbalanced currents, excessive neutral current and reactive power burden in three-phase power systems. Harmonics lower down the efficiency and power factor, increase losses, and result in electromagnetic interference with neighbouring communication lines and other harmful consequences. Over the years, active power filter (APF) has been proven to be a brilliant solution among researchers and application engineers dealing with power quality issues.

Selection of proper reference compensation current extraction scheme plays the most crucial role in APF performance. This thesis describes three time-domain schemes viz. Instantaneous active and reactive power ($p-q$), modified $p-q$, and Instantaneous active and reactive current component (i_d-i_q) schemes. The objective is to bring down the source current THD below 5%, to satisfy the IEEE-519 Standard recommendations on harmonic limits. Comparative evaluation shows that, i_d-i_q is the best APF control scheme irrespective of supply and load conditions. Results are validated with simulations, followed by real-time analysis in RT-Lab.

In view of the fact that APFs are generally comprised of voltage source inverter (VSI) based on PWM, undesirable power loss takes place inside it due to the inductors and switching devices. This is effectively minimized with inverter DC-link voltage regulation using PI controller. The controller gains are determined using optimization technique, as the conventional linearized tuning of PI controller yield inadequate results for a range of operating conditions due to the complex, nonlinear and time-varying nature of power system networks. Developed by hybridization of Particle swarm optimization (PSO) and Bacterial foraging optimization (BFO), an Enhanced BFO technique is proposed here so as to overcome the drawbacks of both PSO and BFO, and accelerate the convergence of optimization problem. Extensive simulation studies and RT-Lab real-time investigations are performed for comparative assessment of proposed implementation of PSO, BFO and

Enhanced BFO on APF. This validates that, the APF employing Enhanced BFO offers superior harmonic compensation compared to other alternatives, by lowering down the source current THD to drastically small values.

Another indispensable aspect of APF is its topology, which plays an essential role in meeting harmonic current requirement of nonlinear loads. APFs are generally developed with current-source or voltage-source inverters. The latter is more convenient as it is lighter, cheaper, and expandable to multilevel and multistep versions for improved performance at high power ratings with lower switching frequencies. There can be different topologies of VSI depending on the type of supply system. With each topology, constraints related to DC-link voltage regulation change. For effective compensation, irrespective of the number and rating of DC-link capacitors used in any particular topology, voltages across them must be maintained constant with optimal regulation of DC-link voltage. Various topologies for three-phase three-wire systems (conventional two-level and multilevel VSIs) and four-wire systems (split-capacitor (2C), four-leg (4L), three H-bridges (3HB) and three-level H-bridge (3L-HB) VSIs) are analyzed and compared based on component requirements, effectiveness in harmonic compensation, cost and area of application.

Keywords: Current harmonics compensation; shunt active power filter; voltage source inverter topologies; multilevel inverter; optimization technique; RT-Lab

Chapter 1

Introduction

1.1. Overview

Harmonics can be defined as "a sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental supply frequency" [1]. Therefore, harmonics can be thought of as voltages and/or currents present in an electrical system at some multiple of the fundamental frequency, which when added together result in a distorted waveform. For example, Figure 1.1 illustrates how the resultant distorted waveform is produced when the 3rd, 5th and 7th order harmonic components are added to the fundamental component of the signal.

Total harmonic distortion (THD) is the measure of effective value of harmonic content in a distorted current or voltage signal. It is defined as the ratio of the RMS of harmonic content to the RMS value of fundamental quantity.

Mathematically, THD in a current signal can be given by (1.1).

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} {i_n}^2}}{i_1} \tag{1.1}$$

Where, i_1 and i_n are the RMS values of fundamental and n^{th} order harmonic components of current respectively.

Similarly, equation (1.2) gives away the THD in a voltage signal.

$$THD_V = \frac{\sqrt{\sum_{n=2}^{\infty} {V_n}^2}}{V_1} \tag{1.2}$$

Where, V_1 and V_n indicate the RMS values of fundamental and n^{th} order harmonic components of voltage respectively.

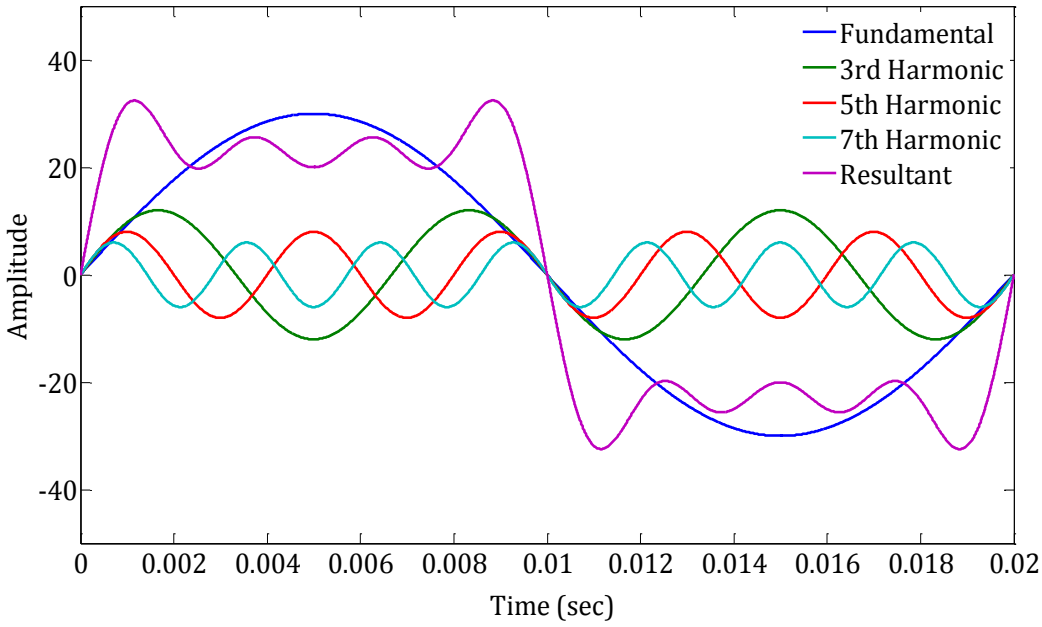


Figure 1.1: Harmonics

1.1.1. Causes behind production of harmonics

Harmonic production is resulted due to the usage of large number of nonlinear loads. Nonlinear loads are the loads which do not draw a sinusoidal current even when they are supplied with a sinusoidal voltage. There are two types of harmonics sources, current source nonlinear loads (CSNLs) producing current harmonics and voltage source nonlinear loads (VSNLs) producing voltage harmonics [2], [3].

However, the work presented in this thesis is confined to mitigation of current harmonics. With the advent of low-cost solid-state electronics, modern forms of power conversions such as static rectifiers and drives have mostly substituted the older methods of conversion. As a consequence, the solid-state converter unit and/or its loads now-a-days represent a substantial portion of the total power system requirements. Current harmonics result from the switching operations of power electronic devices. The loads which are primarily responsible for production of harmonic currents can be as follows:

a) *Commercial loads:* Single-phase power supplies, fluorescent lighting, adjustable speed drives for HVAC, elevators etc.
b) *Industrial loads:* Three-phase power converters (DC and AC drives), arcing devices, saturable devices etc.
c) *Domestic loads:* Computer systems and other electronic loads

1.1.2. Consequences of harmonics

Current harmonics is one of the major culprits behind the rigorous deterioration of power quality as it leads to various harmful consequences [4], [5] such as:

a) Overheating of transformers, motors etc.
b) Overheated neutral conductors
c) Poor efficiency and power factor
d) Increased losses in power system
e) Electro-magnetic interference with nearby communication lines
f) False tripping of protective relays
g) Failure or misoperation of microprocessors
h) Vibration in rotating machines
i) Voltage quality degradation
j) Malfunctioning of medical facilities etc.

In the past few years, the proliferation of nonlinear loads in power system has been growing at an unprecedented pace, following the pervasive use of solid-state control of AC power. Typical nonlinear loads such as arc furnaces, fluorescent lights, power electronic converters, microprocessors, motor drives, electronic loads, saturated transformers, switching mode power supplies, various domestic appliances, etc. draw significant amount of harmonic current from the utility bringing down the efficiency and power factor, and increasing the risk of electromagnetic interference with neighbouring communication lines. The triplen order harmonic currents (3^{rd}, 6^{th}, 9^{th}, etc.) add on to the

neutral conductor being in-phase with each other, which may result in overloaded power feeders, overloaded transformers, voltage distortion and common mode noise [6].

This thesis discusses the basics of passive power filter. This is followed by a description on the role of shunt active power filter (APF) in compensation of the undesirable consequences caused due to nonlinear loads, the priority being mitigation of current harmonics in power system. Three different APF control schemes namely, Instantaneous active and reactive power ($p-q$), modified $p-q$, and Instantaneous active and reactive current component (i_d-i_q) schemes for the extraction of reference compensation currents are analysed rigorously and compared to determine the best one among them. Here the APF is considered to be comprised of a Pulse-width modulation (PWM) based voltage source inverter (VSI); therefore it involves huge power loss inside the inverter itself. To overcome this, a DC-link voltage regulator is used to make the DC-link voltage constant with the help of a PI controller. However, the conventional method of PI controller tuning does not yield satisfactory results for wide range of operating conditions. So, goal of the dissertation is to find out optimized values of PI controller gains with the help of stochastic optimization techniques like Particle swarm optimization (PSO) and Bacterial foraging optimization (BFO). This leads to the lowering down of overall THD of source current. An Enhancement to the BFO algorithm is also proposed here, developed by the hybridization of PSO and BFO algorithms. It is validated to give superior performance even under highly distorted and unbalanced supplies, and sudden load change conditions. Various shunt APF configurations for three-phase three-wire distribution systems are modelled. It also showcases the use of multilevel inverters (MLIs) for active power line conditioning. Furthermore, various three-phase four-wire APF topologies are discussed, the focus being split-capacitor (2C), four-leg (4L), three H-bridges (3HB), and three-level H-bridge (3L-HB) topologies. Performances of all the above mentioned APF topologies are evaluated in terms of current harmonic compensation. The evaluations are carried out by performing simulation studies and real-time performance analysis in RT-Lab. Finally, the general conclusions, major contributions and scope for future research are discussed.

Section 1.2 gives an overall idea about the efforts done so far in order to sort out these power quality issues as literature survey. The tools used for carrying out the analyses presented in this thesis are discussed in Section 1.3. Section 1.4 summarizes the motivation behind the thesis, followed by the objectives in Section 1.5. The next section illustrates the organization of the thesis in various chapters.

1.2. Research Background

In order to solve the problem of harmonic pollution effectively, many harmonic limitation standards such as IEEE 519-2014, IEC 1000-3-2 and IEC 1000-3-4 have been established [7]–[10]. However, IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems (IEEE 519-2014 Standard) [7], [8] provides an excellent basis for limiting harmonics.

IEEE 519-2014 Standard for harmonic current limits for general distribution systems (120–69,000 V) is presented in Table 1.1. A lot of research has been done to find out a tool that would be able to compensate the disturbances caused due to nonlinear loads so that the IEEE-519 Standards can be met even under sudden load changes, irrespective of the supply voltage condition. The supply voltage can be either ideal or non-ideal (distorted and unbalanced supply conditions). Distorted supply is resulted due to static frequency converters, cycloconverters, arcing devices, switching power supplies and other power electronic devices, where a steady state deviation of supply voltage from an ideal sine wave of fundamental operating frequency is observed. Presence of unequal single-phase loads, blown fuses in one of the phases of a three-phase capacitor bank or single phasing conditions result in unbalanced supply condition as the voltage becomes asymmetrically balanced between the three phases of supply.

The detrimental consequences of current harmonics, excessive neutral current and unbalanced source current in the power systems can be avoided by the use of a device known as Active power filter. But, prior to the development of semiconductor technology, Passive power filters were being extensively used for this purpose.

Table 1.1: IEEE 519-2014 Standard for harmonic current limits for general distribution systems (120–69,000 V)

Maximum Harmonic Current Distortion in Percent of I_L	Individual Harmonic Order (Odd Harmonics)					
$\frac{I_{sc}}{I_L}$	<11	$11 \le n < 17$	$17 \le n < 23$	$23 \le n < 35$	$35 \le n$	TDD
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Even harmonics are limited to 25% of the odd harmonic limits above.

Current distortions that result in a DC offset, e.g. half-wave converters, are not allowed.

*All power generation equipments are limited to these values of current distortion, regardless of actual $\left(\frac{I_{sc}}{I_L}\right)$.

Where,

I_L = Maximum demand load current (fundamental frequency component) at the point of common coupling (PCC)

I_{sc} = Maximum short-circuit current at PCC

TDD = Total demand distortion; harmonic current distortion in % of maximum demand load current (15 or 30 min demand)

1.2.1. Passive power filters

Passive filters have been most commonly used to limit the flow of harmonic currents in distribution systems. It comprises of basic linear elements such as resistors, capacitors, inductors and transformers. It provides a low-impedance path to ground for the harmonic frequencies. These are usually custom designed for the application; however they may be tuned to a frequency between two prevalent harmonics so as to help attenuate both. The resistance, inductance, and capacitance values are determined from the filter type and from the following parameters [11]–[14]:

a) Reactive power at nominal voltage
b) Tuning frequencies
c) Quality factor, which is a measure of the sharpness of tuning frequency

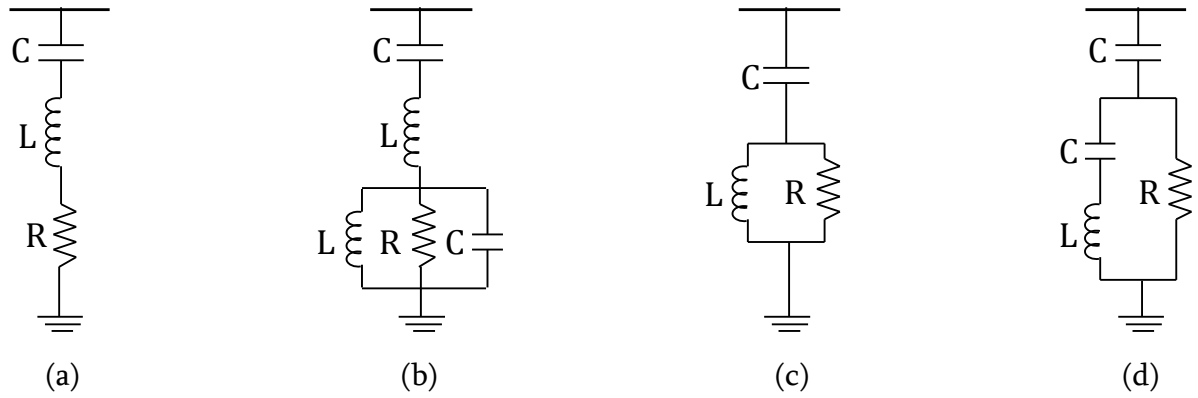


Figure 1.2: Types of three-phase passive harmonic filters, (a) Single-tuned, (b) Double-tuned, (c) High-pass, (d) C-type High-pass

Four types of filters that can be modelled with the three-phase harmonic filter block are shown in Figure 1.2. In order to achieve an acceptable distortion, several banks of filters of different types are usually connected in parallel. The most commonly used filter types are:

a) Band-pass filters: These are used to filter lowest order harmonics such as 5^{th}, 7^{th}, 11^{th}, 13^{th}, etc. Band-pass filters can be tuned at a single frequency (single-tuned filter) or at two frequencies (double-tuned filter).

b) *High-pass filters*: These are used to filter higher order harmonics and cover a wide range of frequencies. A special type of high-pass filter called C-type high-pass filter is used to provide reactive power and avoid parallel resonances. It also allows filtering low order harmonics (such as 3rd), keeping zero losses at fundamental frequency.

Conventionally, passive filter is used to solve the issues of harmonic pollution in industrial power system due to its low cost. However, it suffers from following drawbacks [15]–[17]:

a) Sensitive to the variation of power system impedance
b) Sensitive to frequency variation of the utility
c) Risk of series/parallel resonance with power system impedance
d) Poor flexibility due to selective harmonic compensation
e) Ineffective when the harmonic content varies randomly

Among those listed above, the series/parallel resonance is the most serious disadvantage. It may result in over-current/over-voltage on the inductor and capacitor causing damage to the passive power filter. Since the system impedance has a significant effect on the performance of passive power filter, it is very hard to obtain an excellent filter performance in practical applications. Moreover, the harmonic currents produced by neighbouring nonlinear loads may flow into the passive power filter and result in overloading of the filter.

1.2.2. Active power filters

After the advent of semiconductor switching devices in 1970s, harmonic suppression facilities based on power electronic technique were developed [18]. These active harmonic suppression facilities known as Active power filters (APFs) can suppress different order harmonic components of nonlinear loads simultaneously [16], [19]–[30]. APF confines the load current harmonics at the load terminals, hindering its penetration into the power system. The advantage of active filtering is that it automatically adapts to

changes in the network and load fluctuations [31]. Few most important advantages of APF are:

a) Intelligent filter
b) Can be used globally or locally
c) Extremely efficient even when the harmonic content varies randomly
d) More than one devices can be installed on the same supply

This device uses Insulated gate bipolar transistors (IGBTs) or Gate turn-off thyristors (GTOs), and Pulse-width modulation (PWM) control techniques [32]. The PWM converter comprising of IGBTs/GTOs can have many configurations, but standard inverter topology is mostly preferred [26], [31], [33], [34].

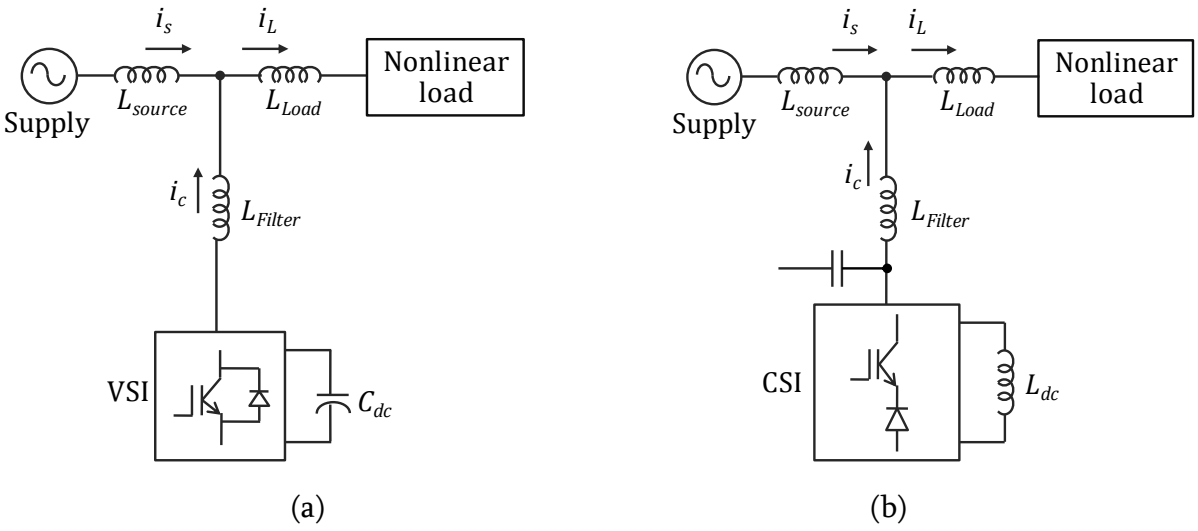


Figure 1.3: (a) APF employing VSI, (b) APF employing CSI

The PWM inverter is either a Voltage source inverter (VSI) or a Current source inverter (CSI) as depicted in Figure 1.3. Here, L_{source}, L_{Load} and L_{Filter} represent source, load and filter impedances respectively. Likewise, source current, load current and compensation filter current are denoted as i_s, i_L and i_c. The energy storage element on DC side of inverter is capacitor (C_{dc}) in case of VSI and inductor (L_{dc}) in case of CSI. This is indicative of a drawback in the latter, as the inductor is less efficient in energy storage compared to capacitor. Further, on-state losses are more in CSI than VSI. These losses are

now-a-days reduced using a diode in series with IGBT for reverse voltage blocking, as shown in Figure 1.3 (b). VSI is the most preferred alternative in industrial applications as well as APFs; as it is less costly, lighter and more efficient compared to CSI. The capacity of power converter employed as APF must be larger than the product of harmonic components and fundamental component of load current and the utility voltage [35].

According to the power circuit configurations and connections, APFs can be divided into shunt APFs, series APFs and other filter combinations [2], [29], [36]. The shunt APF is connected in parallel to the load and generates compensation current which opposes the load harmonic current from being injected into the power feeder. The shunt APF is devised to inject current harmonics of equal magnitude but in phase opposition with the load current harmonics at the point of common coupling (PCC) between source and load as shown in Figure 1.4 (a), thereby cancelling out each other. Similarly, series APF compensates for harmonic voltages generated by nonlinear loads such as a diode rectifier with smoothing DC capacitor [37]. Figure 1.4 (b) shows a voltage harmonic producing load and the connection of series APF for the required voltage harmonic compensation.

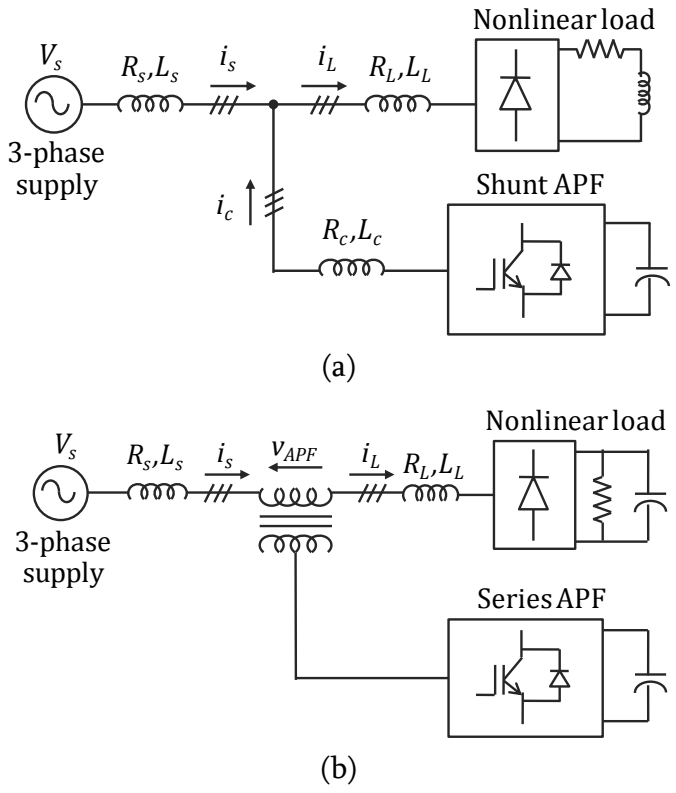


Figure 1.4: Basic types of APF connections (a) Shunt APF, (b) Series APF

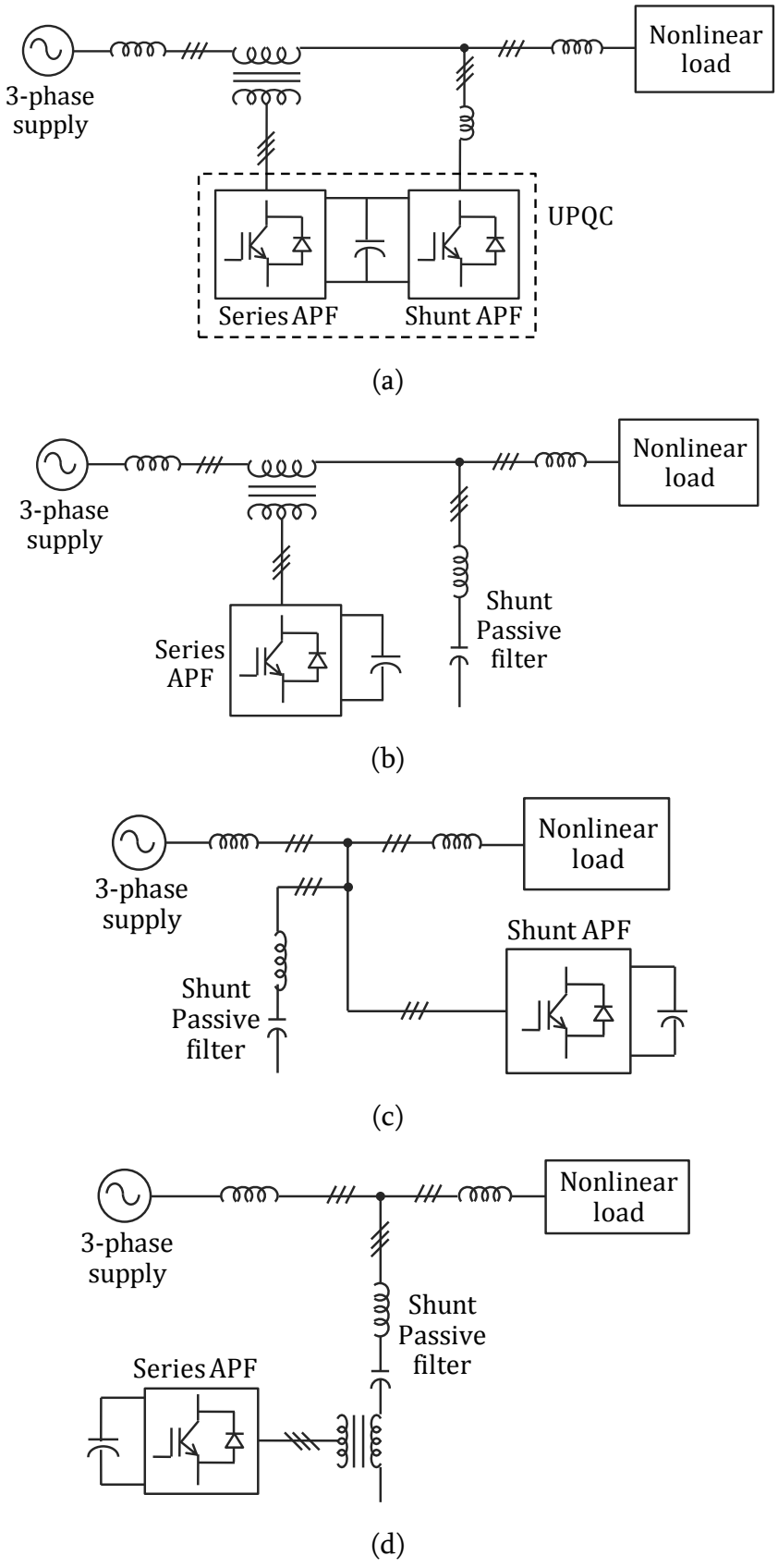


Figure 1.5: Hybrid combinations of filters, (a) Shunt active filter and series active filter, (b) Series active filter and shunt passive filter, (c) Shunt active filter and shunt passive filter, (d) Active filter in series with shunt passive filter

In some applications, the combination of several types of filters can achieve greater benefits [27]–[30]. The hybrid filter consists of a single or multiple numbers of APFs, combined with passive power filters. The major hybrid combinations include shunt active filter and series active filter, series active filter and shunt passive filter, shunt active filter and shunt passive filter, and active filter in series with shunt passive power filter as shown in Figure 1.5 [2], [36].

APFs can also be classified based on the type of compensation such as reactive power compensation, harmonic compensation, balancing of three-phase systems and multiple compensations [29]. However, the conventional shunt APF belongs to multiple compensations type and can compensate for harmonic current, reactive power and unbalanced loading simultaneously [19]–[26].

1.2.3. Control schemes for APF

The control schemes for APF constitute a crucial part in the harmonic compensation, as any inaccuracy leads to inexact compensation. Various schemes such as Instantaneous active and reactive power ($p-q$), Instantaneous active and reactive current component $(i_d - i_q)$, Perfect harmonic cancellation (PHC), Generalized integral, Adaptive filter, Delay-less filtering based on Artificial Neural Network (ANN), Adaptive Linear Neuron (ADALINE), Wavelet Transform, Fast Fourier Transform (FFT) and Recursive Discrete Fourier Transform (RDFT) have been proposed since the development of APFs [38]–[43]. Time-domain methods are preferred here because of (a) fast response to changes in power system, (b) easy implementation with less memory requirements, and (c) less computational burden unlike frequency-domain methods, where the number of calculations increases with an increase in the highest order of harmonics to be eliminated, resulting in longer response time. The ANN and ADALINE methods are also associated with few shortcomings. Number of ADALINE required to tune is equal to the number of harmonics considered in load current, thus slowing down the convergence. Generation of the input vector $X = [\cos \omega t\,, \sin \omega t \ldots \cos n\omega t\,, \sin n\omega t]^T$ is difficult and involves a

tedious process. Moreover, the error being minimized by gradient-based method has likelihood of converging to local minima [43].

Following are the three APF control schemes those are discussed elaborately in Chapter 2 of this thesis. In addition, a comparison of their effectiveness to harmonic compensation is also studied from the simulation and RT-Lab results.

1) Instantaneous active and reactive power ($p-q$) scheme

Out of all the APF control schemes, the $p-q$ method introduced by Akagi *et al.* has gained well recognition as a viable solution to the problems created by nonlinear loads [44], [45]. It is most widely used as it offers a very precise reference compensation current template and allows obtaining a clear difference between instantaneous active and reactive powers. However, it is criticized as a disappointment under non-ideal supply conditions [46]–[48], because the multiplication of instantaneous load currents and voltages while calculating the instantaneous active and reactive powers leads to amplification of harmonic content, when the supply itself is distorted and/or unbalanced.

2) Modified instantaneous active and reactive power (Modified $p-q$) scheme

To overcome the above drawback, Kale and Ozdemir proposed an enhancement to the conventional $p-q$ scheme in the year 2005 [46]. This modified scheme uses voltage harmonic filtering in order to make the source voltage sinusoidal; before utilizing the same for calculation of instantaneous active and reactive powers. Though both $p-q$ and modified $p-q$ schemes have almost same effectiveness to harmonic compensation under ideal supply voltage condition, modified $p-q$ scheme has been validated to possess superior harmonic compensation capability under distorted supply voltage conditions [46], [47]. However, its performance under unbalanced supply still needs improvement.

3) Instantaneous active and reactive current component ($i_d - i_q$) scheme

It has been reported in literature that, the $i_d - i_q$ scheme is more efficient than the $p-q$

scheme [48]. With the implementation of this scheme, harmonics can be mitigated under all kinds of supply voltages (ideal, distorted and unbalanced supplies).

1.2.4. Conventional PI controller for inverter DC-link voltage regulation

During steady state of operation, real power supplied by the source is equal to the real power demand of the loads plus a small power to compensate the losses occurring inside APF due to the presence of inductors and switching devices. Thus, the DC-link voltage can be maintained at a particular reference value. However, during load variation there is a real power difference between the two, which can be compensated by the charging/discharging of DC-link capacitor. If the DC-link capacitor voltage is recovered to attain the reference voltage, real power supplied by the source again becomes equal to that consumed by the load. APF uses a PI controller for minimizing the undesirable losses occurring inside the APF itself, by maintaining a constant DC-link voltage [49].

In the present work, parameters of conventional PI controller are designed using a linear model. The linear model of PWM converter along with DC-link voltage regulator is derived by applying small-signal perturbation technique [49], [50].

1.2.5. Implementation of optimization techniques

Though the APF is efficient enough for load compensation, optimal performance by the APF is always desirable. APFs with conventional PI controller yield inadequate results under a range of operating conditions [50], [51], and are also criticized for being case dependent because, when they are applied to same model with different parameters, the result varies. Moreover, the modelling of power system networks using conventional mathematical based linearized approaches is very difficult as it represents an extremely complex system that is highly nonlinear, non-stationary and involves a large number of inequality constraints. Hence load compensation capability of APF under non-ideal

supply and sudden load change conditions can be enhanced by optimizing the gains of PI controller using various optimization techniques [52]–[55].

A few solutions to the harmonic mitigation problem are found in References [56], [57], where harmonics are minimized through an objective function by optimization. In recent years, many advances have been made to solve optimization problems by the use of numerous non-traditional methods like Simulated annealing, Tabu search, Genetic algorithm (GA), Ant colony optimization (ACO), Artificial Bee colony (ABC) optimization, PSO, BFO etc. in various fields of application and research [50], [52]–[85]. Some artificial intelligence based techniques such as Fuzzy logic, Neural network and GA are exploited in Reference [71] to design a control scheme for APFs dealing with harmonics and reactive power compensation.

1) Particle swarm optimization (PSO)

The biologically inspired optimization technique called as PSO was introduced by Kennedy and Eberhart in the year 1995 [67]. It imitates the swarm behavior exhibited by bird flocks or fish schools, for optimization of nonlinear functions. A swarm consists of number of particles that fly through the feasible solution space to explore optimal solutions. Each particle in the population updates its position based on its own best exploration and best swarm overall experience that is the swarm intelligence.

PSO is being extensively used due to its simple concept, easy implementation, inexpensive computation and well-balanced mechanism to promote both local and global explorations [52], [53], [68]–[70]. Na He *et al.* demonstrated PSO to be effective and suitable for multi-objective optimal design of filters [72]. Multi-objective planning of distribution systems using PSO is also reported in literature [86]–[88]. Despite having so many advantages, it suffers from the severe drawback of premature convergence [73], [74]. Hence, though it performs well in early iterations, slows down or even becomes stagnant as the number of iterations increases. While solving problems with multiple optima, it may easily get trapped in a local optimum instead of global optimum at the end of iterations.

2) Bacterial foraging optimization (BFO)

The concept of BFO was introduced by Passino in 2002, where the social foraging behavior of *Escherichia coli* bacteria has been used to solve multi-optimal non-gradient optimization problems [75]. It is based on the evolutionary process of natural selection that tends to eliminate animals with poor foraging strategies and supports survival of the fittest. Four principal mechanisms such as chemotaxis, swarming, reproduction and elimination-dispersal are observed in bacterial population. The BFO algorithm mimics these mechanisms to map out the global optimum position in a search space. An interesting characteristic feature of BFO is that, it has its own local search mechanism through the computational chemotactic step, and reproduction with elimination-dispersal helps in global search.

Since its inception, BFO has drawn the attention of researchers from diverse fields of applications and has been applied to various real-world problems such as adaptive control [75], harmonic signal estimation [79], optimal power system stabilizers design [81], [82], and optimization of real power loss and voltage stability limit [80]. It is also hybridized with few other state-of-the-art evolutionary computation techniques in order to achieve robust and efficient search performances [76]–[78], [89]. Over certain real-world optimization problems, BFO has been reported to outperform many powerful optimization algorithms like GA, PSO, etc. in terms of convergence speed and final accuracy [50], [77]–[80]. An approach based on BFO technique was also proposed by S. Mishra in 2007 that validated optimal control of APF under sudden switch-on, load change and filter parameters variation with ideal supply voltage [50]. However, this needs an explanation towards the performance of APF when there is a huge unbalance or distortion in supply voltage along with sudden variation in load. The conventional BFO algorithm has also been reported to suffer from problems due to its fixed step size and uncontrolled particle velocities [82]–[85]. Large step size of bacteria leads to lesser accuracy though the particles arrive at the vicinity of optima quickly; whereas smaller step size slows down the convergence process.

3) Enhanced Bacterial foraging optimization (Enhanced BFO)

In an attempt to overcome the drawbacks of PSO and BFO discussed above; an improved optimization algorithm is developed here, having the combined advantages of both PSO and BFO. This makes the convergence of optimization problem towards global optimum solution even faster with significantly more accuracy. In Chapter 3 of this thesis, three types of optimization based PI controllers viz., PSO based, BFO based and Enhanced BFO based PI controllers are proposed to be implemented on APF. The results obtained under ideal, distorted and unbalanced supply conditions are compared to that obtained with APF employing conventional PI controller thus evaluating their degree of harmonic compensation.

1.2.6. Shunt APF configurations

Depending upon the type of power supply, APF configurations are broadly divided into two types, single-phase and three-phase. The single-phase APF finds its use in electric traction or rolling stock [90]–[94]. Apart from this, its utilization remains limited to only low power applications. The three-phase APFs are very popular among researchers and application engineers owing to the applications it serves and the vast usage of three-phase nonlinear loads in power system. Three-phase APFs can again be broadly categorized into three-wire and four-wire topologies. The APF for three-wire systems is used to deal with harmonics produced by nonlinear loads. On the other hand, APF for four-wire systems need to handle additional power quality issues such as neutral current and unbalanced current drawn from the utility.

The power converters that are mostly used for active power conditioning in three-phase power systems are VSI based configurations. The conventional six-switch VSI is very popular as an efficient and economical APF configuration for low-to-medium power applications. However, with the increase in demand for medium-to-high voltage, high power applications; the research progress is heading towards multilevel power converters [95]–[100]. The main objective of multilevel converter is to synthesize a staircase voltage

waveform from a number of levels of voltages. With an increase in the number of levels, the output voltage waveform approaches closer to sinusoidal nature. MLIs when used in APF instead of traditional VSI; can reduce the additional harmonics generated by the APF itself. Chapter 4 of this thesis evaluates the performance of conventional and various higher level MLI configurations (three-level, five-level, seven-level and nine-level cascaded MLI) in harmonic compensation under ideal and non-ideal supply conditions.

There is a distinctive feature for VSIs used as APFs in three-phase four-wire systems, due to the presence of an additional neutral conductor. Thus, APFs in this case need to compensate for neutral currents as well as current harmonics. Chapter 5 deals with various 2-level APF configurations, (a) split-capacitor (2C), (b) four-leg (4L) and (c) three H-bridges (3HB) topologies [19], [26], [38], [39], [47], [101]–[108]. Additionally, a three-level H-bridge (3L-HB) topology is proposed here, followed by its comparison with the 2-level counterparts in terms of component requirements, cost, compensation effectiveness, area of application etc. MLIs of level more than three should not be employed in three-phase four-wire systems, as it results in unbalance in neutral potential [109].

1.2.7. Multilevel inverter based APF

Nabae *et al* first introduced the concept of multilevel converter in the year 1975 [110]. In their work, the term "multilevel" first surfaced with the introduction of a three-level neutral-point clamped inverter, which generated a three-level quasi-square wave output instead of a conventional two-level output. Following this, many multilevel topologies have been developed [97], [111]–[117]. By increasing the number of levels of MLI, the quality of output voltage waveform can be improved. As the voltage has more number of steps, hence is more close to sinusoidal [118].

A major disadvantage associated with multilevel converters is the voltage unbalance problem encountered in higher level converters. The maximum number of attainable voltage levels is limited due to the requirement of more number of power semiconductor switches, each of which needs a related gate drive circuit. The voltage clamping

requirement, circuit layout, and packaging constraints are the other associated drawbacks. This may cause the overall system to be more expensive and complex.

However, several advantages are offered by MLIs over conventional VSIs, such as:

a) Generation of higher voltages with low harmonic content and lower (dv / dt) distortion, therefore electromagnetic compatibility problems can be reduced
b) Two-level inverters have the disadvantages like high-order harmonic noise and additional switching losses due to high-frequency commutation
c) Draw input current with very low distortion
d) Considerable reduction in size and volume, as no bulky coupling transformers or inductors are required
e) Reduce the voltage/current ratings of semiconductors and switching frequency requirements, resulting in reduced switching loss due to semiconductor devices

MLIs are basically classified into three types depending upon topologies and their principle behind generation of multilevel output voltage, namely, (i) Neutral-point clamped inverter, (ii) Flying-capacitor inverter and (iii) Cascaded H-bridge inverter. The working principle, advantages, disadvantages and applications of these MLI configurations are discussed in detail in Chapter 4. Out of these three configurations, the cascaded MLI topology is preferred to be implemented in this presented work because of the following advantages that are discussed in Chapter 4.

a) Possible number of output voltage levels is more than twice the number of DC sources
b) Component requirement in cascaded MLI is less compared to the other two MLIs
c) Modularized layout and packaging of series H-bridges makes the manufacturing process quick and cheap

1.3. Analysis Tools

Modelling of shunt APF is done in MATLAB/Simulink environment on a system with Windows 7 operating system. The testing and validation of power conditioning devices

has become more and more essential in the design and engineering process. The need for constant improvement of component modelling has led to an increase in the system prototyping. But this method has the following major drawbacks:

a) There is a big hurdle in the design process during the leap over from off-line simulation to real prototype. Hence, it is prone to many troubles related to the integration of different modules at a time.
b) The off-line, non-real-time simulation may become tediously long for any moderately complex system.

With advance in the real-time simulation techniques, RT-Lab Simulator developed by the Opal-RT technologies emerged as one of the most promising tools for real-time performance analysis of the system built models by running them on fixed-step solvers for automatic code generation [119]. RT-Lab is an industrial grade, scalable and real-time platform for simulation, control testing and related applications.

The RT-Lab is a real-time digital simulator, where simulations take place at a very high speed owing to the use of multiple numbers of processors. In other words, RT-Lab simulations mimic the real-time scenario in terms of speed of execution, in contrast with other simulation tools like MATLAB. The MATLAB/Simulink models are built in a personal computer (PC) installed with Opal RT-Lab software. The PC is connected to Opal-RT simulator via Ethernet. The results are observed in a Digital storage oscilloscope (DSO) connected to RT-Lab simulator via connecting probes as illustrated in Figure 1.6. Once the model has been prepared in MATLAB, RT-Lab uses Real-Time Workshop to convert the separated models into code for compilation as subsystem simulations on each target processor. Data from the model is directed to the user via a special subsystem, called the Console. Here the signals being generated can be viewed and parameters can be changed on-line to the simulation.

S1 is connected to master reset signal of OP5142 board. Pressing this button forces the FPGA (Field-Programmable Gate Array) reconfiguration, and sends a reset signal to all OP5142 subsystems. JTAG1 gives access to OP5142 JTAG (Joint Test Action Group) chain. It configures the flash memory with its default configuration file. Depending upon

"JUMP4" jumper presence, this interface may give access to both FPGA and CPLD (Complex Programmable Logic Device) configurations, or only the FPGA one. If the "JUMP4" jumpers are set to independent mode, JTAG2 gives access to the CPLD JTAG configuration interface. JTAG connection enables users to manually program the reprogrammable components on the board. JUMP4 enables the JTAG interface of OP5142 CPLD and FGPA to be daisy-chained. JTAG3 gives access to the PCIe (Peripheral Component Interconnect Express) Bridge JTAG interface. JTAG4 gives access to the Texas Instrument Serializer-Deserializer (SerDes) JTAG interface. JP1 implements all data and power transfers needed to be done with external world. It carries to the external PCIe adapter: (i) Synchronization pulse train to a RTSI (Real time system integration) connector; (ii) Data communication packets to the PCIe bus; (iii) Power supply. J1, J2 and J3 exchange all I/O-related data to I/O module, including identification data, serial communication with I²C (Inter-integrated circuit) devices and user I/O dataflow. JUMP1 enables the write protection of the EEPROM (Electrically erasable programmable Read-only memory) located on OP5142. JUMP2 enables the developer to select the way OP5142 FPGA should be configured that is (a) JTAG configuration, or (b) Slave parallel configuration (from the Flash memory). In normal use, the FPGA should always be configured using the Slave parallel feature. JUMP3 is to enable the developer to write some reserved sectors of the configuration flash memory. The PCI-Express port on OP5142 adapter board allows the users to connect the distributed processors together and operate at faster cycle times than ever before. This real-time link takes advantage of the FPGA power to deliver up to 2.5 Gbits/s full-duplex transfer rates. The OP5142 board is used to translate a Simulink design built using particular library blocks into HDL.

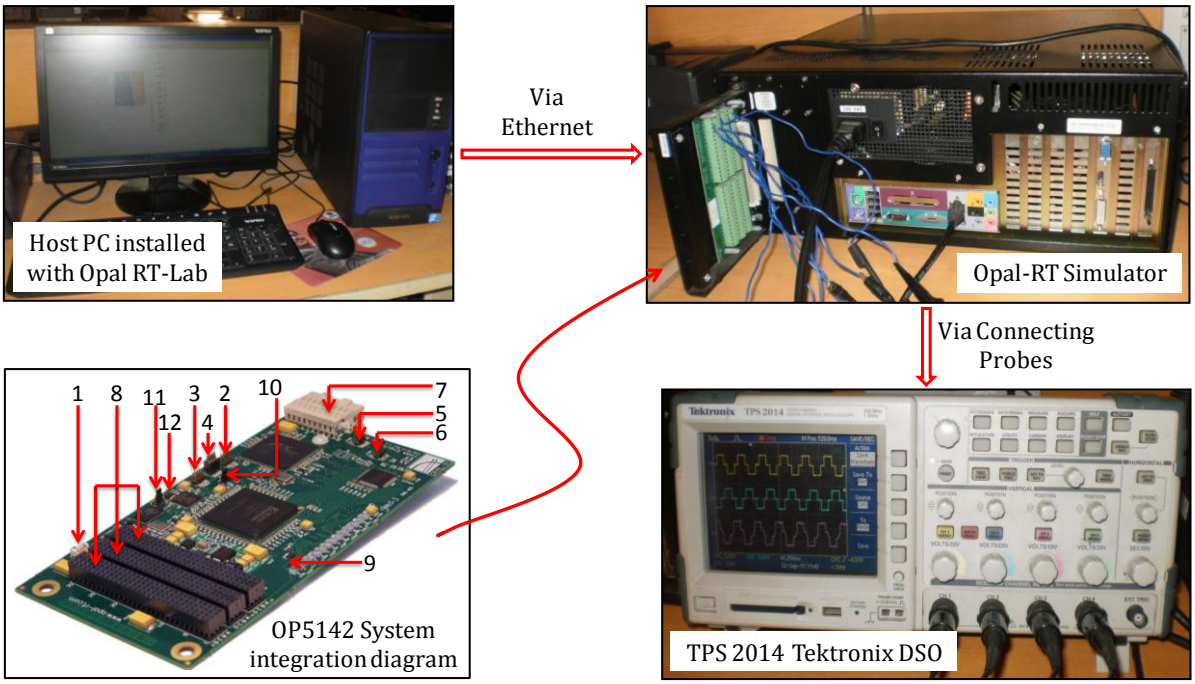
Technical specifications of OP5142 RT-Lab:

(i) Digital I/O:

Number of channels: 256 input/output configurable in 1- to 32-bit groups

Compatibility: 3.3 V

Power-on state: High impedance



#	Name	Description
1	S1	FPGA Engine manual reset
2	JTAG1	FPGA JTAG interface
3	JTAG2	CPLD JTAG interface
4	JUMP4	JTAG Architecture selection
5	JTAG3	PCIe Bridge JTAG interface
6	JTAG4	SerDes JTAG interface
7	JP1	PCIe, Synchronization bus and power supply
8	J1/J2/J3	Backplane data, ID and I²C interface
9	JUMP1	Identification EEPROM write protection
10	JUMP2	FPGA configuration mode selection
11	JUMP3	Flash memory Write protection
12	J4	Flash memory forced programmation voltage

**FPGA - Field-Programmable Gate Array, JTAG - Joint Test Action Group, CPLD - Complex Programmable Logic Device, PCIe - Peripheral Component Interconnect Express, SerDes - Serializer/Deserializer, I²C – Inter-Integrated Circuit, EEPROM - Electrically Erasable Programmable Read-Only Memory*

Figure 1.6: RT-Lab set up and OP5142 system integration showing its components

(ii) Bus:

Dimensions (not including connectors): PCI-express x1

Data transfer: 2.5 Gbit/s

(iii) FPGA:

Device: Xilinx Spartan 3

I/O Package: fg676

Embedded RAM available: 216 Kbytes

Clock: 100 MHz

Platform options: XC3S5000

Logic slices: 33,280

Equivalent logic cells: 74,880

I/O lines: 489

Technical specifications of the computer installed with RT-Lab software:

Microsoft Windows XP (32-bit version)

Xilinx ISE design suite v10.1 with IP update 3

Xilinx System Generator for DSP v10.1

MATLAB R2007b

1.4. Motivation

There are several factors that encouraged deciding this topic for the thesis. Still, the primary sources of motivation for this work are:

1) Proliferation of nonlinear loads is causing alarming rise of harmonic pollution, resulting in many harmful consequences. Traditional low cost passive filters for harmonic mitigation in industrial power system suffer from several drawbacks.

2) Most of the APF control strategies existing in literature are incompetent under non-ideal supply voltage conditions.

a) $p-q$ scheme yields acceptable values of source current THDs only under ideal supply
b) Modified $p-q$ scheme though capable to compensate harmonics under ideal and distorted supply conditions, yields poor results under unbalanced supply

3) Though several frequency-domain control methods for APF exist in literature, the time-domain based control schemes have been preferred to be studied here, due to the various advantages they offer, as discussed in Section 1.2.3.

4) The conventional PI controller tuning has some major drawbacks. These are empirical in nature and require extensive experimentation. Furthermore, modelling of power system network using conventional mathematical based linearized approaches is very difficult as it represents a highly complex, nonlinear and time-varying system.

5) Optimization of APF performance is always desirable. Hence, implementation of non-gradient evolutionary technique called as PSO is proposed to find out optimized values of PI controller gains.

6) The inevitable drawback of premature convergence in PSO degrades the harmonic compensation capability of APF.

7) Since BFO has been validated to outperform many other optimization tools like GA, PSO in terms of convergence speed and final accuracy in various real-world problems, BFO is proposed to be implemented.

8) To further enhance the rate of convergence and hence the APF functionality, a novel Enhanced BFO algorithm is proposed having the combined advantages of both PSO and BFO.

9) On account of the numerous advantages offered by MLIs over conventional VSIs as depicted in Section 1.2.7, MLIs are found to be more effective for medium and high voltage applications as compared to the conventional two-level VSI topologies. Hence, the MLI topology is chosen to be implemented in shunt APF.

10) MLIs can be diode-clamped, flying-capacitor or cascaded type. However, cascaded MLI is preferred to be implemented in this work due to the reasons mentioned in Section 1.2.7.

11) The various VSI-based APF topologies for three-phase three-wire systems (conventional two-level and multilevel VSIs) and four-wire systems (2C, 4L, 3HB and 3L-HB VSIs) being discussed in this thesis need to be compared for selection of a particular configuration for specific application.

12) With each topology, the DC-link capacitor requirements change. Irrespective of the number and rating of capacitors used in any particular topology, the DC-link voltages they are subjected to, need to be maintained constant for an effective compensation. Therefore, optimizing the PI controller gains for regulation of DC-link voltage for each APF topology is essential.

13) Testing and validation of power conditioning devices has become very essential in the design and engineering process. To find out the effectiveness of discussed control schemes, optimization-based PI controllers and topologies of APF in real-time, the simulation results are required to be validated with RT-Lab.

1.5. Scope of the Thesis

1) Modelling of shunt APF
    a) Simulation in MATLAB/Simulink environment, followed by real-time analysis in RT-Lab for APF employing
        (i) $p - q$ scheme
        (ii) Modified $p - q$ scheme
        (iii) $i_d - i_q$ scheme
    b) Comparison of effectiveness of the above control strategies in current harmonics, current unbalance and neutral current compensation under ideal, distorted and unbalanced supplies; with sudden load change conditions

2) Modelling and simulation of shunt APF employing PSO-based PI controller
3) Modelling and simulation of shunt APF employing BFO-based PI controller
4) Development of an Enhanced BFO algorithm by the hybridization of PSO and BFO
5) Modelling and simulation of shunt APF employing Enhanced BFO-based PI controller
6) Comparison of performance for APFs employing conventional PI, PSO-PI, BFO-PI, and Enhanced BFO-PI controllers
7) Analysis of various VSI topologies for three-phase three-wire shunt APF such as
    a) Conventional VSI topology
    b) Multilevel VSI topology (more specifically cascaded MLI)
8) Analysis of various VSI topologies for three-phase four-wire shunt APF such as,
    a) Split-capacitor (2C) topology
    b) Four-leg (4L) topology
    c) Three H-bridges (3HB) topology
    d) Three-level H-bridge (3L-HB) topology
9) Optimizing the PI controller gains for improved regulation of DC-link voltage for each of the above mentioned APF topologies using optimization technique; as the constraints associated with DC-link capacitors vary with each topology of APF.
10) Comparison of topologies based upon the number of switches, DC-bus capacitors, voltage and current sensors required, need of coupling transformer, capability in terms of compensated source current THD, overall cost, and applications.

1.6. Thesis Organization

The entire thesis is divided into six chapters. The organization of the thesis and a brief chapter-wise description of the work presented are as follows:

Chapter 1 provides an overview of the thesis pointing out various causes and detrimental consequences of current harmonics in power systems. Traditional method of harmonic

compensation with passive power filter is illustrated, clearly specifying its advantages and disadvantages. A detailed literature survey on APFs, various existing control schemes, optimization techniques for performance enhancement, and topologies for three-phase three-wire and four-wire systems is presented. Works related to the thesis that are reported in literature are illustrated. Finally, the motivation behind presented work, objectives, and the organization of thesis are outlined.

Chapter 2 discusses various APF control schemes for reference compensation filter current extraction, DC-link voltage regulation of VSI and design of conventional PI controller. This is followed by a comparison between $p-q$, modified $p-q$ and i_d-i_q control schemes. Evaluations are carried out for compensation of current harmonics, neutral current and unbalanced currents in three-phase four-wire systems.

Chapter 3 proposes the implementation of optimization techniques like PSO and BFO for effective regulation of inverter DC-link voltage, under sudden load change and non-ideal supply voltage conditions. Both the optimization algorithms have been explained in detail, clearly citing their mechanisms and iterative algorithms. An Enhanced BFO algorithm is proposed in this chapter by the hybridization of PSO and BFO, in order to overcome the shortcomings of usual PSO and BFO, discussed in Chapter 1. The developed algorithm is tested for optimization of PI controller gains, which consequently affects the overall harmonic mitigation.

Chapter 4 deals with the VSI topologies suitable for active power filtering in three-phase three-wire power systems. As the conventional 2-level APF topologies extensively studied in previous chapters are popular only in low power applications, this chapter concentrates on MLI topologies pertinent for medium-to-high power applications. The working principles, advantages, disadvantages and applications of diode-clamped, capacitor-clamped and cascaded MLIs configurations are presented briefly. The modulation strategies employed in MLIs are also discussed. Taking into account the various advantages offered by cascaded MLI, here cascaded 3, 5, 7 and 9-level APF topologies are studied. As per literature, MLIs make use of a lot of capacitors, making the DC-link voltage regulation a difficult task. A solution to this is depicted in this chapter

with optimal regulation of DC-link voltage using the Enhanced BFO technique proposed in Chapter 3.

Chapter 5 contains a study of various two-level three-phase four-wire topologies like split-capacitor (2C), four-leg (4L) and three H-bridges (3HB), which differ from the three-wire topologies due to the presence of an additional neutral conductor. A three-level H-bridge (3L-HB) topology is proposed enthused by the advantages offered by MLIs. The regulation of DC-link voltage for each topology is put forth separately, since the DC-link capacitor requirements vary with topology. For effective DC-bus voltage regulation, the proposed Enhanced BFO technique is implemented to tune the PI controller. Investigations are carried out to compare the compensation capabilities, component requirements and areas of application of discussed topologies.

Chapter 6 concludes the thesis by summarizing the contributions and conclusions of all the chapters. Ultimately, the final section explores future directions of research that emerged as an outcome of the work presented in this thesis.

Chapter 2

Shunt Active Power Filter And Its Control Schemes

2.1. Introduction

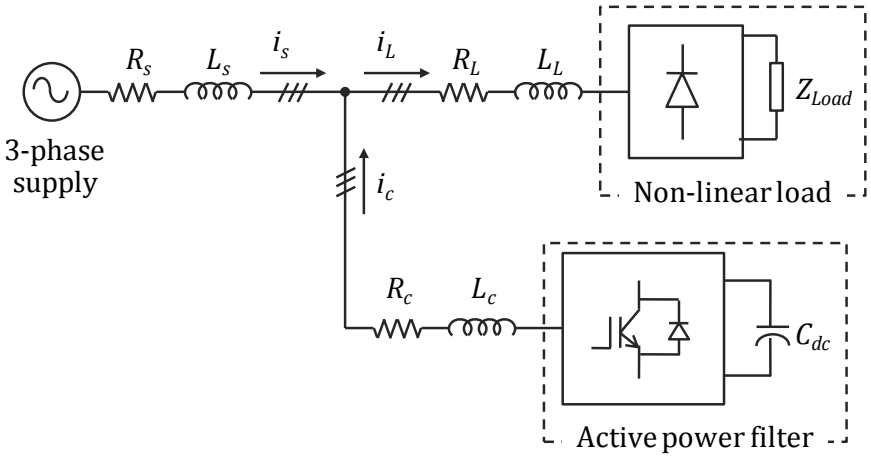
The shunt APF can be controlled to execute selective compensation. It can be made to compensate the harmonics in the source current, load current or an arbitrarily chosen set of harmonic components present in them. However, the conventional shunt APF is intended to perform harmonic current suppression, reactive power compensation and balancing of three-phase currents. The compensation principle behind a shunt APF is injection of harmonics of equal magnitude and opposite phase as that of load current harmonics at the PCC between the source and the load as given by (2.1).

$$i_c(t) = i_s(t) - i_L(t) \tag{2.1}$$

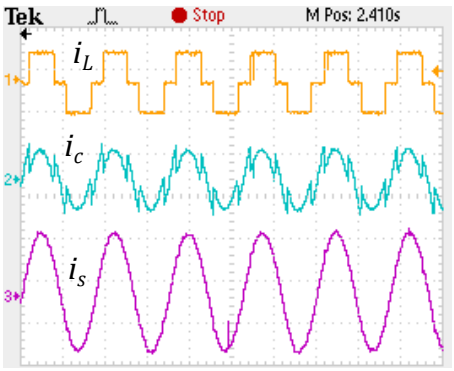
Compensation currents generated by the filter are injected into the power system in order to assure that sinusoidal, balanced and compensated current is drawn from the utility with significant reduction in current harmonic distortion. The compensation principle of shunt APF is depicted in Figure 2.1 with the help of a schematic diagram of APF system along with a nonlinear load, followed by its associated waveforms for load current (i_L), filter current (i_c) and source current after compensation (i_s).

The literature survey on APF control schemes presented in Chapter 1 reveals that, most APF control schemes render ineffective results under non-ideal conditions of supply. Also, selection of proper reference compensation current extraction scheme plays the

most crucial role in APF performance. This chapter mainly deals with the comparison of time-domain based $p-q$, modified $p-q$ and i_d-i_q control schemes. Investigations are carried out for three-phase four-wire systems considering ideal, distorted and unbalanced supply conditions with sudden load change and unbalanced loading scenarios. The effectiveness is assessed in terms of current harmonics, excessive neutral current and current unbalance compensation by means of simulation and RT-Lab results. Here, the APF is comprised of a Hysteresis PWM based VSI. Power loss taking place inside VSI is effectively minimized with inverter DC-link voltage regulation using a PI controller, the gains being extracted using small-signal perturbation technique.



(a)



(b)

Figure 2.1: Compensation principle of shunt APF, (a) Schematic diagram, (b) Waveforms for load current (i_L), filter current (i_c) and compensated source current (i_s)

This chapter commences with an introduction to the shunt APF, describing its basic compensation principle. The general description of shunt APF is presented in Section 2.2. In Section 2.3, the $p-q$, modified $p-q$ and i_d-i_q control strategies of APF for extraction of reference compensation currents are illustrated. Section 2.4 depicts about inverter DC-link voltage regulation for the minimization of undesirable APF losses. Design of conventional PI controller and finding out its gain values are discussed in the next section. The APF system configuration, system parameter values used during simulation, and extensive results obtained with simulations and RT-Lab are presented in Section 2.6. Investigations are performed for three different supply conditions viz. ideal, distorted and unbalanced, with sudden changes in load, along with the simultaneous comparison of results. Finally, Section 2.7 gives a summary of the chapter.

2.2. Shunt APF

The two major building blocks of shunt APF are (a) PWM converter and (b) control scheme for generation of pulses for converter switches, as depicted in Figure 2.2. The Pulse-width modulated (PWM) converter for APF has many configurations, amongst which the standard inverter type configuration is most widely used and discussed as given in [26] and the references there-in.

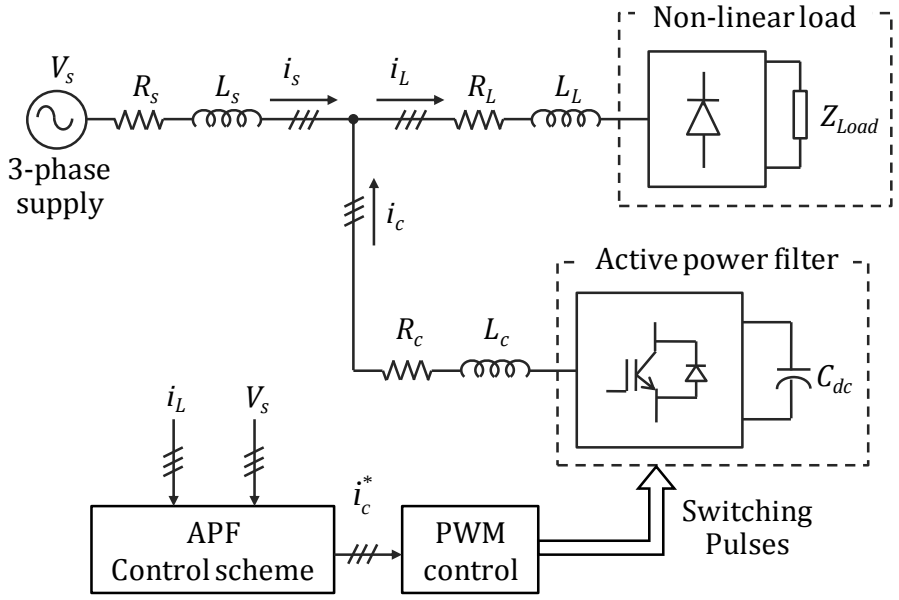


Figure 2.2: General configuration of a shunt APF system

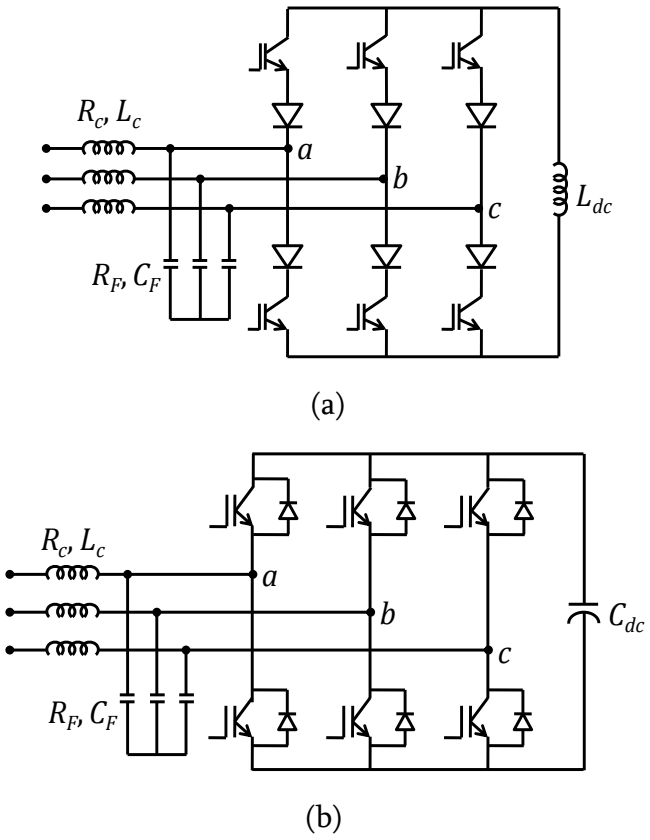


Figure 2.3: Inverter configurations for APF, (a) CSI configuration, (b) VSI configuration

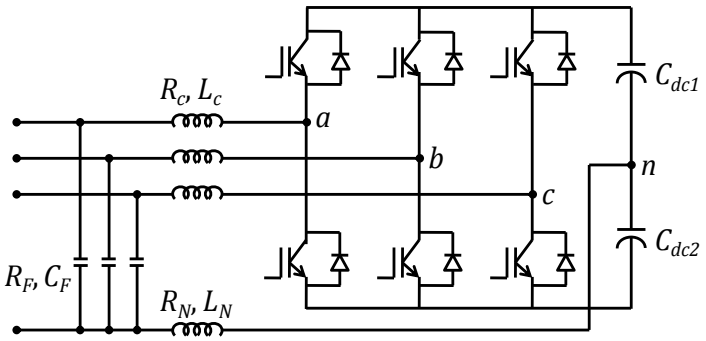
APFs are generally developed with either CSI or VSI as discussed in Section 1.2.2 of Chapter 1. Figure 2.3 (a) shows the CSI structure that behaves as a non-sinusoidal current source to meet the harmonic current requirement of the nonlinear loads. They present good reliability, but have important losses and require higher values of parallel capacitor filters at the AC terminals to remove unwanted current harmonics [26], [31]. A diode is used in series with the self-commutating device (IGBT) for reverse voltage blocking. Moreover, they cannot be used in multilevel or multistep configurations to allow compensation at higher power ratings.

The other converter used in APFs is VSI, shown in Figure 2.3 (b). This converter is more convenient for active power filtering applications, since it is lighter, cheaper, and expandable to multilevel and multistep versions, for improved performance at high power rating applications with lower switching frequencies [26], [33]. The VSI has to be

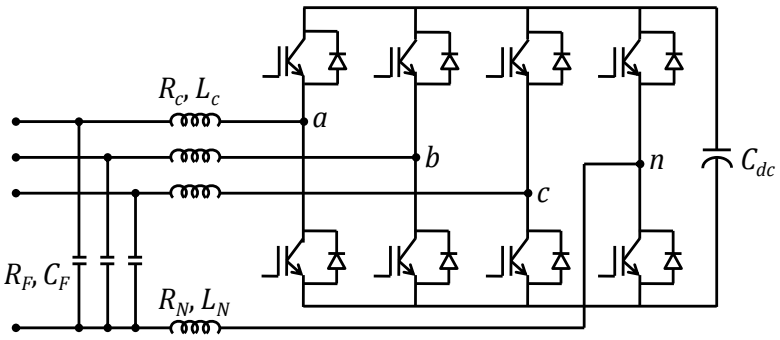
connected to the AC mains through coupling reactors. An electrolytic capacitor keeps the DC-link voltage constant and ripple-free [31]. Therefore, here the use of VSI is preferred.

To employ APF in a three-phase four-wire power system, conventionally two types of configurations are used. One is a three-leg six-switch structure with the neutral conductor being connected to midpoint of DC-link capacitor as depicted in Figure 2.4 (a) and the other one is a four-leg eight-switch structure, where an additional fourth leg is provided exclusively for neutral current compensation as shown in Figure 2.4 (b). The latter configuration is preferred for implementation, as many researchers appoint this configuration as the most proficient alternative to be used in shunt APFs [38], [47], [105]. The three-leg split-capacitor configuration suffers from several shortcomings such as:

a) Control circuit is somewhat complex
b) Voltages of the two capacitors of split-capacitor need to be properly balanced
c) Large DC-link capacitors are required



(a)



(b)

Figure 2.4: Conventional three-phase four-wire APF configurations, (a) Three-leg six-switch VSI, (b) Four-leg eight-switch VSI

Despite of the fact, split-capacitor topology is seldom preferred owing to less number of switching devices and lower switching losses compared to the eight-switch topology. However, the higher order harmonics generated in the eight-switch configuration due to frequent switching of semiconductor devices can be eliminated by the use of RC high-pass filter as shown in Figure 2.4 (b) and switching losses occurring in the VSI can also be minimized by the use of DC-link voltage regulator. Moreover, the four-leg APF has simple DC-link voltage controller, requires small DC-link capacitor, and the control scheme is also quite simple to implement.

In this chapter, a three-phase four-wire power system is considered. This is because, a four-wire system would be more appropriate compared to a three-wire system, to carry out comparative study of various APF control schemes based on their abilities to compensate current harmonics, neutral current and unbalance in source current. The analyses in this chapter are done taking eight-switch VSI configuration of APF, due to the above discussed advantages over six-switch VSI.

2.3. Control Schemes for APF

For proper current harmonic compensation, it is very crucial to choose an appropriate reference compensation current extraction scheme. The actual filter currents are forced to follow the reference compensation currents, obtained with any of the APF control schemes. The continuously tracked actual filter currents ($i_{ca}, i_{cb}, i_{cc}, i_{cn}$) are compared with the reference filter currents ($i_{ca}{}^{*}, i_{cb}{}^{*}, i_{cc}{}^{*}, i_{cn}{}^{*}$) in a Hysteresis band current controller as shown in Figure 2.5 (a). Switching pattern for the IGBTs inside VSI is generated as per the following rule [23], [120], which can be realized from Figure 2.5 (b).

a) If $i_{ca} < (i_{ca}{}^{*} - HB)$,

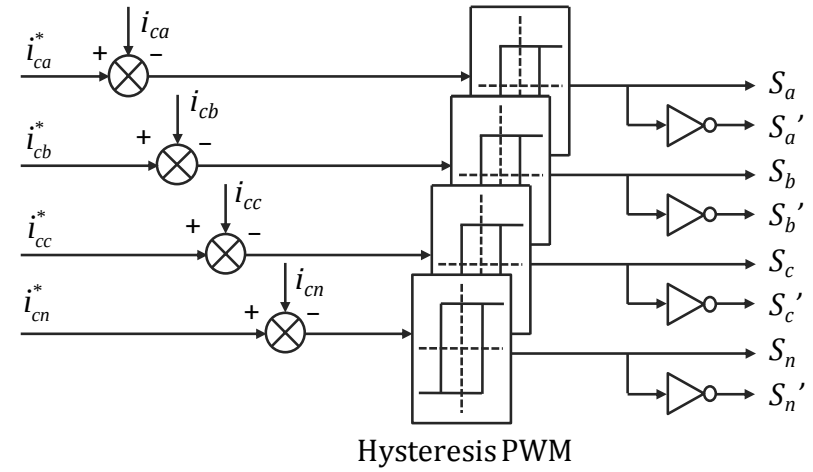
   Upper switch is OFF and lower switch is ON for leg-a.

b) If $i_{ca} > (i_{ca}{}^{*} + HB)$,

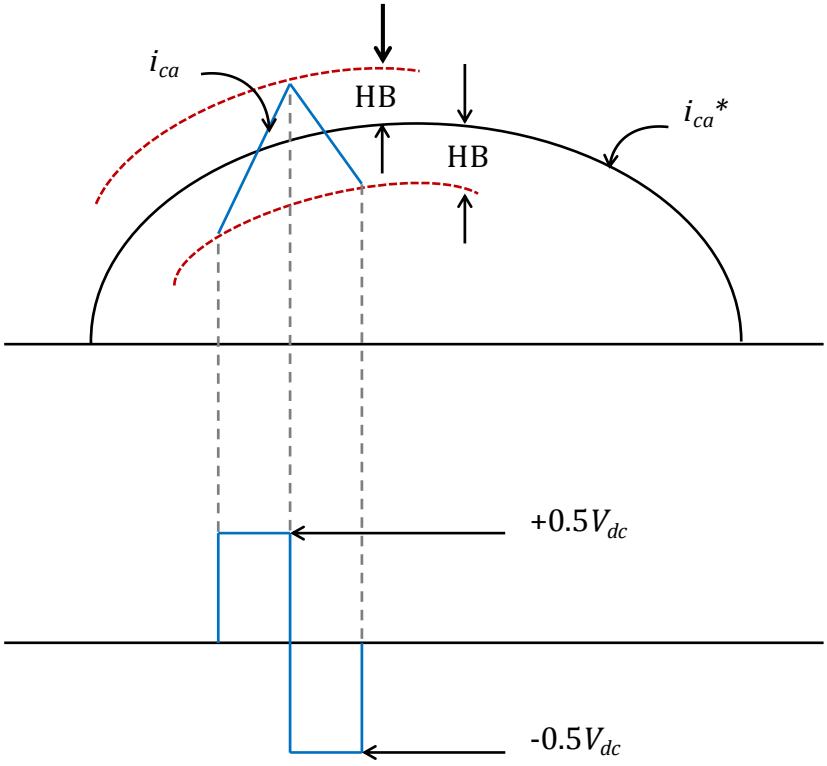
   Upper switch is ON and lower switch is OFF for leg-a.

Here, HB represents the Hysteresis bandwidth.

Similarly, the switching signals for legs b, c and n of VSI are produced using their corresponding actual and reference filter currents. Hysteresis PWM is intended to be used here for instantaneous current harmonic compensation by the shunt APF, on account of its simple implementation, good accuracy and quick prevail over fast current transitions [121], [122].



(a)



(b)

Figure 2.5: Hysteresis PWM current controller, (a) Generation of switching signals, (b) Current and voltage waveforms

The main drawback of this PWM technique is its high switching frequency, which results in generation of some higher order harmonics due to the inherent switching of semiconductor devices inside the inverter. These unwanted additional harmonics present in filter current are filtered out using a small RC high-pass filter at the output of VSI. The VSI in turn generates required compensation filter currents to be injected into the AC lines at PCC.

2.3.1. Instantaneous active and reactive power ($p-q$) method

Though various APF control schemes for extraction of reference compensation currents have been proposed so far in the literature, the $p-q$ method based on instantaneous active and reactive powers is most popular. The control block diagram for entire $p-q$ scheme has been depicted in Figure 2.6.

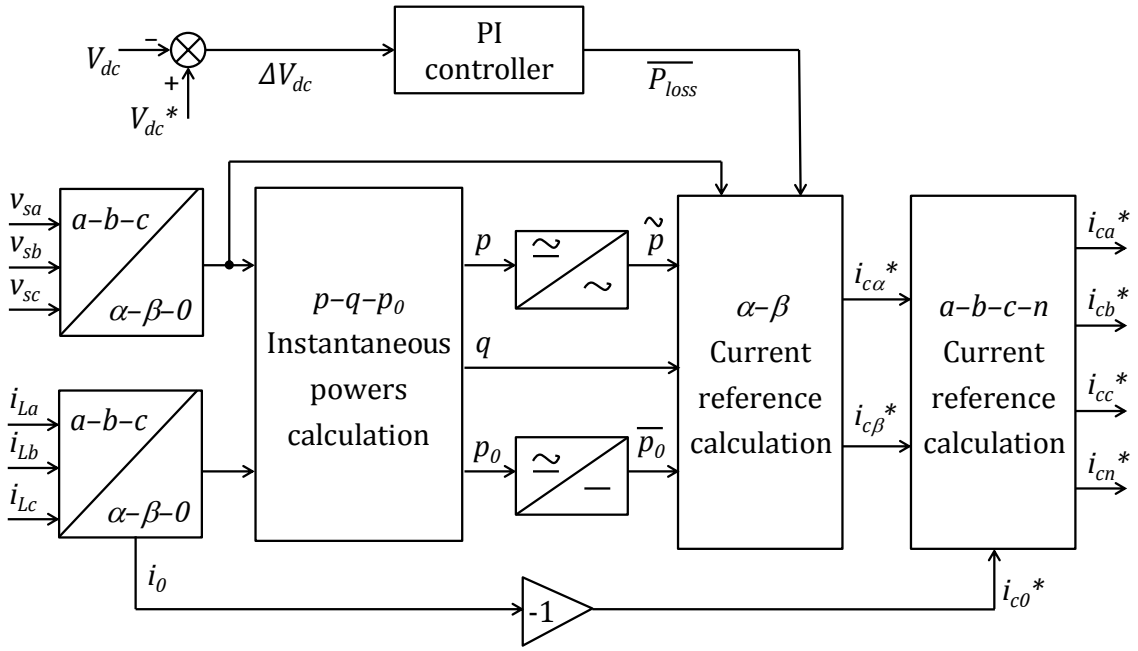


Figure 2.6: Control block diagram for $p-q$ scheme

The instantaneous load currents in three phases (i_{La}, i_{Lb}, i_{Lc}) and source voltages in three phases (v_{sa}, v_{sb}, v_{sc}) are tracked using sensors, followed by a coordinate transformation from $a-b-c$ to $\alpha-\beta-0$ as follows.

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{2.2}$$

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.3}$$

The zero-sequence current (i_0) exists only in three-phase four-wire power systems. Therefore, for simplification of calculations, i_0 can be neglected when the $p-q$ theory is applied to three-phase three-wire systems. Similarly, the zero-sequence voltage (v_0) comes into picture only when there are harmonics and/or unbalance in the mains voltage.

The instantaneous values of active power (p), reactive power (q) and zero-sequence power (p_0) are calculated by multiplying the instantaneous $\alpha-\beta-0$ components of currents and voltages as per (2.4). Each of these powers has an oscillating/AC component and an average/DC component as shown in (2.5), (2.6) and (2.7).

$$\begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{2.4}$$

$$p = \bar{p} + \tilde{p} \tag{2.5}$$

$$q = \bar{q} + \tilde{q} \tag{2.6}$$

$$p_0 = \overline{p_0} + \widetilde{p_0} \tag{2.7}$$

Here, $\bar{p}$, $\bar{q}$ and $\overline{p_0}$ are AC components of p, q and p_0 respectively. Similarly, $\tilde{p}$, $\tilde{q}$ and $\widetilde{p_0}$ represent corresponding DC components. For reactive power and harmonic compensation, the entire reactive power (q) and oscillating component of active power ($\tilde{p}$) are utilized for calculation of reference filter currents in $\alpha-\beta$ coordinates using (2.8).

$$\begin{bmatrix} {i_{c\alpha}}^* \\ {i_{c\beta}}^* \end{bmatrix} = \frac{1}{\sqrt{{v_\alpha}^2 + {v_\beta}^2}} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} + \Delta\bar{p} \\ -q \end{bmatrix} \tag{2.8}$$

The additional average power required to compensate for the losses occurring inside VSI due to the switching of semiconductor devices is given by (2.9).

$$\Delta\bar{p} = \overline{p_0} + \overline{P_{loss}} \tag{2.9}$$

Here, $\overline{p_0}$ is the power required to maintain energy balance inside VSI. Whereas, $\overline{P_{loss}}$ is the average loss occurring inside VSI, which is obtained from DC-link voltage regulator as per (2.10). It is designed to give good compensation and excellent transient response. Actual DC-link voltage (V_{dc}) is compared with a reference ($V_{dc}{}^{*}$) and the error (ΔV_{dc}) is processed in a PI controller.

$$\overline{P_{loss}} = K_p \Delta V_{dc} + K_i \int \Delta V_{dc} \cdot dt \tag{2.10}$$

The zero-sequence reference compensation current ($i_{c0}{}^{*}$) should be same as the zero-sequence component detected in load current (i_0), but in opposite sign; so that it can provide the required zero-sequence current compensation as given by (2.11).

$$i_{c0}{}^{*} = -i_0 \tag{2.11}$$

Finally, reference filter currents in the four wires of VSI can be obtained by following (2.12) and (2.13).

$$\begin{bmatrix} i_{ca}{}^{*} \\ i_{cb}{}^{*} \\ i_{cc}{}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{c0}{}^{*} \\ i_{c\alpha}{}^{*} \\ i_{c\beta}{}^{*} \end{bmatrix} \tag{2.12}$$

$$i_{cn}{}^{*} = i_{ca}{}^{*} + i_{cb}{}^{*} + i_{cc}{}^{*} \tag{2.13}$$

In this scheme, for the system voltages and currents to be in phase synchronization, the utilization of phase-locked loop (PLL) is highly essential. Furthermore, the multiplication of instantaneous load currents and voltages while calculating the instantaneous active and reactive powers, leads to amplification of harmonic content. Thus, it gives rise to imprecise harmonic compensation under non-ideal distorted and unbalanced conditions of supply voltage, though the compensation under ideal supply is acceptable.

2.3.2. Modified $p - q$ method

To overcome the above drawback, Kale and Ozdemir proposed a modification to the conventional $p - q$ scheme in the year 2005. This scheme uses voltage harmonic filtering in order to make the source voltage sinusoidal; before utilizing the same for calculation of instantaneous active and reactive powers. Control block diagram for the entire method of reference current generation using modified $p - q$ scheme is illustrated in Figure 2.7.

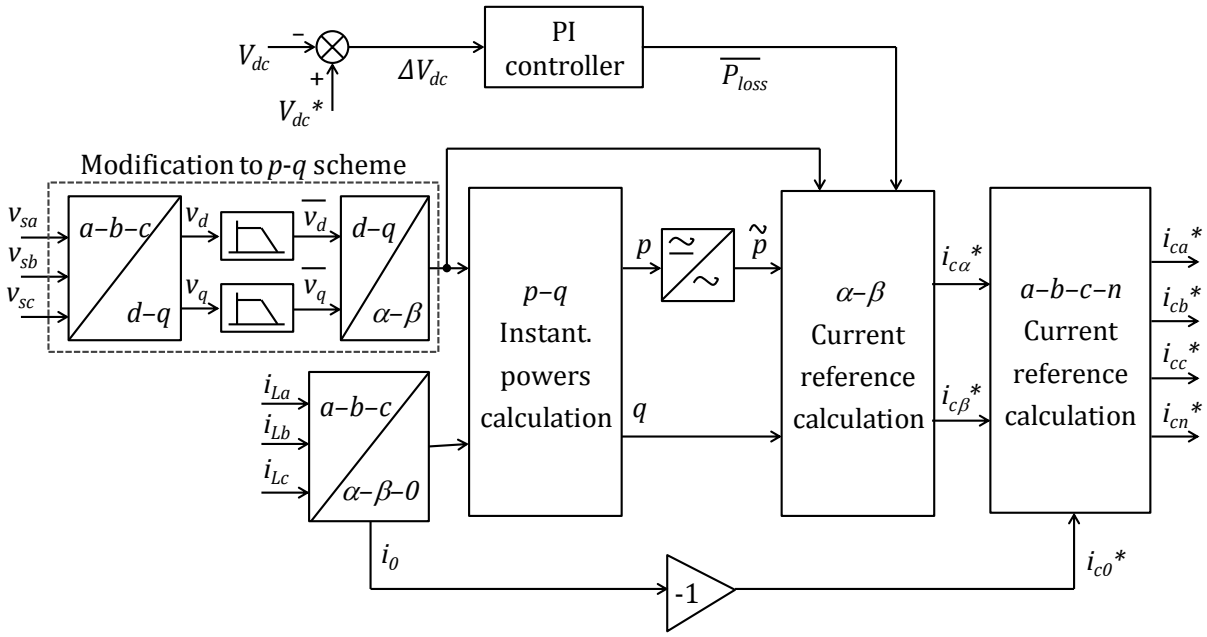


Figure 2.7: Control block diagram for modified $p - q$ scheme

The three-phase supply voltages (v_{sa}, v_{sb}, v_{sc}) are tracked and then transformed from $a - b - c$ coordinates to $d - q$ coordinates using Park's transformation given by (2.14).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\omega t & \cos\omega t \\ -\cos\omega t & -\sin\omega t \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.14}$$

Here ω represents the rotational speed of synchronously rotating $d - q$ axes. The voltages v_d and v_q thus obtained are then subjected to harmonic filtering by use of 5th order low-pass filters with cut-off frequency of 50 Hz each. Voltage harmonic filtering is done in this control scheme in order to filter out the harmonics in source voltage thereby making

it balanced and sinusoidal. Since, the zero-sequence voltage component is filtered out; the zero-sequence power (p_0) is always zero. The outputs of harmonic voltage filtering, $\overline{v_d}$ and $\overline{v_q}$ are then transformed into $\alpha - \beta$ coordinates using (2.15).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} \overline{v_d} \\ \overline{v_q} \end{bmatrix} \tag{2.15}$$

This is followed by the same procedure of reference compensation current extraction as done in case of conventional $p - q$ method.

2.3.3. Instantaneous active and reactive current component $(i_d - i_q)$ method

Initially, the mains voltages (v_{sa}, v_{sb}, v_{sc}) and load currents (i_{La}, i_{Lb}, i_{Lc}) in $a - b - c$ coordinates are transformed into a stationary reference frame of $\alpha - \beta$ coordinates.

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.16}$$

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{2.17}$$

The load current is decoupled into its respective active and reactive components in $d - q$ reference frame using Park's transformation.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{2.18}$$

Angle θ is obtained from instantaneous voltage vectors as follows,

$$\theta = \omega t = \tan^{-1}\left(\frac{v_{s\beta}}{v_{s\alpha}}\right) \tag{2.19}$$

Here ω represents the speed of synchronously rotating $d - q$ frame. The voltage vector angle θ is a constantly increasing function of time under ideal mains condition, whereas this is not the case under non-ideal supply, as it is sensitive to the presence of harmonics

and/or unbalance in supply voltage. The voltage and current space vectors in stationary $(\alpha - \beta)$ and synchronous $(d - q)$ reference frames are illustrated in the Figure 2.8.

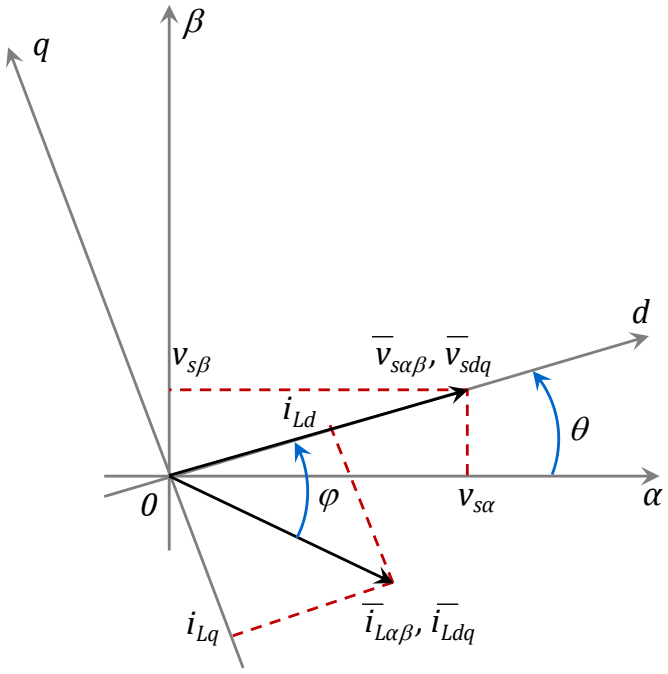


Figure 2.8: Voltage and current space vectors in the stationary $(\alpha - \beta)$ and synchronous $(d - q)$ reference frames

The d-axis component of mains voltage is given by,

$$v_{sd} = |\bar{v}_{sdq}| = |\bar{v}_{s\alpha\beta}| = \sqrt{(v_{s\alpha})^2 + (v_{s\beta})^2} \tag{2.20}$$

The q-axis component is always null i.e. $v_{sq} = 0$.

Hence, instantaneous $d - q$ axes currents can be calculated as,

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{1}{\sqrt{(v_{s\alpha})^2 + (v_{s\beta})^2}} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ -v_{s\beta} & v_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{2.21}$$

Both i_{Ld} and i_{Lq} consist of an average/DC component and an oscillating/AC component as indicated in (2.22).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} i_{Ld1h} + i_{Ldnh} \\ i_{Lq1h} + i_{Lqnh} \end{bmatrix} \tag{2.22}$$

Where, i_{Ld1h} and i_{Lq1h} indicate the fundamental frequency components of i_{Ld} and i_{Lq}.

The oscillating components of i_{Ld} and i_{Lq} i.e., i_{Ldnh} and i_{Lqnh} are filtered out using 2nd order Butterworth type low-pass filters with cut-off frequency of 25 Hz each.

The total active current required to maintain a constant DC-link capacitor voltage and to compensate the power losses occurring inside the APF is represented by i_{d1h}. This is the output signal of PI controller used to minimize the DC-link voltage error ΔV_{dc}, as defined in (2.23).

$$i_{d1h} = K_p \Delta V_{dc} + K_i \int \Delta V_{dc} \cdot dt \tag{2.23}$$

According to $i_d - i_q$ control strategy, only the average value of d-axis component of load current should be drawn from the supply. Hence, the currents i_{Ldnh} and i_{Lqnh} along with i_{d1h} are utilized to generate reference filter currents ${i_{cd}}^*$ and ${i_{cq}}^*$ in $d - q$ coordinates.

$${i_{cd}}^* = -i_{Ldnh} + i_{d1h} \tag{2.24}$$

$${i_{cq}}^* = -i_{Lqnh} \tag{2.25}$$

This is followed by inverse Park's transformation giving away the reference compensation currents ${i_{ca}}^*$, ${i_{cb}}^*$, ${i_{cc}}^*$ and ${i_{cn}}^*$ in the four wires as described in (2.26) and (2.27).

$$\begin{bmatrix} {i_{ca}}^* \\ {i_{cb}}^* \\ {i_{cc}}^* \end{bmatrix} = \begin{bmatrix} \sin \omega t & \cos \omega t & 1 \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} {i_{cd}}^* \\ {i_{cq}}^* \\ {i_{c0}}^* \end{bmatrix} \tag{2.26}$$

$${i_{cn}}^* = {i_{ca}}^* + {i_{cb}}^* + {i_{cc}}^* \tag{2.27}$$

The zero-sequence reference compensation current ${i_{c0}}^*$ in (2.26) can be obtained by using the expression, ${i_{c0}}^* = -i_0$. In Figure 2.9, the block diagram for reference current generation employing $i_d - i_q$ control scheme has been illustrated.

As discussed earlier in this section, $p - q$ and modified $p - q$ schemes involve multiplication of instantaneous voltages and currents leading to amplification of harmonic content. On the contrary, $i_d - i_q$ scheme executes computations involving only current quantities. In to the bargain, $i_d - i_q$ scheme does not require a PLL, as the synchronously rotating $d - q$ frame itself is derived directly from mains voltages. Consequently, many problems related to synchronization can be avoided.

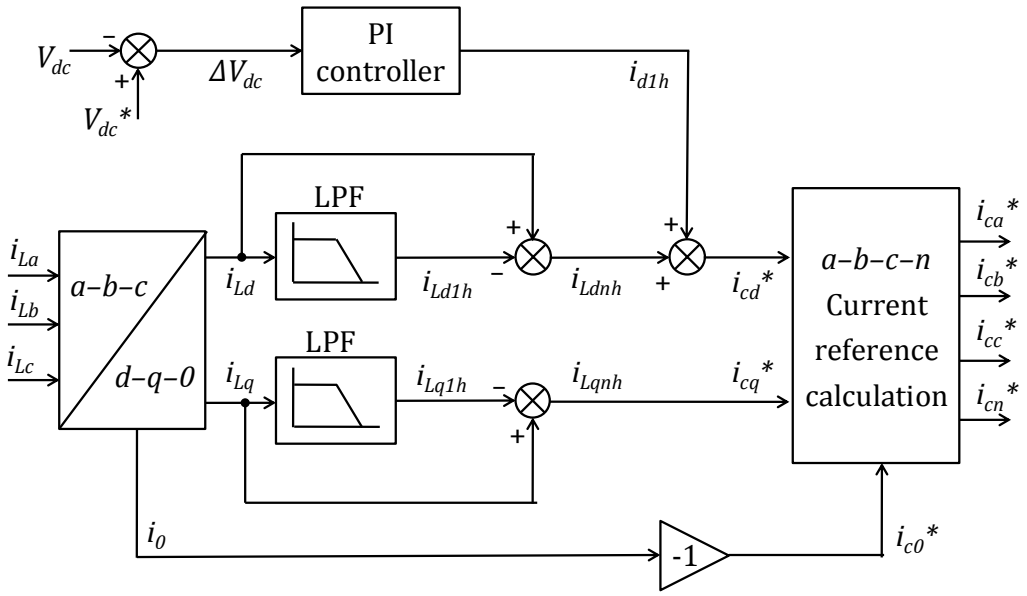


Figure 2.9: Control block diagram for $i_d - i_q$ scheme

2.4. Regulation of Inverter DC-link Voltage

During steady state, real power supplied by the source is equal to the real power demand of the loads plus a small power to compensate the losses occurring inside APF. Thus, the DC-link voltage can be maintained at a constant reference value. However, during load variation the real power balance between the mains and the load is disturbed. This real power difference is compensated by the charging/discharging of DC-link capacitor. If the DC-link capacitor voltage is recovered and it attains the reference voltage; real power supplied by the source again becomes equal to that consumed by the load.

Hence, the role of DC-side capacitor is to serve two major purposes:

a) Maintain a constant DC voltage with small ripples in the steady state
b) Serve as an energy storage element to supply real power difference between load and source during the transient period

The DC bus capacitor can be designed by taking into account the rated filter current $(I_{c,rated})$ and peak-to-peak voltage ripple in V_{dc} $(V_{dc,\max\ \_\text{rip}\ (p-p)})$ as per (2.28) [49].

$$C_{dc} = \frac{\pi \times I_{c,rated}}{\sqrt{3}\omega \times V_{dc,\max\ \_\text{rip}\ (p-p)}} \tag{2.28}$$

The DC bus voltage must be higher than the peak value of utility voltage to force the output current of APF under the command of compensating current. As per [49], by opting for a lesser V_{dc} value, the APF performance degrades; whereas a higher voltage offers lesser THD and V_{dc} settling time. High DC bus voltage has disadvantages like more voltage stress on switches, large filter inductance, and high voltage rating of DC capacitor and power electronic devices. Consequently, larger filter inductor will result in significant power loss, more heat dissipation, bulk dimension and weight, and degraded performance of frequency response. The requirement of high voltage rating of DC capacitor and power electronic devices limits high power application of APFs due to the high power rating and cost of the power converter.

The DC-link capacitor acting as an energy source maintains energy balance inside the VSI. The component of supply reference current (i_{d1h}) and/or average power ($\overline{P_{loss}}$) to restore the energy on DC bus is computed based on energy balance. The nominal stored energy ($e_{dc}{}^{*}$) on the DC bus of APF is given by,

$$e_{dc}{}^{*} = C_{dc}\frac{(V_{dc}{}^{*})^2}{2} \tag{2.29}$$

But, the actual average stored energy on DC bus is given by (2.30), where V_{dca} is the average value of actual DC-link voltage.

$$e_{dc} = C_{dc}\frac{(V_{dca})^2}{2} \tag{2.30}$$

Thus, the energy loss of DC-link capacitor is

$$\Delta e_{dc} = e_{dc}{}^{*} - e_{dc} = C_{dc}\left\{\frac{(V_{dc}{}^{*})^2 - (V_{dca})^2}{2}\right\} \tag{2.31}$$

This energy difference encountered in APF is supplied by AC mains with the help of DC-link voltage regulator.

2.5. Design of Conventional PI Controller

The conventional PI controller is designed using a linear model [49], [50]. Linear model of the PWM converter along with DC-link voltage regulator can be derived by applying

small-signal perturbation technique. A small perturbation (ΔI_c) is applied in the input filter current (I_c) of converter, about a steady state operating point (I_{c0}). The average DC-link voltage also gets perturbed by a small amount (ΔV_{dc}) about its steady state operating point V_{dc0} (same as $V_{dc}{}^*$). Let L_c and R_c are the filter inductance and resistance, and V_c is AC-side voltage of VSI. The characteristics equation is as follows:

$$1 + \left(K_p + \frac{K_i}{s}\right)\left(\frac{3[V_c - L_c I_{c0} s - 2I_{c0} R_c]}{C_{dc} V_{dc0} s}\right) = 0 \tag{2.32}$$

2.6. Results and Discussion

Extensive investigations are carried out by performing simulations and using RT-Lab, in order to find out the effectiveness of the three discussed APF control schemes. System configuration of shunt APF along with three-phase and single-phase nonlinear diode rectifier loads is depicted in Figure 2.10.

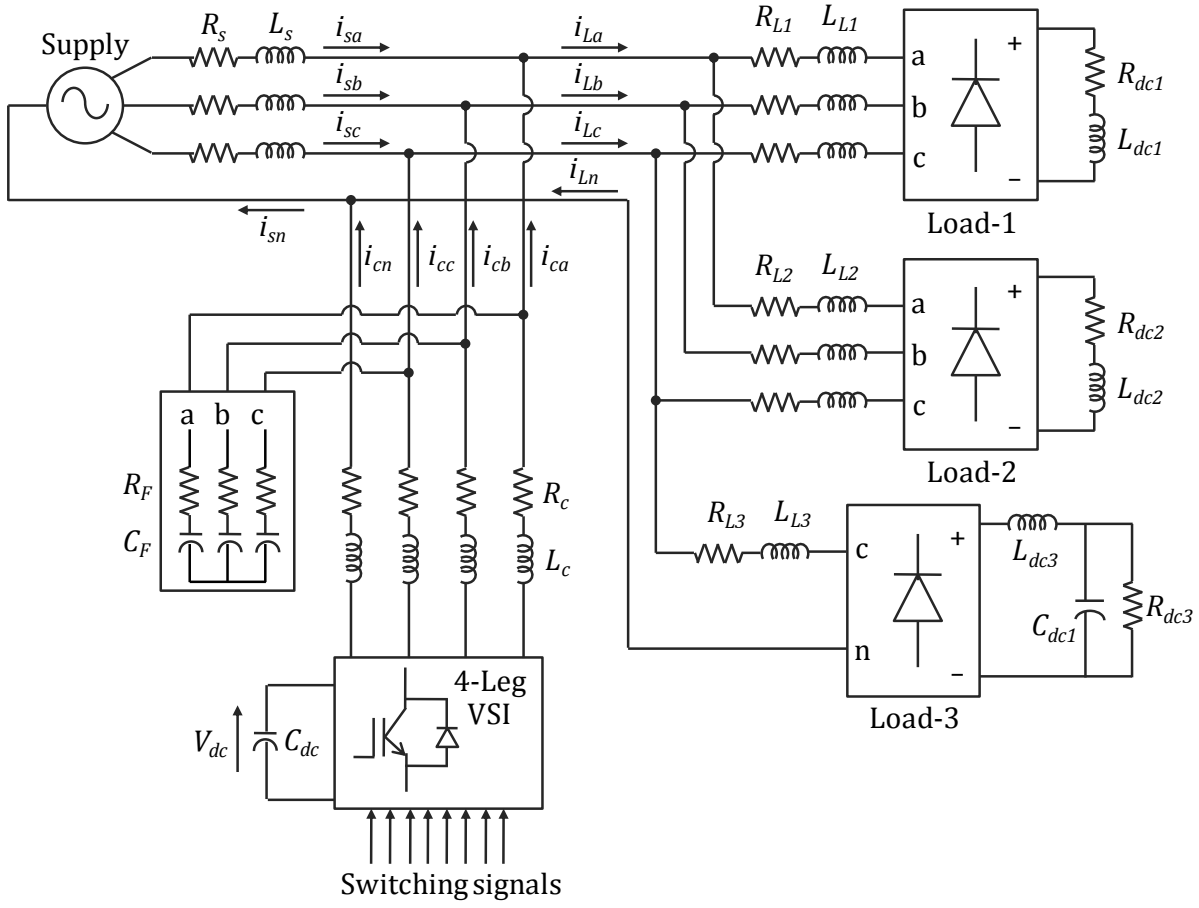


Figure 2.10: Three-phase four-wire APF system configuration with nonlinear loads

The values of system parameters used for simulation are indicated in Table 2.1. Values of filter inductor (L_c), DC-side capacitor (C_{dc}) and reference value of DC-side capacitor voltage ($V_{dc}{}^*$) have been found out as per Reference [49]. Demonstration is done under three different conditions of supply voltage. For ideal supply, completely balanced and sinusoidal voltage of 230 V RMS is considered. Distorted supply condition is created by incorporating 3rd harmonic component into the supply voltage. During unbalanced supply, voltage in one of the phases is 200 V RMS, while in the other two it is 230 V RMS, voltages in all the phases being sinusoidal.

Table 2.1: Values of system parameters used in simulation

Parameter	Notation	Value
Supply frequency	f	50 Hz
Source impedance	(R_s, L_s)	(10 mΩ, 50 μH)
Load-1 parameters	(R_{L1}, L_{L1}), (R_{dc1}, L_{dc1})	(0.1 Ω, 3 mH), (25 Ω, 25 mH)
Load-2 parameters	(R_{L2}, L_{L2}), (R_{dc2}, L_{dc2})	(0.1 Ω, 3 mH), (25 Ω, 60 mH)
Load-3 parameters	(R_{L3}, L_{L3}), $(R_{dc3}, L_{dc3}, C_{dc1})$	(1.5 Ω, 15 mH), (25 Ω, 50 mH, 540 μF)
DC-link capacitance	C_{dc}	3 mF
Reference DC-link voltage	$V_{dc}{}^*$	800 V
AC-side filter parameters	(R_c, L_c), (R_F, C_F)	(0.1 Ω, 1 mH), (0.5 Ω, 25 μF)

PI controller gains are suitably decided by considering the overshoot and settling time in transient response for a step change in DC voltage reference, as explained in Section 2.5 [50]. Adapting a compromise between overshoot and settling time, the values of K_p and K_i are chosen from the Tables 2.2 – 2.4.

The best values of gains K_p and K_i are found out to be:

a) 0.91 and 42 for $p - q$ scheme

b) 0.46 and 4.95 for modified $p - q$ scheme

c) 0.78 and 28 for $i_d - i_q$ schemes

Table 2.2: Overshoots and settling times for different K_p and K_i with $p-q$ scheme

Sl. No.	K_p	K_i	Maximum overshoot (Volts)	Settling time (sec)
1	0.2	15.5	36.6	0.084
2	0.43	10	60.6	0.060
3	0.55	12.7	43.8	0.077
4	0.76	25	38.1	0.071
5	**0.91**	**42**	**39.5**	**0.065**

Table 2.3: Overshoots and settling times for different K_p and K_i with modified p-q scheme

Sl. No.	K_p	K_i	Maximum overshoot (Volts)	Settling time (sec)
1	0.2	15	36.4	0.079
2	**0.46**	**4.95**	**39.2**	**0.064**
3	0.6	12.5	38.3	0.075
4	0.75	25	56.7	0.062
5	0.9	12	49.1	0.077

Table 2.4: Overshoots and settling times for different K_p and K_i with $i_d - i_q$ scheme

Sl. No.	K_p	K_i	Maximum overshoot (Volts)	Settling time (sec)
1	0.23	19.5	36.5	0.079
2	0.4	22	56.3	0.070
3	0.62	17.5	43.7	0.055
4	**0.78**	**28**	**37.1**	**0.057**
5	0.85	19	36.8	0.075

2.6.1. Simulation results

Initially, only Load-1 is put into operation until $t = 0.1\,s$, to evaluate the harmonic compensation capability. Performance under dynamic conditions is observed by sudden switching on of Load-2 and 3 at $t = 0.1\,s$ for compensation of current harmonics, neutral current and unbalanced source current resulted due to the single-phase load (Load-3).

1) Ideal supply

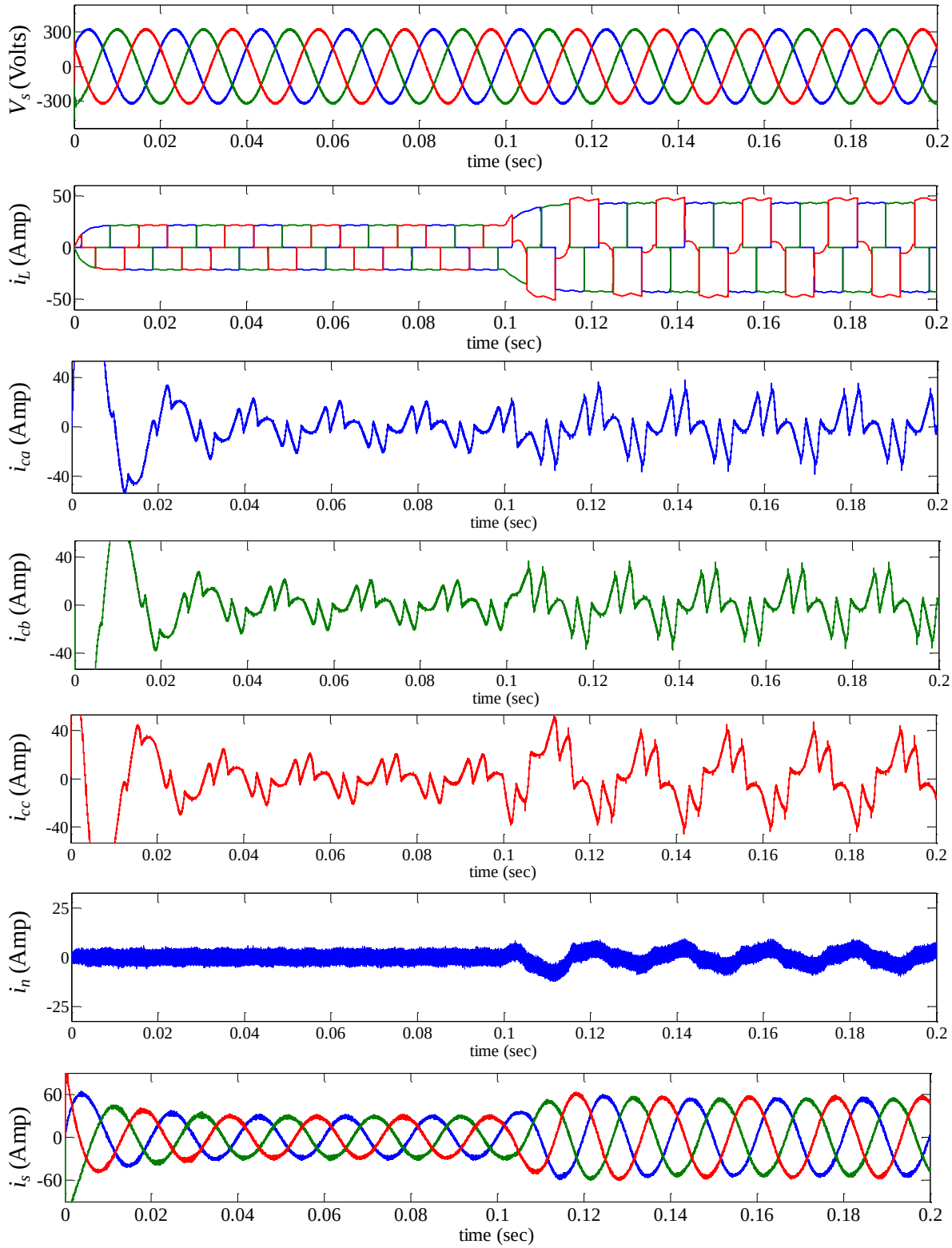


Figure 2.11: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing $p-q$ control scheme under ideal supply condition

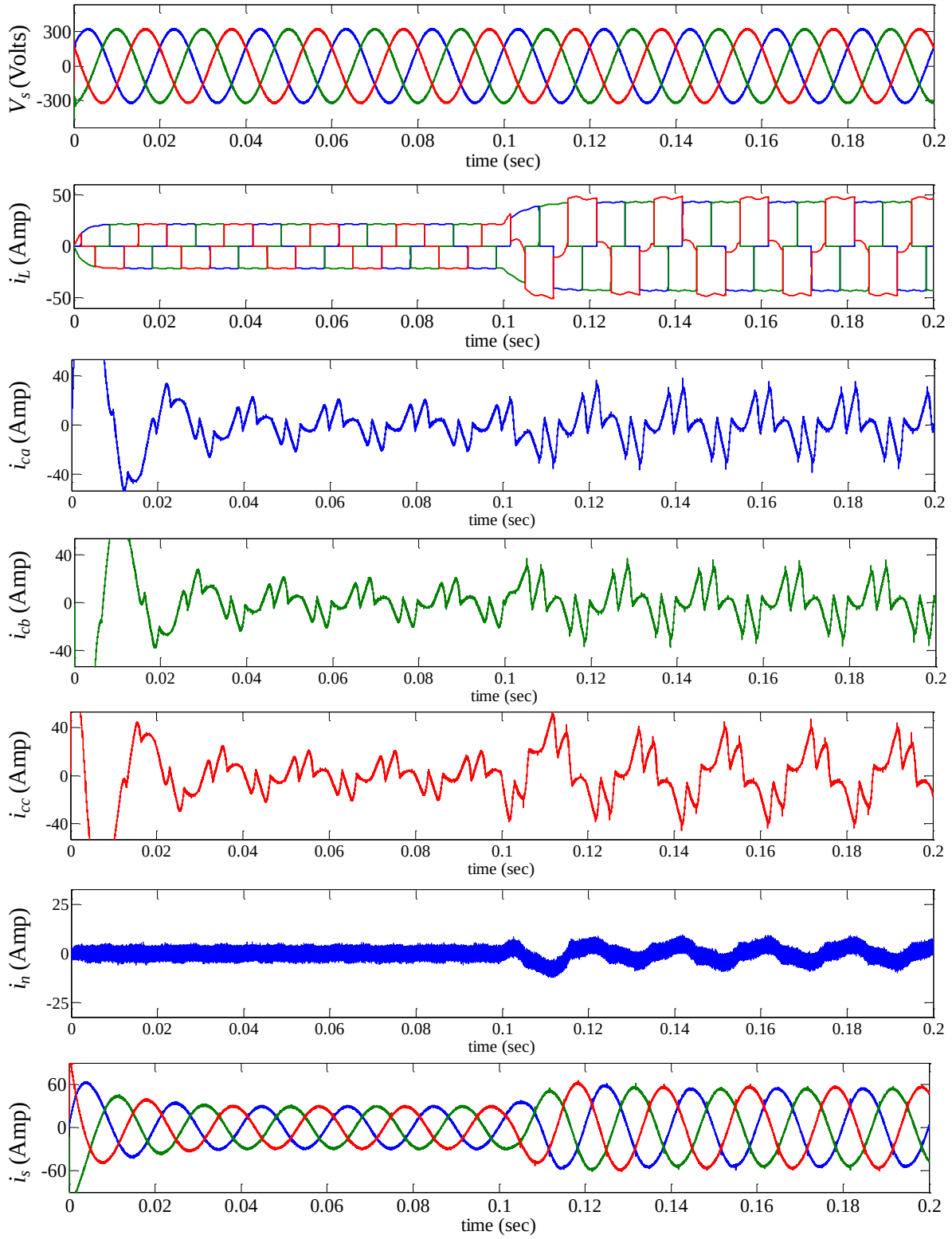


Figure 2.12: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing modified $p-q$ control scheme under ideal supply condition

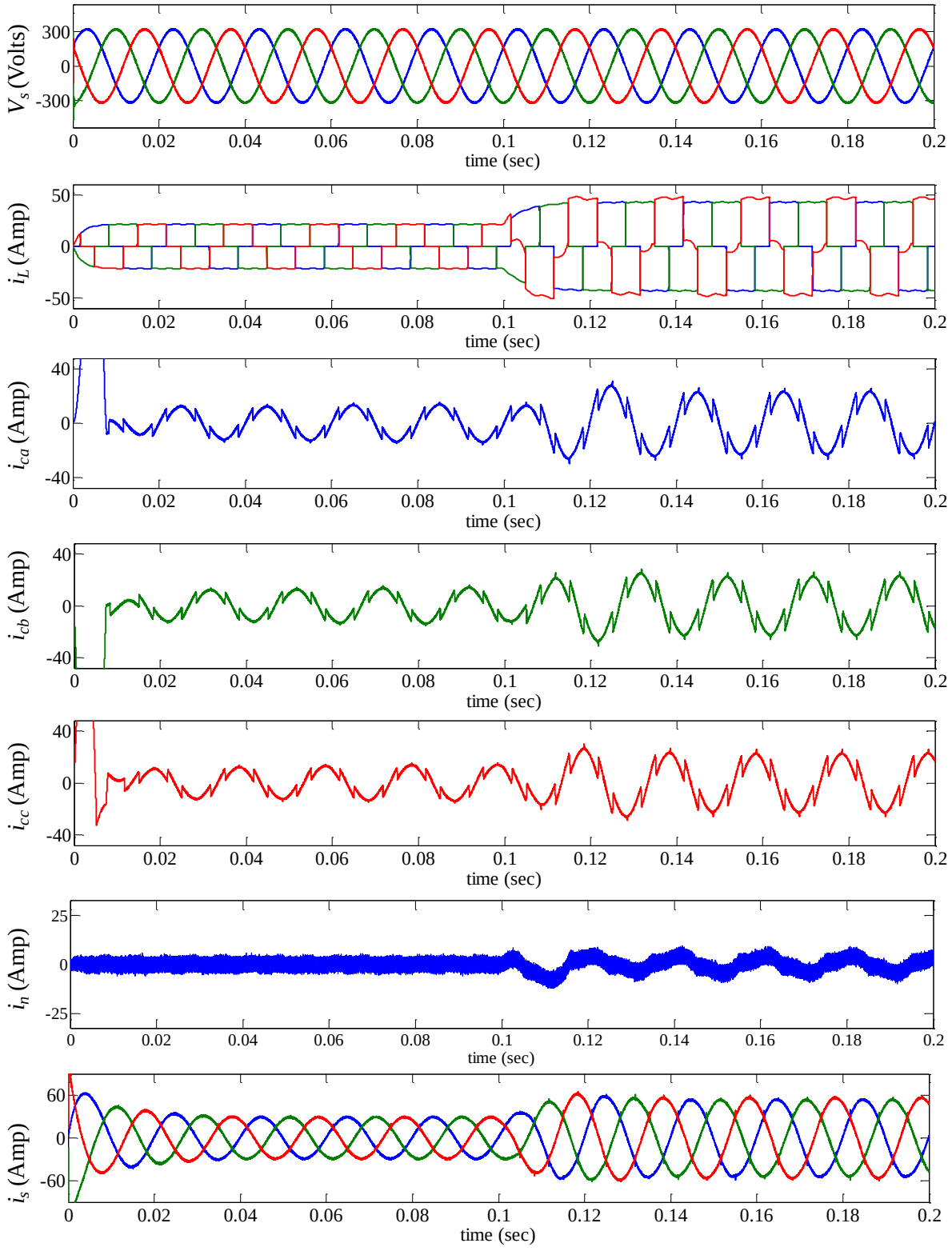


Figure 2.13: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing $i_d - i_q$ control scheme under ideal supply condition

2) Distorted supply

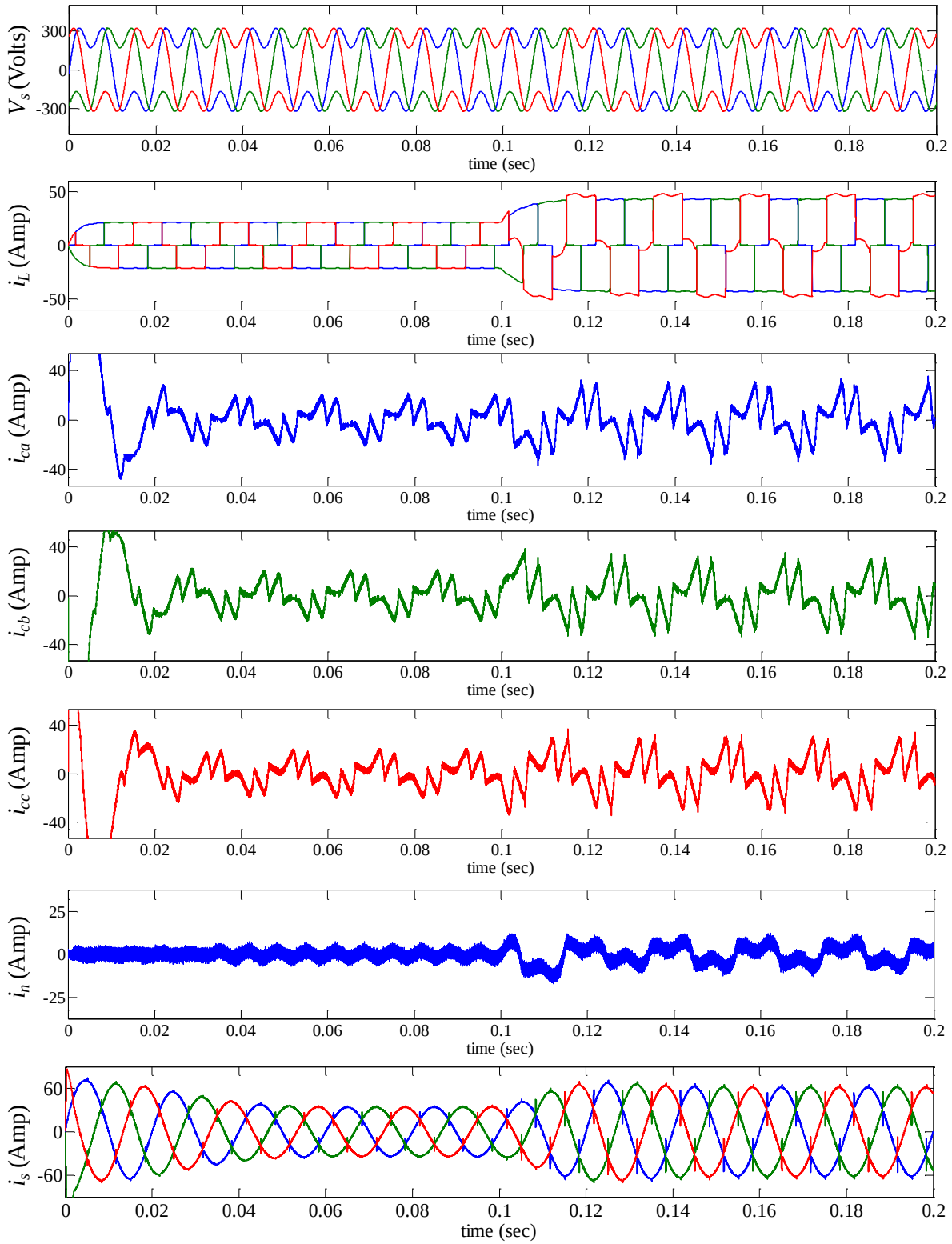


Figure 2.14: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing $p-q$ control scheme under distorted supply condition

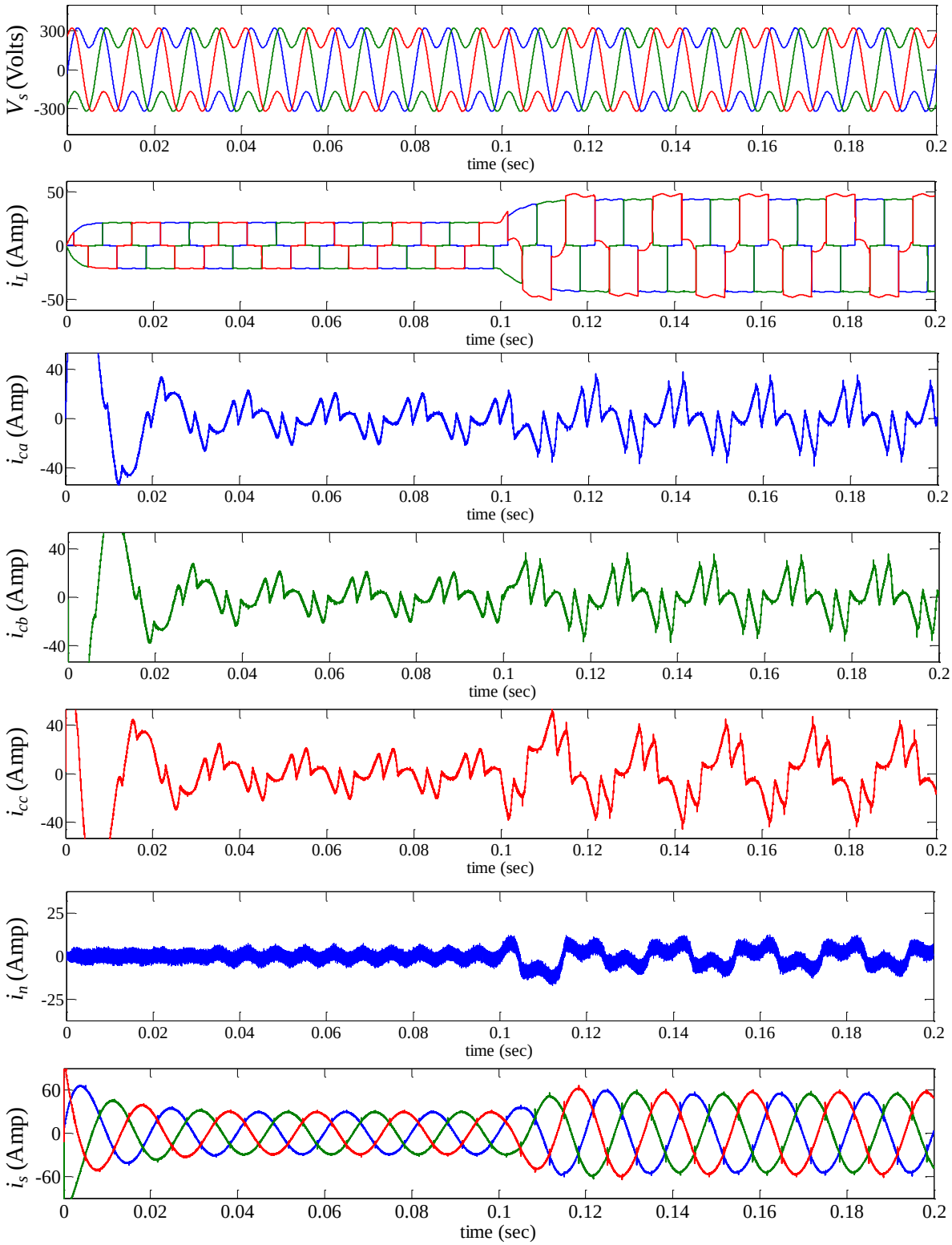


Figure 2.15: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing modified $p-q$ control scheme under distorted supply condition

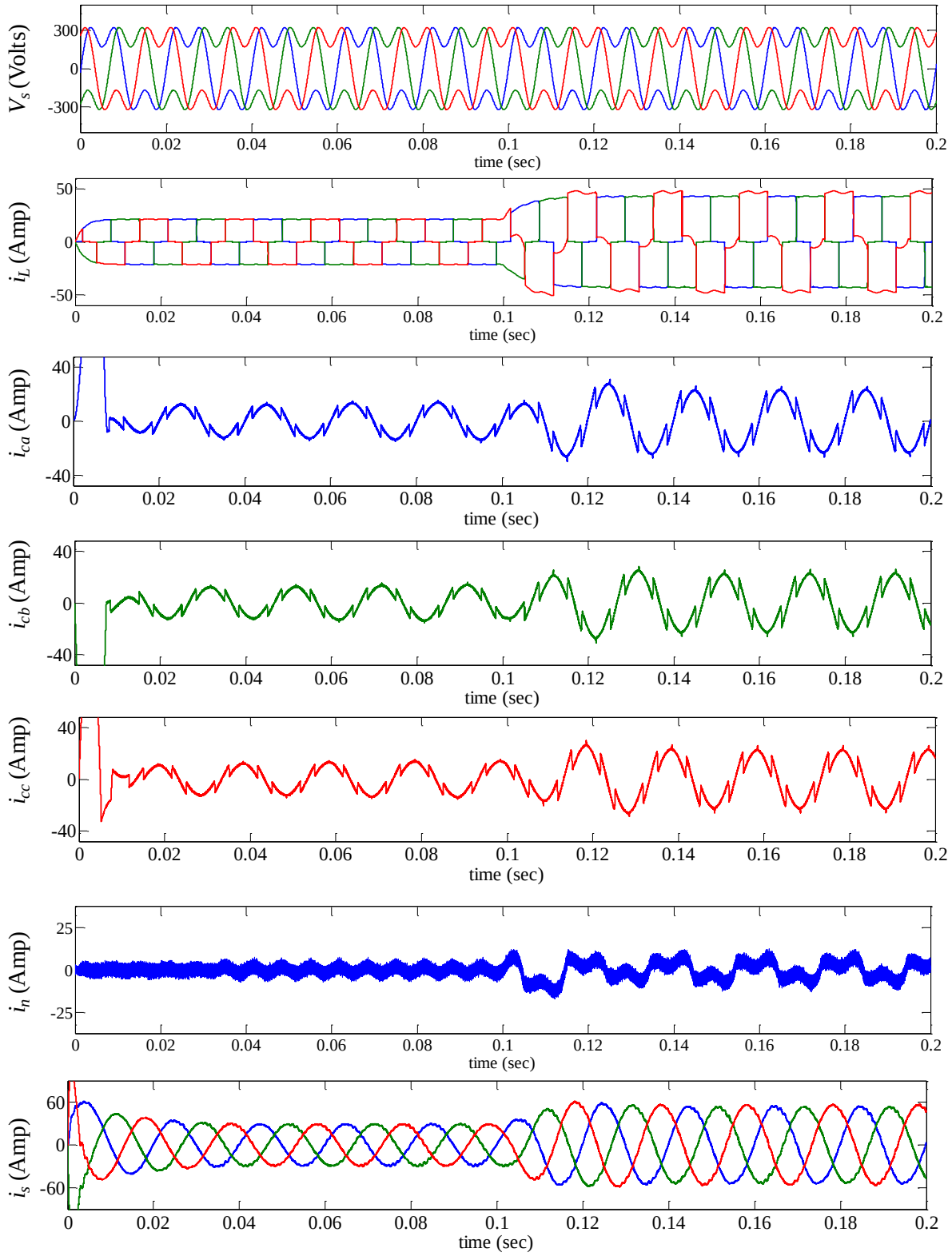


Figure 2.16: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing $i_d - i_q$ control scheme under distorted supply condition

3) Unbalanced supply:

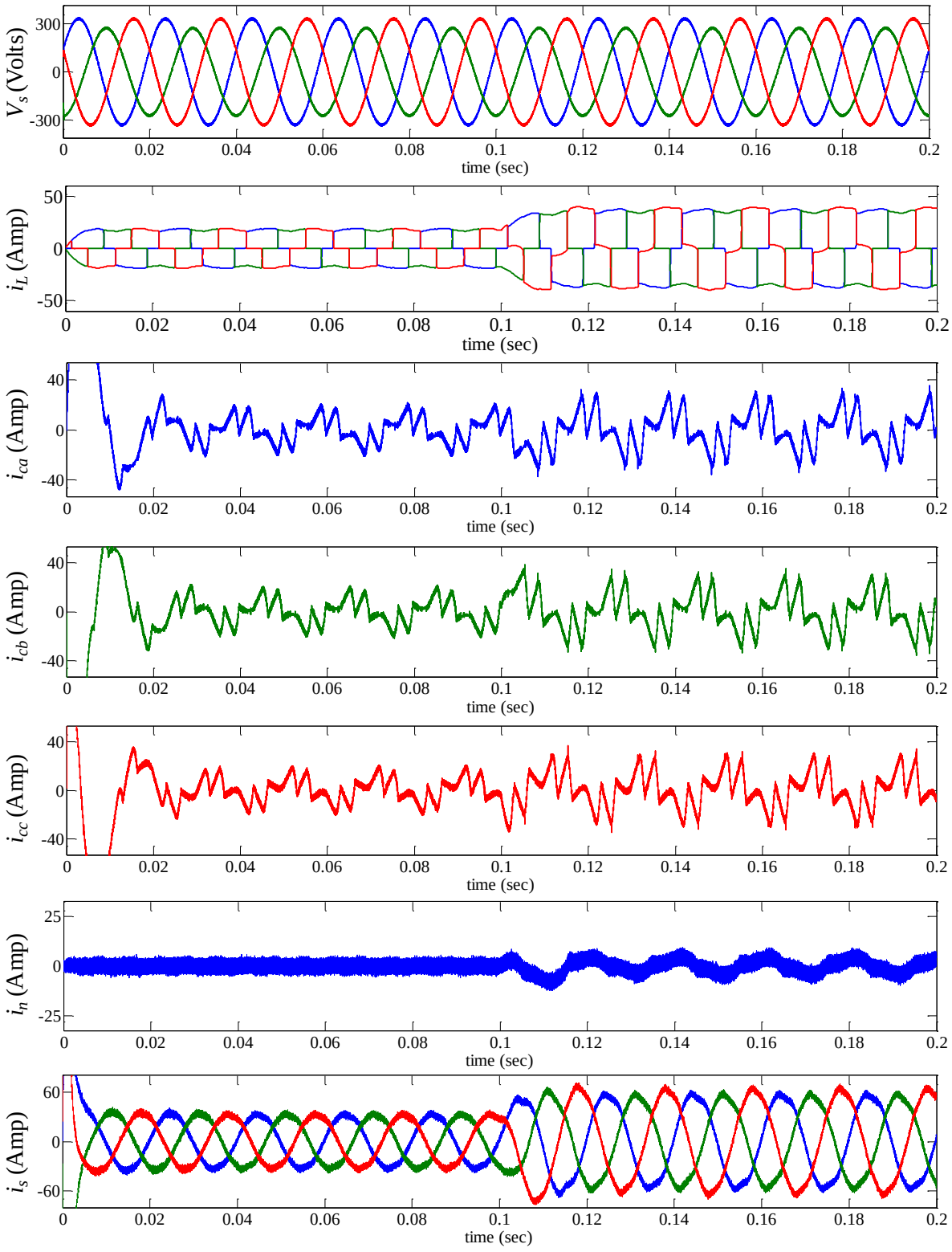


Figure 2.17: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing $p-q$ control scheme under unbalanced supply condition

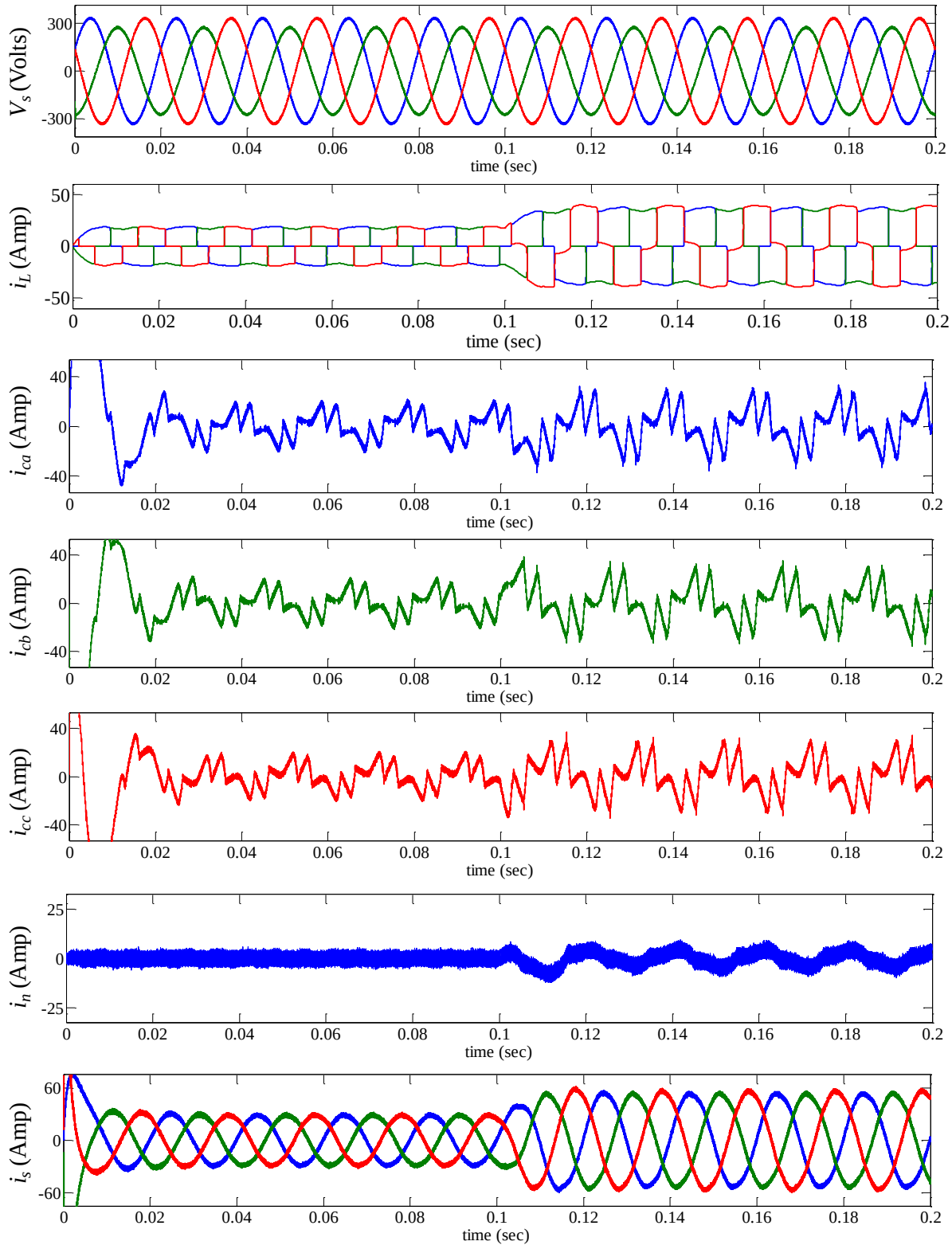


Figure 2.18: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing modified $p-q$ control scheme under unbalanced supply condition

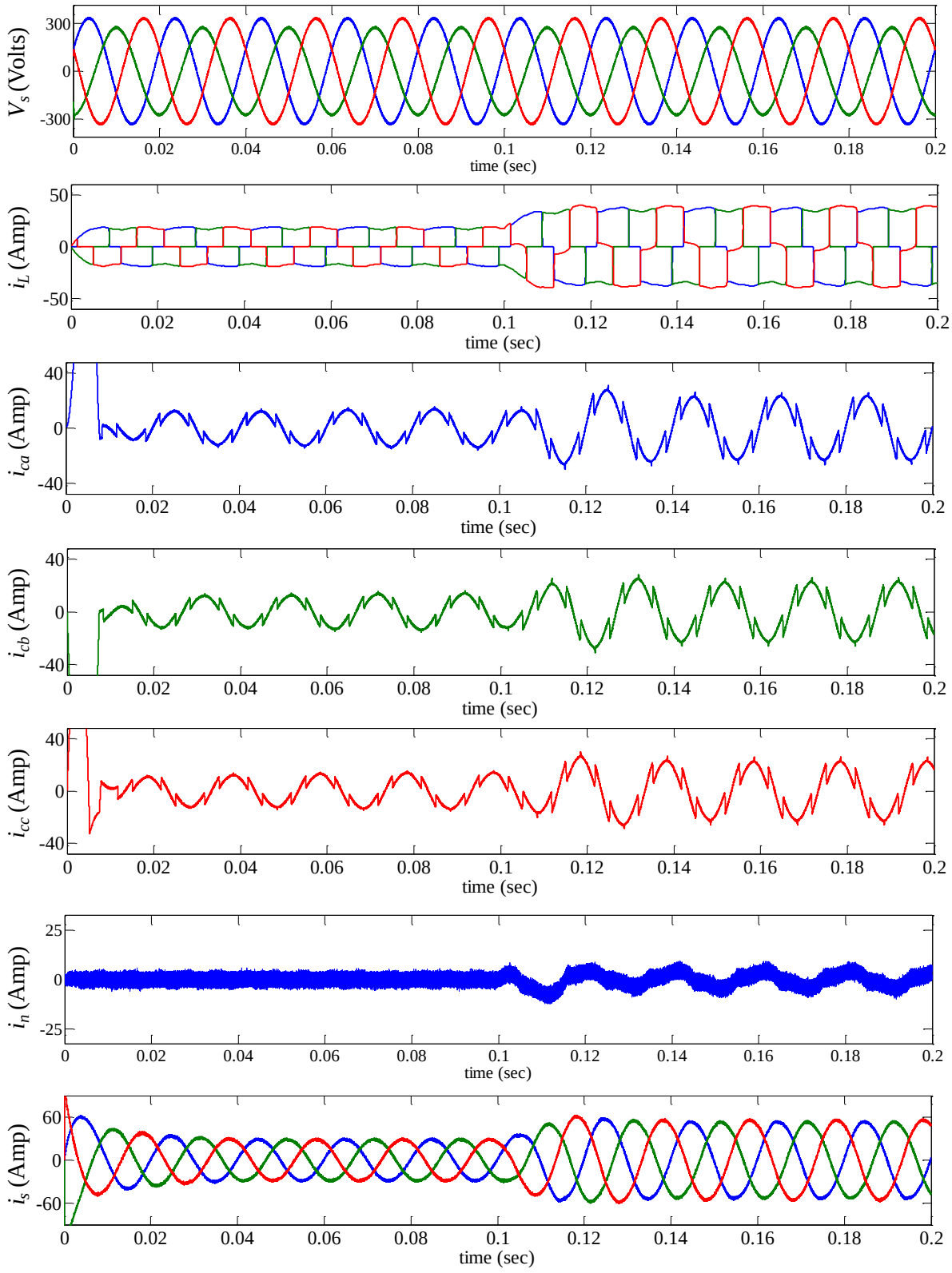


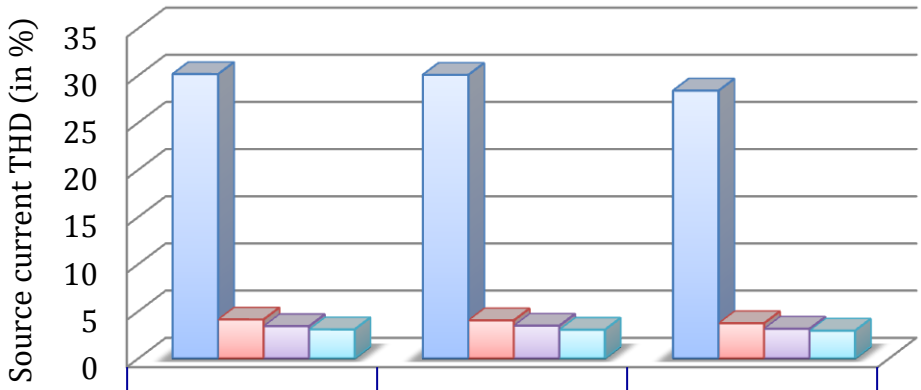
Figure 2.19: Supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms for APF employing $i_d - i_q$ control scheme under unbalanced supply condition

Simulation results for APF employing $p-q$, modified $p-q$ and i_d-i_q control schemes under ideal supply voltage condition are shown in Figures 2.11, 2.12 and 2.13 respectively. The supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms are presented in top to bottom order. The nature of source current before compensation is exactly same as the load current. Neutral current, that is the current flowing in neutral conductor comes into significance only during the time unbalance in load current exists, that is from $t = 0.1\ s$ to $t = 0.2\ s$. The current harmonics, neutral current and unbalance have been successfully cancelled with all the three control methods.

Simulation results for APF employing $p-q$, modified $p-q$ and i_d-i_q control schemes under distorted supply voltage condition are shown in Figures 2.14, 2.15 and 2.16 respectively. It depicts the supply voltage (V_s), load current (i_L), compensation currents in phases a, b and c (i_{ca}, i_{cb}, i_{cc}), neutral current (i_n) and source current (i_s) waveforms in top to bottom order. Current harmonics, neutral current and unbalance in source current have been compensated employing all the discussed control schemes.

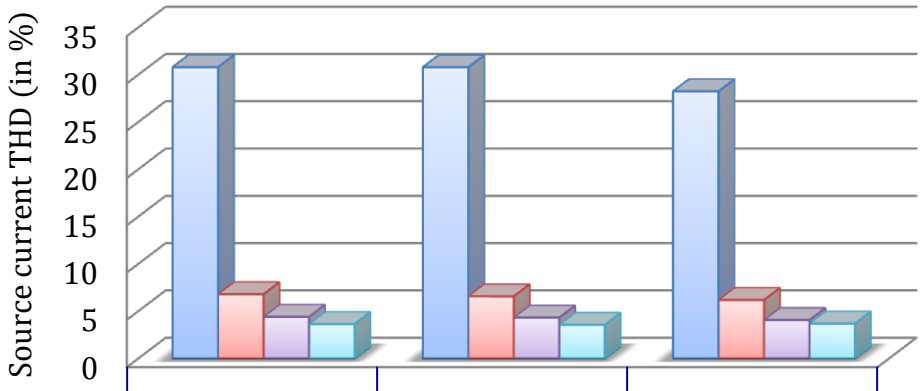
This is followed by simulation results for APF employing the three control schemes under unbalanced supply condition, given in Figures 2.17, 2.18 and 2.19. Even under highly unbalanced supply, current harmonics and neutral current are lowered down to small values with all the three control schemes. In addition, unbalance in source current has also been minimized to some extent employing $p-q$ and modified $p-q$ schemes, and to a large extent employing i_d-i_q scheme.

FFT analysis is performed in order to figure out the overall THD in the three phases of source current under all the three supply conditions, before and after compensation with the three control schemes. The source current THDs without and with APF employing $p-q$, modified $p-q$ and i_d-i_q control schemes under ideal, distorted and unbalanced supply conditions are clearly presented in Figures 2.20, 2.21 and 2.22 respectively. The chart diagrams show a comparison of these source current THD values.



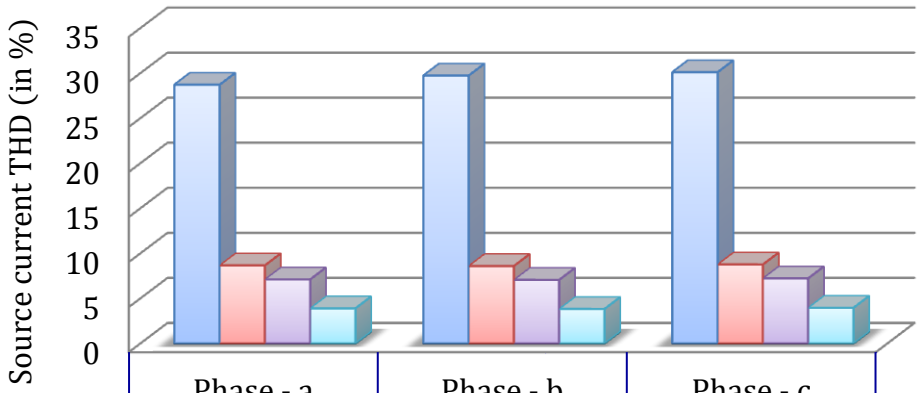
	Phase - a	Phase - b	Phase - c
Without APF	30.13	30.05	28.38
p-q scheme	4.12	4.03	3.72
Modified p-q scheme	3.41	3.46	3.14
Id-Iq scheme	3.07	3.03	2.94

Figure 2.20: Chart diagram showing source current THDs (in %) before and after compensation with $p-q$, modified $p-q$ and i_d-i_q control schemes for simulations under ideal supply condition



	Phase - a	Phase - b	Phase - c
Without APF	30.78	30.77	28.23
p-q scheme	6.78	6.56	6.17
Modified p-q scheme	4.39	4.31	4.05
Id-Iq scheme	3.62	3.54	3.68

Figure 2.21: Chart diagram showing source current THDs (in %) before and after compensation with $p-q$, modified $p-q$ and i_d-i_q control schemes for simulations under distorted supply condition



	Phase - a	Phase - b	Phase - c
Without APF	28.71	29.72	30.1
p-q scheme	8.66	8.59	8.76
Modified p-q scheme	7.1	7.05	7.22
Id-Iq scheme	3.89	3.82	3.95

Figure 2.22: Chart diagram showing source current THDs (in %) before and after compensation with $p-q$, modified $p-q$ and i_d-i_q control schemes for simulations under unbalanced supply condition

It is clearly observed from the simulation results obtained under ideal supply that, the THD in source current has been lowered down to nearly 3% with $p-q$ and modified $p-q$ schemes from the uncompensated source current THD of nearly 30%. However, i_d-i_q scheme is found to be more proficient, as it lowers down the source current THD to nearly 3% even during large change in load and unbalanced loading conditions. Hence, all the control schemes are found to be successful in lowering down the THDs in source current well below 5%. Under highly distorted supply, though modified $p-q$ scheme works comparatively better than $p-q$ scheme, i_d-i_q scheme outperforms the other two schemes by lowering down the source current THDs in three phases to 3.62%, 3.54% and 3.68% even under sudden load change and unbalanced loading conditions. Results obtained under unbalanced supply indicate that, $p-q$ and modified $p-q$ schemes are not efficient enough in lowering down the source current THD below 5%, whereas i_d-i_q scheme lowers down the overall THDs to 3.89%, 3.82% and 3.95% in three phases of source current.

2.6.2. RT-Lab results

Investigations with the help of RT-Lab are carried out in order to compare the efficiencies of $p-q$, modified $p-q$ and i_d-i_q control schemes under three different supply voltages. The same APF configurations of Figure 2.10 and system parameter values of Table 2.1 have been considered with all the three nonlinear loads operating at the same time. The RT-Lab results observed with the help of a DSO are presented here, with the scales along voltage/current and time axes indicated below the figures. The natures of source currents obtained with the three APF control schemes are evaluated to compare the harmonic contents in them.

1) Ideal supply: The ideal supply voltage (V_s) simulation waveform is shown below in Figure 2.23 (a). Load currents in three phases (i_{La}, i_{Lb}, i_{Lc}) are presented in Figure 2.23 (b). Compensation currents in the four wires ($i_{ca}, i_{cb}, i_{cc}, i_{cn}$) for $p-q$, modified $p-q$ and i_d-i_q schemes are depicted in Figures 2.23 (c), (e) and (g) respectively. Similarly, Figures 2.23 (d), (f) and (h) illustrate the source currents in three phases (i_{sa}, i_{sb}, i_{sc}) for $p-q$, modified $p-q$ and i_d-i_q schemes.

2) Distorted supply: Various real-time RT-Lab results such as, source voltage (V_s), load currents (i_{La}, i_{Lb}, i_{Lc}), compensation currents in four wires ($i_{ca}, i_{cb}, i_{cc}, i_{cn}$) and source currents ($i_{sa}, i_{sb}, i_{sc}$) with APFs employing $p-q$, modified $p-q$ and i_d-i_q control schemes under distorted supply are shown in Figure 2.24. The nature of supply voltage in RT-Lab is same as that considered in simulations and is shown in Figure 2.24 (a). Nature of current drawn by the same loads under distorted supply is different than that drawn under ideal supply, as seen in Figure 2.24 (b).

3) Unbalanced supply: The analysis in RT-Lab for unbalanced supply condition is performed by taking the same nature of source voltage as in simulation studies, presented in Figure 2.25 (a), followed by load current in Figure 2.25 (b). The compensation filter currents and source currents for $p-q$, modified $p-q$ and i_d-i_q control schemes are given in Figures 2.25 (c) to (h).

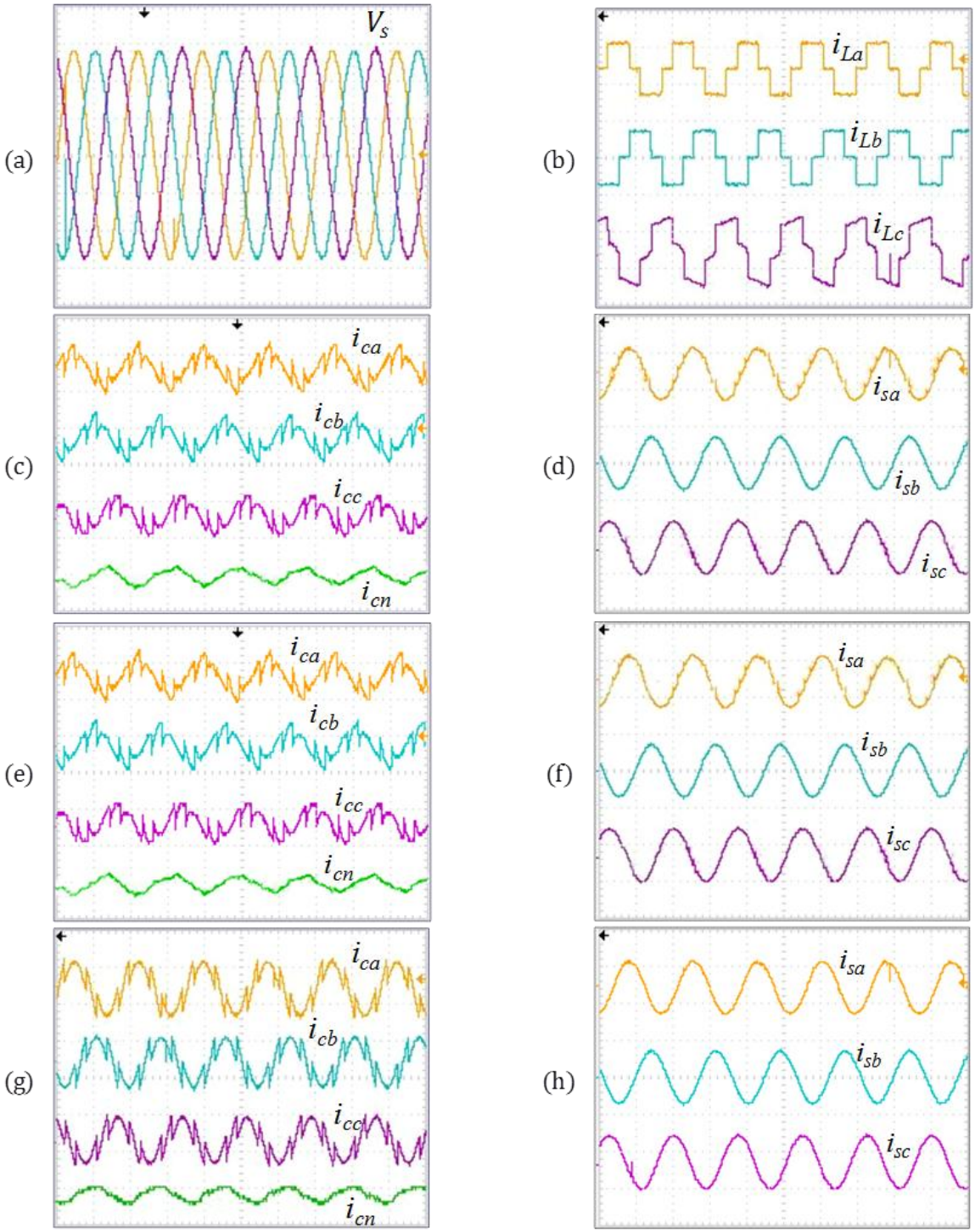


Figure 2.23: RT-Lab results under ideal supply for **(a)** Supply voltage [scale: 60 V/div], **(b)** Load current [scale: 20 A/div], **(c)** Filter current for $p-q$ scheme [scale: 10 A/div], **(d)** Source current for $p-q$ scheme [scale: 40 A/div], **(e)** Filter current for modified $p-q$ scheme [scale: 10 A/div], **(f)** Source current for modified $p-q$ scheme [scale: 40 A/div], **(g)** Filter current for i_d-i_q scheme [scale: 10 A/div], **(h)** Source current for i_d-i_q scheme [scale: 40 A/div]; Time scale: 10 ms/div

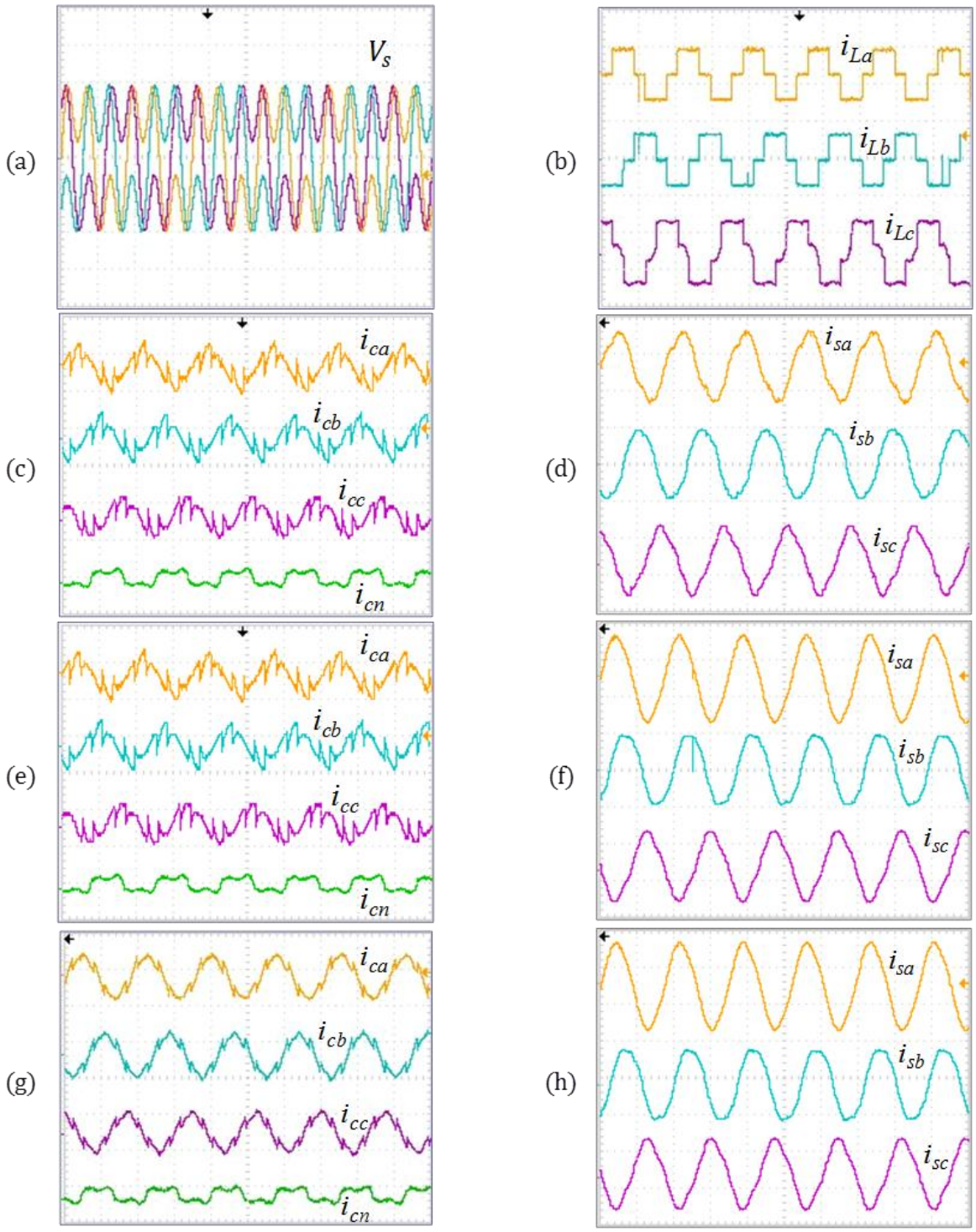


Figure 2.24: RT-Lab results under distorted supply for **(a)** Supply voltage [scale: 100 V/div], **(b)** Load current [scale: 20 A/div], **(c)** Filter current for $p-q$ scheme [scale: 10 A/div], **(d)** Source current for $p-q$ scheme [scale: 30 A/div], **(e)** Filter current for modified $p-q$ scheme [scale: 10 A/div], **(f)** Source current for modified $p-q$ scheme [scale: 30 A/div], **(g)** Filter current for i_d-i_q scheme [scale: 10 A/div], **(h)** Source current for i_d-i_q scheme [scale: 30 A/div]; Time scale: 10 ms/div

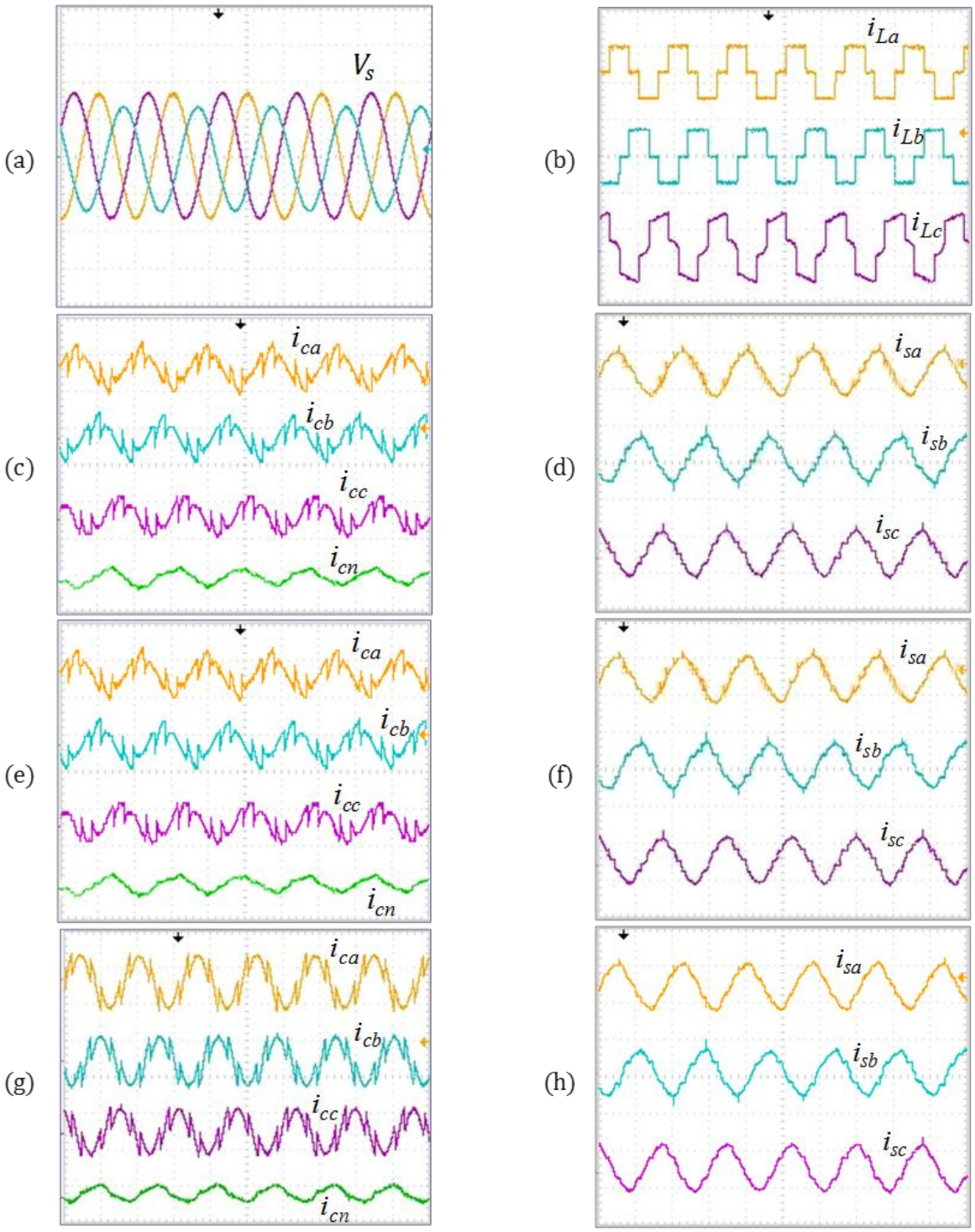
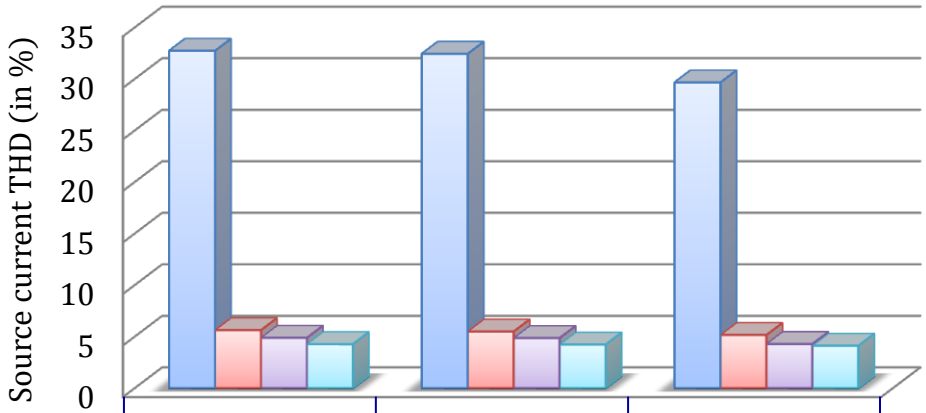


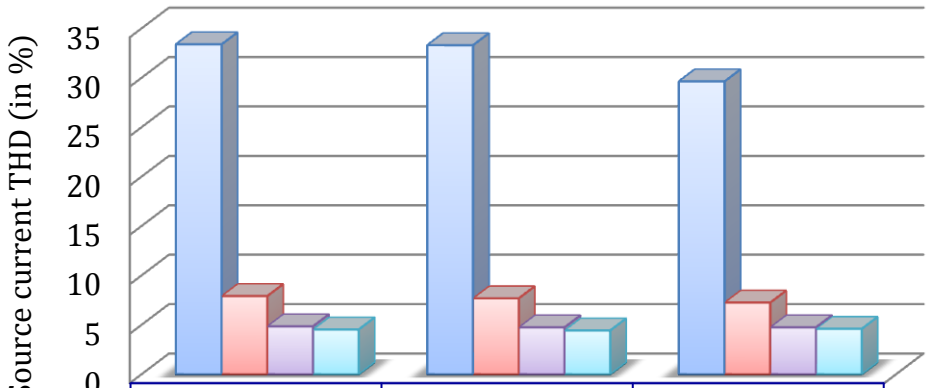
Figure 2.25: RT-Lab results under unbalanced supply for **(a)** Supply voltage [scale: 100 V/div], **(b)** Load current [scale: 20 A/div], **(c)** Filter current for $p-q$ scheme [scale: 10 A/div], **(d)** Source current for $p-q$ scheme [scale: 40 A/div], **(e)** Filter current for modified $p-q$ scheme [scale: 10 A/div], **(f)** Source current for modified $p-q$ scheme [scale: 40 A/div], **(g)** Filter current for i_d-i_q scheme [scale: 10 A/div], **(h)** Source current for i_d-i_q scheme [scale: 40 A/div]; Time scale: 10 ms/div

It is clearly observed from the RT-Lab results that, the load currents, compensation filter currents and source currents after compensation with $p-q$, modified $p-q$ and i_d-i_q schemes exactly follow the simulation results under ideal, distorted and unbalanced supplies. The source current THDs without and with APF employing $p-q$, modified $p-q$ and i_d-i_q control schemes under ideal, distorted and unbalanced supply conditions are clearly presented in Figures 2.26, 2.27 and 2.28 respectively. The chart diagrams show a comparison of these source current THD values. When compared, THDs of source currents obtained with RT-Lab exhibit slightly higher values than respective current THDs obtained with simulation studies. The THDs of Figures 2.27 reveal that, modified $p-q$ scheme yields less distorted source currents than $p-q$ scheme under distorted supply. However, THDs of source currents after compensation with i_d-i_q scheme are the lowest irrespective of supply condition, thus validating the results obtained with simulations.



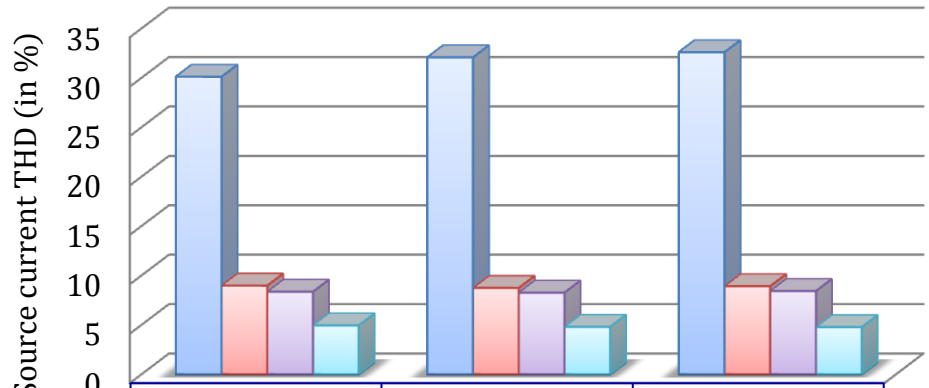
	Phase - a	Phase - b	Phase - c
Without APF	32.74	32.45	29.67
p-q scheme	5.63	5.5	5.16
Modified p-q scheme	4.89	4.87	4.29
Id-Iq scheme	4.27	4.23	4.12

Figure 2.26: Chart diagram showing source current THDs (in %) obtained with RT-Lab before and after compensation with $p-q$, modified $p-q$ and i_d-i_q control schemes under ideal supply condition



	Phase - a	Phase - b	Phase - c
Without APF	33.38	33.3	29.63
p-q scheme	7.91	7.68	7.25
Modified p-q scheme	4.85	4.74	4.75
Id-Iq scheme	4.53	4.43	4.59

Figure 2.27: Chart diagram showing source current THDs (in %) obtained with RT-Lab before and after compensation with $p-q$, modified $p-q$ and $i_d - i_q$ control schemes under distorted supply condition



	Phase - a	Phase - b	Phase - c
Without APF	30.11	32.07	32.59
p-q scheme	8.97	8.73	8.91
Modified p-q scheme	8.35	8.26	8.42
Id-Iq scheme	4.94	4.8	4.76

Figure 2.28: Chart diagram showing source current THDs (in %) obtained with RT-Lab before and after compensation with $p-q$, modified $p-q$ and $i_d - i_q$ control schemes under unbalanced supply condition

2.7. Summary

The chapter commences with the depiction of basic compensation principle and general description of shunt APF. Next section illustrates the generation of switching signals for the IGBTs inside VSI with the help of Hysteresis PWM, and the extraction of reference compensation currents using $p-q$, modified $p-q$ and i_d-i_q schemes. The significance of DC-link voltage of VSI for reliable performance by APF is also described. The DC-link voltage regulator uses a PI controller to overcome the deviation in DC-link voltage from its reference value, thereby minimizing the undesirable real power loss occurring inside APF. The gains of PI controller are extracted using small-signal perturbation technique. Next section analyzes the harmonic compensation capabilities of three APF control schemes under ideal, distorted and unbalanced supplies along with sudden load change and asymmetrical loading conditions. Extensive results obtained using simulation studies and RT-Lab are presented. Finally, the THDs of source currents obtained with all the control schemes are compared and it shows that, IEEE-519 standard is met with

a) All the control schemes under ideal supply
b) Modified $p-q$ and i_d-i_q schemes under distorted supply
c) Only i_d-i_q control scheme under unbalanced supply

Moreover, the generation of reference compensation currents in i_d-i_q scheme does not require a PLL, as the synchronous rotating frame itself is derived from the mains voltages. In the contrary, most of the APF control schemes including the $p-q$ and modified $p-q$ schemes need a PLL for successful operation. This makes the i_d-i_q scheme capable of avoiding many synchronization problems.

Chapter 3

Optimizing APF Performance Using PSO and BFO, and Development of an Enhanced BFO Technique

3.1. Introduction

For consistent performance of APF, the DC-link capacitor voltage needs to be maintained constant, as discussed earlier. This is achieved via a conventionally tuned PI controller in Chapter 2. However, in conventional linearization-based approaches, recommended settings are empirical in nature and obtained from extensive experimentation. Besides, power system network represents a highly complex, nonlinear and time-varying system involving large number of inequality constraints. Thus, optimized values of gains K_p and K_i can always be obtained, to satisfy the conditions of both dynamics and stability. This can be accomplished with the help of optimization algorithms. The advantages of optimization based controllers over conventional controllers are:

a) Do not need accurate mathematical modelling
b) Can work with imprecise inputs
c) Can handle nonlinearity
d) More robust than conventional controllers

A simple continuous optimization problem is defined as a pair (S, f) where,

S: Set of all possible solutions: $S = \Re^P$, where P = No. of controllable parameters

f: A single objective function, $f : S \rightarrow \Re$ that needs to be optimized

An optimization problem can either be maximization or minimization problem. In maximization, a solution greater than or equal to all other solutions is searched for. In minimization, a solution smaller than or equal to all other solutions is searched for.

The set of maximal solutions $S_{max} \subseteq S$ of a function $f : S \rightarrow \Re$ is defined as,

$$\vec{x}_{max} \in S_{max} \Leftrightarrow \forall \vec{x} \in S : f(\vec{x}_{max}) \geq f(\vec{x}) \tag{3.1}$$

The set of minimal solutions $S_{min} \subseteq S$ of a function $f : S \rightarrow \Re$ is defined as,

$$\vec{x}_{min} \in S_{min} \Leftrightarrow \forall \vec{x} \in S : f(\vec{x}_{min}) \leq f(\vec{x}) \tag{3.2}$$

Solution vector $\vec{x}$ is often limited between a lower bound and an upper bound, $\vec{x}_{lb} \leq \vec{x} \leq \vec{x}_{ub}$. In this thesis, a minimization problem has been chosen to be solved.

3.1.1. Problem formulation

3.1.1.1. Regulation of inverter DC-link voltage

As explained in Section 2.4, the energy difference encountered in APF is supplied from AC mains by regulating the DC-link voltage using a PI controller. A PI controller offers dual advantages as the Proportional (P) action provides fast response and the Integral (I) action provides zero steady-state error. The output of a PI controller is given by,

$$u(t) = K_p.e(t) + K_i \int_0^t e(t).dt = K_p.[r(t) - c(t)] + K_i \int_0^t [r(t) - c(t)].dt \tag{3.3}$$

Here, t represents the instantaneous time, $e(t)$ is the system error between the desired output $r(t)$ and actual output $c(t)$, $u(t)$ is the controlled input for nonlinear system, K_p is the proportional gain, and K_i is the integral gain. The proportional term considers only the current value of error at any time, whereas the integral term considers the sum of instantaneous errors over time, or how far the actual measured output value has been from the reference since the start time. Here, the error being minimized using PI controller is DC-link voltage error ($\Delta V_{dc} = V_{dc}^* - V_{dc}$) as expressed in (2.23).

3.1.1.2. Need for optimization

The conventional tuning of PI controller comes with several shortcomings as discussed in

Section 1.2.5. In order to satisfy the conditions of both dynamics and stability, optimized values of gains K_p and K_i ought to be obtained. Figure 3.1 demonstrates the block diagram for extraction of PI controller gains using optimization technique.

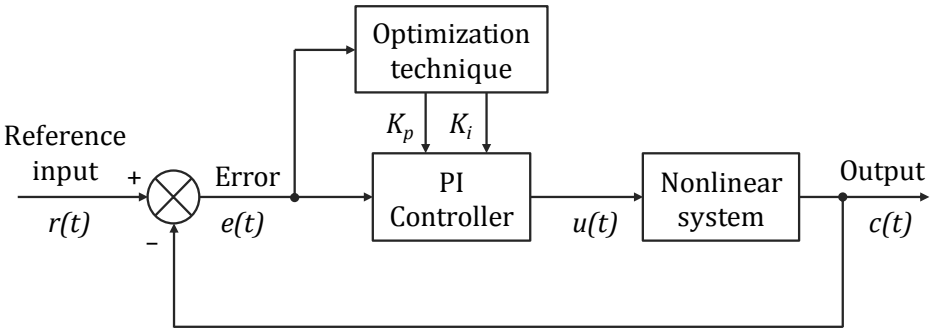


Figure 3.1: Block diagram for PI controller design with optimization technique

3.1.1.3. Objective function and optimization parameters

Here, optimization parameters are the PI controller gains K_p and K_i in the range $0 < K_p < 100$ and $0 < K_i < 100$. Maximum overshoot, rise time, settling time and steady-state error are the constraints that imply optimality of a PI controller. Performance criterion chosen in this paper is integral square error (ISE) that treats both positive and negative errors equally. The objective function to be optimized (J_{ISE}) is formulated as,

$$J_{ISE}(K_p, K_i) = \int_0^t (\Delta V_{dc})^2 dt \tag{3.4}$$

This chapter proposes the implementation of PSO and BFO techniques to find out the optimized gain values of PI controller intended for DC-link voltage regulation of VSI. As discussed in previous chapters, the real power loss inside APF results in performance deterioration. The conventional linear tuning of PI controller adopted in Chapter 2 does not yield satisfactory results for a range of operating conditions. Developed by hybridization of PSO and BFO, an Enhanced BFO technique is proposed in this chapter so as to overcome the drawbacks in both PSO and BFO, and accelerate the convergence of optimization problem. Comparative evaluation of PSO, BFO and Enhanced BFO are carried out with regard to compensation of harmonics in source current in a three-phase

three-wire system with the help of simulations followed by real-time performance analysis in RT-Lab, under a range of supply and sudden load change conditions.

The mechanisms and iterative algorithms of PSO and BFO are explained in Sections 3.2 and 3.3. Section 3.4 describes the mechanism and algorithm of proposed Enhanced BFO technique, developed by the hybridization of PSO and BFO. This is followed by simulation and RT-Lab results obtained with APFs employing conventional and optimized PI controllers in Section 3.5. Finally, Section 3.6 summarizes the chapter.

3.2. Particle Swarm Optimization

Inspired by the social behavior of organisms in a bird flock or fish school, and introduced by Eberhart and Kennedy in the year 1995, PSO emerged as a promising nature-inspired stochastic approach of evolutionary computation. With time, PSO has established itself as a potential non-gradient optimization tool. The PSO algorithm is very simple to implement, computationally less expensive because of its low CPU and memory requirements, and independent of nature and initial condition of the system.

3.2.1. Mechanism of PSO

For initialization, a group of randomly dispersed particles are assigned with some arbitrary velocities. The particles fly through the problem space in search of global optimum position. The PSO system combines a social-only model and a cognition-only model [69], [123]. The social-only component suggests the individuals to ignore their own experiences and adjust their behavior according to the intelligence of neighboring individuals. In contrast, the cognition-only component treats the individual experience of each particle. The fundamental elements of PSO are defined as follows:

a) **Particle position:** It is a candidate solution represented by a P-dimensional vector, where P is the number of parameters to be optimized. At k^{th} iteration, the i^{th} particle X_k^i can be described as,

$$X_k^i = \left[x_k^{i,1}, x_k^{i,2}, \dots, x_k^{i,P}\right] \quad (3.5)$$

Where,

$x_k^{i,1}, x_k^{i,2}, \dots, x_k^{i,P}$: Parameters to be optimized

$x_k^{i,m}$: Position of i^{th} particle with respect to m^{th} dimension i.e., the value of m^{th} optimization parameter in i^{th} candidate solution

b) **Population:** It is a set of S number of particles at k^{th} iteration, given by

$$Population_k = [X_k^1, X_k^2, \dots, X_k^S]^T \quad (3.6)$$

c) **Swarm:** It is an apparently disorganized population of moving particles that tend to cluster together while each particle seems to be moving in a random direction.

d) **Particle velocity:** It is the velocity of moving particles represented by a P-dimensional vector. The velocity of i^{th} particle at k^{th} iteration can be expressed as,

$$V_k^i = \left[v_k^{i,1}, v_k^{i,2}, \dots, v_k^{i,P}\right] \quad (3.7)$$

Where, $v_k^{i,m}$ is the velocity component of i^{th} particle with respect to m^{th} dimension.

e) **Individual or Local best:** As a particle moves through the search space, it compares its current fitness value to the best fitness value it has ever attained at any point of time during its journey. The best position associated with the best fitness achieved thus far by the i^{th} particle is called the individual best (x_{Lbest}^i).

In a minimization problem with objective function J, the individual best of i^{th} particle at k^{th} iteration is determined such that,

$$J\left(X_{Lbest}^i\right) \leq J\left(X_\tau^i\right), \tau \leq k \quad (3.8)$$

For i^{th} particle, individual best at k^{th} iteration can be expressed as,

$$X_{Lbest}^i = \left[x_{Lbest}^{i,1}, x_{Lbest}^{i,2}, \dots, x_{Lbest}^{i,P}\right] \quad (3.9)$$

f) **Global best:** It is the best position attained by any of the particles in the swarm. Hence global best position can be defined as,

$$J\left(X_{Gbest}^i\right) \leq J\left(X_{Lbest}^i\right), i = 1,2, \dots S \quad (3.10)$$

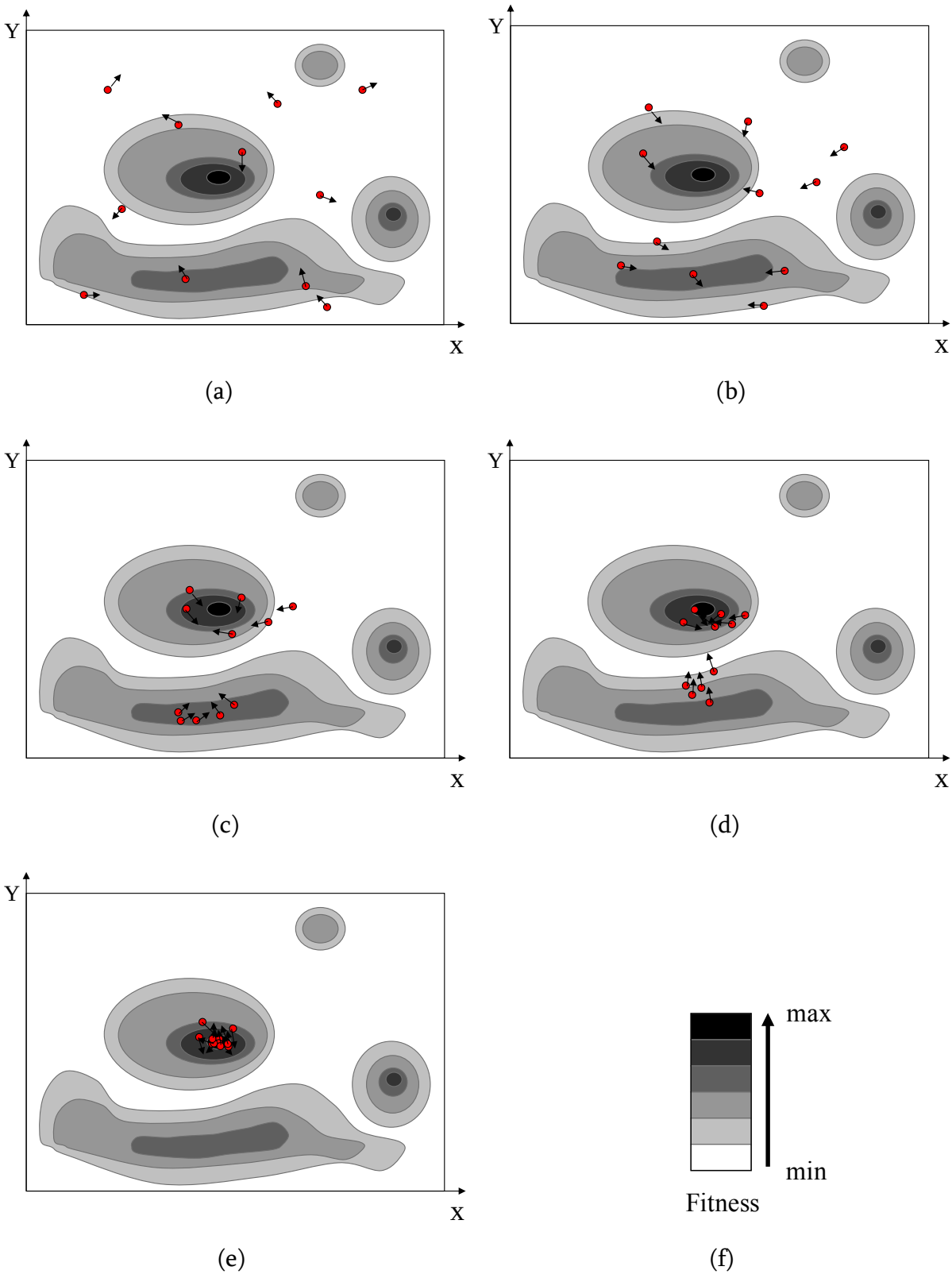


Figure 3.2: Trajectory of particles in the search space at various iterations in order (a)-(e) while moving towards the global minima, (f) Figure indicating the values of fitness function at various locations in the search space

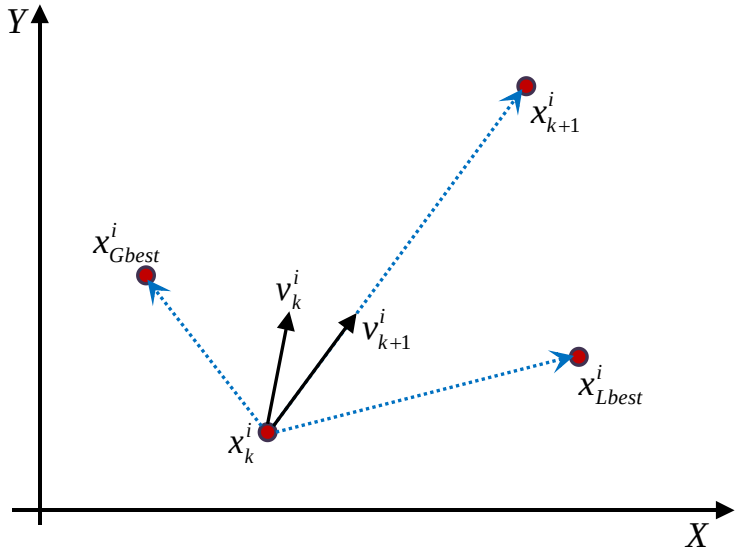


Figure 3.3: Position and velocity update of i^{th} particle in the swarm

The trajectory of particles while moving towards global optima in search space is shown in Figure 3.2. Figure 3.3 depicts the position and velocity update of particles in PSO.

The particles update their positions and velocities in accordance with (3.11) and (3.12), formulated by taking into account both the social-only and cognition-only components.

$$v^i_{k+1} = w \cdot v^i_k + c_1 \cdot r_1 \cdot \left[x^i_{Lbest} - x^i_k\right] + c_2 \cdot r_2 \cdot \left[x^i_{Gbest} - x^i_k\right] \tag{3.11}$$

$$x^i_{k+1} = x^i_k + v^i_{k+1} \tag{3.12}$$

In the expressions (3.11) and (3.12),

k and i	:	Indices for number of iterations and particle number
x^i_k and v^i_k	:	Current position and velocity of i^{th} particle at k^{th} iteration
x^i_{k+1} and v^i_{k+1}	:	Current position and velocity of i^{th} particle at $(k+1)^{\text{th}}$ iteration
w, c_1 and c_2	:	Inertia, cognitive and social constants
r_1 and r_2	:	Random numbers in the interval $[-1, 1]$

Acceleration of particles is decided by the values of constants c_1 and c_2, whereas w provides a sense of balance between local and global searches. The exploration of new search space depends upon the value of inertia constant (w).

Eberhart and Shi brought in an inertia constant that decreases linearly with successive iterations as given in (3.13) [124].

$$w = w_{max} - (w_{max} - w_{min})\frac{g}{G} \tag{3.13}$$

Where,

g	:	Index representing current number of evolutionary generation
G	:	Predefined value of maximum number of generations
w_{max} and w_{min}	:	Maximal and minimal inertial weights

Initially, the value of w is taken 0.9 in order to allow the particles to find the global optimum neighborhood faster. Value of w is set to 0.4 upon finding out the optima, so that the search is shifted from exploratory mode to exploitative mode.

The search for global optimum position terminates when one of the following two stopping criteria is met:

a) The predefined maximum number of iterations are executed
b) Further better optimum solution is not available

3.2.2. Iterative algorithm for PSO

The iterative algorithm of PSO is as follows and the flowchart of PSO algorithm is presented in Figure 3.4.

Step 1: Initialize the size of swarm, dimension of search space, maximum number of iterations and the PSO constants w, c_1 and c_2.

Define the random numbers r_1 and r_2.

Find out the current fitness of each particle in the population.

Step 2: Assign the particles with some random initial positions (x) and velocities (v).

Set the iteration counter (k) to zero.

For the initial population, local best fitness of each particle is its own fitness and local best position (x^i_{Lbest}) of each particle is its own current position i.e.

$$x^i_{Lbest} = \text{ current position of } i^{\text{th}} \text{ particle}$$

Step 3: The global best fitness value can be calculated by,

$$\text{Global best fitness} = min \text{ (local best fitness)}$$

The position corresponding to global best fitness is the global best position $\left(x_{Gbest}^{i}\right)$.

Step 4: Update the particle velocity and particle position of swarm for next iteration by,

$$v_{k+1}^{i} = w \cdot v_{k}^{i} + c_1 \cdot r_1 \cdot \left[x_{Lbest}^{i} - x_{k}^{i}\right] + c_2 \cdot r_2 \cdot \left[x_{Gbest}^{i} - x_{k}^{i}\right]$$

$$x_{k+1}^{i} = x_{k}^{i} + v_{k+1}^{i}$$

Step 5: Increment the iteration counter by setting, $k = k + 1$.

Find out the value of current fitness function for each particle.

If current fitness < local best fitness, then set

$$\text{Local best fitness} = \text{current fitness}$$

$$x_{Lbest}^{i} = \text{current position}$$

Step 6: After calculating the local best fitness of each particle, the current global best fitness for the k^{th} iteration is determined by,

$$\text{Current global best fitness} = min \text{ (local best fitness)}$$

If current global best fitness < global best fitness, then

$$\text{Global best fitness} = \text{current global best fitness}$$

The position corresponding to global best fitness is assigned to x_{Gbest}^{i}.

Step 7: Repeat Steps 5 and 6 until k becomes equal to the maximum number of iterations defined in Step 1 or there is no further improvement in the global best fitness value.

Step 8: Terminate the iterative algorithm, when there is no further execution of iterations.

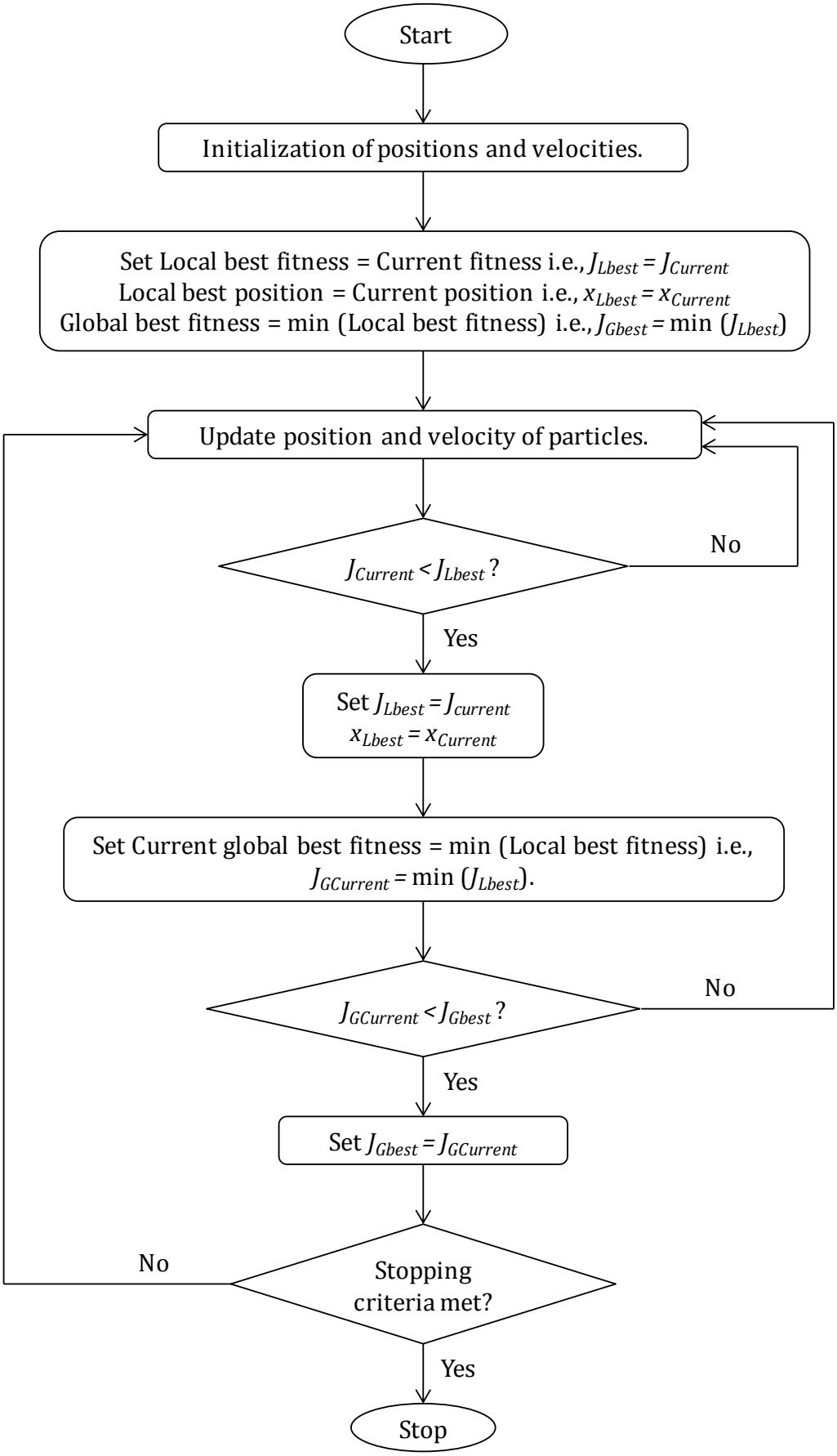


Figure 3.4: Flowchart of PSO

3.3. Bacterial Foraging Optimization

The non-gradient optimization technique BFO is inspired by the foraging strategy used by *E.coli* bacteria inside human intestine in such a way that, it maximizes their energy intake (E) per unit time (T) spent in foraging. Here the bacteria undergo Natural selection, in which the ones with poor foraging strategy are eliminated and those with good foraging strategies survive. It was introduced by Passino in 2002 as a global optimization tool and further established by Mishra in the year 2005 for harmonic estimation in power system voltage/current waveforms. In this short span of time, BFO has grabbed very much attention, since it finds vast application in many real world optimization problems.

3.3.1. Mechanism of BFO

The BFO technique mimics four principal mechanisms observed in bacteria viz. chemotaxis, swarming, reproduction and elimination-dispersal. These are explained below in brief.

1) Chemotaxis

If θ and $J(\theta)$ represent the position and fitness of a bacterium, the objective is to find the minimum of $J(\theta), \theta \in \Re^P$; where the measurements or an analytical description of the gradient $\nabla J(\theta)$ is not available.

Following are the three conditions that arise

a) $J(\theta) < 0$; nutrient-rich environment

b) $J(\theta) = 0$; neutral environment

c) $J(\theta) > 0$; noxious environment

Basically, Chemotaxis is the movement of *E.coli* bacteria inside human intestine in search of nutrient-rich location and away from noxious environment. This is accomplished with the help of locomotory organelles known as Flagella.

Chemotactic movement is achieved by either of the following two ways,

a) Swimming (in the same direction as the previous step)

b) Tumbling (in an absolutely different direction from the previous one)

Suppose $\theta^i(j,k,l)$ represents the i^{th} bacterium at j^{th} chemotactic, k^{th} reproductive and l^{th} elimination-dispersal step.

Then, chemotacic movement of the bacterium may be mathematically represented by (3.14).

$$\theta^i(j+1,k,l) = \theta^i(j,k,l) + C(i)\frac{\Delta(i)}{\sqrt{\Delta^T(i)\cdot\Delta(i)}} \tag{3.14}$$

In the expression, $C(i)$ is the size of unit step taken in a random direction and $\Delta(i)$ indicates a vector in the arbitrary direction whose elements lie in $[-1,1]$.

2) Swarming

This group behavior is seen in several motile species of bacteria, where the cells when stimulated by high level of a chemical *Succinate*, release an attractant *Aspertate*. This helps them to propagate collectively as concentric patterns of swarms with high bacterial density, while moving up in the nutrient gradient. A repelling behavior is also seen in the population, where a bacterium keeps the nearby bacteria from consuming nutrients closer to its present location. Moreover, there exist is a constraint that, any two bacteria can't occupy the same location. This characteristic is termed as repellent effect.

The cell-to-cell signaling in bacterial swarm via attractant and repellant ($J_{cc}(\theta(i,j,k,l))$) may be modelled as per (3.15).

$$\begin{aligned} J_{cc}\big(\theta(i,j,k,l)\big) &= \sum_{i=1}^{S} J_{cc}\left(\theta,\theta^i(j,k,l)\right) \\ &= \sum_{i=1}^{S}\left[-d_{att}\exp\left(-w_{att}\sum_{m=1}^{P}\left(\theta_m-\theta_m^i\right)^2\right)\right] \\ &+ \sum_{i=1}^{S}\left[h_{rep}\exp\left(-w_{rep}\sum_{m=1}^{P}\left(\theta_m-\theta_m^i\right)^2\right)\right] \end{aligned} \tag{3.15}$$

Here S indicates the total number of bacteria in the population, P is the number of variables to be optimized, $\theta = [\theta_1, \theta_2, \dots, \theta_P]^T$ is a point in the P-dimensional search domain that represents the positions of bacteria in the swarm, and θ_m^i is the m^{th} component of the i^{th} bacterium position θ^i. Coefficients d_{att} and w_{att} are the measures of quantity and diffusion rate of the attractant signal respectively. Similarly, h_{rep} and w_{rep} represent the measures of quantity and diffusion rate of repellant effect respectively.

Now, the resulting objective function $J\big(\theta(i,j,k,l)\big)$ becomes

$$J\big(\theta(i,j,k,l)\big) = J\big(\theta(i,j,k,l)\big) + J_{cc}\big(\theta(i,j,k,l)\big) \tag{3.16}$$

3) Reproduction

The fitness value of a bacterium after travelling N_c chemotactic steps can be evaluated by,

$$J_{health}^i = \sum_{j=1}^{N_c+1} J^i(j,k,l) \tag{3.17}$$

In (3.17), J_{health}^i represents the health of i^{th} bacterium.

The least healthy bacteria constituting half of the population (S_r) are eventually eliminated, while each of the healthier bacteria asexually reproduce by splitting into two, which are then placed in the same location. Ultimately, the population remains constant.

If S number of bacteria constitute the population,

$$S_r = \frac{S}{2} \tag{3.18}$$

4) Elimination and dispersal

It is possible that the local environment where bacterial population live changes either gradually via consumption of nutrients or suddenly due to some other influence such as significant heat rise. Following this behaviour, BFO algorithm makes some bacteria to get eliminated and dispersed with probability P_{ed} after N_{re} number of reproductive events. This is to ensure that the bacteria do not get trapped into a local optimum instead of global optima.

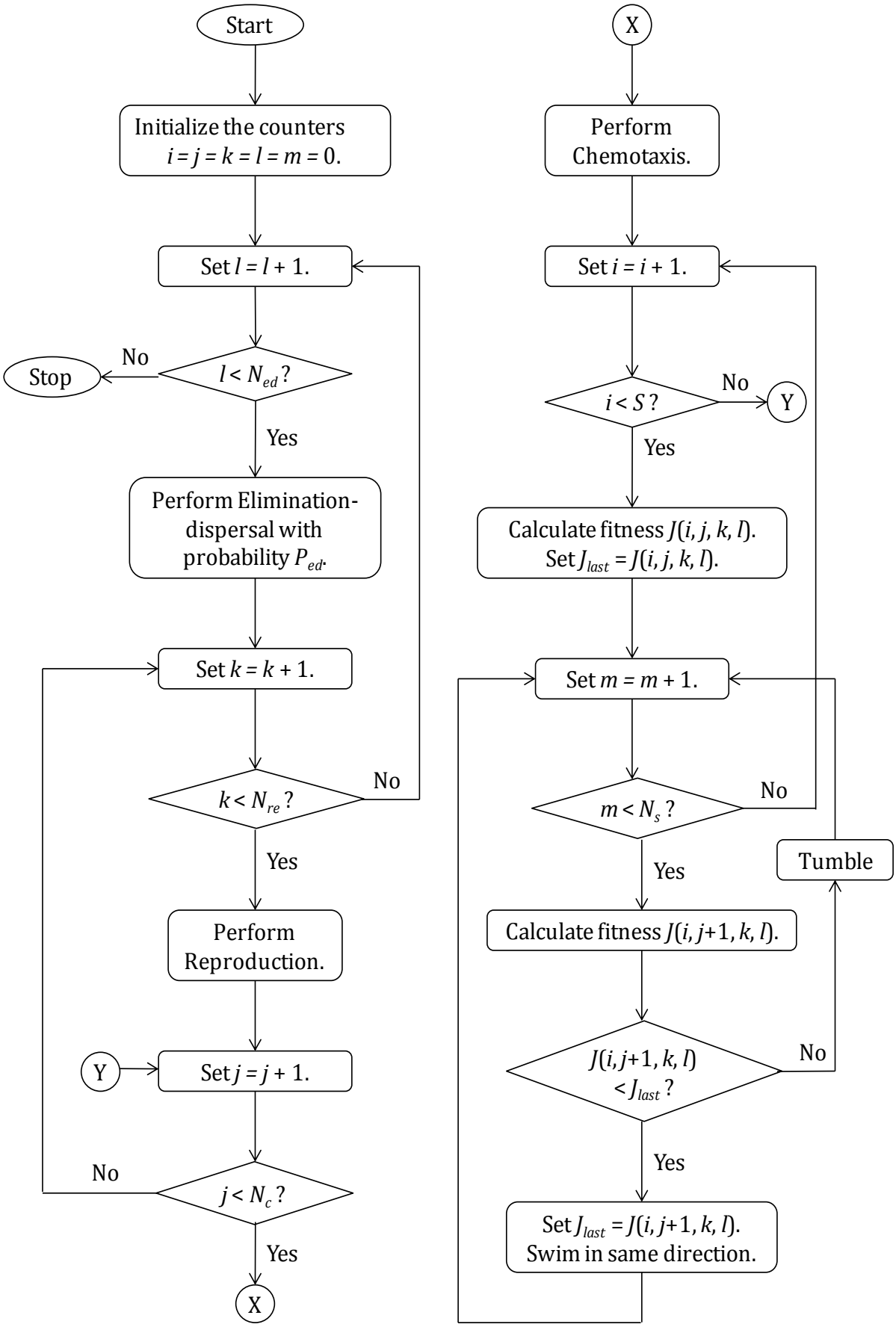


Figure 3.5: Flowchart of BFO

3.3.2. Iterative algorithm for BFO

The iterative algorithm of BFO is as follows and the flowchart is depicted in Figure 3.5.

Parameters initialization:

Step 1: Initialize the following parameters.

P : Dimension of search space

S : Total number of bacteria in the population

N_c : Number of chemotactic steps

N_s : Swim length

N_{re} : Number of reproduction steps

N_{ed} : Number of elimination-dispersal events

P_{ed} : Probability at which elimination-dispersal occurs

$C(i)$: Size of step taken by i^{th} bacterium in a random direction specified by tumble, for $i = 1,2 \dots S$

θ^i : Position of i^{th} bacterium in the search space, for $i = 1,2 \dots S$

Initially, all the counters (counters for population, chemotaxis, reproduction and elimination-dispersal) are set to zero i.e., $i = j = k = l = 0$.

Iterative algorithm:

Step 2: Elimination-dispersal loop: $l = l + 1$.

Step 3: Reproduction loop: $k = k + 1$.

Step 4: Chemotaxis loop: $j = j + 1$.

a) For each of the bacteria ($i = 1,2,3 \dots, S$) in the population take a chemotactic step as follows.

b) Compute fitness function $J(i, j, k, l)$ and set

$$J(i, j, k, l) = J(i, j, k, l) + J_{cc}(\theta(i, j, k, l)).$$

Here, $J_{cc}(\theta(i, j, k, l))$ is the cell-to-cell signaling effect defined in (3.15).

c) Set $J_{last} = J(i,j,k,l)$ to save this value since a better cost may be found via a run.

d) Tumble:

Generate a random vector $\Delta(i) \in \Re^P$, which indicates a vector in arbitrary direction whose elements lie in $[-1, 1]$.

e) Perform chemotactic movement as per (3.14). This results in a step of size $C(i)$ in the direction of the tumble for i^{th} bacterium.

f) Compute $J_{cc}(\theta(i, j+1, k, l))$.

Set $J(i, j+1, k, l) = J(i, j, k, l) + J_{cc}(\theta(i, j+1, k, l)$.

g) Swim:

(i) Let $m = 0$ (counter for swim length).

(ii) While $m < N_s$ (if have not climbed down too long).

Let $m = m + 1$.

If $J(i, j+1, k, l) < J_{last}$ (if doing better), set

$$J_{last} = J(i, j+1, k, l)$$

$$\theta^i(j+1, k, l) = \theta^i(j, k, l) + C(i)\frac{\Delta(i)}{\sqrt{\Delta^T(i) \cdot \Delta(i)}}$$

Use this $\theta^i(j+1, k, l)$ to compute the new $J(i, j+1, k, l)$ as shown in (f).

Else, let $m = N_s$.

h) If $i \neq S$, go to next bacterium $(i + 1)$ and execute (b).

Step 5: If $j < N_c$, go to step 4. In this case continue chemotaxis since the life of the bacteria is not over.

Step 6: Reproduction:

a) For the given k and l, and for $i = 1,2 \ldots S$, find the fitness J^i_{health} of each bacteria using (3.17).

b) Sort the bacteria and chemotactic parameters $C(i)$ in ascending order of cost J_{health} (higher cost means lower health).

c) The S_r number of bacteria with highest values of J_{health} die. At the same time, the remaining S_r number of bacteria with lower values of cost function split into two.

Step 7: If $k < N_{re}$, go to step 3. In this case, the number of specified reproduction steps is not reached, so the next generation of chemotactic loop is started.

Step 8: Elimination-dispersal:

a) For $i = 1,2\ldots,S$, perform elimination and dispersal of bacteria with probability P_{ed} (this keeps the population of bacteria constant).
If a bacterium is eliminated, simply disperse another one to a random location on the optimization domain.

b) If $l < N_{ed}$, then go to step 2. Otherwise, end.

3.4. Enhanced BFO

Taking into consideration all the drawbacks and advantages of PSO and BFO algorithms discussed in Chapter 1, an Enhanced BFO algorithm is developed here that has the combined advantages of BFO and PSO, and is also capable of overcoming the limitations in both. The performance of PSO is degraded in problems with multiple optima owing to a phenomenon called premature convergence, where the particles tend to converge and ultimately get trapped in a local best position as the global best remains undiscovered. Enhanced BFO overcomes this drawback through elimination-dispersal of bacteria, thereby ensuring convergence to global optimum. Furthermore, the movement of individuals in traditional BFO algorithm is not defined in any specific direction. Random search directions delay the convergence to global solution. However, unlike BFO, at any particular instant in PSO each particle memorizes its own best solution (local best) as well

as the best solution of entire swarm (global best) owing to the memory it possesses. Thereby, velocity and direction of particles are obtained as outcome of their social interactions and memory storage capability. This characteristic of PSO is incorporated in Enhanced BFO that improves search efficiency, global optimum solution accuracy and convergence speed, which are the key attributes of an optimization algorithm. In Enhanced BFO, the chemotaxis, swarming, reproduction, and elimination-dispersal events carried out in BFO realizing cell-to-cell communication, survival of the fittest, elimination of least healthy bacteria in the population, and exploration of new search areas are supplemented with the ability of PSO to exchange social information and possession of adaptable particle velocity. Hence, this algorithm yields relatively more optimized result compared to BFO and PSO implemented alone. The mechanism of Enhanced BFO and iterative algorithm realizing this mechanism are presented below.

3.4.1. Mechanism of Enhanced BFO

In the beginning of search process, a group of bacteria are randomly dispersed all throughout the search space. Each bacterium is assigned with an arbitrary particle velocity. Fitness values of the bacteria are calculated by taking into consideration the cell-to-cell swarming effect. For the initial population, the local best and global best positions are figured out in exactly same way as done in PSO. In order to update the positions of individuals, chemotaxis is carried out, which utilizes a velocity factor obtained from the velocity update expression used in PSO. After each chemotactic step, fitness value of each particle is calculated. During the search, reproduction and elimination-dispersal events of BFO are also executed. For reproduction, half of the bacterial population with least health are eliminated, while rest half of the population asexually reproduce by each of them splitting into two. Ultimately, the population size remains constant. To simulate elimination-dispersal phenomenon, some bacteria are liquidated at random with a very small probability, while the new replacements are randomly initialized over the search space. At the end of search process, the bacteria reach at the global optimum position. A flowchart of the Enhanced BFO technique is depicted in Figure 3.6.

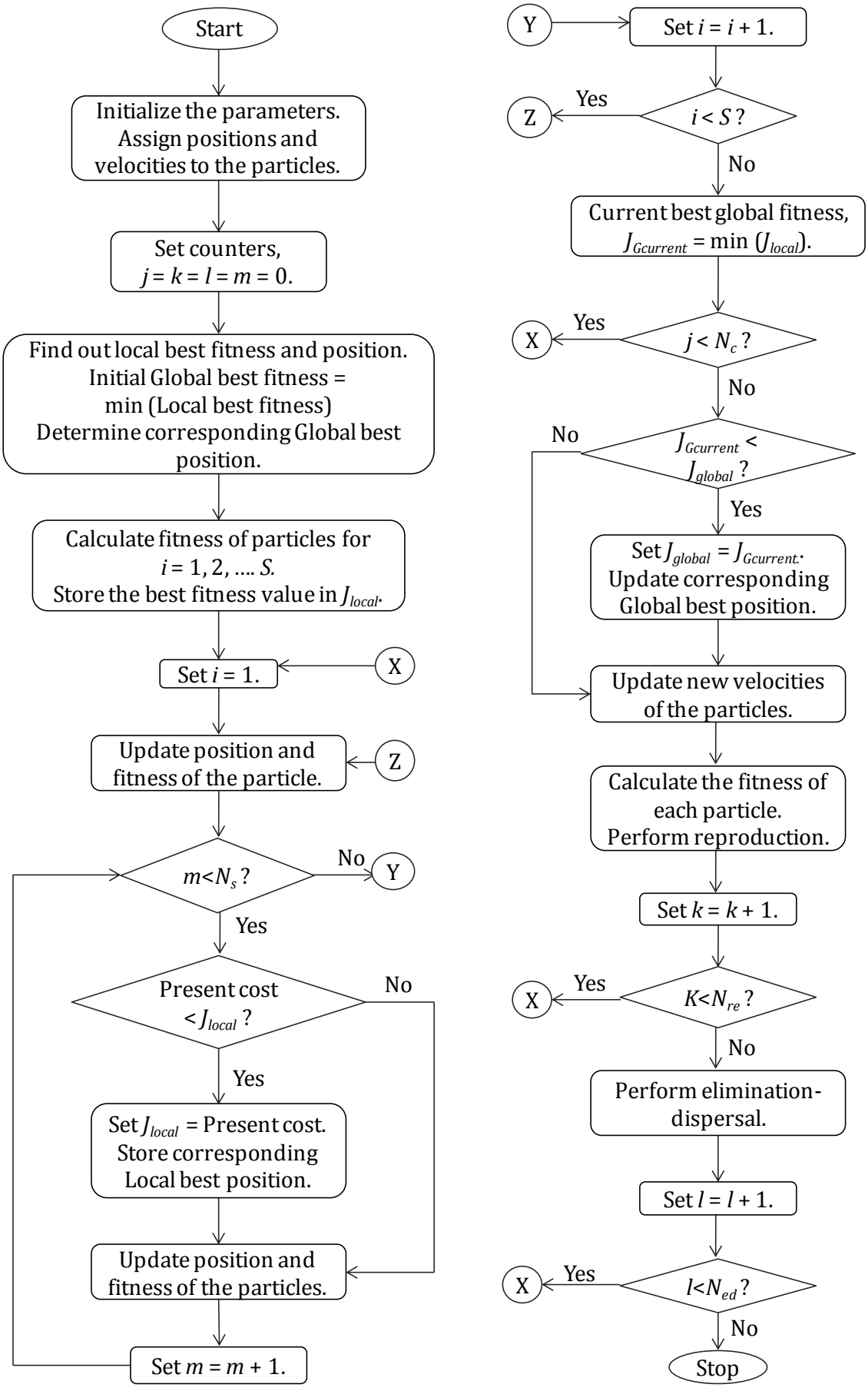


Figure 3.6: Flowchart of Enhanced BFO

3.4.2. Iterative algorithm for Enhanced BFO

Step 1: Initialization:

To begin with, all the parameters related to proposed algorithm are initialized. Each particle in the group are assigned with some random initial position $\theta(i)$, and initial velocity (v) which is a random number in the interval $[-1, 1]$ with elements $n(i); n = 1,2,\ldots,P$.

Step 2: Preliminary assessment of bacterial population:

a) For $i = 1,2,\ldots,S$, current fitness $(J^i_{current})$ of each bacterium in the search space is determined as per the following expression.

$$J^i_{current} = J(i,j,k,l)$$

b) In the beginning of search process, since the bacterial movement is not yet started, the local best fitness (J^i_{local}) and local best position (x^i_{Lbest}) of each bacterium are its current fitness value and current position respectively i.e.

$$J^i_{local} = J^i_{current}$$

$$x^i_{Lbest} = \theta(i,j,k,l)$$

c) The initial global best fitness (J_{global}) of the population is the minimum value of fitness possessed by any of the particle in the population and can be given by,

$$J_{global} = min(J^i_{local})$$

Where, $i = 1,2\ldots S$.

The position corresponding to J_{global} is assigned the global best position (x^i_{Gbest}).

Step 3: Iterative algorithm:

a) Initially the counters for chemotactic loop (j), reproduction loop (k), elimination-dispersal loop (l), and swim length (m) are all set to zero.

b) Taking into account the cell-to-cell attractant effect, the cost function estimated for each of the $i = 1,2, \ldots S$ bacteria is calculated as,

$$J_{cc}\big(\theta(i,j,k,l)\big) = \sum_{i=1}^{S}\left[-d_{att}\cdot \exp\left(-w_{att}\sum_{n=1}^{P}\big(\theta_n - \theta_n^i\big)^2\right)\right] + \sum_{i=1}^{S}\left[h_{rep}\cdot \exp\left(-w_{rep}\sum_{n=1}^{P}\big(\theta_n - \theta_n^i\big)^2\right)\right]$$

$$J(i,j,k,l) = J(i,j,k,l) + J_{cc}\big(\theta(i,j,k,l)\big)$$

$$J_{last} = J(i,j,k,l)$$

The best cost function value is stored in J_{last} until a further better cost is obtained and the best cost of each bacterium (J_{local}^{i}) is updated as,

$$J_{local}(i,j,k,l) = J_{last}(i,j,k,l)$$

c) Chemotactic loop: Starting with $i = 1$, the position and cost function for all the S number of bacteria in the entire population are updated using the expressions,

$$\theta(i,j+1,k,l) = \theta(i,j,k,l) + C(i)\frac{v_k^i}{\sqrt{\left(v_k^i\right)^T \cdot v_k^i}}$$

$$J(i,j+1,k,l) = J(i,j+1,k,l) + J_{cc}\big(\theta(i,j+1,k,l)\big)$$

While $m < N_s$,

If $J(i,j,k,l) < J_{local}$,

Then set $J_{local} = J(i,j,k,l)$.

Updating position and cost function we get,

$$\theta(i,j+1,k,l) = \theta(i,j+1,k,l) + C(i)\frac{v_k^i}{\sqrt{\left(v_k^i\right)^T \cdot v_k^i}}$$

$$J(i,j+1,k,l) = J(i,j+1,k,l) + J_{cc}\big(\theta(i,j+1,k,l)\big)$$

The current position ($x_{current}$) of each bacterium can be given by,

$$x_{current}(i,j+1,k,l) = \theta(i,j+1,k,l)$$

The position corresponding to local best fitness (J^i_{local}) is stored in x^i_{Lbest}.

Increment the counter as, $m = m + 1$.

End the while loop.

To proceed to next bacterium, set $i = i + 1$ until $i = S$.

d) In each chemotactic step, calculate the current global best fitness function value ($J_{Gcurrent}$) and continue the chemotactic loop if still $j < N_c$.

$$J_{Gcurrent} = \min\left(J^i_{local}\right)$$

Where, $i = 1, 2 \ldots S$.

If $J_{Gcurrent} < J_{global}$, set $J_{global} = J_{Gcurrent}$.

The global best position (x^i_{Gbest}) is updated with the position corresponding to J_{global}.

e) The particles update their new velocities and directions by the equation,

$$v^i_{k+1} = w \cdot v^i_k + c_1 \cdot r_1 \cdot \left[x^i_{Lbest} - x^i_{current}\right] + c_2 \cdot r_2 \cdot \left[x^i_{Gbest} - x^i_{current}\right]$$

f) Reproduction:

The health of each bacterium is calculated using the expression given below and then sorted in ascending order of cost function.

$$J^i_{health} = \sum_{j=1}^{N_c+1} J^i(j, k, l)$$

S_r is the number of least healthy bacteria that are discarded out of the population and individuals with best health are split into two, keeping the population size constant.

g) If $k < N_{re}$, continue with the next reproductive iteration by setting, $k = k + 1$.

The entire iterative process is executed repeatedly until the specified number of reproductive steps (generations) are executed.

h) Elimination-dispersal loop:

With a probability of P_{ed}, the elimination-dispersal is performed to ease the exploration of new search areas that may lead to better optimal solution.

If elimination-dispersal counter $l < N_{ed}$, execute successive elimination-dispersal events with the increment of counter l after each iteration.

Terminate the iterative process when the counter l reaches its maximum specified value i.e., the number of elimination-dispersal events N_{ed}.

3.5. Results and Discussion

Extensive simulations are carried out followed by analysis in RT-Lab, in order to find out the effectiveness of APF with the above discussed optimization techniques under three different supply conditions. System configuration of shunt APF along with the three-phase nonlinear diode rectifier loads is depicted in Figure 3.7. Values of all the system parameters used for simulation and parameters used in optimization techniques are clearly indicated in Tables 3.1 and 3.2 respectively.

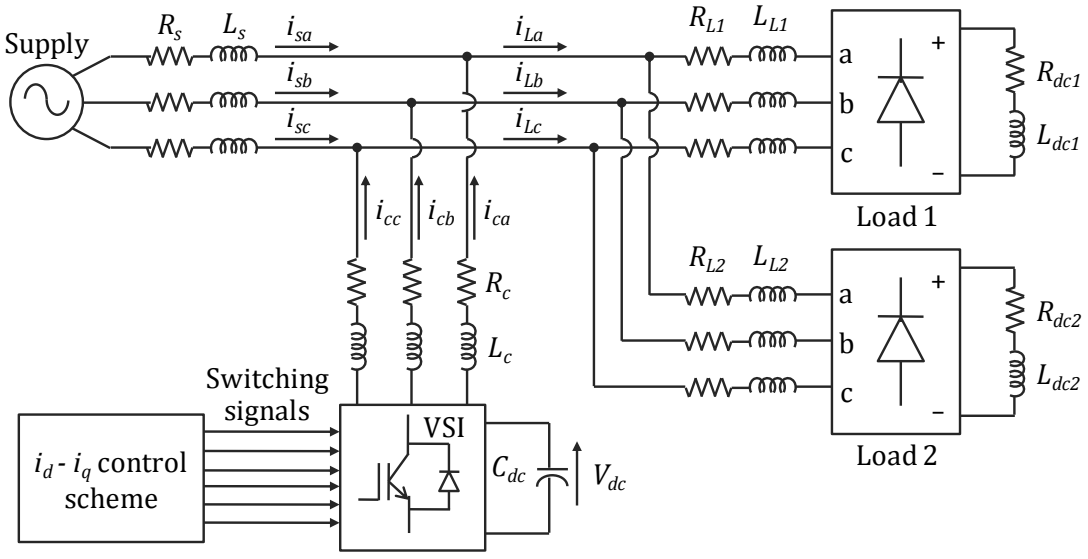


Figure 3.7: VSI-based shunt APF system configuration along with the nonlinear loads

Table 3.1: Values of system parameters used in simulation

Parameter	Notation	Value
Supply frequency	f	50 Hz
Source impedance	(R_s, L_s)	(10 mΩ, 50 μH)
Load-1 parameters	(R_{L1}, L_{L1}), (R_{dc1}, L_{dc1})	(0.1 Ω, 3 mH), (25 Ω, 25 mH)
Load-2 parameters	(R_{L2}, L_{L2}), (R_{dc2}, L_{dc2})	(0.1 Ω, 3 mH), (25 Ω, 60 mH)
DC-link capacitance	C_{dc}	3 mF
Reference DC-link voltage	${V_{dc}}^*$	800 V
AC-side filter parameters	(R_c, L_c)	(0.1 Ω, 1 mH)

Table 3.2: Values of parameters used in Optimization techniques

Parameter	Notation	Value
Population size	S	8
Maximum No. of iterations	N	50
Dimension of search space	P	2
Acceleration constants	c_1, c_2	1.2, 0.12
Inertia constant	w_{max}, w_{min}	0.9, 0.4
No. of chemotactic steps	N_c	5
Length of swim	N_s	3
No. of reproduction steps	N_{re}	10
No. of elimination-dispersal steps	N_{ed}	3
Probability of elimination-dispersal events	P_{ed}	0.25
Coefficients of swarming for attractant signal	d_{att}, w_{att}	0.01, 0.04
Coefficients of swarming for repellent effect	h_{rep}, w_{rep}	0.01, 10

The main purpose of this chapter being optimization of APF performance in harmonic compensation, a conventional six-switch VSI based APF for three-phase three-wire system has been considered for simplicity of analysis. From Chapter 2 it is found that, $i_d - i_q$ scheme offers superior load compensation under all kinds of supply and loading conditions. Hence, it has been employed for generation of reference compensation currents in this chapter. Figure 3.8 illustrates the block diagram for closed loop control of inverter DC-link voltage for the APF employing optimization technique (PSO, BFO and Enhanced BFO). The closed loop voltage control is accomplished as:

a) The error in DC-link inverter voltage (ΔV_{dc}) with respect to a reference value is tracked and fed to a PI controller (whose gains are optimized).
b) Output of PI controller (i_{d1h}) is utilized for generation of reference filter currents.
c) The actual and reference filter currents are compared in Hysteresis controller.
d) The PWM pulses thus generated are then utilized to switch the IGBTs inside VSI.

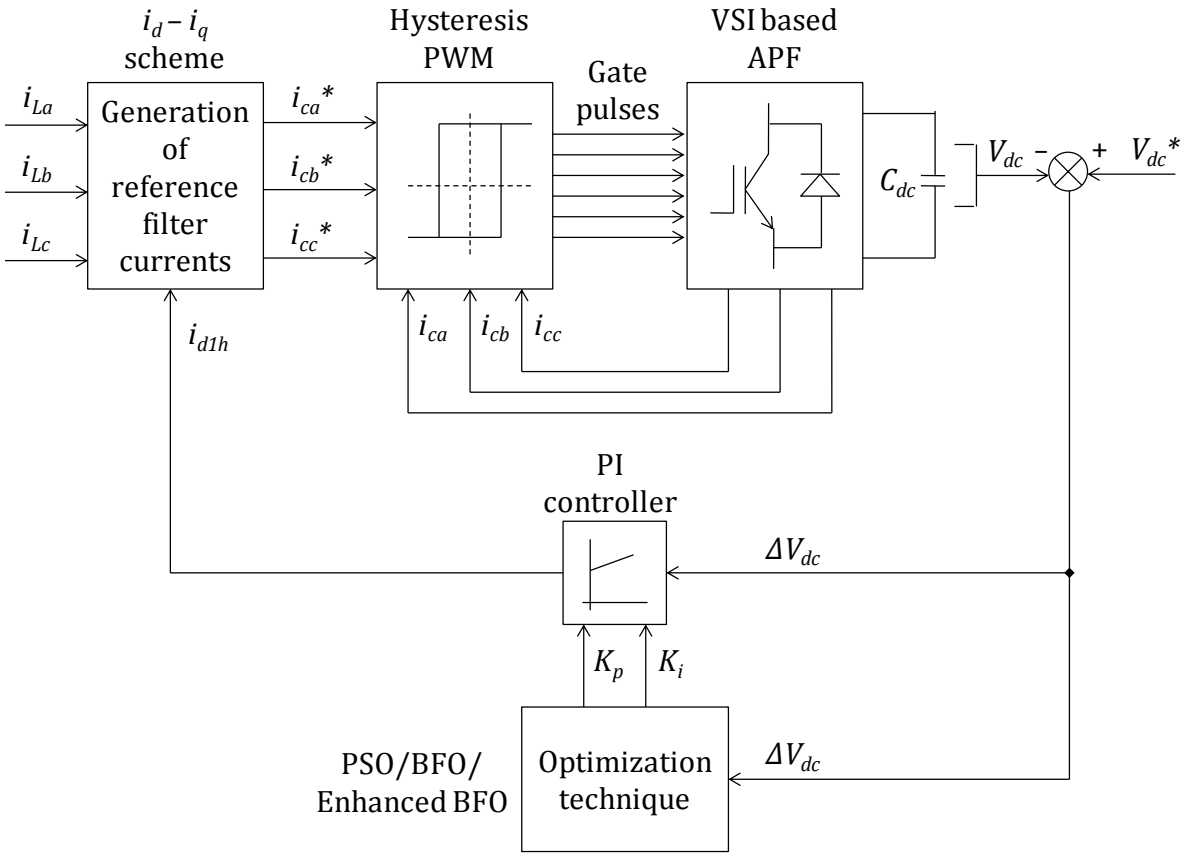


Figure 3.8: Block diagram of closed loop control of inverter DC-link voltage for the APF system employing optimization techniques

3.5.1. Simulation results

The algorithms for PSO, BFO and Enhanced BFO are developed using MATLAB programming, which are further linked to the APF system model developed in MATLAB/Simulink.

This is achieved using the "*simopt*" and "*simset*" commands as follows,

simopt = simset('solver','ode45','SrcWorkspace','Current','DstWorkspace','Current');

To supersede the base workspace for data output, an options structure is provided to the *sim* command and both of the following structure fields are set:

a) SrcWorkspace: Specifies which workspace is searched last during hierarchical symbol resolution
b) DstWorkspace: Specifies which workspace is the destination of any logged or exported data

Each of these fields can take any of these three values:

a) Base: Use the base workspace, just as it would be used if no options structure had been provided
b) Current: Supersede the base workspace with the workspace of the function that called the sim command
c) Parent: Supersede the base workspace with the workspace of the function that called the function that called the sim command

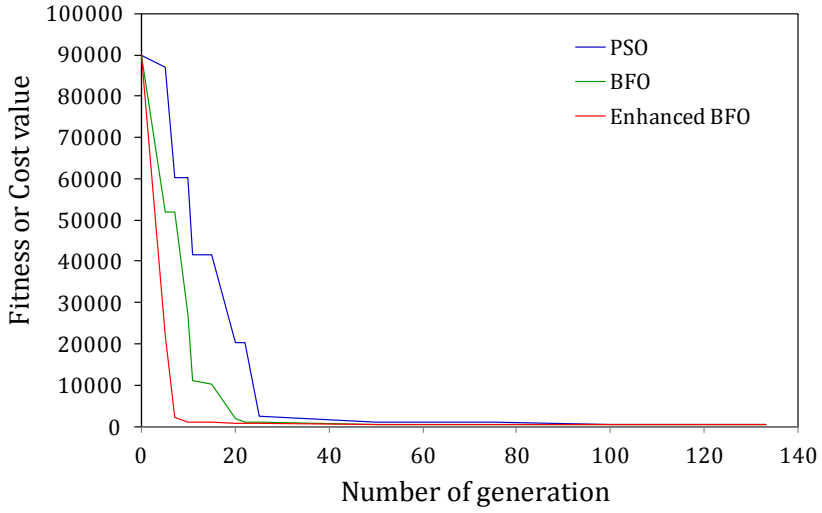
The value of ΔV_{dc} obtained via MATLAB model (.mdl file) is stored in a workspace and hence is accessible at the PSO, BFO and Enhanced BFO programs (.m files) during their execution. The PI controller gain values (K_p and K_i) obtained as outputs of the program files are the required optimized parameter values that are set to be used in the Simulink model. The "solver" is set to "ode45" for variable-step type of solver and to "ode3" for fixed-step type of solver. This is how the optimization algorithms are implemented by linking the MATLAB/Simulink model file to the MATLAB program file. The PI controller gain values obtained with the use of optimization techniques are adjusted dynamically with changes in supply and loading conditions.

Initially, only Load-1 is put into operation until $t = 0.1\,s$ in order to evaluate the harmonic compensation capability of APF. Performance under dynamic conditions is observed by sudden switching on of Load-2 at time instant $t = 0.1\,s$. The nature of supply voltage considered for ideal, distorted and unbalanced supply conditions is exactly same as that taken in Chapter 2.

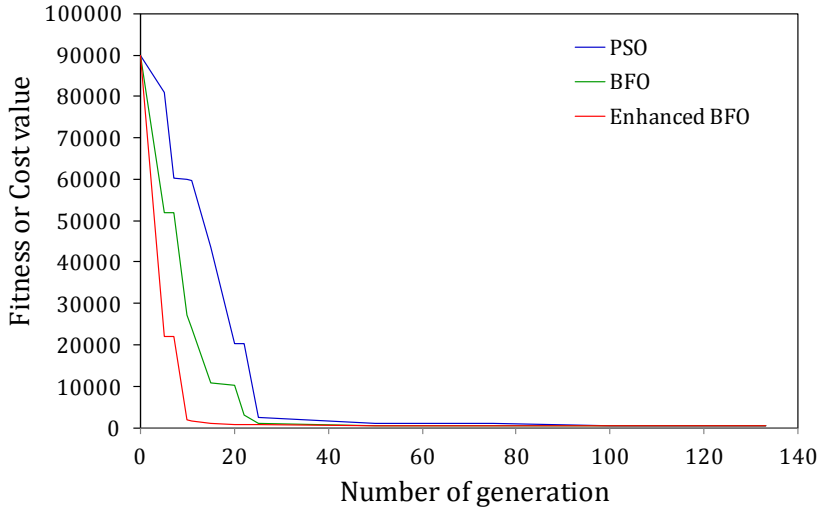
The convergence characteristics of PSO, BFO and Enhanced BFO showing fitness value against number of generations is depicted in Figure 3.9. It shows that, Enhanced BFO reaches at minima in least number of generations compared to PSO and BFO under all kinds of supply voltage conditions, thereby providing approximately instantaneous harmonic compensation.

Relative convergence of DC-link voltage V_{dc} with conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers to overcome the DC-link voltage deviation under the three different supply voltage conditions is presented in Figure 3.10. This indicates that, V_{dc} reaches at its reference of 800 V within nearly one cycle under ideal and distorted supplies; and within 1.5 cycles under unbalanced supply. The convergence to attain the zero-error state is the fastest for Enhanced BFO-based PI controller followed by BFO-based, PSO-based and conventional PI controllers. This small settling time also signifies quick prevail over current harmonics.

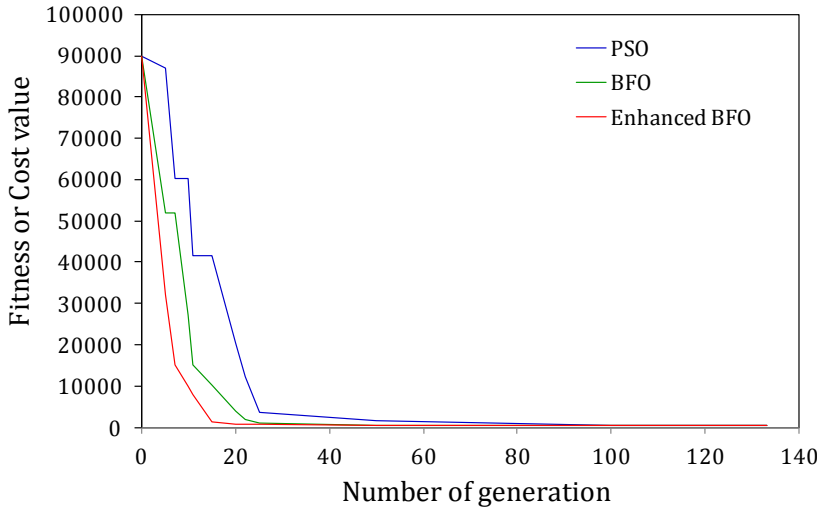
During load variation at $t = 0.1\,s$, the deviation in V_{dc} is maximum for conventional PI and minimum for Enhanced BFO-based PI. The overshoots, undershoots and settling times of V_{dc} transient at starting (at $t = 0\,s$) and during load change (at $t = 0.1\,s$) under ideal, distorted and unbalanced supplies are listed in Tables 3.3, 3.4 and 3.5 respectively for conventional, PSO, BFO and Enhanced BFO-based APFs. There exist overshoots in case of conventional controller at the starting; which is negligible in case of PSO-based, BFO-based and Enhanced BFO-based PI controllers. Furthermore, during the load variation at $t = 0.1s$, conventional PI controller shows the maximum deviation in DC-link voltage whereas; Enhanced BFO-based controller shows the least. Besides, ripples in V_{dc} during steady state are observed to be highest for conventional case and the lowest for Enhanced BFO.



(a)

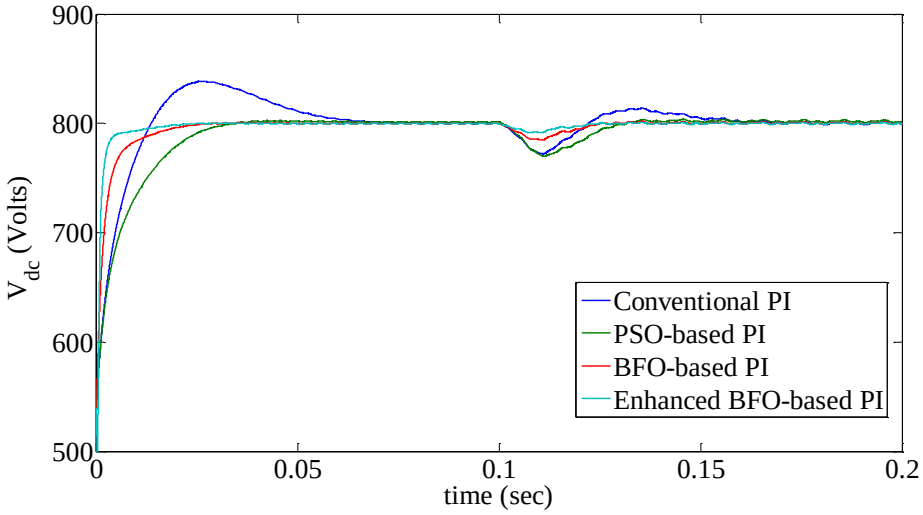


(b)

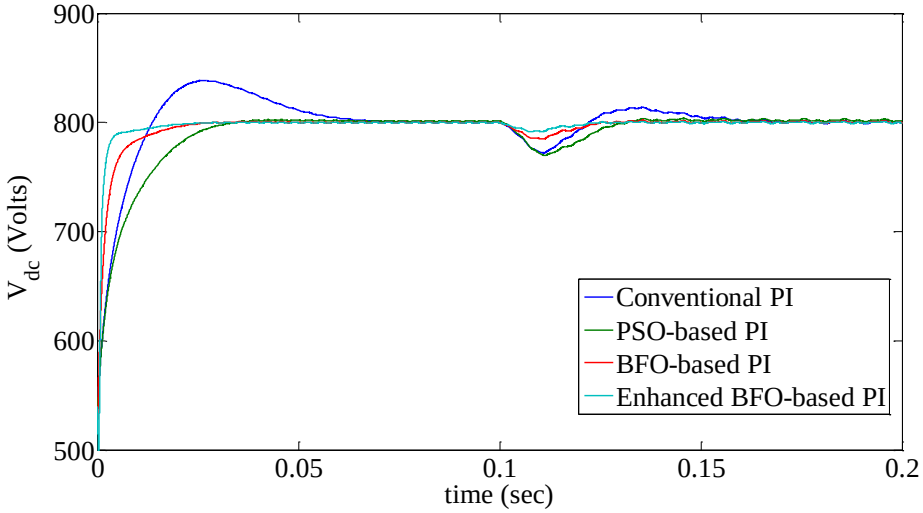


(c)

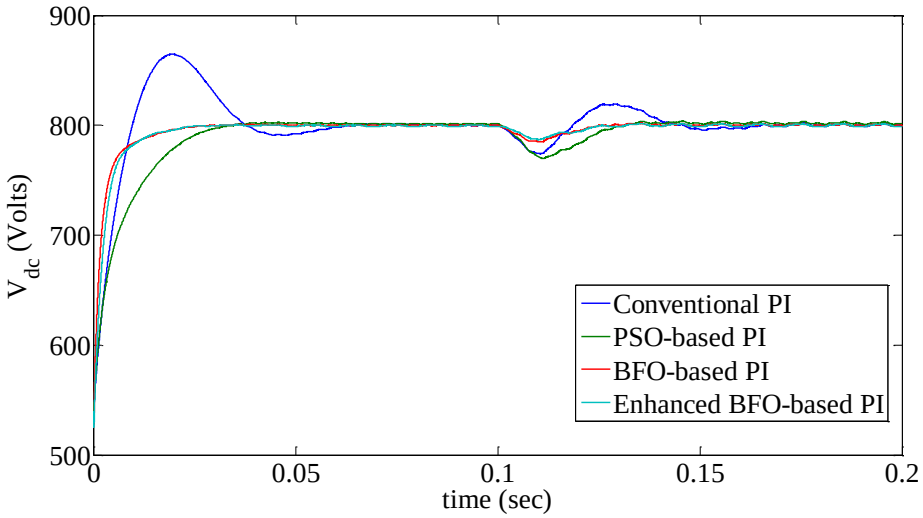
Figure 3.9: Convergence characteristics of PSO, BFO and Enhanced BFO algorithms under (a) Ideal, (b) Distorted, (c) Unbalanced supplies



(a)



(b)



(c)

Figure 3.10: Relative convergence of V_{dc} for conventional, PSO, BFO and Enhanced BFO-based APFs under (a) Ideal, (b) Distorted, (c) Unbalanced supplies

Table 3.3: Comparison of maximum overshoots undershoots and settling times of the four controllers from V_{dc} transient response under ideal supply

Technique employed	At the starting		During load change		
	Maximum overshoot (Volts)	Settling time (sec)	Maximum overshoot (Volts)	Maximum undershoot (Volts)	Settling time (sec)
Conventional	37.1	0.064	13.9	27.9	0.055
PSO	—	0.042	3.8	30.4	0.036
BFO	—	0.027	4.7	16.2	0.025
Enhanced BFO	—	0.016	2.8	7.9	0.022

Table 3.4: Comparison of maximum overshoots undershoots and settling times of the four controllers from V_{dc} transient response under distorted supply

Technique employed	At the starting		During load change		
	Maximum overshoot (Volts)	Settling time (sec)	Maximum overshoot (Volts)	Maximum undershoot (Volts)	Settling time (sec)
Conventional	38.5	0.067	13.8	29.4	0.058
PSO	—	0.051	3.7	29.1	0.038
BFO	—	0.028	5.3	17.3	0.030
Enhanced BFO	—	0.019	3.3	8.1	0.022

Table 3.5: Comparison of maximum overshoots undershoots and settling times of the four controllers from V_{dc} transient response under unbalanced supply

Technique employed	At the starting		During load change		
	Maximum overshoot (Volts)	Settling time (sec)	Maximum overshoot (Volts)	Maximum undershoot (Volts)	Settling time (sec)
Conventional	66.8	0.063	20.8	33.6	0.065
PSO	—	0.058	3.7	35.3	0.037
BFO	—	0.027	5.2	15.8	0.027
Enhanced BFO	—	0.022	3.0	14.9	0.027

Figure 3.11 shows the simulation waveforms for supply voltage (V_s), load current (i_{La}), compensation current (i_{ca}), and source currents obtained after compensation with APFs employing conventional PI (i_{sa1}), PSO-PI (i_{sa2}), BFO-PI (i_{sa3}) and Enhanced BFO-PI (i_{sa4}) under ideal supply. In order to reduce the complexity during the performance analysis, the load current, compensation current and source current of only one phase (phase-a) have been considered and presented here. Similarly, Figure 3.12 shows the simulation waveforms obtained with APF employing conventional, PSO, BFO and Enhanced BFO-based PI controllers under distorted supply. This is followed by the simulation waveforms for APF employing the discussed conventional and optimization based PI controllers in Figure 3.13. The nature of source current waveform before compensation is exactly same as the load current.

It is clearly observed from the simulation results that, irrespective of the nature of supply condition, with the implementation of APF, harmonics in source current are fully compensated by injecting suitable compensating filter currents. However, their THD values signify the major differences in their level of distortion. FFT analyses are done to find out the source current THDs under ideal, distorted and unbalanced supplies. The overall THDs in phase-a of source current before compensation (i.e., load current THD) is found out to be 30.07%, 30.65% and 28.47% for ideal, distorted and unbalanced supply conditions respectively. Chart diagrams in Figures 3.14, 3.15 and 3.16 illustrate a comparative assessment of source current THDs of all three phases obtained with PSO, BFO and Enhanced BFO-based APFs, with that obtained using conventional APF under ideal, distorted and unbalanced supplies. It is revealed that, all the optimization algorithms offer lesser THDs than the conventional APF under all kinds of supplies. Yet Enhanced BFO is the best alternative in terms of harmonics mitigation. The source current THDs are lowered down to nearly 1% with proposed Enhanced BFO even under highly distorted and unbalanced supplies along with sudden change in loading condition. The compensation of current harmonics to such a large extent irrespective of supply voltage is also due to the lower value of source impedance, which contributes to low influence of supply on source current and vice-versa.

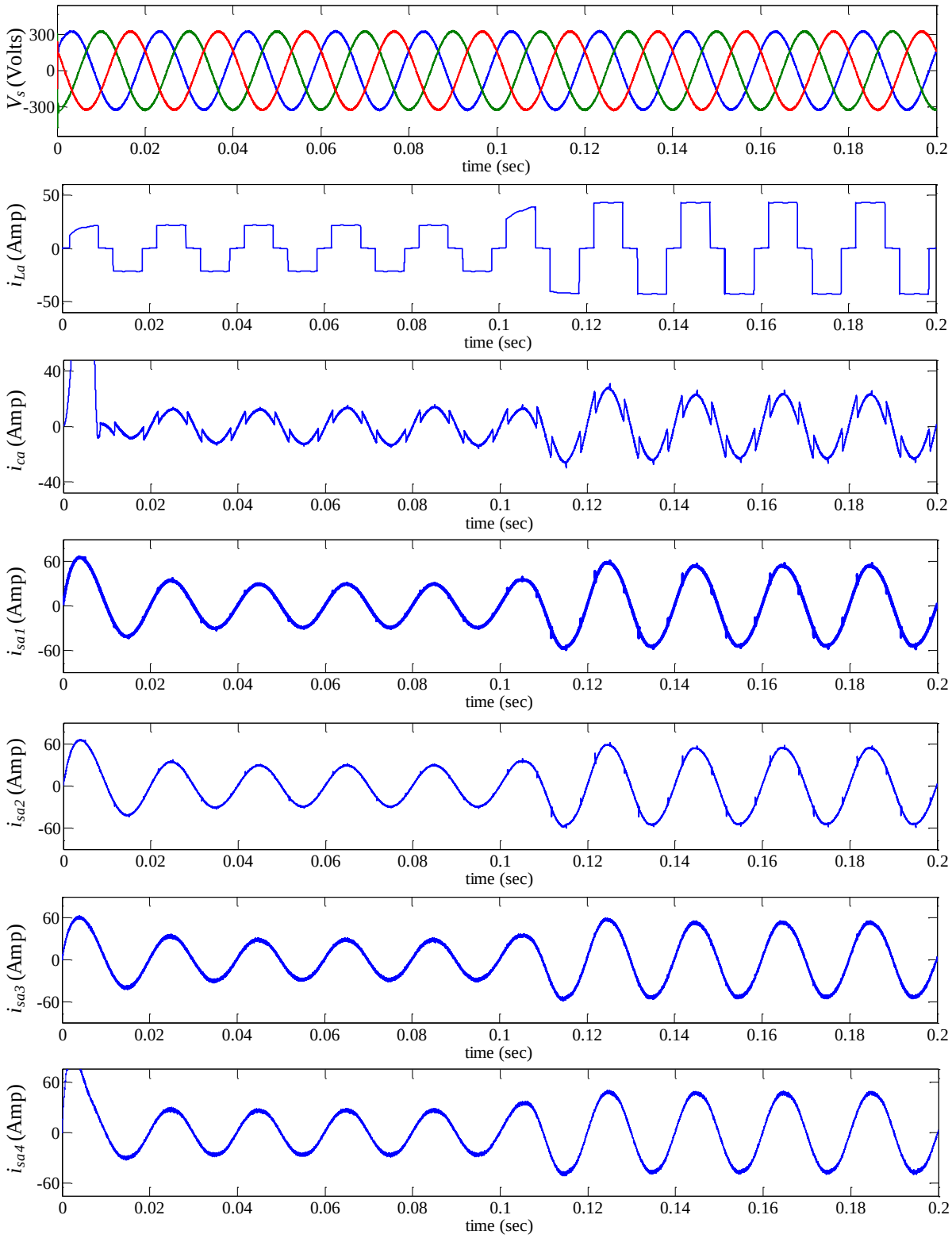


Figure 3.11: Simulation waveforms for supply voltage (V_s), load current in phase-a (i_{La}), compensation current in phase-a (i_{ca}), and source currents in phase-a for APF employing conventional PI (i_{sa1}), PSO-based PI (i_{sa2}), BFO-based PI (i_{sa3}) and Enhanced BFO-based PI (i_{sa4}) under ideal supply

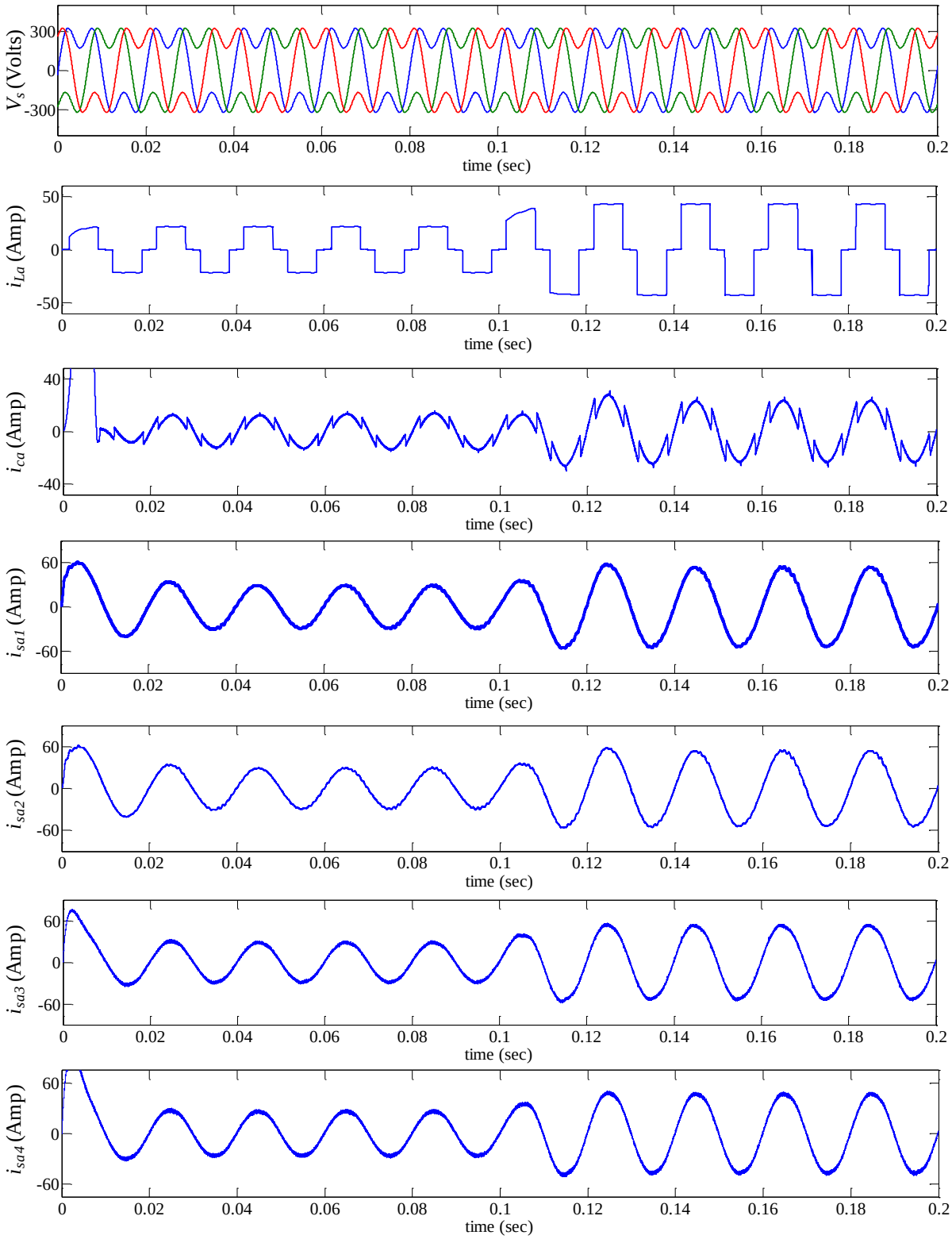


Figure 3.12: Simulation waveforms for supply voltage (V_s), load current in phase-a (i_{La}), compensation current in phase-a (i_{ca}), and source currents in phase-a for APF employing conventional PI (i_{sa1}), PSO-based PI (i_{sa2}), BFO-based PI (i_{sa3}) and Enhanced BFO-based PI (i_{sa4}) under distorted supply

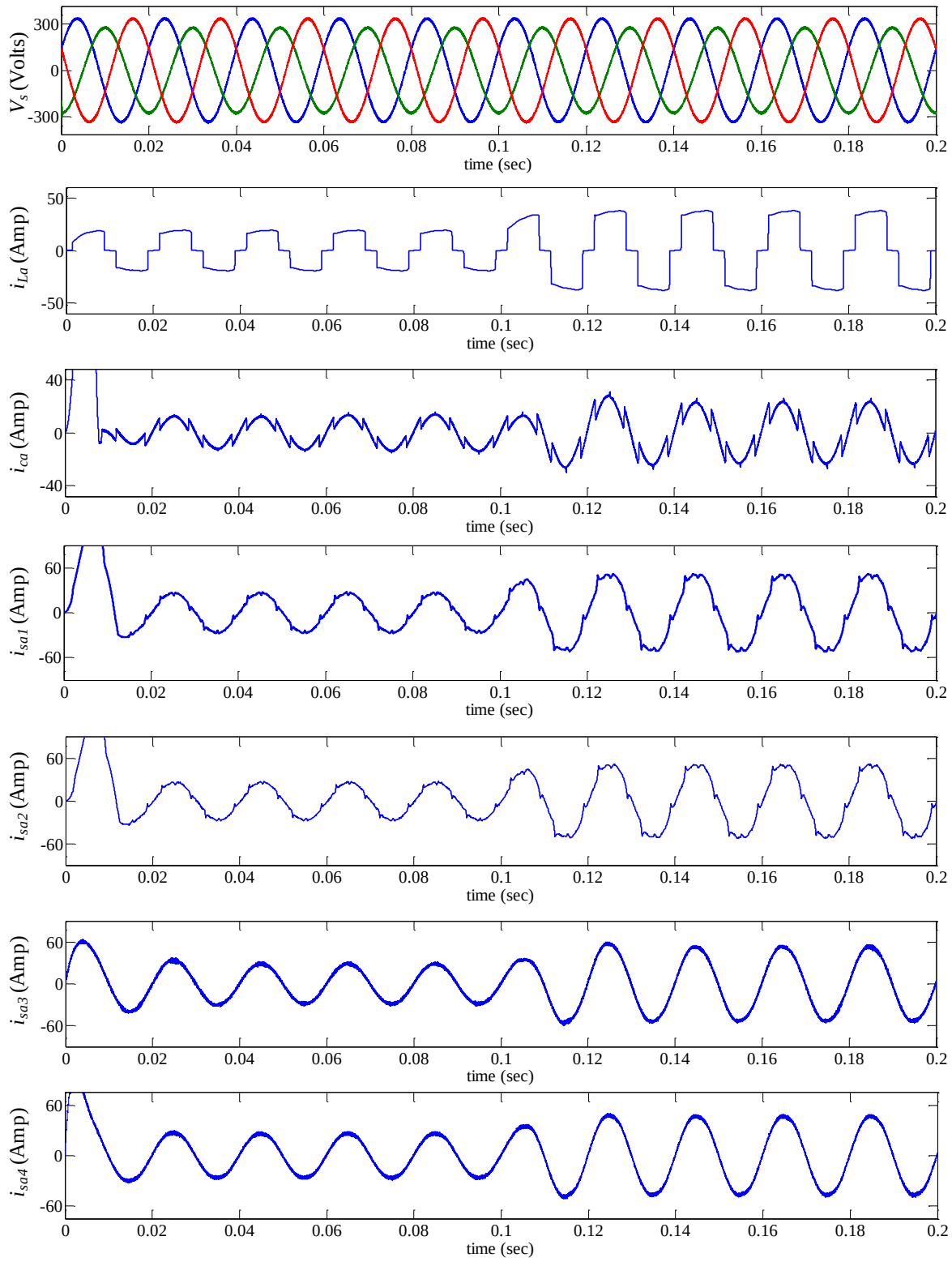
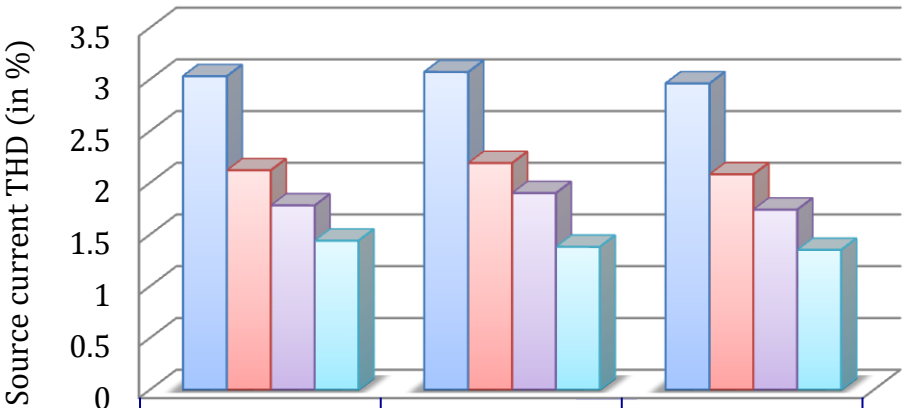
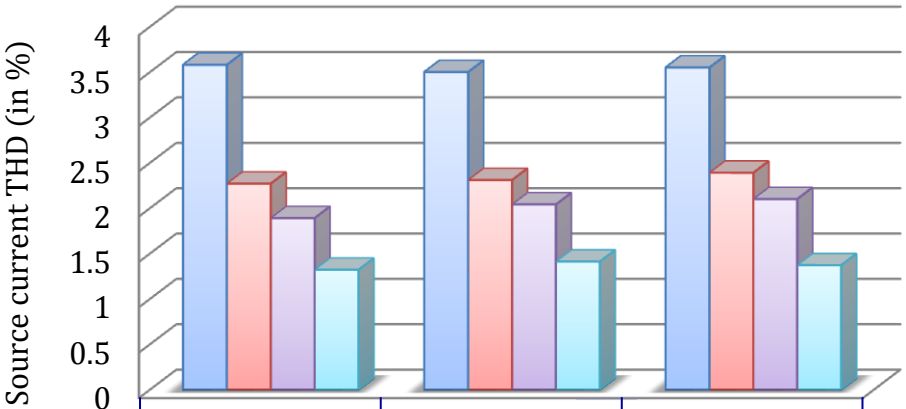


Figure 3.13: Simulation waveforms for supply voltage (V_s), load current in phase-a (i_{La}), compensation current in phase-a (i_{ca}), and source currents in phase-a for APF employing conventional PI (i_{sa1}), PSO-based PI (i_{sa2}), BFO-based PI (i_{sa3}) and Enhanced BFO-based PI (i_{sa4}) under unbalanced supply



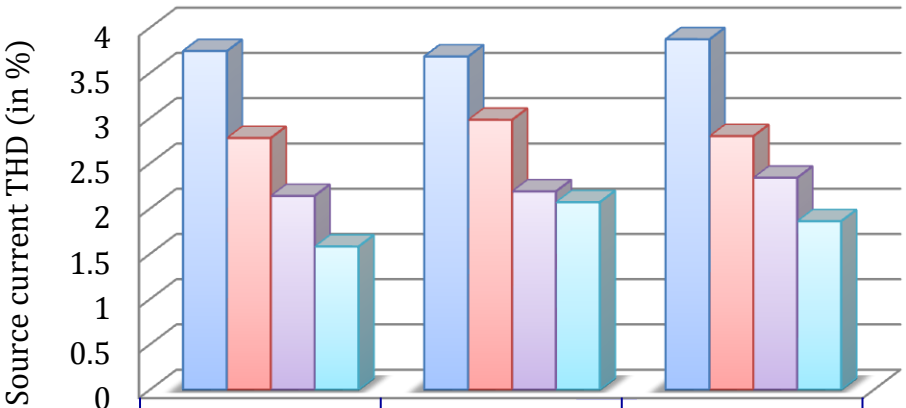
	Phase - a	Phase - b	Phase - c
Conventional PI	3.03	3.07	2.96
PSO-based PI	2.12	2.19	2.08
BFO-based PI	1.78	1.9	1.74
Enhanced BFO-based PI	1.44	1.38	1.35

Figure 3.14: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers under ideal supply condition



	Phase - a	Phase - b	Phase - c
Conventional PI	3.58	3.5	3.55
PSO-based PI	2.27	2.31	2.39
BFO-based PI	1.89	2.04	2.1
Enhanced BFO-based PI	1.32	1.41	1.37

Figure 3.15: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers under distorted supply condition



	Phase - a	Phase - b	Phase - c
Conventional PI	3.74	3.68	3.87
PSO-based PI	2.78	2.98	2.8
BFO-based PI	2.14	2.19	2.34
Enhanced BFO-based PI	1.58	2.07	1.86

Figure 3.16: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers under unbalanced supply condition

3.5.2. RT-Lab results

Comparison between the four types of aforementioned APF controllers namely, conventional, PSO-based, BFO-based and Enhanced BFO-based controllers is done in this section of the chapter with the help of RT-Lab. The real-time simulation results for ideal, distorted and unbalanced supplies are presented below, the simulation parameters and system configuration being same as that used during simulations in MATLAB, by operating both the loads at a time. The supply voltage, load current in phase-a, compensation filter current in phase-a, DC-link voltage, and source currents in phase-a for conventional, PSO-based, BFO-based and Enhanced BFO-based APFs under ideal supply are shown in Figure 3.17. Similarly, Figures 3.18 and 3.19 present the respective RT-Lab results under distorted and unbalanced supply conditions. The THDs in phase-a of load current are found out to be 32.68%, 33.24% and 29.97% under ideal, distorted and unbalanced supplies respectively.

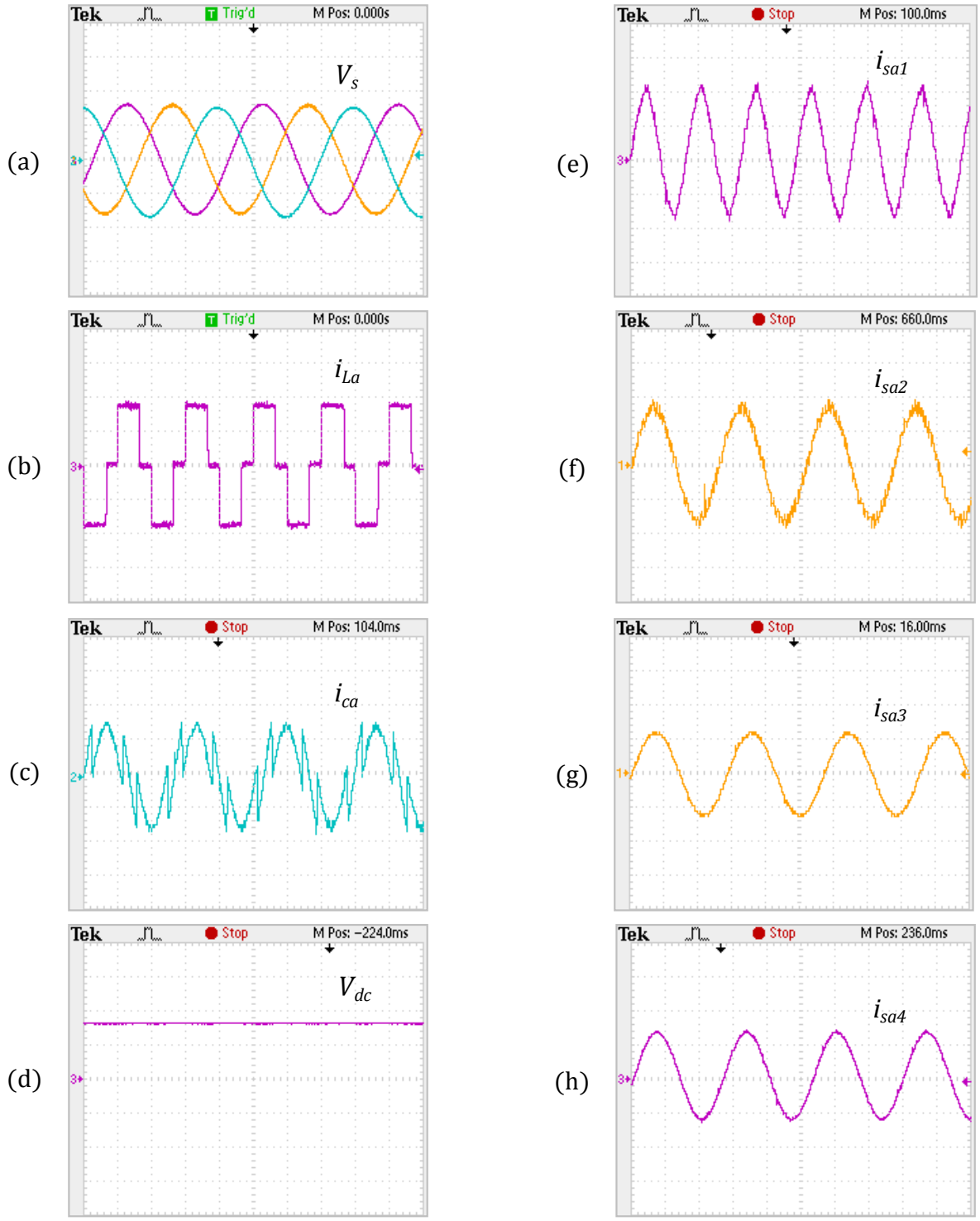


Figure 3.17: RT-Lab results for **(a)** Supply voltage (V_s) [scale: 200 V/div], **(b)** Load current in phase-a (i_{La}) [scale: 25 A/div], **(c)** Compensation filter current in phase-a (i_{ca}) [scale: 25 A/div], **(d)** DC-link voltage (V_{dc}) [scale: 500 V/div], **(e) - (h)** Source current in phase-a for APF employing conventional PI (i_{sa1}) [scale: 25 A/div], PSO-PI (i_{sa2}) [scale: 30 A/div], BFO-PI (i_{sa3}) [scale: 50 A/div] and Enhanced BFO-PI (i_{sa4}) [scale: 40 A/div] under ideal supply

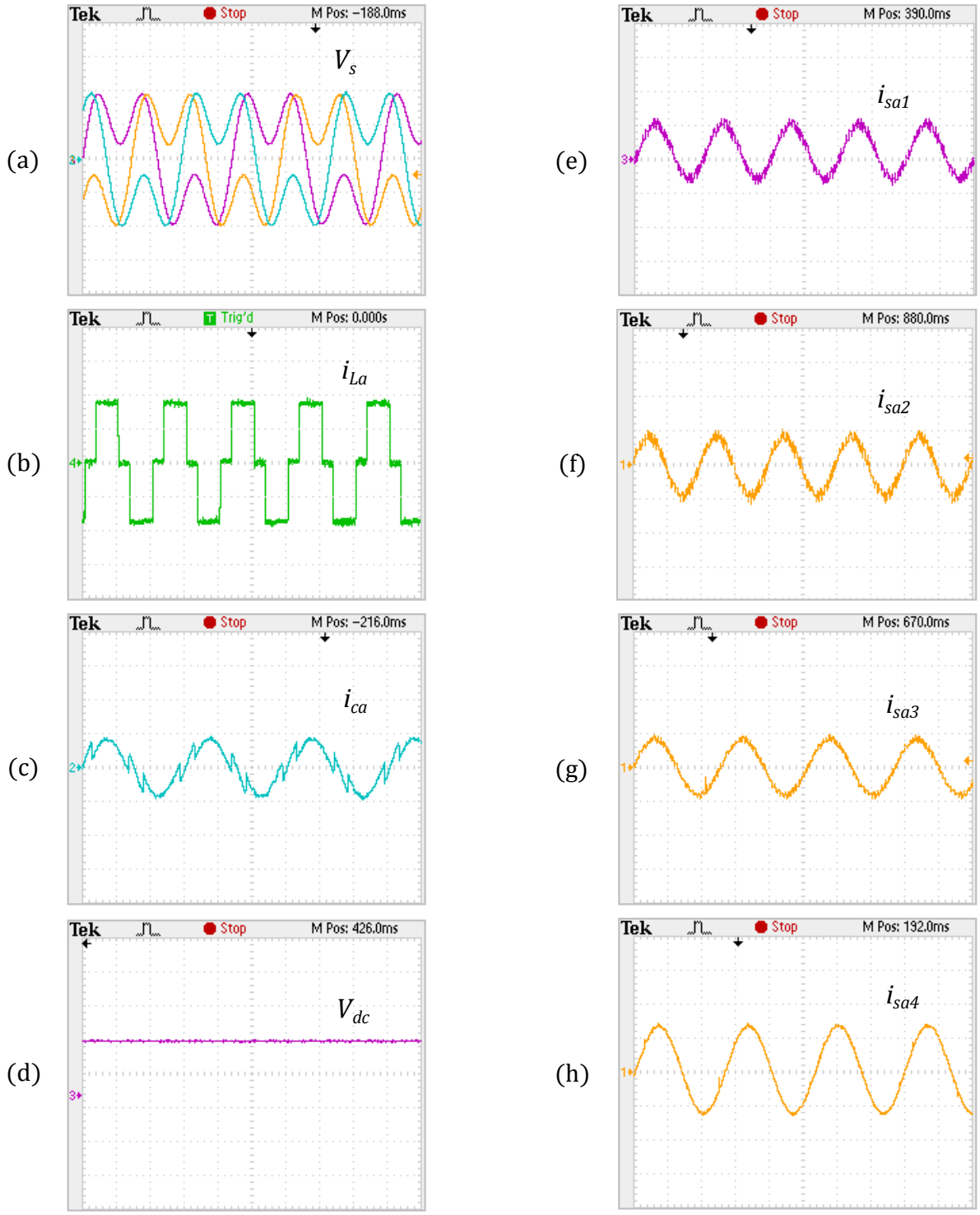


Figure 3.18: RT-Lab results for **(a)** Supply voltage (V_s) [scale: 200 V/div], **(b)** Load current in phase-a (i_{La}) [scale: 25 A/div], **(c)** Compensation filter current in phase-a (i_{ca}) [scale: 40 A/div], **(d)** DC-link voltage (V_{dc}) [scale: 500 V/div], **(e) - (h)** Source current in phase-a for APF employing conventional PI (i_{sa1}) [scale: 50 A/div], PSO-PI (i_{sa2}) [scale: 70 A/div], BFO-PI (i_{sa3}) [scale: 60 A/div] and Enhanced BFO-PI (i_{sa4}) [scale: 40 A/div] under distorted supply

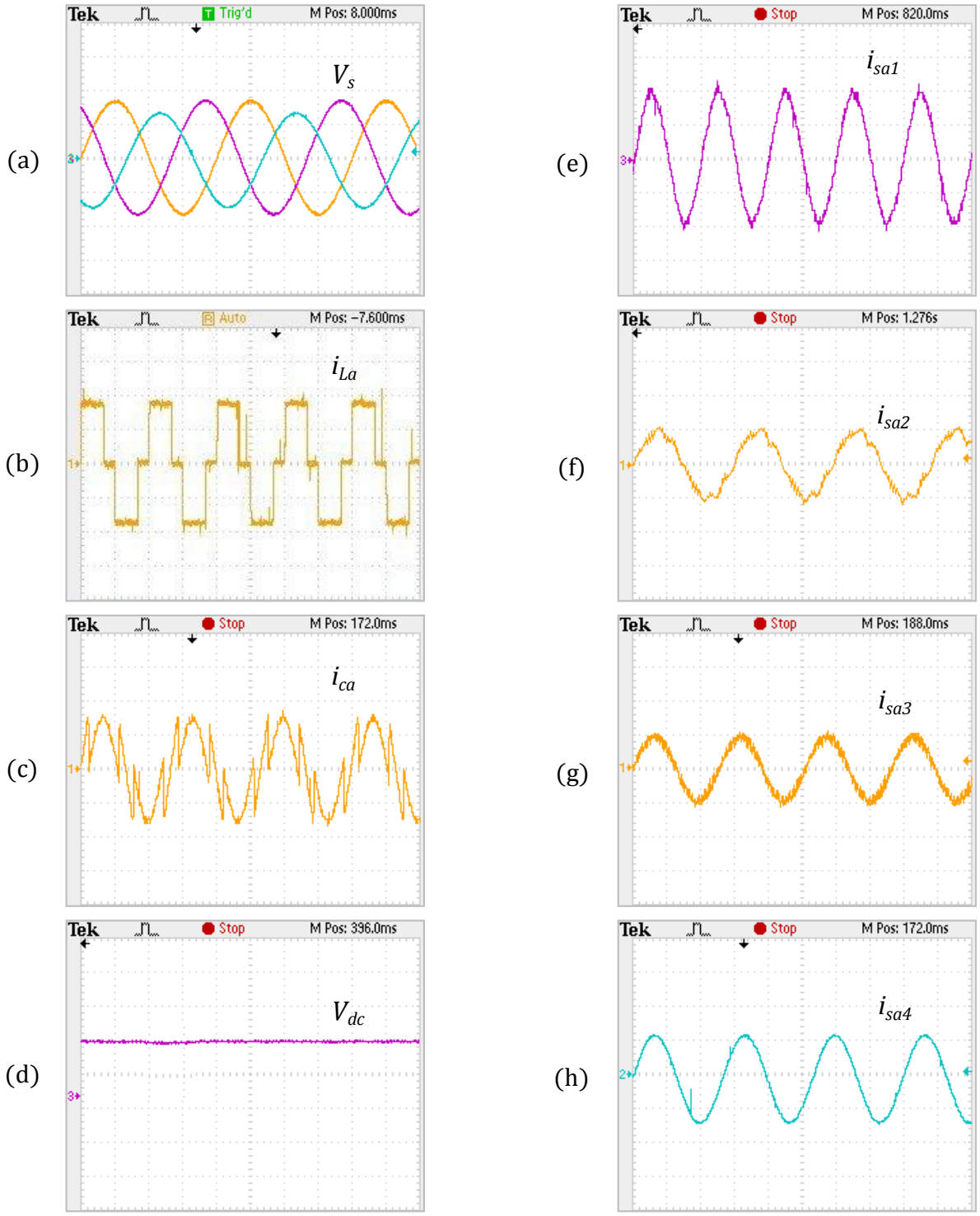
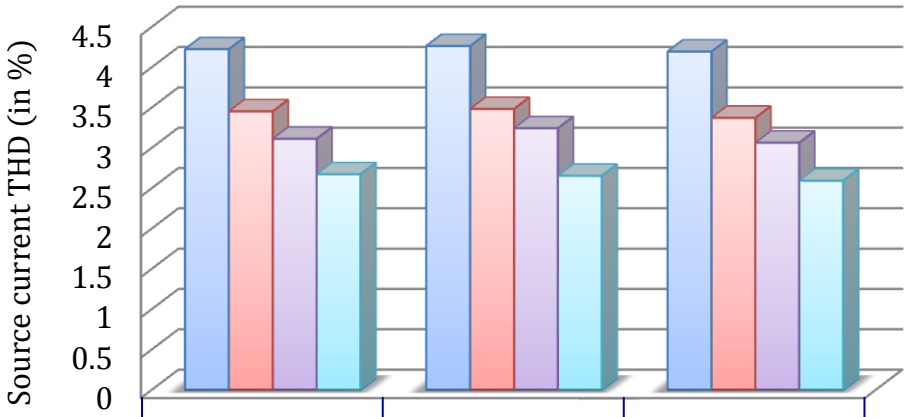


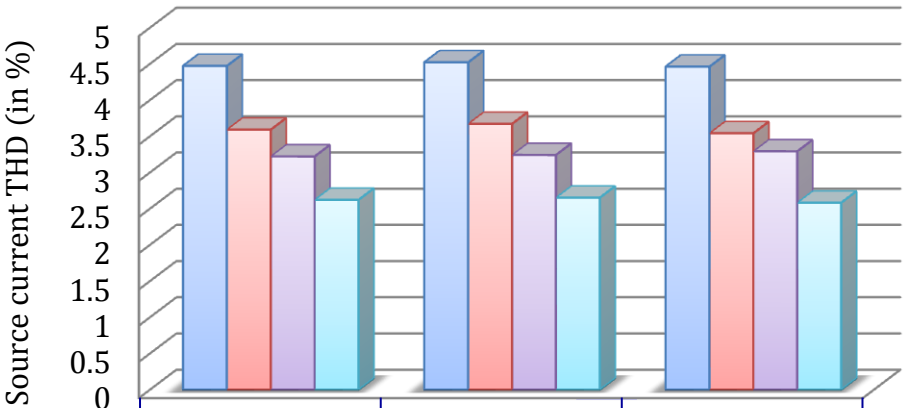
Figure 3.19: RT-Lab results for **(a)** Supply voltage (V_s) [scale: 200 V/div], **(b)** Load current in phase-a (i_{La}) [scale: 25 A/div], **(c)** Compensation filter current in phase-a (i_{ca}) [scale: 25 A/div], **(d)** DC-link voltage (V_{dc}) [scale: 500 V/div], **(e) - (h)** Source current in phase-a for APF employing conventional PI (i_{sa1}) [scale: 25 A/div], PSO-PI (i_{sa2}) [scale: 60 A/div], BFO-PI (i_{sa3}) [scale: 60 A/div] and Enhanced BFO-PI (i_{sa4}) [scale: 50 A/div] under unbalanced supply

The THDs of source current after compensation act as the indicator for comparative effectiveness of APFs employing discussed optimization techniques in current harmonic compensation. Source current THDs in a, b and c phases are clearly listed down in charts shown in Figures 3.20, 3.21 and 3.22 for ideal, distorted and unbalanced supply conditions respectively. These THD charts illustrate that, the source current THD values go on decreasing with the use of APF employing conventional, PSO-based, BFO-based and proposed Enhanced BFO-based PI controllers in that order. The THDs obtained after compensation with APF employing conventional PI controller and $i_d - i_q$ scheme are within the range of 4-5%. The use of optimized PI controllers (PSO-PI and BFO-PI) for active harmonic filtering yields smaller values of current THDs compared to conventional APFs as observed from the chart diagrams shown above. Ultimately, THDs have been brought down to the lowest values in the range of 2-3%, with the use of Enhanced BFO based APF under all kinds of supply. Hence, the RT-Lab real-time results further validate the simulation results.



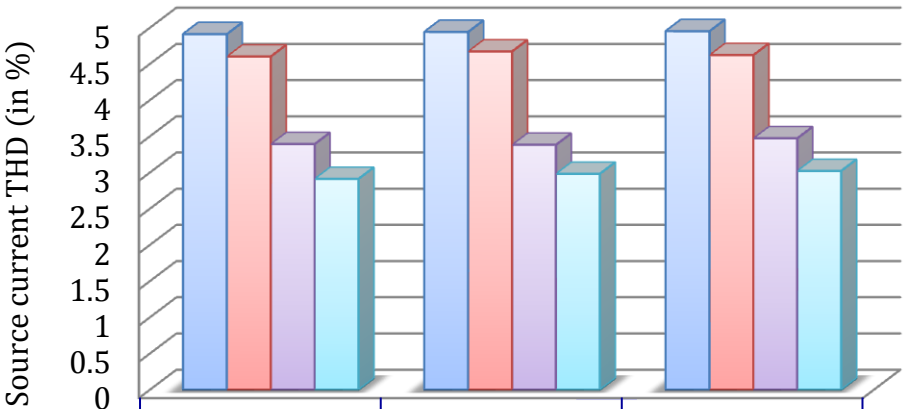
	Phase - a	Phase - b	Phase - c
Conventional PI	4.22	4.26	4.19
PSO-based PI	3.45	3.48	3.37
BFO-based PI	3.11	3.24	3.06
Enhanced BFO-based PI	2.67	2.65	2.59

Figure 3.20: Chart diagram showing source current THDs (in %) obtained in RT-Lab with APF employing conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers under ideal supply condition



	Phase - a	Phase - b	Phase - c
Conventional PI	4.47	4.52	4.46
PSO-based PI	3.59	3.67	3.54
BFO-based PI	3.22	3.24	3.29
Enhanced BFO-based PI	2.62	2.65	2.58

Figure 3.21: Chart diagram showing source current THDs (in %) obtained in RT-Lab with APF employing conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers under distorted supply condition



	Phase - a	Phase - b	Phase - c
Conventional PI	4.91	4.94	4.95
PSO-based PI	4.6	4.67	4.62
BFO-based PI	3.39	3.38	3.47
Enhanced BFO-based PI	2.91	2.98	3.02

Figure 3.22: Chart diagram showing source current THDs (in %) obtained in RT-Lab with APF employing conventional, PSO-based, BFO-based and Enhanced BFO-based PI controllers under unbalanced supply condition

3.6. Summary

The chapter proposes the implementation of typical global optimization tools PSO and BFO to solve the current harmonics problem. Optimization algorithms are utilized here to find out optimized values of PI controller gains for improved DC-link voltage regulation. The first section provides a brief introduction regarding the optimization problems and the advantages of optimization-based approaches over conventional approaches. The next section explains the PSO mechanism which follows the behaviour exhibited by bird flocks and fish schools while searching for the most food-rich location. It also describes an iterative process to develop the computational algorithm. Next section of the chapter demonstrates the mechanism of BFO and its iterative algorithm. Following this, illustrations of major disadvantages in PSO and BFO that result in performance deterioration are presented. This chapter also proposes the development of a novel optimization strategy by hybridization of PSO and BFO, which combines the advantages of both the algorithms. The implementation of this Enhanced BFO approach on a conventional VSI-based three-phase three-wire shunt APF is studied.

Various results obtained with simulation studies and RT-Lab are presented in the subsequent section, performed by employing the discussed optimization algorithms on APF. The settling times, overshoots and undershoots in V_{dc} transients are compared for conventional, PSO-based, BFO-based and Enhanced BFO-based APFs. The maximum overshoot is exceptionally small for optimization-based APFs at the starting. Moreover, the DC-link voltage settles down to its reference value in the smallest time with Enhanced BFO, followed by BFO, PSO and conventional approaches. FFT analyses indicate the THD obtained with Enhanced BFO to be the lowest, though BFO and PSO also yield lesser THDs compared to the conventional one. It shows that, Enhanced BFO gives excellent V_{dc} transient response and outperforms other alternatives in current harmonics mitigation by providing the least values of source current THDs. Hence, Enhanced BFO algorithm has an edge over the classical BFO and PSO, especially in context to the convergence behaviour of the algorithm very near to the optima. This fact has been supported here both analytically and experimentally.

Chapter 4

APF Topologies for Three-Phase Three-Wire Systems

4.1. Introduction

APFs have different configurations depending upon the type of power supply system, viz. single-phase, three-phase three-wire, and three-phase four-wire. However, the APF control schemes have identical functionality i.e., to force the PWM converter to behave as a controlled current source. There is no power supply, rather only an energy storage element (capacitor) is attached to the DC side of converter. Because, average energy transferred between the APF and power system should be zero, and APF just behaves as a compensator. Lack of neutral conductor is a distinctive feature of three-phase three-wire system. Hence, there is absence of zero-sequence current components.

As per the reasons elucidated in Sections 1.2.2 and 2.2, the two-level VSI configuration of APF has been the preferred choice for the work presented here so far. However, as the demand for medium and high voltage, high power applications is increasing, the research progress is heading towards multilevel power converters. Nabae *et al* first introduced the concept of multilevel converter in the year 1975 [110]. MLIs when used in APF instead of traditional VSI; can reduce the additional harmonics generated by the APF itself. By increasing the number of levels of MLI, the quality of output voltage waveform can be improved. As the voltage has more number of steps, hence is more close to sinusoidal [118]. This chapter aims at the investigation of an APF comprised of a transformerless MLI for power conditioning in three-phase three-wire distribution network. The use of

conventional VSI is already discussed in detail in previous chapter. Therefore, this chapter is merely confined to multilevel VSI configurations.

There are basically three variants of MLI topologies viz. neutral-point clamped inverter, flying-capacitor inverter and cascaded H-bridge inverter. All these configurations are discussed in depth in the following section. The utilization of several optimization approaches in MLIs is reported so far in literature, most of which deal with harmonic minimization in cascaded MLIs. In the year 2005, a paper on harmonic optimization of cascaded 7-level converter was published that used Genetic Algorithm (GA) to find out optimized switching angles [125]. This helps the MLI to achieve lesser THD in output voltage, by eliminating specific lower order dominant harmonics, without affecting the fundamental voltage. This method of PWM involving suppression of specific lower order harmonics is known as selective harmonic elimination (SHE). Subsequently, identical applications of PSO on cascaded MLIs have been presented in References [126]–[129]. An implementation of Bee algorithm on SHE-PWM is also demonstrated in [130]. Nevertheless, not many papers concentrate on the optimal regulation of DC-link capacitor voltage of MLIs. Despite considerable progress in advanced controllers, the researchers and application engineers still prefer to employ the classical PI controller [131]. This chapter proposes the implementation of Enhanced BFO discussed in Chapter 3 to extract the optimized gains of PI controller, for optimum regulation of DC-link voltage of MLI. Here, the inverter topologies under study are 3, 5, 7 and 9-level cascaded MLIs. Hence, the objective of this chapter is to illustrate the combined advantages of using MLIs and Enhanced BFO-based PI controller in APFs. Adequate simulation results are presented. Additionally, the performance is validated in real-time using RT-Lab. The proposed work provides simple and effective DC-link voltage regulation, quick prevail over current harmonics and reduces overall source current THD.

The rest of the chapter is organized under following headings. The next section discusses MLI topologies and PWM schemes. Section 4.3 illustrates the shunt APF system configuration with cascaded MLI. It also describes the improved regulation of DC-link capacitor voltage in MLI using Enhanced BFO-based PI controller. Investigations are

carried out under identical test environments for ideal, distorted and unbalanced supply conditions. Results obtained from simulations and real-time performance analyses in RT-Lab are presented in Section 4.4. Finally, summary of the chapter is given in Section 4.5.

4.2. Multilevel Inverter (MLI)

The elementary concept of a typical multilevel converter is to synthesize a sinusoidal voltage waveform from a number of levels of voltages. Generally, a staircase voltage waveform can be generated by either of the following means:

a) Using traditional magnetic coupled multi-pulse converters and varying transformer turns ratio with zigzag connections
b) Using multilevel converters and capacitor voltage synthesis method

The former has some severe drawbacks associated with it, as it is bulky, heavy, lossy and involves complicated zigzag transformer connections. Therefore, capacitor voltage synthesis method is the preferred alternative amongst the two.

The output voltage waveform of a MLI approaches closer to sinusoidal with an increase in the number of voltage levels. The semiconductor devices connected in series help to withstand higher voltages without device voltage sharing problems. However, few constraints such as voltage unbalance, voltage clamping requirements, circuit layout and packaging constraints limit the number of attainable voltage levels. A major disadvantage associated with multilevel converters is requirement of more number of power semiconductor switches, each of which need a related gate drive circuit. This may cause the overall system to be more expensive and complex. Nevertheless, advantages offered by MLIs over conventional two-level VSIs predominantly take over the disadvantages mentioned above. Higher voltages can be generated with low harmonic content and lower (dv / dt) distortion; therefore electromagnetic compatibility problems can be reduced. Two-level inverters have the disadvantages like high-order harmonic noise and additional switching losses due to high-frequency commutation. MLIs draw input current with very low distortion. There is a considerable reduction in size and volume, as no

bulky coupling transformers or inductors are required. There is reduction in voltage/current ratings of semiconductor switches and switching frequency requirements, resulting in reduced switching power loss.

4.2.1. Types of MLI

MLIs are basically categorized into three types depending upon the topologies and their principle behind generation of multilevel output voltages [99]. The multilevel inverter configurations are namely, (a) Diode-clamped (Neutral-point clamped) inverter, (b) Capacitor-clamped (Flying-capacitor) inverter and (c) Cascaded H-bridge inverter.

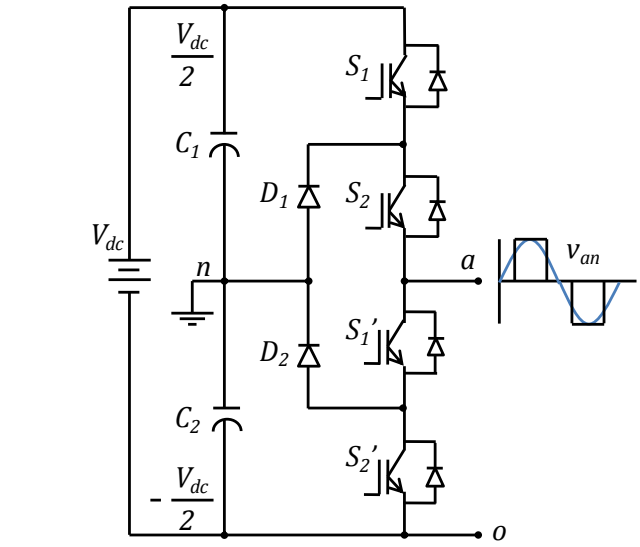
4.2.1.1. Diode-clamped (Neutral-point clamped) inverter

It is composed of main switching devices operating as switches for PWM and auxiliary diodes to clamp the output terminal potential to the neutral point potential. The 3-level and 5-level diode-clamped inverter configurations are depicted in Figure 4.1.

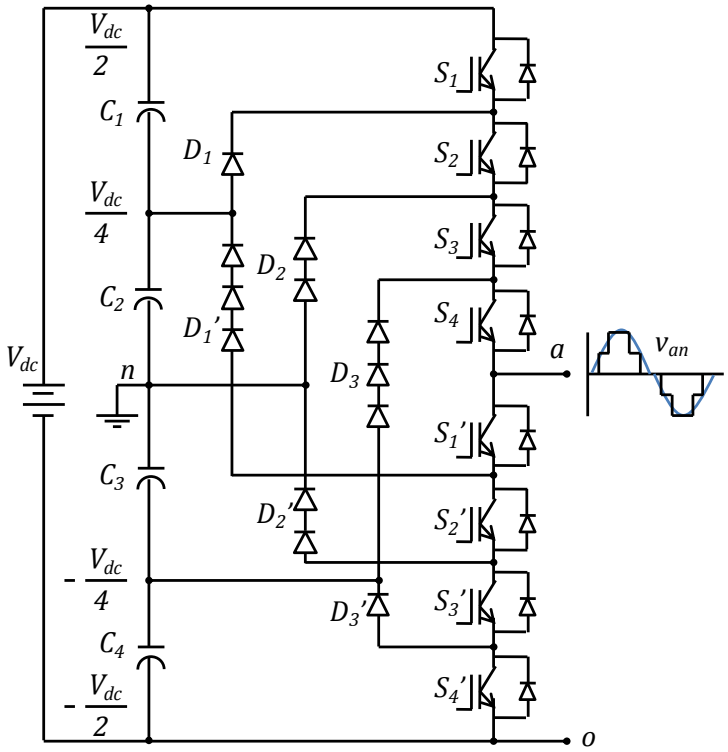
It can be seen from Figure 4.1 (a) that, the leg A of inverter consists of four switches (S_1, S_2, S_3 and S_4) and four diodes connected in anti-parallel across the switches. On the DC-side of the inverter are the DC-bus capacitors C_1 and C_2, that provide a neutral point n. The voltage across each of the capacitors is $\frac{V_{dc}}{2}$. The capacitors along with clamping diodes (D_1 and D_2) are used to divide the DC voltage V_{dc} into three output voltage levels, $+\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$ as per different switching combinations described below.

a) When the upper two switches S_1 and S_2 of leg A conduct, the inverter output phase-to-neutral voltage for phase A (v_{an}) is $+\frac{V_{dc}}{2}$.
b) Likewise, when lower two switches S_3 and S_4 are on, the output voltage is $-\frac{V_{dc}}{2}$.
c) Voltage $v_{an} = 0$ is achieved via clamping diodes, when S_2 and S_3 are switched on.

Switches S_1 and S_3 represent complementary pair of switches, so does the pair consisting of S_2 and S_4. The inverter output phase voltages for three-phases (v_{an}, v_{bn}, v_{cn}) are identical and phase-shifted from each other by $\frac{2\pi}{3}$.



(a)



(b)

Figure 4.1: Configurations for one phase (phase-a) of diode-clamped inverter of (a) Level 3, (b) Level 5

The line-to-line voltage is obtained as, $v_{ab} = v_{an} - v_{bn}$, which contains five voltage levels $\left(+V_{dc}, +\frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2}, -V_{dc}\right)$.

Similarly, other two line voltages are given by, $v_{bc} = v_{bn} - v_{cn}$ and $v_{ca} = v_{cn} - v_{an}$.

Likewise, a 5-level output phase voltage can be generated using the inverter configuration shown in Figure 4.1 (b). An m-level diode-clamped inverter has 'm' number of levels in output phase voltage and $(2m - 1)$ levels in its output line voltage.

Advantages of this type of MLIs are:

a) No dynamic voltage sharing problem, as each switch is subjected to a small voltage during commutation
b) Less capacitance requirements, as a common DC-bus is shared between all phases
c) Capacitors can be pre-charged in a group
d) Efficient for fundamental switching frequency operations

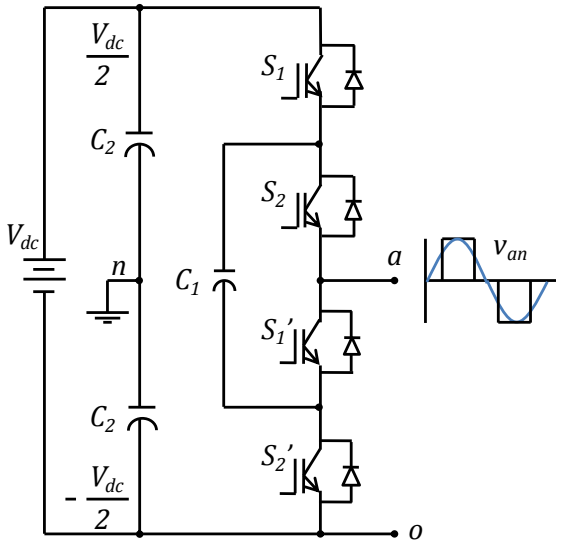
Disadvantages of this MLI include:

a) Requirement of additional clamping diodes
b) Possible deviation of neutral point voltage
c) PWM switching pattern generation is complicated

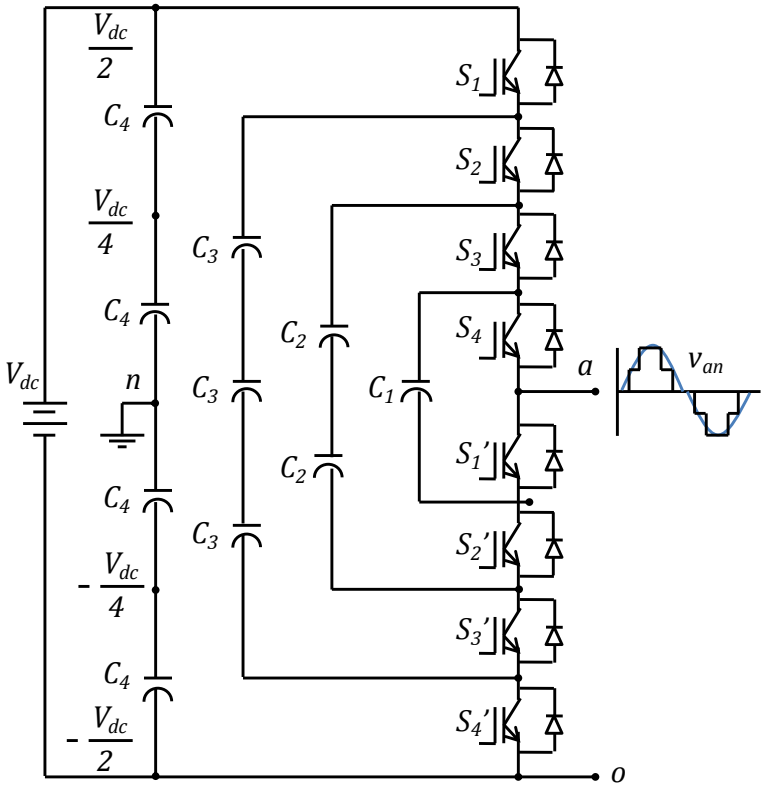
Diode-clamped inverters have been reported to serve in several areas of application and research according to the literature. It can be used for interfacing between a high-voltage DC transmission line and an AC transmission line [99]. Besides, its application as variable speed drive in high-power medium-voltage (2.4–13.8 kV) motors is also very popular [96], [99], [111], [132], [133]. Applications of the MLI in photovoltaic systems and direct-driven wind energy conversion system are portrayed in literature [134], [135]. Moreover, this MLI is also capable of serving as Static var compensator [31].

4.2.1.2. Capacitor-clamped (Flying-capacitor) inverter

Its structure is similar to diode-clamped MLI except the point that, it uses capacitors in place of clamping diodes. Circuit topologies for 3-level and 5-level flying-capacitor MLIs are illustrated in Figure 4.2. It has a ladder structure of DC-side capacitors, where the voltage on each capacitor differs from that of the next capacitor. Size of the voltage steps in output waveform is a result of voltage increment between two adjacent capacitor legs.



(a)



(b)

Figure 4.2: Configurations for one phase (phase-a) of capacitor-clamped MLI of (a) Level 3, (b) Level 5

Inverter configuration shown in Figure 4.2 (a) can generate three levels of voltage output.

a) Positive voltage level $+\frac{V_{dc}}{2}$, when switches S_1 and S_2 are turned on.

b) Voltage level of $-\frac{V_{dc}}{2}$, when switches $S_1^{'}$ and $S_2^{'}$ are turned on.

c) Whereas, switching on of pairs $(S_1, S_1^{'})$ or $(S_2, S_2^{'})$ result in zero voltage.

Clamping capacitor C_1 is charged when the switches S_1 and S_2 conduct, and discharges when the other two switches conduct. Conversely, the reverse applies to capacitor C_2.

The inverter configuration of Figure 4.2 (b) can generate a 5-level output phase voltage waveform. Typically $\frac{(m-1)(m-2)}{2}$ numbers of clamping capacitors and $(m-1)$ DC-link capacitors are required for a single phase leg of a flying-capacitor MLI, in order to generate a phase voltage of 'm' levels and line-to-line voltage of $(2m-1)$ levels. All the capacitors should be of same voltage rating as that of the main power switch.

Advantages of capacitor-clamped MLI include:

a) Phase redundancies are available for balancing the voltage levels of capacitors

b) Real and reactive power flow can be controlled

c) The use of large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags

Following are the disadvantages associated with this MLI:

a) Control is complicated to track the voltage levels for all of the capacitors. Also, pre-charging all of the capacitors to the same voltage level and startup are complex

b) Switching utilization and efficiency are poor for real power transmission

c) Large number of capacitors makes this MLI expensive and bulky, compared to clamping diodes in diode-clamped MLI

d) Packaging also becomes more difficult in inverters with higher number of output voltage levels

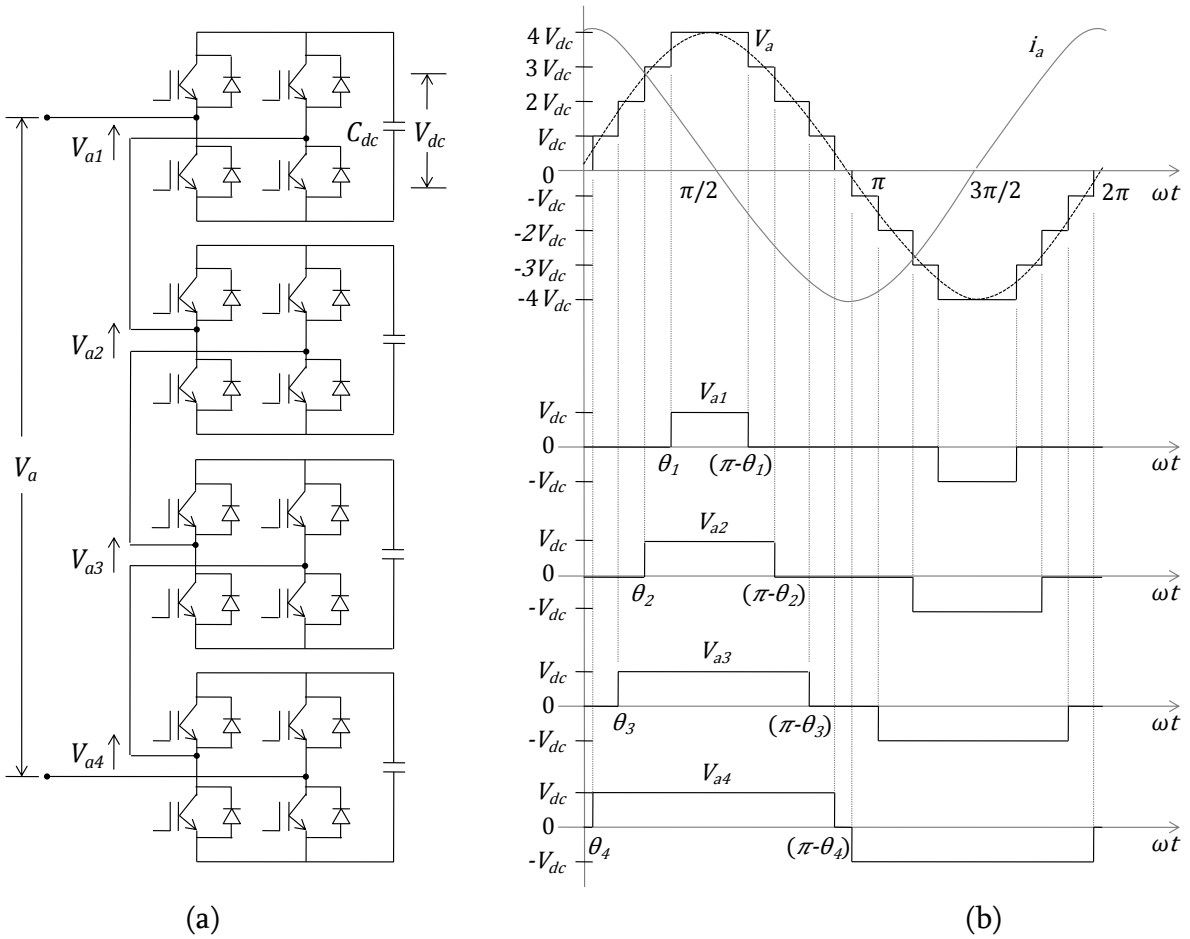
The flying-capacitor type of MLI offers its application in static var generation [96], [99]. Its application in power-line conditioning has been discussed in various literatures [136]–[139] with the MLI acting as shunt APF, series APF or Unified power quality conditioner (UPQC). A flying-capacitor MLI based Dynamic voltage restorer (DVR) has also been proposed to overcome various power quality issues such as voltage harmonics, sag, voltage unbalance etc. simultaneously [140]. This MLI is also well suited to motor drives that are

directly connected to high-to-medium voltage utility power systems and for adjustable speed drives in industries [141], [142].

4.2.1.3. Cascaded inverter

Unlike diode-clamped and capacitor-clamped topologies, the cascaded inverter structure does not require additional clamping diodes or voltage balancing capacitors. Figure 4.3 (a) shows the basic configuration of cascaded MLI with capacitors acting as DC sources. Each DC-link capacitor is connected to a single-phase H-bridge inverter. A cascaded m-level inverter consists of $\frac{(m-1)}{2}$ number of H-bridges.

Each H-bridge generates a quasi-square voltage waveform with three-level outputs: $+V_{dc}$, 0 and $-V_{dc}$.



(a) (b)

Figure 4.3: (a) Circuit diagram, (b) Output phase voltage waveform for one phase (phase-a) of a cascaded H-bridge 9-level inverter

These voltages sum up to produce the phase voltage, since AC terminal voltages of different levels $(V_{a1}, V_{a2}, \ldots V_{a[(m-1)/2-1]}, V_{a[(m-1)/2]})$ are connected in series.

The phase output voltage (V_a) can be given as,

$$V_a = V_{a1} + V_{a2} + \cdots + V_{a[(m-1)/2-1]} + V_{a[(m-1)/2]} \quad (4.1)$$

The phase voltage waveform for one phase of a 9-level cascaded inverter is presented in Figure 4.3 (b).

Table 4.1 provides a comparison of component requirements for m-level diode-clamped, capacitor-clamped and cascaded MLI topologies. This shows that, number of main switching devices and main diodes required in all three MLI configurations is exactly same. However, no clamping diodes or balancing capacitors are required for cascaded configuration. Furthermore, the number of DC-bus capacitors required in case of cascaded topology is the lowest compared to the other two.

Table 4.1: Comparison of component requirements for MLI topologies

Feature	Diode-clamped	Capacitor-clamped	Cascaded
Main switching	$2(m-1)$	$2(m-1)$	$2(m-1)$
Main diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
Balancing capacitors	0	$\frac{(m-1)(m-2)}{2}$	0
DC-bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$

The cascaded MLI is preferred to be implemented in this work due to following reasons:

a) Number of possible output voltage levels is more than twice the number of DC sources
b) Component requirement in cascaded MLI is less compared to the other two MLIs
c) Modularized layout and packaging of series H-bridges makes the manufacturing process quick and cheap

Though several topologies of cascaded MLI make use of transformers, a transformerless MLI has been preferred here because of the several drawbacks encountered in the former such as, (a) expensiveness, (b) increased power loss, (c) bulky nature and (d) proneness to failure.

The cascaded MLI was first introduced for motor drive applications [143] and was later used for reactive and harmonic compensation [144]. Further work has been reported on universal power conditioning of power systems, especially for medium-voltage systems [98], [145]. This inverter is of lower cost, and provides higher performance, less electromagnetic interference (EMI), and higher efficiency than the conventional inverters for power line conditioning applications, both series and shunt compensation [95]. The cascaded inverter has inherent self-balancing characteristics. However, because of the circuit component losses and limited controller resolution, a slight voltage imbalance can occur. The MLI technology has also been applied to traction systems. An application of a back-to-back cascaded topology of MLI on electric vehicles is reported in the paper [146]. Nearly every energy industry such as chemical, oil, liquefied natural gas, geothermal, nuclear power, water plants, thermal management/cooling systems, boilers furnaces etc. extensively use high-voltage high-power fans and pumps [100], [147]. Generally, in such applications cascaded MLI is the choice for variable speed drives. Another application of cascaded MLI is observed in Naval ship propulsion drives as presented in References [148], [149].

4.2.2. PWM schemes for Cascaded MLI

As the MLIs can be operated at both fundamental and high switching frequencies, their modulation schemes can be broadly divided into two types based on switching frequency. Figure 4.4 shows the classification of various PWM schemes for MLIs. Fundamental frequency switching type PWM schemes involve one or two commutations of power semiconductor switching devices in one cycle of fundamental output voltage. However, the other type of PWM requires many commutations per cycle of output voltage.

Fundamental switching frequency type of modulation includes Space vector modulation and Selective harmonic elimination (SHE). However, carrier-based PWM belong to high switching frequency modulation type.

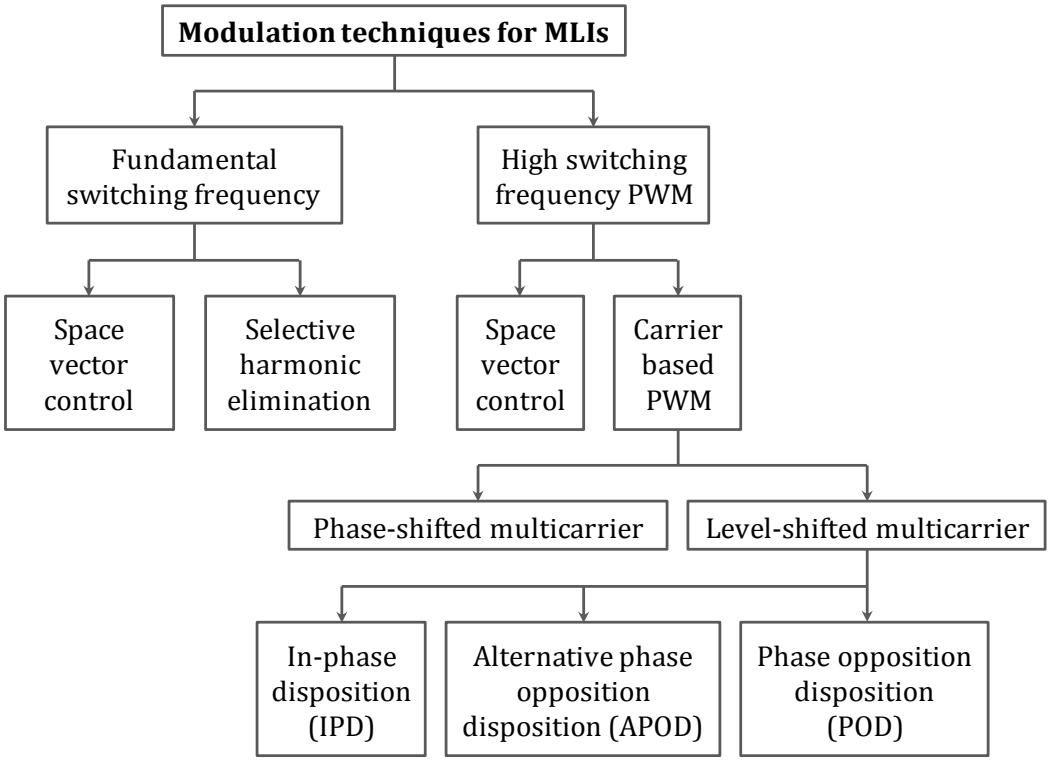


Figure 4.4: Classification of modulation strategies for MLI

4.2.2.1. Space vector modulation (SVM)

Space vector modulation is a commonly used PWM technique in conventional two-level power converters [150]–[154]. The SVM for MLIs is an extended version of the two-level SVM [155], [156]. In SVM, the voltage signal is transformed into $\alpha - \beta$ coordinates, which can be represented in the form of space vectors, provided the impedances and total power are kept unchanged. According to the switching positions of a two-level inverter, there can be eight switching states and six sectors. The state matrix becomes more and more complex with increase in the level of output voltage for multilevel inverter. This consequently results in high computational burden while generating the switching pulses. Therefore, the application of SVM is restricted to only lower level MLIs (five or fewer levels) [157].

4.2.2.2. Selective harmonic elimination (SHE)

Consider a MLI with 's' number of steps in the output voltage such that, $s = \frac{(m-1)}{2}$. The Fourier series expansion of the stepped waveform is as follows,

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)] \times \frac{\sin(n\omega t)}{n} \qquad (4.2)$$

Here, $n = 1, 3, 5 \ldots$ i.e., it represents odd harmonic orders such as 1st, 3rd, 5th etc. $\theta_1, \theta_2, \ldots, \theta_s$ are the switching angles of 's' individual H-bridges of cascaded MLI as shown in Figure 4.5 such that, $0 < \theta_1 < \theta_2 < \theta_s < \frac{\pi}{2}$.

The magnitudes of Fourier coefficients when normalized with respect to V_{dc} are given by,

$$H(n) = \frac{4}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)] \qquad (4.3)$$

The angles $\theta_1, \theta_2, \ldots, \theta_s$ are to be set to such values that it minimizes the THD of synthesized output voltage. The condition is that, it must result in a voltage, $V(\omega t) = V_1 \sin(\omega t)$, where V_1 is the desired fundamental voltage. The switching angles are so chosen that, the dominant lower harmonic orders are eliminated. Number of harmonics that can be eliminated with SHE-PWM for a cascaded m-level MLI having 's' number of separate DC sources is $(s-1)$. Consider a cascaded 11-level MLI consisting of five DC sources. For eliminating dominant orders of harmonics such as 5th, 7th, 11th and 13th, the mathematical conditions of (4.2) can now be reduced to following set of equations.

$$\frac{4V_{dc}}{\pi}[\cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4] = V_1$$

$$\cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 + \cos 5\theta_4 = 0$$

$$\cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 + \cos 7\theta_4 = 0$$

$$\cos 11\theta_1 + \cos 11\theta_2 + \cos 11\theta_3 + \cos 11\theta_4 = 0$$

$$\cos 13\theta_1 + \cos 13\theta_2 + \cos 13\theta_3 + \cos 13\theta_4 = 0 \qquad (4.4)$$

These nonlinear equations can be solved using Newton-Raphson method, Resultant theory or Genetic algorithm [100], [158], [159]. After the elimination of lower frequency harmonics, the higher order harmonic components can be easily filtered out from the output voltage of MLI. This PWM strategy involves an optimizing algorithm, as it

minimizes the THD of MLI output voltage, with optimized values of switching angles. Hence, the synthesized voltage in case of SHE-PWM is better compared to other PWM techniques. The major drawbacks associated with this PWM are involvement of extensive mathematical computations and large memory requirement.

4.2.2.3. Carrier-based PWM

The carrier-based modulation schemes for cascaded MLIs can be basically of two types, namely, (a) Phase-shifted and (b) Level-shifted.

(a) Phase-shifted multicarrier modulation

In phase-shifted modulation of MLI, $(m-1)$ numbers of carriers are required to generate an m-level output voltage. Carrier signals are triangular in nature having same amplitude and frequency; and are phase-shifted from each other by an angle (φ_{cr}) given by,

$$\varphi_{cr} = \frac{360^{\circ}}{(m-1)} \tag{4.5}$$

The modulating/reference signal is generally sinusoidal in nature. For a 3-phase inverter, the modulating signals are three-phase sinusoidal signals having adjustable magnitude and frequency. All the carrier signals are compared with the reference signal of each phase so as to produce the required gate signals for corresponding phase leg of the inverter.

The arrangement of carrier and reference waves for a 5-level inverter with phase-shifted PWM is illustrated in Figure 4.5. In the Figure, v_{cr1}, v_{cr2}, v_{cr3} and v_{cr4} represent the four carrier signals required to produce a 5-level output, whereas v_{ref} signifies the reference.

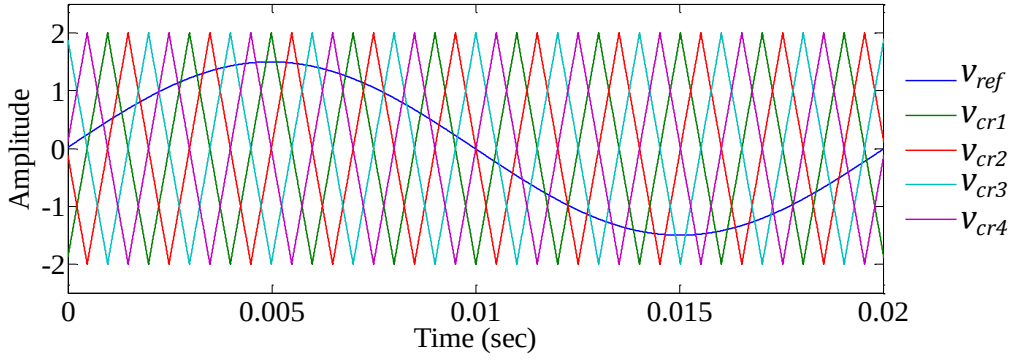
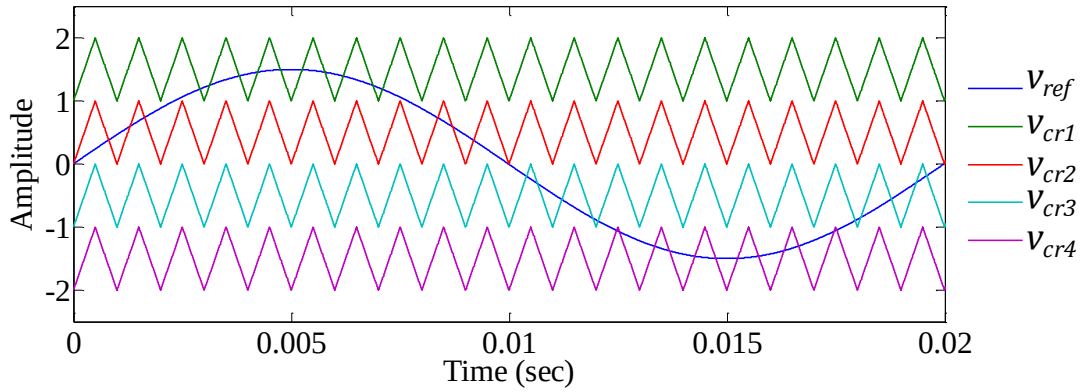


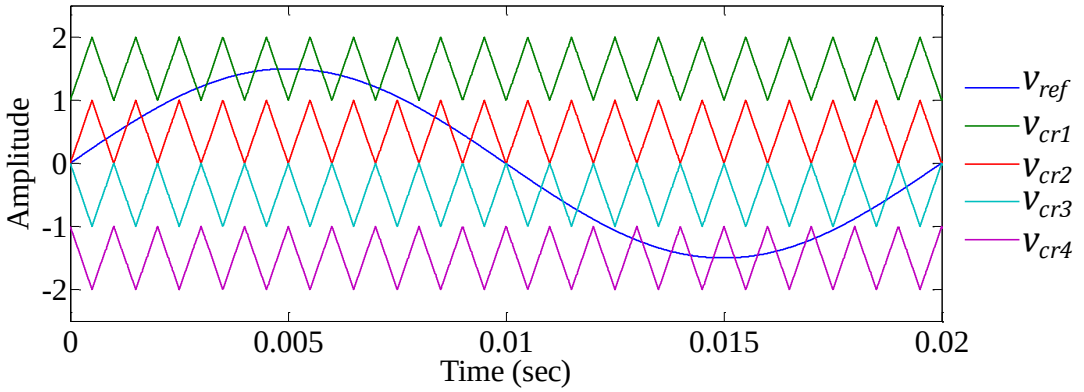
Figure 4.5: Phase-shifted multicarrier PWM for a 5-level cascaded MLI

(b) Level-shifted multicarrier modulation

Level-shifted modulation also requires $(m-1)$ number of carrier signals to generate m-levels of output voltage. Here the triangular carrier signals are equal in amplitude and frequency similar to phase-shifted modulation. However, the carriers are vertically disposed with respect to each other so that they occupy adjacent bands.



(a)



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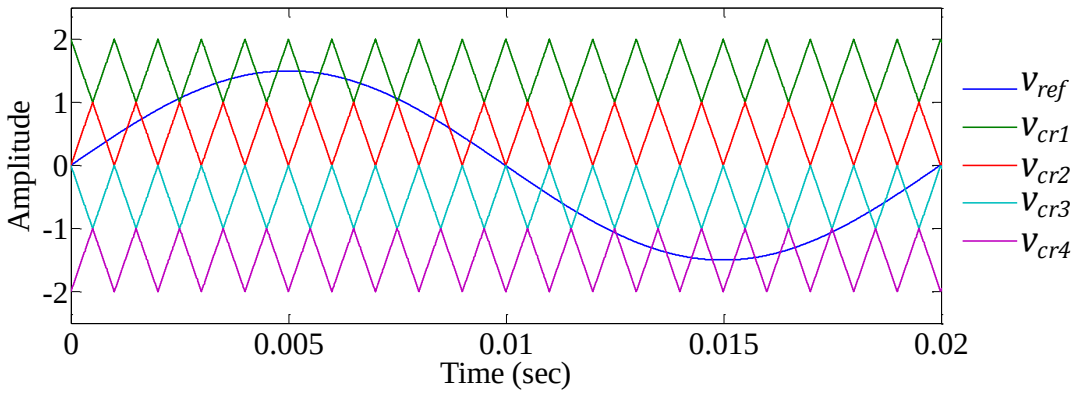


(c)

Figure 4.6: Level-shifted PWM for 5-level cascaded MLI, (a) IPD, (b) POD, (c) APOD

Level-shifted modulation can be divided as follows depending upon the nature of carriers.

i) *In-phase disposition (IPD):* where all carriers are in phase
ii) *Phase opposite disposition (POD):* where all carriers above the zero reference are in phase but in opposition with those below the zero reference
iii) *Alternative phase opposite disposition (APOD):* where all carriers are alternatively in opposite disposition

A 5-level MLI requires four number of carrier signals. The arrangements of carriers for IPD, POD and APOD level-shifted PWM for a 5-level cascaded MLI are illustrated in Figure 4.6 for one cycle of supply frequency (50 Hz). Here, v_{ref} represent the sinusoidal reference or modulating signal, whereas, v_{cr1}, v_{cr2}, v_{cr3} and v_{cr4} represent the triangular carrier signals.

Comparison between phase-shifted and level-shifted modulations:

(i) Modulation indices

The frequency modulation index (m_f) for both phase-shifted and level-shifted modulations can be given by (4.6), where f_c and f_m indicate the frequencies of carrier and modulating signals respectively.

$$m_f = \frac{f_c}{f_m} \tag{4.6}$$

The amplitude modulation index (m_a) for phase-shifted modulation is defined by (4.7), where A_m and A_c are the peak amplitudes of modulating and carrier signals respectively.

$$m_a = \frac{A_m}{A_c} \tag{4.7}$$

The amplitude modulation index (m_a) for level-shifted modulation can be given by,

$$m_a = \frac{A_m}{A_c(m-1)} \tag{4.8}$$

Here, A_m indicates the peak amplitude of modulating wave, and A_c is the peak amplitude of each carrier.

The amplitude modulation index lies in the range of 0 to 1 for both phase-shifted and level-shifted modulations.

(ii) Device and inverter switching frequencies

The device switching frequency of a phase-shifted carrier type MLI is same as the frequency of its carrier signal i.e.

$$f_{dev} = f_c \tag{4.9}$$

Switching frequency of the inverter with phase-shifted modulation can be given by the following equation.

$$f_{inv} = (m-1)f_{dev} \tag{4.10}$$

On the contrary, the inverter switching frequency of a level-shifted carrier type MLI is same as the frequency of its carrier signal i.e.

$$f_{inv} = f_c \tag{4.11}$$

The device switching frequency for level-shifted can be obtained from expression (4.12),

$$f_{dev} = \frac{f_{inv}}{(m-1)} \tag{4.12}$$

(iii) Device conduction period

The time for which each device in case of phase-shifted carrier based inverter conduct is same for all. However it is different for level-shifted modulation.

(iv) Need of rotating carrier

An uneven distribution of power between various cells is resulted in case of level-shifted PWM, giving rise to high harmonic content in the input current of MLI. This drawback is overcome by using a rotating carrier. It consequently gives rise to uniform power distribution among the inverter cells. This problem does not exist in phase-shifted PWM as the carriers are shifted from each other by a definite angle, such that the harmonic content of output voltage is reduced.

Hence, it can be summarized from the above comparison between phase-shifted and level-shifted modulation techniques that,

a) The device switching frequency is same for all devices in phase-shifted modulation, whereas in case of level-shifted it is different.

b) The device conduction period is same for all devices in case of phase-shifted, but different for level-shifted modulation.
c) Rotation of switching patterns is required only in case of level-shifted modulation.
d) And finally, the THD of output voltage is better in case of level-shifted PWM which has been proven later in this chapter.

4.3. System Description of Cascaded MLI Based APF

This chapter focuses on the application of MLI on APF for current harmonics compensation. Figure 4.7 shows the system configuration of shunt APF employing cascaded m-level MLI. Supply voltage in three phases is shown as (V_{sa}, V_{sb}, V_{sc}). A diode rectifier with RL load on its DC side is present, that draw non-sinusoidal current (i_{La}, i_{Lb}, i_{Lc}). In absence of APF, current drawn from the utility (i_{sa}, i_{sb}, i_{sc}) is exactly same as the load current i.e.

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{4.13}$$

The necessary compensation filter current (i_{ca}, i_{cb}, i_{cc}) generated by the shunt APF is injected into the power lines at the PCC, so as to make the resultant source current sinusoidal, i.e.

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} \tag{4.14}$$

A small RL filter inductor (R_c, L_c) at the AC-side of VSI suppresses the additional undesirable high frequency current harmonics generated during switching action of power electronic devices. This prevents the other sensitive loads present on the common utility grid from getting disturbed [103], [160]. Using a large filter inductor will result in a huge power loss, more heat dissipation, poor efficiency, bulk dimension and weight; and also degradation of high-frequency response. To find out the values of parameters R_c and L_c, let us consider only phase-a for simplicity. The filter output voltage for phase-a of MLI (V_{ca}) depends entirely upon the DC-link voltage and modulation index of inverter.

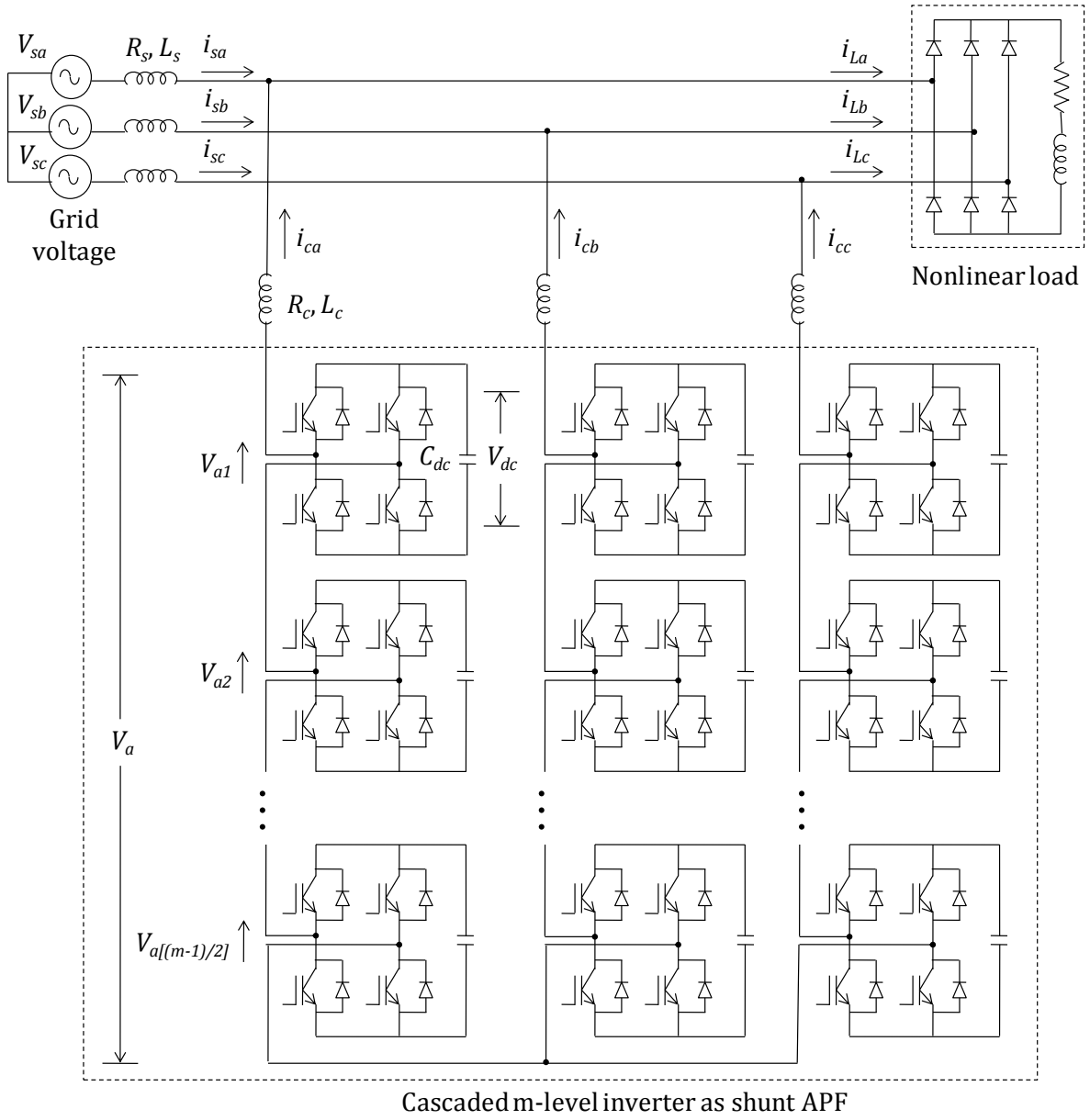


Figure 4.7: System configuration of shunt APF employing cascaded MLI

If I_{ca} represents the converter phase-a current vector, and X_c is the impedance of filter inductor [99], the source voltage vector for phase-a can be given by (4.15),

$$V_{sa} = V_{ca} + jI_{ca}X_c \tag{4.15}$$

The minimum value of filter inductor to limit the ripple current can be given by (4.16), where f_s is the switching frequency, V_m is the amplitude of mains voltage and $\hat{v}_t$ is amplitude of triangular carrier signal [161].

$$L_{cmin} = \frac{V_m}{\hat{v}_t f_s} \tag{4.16}$$

Output voltage of MLI contains lesser switching frequency ripple than 2-level VSIs. Also, generated filter currents are smoother. So, coupling filter inductor can be reduced [162].

The DC-link voltage of inverter must be maintained constant all the time, irrespective of load and supply condition. Despite of considerable advance in advanced controllers, the classical PI controller still remains the most preferred controller by researchers and application engineers, due to its simple structure and robustness. Here, Enhanced BFO introduced in Chapter 3 has been implemented for regulation of DC-bus voltage.

As observed from Figure 4.3 (b), the phase current i_a is lagging/leading the phase voltage V_a by an angle 90^o. The use of rotating carrier, makes the average charge of each DC capacitor of a m-level MLI equal to zero over $\left(\frac{m-1}{2}\right)$ half cycles of supply frequency [145]. Therefore, all the DC-link capacitor voltages of a cascaded MLI can be balanced.

The average charge of each capacitor over a half cycle $[0, \pi]$ can be given by,

$$Q_i = \int_{\pi-\theta_i}^{\theta_i} \sqrt{2} I \cos\theta \, d\theta = 0 \tag{4.17}$$

Where, $i = 1,2, \ldots, \frac{m-1}{2}$; $[\theta_i, \pi - \theta_i]$ represents the time interval during which DC capacitor connects to the AC side, and I is the rms value of line current.

In order to regulate the average voltages of all the DC-link capacitors in a cascaded MLI, only one capacitor's voltage needs to be detected and fed back [98], [145]. This makes the control of DC-link voltage very simple and reliable. Since the reference signal is a DC voltage, zero steady-state error can be secured by using a Proportional-integral (PI) controller. Given that $i_d - i_q$ method is employed here, the output of PI controller can be expressed as (4.18), where, $\Delta V_{dc} = {V_{dc}}^* - V_{dc}$.

$$i_{d1h} = K_p \Delta V_{dc} + K_i \int \Delta V_{dc} \cdot dt \tag{4.18}$$

Figure 4.8 shows the closed-loop control of cascaded MLI based APF system. This resembles the Figure 3.8, except the fact that in conventional VSI only one DC-bus capacitor is present. Whereas, many DC-bus capacitors are there in cascaded MLI and voltages across them can be controlled by taking care of only one capacitor voltage.

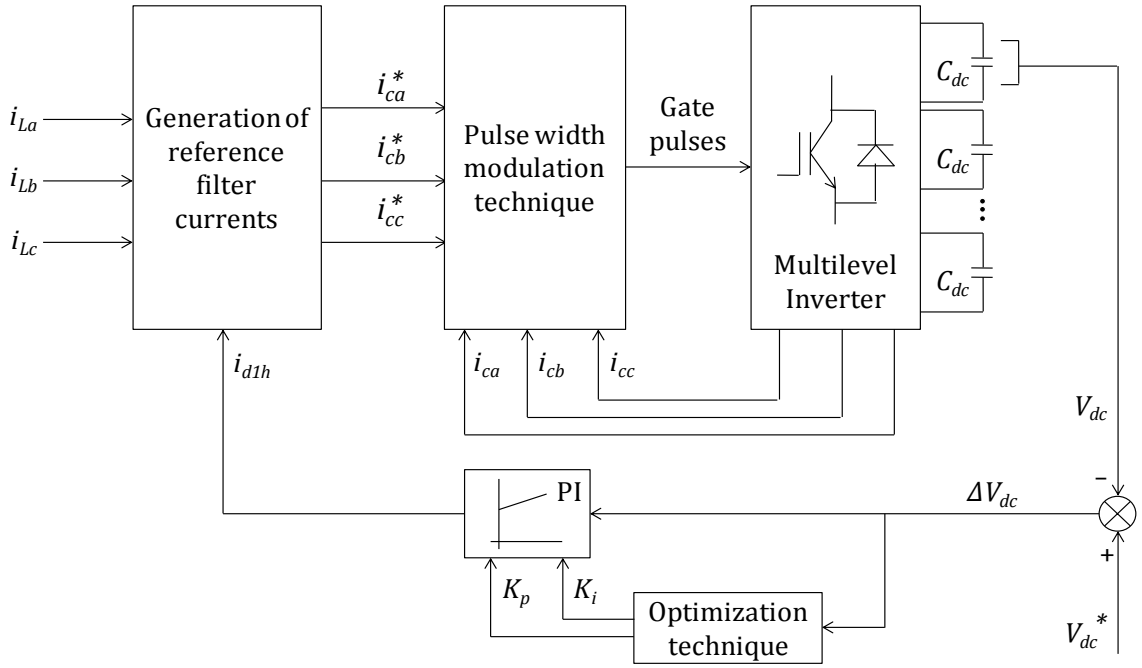


Figure 4.8: Closed loop control block diagram of the cascaded MLI based APF system

4.4. Results and Discussion

4.4.1. Simulation results

The advantage of employing MLIs in APF is that, they can reduce the additional undesired harmonics present in compensation current generated by the filter itself, since they can produce voltage with more number of levels than conventional 2-level inverters. The more levels the MLI has, the better the quality of voltage generated. To validate this, extensive simulations were carried out for 3, 5, 7 and 9-level cascaded MLIs with separate 100V DC sources. The carrier-based PWM technique used in 2-level VSIs can be extended for multilevel inverters using a single sinusoidal reference and multiple numbers of triangular carrier signals that are either level-shifted or phase-shifted, as explained in Section 4.2. Number of carrier signals required for producing an inverter output voltage with m number of distinct levels is $(m-1)$. The output phase voltage waveforms obtained with phase-shifted, IPD, POD and APOD PWM techniques along with their corresponding THDs are depicted in Figures 4.9 – 4.12 for 3-level, 5-level, 7-level and 9-level cascaded MLIs respectively. These harmonic spectra are calculated by performing Fast Fourier Transform (FFT) analyses in MATLAB.

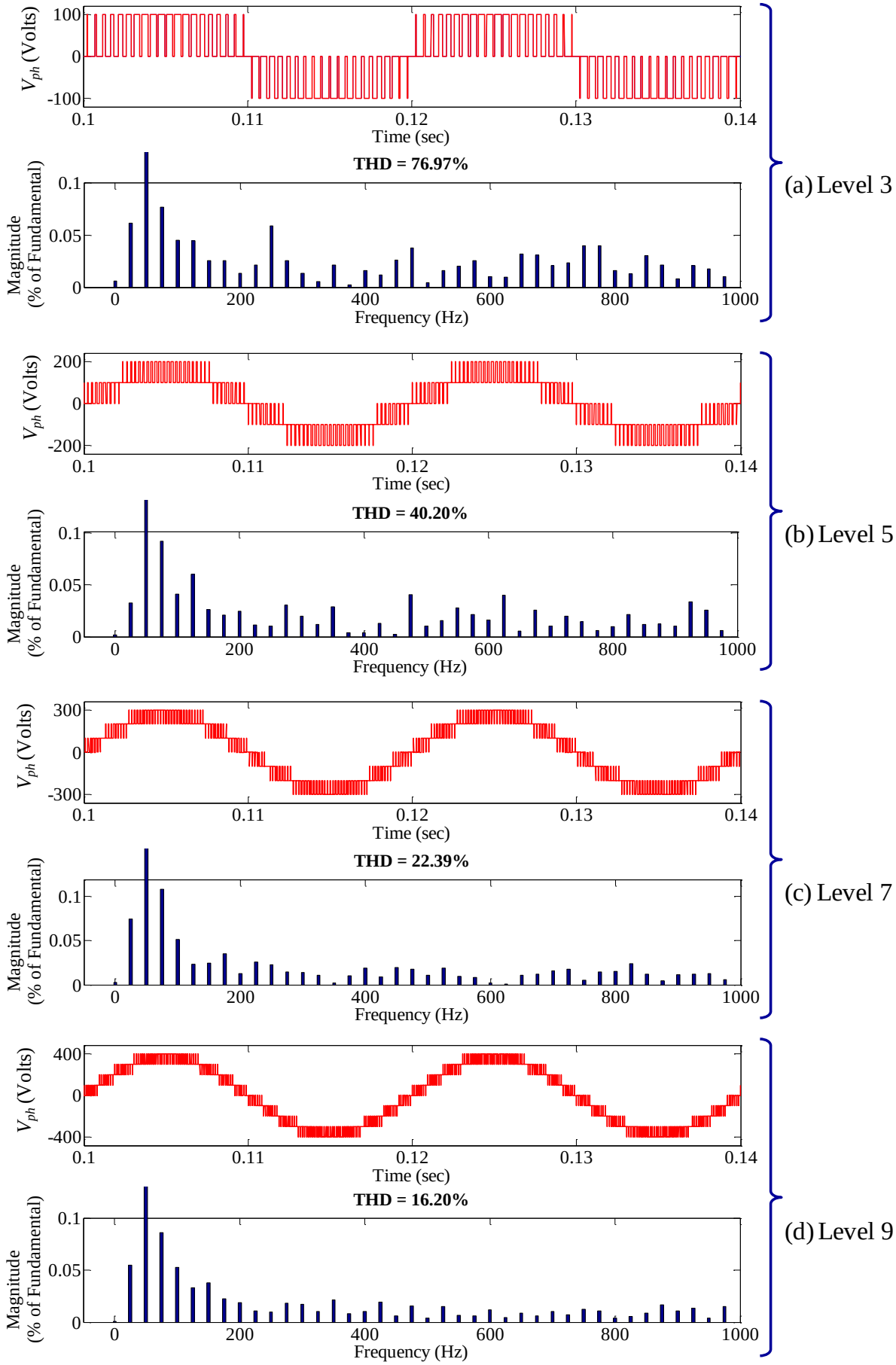


Figure 4.9: Phase voltages and THDs for MLIs using phase-shifted PWM

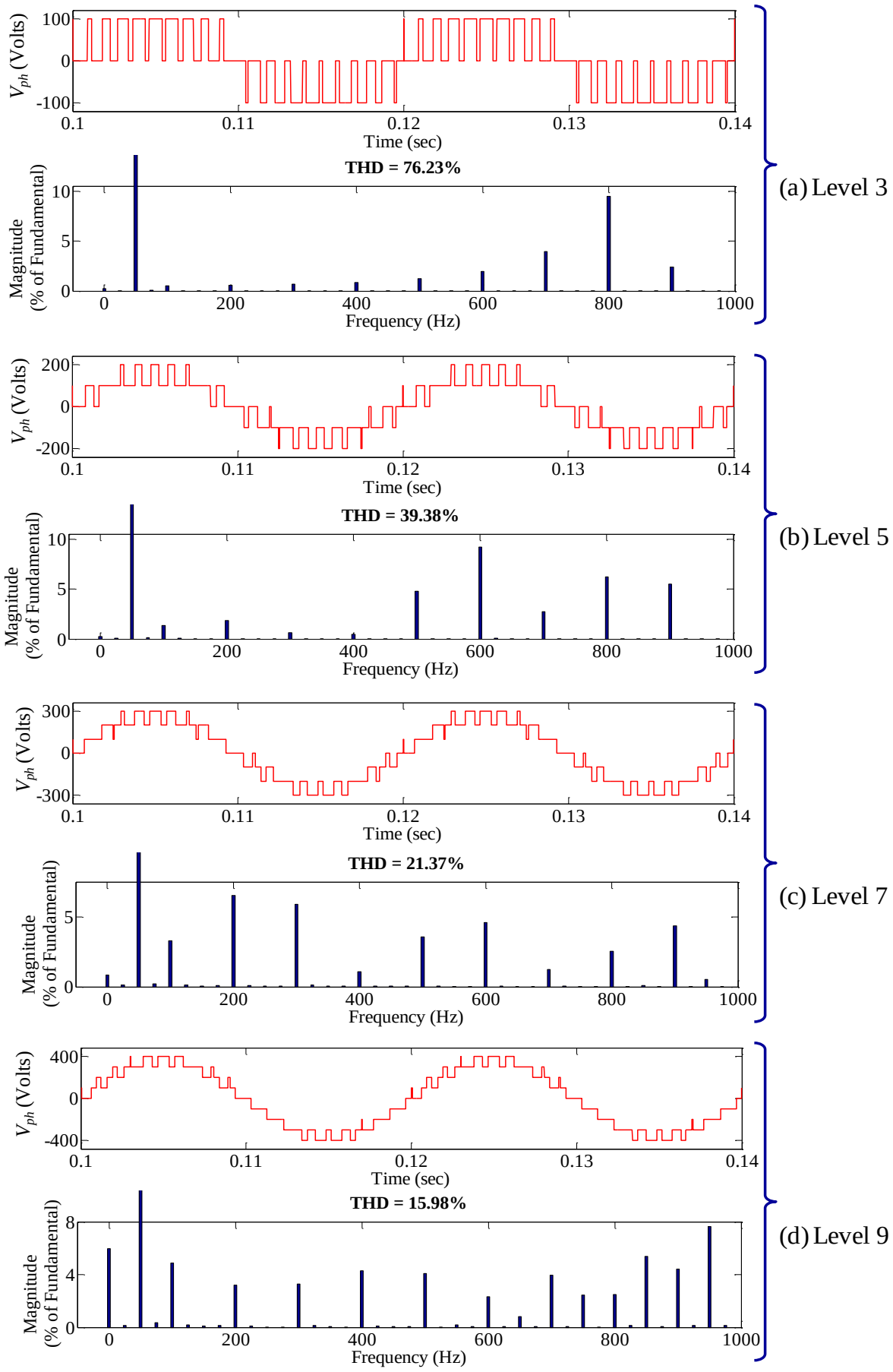


Figure 4.10: Phase voltages and THDs for MLIs using level-shifted IPD PWM

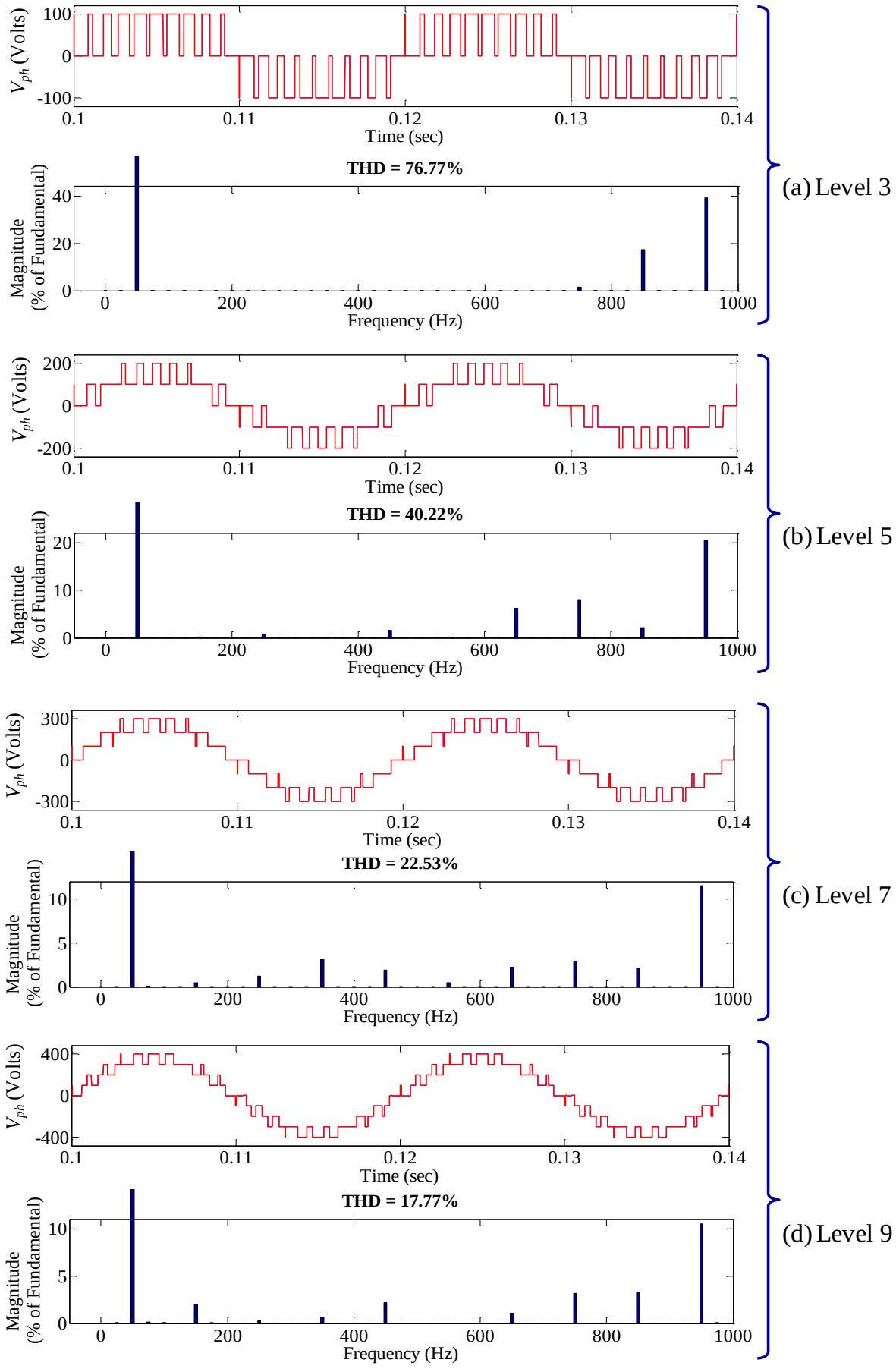


Figure 4.11: Phase voltages and THDs for MLIs using level-shifted POD PWM

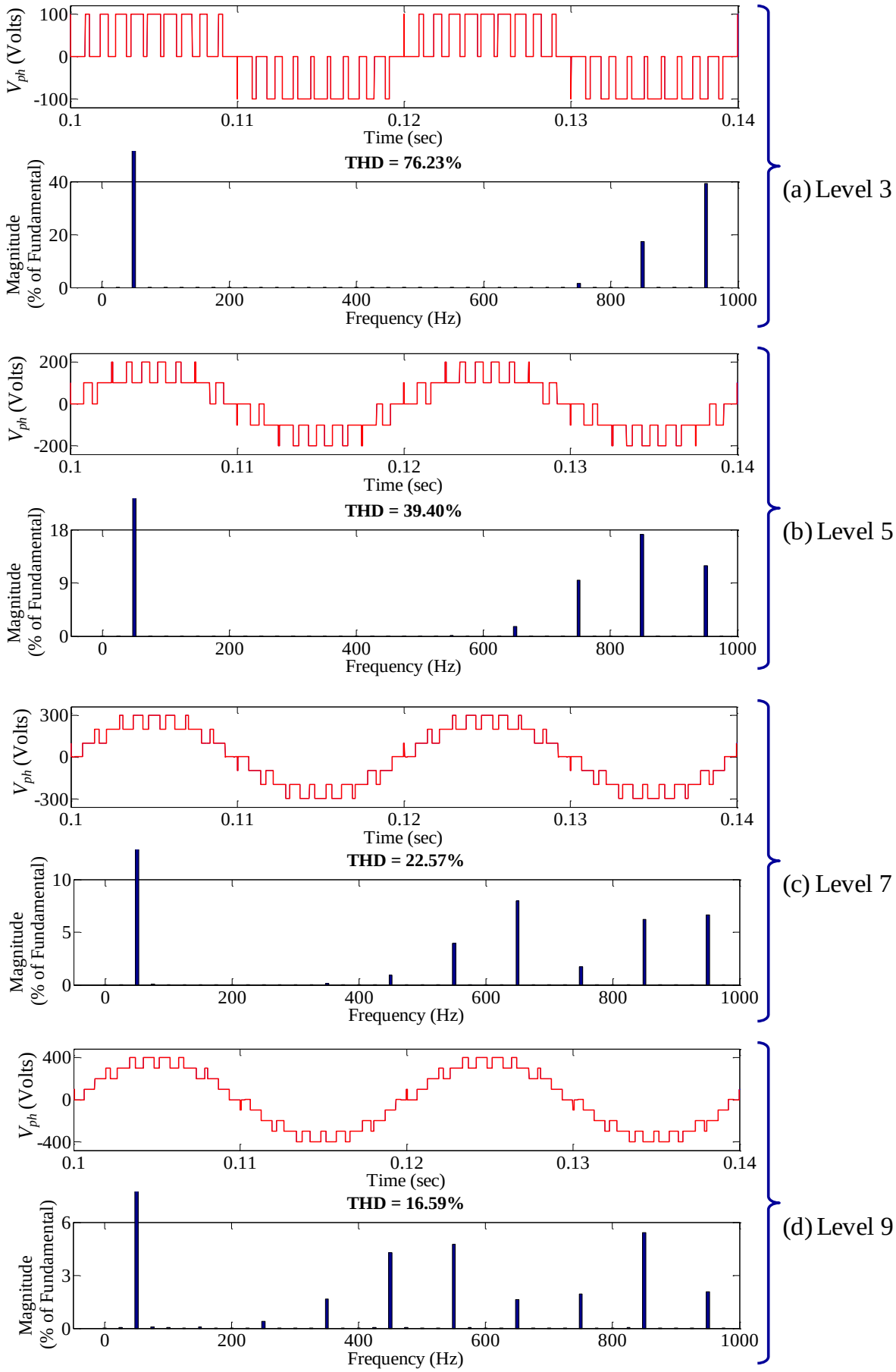


Figure 4.12: Phase voltages and THDs for MLIs using level-shifted APOD PWM

The output voltages have amplitudes 100V, 200 V, 300V and 400V for 3, 5, 7 and 9-level MLIs respectively. The output voltage THDs obtained with different carrier-based PWM techniques for cascaded MLIs of level 3, 5, 7 and 9 are showcased in Table 4.2 for comparison. It can be observed that with increase in number of voltage levels, the nature of output voltage waveforms approaches to sinusoidal, resulting in reduction of harmonic content. With phase-shifted PWM, the THD is brought down to 76.97%, 40.20%, 22.39% and 16.20% with 3, 5, 7 and 9-level MLIs respectively. Similarly, with level-shifted IPD modulation, the corresponding THDs obtained are 76.23%, 39.38%, 21.37% and 15.98%. Meanwhile, the PWM with POD results in THDs of 76.77%, 40.22%, 22.53% and 17.77% in respective order. Likewise, the APOD level-shifted PWM yields THDs of 76.23%, 39.40%, 22.57% and 16.59%. Hence, this proves that the IPD PWM technique provides the best harmonic profile amongst all three modulation schemes as stated in References [163] and [164]. Here onwards, level-shifted carrier based PWM for MLIs is used in this chapter and the carriers are in phase (IPD) for generation of switching signals.

Table 4.2: THDs of output phase voltages for cascaded MLIs employing phase-shifted, IPD, POD and APOD PWM techniques

Cascaded MLI	Phase-shifted PWM	Level-shifted PWM		
		IPD	POD	APOD
Level - 3	76.97%	76.23%	76.77%	76.23%
Level - 5	40.20%	39.38%	40.22%	39.40%
Level - 7	22.39%	21.37%	22.53%	22.57%
Level - 9	16.20%	15.98%	17.77%	16.59%

Simulations are performed to find out the effectiveness of MLI-based shunt APFs under ideal and non-ideal supply voltage conditions. The compensation characteristics of APFs during transient conditions with various control schemes and optimization techniques are already comprehensively studied in chapters 2 and 3 brings out a conclusion that, a nearly

instantaneous compensation can be achieved during transient conditions with the implementation of $i_d - i_q$ scheme in combination with Enhanced BFO. This chapter deals with only the steady state performance of APF. Hence, the effectiveness of various three-phase three-wire MLI topologies in harmonic compensation is judged only in terms of their source currents THDs. Therefore, the investigations in this chapter are conducted with only one nonlinear load i.e. a three-phase diode-rectifier with a series RL load on its DC-side. Unlike conventional VSIs, a three-phase cascaded m-level inverter requires $\frac{3(m-1)}{2}$ number of DC-link capacitors. All the DC-link capacitors in a MLI are identical and hence voltages across them are equal. The capacitor values are so chosen that, the individual DC-bus voltages of all the H-bridges of a MLI add up to an equal total voltage irrespective of the level of MLI [145]. All other system parameter values are identical to that of previous chapter, as listed in Table 3.1. Values of optimization parameters for Enhanced BFO algorithm are kept same as the Table 3.2 of Chapter 3.

For ideal supply condition, voltages in the three phases of utility are taken as completely balanced and sinusoidal as shown in Figure 4.13. APF performance under distorted supply condition is investigated taking a highly distorted supply voltage containing a high third harmonic component of supply in it, as shown in Figure 4.14. Similarly, simulations under unbalanced condition are studied by making the voltage in one of the phases comparatively smaller than the other two, which has been shown in Figure 4.15. Source current before compensation is same as the current drawn by the nonlinear load. The results shown in Figures 4.13 - 4.15 are the simulation waveforms for supply voltage (V_s), load current in phase-a (i_{La}), filter current in phase-a (i_{ca}), and compensated source currents in phase-a obtained with APF employing 3-level (i_{sa1}), 5-level (i_{sa2}), 7-level (i_{sa3}) and 9-level (i_{sa4}) MLIs under ideal, distorted and unbalanced supply conditions respectively. For simplicity of analysis, only phase-a current waveforms have been presented here. However, FFT analyses have been performed for computing the THDs in all the three phases of source currents before and after compensation, which are discussed later in this section.

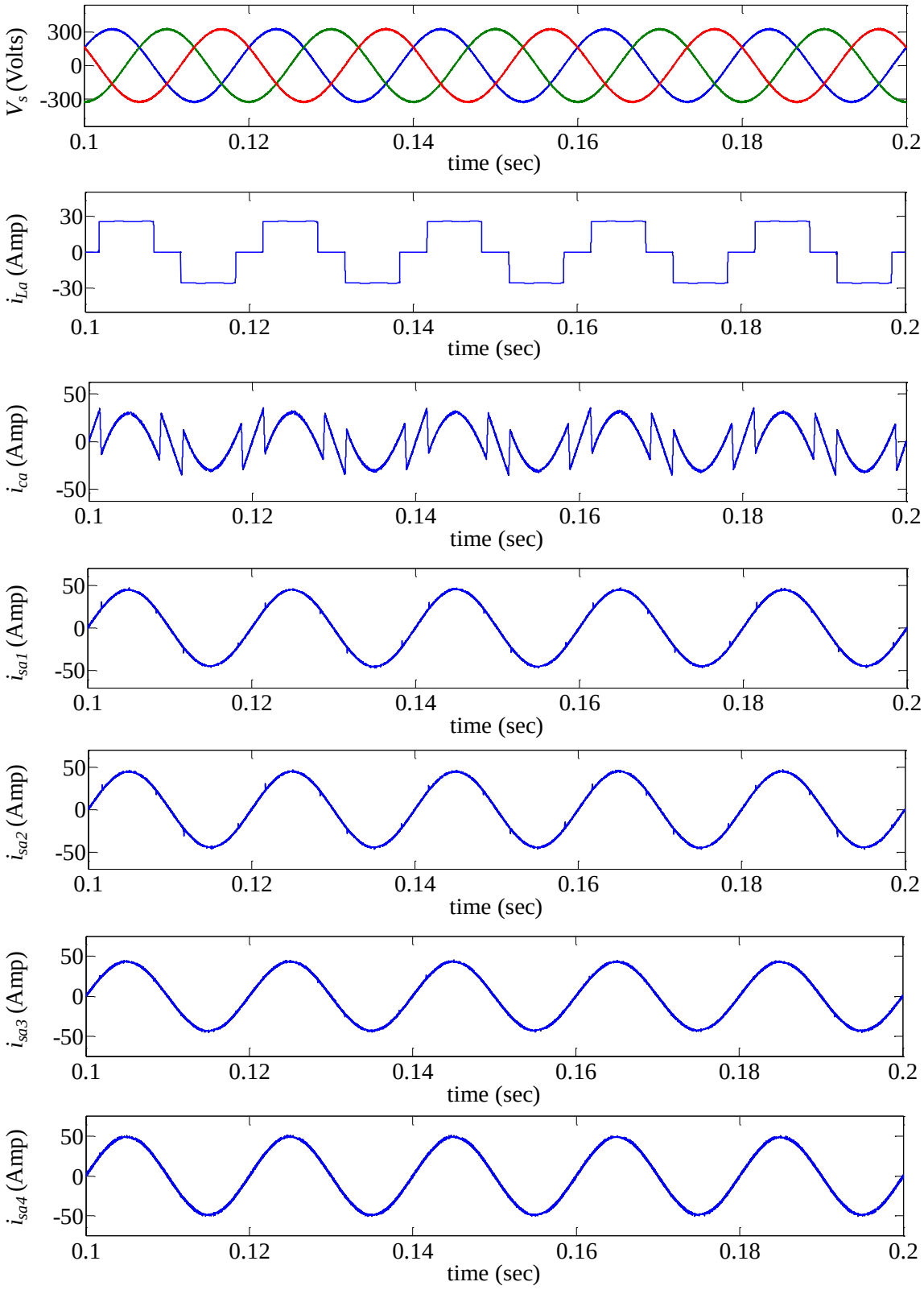


Figure 4.13: Simulation results for supply voltage (V_s), load current in phase-a (i_{La}), filter current in phase-a (i_{ca}), and compensated source currents in phase-a obtained with APF employing 3-level (i_{sa1}), 5-level (i_{sa2}), 7-level (i_{sa3}) and 9-level (i_{sa4}) MLIs under ideal supply condition

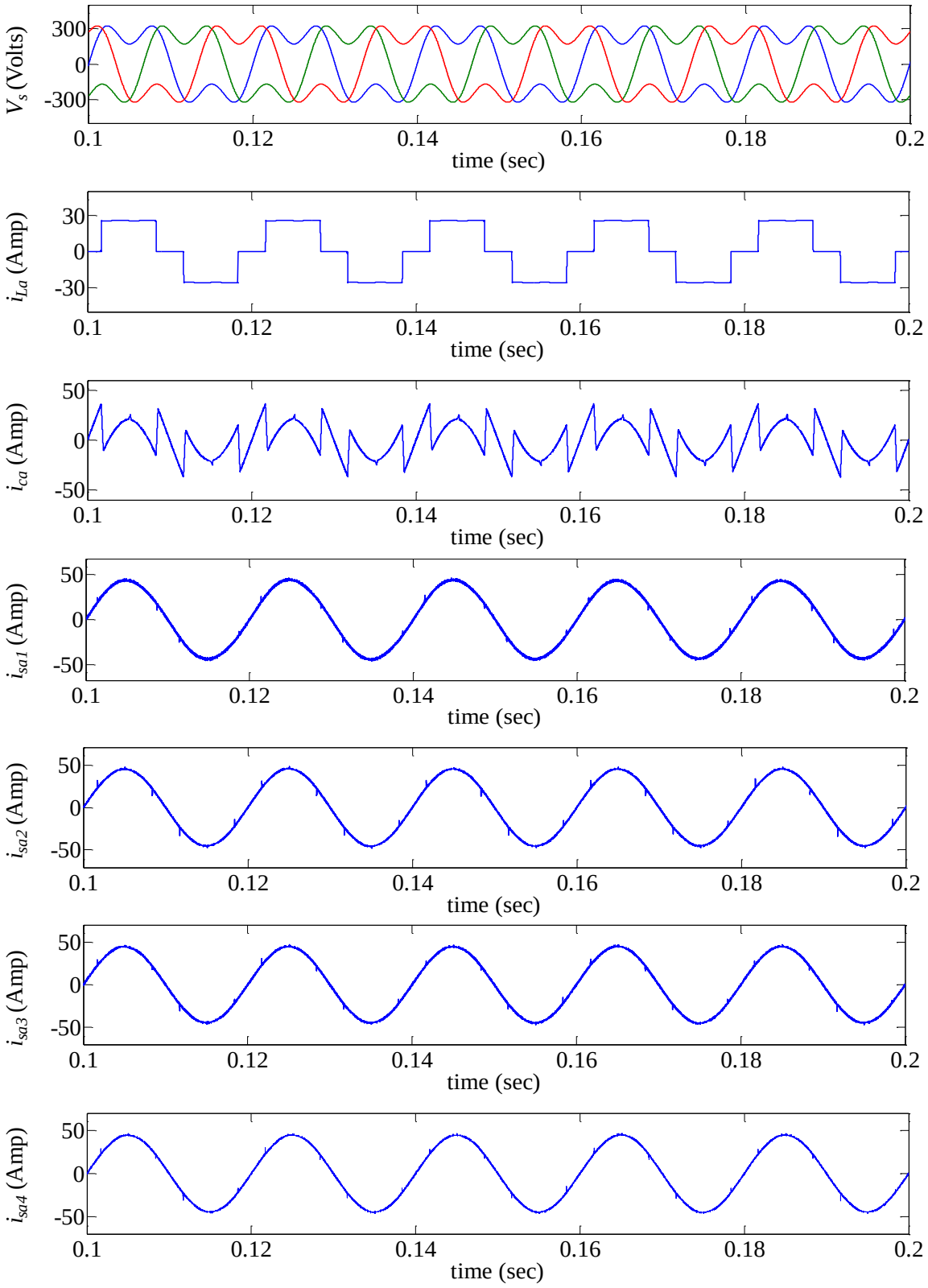


Figure 4.14: Simulation results for supply voltage (V_s), load current in phase-a (i_{La}), filter current in phase-a (i_{ca}), and compensated source currents in phase-a obtained with APF employing 3-level (i_{sa1}), 5-level (i_{sa2}), 7-level (i_{sa3}) and 9-level (i_{sa4}) MLIs under distorted supply condition

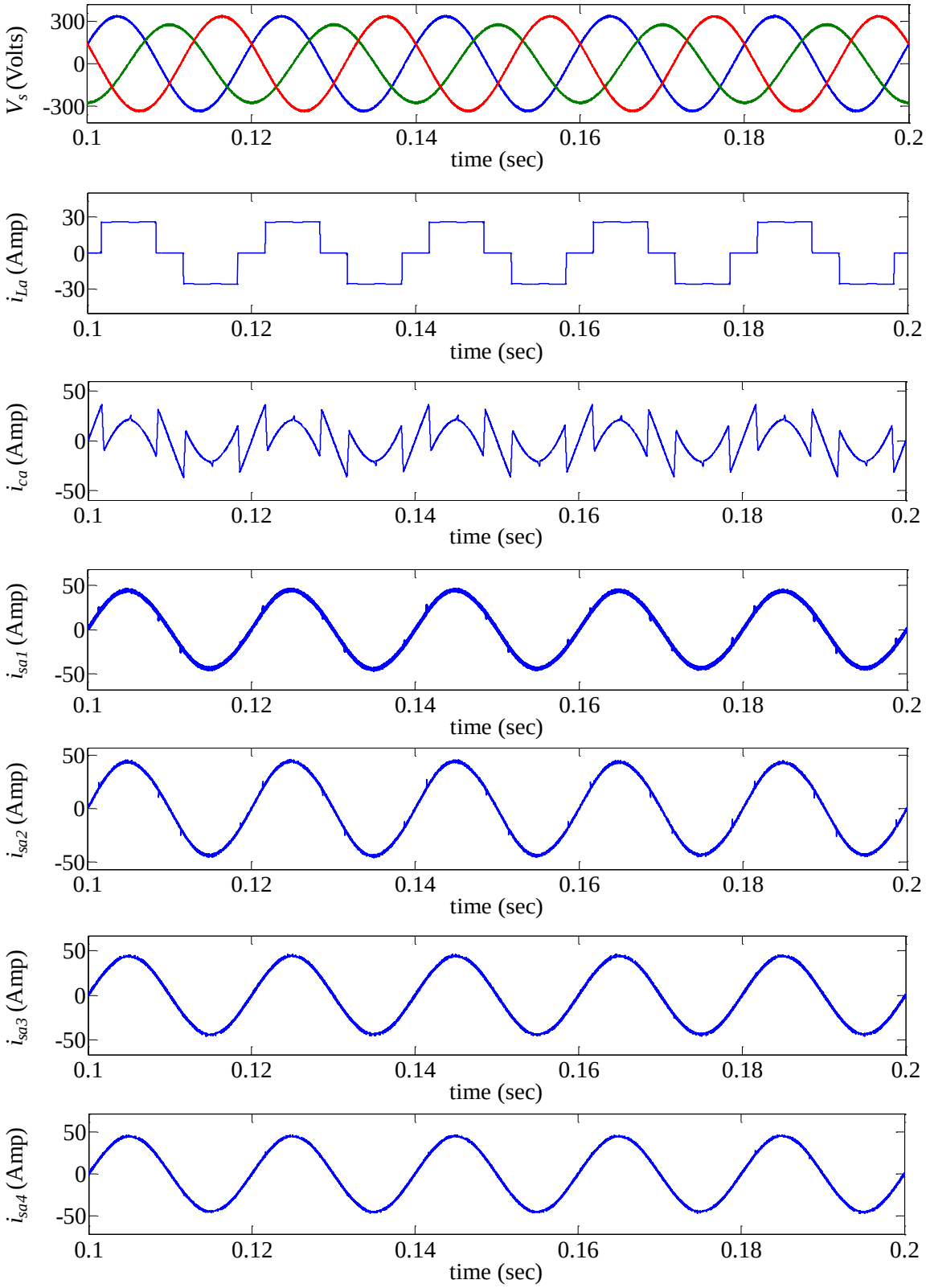
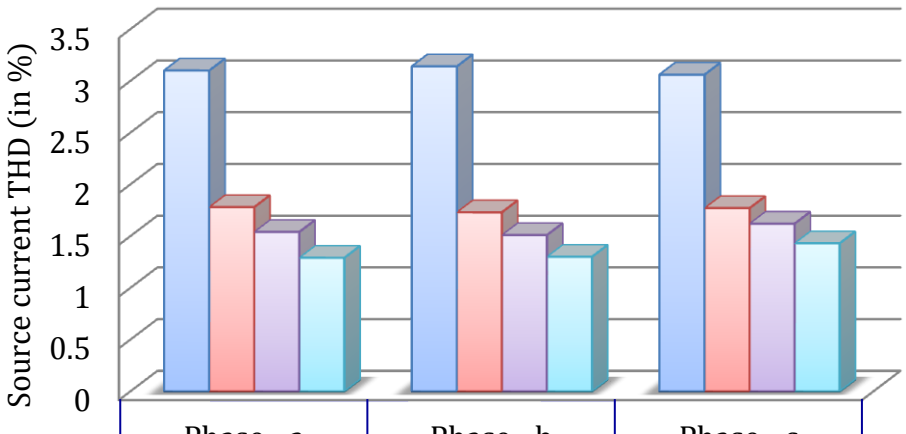


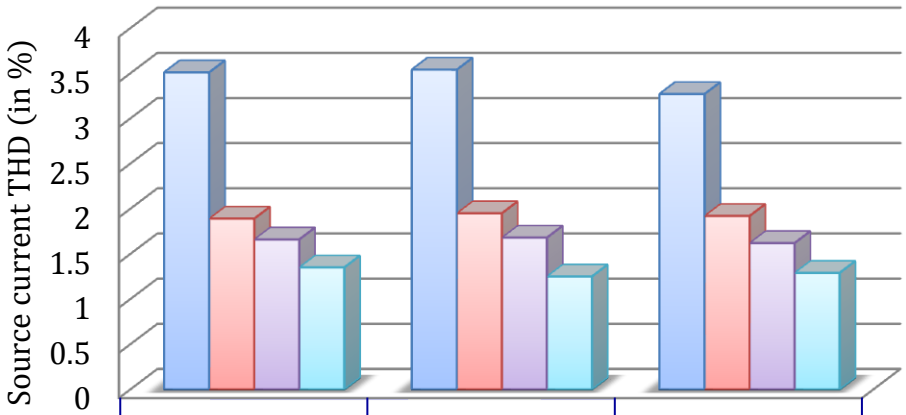
Figure 4.15: Simulation results for supply voltage (V_s), load current in phase-a (i_{La}), filter current in phase-a (i_{ca}), and compensated source currents in phase-a obtained with APF employing 3-level (i_{sa1}), 5-level (i_{sa2}), 7-level (i_{sa3}) and 9-level (i_{sa4}) MLIs under unbalanced supply condition

It is observed from the above Figures 4.13 – 4.15 that, the level of distortion in resultant source currents obtained after compensation with cascaded MLI based APFs, goes on reducing as the number of levels in the MLI is increased. To validate this, the level of distortion in each phase of source currents for 3-level, 5-level, 7-level and 9-level MLI-based APFs have been analyzed in accordance with their THDs. The THDs in phases-*a*, *b* and *c* of source current before compensation were found out to be 29.65%, 29.36% and 29.97% respectively when the supply voltage was ideal. Whereas, corresponding source current THDs were 27.89%, 28.58% and 28.09% when balanced and non-sinusoidal supply was considered for simulation. And, THDs under unbalanced sinusoidal supply were found out to be 28.01%, 28.26% and 28.19% in that order. The chart diagrams of Figures 4.16 – 4.18 show the THDs (in %) in source current after compensation with APFs employing 3-level, 5-level, 7-level and 9-level MLIs under all the above mentioned supply conditions obtained with simulations. The THD values prove that, the 9-level cascaded MLI based APF yields lowest THDs under all kinds of supply voltage.



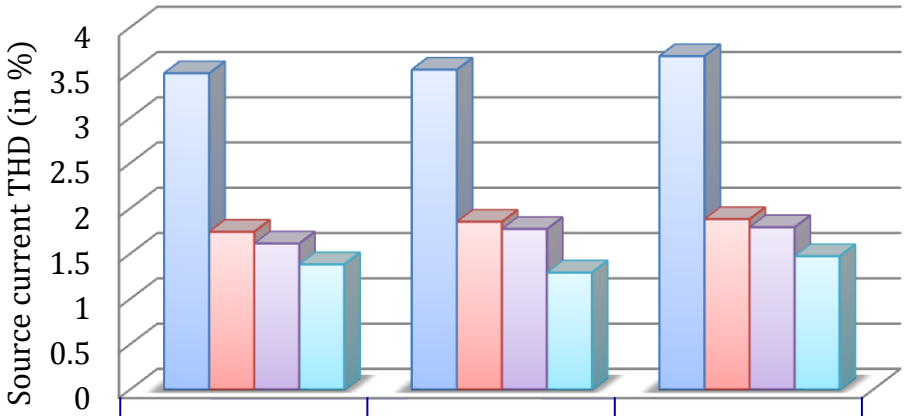
	Phase - a	Phase - b	Phase - c
3-level MLI based APF	3.1	3.14	3.06
5-level MLI based APF	1.78	1.73	1.77
7-level MLI based APF	1.54	1.51	1.62
9-level MLI based APF	1.29	1.3	1.43

Figure 4.16: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing 3-level, 5-level, 7-level and 9-level cascaded MLIs under ideal supply condition



	Phase - a	Phase - b	Phase - c
3-level MLI based APF	3.51	3.54	3.27
5-level MLI based APF	1.89	1.95	1.92
7-level MLI based APF	1.66	1.68	1.62
9-level MLI based APF	1.35	1.25	1.29

Figure 4.17: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing 3-level, 5-level, 7-level and 9-level cascaded MLIs under distorted supply condition



	Phase - a	Phase - b	Phase - c
3-level MLI based APF	3.49	3.53	3.68
5-level MLI based APF	1.74	1.85	1.88
7-level MLI based APF	1.61	1.77	1.79
9-level MLI based APF	1.38	1.29	1.47

Figure 4.18: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing 3-level, 5-level, 7-level and 9-level cascaded MLIs under unbalanced supply condition

4.4.2. RT-Lab results

The MLI output phase voltage waveforms for 3-level 5-level, 7-level and 9-level obtained with RT-Lab are depicted in Figure 4.19. Here, the cascaded MLIs utilize separate DC sources of 100 V, and the modulation technique being used is IPD level-shifted PWM. A single sinusoidal reference is compared against $(m-1)$ number of triangular carrier signals, in order to generate a m-level output voltage. RT-Lab results of Figure 4.19 can be compared against the simulation results of Figure 4.10.

Figures 4.20 - 4.22 show the RT-Lab results under ideal, distorted and unbalanced supply conditions. The results include supply voltage (V_s), load current (i_{La}), filter current (i_{ca}) and source currents after compensation with APF employing MLIs of level-3 (i_{sa1}), level-5 (i_{sa2}), level-7 (i_{sa3}) and level-9 (i_{sa4}). System parameters and optimization parameters for analysis in RT-Lab are exactly same as that considered during simulation studies.

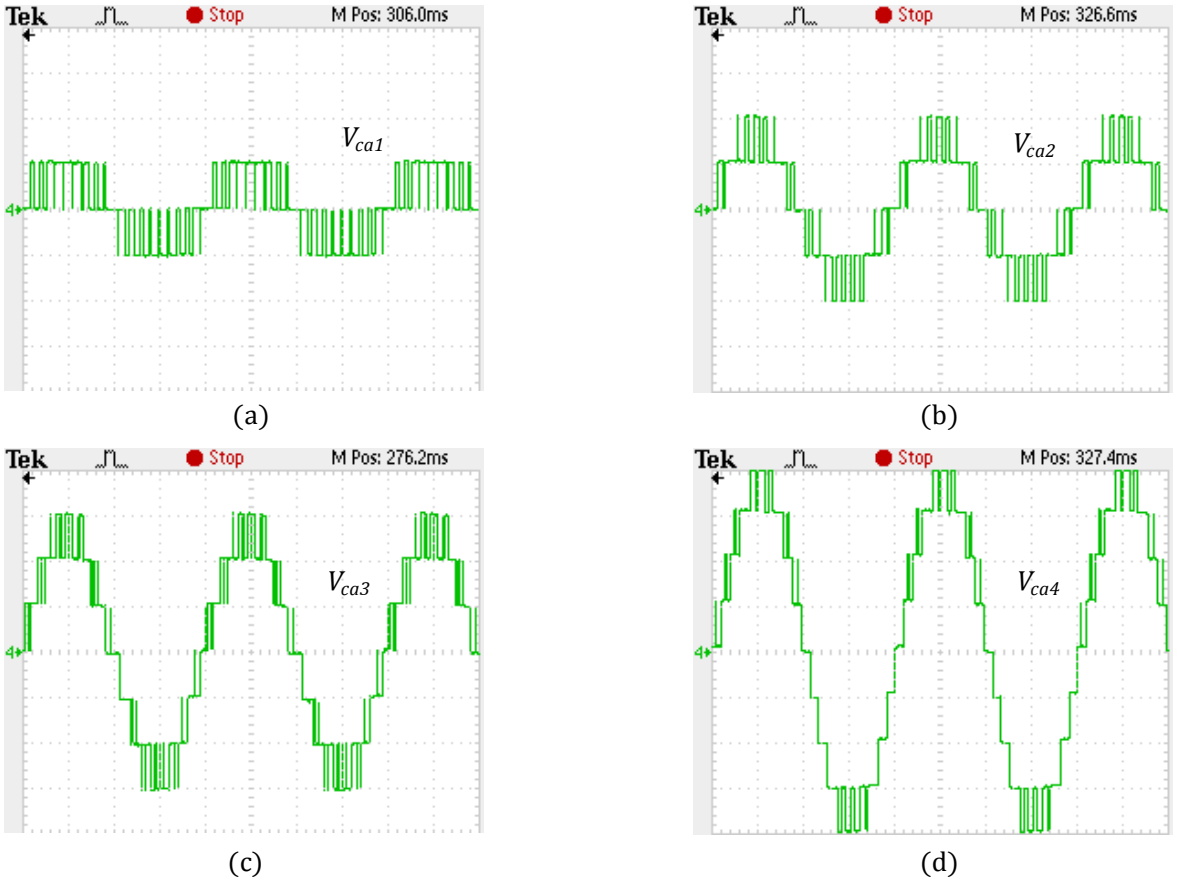
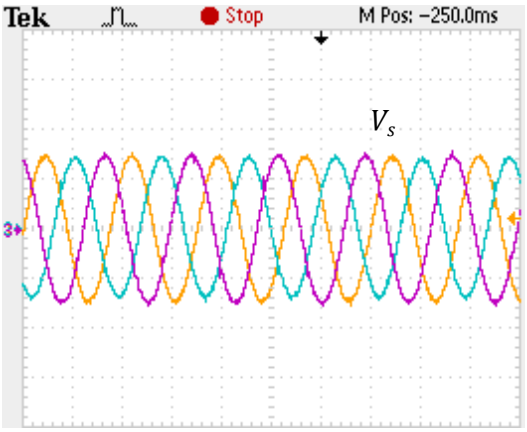
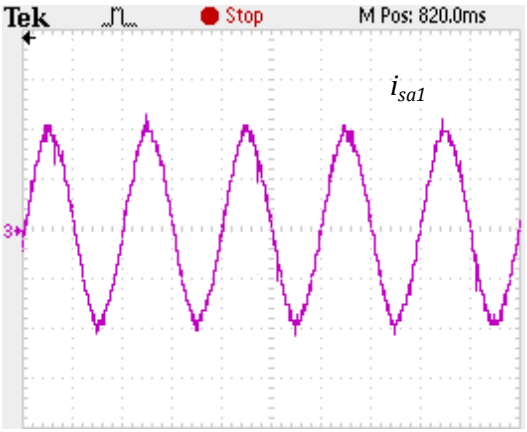


Figure 4.19: RT-Lab results for output phase voltages for cascaded MLIs of **(a)** Level-3 (V_{ca1}), **(b)** Level-5 (V_{ca2}), **(c)** Level-7 (V_{ca3}), **(d)** Level-9 (V_{ca4}); [scale: 100 V/div]

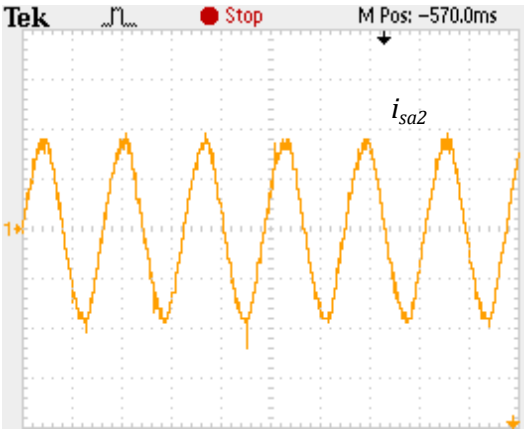


(a)

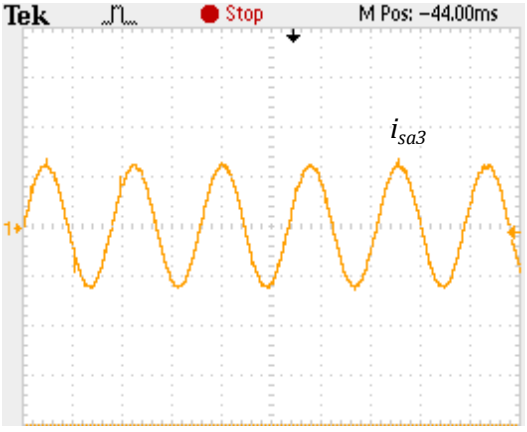
(b)



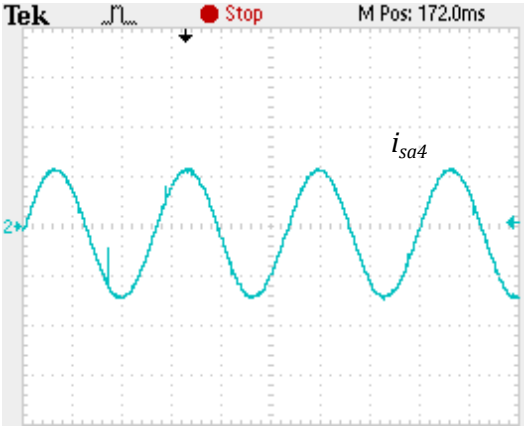
(c)



(d)



(e)



(f)

Figure 4.20: RT-Lab results for **(a)** Supply voltage (V_s) [scale: 220 V/div], **(b)** Load current (i_{La}) [scale: 35 A/div] and filter current (i_{ca}) [scale: 35 A/div], **(c) – (f)** Source currents after compensation with APF employing MLIs of level-3 (i_{sa1}) [scale: 25 A/div], level-5 (i_{sa2}) [scale: 30 A/div], level-7 (i_{sa3}) [scale: 40 A/div] and level-9 (i_{sa4}) [scale: 40 A/div] under ideal supply

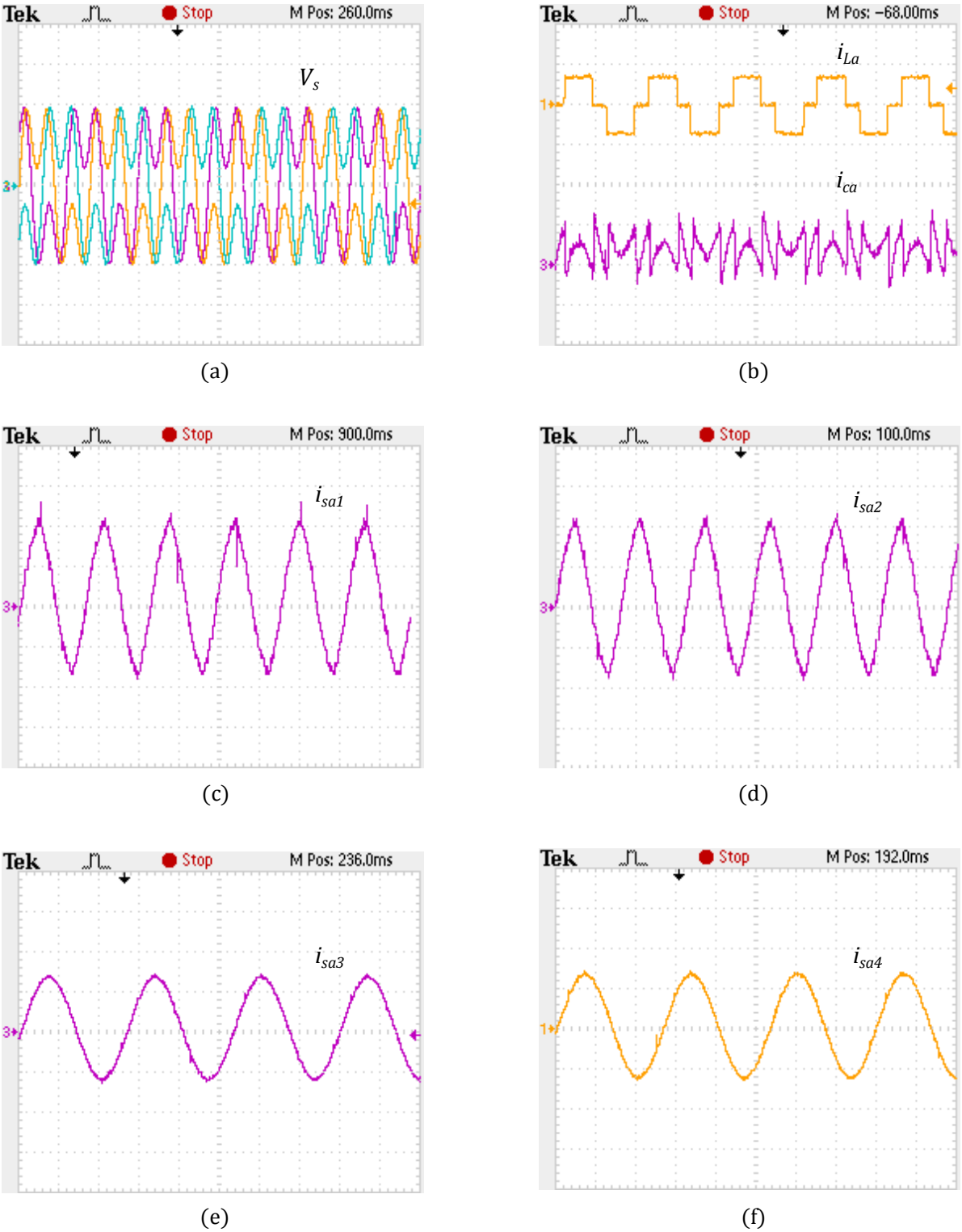


Figure 4.21: RT-Lab results for **(a)** Supply voltage (V_s) [scale: 160 V/div], **(b)** Load current (i_{La}) [scale: 35 A/div] and filter current (i_{ca}) [scale: 35 A/div], **(c) – (f)** Source currents after compensation with APF employing MLIs of level-3 (i_{sa1}) [scale: 25 A/div], level-5 (i_{sa2}) [scale: 25 A/div], level-7 (i_{sa3}) [scale: 40 A/div] and level-9 (i_{sa4}) [scale: 40 A/div] under distorted supply

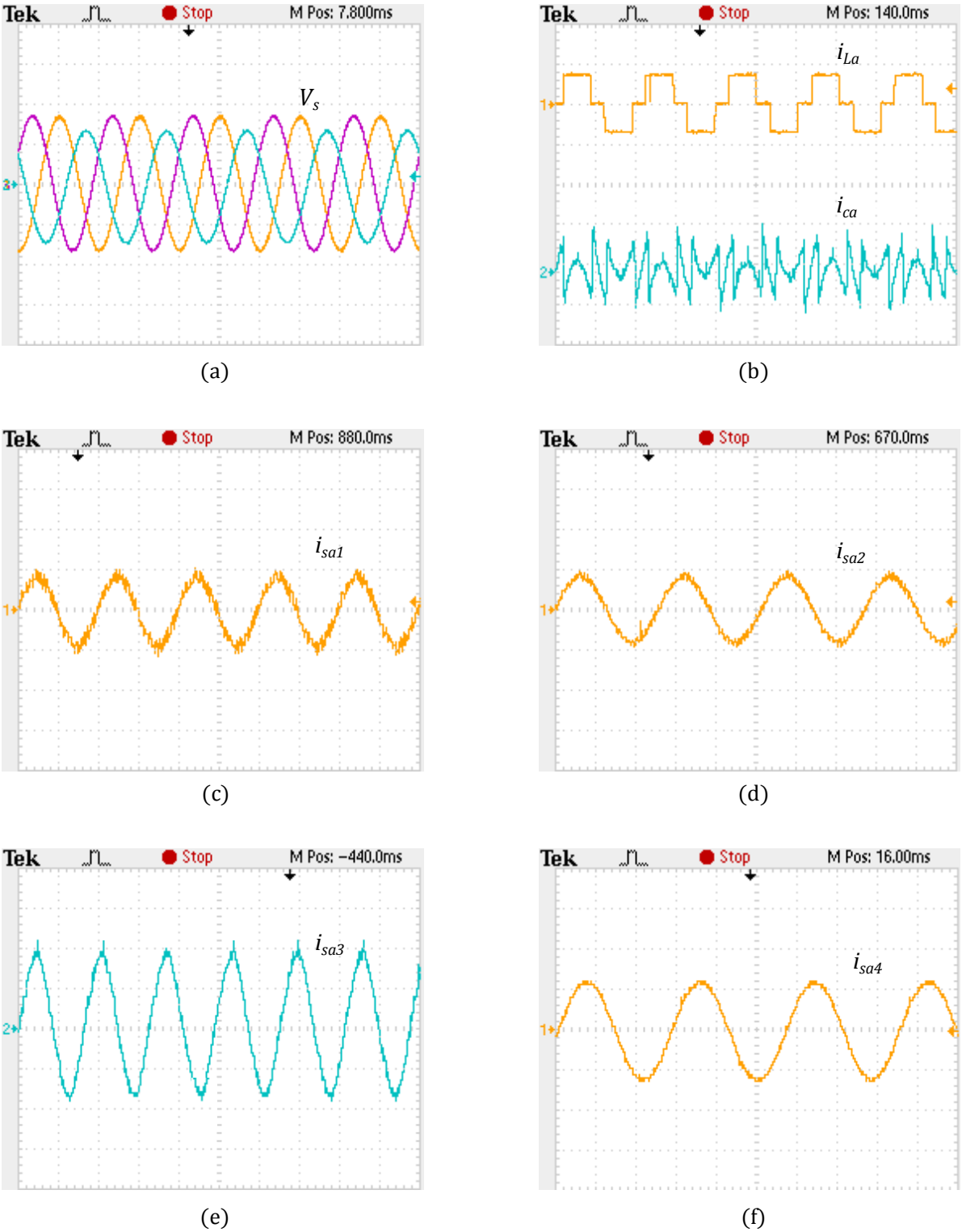
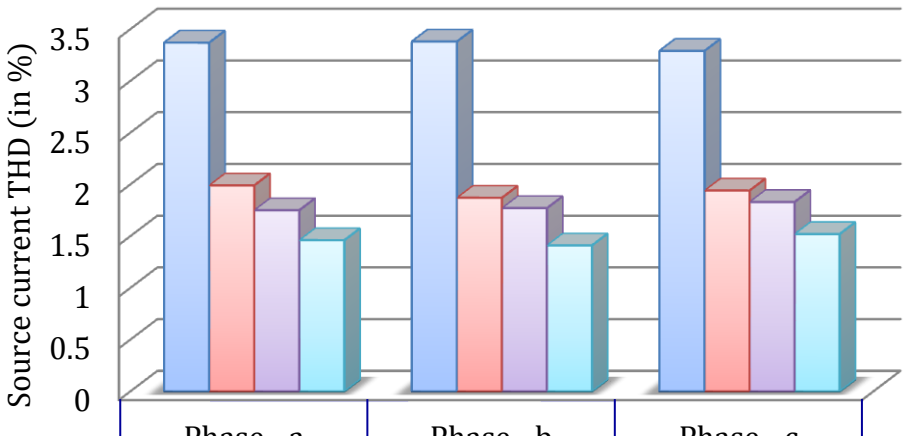


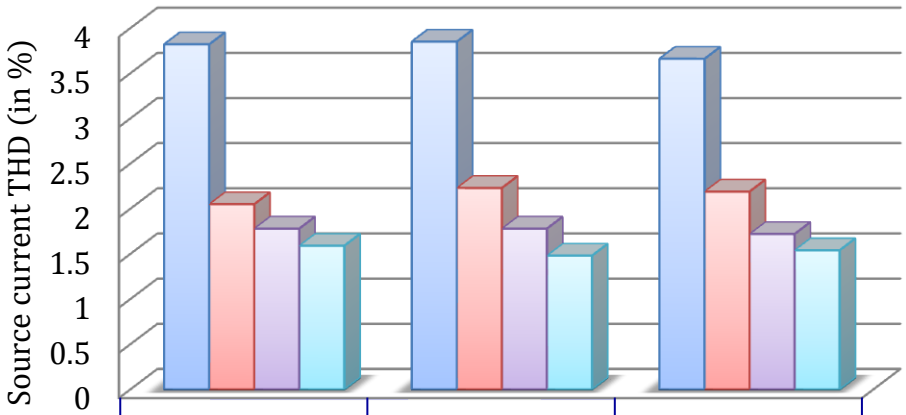
Figure 4.22: RT-Lab results for **(a)** Supply voltage (V_s) [scale: 200 V/div], **(b)** Load current (i_{La}) [scale: 35 A/div] and filter current (i_{ca}) [scale: 35 A/div], **(c) – (f)** Source currents after compensation with APF employing MLIs of level-3 (i_{sa1}) [scale: 50 A/div], level-5 (i_{sa2}) [scale: 50 A/div], level-7 (i_{sa3}) [scale: 25 A/div] and level-9 (i_{sa4}) [scale: 40 A/div] under unbalanced supply

The THDs in *a*, *b* and *c* phases of load current obtained with RT-Lab are: 30.82%, 30.64% and 30.37% under ideal supply; 28.06%, 29.18% and 28.87% under distorted supply; and 28.47%, 28.94% and 29.06% under unbalanced supply respectively. These also specify the THDs of source current before compensation. It is observed from Figures 4.23 – 4.25 that, with the use of MLIs of level 3, 5, 7 and 9, the THDs in phase-*a* of source current could be brought down to 3.37%, 1.99%, 1.75% and 1.46% under ideal supply condition; 3.82%, 2.05%, 1.78% and 1.59% under non-sinusoidal supply; and 3.67%, 1.97%, 1.73% and 1.64% under unbalanced supply respectively. Similarly, the THDs in other two phases of source currents are also provided in the charts. Hence, this shows that, the current THDs are lowered down sufficiently below 5% and are well acceptable as per IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems. This considerable reduction in THD is possible not only due to the use of MLIs as APF, but also due to the implementation of Enhanced BFO technique to optimize the PI controller gains for improved DC-link voltage regulation.



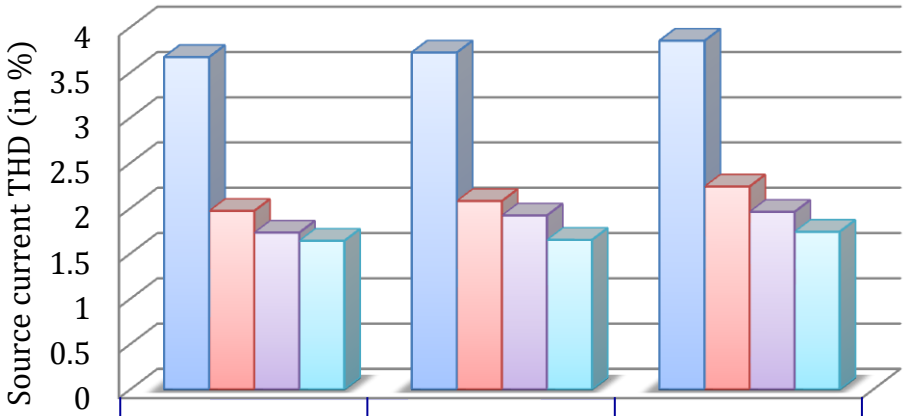
	Phase - a	Phase - b	Phase - c
3-level MLI based APF	3.37	3.38	3.29
5-level MLI based APF	1.99	1.87	1.94
7-level MLI based APF	1.75	1.77	1.83
9-level MLI based APF	1.46	1.41	1.52

Figure 4.23: Chart diagram showing source current THDs (in %) obtained in RT-Lab after compensation with APFs employing 3-level, 5-level, 7-level and 9-level MLIs under ideal supply condition



	Phase - a	Phase - b	Phase - c
3-level MLI based APF	3.82	3.85	3.66
5-level MLI based APF	2.05	2.23	2.19
7-level MLI based APF	1.78	1.78	1.72
9-level MLI based APF	1.59	1.48	1.54

Figure 4.24: Chart diagram showing source current THDs (in %) obtained in RT-Lab after compensation with APFs employing 3-level, 5-level, 7-level and 9-level MLIs under distorted supply condition



	Phase - a	Phase - b	Phase - c
3-level MLI based APF	3.67	3.72	3.85
5-level MLI based APF	1.97	2.08	2.24
7-level MLI based APF	1.73	1.92	1.96
9-level MLI based APF	1.64	1.65	1.74

Figure 4.25: Chart diagram showing source current THDs (in %) obtained in RT-Lab after compensation with APFs employing 3-level, 5-level, 7-level and 9-level MLIs under unbalanced supply condition

4.5. Summary

The chapter presents cascaded MLI configuration of VSI as an appropriate choice for compensation of current harmonics in distribution networks. Practically, the modular layout and packaging enables any number of H-bridge modules to be stacked in order to get the desired inverter output and makes it suitable for medium-to-high power, high voltage applications. Besides, a major purpose the MLI serves is reduction of stresses across the semiconductor switching devices. A comparison between APFs employing cascaded 3, 5, 7 and 9-level MLIs is realized under ideal, distorted and unbalanced supply voltage conditions. The reference compensation filter currents for three-phases are extracted using $i_d - i_q$ scheme and multilevel carrier based IPD-PWM is carried out to generate switching signals for MLI. Optimal harmonic compensation is ensured by the proposed implementation of Enhanced BFO-based PI controller for successful regulation of inverter DC-link voltage, thus minimizing the undesirable power loss responsible for degradation of APF performance. The results obtained with simulations and RT-Lab demonstrate that, with increase in the number of levels from 3 to 9, the distortion in source current is reduced to negligibly small amount that is, APF employing cascaded 9-level MLI yields the lowest values of source current THDs irrespective of the supply voltage condition.

Chapter 5

APF Topologies for Three-Phase Four-Wire Systems

5.1. Introduction

Along with other power quality problems such as harmonic currents and unbalanced loading; the three-phase four-wire distribution systems are continuously being subjected to another severe problem of excessive neutral current. The issues related to harmonic currents have already been clearly discussed in previous chapters. Unbalance in source current is either due to unbalanced single-phase and three-phase loads in the system, or because of unbalanced supply voltage. Presence of unequal single-phase loads, blown fuses in one of the phases of a three-phase capacitor bank or single phasing conditions result in unbalanced supply condition; as the voltage becomes asymmetrically balanced between the phases of supply.

A three-phase four-wire electrical distribution system typically supplies power to various industrial and domestic loads such as, adjustable speed drives for heaters, ventilators and air-conditioning systems, fluorescent lighting circuits with conventional and electronic ballasts, computers for data processing and automation in industrial plants and many other power electronic loads. A switched mode type power electronic converter is almost an integral part of each of these loads. Hence, they draw significant amount of harmonic currents having orders in odd multiples of three. The frequency of triplen order harmonics being thrice the fundamental supply frequency, they are displaced from each other in space by an angle of 120°. This makes the triplen harmonics in phase with each

other as shown in Figure 5.1. As a result, these harmonics do not cancel out each other, rather their cumulative addition leads to an excessive current in the neutral conductor.

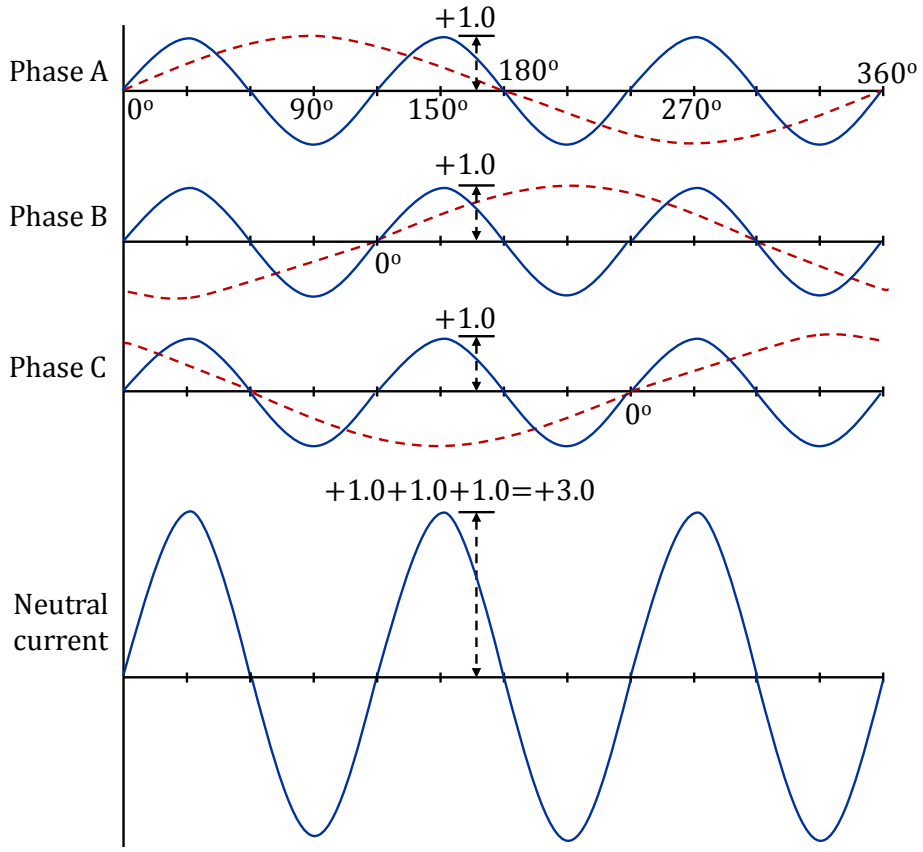


Figure 5.1: Triplen harmonic currents in three-phase power systems

The current in neutral conductor when operating conditions are normal and loads are balanced, should not exceed 20% of the normal phase current magnitude [107]. Unfortunately such ideal operating conditions no longer exist, owing to the proliferation of advanced power conversion technologies and computer/data processing equipments as stated above. This high neutral current may give rise to severe detrimental consequences such as, (a) overloaded power feeders due to improper sizing of neutral conductor, (b) overheating of transformers due to harmonic currents, (c) damage or failure of insulation, (d) common mode noise, (e) voltage drop created by neutral current causes an excessive neutral to ground voltage resulting in voltage distortion. This common mode potential can result in the malfunction of sensitive electronic components [6].

Though APFs for three-phase three-wire systems were successfully developed, the concept of three-phase four-wire APFs came into existence in 1980's [165]. Various three-phase four-wire APF topologies have gained attention to solve the power quality issues such as harmonics, unbalanced currents, neutral currents and load reactive power.

In this chapter, a three-level H-bridge (3L-HB) VSI topology for three-phase four-wire shunt APF is proposed, that possesses all the advantages of MLI, as discussed in Chapter 4. This can be connected to the distribution lines directly, and does not require bulky and expensive coupling transformers. The 3L-HB APF topology is compared with the existing two-level split-capacitor (2C), four-leg (4L) and three H-bridges (3HB) VSI topologies, showing their topological differences, areas of application and load compensation capabilities under ideal, distorted and unbalanced supply voltage conditions. Evaluations are carried out taking into consideration the unbalanced loading scenario (with both three-phase and single-phase loads being operated at a time), which is prevalent in three-phase four-wire systems. For effective compensation, irrespective of the number and rating of capacitors used in any particular topology, voltages across them must be maintained constant. Hence, the chapter also proposes the implementation of Enhanced BFO for optimum regulation of DC-link voltages of all the above mentioned topologies.

This chapter provides a review of various two-level VSI topologies, such as 2C, 4L and 3HB in Sections 5.2, 5.3 and 5.4 respectively. The proposed 3L-HB APF topology is presented in Section 5.5. With each topology, its corresponding DC-link voltage regulation is also explained. In Section 5.6, the simulation results and RT-Lab real-time results are presented, along with simultaneous comparison of the topologies in terms of topological features and performance under ideal and non-ideal supply conditions. Finally, the concluding section gives a summary of this chapter.

5.2. Split-Capacitor (2C) Topology

The APF system configuration with split-capacitor VSI topology is depicted in Figure 5.2. It utilizes the least number of power semiconductor devices among the four three-phase

four-wire topologies being discussed in this chapter. The VSI is a conventional three-leg six-switch structure, with the neutral wire being connected to the mid-point of a split capacitor. Therefore, the DC-link capacitors in turn provide a path for the flow of whole neutral current. Switching pulses for VSI are generated with the help of hysteresis PWM control, thereby making the inverter behave as a controlled current source. Few higher order harmonics are present at the output of VSI, as a result of high frequency switching. These can be passed through a small RC high-pass filter (R_F, C_F) as shown in the figure.

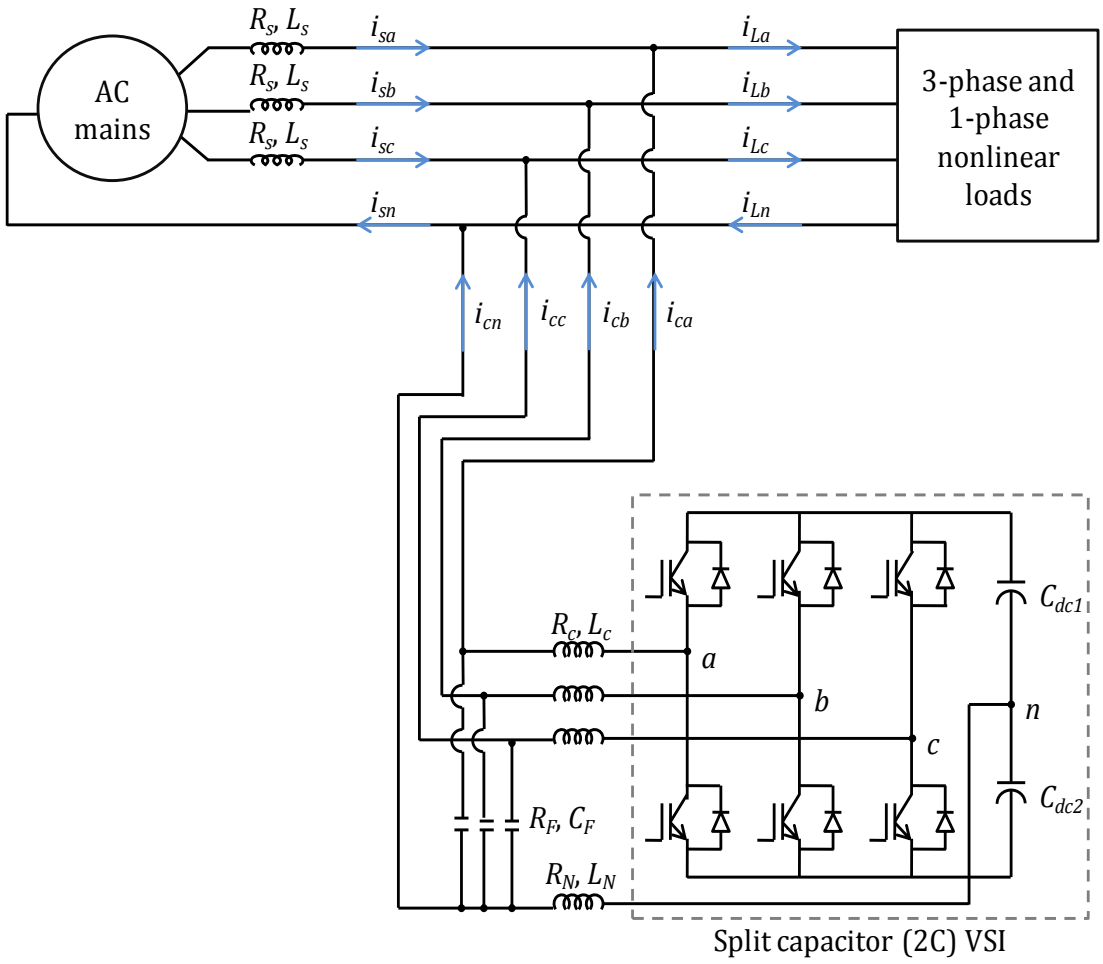


Figure 5.2: System configuration of split-capacitor (2C) VSI based shunt APF

The presence of split-capacitor in this topology demands the voltages across each capacitor to be equal. Otherwise, this unbalanced DC-bus voltages give rise to DC circulating currents, which consequently affect the compensation action. Voltages across the capacitors can be determined with the help of two voltage sensors by either (a) one

sensor each for both the capacitors or (b) one to sense the voltage across one capacitor, and the other to find out the total DC-bus voltage.

The minimum DC-bus voltage for 2C topology is given by following equation [101], [105].

$$V_{dc(\min)} = \frac{\sqrt{3} \times \sqrt{2}}{0.87} V_{s(\text{rms})} = 2.815 \times V_{s(\text{rms})} \tag{5.1}$$

The 2C VSI topology behaves as three single-phase VSIs, when the mid-point of split capacitor is grounded. This can be used for compensation of unbalanced load currents [166]. If the filter current of any phase contains zero-sequence harmonics, the neutral current returns through AC neutral wire. The filter current of each phase flows though any one of the switches (upper or lower) of the corresponding inverter leg and any one DC bus capacitor (upper or lower). The flow of this current though switches and capacitors can be in both directions; which decides the charging or discharging of a certain capacitor. The following table referred from [38] shows the conditions for charging and discharging of capacitors C_{dc1} and C_{dc2} with filter current of phase-a (i_{ca}).

Table 5.1: Conditions for charging and discharging of capacitors C_{dc1} and C_{dc2}

i_{ca}	$\frac{di_{ca}}{dt}$	Effect on capacitor voltage
$i_{ca} > 0$	$\frac{di_{ca}}{dt} < 0$	Increase in voltage V_{dc1}
$i_{ca} < 0$	$\frac{di_{ca}}{dt} < 0$	Decrease in voltage V_{dc1}
$i_{ca} < 0$	$\frac{di_{ca}}{dt} > 0$	Increase in voltage V_{dc2}
$i_{ca} > 0$	$\frac{di_{ca}}{dt} > 0$	Decrease in voltage V_{dc2}

As seen from Table 5.1, the voltage across C_{dc1} (V_{dc1}) increases and that across C_{dc2} (V_{dc2}) drops off, when the current $i_{ca} > 0$. However, the rise and fall of voltages are not equal, since the rates of change of current $\left(\frac{di_{ca}}{dt}\right)$ are not identical. The similar thing happens

when $i_{ca} < 0$, as the voltage across C_{dc1} (V_{dc1}) decreases and that across C_{dc2} (V_{dc2}) rises. This induces a voltage difference between the two capacitors of split-capacitor.

Let the capacitance values, $C_{dc1} = C_{dc2} = C$.

If capacitor voltages V_{dc1} and V_{dc2} are not balanced, it gives rise to a differential voltage given by,

$$\Delta V_{dc} = \frac{1}{C}\int_0^t (i_{C1} + i_{C2})dt = \frac{1}{C}\int_0^t \left(\frac{V_{dc1} + V_{dc2}}{V_{dc}} i_n\right) dt = -\frac{1}{C}\int_0^t i_n dt \qquad (5.2)$$

In the above expression, the currents through upper DC-bus and lower DC-bus are denoted as i_{C1} and i_{C2} respectively, and i_n represents the neutral current.

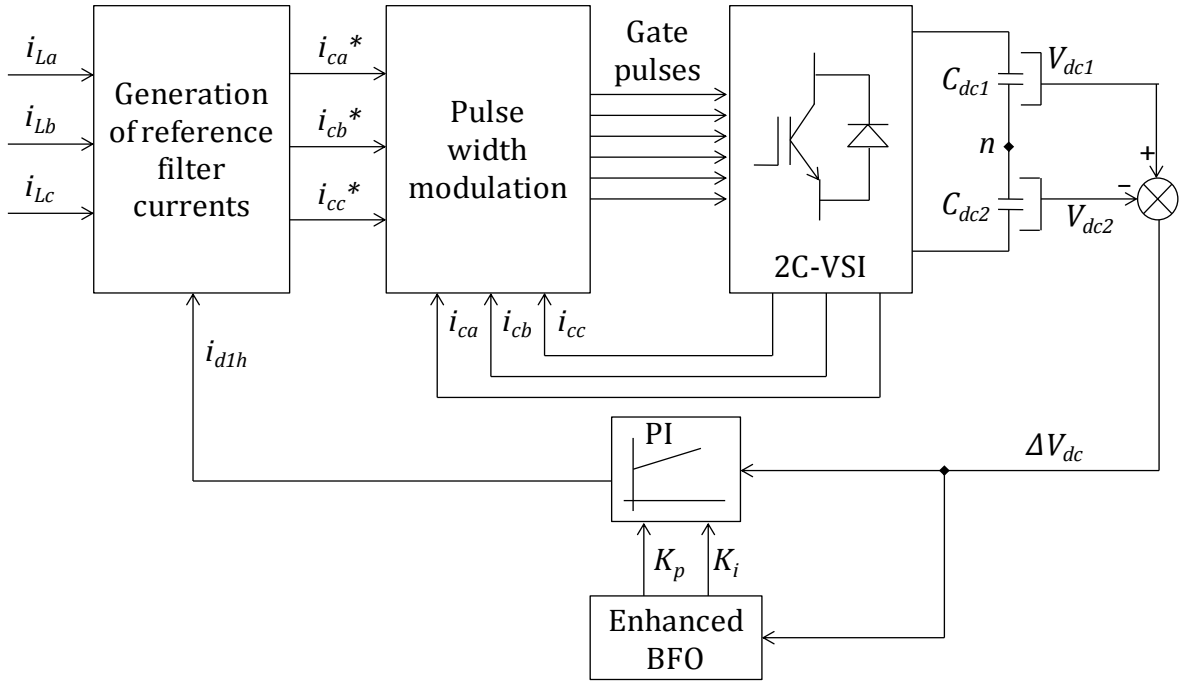


Figure 5.3: Closed loop block diagram for DC-link voltage control in 2C topology

The regulation of DC-link voltage in 2C topology differs from all other topologies discussed thus far. In all other APF topologies, there is only a single DC-link capacitor. Hence, the voltage difference between the actual DC-link voltage and its pre-specified reference needs to be minimized. Alternatively, in 2C topology, difference between the voltages across the two DC bus capacitors needs minimization. Here, the voltage error

($\Delta V_{dc} = V_{dc1} \sim V_{dc2}$) is fed to a PI controller for effective compensation by APF. This is further optimized in this chapter by the implementation of proposed Enhanced BFO algorithm. The closed loop block diagram for DC-link voltage control in 2C topology of APF is presented in Figure 5.3.

The use of 2C topology is limited owing to its drawback related to complexity of DC-link voltage regulation. The neutral current compensation procedure does not have a direct control; rather the compensation occurs as a result of the algebraic difference of currents injected by the remaining phases. However, this topology is seldom preferred due to the use of less number of semiconductor devices and low switching losses. Also, there is no need of a neutral current sensor. This topology of three-phase four-wire VSI is suitable for low-to-medium voltage and low power applications.

5.3. Four-Leg (4L) Topology

Figure 5.4 illustrates the system configuration of APF employing four-leg (4L) VSI along with the three-phase and single-phase nonlinear harmonic producing loads. An additional fourth leg in this topology is exclusively for neutral current compensation. Since the control of neutral current is direct, a better neutral current compensation is accomplished with this topology than its competitor 2C topology. This topology requires a neutral current sensor. The reference for neutral current on source side ought to be zero. However, the reference neutral compensation current is computed by the addition of compensation currents in individual phases i.e. $i_{cn}{}^{*} = i_{ca}{}^{*} + i_{cb}{}^{*} + i_{cc}{}^{*}$. Utilization of eight semiconductor switches involves some extra cost. This also accounts for additional switching losses in the VSI. There is only one DC-link capacitor (C_{dc}) that controls the flow of real power from DC side to AC side of VSI and maintains a constant DC voltage.

The minimum DC-bus voltage for 4L topology can be given by (5.3) [101], [105].

$$V_{dc(\min)} = \sqrt{3} \times \sqrt{2} \times V_{s(\mathrm{rms})} = 2.45 \times V_{s(\mathrm{rms})} \tag{5.3}$$

As indicated from (5.1) and (5.3), a relatively smaller capacitor is required in case of 4L topology compared to 2C-VSI [104].

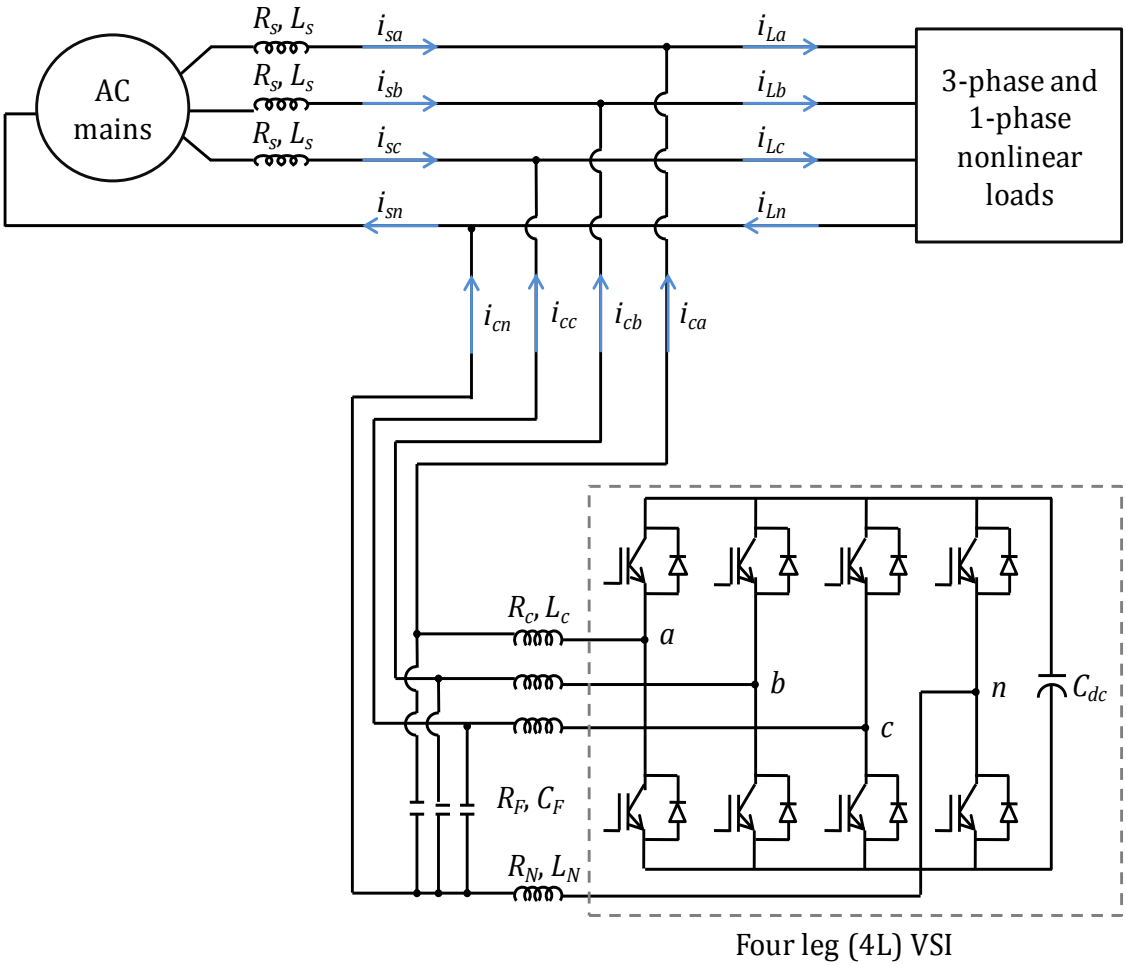


Figure 5.4: System configuration of four-leg (4L) VSI based shunt APF

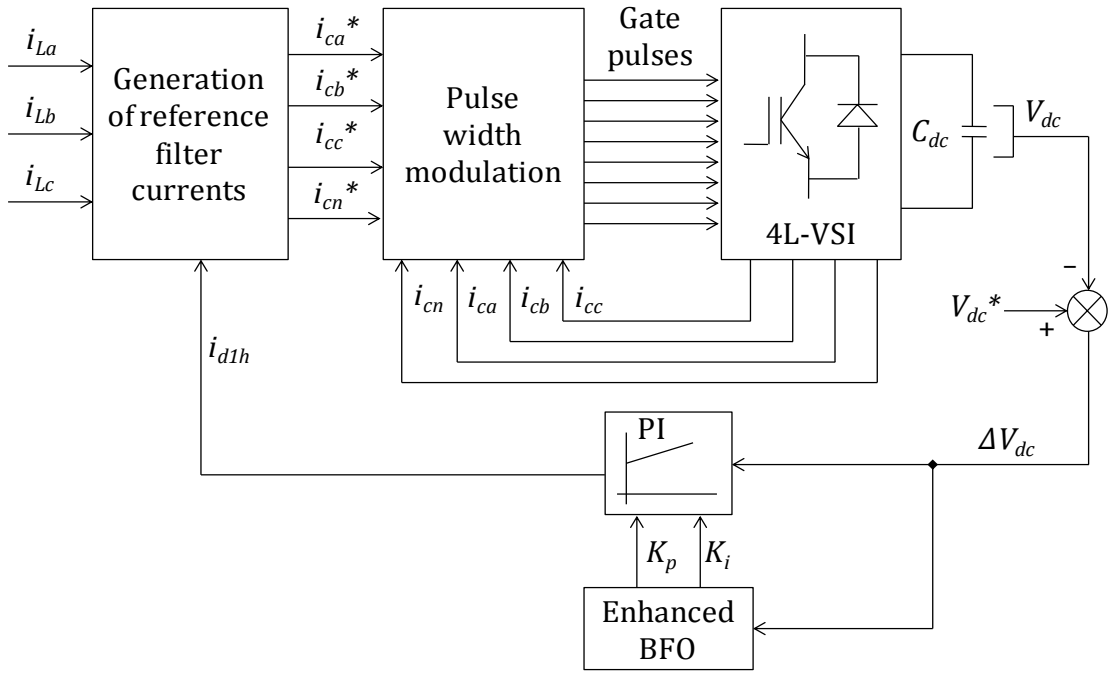


Figure 5.5: Closed loop block diagram for DC-link voltage control in 4L topology

Higher order harmonics generated in 4L-VSI due to frequent switching of semiconductor devices can be eliminated by the use of RC high-pass filter (R_F, C_F) as shown in Figure 5.4. An Enhanced BFO based optimized PI controller is used for minimization of DC-link voltage error. The closed loop control of inverter DC-link voltage using Enhanced BFO is depicted in Figure 5.5. Thereby, it also minimizes the power losses occurring inside VSI. This topology requires a single DC voltage sensor for obvious reasons.

Thus, the 4L-VSI has simple DC-link voltage control, requires small DC-bus capacitor, and the control scheme is also quite simple to implement. However, the cost for extra two switches and corresponding control circuitries are the disadvantages. It is preferred in low voltage and low-to-medium power applications, as many researchers have appointed this topology as the most proficient alternative to be implemented on shunt APFs [38], [47], [105]. Implementation of 4L-VSI on shunt APF is already illustrated in Chapter 2.

5.4. Three H-Bridges (3HB) Topology

Figure 5.6 depicts the system configuration of 3HB-VSI based shunt APF. This topology was first introduced by Dell'Aquila and Lecci in the year 2002 [108] and its use has been further reported in References [101] and [106]. The fundamental aspect of this topology involves the use of twelve semiconductor switches. Here, three single-phase H-bridges are connected to a single DC-link capacitor (C_{dc}). This topology can guarantee improved APF performance, as each phase of the three-phase four-wire system can be controlled independently, irrespective of the other remaining phases.

In contrast with 2C and 4L VSIs, here the maximum voltage appearing across DC-link capacitor is just a single-phase voltage, and not three-phase voltage. Hence, the DC-link capacitor is subjected to a voltage that is further lesser than the 4L-VSI by a factor of $\sqrt{3}$.

The minimum DC-bus voltage for 3HB topology can be given as follows [101], [105].

$$V_{dc(\min)} = \sqrt{2} \times V_{s(\text{rms})} = 1.414 \times V_{s(\text{rms})} \tag{5.4}$$

Thus, it can be concluded that though 3HB-VSI requires more number of semiconductor devices, the rating and cost of inverter switches are reduced to some extent.

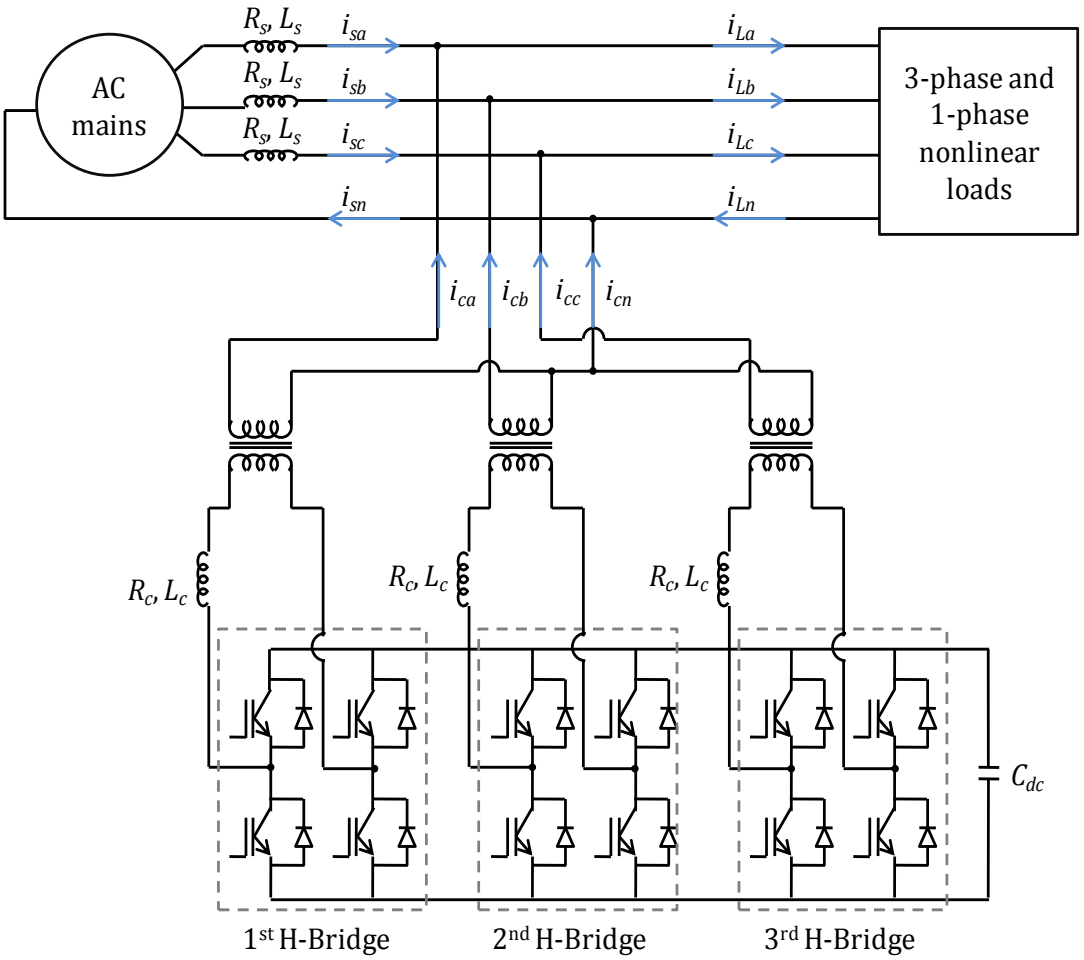


Figure 5.6: System configuration of three H-bridges (3HB) VSI based shunt APF

Since the 3HB VSI is comprised of twelve number of semiconductor devices compared to six switches in case of conventional 2-level VSIs, it suffers from heavy switching power loss. This accounts for a significant amount of the total power loss in the APF system. This can be minimized by maintaining the voltage across DC-link capacitor at a constant reference value ($V_{dc}{}^{*}$). A PI controller whose gains are optimized using the proposed Enhanced BFO technique is employed for this purpose, as shown in Figure 5.7.

The generated compensation currents are injected into the AC lines at PCC via series passive filter (R_c, L_c). The amplitude and frequency of switching ripples generated due to more number of switching devices and frequent switching operations are limited at the output of APF with the help of this filter. The 3HB-VSI topology does not require any additional DC-bus voltage sensor or neutral current sensor. There is no direct control over neutral current in this topology. As seen from the system configuration, the 3HB-

VSI can't be connected to the AC lines directly; rather it makes use of three single-phase isolation transformers. This particular four-wire topology is suitable for high voltage and medium-to-high power applications.

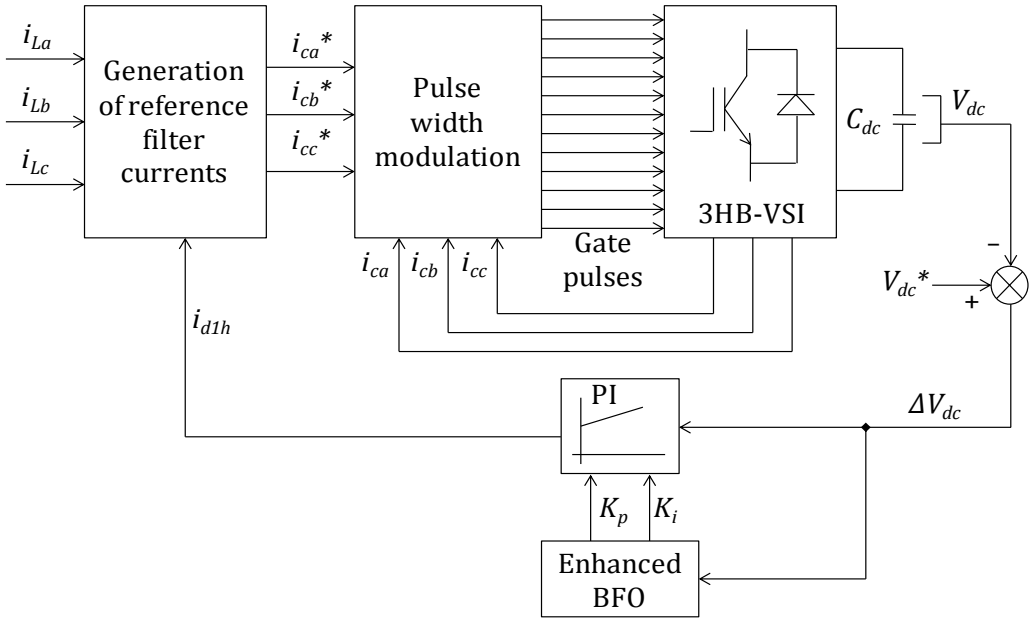


Figure 5.7: Closed loop block diagram for DC-link voltage control in 3HB topology

5.5. Three-Level H-Bridge (3L-HB) Topology

The 2-level VSIs are predominantly used as APFs in three-phase power systems. However, for medium-voltage applications, 3-level VSIs have been proven to be far superior compared to the conventional 2-level inverters in both three-wire and four-wire APFs [102]–[104], [167]. Unlike three-phase three-wire systems, MLI of level more than three, can't be used in four-wire systems, as it may lead to unbalance in neutral potential [109]. The 3-level VSI topology proposed here in fact belongs to the cascaded H-bridge type of MLI discussed in Chapter 4. Few works involving cascaded MLI has been reported on universal power conditioning of power systems, especially for medium-voltage systems [98], [145].

Various advantages offered by 3-level VSIs over 2-level VSIs are: (a) lesser harmonic distortion in the inverter output voltage/current, (b) more suitable for use in higher voltage applications, (c) lower switching frequency, and (d) reduced power loss. It also

costs less, and provides better performance, less electromagnetic interference (EMI), and higher efficiency than 2-level VSIs for power line conditioning applications i.e. both series and shunt compensation [95]. The cascaded HB inverter has inherent self-balancing characteristics. A simple control scheme ensuring DC voltage balance has been proposed for reactive and harmonic compensation in [144].

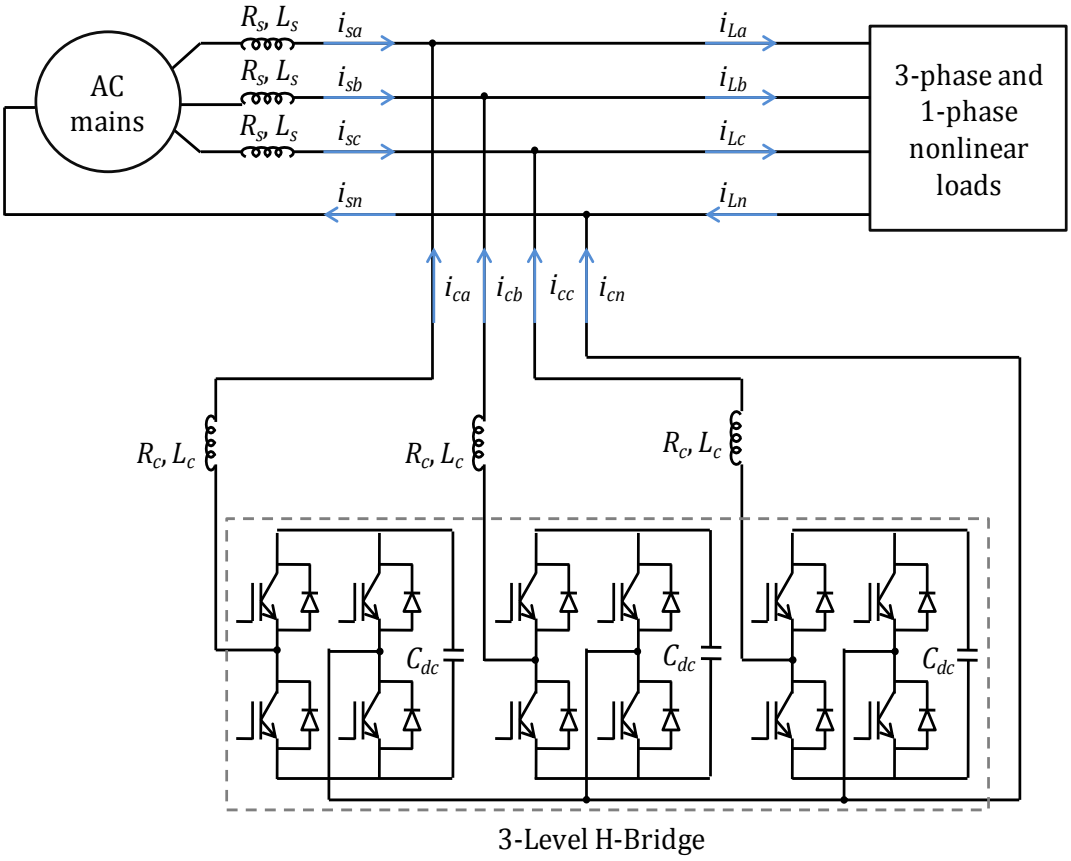


Figure 5.8: System configuration of three-level H-bridges (3L-HB) VSI based shunt APF

The system configuration of 3L-HB APF topology is presented in Figure 5.8. Each DC-link capacitor (C_{dc}) is connected to a single-phase H-bridge inverter. As a result, each H-bridge of the 3-level inverter generates a quasi-square wave with 3-level outputs, $+V_{dc}$, 0 and $-V_{dc}$. Harmonic content of output voltage in case of 3-level VSI is very less compared to 2-level VSI. Moreover, modular structure of H-bridges makes the manufacturing process simple, cheap and quick. This VSI can make direct connection with distribution lines without the use of any additional transformers. In high power applications, an additional passive power filter is required at the output of VSI in order to filter out the

harmonics produced by it. This is due to the fact that the switching frequency of semiconductor devices is limited to a fraction of kilohertz [103], [168]. A series passive filter (R_c, L_c) is used for coupling it to the AC system. As evident from Figure 5.8, there is no direct control over neutral current compensation. This topology provides superior neutral current compensation compared to 2C and 3HB APF topologies.

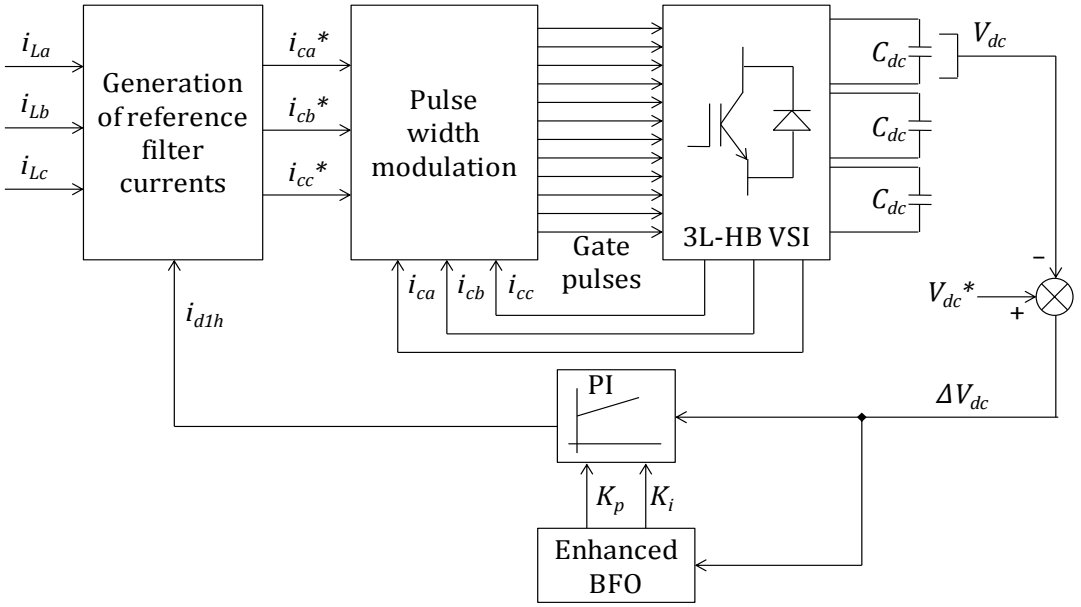


Figure 5.9: Closed loop block diagram for DC-link voltage control in 3L-HB topology

To control the average voltage of all three DC-link capacitors of 3L-HB configuration, only one capacitor voltage needs to be tracked and fed back [145]. Therefore, this lessens the complexity of voltage regulation of all the capacitors, reduces the necessity of voltage sensors and increases the reliability. 3L-HB topology of three-phase four-wire VSI operates in similar manner as 3-level cascaded MLI topology of three-phase three-wire VSI discussed in the previous chapter. The PI controller for DC-link voltage regulation is optimized using the Enhanced BFO approach here as well, as shown in Figure 5.9.

As it involves more number of semiconductor switches i.e. twelve; the cost of 3L-HB topology is definitely more than its 2-level counterparts 2C and 4L VSIs. Though both 3HB and 3L-HB topologies use twelve switches, overall cost of 3L-HB is lesser as it does not require any coupling transformer. According the research paper [169], if power loss savings are taken into account, the life-cycle cost of 3-level VSI is a considerable option

over 2-level VSIs (2C and 4L); though initial cost of the former is slightly more. It is also reported that, the power loss savings at 0.2 p.u. is around 50 to 55% more than 2-level inverters. Similarly at 1 p.u., it is 25% more than 2-level VSIs. A paper by Vodyakho and Kim [104] specifies that, using a 3-level converter, the switching frequency component of common-mode voltage gets reduced by 25 to 30%, which in turn has an impact on the size of inductor. This topology of three-phase four-wire VSI finds its use in high voltage and medium-to-high power applications.

5.6. Results and Discussion

Investigations are carried out with the help of simulations and RT-Lab, the system configuration being same as Figure 2.10. However, here the harmonics and unbalance are generated using a single-phase and a three-phase nonlinear load. The single-phase load is a diode rectifier with series connection of L with a parallel R and C connected at its DC-side. And, the three-phase load is a diode rectifier with a series RL load connected at its DC-side. The three-phase four-wire APF system is simulated taking one out of the 2C, 4L, 3HB and 3L-HB VSIs at a time,. The APF control scheme opted here is $i_d - i_q$ scheme. In 2C, 3HB and 3L-HB VSIs, the reference filter currents for three wires ($i_{ca}{}^*, i_{cb}{}^*, i_{cc}{}^*$) are generated; whereas in 4L-VSI an additional reference compensation current for neutral wire is computed ($i_{cn}{}^* = i_{ca}{}^* + i_{cb}{}^* + i_{cc}{}^*$). Here, simulation results for load currents, compensation currents and source currents in all three phases are provided because, the harmonic compensation is not identical in all phases, due to the presence of single-phase load, resulting in unbalanced loading and unequal harmonic content in all phases.

5.6.1. Simulation results

The simulation results for supply voltage (V_s), load current (i_L), filter current (i_c), neutral current (i_n) and source currents after compensation with APF employing 2C-VSI (i_{s1}), 4L-VSI (i_{s2}), 3HB-VSI (i_{s3}) and 3L-HB VSI (i_{s4}) under ideal, distorted and unbalanced supply conditions are presented in Figures 5.10, 5.11 and 5.12 respectively.

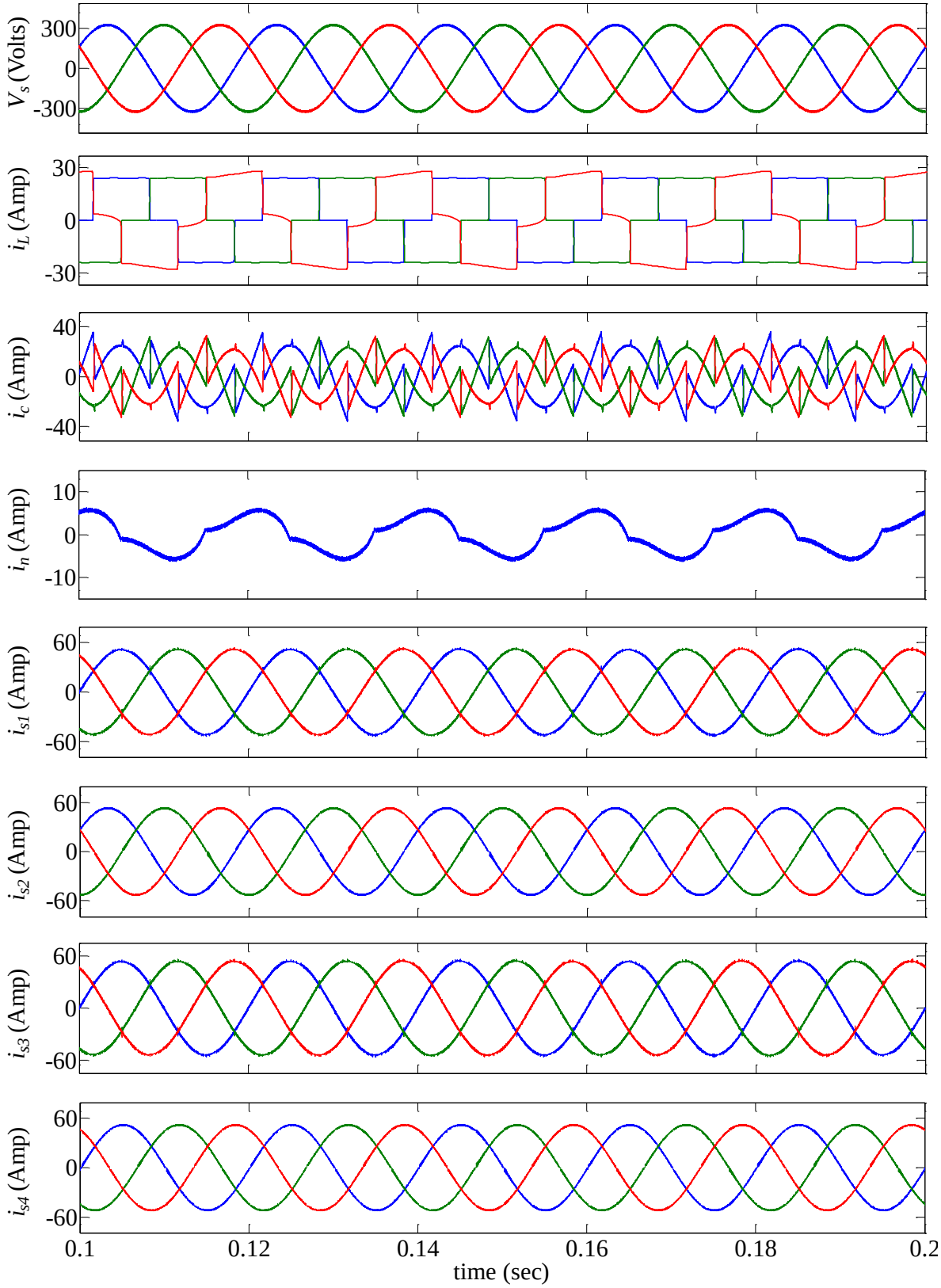


Figure 5.10: Simulation results for supply voltage (V_s), load current (i_L), filter current (i_c), neutral current (i_n) and source currents after compensation with APF employing 2C-VSI (i_{s1}), 4L-VSI (i_{s2}), 3HB-VSI (i_{s3}) and 3L-HB VSI (i_{s4}) under ideal supply

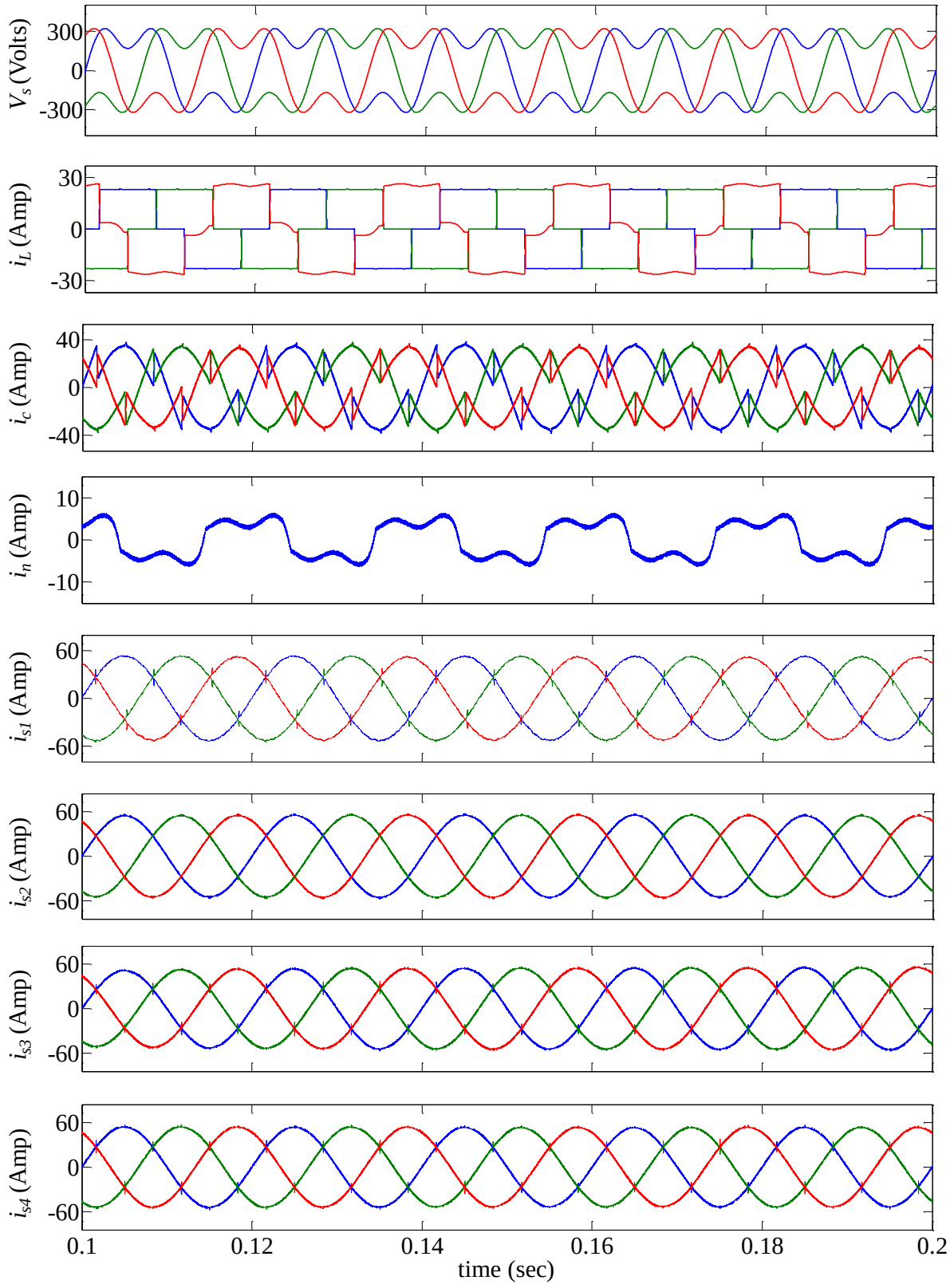


Figure 5.11: Simulation results for supply voltage (V_s), load current (i_L), filter current (i_c), neutral current (i_n) and source currents after compensation with APF employing 2C-VSI (i_{s1}), 4L-VSI (i_{s2}), 3HB-VSI (i_{s3}) and 3L-HB VSI (i_{s4}) under distorted supply

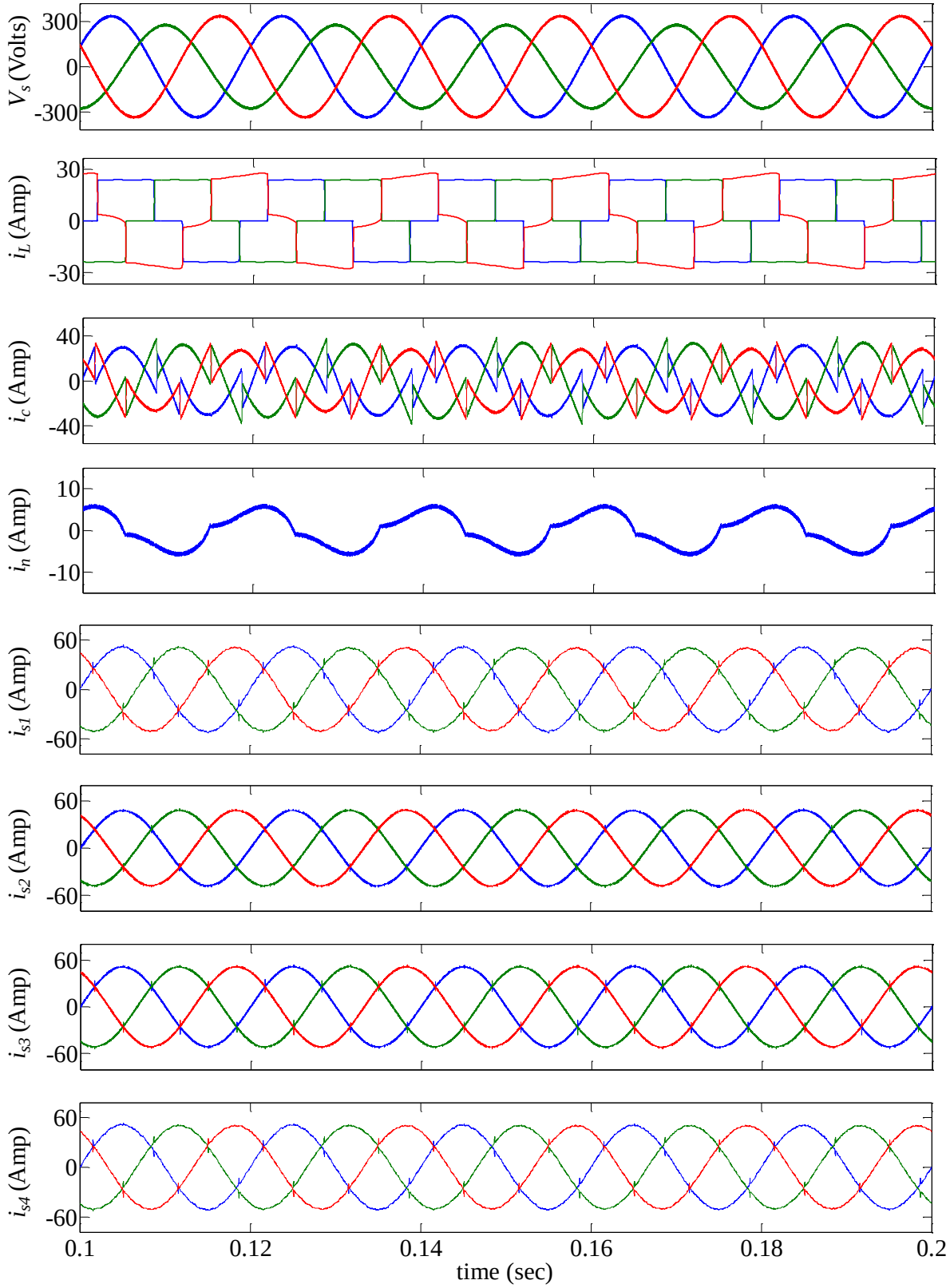
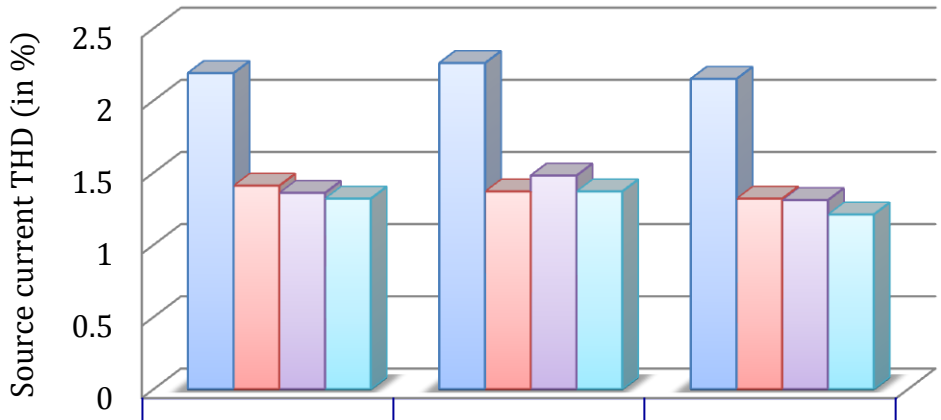
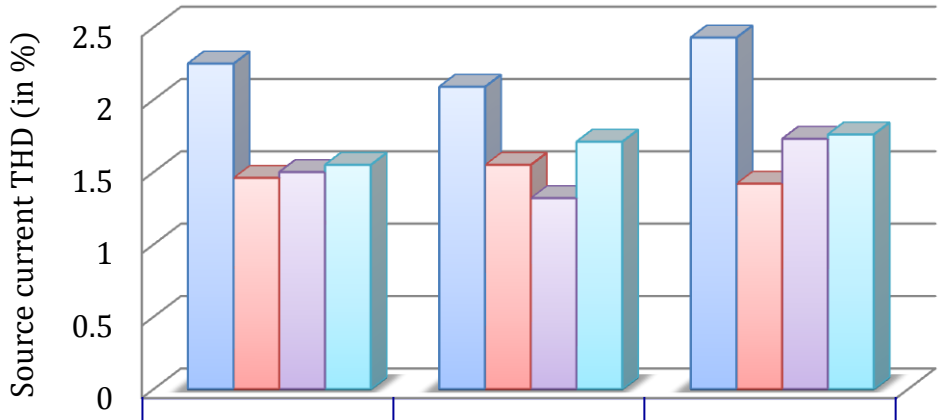


Figure 5.12: Simulation results for supply voltage (V_s), load current (i_L), filter current (i_c), neutral current (i_n) and source currents after compensation with APF employing 2C-VSI (i_{s1}), 4L-VSI (i_{s2}), 3HB-VSI (i_{s3}) and 3L-HB VSI (i_{s4}) under unbalanced supply



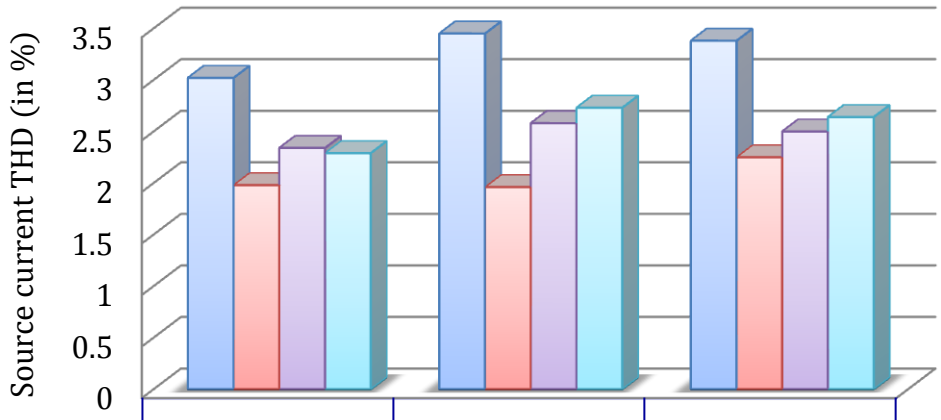
	Phase - a	Phase - b	Phase - c
2C VSI based APF	2.19	2.26	2.15
4L VSI based APF	1.41	1.37	1.32
3HB VSI based APF	1.36	1.48	1.31
3L-HB VSI based APF	1.32	1.37	1.21

Figure 5.13: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing 2C, 4L, 3HB and 3L-HB VSI topologies under ideal supply condition



	Phase - a	Phase - b	Phase - c
2C VSI based APF	2.25	2.09	2.43
4L VSI based APF	1.46	1.55	1.42
3HB VSI based APF	1.5	1.32	1.73
3L-HB VSI based APF	1.55	1.71	1.76

Figure 5.14: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing 2C, 4L, 3HB and 3L-HB VSI topologies under distorted supply condition



	Phase - a	Phase - b	Phase - c
2C VSI based APF	3.02	3.45	3.38
4L VSI based APF	1.98	1.96	2.25
3HB VSI based APF	2.34	2.58	2.5
3L-HB VSI based APF	2.29	2.73	2.64

Figure 5.15: Chart diagram showing source current THDs (in %) obtained with simulation of APF employing 2C, 4L, 3HB and 3L-HB VSI topologies under unbalanced supply condition

The THDs in phases a, b and c of load current were found out to be 29.58%, 29.65% and 23.29% respectively when the supply voltage was ideal. Correspondingly, source current THDs were 29.55%, 29.59% and 24.07% when non-sinusoidal supply was considered for simulation. And, THDs under unbalanced supply were found out to be 29.37%, 30.92% and 22.18% respectively. Chart diagrams of Figures 5.13 – 5.15 show source current THDs (in %) after compensation with 2C, 4L, 3HB and 3L-HB APFs.

5.6.2. RT-Lab results

The RT-Lab results for supply voltage (V_s), load current in four wires ($i_{La}, i_{Lb}, i_{Lc}, i_{Ln}$), compensation current (i_{ca}, i_{cb}, i_{cc}), DC-link voltage (V_{dc}) and source currents after compensation with 2C APF (i_{s1}), 4L APF (i_{s2}), 3HB APF (i_{s3}) and 3L-HB APF (i_{s4}) under various supplies are presented in Figures 5.16 - 5.18. System and optimization parameters are exactly same as that considered during simulations.

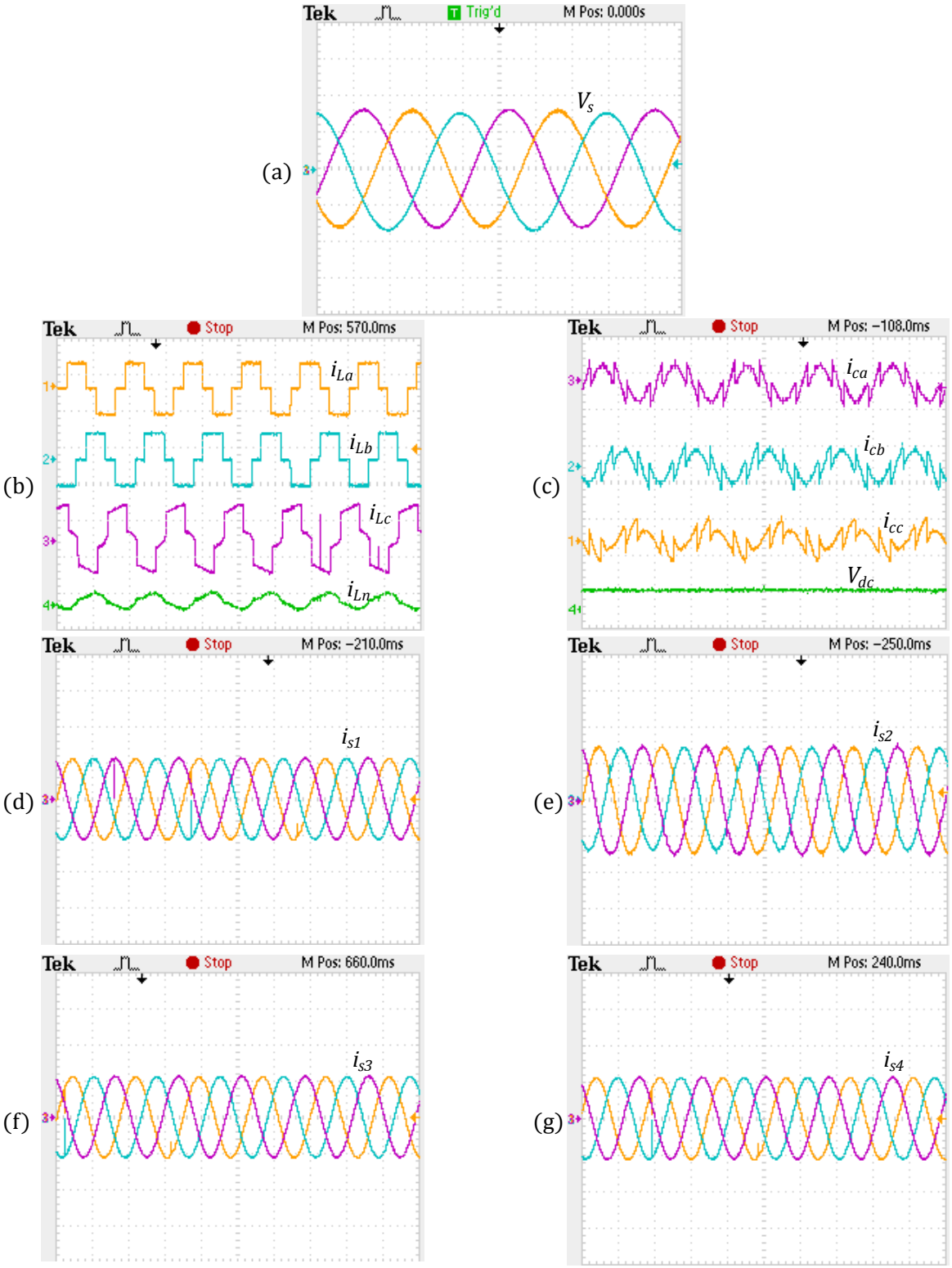


Figure 5.16: RT-Lab results under ideal supply for **(a)** Supply voltage [scale: 200 V/div], **(b)** Load current in four wires [scale: 40 A/div], **(c)** Compensation current in three phases [scale: 40 A/div] and DC-link voltage [scale: 2000 V/div], **(d)-(g)** Source currents after compensation with 2C APF (i_{s1}) [scale: 40 A/div], 4L APF (i_{s2}) [scale: 35 A/div], 3HB APF (i_{s3}) [scale: 40 A/div] and 3L-HB APF (i_{s4}) [scale: 40 A/div] respectively

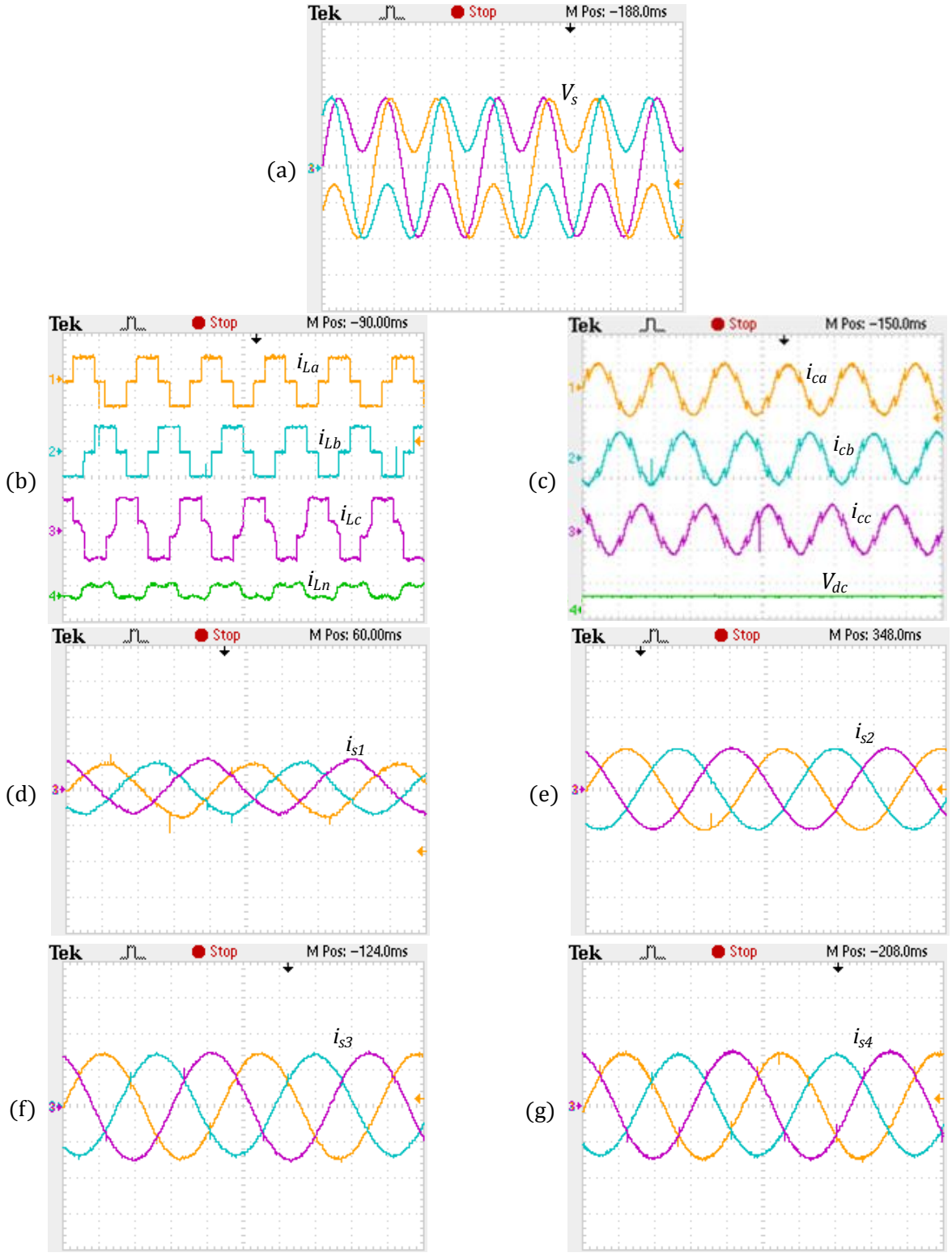


Figure 5.17: RT-Lab results under distorted supply for **(a)** Supply voltage [scale: 150 V/div], **(b)** Load current in four wires [scale: 40 A/div], **(c)** Compensation current in three phases [scale: 40 A/div] and DC-link voltage [scale: 2500 V/div], **(d)-(g)** Source currents after compensation with 2C APF (i_{s1}) [scale: 70 A/div], 4L APF (i_{s2}) [scale: 40 A/div], 3HB APF (i_{s3}) [scale: 35 A/div] and 3L-HB APF (i_{s4}) [scale: 35 A/div] respectively

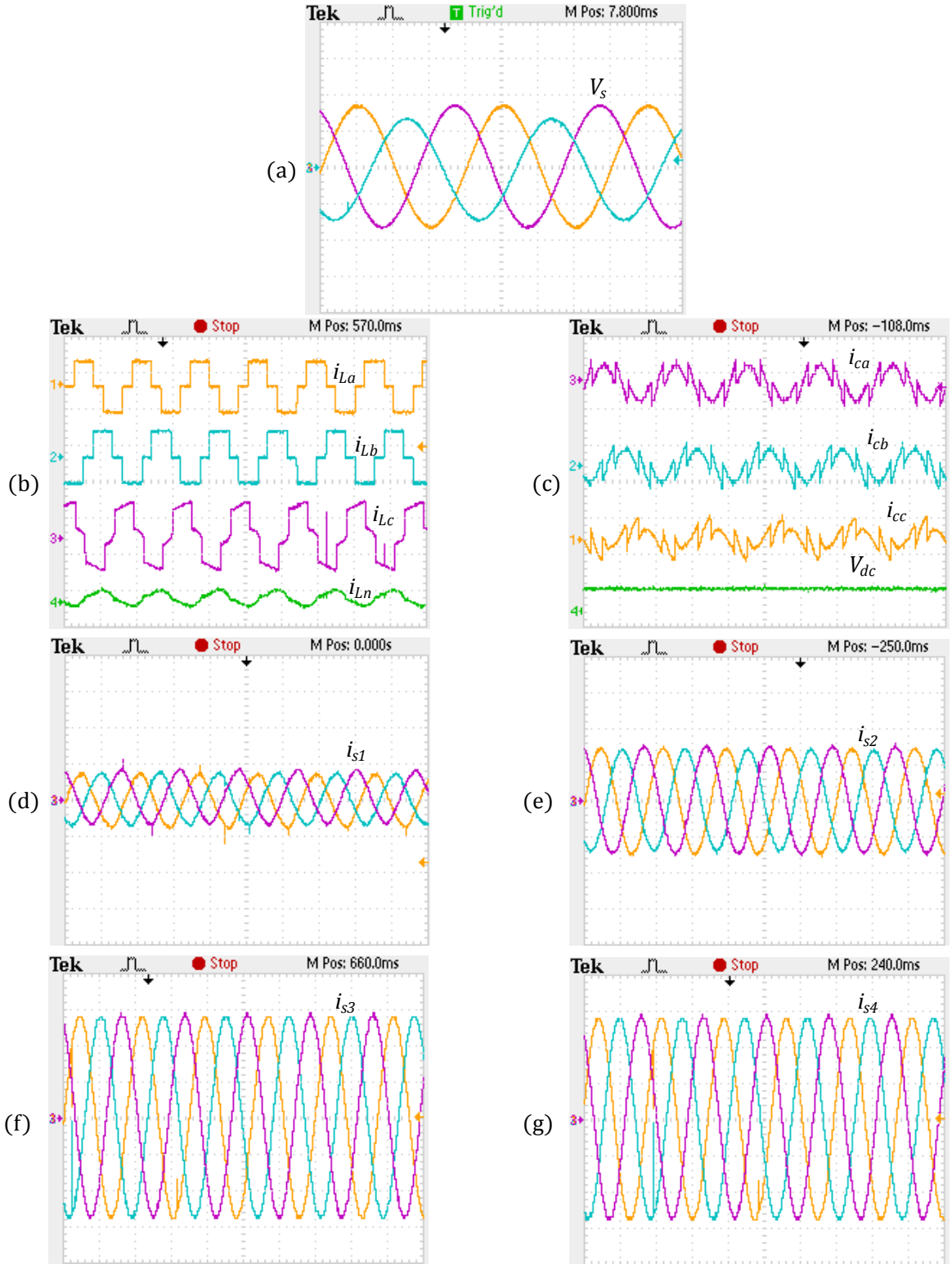
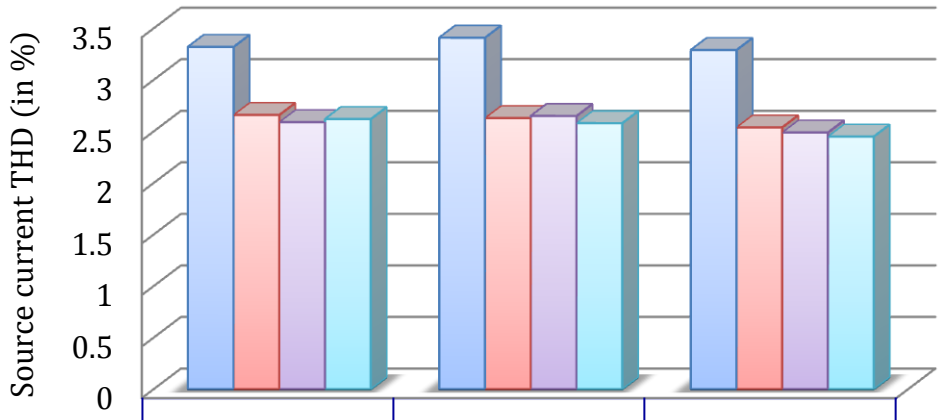
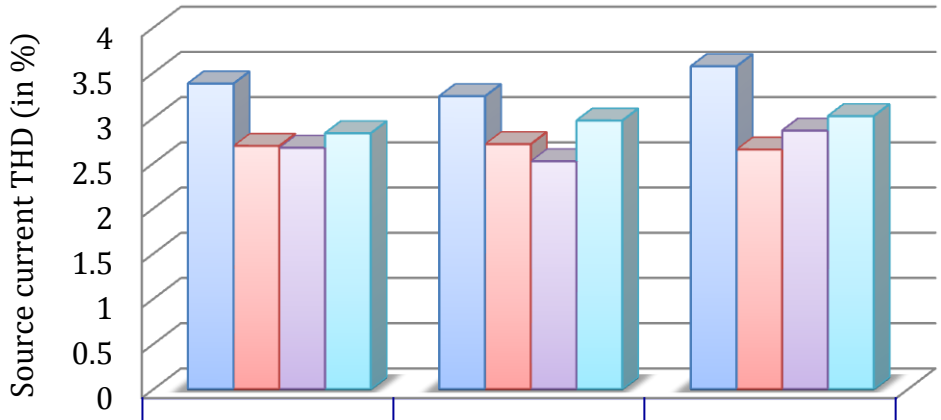


Figure 5.18: RT-Lab results under unbalanced supply for **(a)** Supply voltage [scale: 200 V/div], **(b)** Load current in four wires [scale: 40 A/div], **(c)** Compensation current in three phases [scale: 40 A/div] and DC-link voltage [scale: 1500 V/div], **(d)-(g)** Source currents after compensation with 2C APF (i_{s1}) [scale: 70 A/div], 4L APF (i_{s2}) [scale: 35 A/div], 3HB APF (i_{s3}) [scale: 18 A/div] and 3L-HB APF (i_{s4}) [scale: 18 A/div] respectively



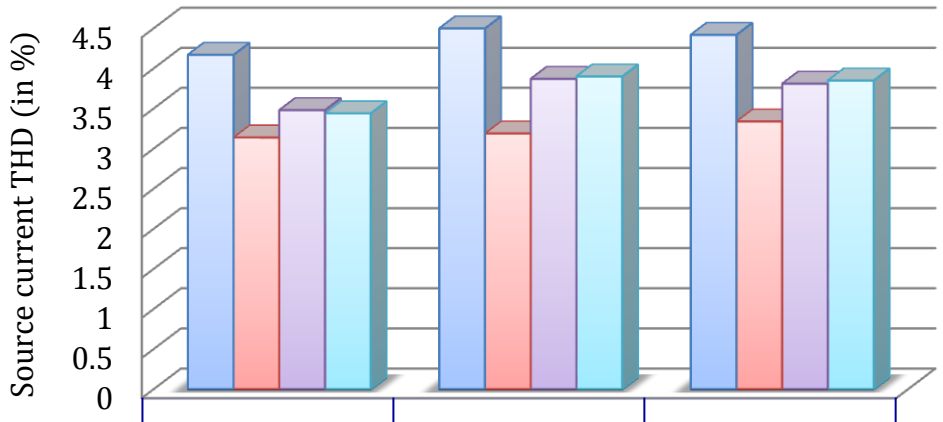
	Phase - a	Phase - b	Phase - c
2C VSI based APF	3.32	3.41	3.29
4L VSI based APF	2.66	2.63	2.54
3HB VSI based APF	2.59	2.65	2.49
3L-HB VSI based APF	2.62	2.58	2.45

Figure 5.19: Chart diagram showing source current THDs (in %) obtained in RT-Lab after compensation with APFs employing 2C, 4L, 3HB and 3L-HB VSI topologies under ideal supply condition



	Phase - a	Phase - b	Phase - c
2C VSI based APF	3.38	3.24	3.57
4L VSI based APF	2.69	2.71	2.65
3HB VSI based APF	2.67	2.52	2.86
3L-HB VSI based APF	2.83	2.97	3.02

Figure 5.20: Chart diagram showing source current THDs (in %) obtained in RT-Lab after compensation with APFs employing 2C, 4L, 3HB and 3L-HB VSI topologies under distorted supply condition



	Phase - a	Phase - b	Phase - c
2C VSI based APF	4.17	4.5	4.42
4L VSI based APF	3.14	3.19	3.34
3HB VSI based APF	3.48	3.87	3.81
3L-HB VSI based APF	3.44	3.9	3.85

Figure 5.21: Chart diagram showing source current THDs (in %) obtained in RT-Lab after compensation with APFs employing 2C, 4L, 3HB and 3L-HB VSI topologies under unbalanced supply condition

The THDs in *a*, *b* and *c* phases of load current obtained with RT-Lab are: 30.83%, 30.86% and 24.04% under ideal supply; 30.82%, 30.84% and 25.16% under distorted supply; and 30.64%, 32.85% and 23.04% under unbalanced supply respectively. These also specify the THD of source current before compensation. From the Figures 5.19 – 5.21, it is observed that with the use of 2C, 4L, 3HB and 3L-HB APF topologies, the THD in all phases of source current could be brought down to less than 5% under all kinds of supply.

As the THD charts of Figures 5.13, 5.14, 5.15, 5.19, 5.20 and 5.21 indicate, there is no particular order in which the VSI topologies can be ranked based on their performance in harmonic compensation. All the VSI topologies are capable of bringing down the source current THD below 5%. However, the harmonic content in source currents obtained after compensation with 2C topology of APF is the highest under all kinds of supply. Table 5.2 offers a comparison between the topological features, cost, compensation effectiveness and area of application of the 2C, 4L, 3HB and 3L-HB VSIs.

Table 5.2: Comparison between 2C, 4L, 3HB and 3L-HB VSI topologies of shunt APF

Feature	2C-VSI	4L-VSI	3HB-VSI	3L-HB VSI
No. of semiconductor devices	6	8	12	12
DC-bus capacitors	2	1	1	3
Additional sensor requirement	1 more DC-bus voltage sensor	1 more neutral current sensor	None	None
Need of coupling transformer	Not required	Not required	Required	Not required
Neutral current compensation	Indirect	Direct	Indirect	Indirect
Effectiveness in neutral current compensation	May degrade due to voltage difference between the two capacitors	Better than 2C and 3HB	Better than 2C	Better than 2C and 3HB
Source current THD	Less than 5%	Less than 5%	Less than 5%	Less than 5%
Overall cost	Lowest	Higher than 2C	Highest	Less than 3HB
Application	Low to medium power applications	Low to medium power applications	High voltage, medium to high power applications	High voltage, medium to high power applications

5.7. Summary

The chapter presents a review of various three-phase four-wire APF topologies such as 2C, 4L, 3HB and 3L-HB, taking into account the constraints related to DC-link voltage regulation for each topology. Enhanced BFO is implemented for effective harmonic compensation by the shunt APF. An extensive analysis of the four mentioned topologies is carried out focusing on the disturbances generated due to nonlinear and unbalanced loads in three-phase four-wire systems. For a nonlinear load drawing a current having THD nearly 30% in the absence of APF, is brought down to drastically small values (less than 5%) by the use of these topologies of APFs, thereby following the IEEE-519 Standard Recommendations on harmonic limits. The 4L topology could be a better choice for superior performance in low-to-medium-power applications, whereas, for the same applications with slight compromise on performance, the low cost 2C topology would be more appropriate. Similarly, for high-voltage, medium-to-high power applications, both 3HB and 3L-HB topologies are promising candidates. The choice of a particular topology indicates a compromise over cost, solution quality and suitability for low/high voltage, low/medium/high power applications.

Chapter 6

Thesis Contributions, General Conclusions, And Scope for Future Research

6.1. Thesis Contributions

The following is a brief outline of the contributions in this thesis.

1) Comparison of the load compensation capabilities of $p-q$, modified $p-q$ and i_d-i_q control schemes for shunt APF under non-ideal supply, sudden load change and unbalanced loading conditions
2) Design of an optimal DC-link voltage regulator using PSO
3) Design of an optimal DC-link voltage regulator using BFO
4) Development of an Enhanced BFO algorithm by the hybridization of PSO and BFO
5) Design of an optimal DC-link voltage regulator using Enhanced BFO and its comparison with conventional, PSO-based and BFO-based controllers under a range of supply and sudden load change conditions
6) Modelling, development and performance optimization of three-phase three-wire shunt APFs employing cascaded 3, 5, 7 and 9-level MLIs to showcase the potential advantages of MLI over conventional 2-level VSIs
7) Modelling, development and performance optimization of various three-phase four-wire APF topologies such as 2C, 4L, 3HB and 3L-HB VSIs, followed by topological and performance comparison between them

8) Extensive investigations on the proposed implementation of APF control schemes, optimization techniques and topologies, using simulation studies and real-time analysis in RT-Lab. This illustrates whether the resulting source currents THDs eventually satisfies the IEEE 519-2014 Standard Recommendations on harmonic limits under both ideal and non-ideal supply conditions

6.2. General Conclusions

The sole objective of this thesis being compensation of current harmonics generated due to the presence of nonlinear loads in three-phase three-wire and four-wire power systems, the research studies presented here starts with an introduction to harmonics clearly specifying its causes and consequences. The role of passive power filters in harmonics elimination is discussed. However, the research work presented in this thesis deals with the use of APFs due to the several inevitable drawbacks associated with passive filters. Performances of $p-q$, modified $p-q$ and i_d-i_q strategies are evaluated by comparing the THDs in compensated source currents under ideal supply, non-ideal supply and sudden load change conditions. DC-link voltage regulation with the help of PI controller to minimize the power losses occurring inside APF is studied. Various drawbacks encountered in conventional PI controller under a range of supply and loading conditions are discussed. The subsequent segment of thesis concentrates on the implementation of optimization techniques such as PSO and BFO for optimal tuning of PI controller gains K_p and K_i. However, this also suffers from several shortcomings, resulting in severe deterioration of APF performance. Hence a novel Enhanced BFO algorithm is developed with the combined advantages of PSO and BFO; that could overcome the drawbacks observed in the optimization algorithms when implemented alone. The Enhanced BFO based PI controller outperforms all other approaches discussed here as yet, by yielding the fastest rate of convergence to reach the global optima and the least value of source current THDs. The inverter topology being another indispensable aspect of APF, various topologies for three-phase three-wire systems (two-level and multilevel VSIs) and four-wire systems (2C, 4L, 3HB and 3L-HB VSIs) are analyzed and compared

based on component requirements, compensation effectiveness, cost and area of application. For effective compensation, irrespective of the number and rating of DC-link capacitors used in any particular topology, voltages across them could be successfully maintained constant with optimal regulation of DC-link voltage. The studies when extended towards real-time performance analysis using RT-Lab further validated the simulation results indicating the superiority of proposed approaches.

Investigations performed in this research work yield the following important conclusions.

1) $p-q$ scheme yields poor results under non-ideal supply conditions.

2) Modified $p-q$ scheme though provides comparatively better result under distorted supply condition; it is inefficient when there is unbalance in supply voltage.

3) i_d-i_q scheme is the best control scheme for a wide variety of supply and loading conditions. Source current THD is lowered down satisfactorily below 5% thereby satisfying IEEE-519 Standards. Simultaneously, it compensates for excessive neutral current and unbalanced source current in three-phase four-wire systems.

4) Implementation of PSO to find out the optimized gains K_p and K_i helps in providing improved V_{dc} transient response compared to conventional PI controller in terms of settling time, maximum overshoot and maximum undershoot under all conditions of supply. The overall source current THDs are also brought down to lower values.

5) The simulation results employing BFO conclude that, V_{dc} transient settles down in the smallest time for APF employing BFO compared to conventional and PSO based APFs. Hence BFO technique offers fast prevail over current harmonics. In addition, the overshoots and undershoots in V_{dc} are also the minimum for BFO.

6) Moreover, there are ripples in V_{dc} after reaching the steady state, which is very high for conventional PI controller. Hence there exists a steady-state distortion in the corresponding supply current. PSO is able to lower down the overall THD to a lower level compared to conventional PI controller thereby giving a better DC-link voltage regulation. But this has been minimized to a still lower level using BFO. To sum it up,

the overall THD in source current has been reduced to lower value with the proposed implementation of BFO.

7) An Enhanced BFO algorithm is successfully developed that provides faster convergence to reach the global optima. With this algorithm, the DC-link voltage error is minimized in the smallest amount of time (approximately one cycle) irrespective of the supply condition. Additionally, source current THDs are lowered down to negligibly small values. Adequate results are provided to validate that Enhanced BFO outperforms the discussed PSO and BFO techniques.

8) Cascaded MLI topology of shunt APF for current harmonic mitigation is realized for three-phase three-wire system. With increase in the number of levels as 3, 5, 7 and 9, the distortion in source current reduces to negligibly small amount. APF employing cascaded 9-level MLI and Enhanced BFO, yields the lowest values of source current THDs irrespective of supply conditions.

9) Comparative analysis of three-phase four-wire APF topologies; 2C, 4L, 3HB and 3L-HB indicate that, 4L topology could be a better choice for superior performance in low-to-medium power applications, whereas for the same applications with slight compromise on performance, the low cost 2C VSI would be more appropriate. Similarly, for high-voltage medium-to-high power applications, 3L-HB is a promising candidate. The choice of a particular topology indicates a compromise over cost, solution quality and suitability for low/high voltage, low/medium/high power applications. However, all these APF topologies are capable of limiting the THD to permissible values (less than 5%) under all kinds of supply conditions.

6.3. Scope for Future Research

Research work presented in this thesis can be extended in following dimensions in future.

1) Experimental investigations can be done on shunt active power filter by developing prototype models in the laboratory to verify the effectiveness of various control schemes, controllers and topologies.

2) The Enhanced BFO algorithm can be applied to other fields of research to find out a global optimum solution.

3) There are several other recent optimization techniques like Cuckoo search, Firefly algorithm, Bat algorithm, Seeker optimization and Flower pollination algorithm that can be applied to this problem of power conditioning.

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Thesis Disseminations

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