B.Tech Project 2014-15

Department Of Electrical Engineering

NIT Rourkela

Project Thesis

Designing a Forward Convertor with Transformer Reset and Synchronous Rectification

Project In-Charge

Prof. Susovon Samanta

By

Raj Kishore Das (111EE0206)

CERTIFICATE

Department of Electrical Engineering

National Institute of Technology, Rourkela

This is to certify that the work in the thesis entitled Designing a Forward Convertor with Transformer Reset and Synchronous Rectification by Raj Kishore Das is a record of an original research work carried out under my supervision and guidance in partial fulfilment of the requirements for the award of the degree of Bachelor of Technology in Electrical Engineering. Neither this thesis nor any part of it has been submitted for any degree or academic award elsewhere.

.

Susovon Samanta
Assistant Professor,
Dept of Electrical Engineering,
NIT Rourkela

Acknowledgement

I avail this opportunity to express my hereby indebtedness, deep gratitude and sincere thanks to my guide, Mr. Susovon Samanta, Assistant Professor, Electrical Engineering Department for his in depth supervision and guidance, constant encouragement and co-operative attitude for bringing out this thesis work.

I extend my sincere thanks to Dr. A.K. Panda, Professor and Head of the Department, Electrical Engineering Department, N.I.T. Rourkela for his valuable suggestions for bringing out this edition in time.

Finally I extend my sincere thanks to all those who have helped me during my dissertation work and have been involved directly or indirectly in my endeavour.

Raj Kishore Das

Roll No- 111EE0206

Contents

ABSTRACT

The use of an active clamp circuit over the famous RCD clamp is due to its superiority for its better efficiency, more duty cycle, lower current stress and no energy dissipation as the magnetising current is recycled and used again. The use of the transformer instead of the normal buck converter is because by using a transformer the voltage can be stepped down to quite a low value, i.e. more than 2 times less of the input voltage which was not possible in the buck converter. The use of synchronous rectification is to increase the efficiency of the system, as the body diode conduction losses are quite low for a Mosfet and thus less heat produced in using that. The circuit for a forward converter with an active clamp and transformer reset is made with the synchronous rectification.

Chapter 1

INTRODUCTION

INTRODUCTION

1.1 SWITCHING OF AN ACTIVE CLAMP

A low side active clamp connection is completed in a full switching cycle of T_0-T_4, which can be shortened and described in 4 intervals.

1. **T_0-T_1 (Transfer of power)**

   Primary Side:-

   - As the main switch is conducting the power is transferred to the secondary.
   - The main switch was turned-on in ZVS condition as the body diode was earlier conducting.
   - The transformer magnetising current and the reflected secondary current make up the primary current that flows through the channel resistance of Qmain.

   Secondary Side:-

   - The forward Synchronous rectifier, Qf was turned on and the full load current is flowing through it.
   - In the earlier case the load current was freewheeling through the body diode of the reverse synchronous rectifier Qr.
   - Thus Qf is suffers some turn-on loss as it is hard switched.

2. **T_1-T_2 (1^{st} Resonant period)**

   This one is the first of the 2 resonant conditions that occur in a full switching cycle.

   Primary Side:-

   - Qmain is turned-off during this period in ZVS condition.
   - But the primary current flows continuously as it is averted through the body diode Daux, of Qaux.

- Because of the direction of the primary current the clamp switch Qaux must be a P-Channel Mosfet.
- There is no reflected primary current, as the secondary load current is freewheeling, so the only current flowing through Daux is the transformer magnetising current.
- The body diode conduction loss of Qaux is minimal and the condition are set for Qaux to turn on under ZVS condition.
- The delay time between Qmain turn-off and Qaux turn-on is known as the resonant period.

Secondary Side:-

- Qf has turned-off under hard switching and the full output load current is now freewheeling through diode of Qr, i.e. Dr.
- The body diode loss is the major reason for power loss in a system.
- But the conduction of the Dr is necessary for the turning-on of Qr under ZVS. So it is preferred to lessening the conduction time of Dr preferably to zero, but still let Qr to turn-on under ZVS condition.

3. T_2-T_3 (Active clamping)

This is the time when the transformer reset occurs. The transition from positive to negative current flow is even, and had begun during earlier state when the magnetising current had reached the maximum positive peak value.

Primary Side:-

- The Qaux is fully turned on under ZVS, and the difference between the clamp capacitor voltage and the input voltage is now applied across primary side of the transformer.
- The Qaux is subjected to nominal conduction loss as the magnetising current is only flowing.

Secondary Side:-

- Full load current is now flowing over the channel resistance of Qr which had turned on under ZVS, and is suffering high conduction losses.

4. T_3-T_4 (2^{nd} Resonant period)

It is the 2nd resonant period that occurs during the full cycle.

Primary Side:-

- The Qaux is turned off under ZVS and the current is now flowing in the body diode Dmain of the main switch Qmain.
- The primary current is flowing in negative direction has started the direction change when the magnetising current reached its max negative value.
- Conduction through the body diode of Qmain initiates, which is necessary for the Qmain to turn on under ZVS.

Secondary Side:-

- Just before Qr turns off the Dr begins to conduct.
- Although Qr turns off under ZVS condition it suffers inevitable power loss due to the conduction of body diode.
- After the completion of T_4, the cycle goes back to T_0 and starts repeating itself.

1.2 DESIGN SPECIFICATION

Parameter	Symbol	Value	Unit
Input Voltage	Vin	48	V
Efficiency	n	92	
Duty Cycle	D	60%	
Output Voltage	Vo	4.7	V
Output Voltage Ripple	Vo(rip)	47	mVpp
Load Current	Io	30	A
Switching Frequency	Fsw	300	kHz

Chapter 2

POWER STAGE DESIGN

POWER STAGE DESIGN

2.1 SECONDARY SIDE DESIGN

2.1.1 Output Inductor

Assuming the pk-pk inductor Ripple Current is about 15% of max output current, Faraday's law can be used to solve for Lo.

$$L_o = \frac{V_o}{0.15 * I_{o(max)} * F_{sw}} * (1 - D_{min})$$

$$= 1.8667\text{uH}$$

Now rounding this up causes fewer ripple current in the inductor whereas rounding down lets more ripple current and lesser inductor value. But when the ΔI_{lo} is allowed to rise the ripple current flowing through the output capacitor rises and thus increases the switching losses suffered by the output capacitors.

Now the ΔI_{lo} actual value can be back designed for a selected value of Lo i.e. 2uH.

$$\Delta I_{lo} = \frac{V_o}{L_o * F_{sw}} * (1 - D_{min})$$

$$= 4.2\text{App}$$

Now a current of 4.2App refers to 14% of total load current, which is quite high to be accepted. Thus the I_{lo} rms is found out by

$$I_{lo(rms)} = \sqrt{I_o^2 + {\Delta I_{lo}^2}/{3}}$$

$$= 30.1\ \text{Arms}$$

2.1.2 Output Capacitor

The output capacitor is determined as the minimum capacitance required to hav a maximum allowable ripple voltage of about 1% of load voltage.

$$C_{o(min)} = {\Delta I_{lo}}/{8 * F_{sw} * \Delta V_{o(rip)}}$$

$$= 58\text{uF}$$

Now this value is dominated by the $R_{ESR(out)}$ and other transient conditions. Thus for limiting the output ripple to a small value the below condition must be fulfilled

$$R_{ESR(out)} \leq {\Delta V_{o(rip)}}/{\Delta I_{lo}}$$

$$= 8\text{m}\Omega$$

As the transient response is a part of design concern, the C_o (output capacitance) can be calculated by inspecting the transient voltage overreach, Vos that can be handled by the change in output current. By equating we get

$$C_o = {L_o * I_{step}^2}/{V_{os}^2}$$

$$= {L_o * (I_{step(\max)}^2 - I_{step(min)}^2)}/{(V_{os(max)}^2 - V_{os(min)}^2)}$$

$$= 672 \text{ uF}$$

2.1.3 Synchronous Rectifiers

The meaning of Synchronous rectification is the use of power thyristors or mosfets as switches instead of normal diodes in rectification process. The main reason behind the use of mosfets is to remove the losses associated with the diode conduction loss. Eliminating this would result in increased efficiency of the system.

In this system we use two mosfets, one in forward direction and one in reverse. A self-driven use the gate-source is directly derived from the transformer secondary. Thus it differs as a

function of Vin (input voltage) and transformer reset voltage, divided by N (transformer turns ratio). The synchronous rectification is not a good option if the input voltage range is broader than 2 to 1.

The minimum secondary voltage needs to be calculated.

$V_{s(min)}$ =5.79V

Now as we know the minimum input voltage we can calculate the turns ratio on the transformer to be used

$$N = \frac{N_p}{N_s} = {V_{in(min)}}/{V_{s(min)}}$$

$$= 6$$

Now the Vgs of the Qf differs according to the input voltage divided by the turns ratio. For the Vin to be in-between 36V to 72V, the gate source voltage of Qf is between 6V to 12V, which is enough for a typical Mosfet. For the reverse Mosfet Qr, the gate to source voltage is found to be in between 5V to 8V for the Vin of 36V to 72V.

During turn on the Mosfet Qf suffers switching losses as it is hard switched.but the reverse mosfet Qr is turned on under ZVS condition thus it faces less losses. To avoid such losses mosfets with extremely low internal resistance should be used. Although this doesn't completely eradicate the mosfet losses, it surely reduces them.

2.2 POWER TRANSFORMER

The biggest advantage that a forward converter with transformer over the normal buck converters is that we can reduce the secondary voltage as per the requirement, as per ones need, whereas in the normal buck converter the voltage just gets half and more step down is not possible. The transformer provides galvanic isolations to the both sides of the system, thus providing better control, and more efficiency.

Here in this system we use a transformer of turns ratio of 6, thus the input voltage gets reduced six times at the secondary, and this voltage is applied across the mosfets, as it acts as their gate to source and drain to source voltages.

Single directional flow of current would cause the transformer to reach saturation too soon, thus stopping it from working. Therefore we need to reset the transformer. This is done by the help of an active clamp.

In the design the turns ratio is maintained at six by the connection of two primary winding in parallel to each other and two secondary windings in parallel. This helps in reducing the dc winding by half, and thus greatly reducing the losses in the system.

At such a high frequency such as 300 kHz, the main losses in a transformer is due to the core loss, occurring due to the time varying flux, of the transformer B-H curve. The copper losses are due to the Rms current flowing through the secondary and primary windings thus causing I^2R losses.

The losses associated with a transformer is predefined by the manufacturer, as the core loss is pre-calculated and provided by the manufacturer. And the internal resistance of both the sides are provided by the manufacturer, thus all one needs to do is to find out the current flowing through the transformer primary and secondary windings. And from these values, the total loss in a transformer can be calculated. The power loss is associated with heating of the transformer and thus the system, thus affecting it, so special care should be taken to reduce or check the heating taking place in a transformer.

2.3 PRIMARY SIDE DESIGN

2.3.1 Active Clamp

2.3.1.1 Introduction

The purpose of the active clamp is to clamp the input current to a certain value and as the capacitor stores charge during the conduction period, it discharges and forces the current to flow in opposite direction and thus helping the transformer to reset. The reset of transformer is necessary as the transformer cannot work if the current flows in a single direction or in a DC mode cause it would get saturated pretty soon and thus stop working. Thus the transformer is feed negative voltage that brings down the magnetising current and makes it zero, thus stopping it from getting saturated. The active clamp consists of a clamp capacitor C_{CL} and a switch which is mostly a mosfet, due its less conduction loss.

The Active clamp technique is the most advanced and best method of the generation of forward converters. The first were the Conventional Forward Converters, which operate below 50% duty cycle. This is done so that the transformer can be reset without causing any potential transformer saturation. A separate reset winding was used along with the main transformer so to help clamping the reset voltage amplitude to input voltage. This ensures proper functioning and reset with any load and line conditions. The only problem with this was the limitation in duty cycle.

The second were the RCD type forward converter, the biggest advantage in this method was overcoming the 50% duty cycle barrier. As the name suggest the Resistor, Capacitor and Diode form a clamp voltage to which the magnetising energy can be dissipated. Now the use of high clamp voltage with an amplitude bigger than input voltage can help to stretch over the 50% duty cycle easily. The drawbacks in this method was the high voltage stress on the semiconductors and the dissipation of energy through the resistance of the RCD clamp. This lead to the development of the Active Clamp techniques.

In this this method the diode of the RCD clamp is replaced with an active Mosfet switch. Its purpose is to clamp the primary to the reset capacitor and to have a controlled energy transfer from the reset capacitor to the primary side. Now the current in the mosfet switch can flow in both direction, and is only active in the switching cycle and operate when the main switch is

off. The main advantages achieved by this method was the higher efficiency and ZVS (Zero Voltage Switching).

The significant advantages gained by using Active Clamp are:-

- The transformer magnetising current is recycled instead of dissipated to the resistance.
- The introduction of ZVS, increases the efficiency as soft switching takes place.
- Use of lower voltage mosfets
- Operates at a fixed frequency
- More than 50% duty cycle in possible.
- Higher frequency operation is possible
- Reduced EMI
- The main transformer actively reset to the 3rs quadrant of B-H curve.

Comparison between Conventional Forward Converter, RCD clamp and Active Clamp

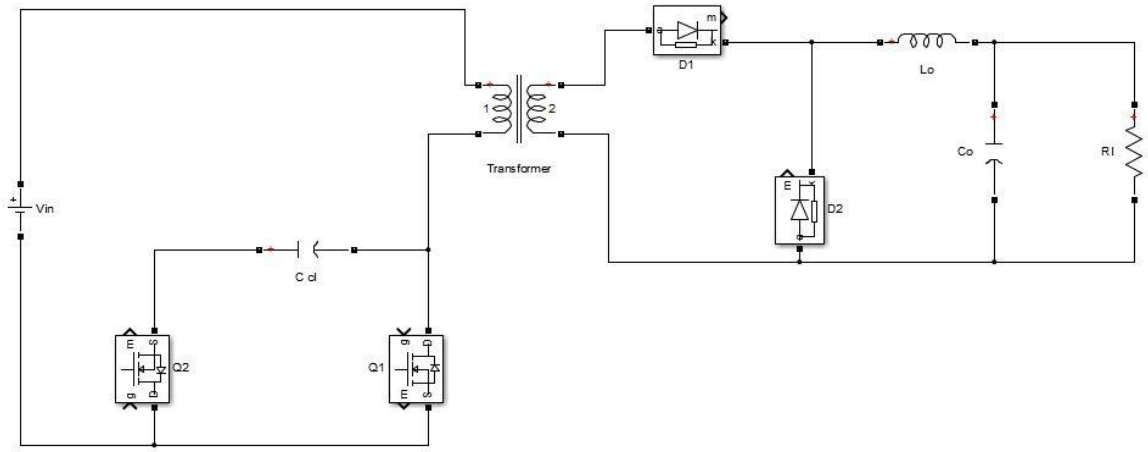
Parameter	**Conventional**	**RCD Clamp**	**Active Clamp**
Efficiency	High	high	highest
Duty Cycle (max)	<50%	>50%	>50%
Turn Ratio	lower	high	high
Voltage Stress	Lowest	highest	high
Current Stress	Higher	lower	lower
I (mag)	recycled	dissipated	recycled
I (lkg)	recycled	dissipated	recycled
High Frequency	Good	fair	best
Complexity	Lowest	moderate	highest

2.3.1.2 Types of Active Clamp

There are two types of connections possible with an active clamp technique i.e.

1. Low Side – Clamp resent directly through drain to source of the main mosfet switch
2. High Side – Clamp circuit across transformer primary.

Low Side Clamp:-



- When Q1 is conducting the full input voltage in across the transformer primary
- When Q2 is conducting the variance between the input voltage and the clamp voltage is applied across the transformer magnetising inductance and is the transformer reset period.
- Q2 carries only the magnetising current.
- There is also a dead time introduced in between Q1 turnings-off and Q2 turning-on. Through this period the primary current flows in the body diode. This is called resonant period in which conditions are set foe transformer reset under ZVS condition.

By volts seconds balance

$D * Vin = (1-D) * (Vc_{ls} - Vin)$

⇨ $D*Vin = (1-D)\ Vc_{ls} - (1-D)\ Vin$

⇨ $Vc_{ls} = (\frac{1}{1-D}) * Vin$

Note- this is similar to the output of a boost converter therefore the low side clamp is sometimes called boost type clamp.

Also, $Vds_{(ls)Q1} = Vc_{ls} = (1/1\text{-}D) * Vin$

During the transformer reset period the dot polarity reverses so the voltage applied to primary is now defined as

$$V_{Reset(ls)} = V_{c(ls)} - V_{in}$$

⇨ $V_{Reset(ls)} = (\left(\frac{1}{1-D}\right) * V_{in}) - V_{in}$

⇨ $V_{Reset(ls)} = (\frac{D}{1-D})V_{in}$

⇨ $D = \left(\frac{Vo}{Vin}\right) * N$, where V_o = output voltage, V_{in} = input voltage, N = Np/Ns

⇨ $V_{ds(ls)} = V_{c(ls)} = \frac{1}{1-\frac{V_o}{V_{in}}N} * V_{in}$

⇨ $V_{c(ls)} = \frac{V_{in}^2}{V_{in}-N*V_o} = V_{ds(ls)}$

⇨ $V_{Reset(ls)} = \frac{V_0*V_{in}*N}{V_{in}-NV_o}$

⇨ $V_{ds(ls)} = V_{c(ls)} = \frac{V_{in}^2}{V_{in}-NV_o}$

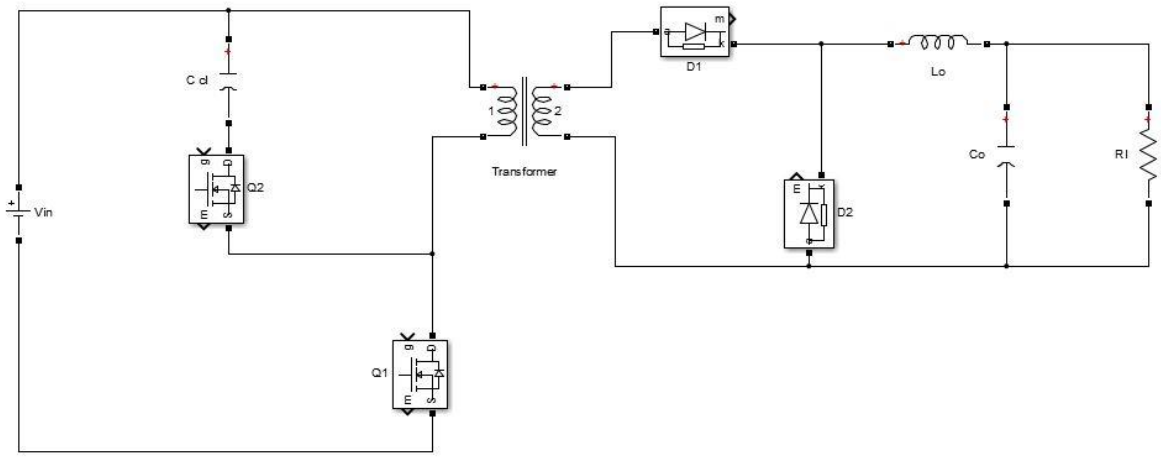
And, $V_{Reset(ls)} = (\frac{V_0 V_{in} N}{V_{in}-NV_o})$

A graph can be plotted between Vin and Vds of Q1, this graph would show, the variation in voltage stress on the mosfet during low input voltage. For this we need to precisely limit the maximum duty cycle. The consequences can be destructive on the mosfets as the high voltage can burn them out. Thus the clamp capacitor should be selected carefully.

High Side Clamp:-

- Alike to the low side clamp when the main mosfet Q1 is conducting the full input voltage appears across the transformer primary and this is reversed to as power transfer mode.
- When the Q2, auxiliary Mosfet is conducting the clamp voltage, $Vc_{(hs)}$ is applied directly across the transformer magnetising inductance and is denoted to as the transformer reset period.

- This is quite dissimilar than the low side case where the clamp voltage, $Vc_{(ls)}$ was applied directly across the drain to source connection of the main mosfet.
- Here thee auxiliary mosfet is N channel unlike the low side case.



Putting the volts second balance

$$DV_{in} = (1 - D)V_{c(hs)}$$

$\Rightarrow V_{c(hs)} = \frac{D}{1-D}V_{in}$

The above equation is similar to the TF of a nonisolated flyback converter. Thus is why the high side clamp is usually referred to as a flyback type clamp.

$$V_{Reset(hs)} = V_{c(hs)} = \frac{D}{1-D}V_{in}$$

During the transformer reset period the dot polarity on the transformer primary changes, so the voltage applied to drain to source of the main Mosfet Q1 can be stated as

$$V_{ds(hs)} = V_{in} - V_{c(hs)}$$

$\Rightarrow V_{ds(hs)} = V_{in}(1 + \frac{D}{1-D})$

$\Rightarrow V_{ds(hs)} = \frac{V_{in}}{1-D}$

Now,

$D = \frac{V_o}{V_{in}}N$; Where N= Np/Ns

Therefore, $V_{c(hs)} = \frac{NV_o}{1-\frac{NV_o}{V_{in}}} = \frac{NV_o - V_{in}}{V_{in} - NV_o}$

- $V_{ds(hs)} = \frac{V_{in}^2}{V_{in} - NV_o}$

We now realise that Vds(hs) = Vds(ls)

2.3.1.3 Choosing the Clamp Capacitor

No matter whether it is a low side or high sideactive clamp circuit, the volt second balance is a necessity for both case.

The primary mosfet drain-source are the same for each circuiit it id the varying clamp voltage applied over the clamp capacitor that must be measured.

The details of clamp capacitor variations can be seen by comparing the difference between the clamp voltage transfer function for each case.

$\Delta V_c = V_{c(ls)} - V_{c(hs)}$

$= (1/1 - D - D/1 - D)V_{in}$

$= V_{in}$

The above result shows that $V_{c(ls)} > V_{c(hs)}$ by V_{in}, therefore low side clamping is preferred.

The value of clamp capacitor is so chosen that the total of ripple voltage is tolerable.

Larger capacitors give less ripple voltage but have high transient time period, and small capacitors have small transient time period but high ripple voltage. So ideally the clamp capacitor is so chosen that the amount of ripple voltage is not high, but allow some but it should be controlled as not to allow unnecessary drain-source voltage stressto the main mosfet i.e. Q1. Thus about 0.2 times of voltage ripple is allowed.

Now for finding the clamp capacitor value

$$2\pi\sqrt{Lmag * Ccl} > 10 * Toff$$

This can be reduced to

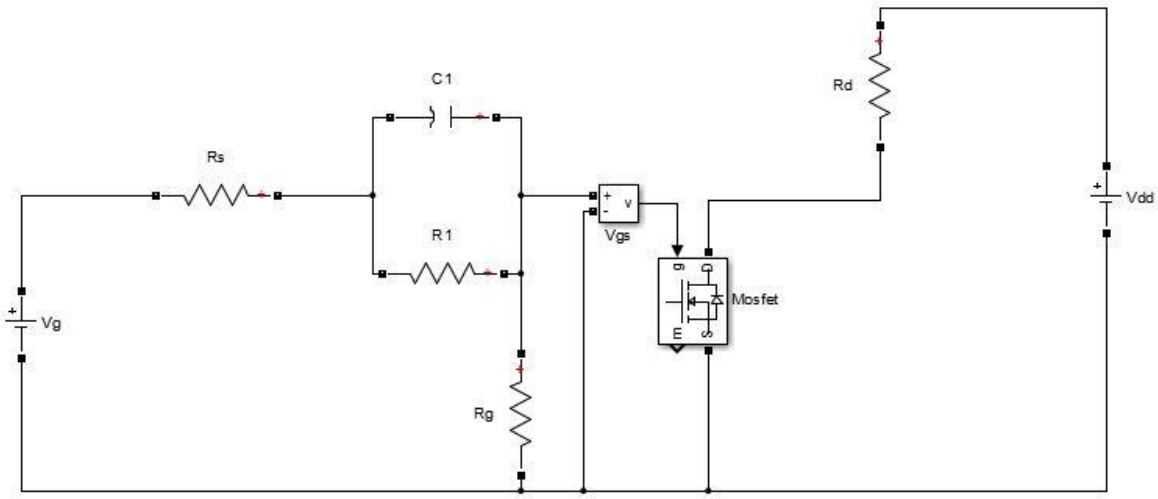
$$Ccl > \frac{(10(1-D))^2}{(2\pi F)^2 * Lmag}$$

= 22nF

2.3.2 Gate Drive Circuit

Mosfets are voltage controlled circuits and have very high input impedance, the gate draws very small leakage current in order of Nano amperes.

The turn on of a mosfet depends on charging time of the input or gate capacitance. The turn on time of a mosfet can be reduced by connecting a RC circuit as show in the figure below.



When the gate is turned on, the initial charging current is Iq = Vg/Rs

And the steady state values of gate voltage is given by Vgs = (Rg*Vg)/(R1+Rs+Rg)

PNP and NPN transistors act as emitters followers and offer a low output impedance. These transistors operate in linear mode instead of the saturation mode thereby minimizing the delay time. The gate signal maybe op amp generated.

2.3.3 The Primary Mosfet Qmain

As the clamp voltage is already been calculated, the drain to source voltage is already known. Now $I_{PIR(rms)}$ is the drain current that flows through the mosfet. The max rms drain current that occurs at min input voltage and max load current. So a mosfet of high rating is required so that it can withstand high input voltage.

Now as Qmain constantly turns-off under ZVS, it is still suffers some turn-on losses. Now ZVS is a cost of some minimum load current which is about 40% in the case.

Power loss can also happen due to charging and discharging of the mosfet. This loss is minimum for lower voltage applications, but rises with the level of voltage

.

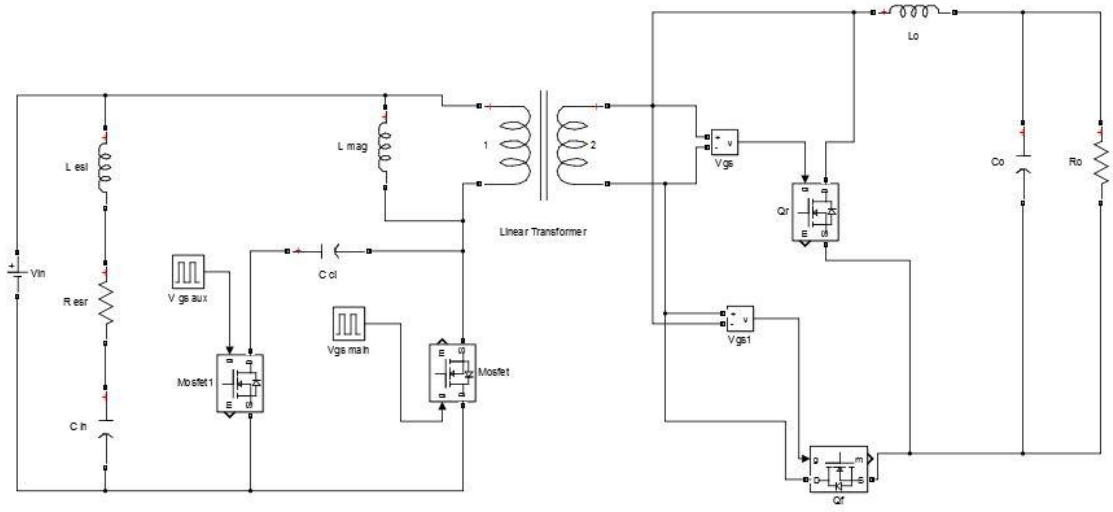
2.3.3.1 ZVS Consideration

The ZVS conditions are that the switching of Qmain (on /off) must done when the drain to source voltage is zero. Now this condition can be achieved when the voltage at node Va is resonantly compelled to zero volts, within the set time between the Qmain turn off and turn on.

During the T_1-T_2 interval, Qmain has just turned-off under ZVS condition and Qaux is about to turn-on. As Coss is charged to Va, the body diode of Qmain is reversed biased, and that current that was previously flowing through the channel resistance of Qmain is now diverted to Coss. An amount of current is also averted to the output capacitance of the auxiliary mosfet Qaux. Now the current logically flows in the same direction of as that of resonant current flowing out of Va. So, as the two currents are additive the Qmain always turns on under ZVS condition no matter what amount of current is charging Coss.

During next resonant interval, T_3-T_4, Qmain is about to turn-on and the Qaux has just turned-off. The Resonant current, I_{RES} is reqired to move Va to Zero volts so as to oppose the current necessary for Qmain of ZVS turn on. Now as these two currents are opposing each other the Qmain experiences SVS under certain specific conditions.

2.3.4 Input Capacitance



The Forward converter with Active clamp techniques is a buck consequent power topology with a pulsated AC input current. The input capacitor shown is present alongside its equivalent series resistance and series inductance, which both add to total input ripple voltage. The purpose of this capacitor is to provide high frequency filtering so that the input voltage can be closest to a pure dc source, with low ore none ripple or noise.

So for determining the input capacitor we first need to find out the input current (max RMS). The rms capacitor current is resultant from Ic(in).

For initial selection of input capacitor, it is assumed that the change in ripple voltage is capacitance dominant, but for higher frequency procedure the equivalent series resistance and series inductance can be dominant over Cin. To limit the input voltage ripple to about 5% of min input current the required input capacitance value (minimum) is given by-

$C_{in(min)} = (I_{in} + I_{mag})/(0.05 * V_{in})$*$T_{off}$

$= (I_{in} + I_{mag})/(F_{sw} * (0.05 * V_{in}))$* (1-D)

Now at min Vin, max Duty cycle, max Iout and addition of 25% design boundary

$C_{in(min)} = \frac{V_o * I_{o\,(max)} + I_{mag} * n * V_{in(min)}}{n * V_{in(min)} * F_{sw} * (0.05 * V_{in(min)})} * (1 - D_{max})\backslash$

$= 4uF$

As the amount of ripple voltage is way bigger than amount of ripple current R_{ser} is of lesser concern

$R_{ser(in)} < \frac{0.05 * V_{in(min)}}{(I_{pri(pk)} + \frac{I_{mag}}{2})}$

$= 272m\Omega$

Chapter 3

Simulation

SIMULATION

3.1 INTRODUCTION

For the given circuit two simulations were done. One with an open loop and another with a closed loop. The result in both the cases were observed and inference were taken.

Parameters

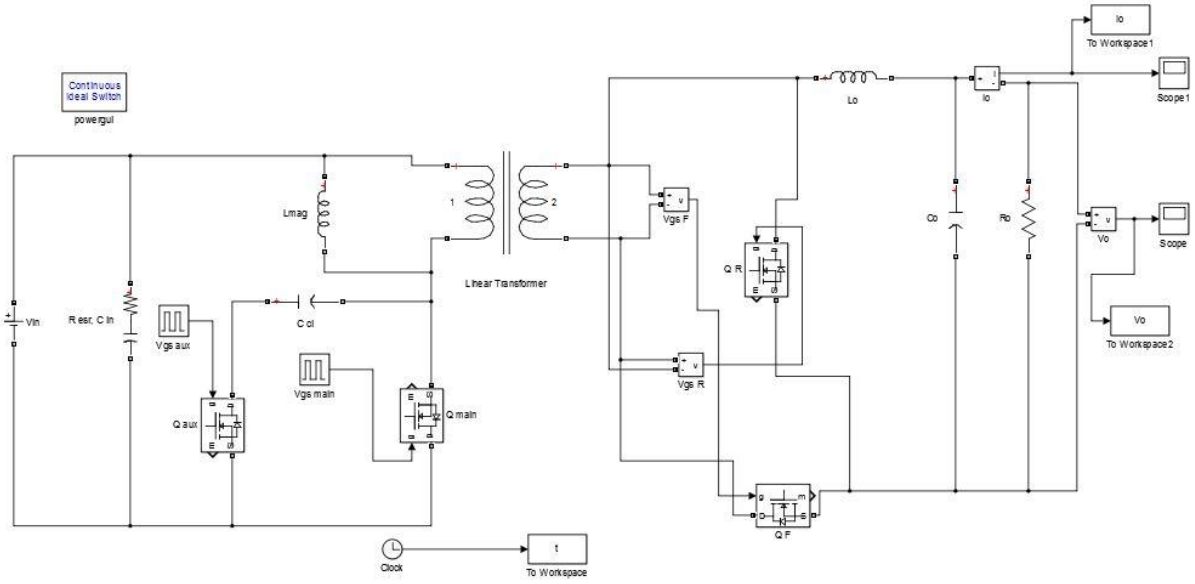
Vin = 48 V, Fsw = 300 kHz, Ccl = 22nF

Cin = 4 uF, Resr = 272 mΩ, Lmag = 195uH

N = 6, Co = 672uF, Lo = 1.87uH

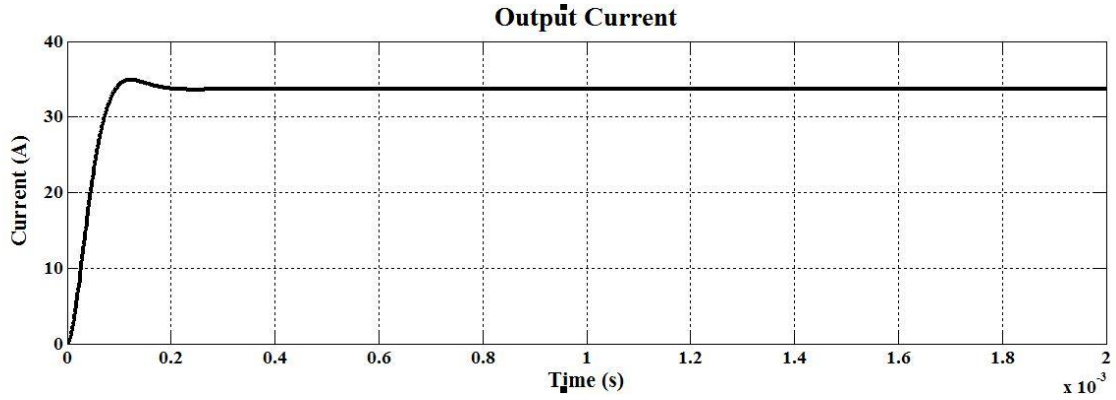
3.1.1 Open Loop Connection

Circuit Design

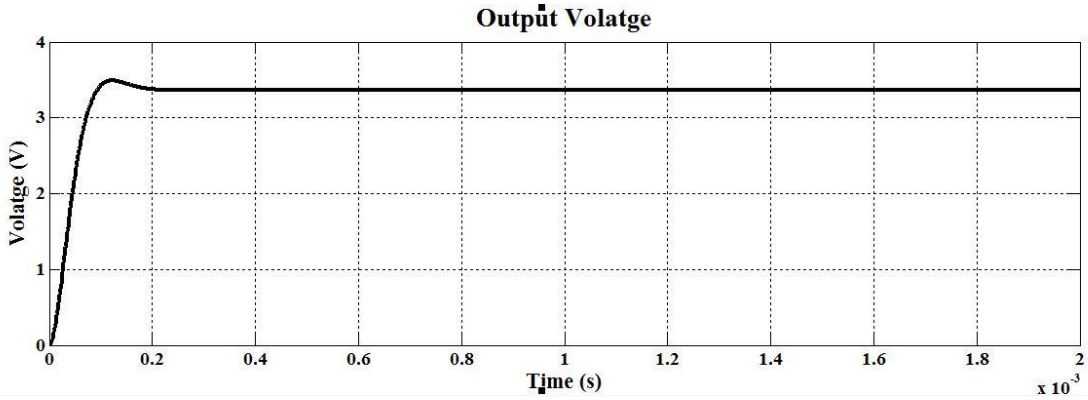


Waveforms

Output Current



Output Voltage

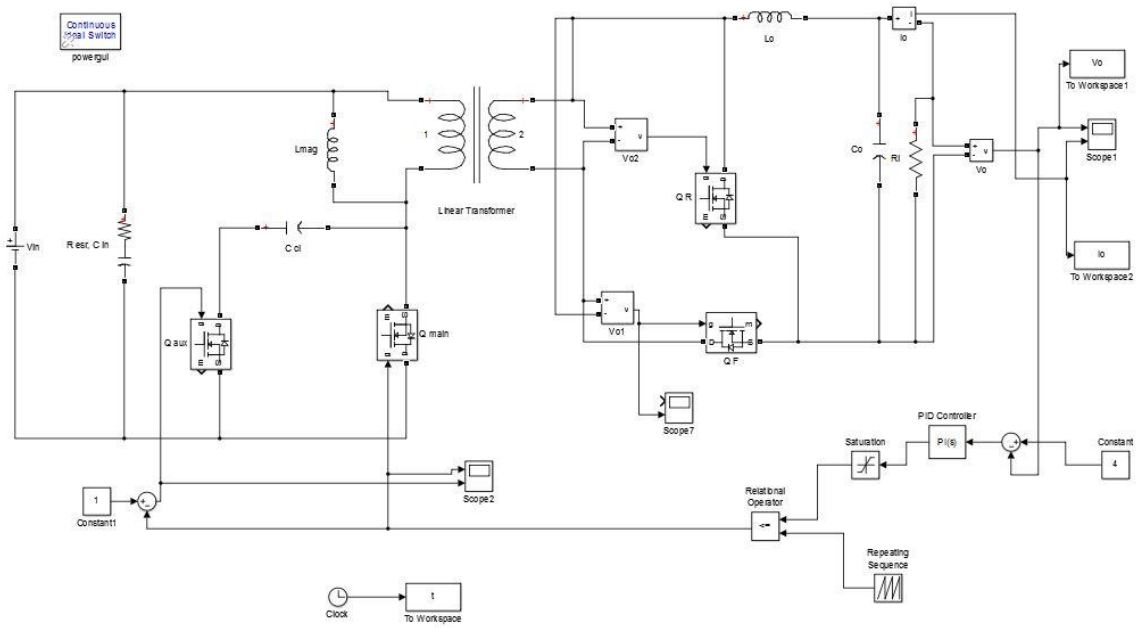


Inference

The circuit was run in Matlab Simulink and the output voltage and current are given above. The initial overshoot in both the cases are due to the presence of ripple factor in the input and output. To check this, the circuit is redrawn with a closed loop to control the output and the result follows.

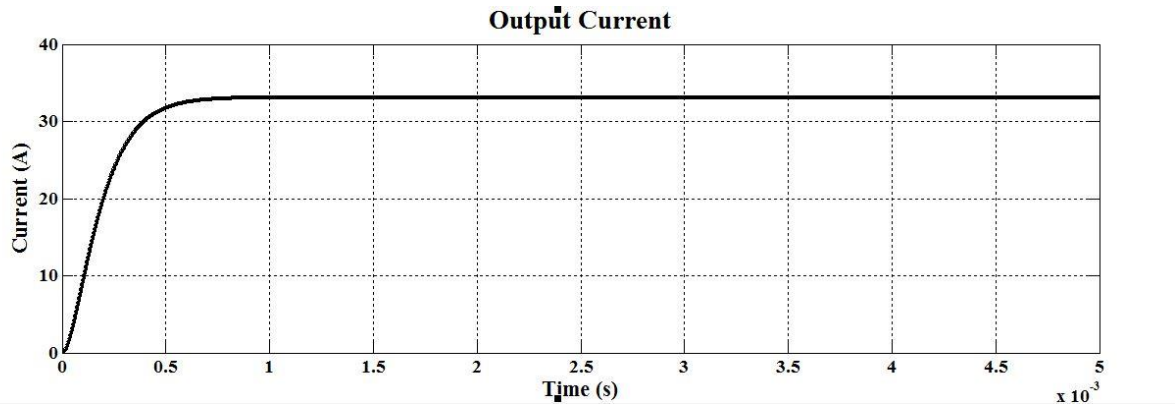
3.1.2 Closed loop Connection

Circuit Design

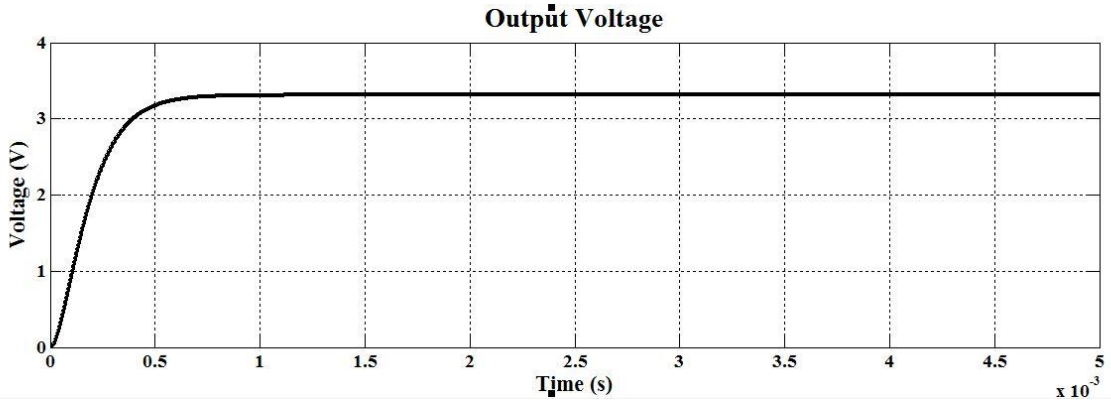


Waveforms

Output Current



Output Voltage



Inference

The previous circuit was redrawn with a feedback i.e. in a closed loop. The result are given above. We can see here the absence of the earlier overshoot, this is achieved by controlling the output voltage by giving a feedback to the both mosfets. A Vref of 4V was used to find the stable output.

3.2 CONCLUSION

A forward converter with active clamp and synchronous rectification was designed. The transformer was used to effectively reduce the secondary voltage n times as per requirement, which was not possible with normal buck converter. The values of all parameters was calculated to have a controlled output voltage and output current. Two designs were made, one with an open loop and another in a closed loop. The open loop output experienced certain ripple due to disturbances, which was eliminated while in a closed loop by use of a feedback feed to the Mosfets Qmain and Qaux. By using the feedback the results became stable and required output was achieved.

References:-

- Steve Mappus, Designing for High Efficiency with the Active Clamp UCC2891 PWM Controller (SULA303)
- UCC2891 current mode active clamp pwm controller, datasheet (SLUS542)
- Steve Mappus, *UCC2891EVM, 48-V to 1.3-V, 30-A forward converter with active clamp reset*, user's guide to accommodate UCC2891EVM, (SLUU178)
- Bill Andreycak, *active clamp and reset technique enhances forward converter performance*, power supply design seminar SEM-1000, Topic 3, (SLUP108)
- *48-V Input, 3.3V/100 Watt Converter with UCC3580-1 Controller*, user's guide to accommodate pmp206_c reference design, (SLUU146)
- Qiong Li, F. C. Lee, *design considerations of the active clamp forward converter with current mode control during large-signal transient*, IEEE 2000
- A. Fontán, S. Ollero, E. de la Cruz, J. Sebastián, *peak current mode control applied to the forward converter with active clamp*, IEEE 1998