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Atlas Simulation Based Performance Study of Fully-Depleted Dual-Material-Gate Silicon on Insulator MOSFETs

A Thesis Submitted in Partial Fulfillment of the Requirements for

The Degree of

Bachelor of Technology

In

Electronics and Instrumentation Engineering

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DEPARTMENT OF ELECTRONICS AND INSTRUMENTATIONENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGYROURKELA

2015

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Submitted by

Abdul Wali

(111EI0559)

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Under The Guidance of

Prof. P. K. Tiwari

Department of Electronics and Instrumentation Engineering

National Institute of Technology Rourkela

Orissa - 769008, India

2015

NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA,
ORISSA-769008, INDIA

CERTIFICATE

This is to certify that the thesis entitled, **"Atlas simulation based performance study of fully-depleted dual-material-gate silicon on insulator MOSFETs"** submitted by **Abdul Wali** in partial fulfillment of the requirement for the award of **Bachelor of Technology degree in Electronics and instrumentation Engineering** at the National Institute of Technology Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of our knowledge, the matter embodied in the thesis has not been submitted to any other University/ Institute for the award of any degree or diploma.

Date: Dr. P.K. Tiwari

Place: Department of Electronics and Instrumentation Engineering

National Institute of Technology Rourkela

Rourkela-769008

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There is no need to mention that a big part of this thesis is the result of joint work with him, without which the completion of the work would have been impossible.

I would like to thank my parents, without their love, patience and support; I could not have completed this work. Finally, I wish to thank many friends for the encouragement during these difficult years.

Abdul Wali

2015

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Abstract

In this project the characteristics of fully depleted dual metal gate silicon on insulator is studied and presented, the result is compared with that of single material gate MOSFET the result indicates that short channel effect reduces in dual material gate MOSFET.Moreover the electrical characteristics of MOSFET can be controlled by gate length and work function engineering. So this work shows better performance of dual material gate with compare to that of single material gate silicon on insulator.

Chapter 1

1.1 Introduction

First time structure of MOSFET was proposed and patented by Lilienfeld and Heil in the year 1930, yet was not effectively showed until year 1960.The fundamental innovative issues were the control and decrease of the surface states at the interface between the oxide and the semiconductor.at the first it was possible to slim down an existing n-type channel by applying a voltage to the gate. This type of devices conducting between source and drain even at the absence of gate voltage and are called **"depletion-mode"** devices. With the decrease of the surface states it was not possible to fabricate the devices which don have a conducting channel until a positive voltage is applied. This kind of devices is called **"enhancement-mode"** MOSFET. The negative charge accumulate below gate oxide-semiconductor junction are in a thin layer (~11.5 nm thick) which is called as inversion layer. So this kind of MOSFETreferred as "enhancement-mode" MOSFET.

The full form of MOSFET term is metal oxide semiconductor field effect transistor. MOSFET is a unipolar transistor, which control current. In MOSFETcurrent at drain and source is controlled by an electric field which is induced due to appliedvoltage at the gate.MOSFET consists ofgate electrode, drain electrode, source electrode and substrate. But source terminal is connected to the substrate of MOSFET, make it a three-terminal device. Because drain and source electrode are shortedinternally, so only drain,source and gate electrodes appear in electrical scheme.

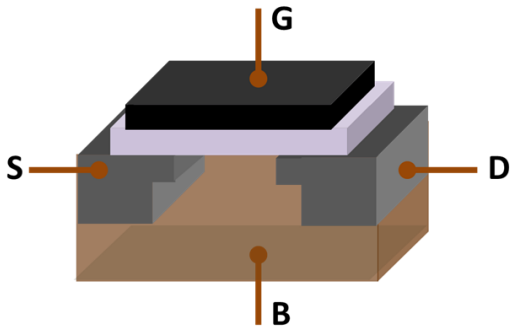
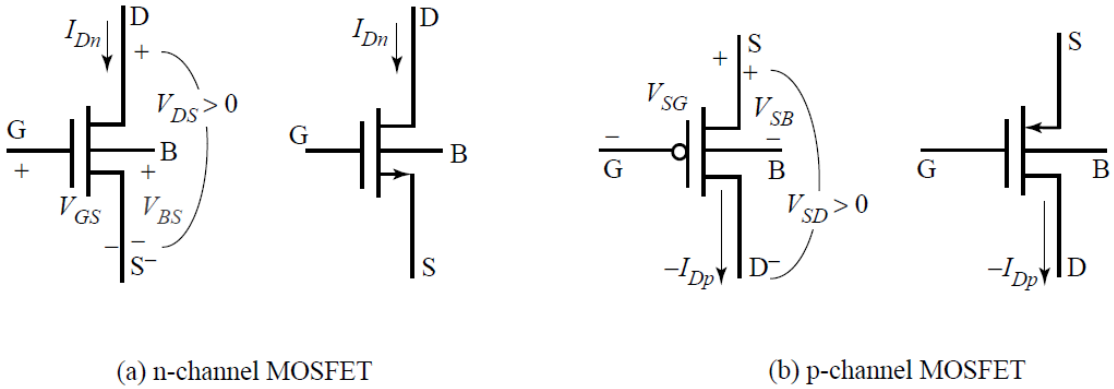


Figure 1: Structure of conventional MOSFET

Two-terminal device:

n-typeMOSFET (n-channel) on p-Silicon body(uses electron inversion layer)

p-type MOSFET (p-channel) on n-Silicon body(uses hole inversion layer)



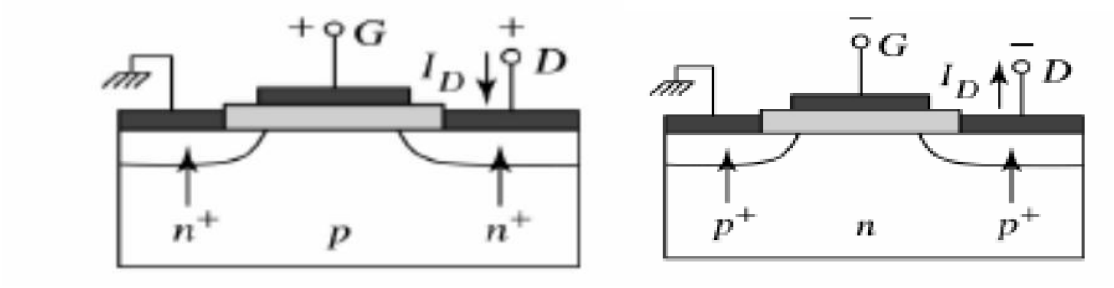
(a) n-channel MOSFET (b) p-channel MOSFET

Figure 2:MOSFET symbol

1.2 TYPES OF MODES IN A MOSFET

Voltage applied at gate oxide cause formation of conducting channel between source and drain and conductivity of the channel is proportional to the magnitude of voltage applied to the gate oxide. The enhancement mode means the conductivity of MOSFET proportional to the voltage applied at gate.Which cause accumulationofelectrons in a n-type device and hole in a p-type device in between to the drain and source electrodes, and calledas "*inversion layer*". If the channel contains electrons referred as an n-MOSFET or n-MOS, or holes

referred as a p-MOSFET or p-MOS, a p-type MOSFET consist of holes in its body in a p-type MOSFET substrate is consist of electrons



n-channelMOSFET **p-channel MOSFET**

Figure 3: Cross section of MOSFET

When voltage between gate and drain is zero , the conducting path is very narrow and conducting width increases with increase of the gate to source voltage There exist a pair of small n-type regions just below the drain and source terminals. If a positive voltage applied to gate, will remove away the holes into the p-type body and attracts the electrons in the n-type channel below the source and drain terminals. By increasing the applied voltage to the gate it further removes the p-type holes away and increases the thickness of the n-type region. As a causes increases the current which produces between sourceto drain because of this, this kind of device is refers an Enhancement mode MOSFET.

Three Operational Modes:

1.2.1 Cut-off mode:

Here,VGS < VT , VGD < VT with VDS > 0.whereVT is the threshold voltage of the MOSFET.if the voltage applied at gate electrode is less than the voltage require to on the device there is not significant current between source and drain so MOSFET is in cut off region , and there is no conducting channel between sours and drain.

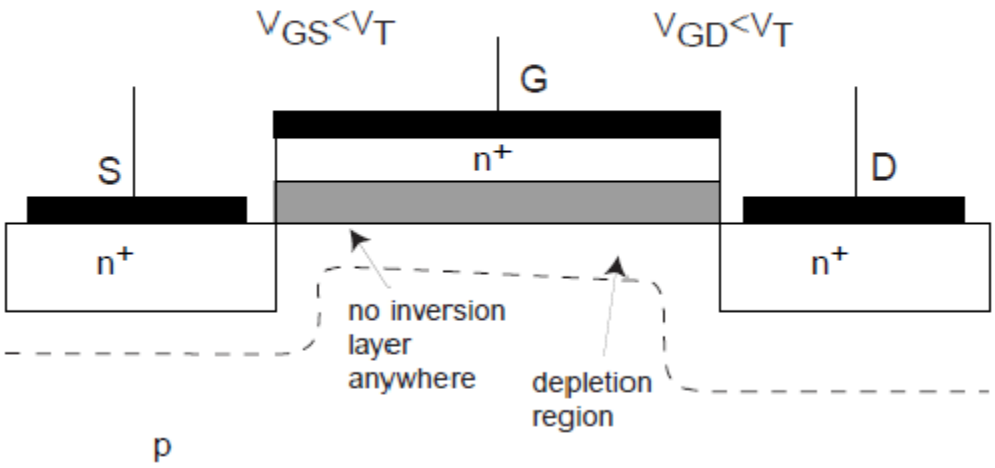


Figure 4: internal diagram of MOSFET

So Id=0

1.2.2 linear or triode region:

Here, VGS >VT , VGD > VT , with VDS > 0.

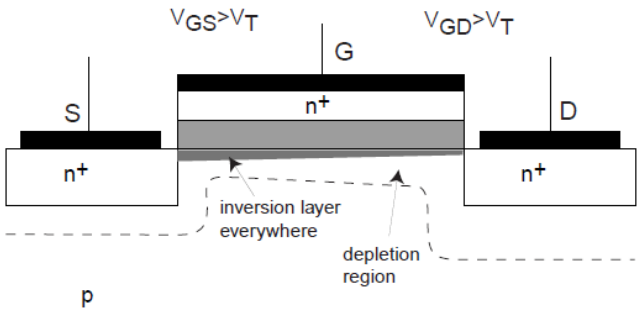


Figure5: Internal diagram of MOSFET

In this region MOSFET is on, and voltage applied to the gate electrode is sufficient to induce conducting path between drain and source which cause current flow from drain to source. in this region the transistor behave as a resistor , and the magnitude of the resistor is proportional to the voltage applied to the gate of MOSFET and it also depend upon the voltage applied to the drain and source of transistor. The drain current equation is as follow:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Where $\mu_n$is the electron mobility, ***W*** is the width of gate oxide, ***L***is the length of the gate oxide gate and C_{ox} is the capacitance between channel gate oxide per unit area. The transition from the exponential sub threshold region to the linear region is not as sharp as the equations gives.

1.2.3 saturation mode:

Here, VGS >VT , VGD < VT (VDS > 0).

ID independent of VDS: ID = ID_{sat}

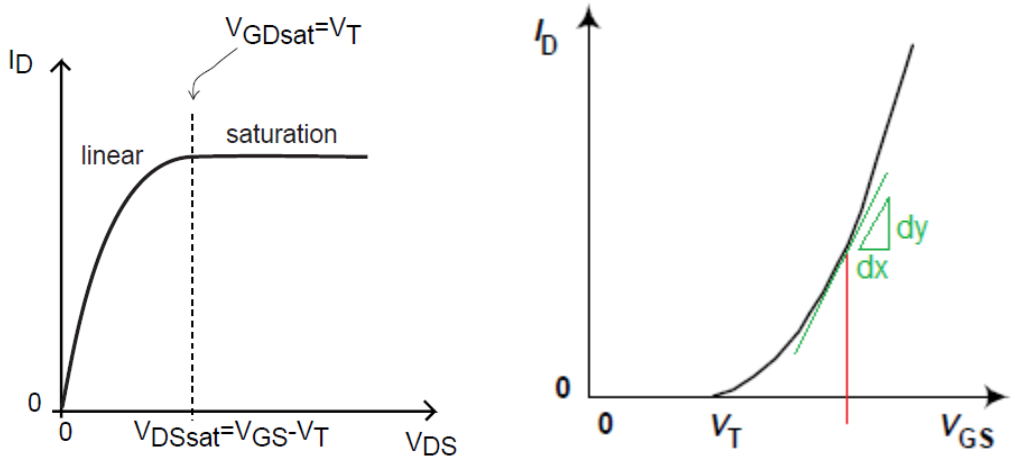
If the voltage applied at drain is greater in magnitude than the voltage applied to the gate, the electrons flow, is not concentrated and conduction is not through a narrow regionrather through a wide area, current flow through different dimension distribution and this large enough voltage applied to the gate and drain cause expansion of conducting area into substrate.This region is also called as **pinch-off** to show the narrow channel region close to the drain. Now drain current is almost independent ofvoltageapplied to the drain and only proportional to the by the gate to source voltage, and drain equation is approximately as following:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \left(1 + \lambda (V_{DS} - V_{DSsat})\right).$$

Here λ, is the channel-length modulation parameter, current dependence on voltage applied to the drain because of the Early Effect or channel. According to this equation, a most important design parameter, the MOSFET transconductance is:

$$g_m = \frac{2I_D}{V_{GS}-V_{th}} = \frac{2I_D}{V_{ov}},$$

Here the V_{ov} = VGS – $V_{th}$is referred as the overdrive voltage and where VDS_{sat} = VGS – V_{th} *is* voltage corresponding to the small discontinuity which is in between linear region and saturation region.



6.a **6.b**

Figure 6:(a)Idversus V_{ds} b)Id versus V_{gs}

MOSFET dependencies:

• VDS increases ------ ID increases (higher lateral electric field)
• VGS increases ------ ID increases (higher electron concentration)
• L increases ---------- ID decreases (lower lateral electric field)
• W increases -------- ID increases (wider conduction channel)

Chapter 2

DISADVANTAGES OF CONVENTIONAL MOSFETS

The MOSFET scaling required to increase the MOSFET performances and to reduce the size and density of the MOSFET, but it degrades the MOSFET operation in terms of short channel effect and leakage current .To continue the scaling process there is need of device structure that provide better performance in deep submicron regime. Due to reduction in the channel length scaling, threshold voltage is decreasing that increasing the leakage current and "short channel" effects. Unfortunately there is self heating effect create in the electronics device. Furthermore there are a large number of short channel effects which affects the performance ofMOSFET. Scaling trend in CMOS approaching physical limits prompts the need for alternative device.

Due to the continue of scaling the device channel length is decreases .as the channel length decreases the source-substrate and drain substrate depletion widths ,the charge in the conducting path due to these parasitic diodes become comparable to the depletion charge due to MOSFET gate-substrate voltage rendering the gate and substrate electrode is not so much effective.

Some short channel effects are explained below:-

Thereare five different short-channel effects and they are as follow :

1. Drain-induced barrier lowering (DIBL)
2. Surface scattering
3. Velocity saturation
4. Impact ionization
5. Hot electrons

2.1 Drain Induced Barrier Lowering(DIBL)

Effect of the drain potential on the conducting path region can have very serious impact on the performance of submicron MOSFET transistors. One effect that is very similar to the punch through effect is Drain-Induced Barrier Lowering (DIBL). In the literature punch through is sometimes called as subsurface drain induced barrier lowering in contrast to surface DIBL.

In the weak inversion regime there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. If a high drain voltage is applied, the barrier height can decrease, leading to an increased drain current. Thus the drain current is controlled not only by the gate voltage, but also by the drain voltage. For device modeling purposes this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage. The DIBL effect becomes obvious when looking at the transfer curves of a MOS transistor for the linear and saturated. The DIBL effect can be measured by the lateral shift of the transfer curves in the sub threshold regime ΔV_{th} divided by the drain voltage difference of the two curves and is given in units (mV/V)

2.2 Surface scattering

When the channel length reduces due to the lateral expansion of the depletion layer into the channel region, the effect of electric field increases, and the mobility of surface becomes depend upon electric field. Since the electron or hole transportationin a transistor is only within in the narrow channel which is created by voltage applied at the gate , and there is reduction of the mobility cause by the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by Ex), the electrons flow with great

difficulty parallel to the interface, so that the average surface mobility, even for small values of Ex, is about half as much as that of the bulk mobility.

Characteristics of short-channel MOSFET are also influenced by velocity saturation, that cause decreases the transconductance in the saturation mode of operation. At low E_y, the electron drift velocity V_{de} in the channel varies linearly with the electric field intensity. The drain current is also limited by velocity saturation instead of pinch off. This happens in short channel MOSFET when the dimensions of the MOSFET are scaled without lowering the bias voltage

2.3 Impact ionization

It is also a kind of short-channel effect which is undesirable, especially in N-channel MOSFET, it happens because of the high velocity of electrons due to existence of high longitudinal fields that cause generation of electron-and hole (e-h) pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them. It occur as following: generally, electrons tries to accumulate near to drain, while the holes tries to inter the body(substrate) to form the parasitic body current. Furthermore, the channel induced between the source and the drain can operate like the base of an n-p-n MOSFET, with the source working as the emitter and the drain working as of the collector. If the aforementioned holes are attracted by the source, and the corresponding hole current induces a voltage drop across the substrate material in the range of 6V, the reversed-biased substrate-source p-n junction will start conducting conduct appreciably. Consequently electrons inject from the source into body, which is similar to the injection of electrons from the emitter to the base of bipolar junction transistor. They can achieve enough energy when they travel toward the drain to induce new of electron and hole pairs. The situation become worsen if some electrons generated by the effect of high fields escape the drain field to travel into the body, consequently affecting other part on a chip.

2.4 Hot electrons

Another impact or problem, due to high electric fields, is caused by called hot electrons. These electrons with high energy can go to the oxide, where they might be trapped, and results oxide charging that can increases with time and effect the MOSFET characteristics by increasing threshold voltage and affect badly the gate's control on the current which is induced in channel.

So because of the above mentioned limitations in conventional MOSFETs we moved on to the next structure i.e. conventional silicon on insulator MOSFET.

2.5 Silicon on insulator MOSFET

(A) SOI MOSFET stands for silicon on insulator MOSFETs.In this kind of structures a semiconductor layer for example, germanium,silicon is formed above an insulator layer which may be a buried oxide layer formed on a semiconductor substrate.

Types of silicon on insulator MOSFET:

Partially Depleted (PD)

Fully Depleted (FD) SOI MOSFETs

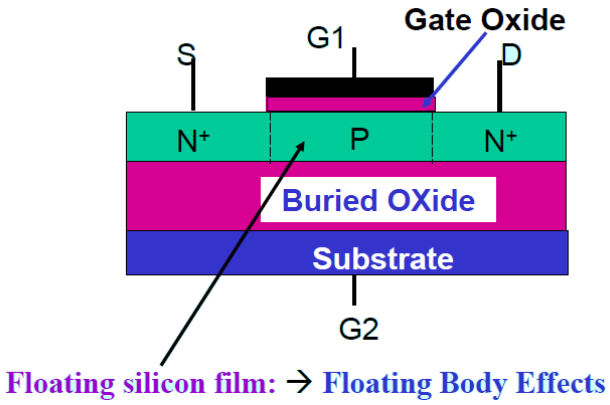


Figure 7:SOI MOSFET Structure

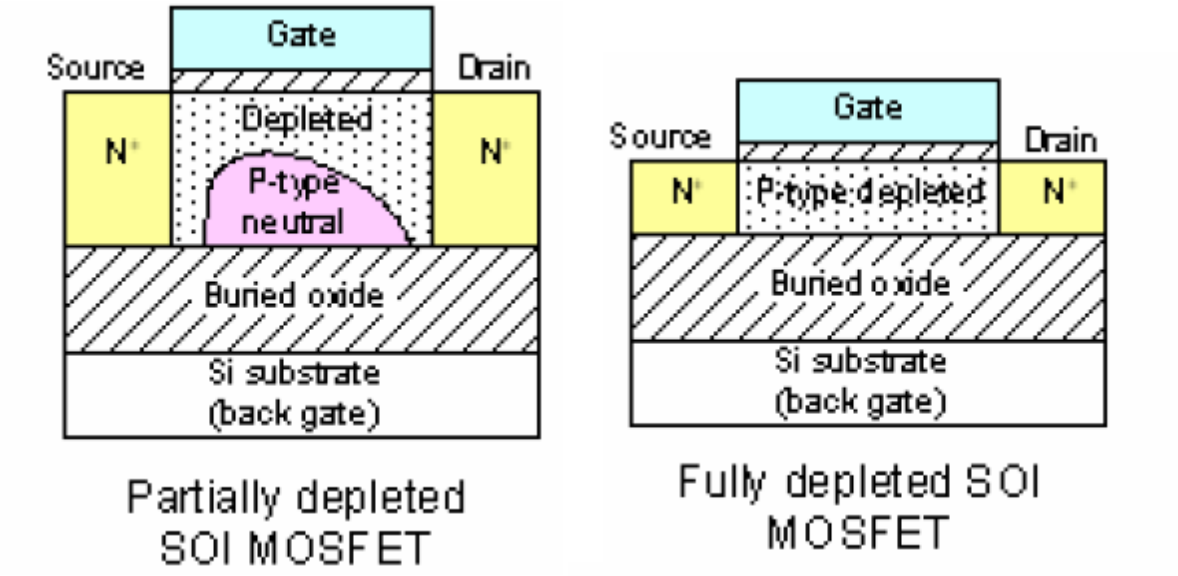


Figure 8:(a)PARTIALLYDEPLETED and fully depleted SOIMOSFET

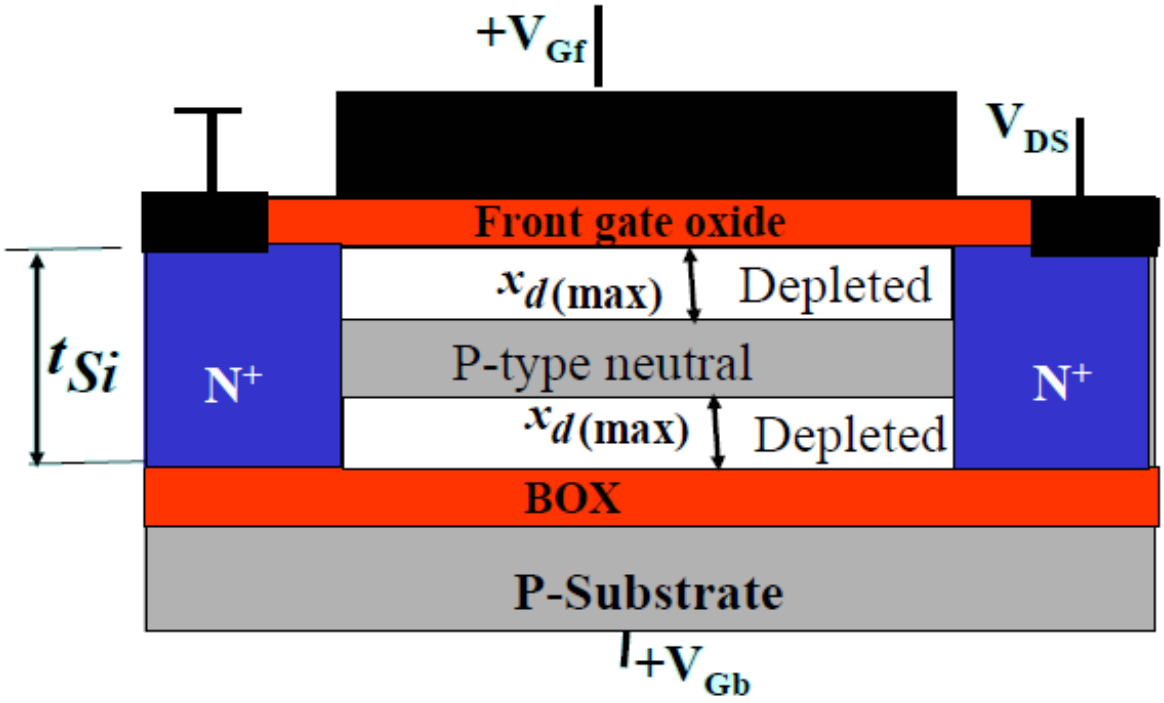


Figure 9: Cross sectional of MOSFET

The basic device equations of PD SOI MOSFETs are the same as for bulk devices, except of course from the complications arising from the floating body (FBE).

FULLY DEPLETED SOI MOSFETS

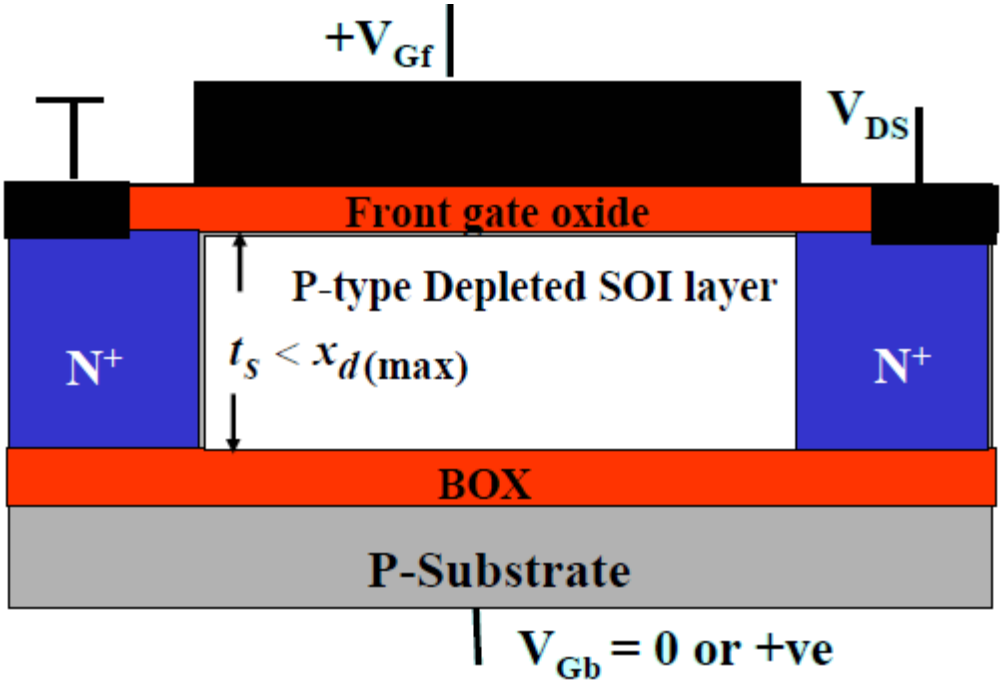


Figure 10: Fully depleted SOI MOSFETS

In FDSOI case, the front and back channels are electro-statically coupled during device operation**.** This electrostatic coupling makes the front channel FD device parameters dependent on the back gate Voltage, including drain current, threshold voltage, sub-threshold slope etc.

Chapter 3

Results and Discussion

3.1 Simulated Structure of Silicon on Insulator MOSFET

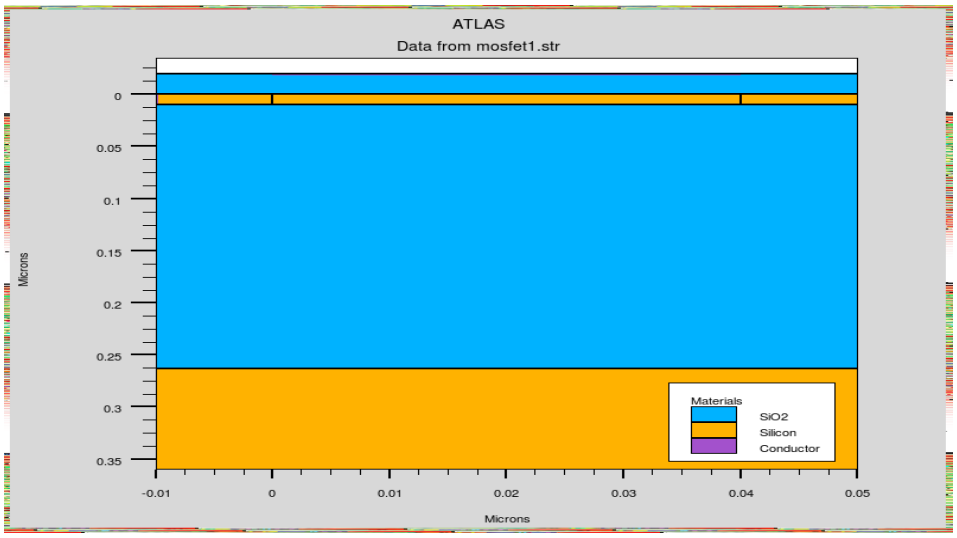


Figure 11:Simulated Structure of SOI MOSFET with work function of 4.8

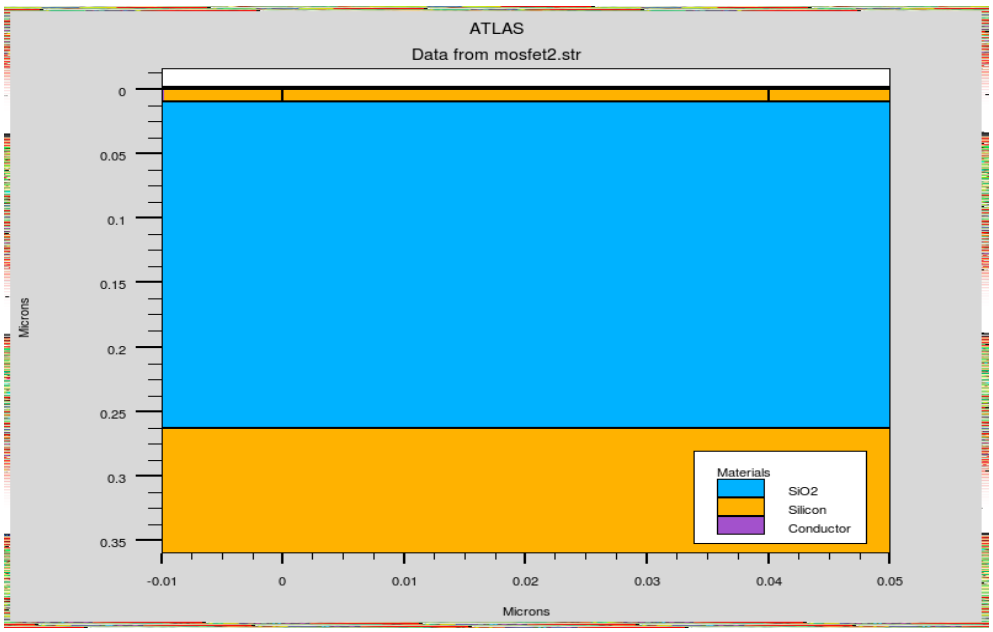


Figure 12: Simulated Structure of SOI MOSFET with work functions of 4.8 and 4.6

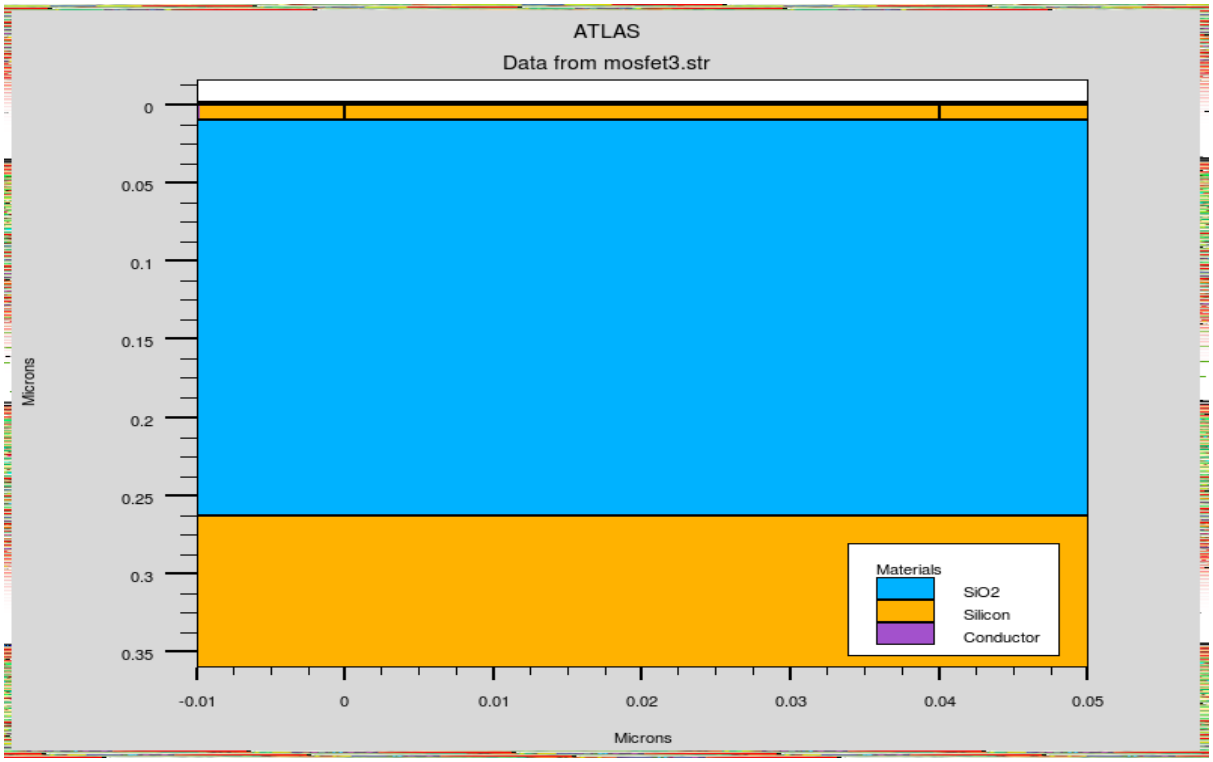


Figure 13: Simulated Structure of SOI MOSFET with work functions of 4.8, 4.6 and 4.4

- The simulated structures mentioned in the previous slides are similar except in gate materials.
- Region one is silicon dioxide layer of 2nano-meter on the top of drain,source and gate
- Region tow-gate region of length forty nano-meter and width 10nanometer
- Region three is oxide layer of silicon dioxide with the length andwidth respectively 60nanometer and 250nanometer
- Region four is substrate of silicon under insulator of length and widthof 60nanometer and 100nanometer respectively
- Region five is source region of length and width10 nanometer and 10nanometer respectively

- Region six is drain region of length and width 10nanometer and10 nanometer respectively

So by partition of the above structure into definite regions, we have been able to design the structure correctly. The box area is made of silicon dioxide.And body is made of silicon.

The Doping Profile of the simulated Structures are all similar and given below:

- The doping density in region2---uniform, p-type 1e16
- The doping density in region 4------uniform, p-type, 1e16
- The doping density in region 5------uniform, n-type, 1e18
- The doping density in region 6------uniform, n-type, 1e18

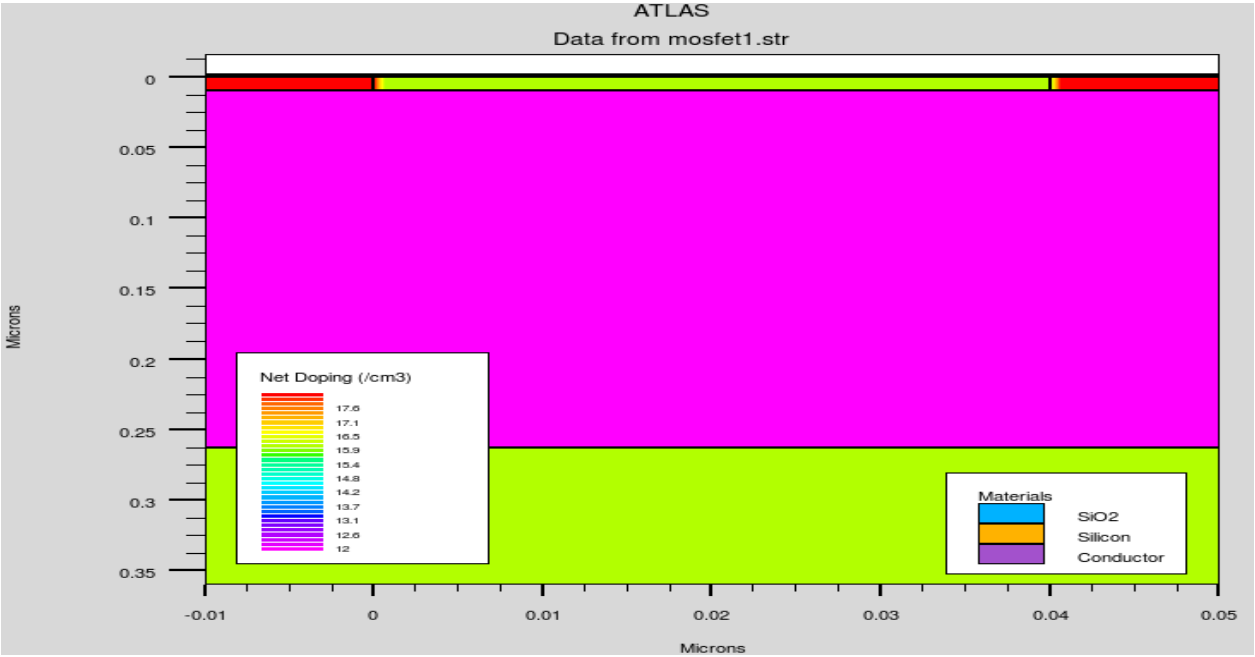


Figure 15: Doping profile

3.2 Various Curves and Their Analysis

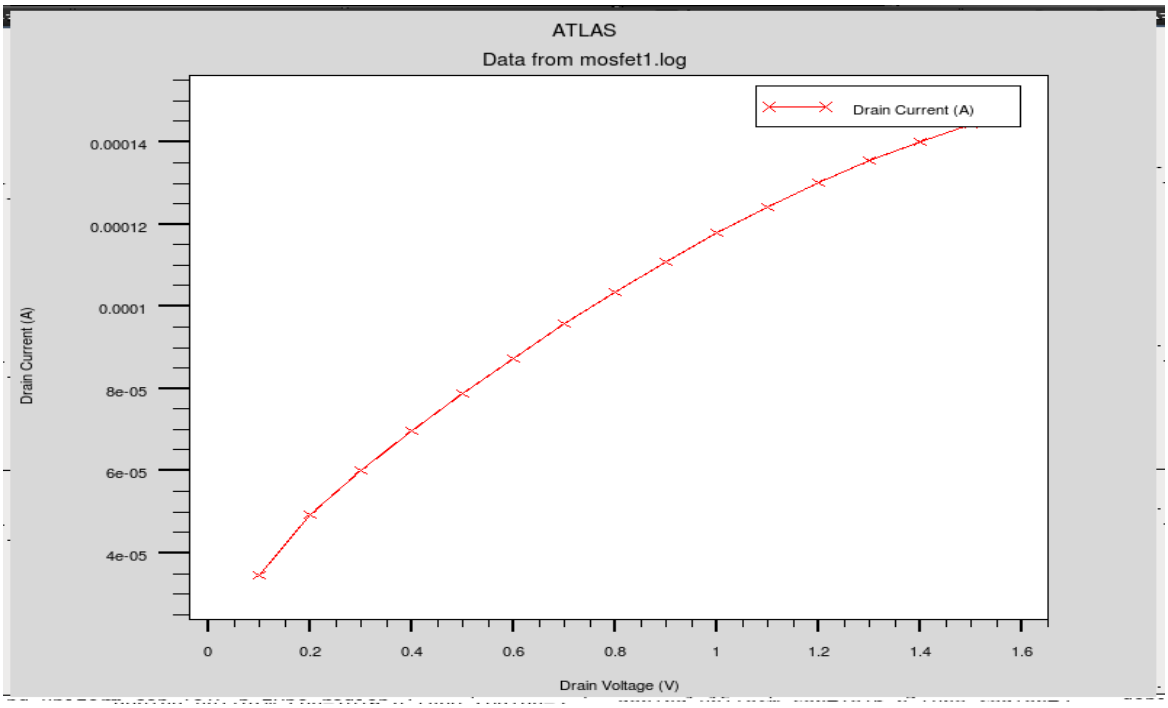


Figure 16:ID vs VD Curve for Single Material Gate

Analysis:

The curve between drain current and drain voltage was obtained by varying thevalue of gate voltage between 0.1v to 0.7v. Different values of drain current i.e. id values were obtained for different values from 0.1v to 1.5v of drain source voltage. Hence the corresponding curve was plot using the data obtained from atlas software.

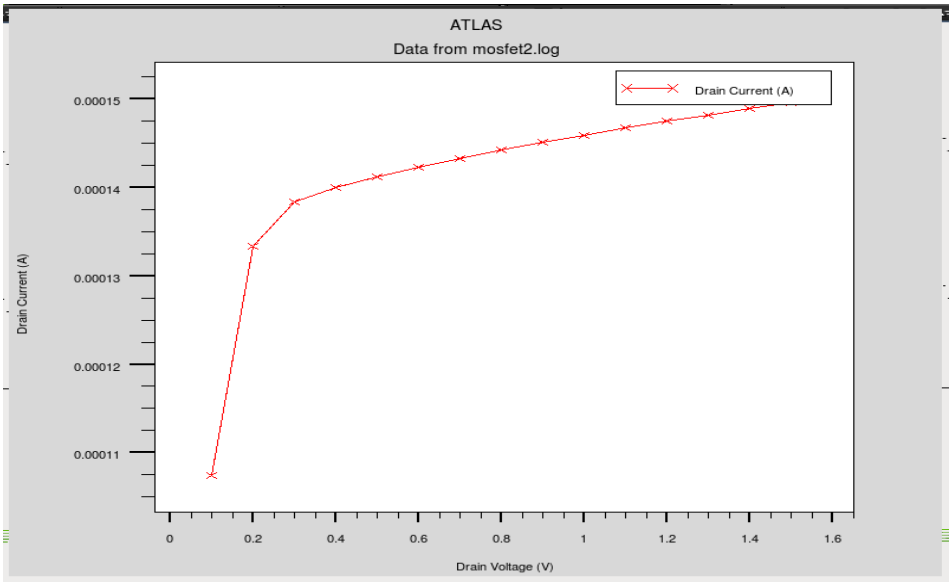


Figure 17: Id vsV_d Curve for Dual Material Gate

Analysis:

The curve between drain current and drain voltage was obtained by varying thevalue of gate voltage between 0.1v to 0.7v. Different values of drain current i.e. id values were obtained for different values from 0.1v to 1.5v of drain source voltage. Hence the corresponding curve was plot using the data obtained from atlas software.

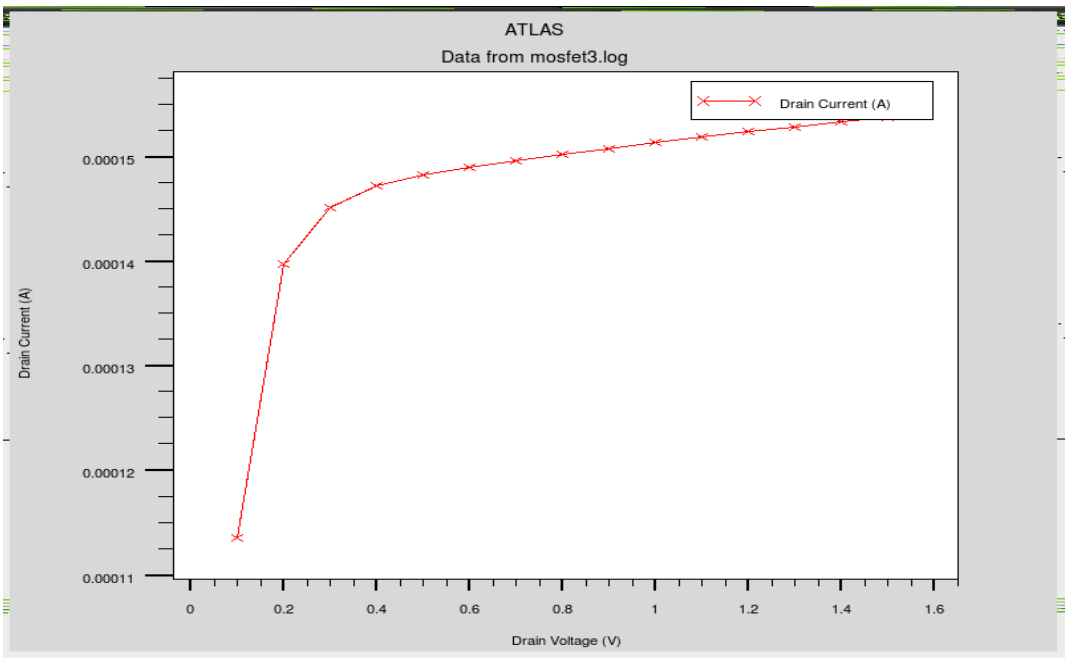


Figure 18: Id vsV_d Curve for Triple Material Gate

Analysis:

The curve between drain current and drain voltage was obtained by varying thevalue of gate voltage between 0.1v to 0.7v. Different values of drain current i.e. id values were obtained for different values from 0.1v to 1.5v of drain source voltage. Hence the corresponding curve was plot using the data obtained from atlas software.

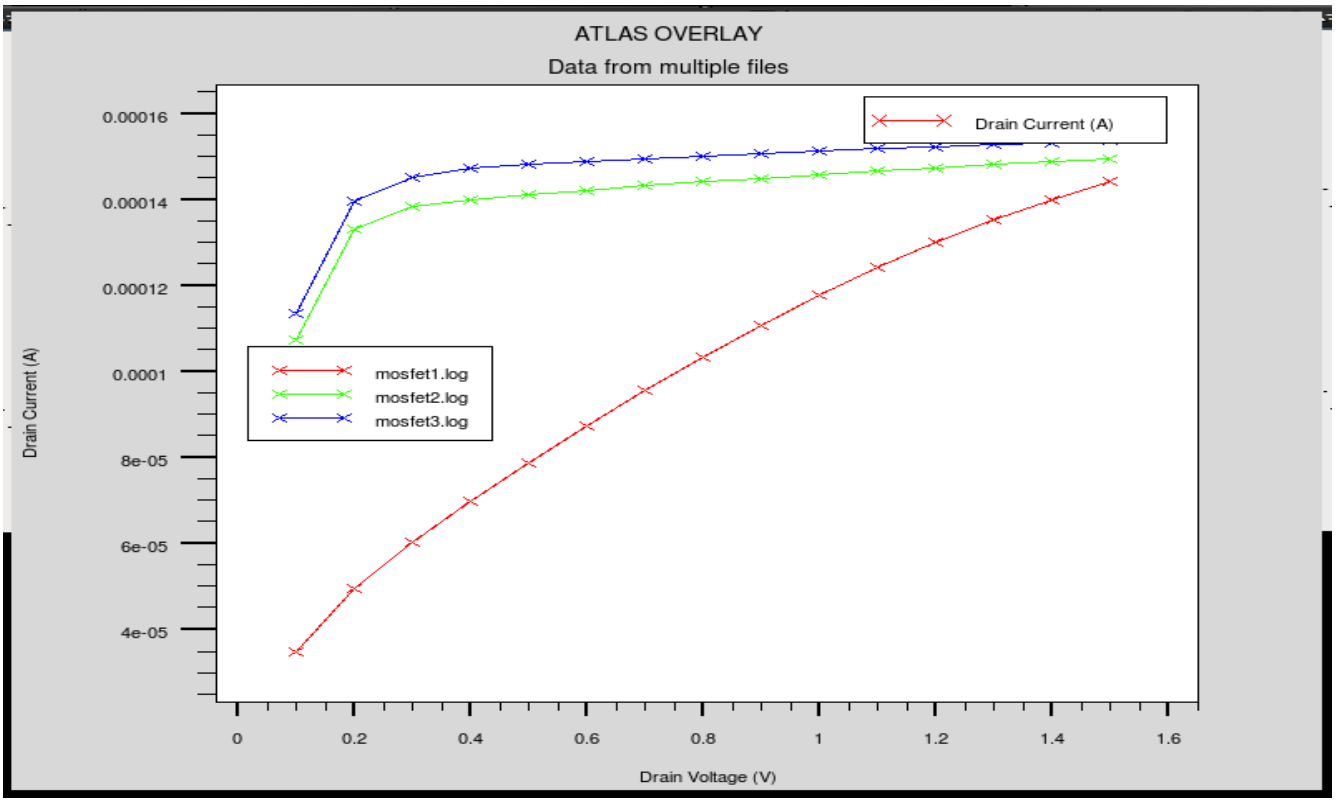


Figure 19: Comparison between the Id vs V_d curves

Analysis:

Characteristics of triple, dual material and single material gates structures are compared to each other for same channel length L=40nm.

From the graph it can be seen that the drain current of TMG is greater than SMG and DMG, where the drain current of DMG is greater than SMG. becauseof the difference in threshold voltages.

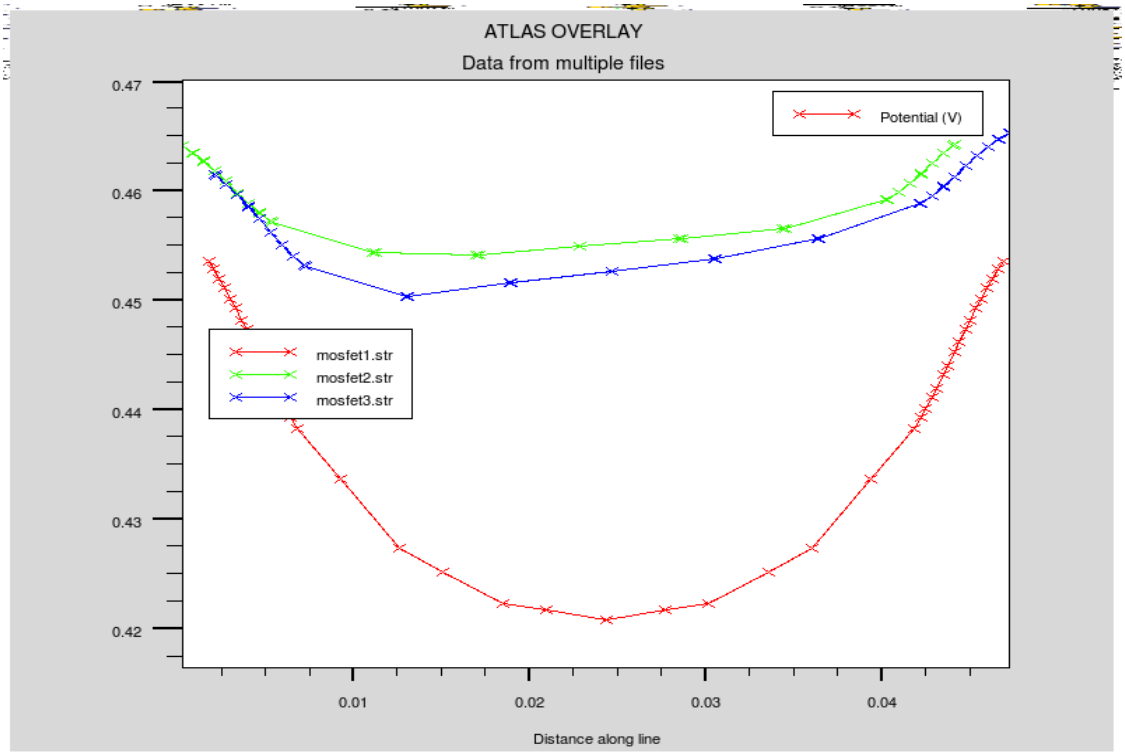


Figure 20: Surface Potential vs Channel Length of different Material Gate

Analysis:

It can be observed that the barrier height of SMG structure is more than Double Metal Gate (DMG), and that of DMG is more than TMG, so the

surface potential of TMG is higher than DMG, and DMG is higher than SMG. So threshold voltage of TMG is lower than DMG, and DMG is lower than SMG.

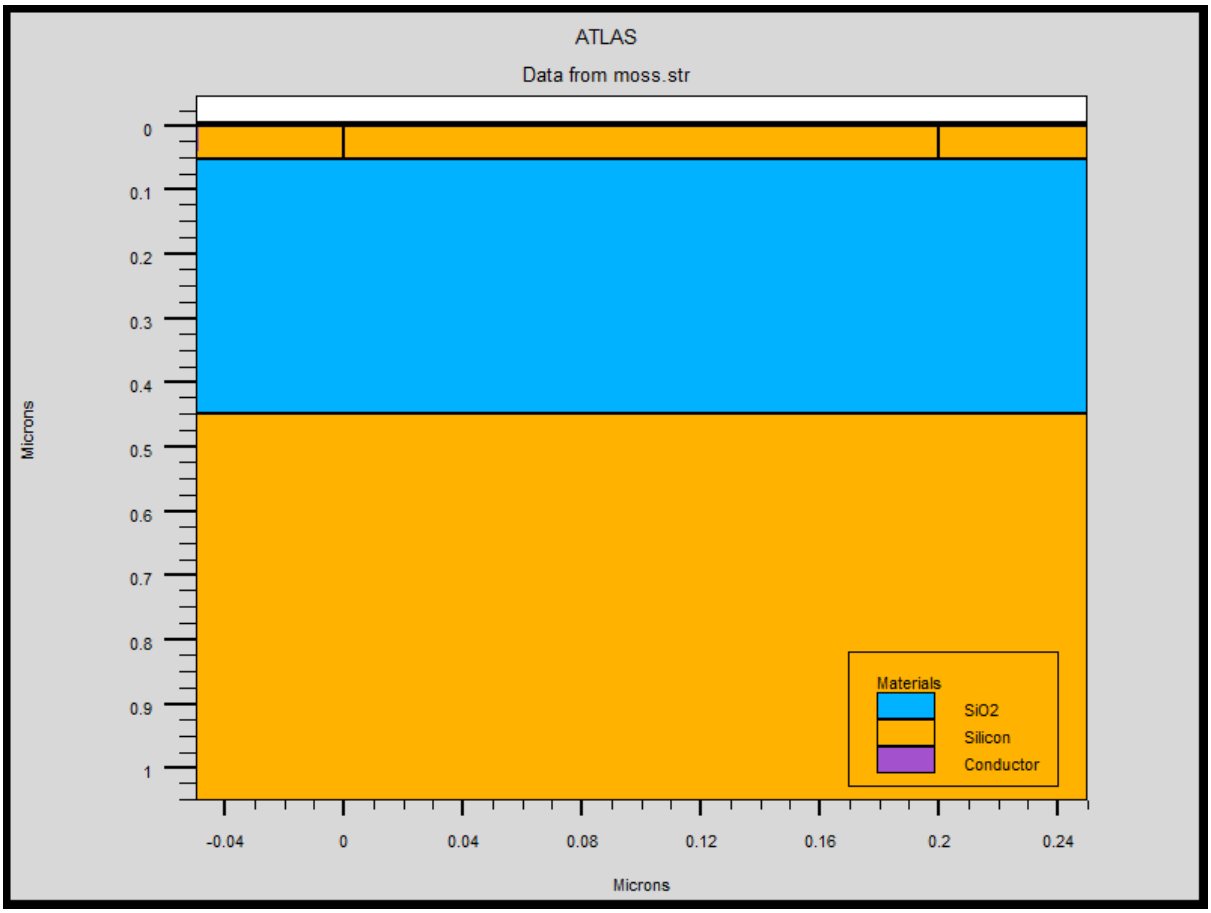


Figure 21: Simulated Structure of DMG SOI MOSFET with work function of 4.8 and 4.2.

Description of simulated structure of FD SOI MOSFET:

Region one-silicon dioxide layer of 5nm on the top of drain,source and gate

Region tow-gate region of length 200 nm and width 50 nm

Region three – silicon dioxide(sio2) with length and width of 500nm and 300nm respectively

□□Region four-body(substrate) of silicon under insulator of length and width of 500nm and 600nm respectively

□□Region five- source area with length and width equal and 50nm

□□Region six-drain area with length and width equal and 50nm

So by partition the mentioned structure into distinguish regions, we can design the MOSFET structure correctly. The box region is made of silicon dioxide(sio2).and body or substrate is made of silicon(SI).

The Doping Profile of the simulated Structures are all similar and given below:

- The doping density in region tow is uniform, and is p-type 5e16
- The doping density in region four is uniform and is p-type, 5e16
- The doping density in region five is uniform and is n-type, 6e19
- The doping density in region six is uniform and is n-type, 6e19

Simulation result are as follow :

The structure of MOSFET is simulated by use of SILVACO atlas simulator to explain the characteristics

of dual material gate silicon on insulator with and compare to the single material gate silicon on insulator

The aim is to compare their threshold voltage (v_t), saturation current and leakage current

A. characteristics of MOSFET at constant channel length:

The structure of MOSFET is simulated to understand characteristics MOSFET for different values of channel length of gate one(L1), and all other parameters have taking theirsame values.

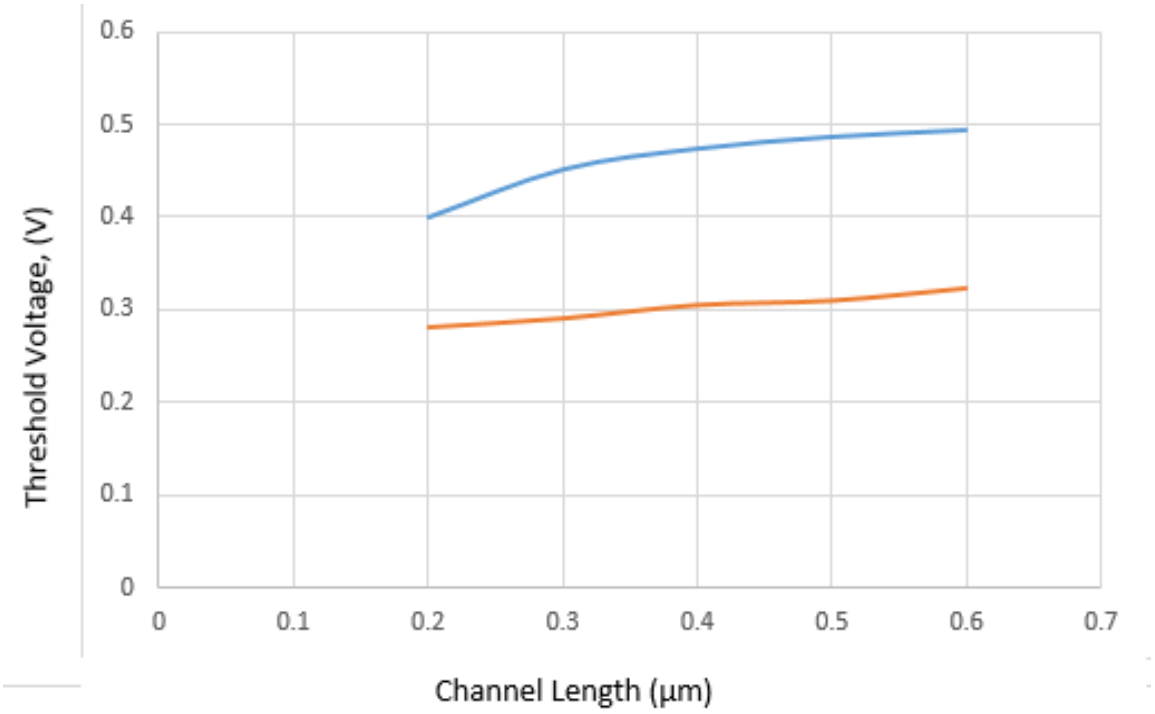


Figure 22: Threshold voltage versus channel length of DMG and SMG

As shown in the above figure most improvement of dual material gate over single material gate MOSFETis threshold voltage (vt). In dual material gate the threshold voltage is less sensitive compare to that of single material gate which is very important for design of MOSFET with very small channel length.

B. Effect of RatioL1/L2 when the channel length is constant:

When the total channel length is fixed and is equal to (L), the location of the potential step is possible toregulate for different ratio ofthe L1/L2. This characteristicis studied with ranging single material gate length from 0to 0.15µ m at total channel length fixed and equal to 0.2µ m for the understanding parameters of threshold voltage and VDIBL:

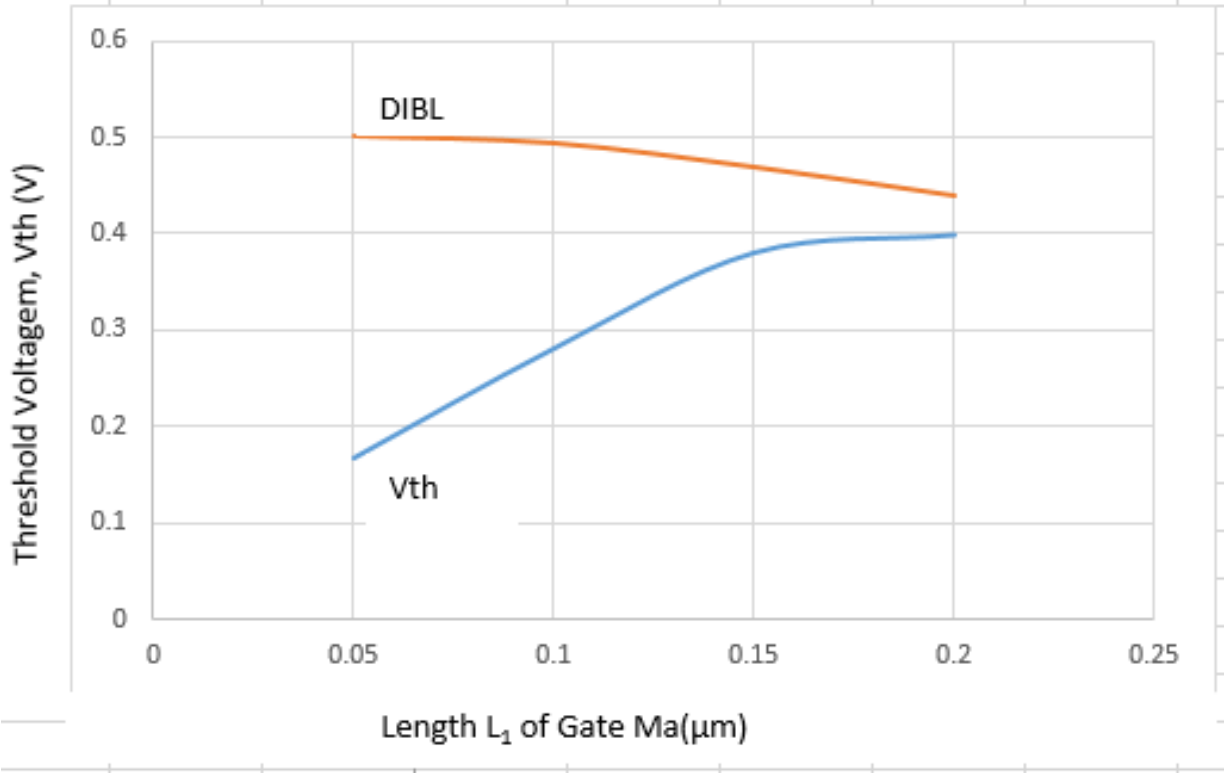


Figure 23: Threshold voltage and DIBL versus channel of gate one

as shown in the above graph when the L1 is increases the L1/L2 ratio is also increases, consequently threshold voltage (v_t) is increases .and VDIBL is curve is decreases it means effect of drain voltage or drain electric field on conducting path is reduces .it can be seen that as L1value is increases and approaches to the total channel length LVDIBL is also reduces and MOSFET start to operate as a single material gate with large work function .so it means the dual material gate MOSFET has better performances than that of single material gate.

Channel length L1(In Micrometer)	Off state current at Vg=0.1v in A	On state current at Vg=1 v In A
0.0	$3.5x10^{-5}$	0.0004019
0.05	$2.11x10^{-6}$	0.0002865
0.1	$5.5x10^{-8}$	0.0002191
0.15	$3.3x10^{-10}$	0.00015275
0.2	$1.225x10^{-10}$	0.0001385

Table one: Channel length VS I_{off} and I_{on}:

Above table indicates that as L1 is increasing the leakage current is also decreasing. This is because of the threshold voltage increases as L1 increasing.

Trans conductance = ΔId /ΔVg = gm

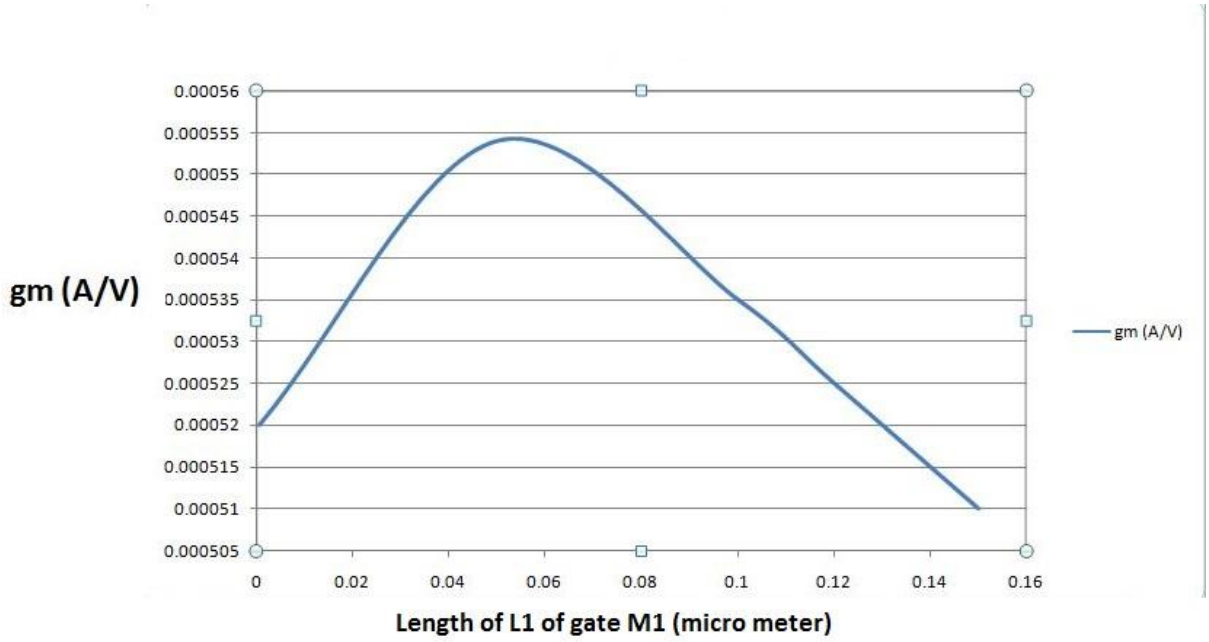


Figure 24:Transconductance versus length of L1 of gate M1

As shown in the above graph the variation of transconductance as a function of L1 in a fully deplete MOSFET. It can be seen that gm is higher for dual material gate with compare to single material gate (L1=0) .asL1 screened the total cannel length L, MOSFET become a single material gate SOI with a higher work function.

Drain conductance = ΔId /ΔVd = gd

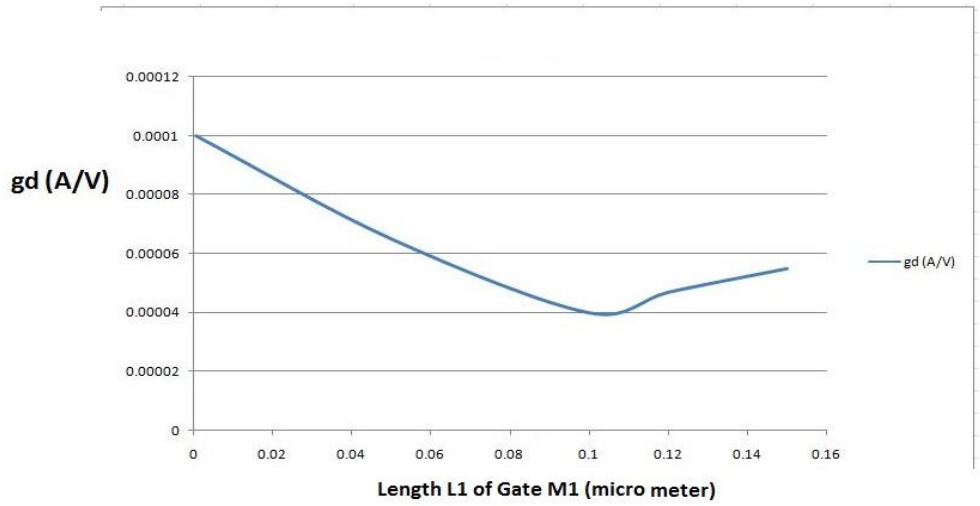


Figure 25: Drain conductance versus length L1 of gate M1

Above graph indicate that drain conductance(gd)reduces as the L1is increases and the MOSFET operate as a single material gate MOSFET consequently the drain current influence is reduces over channel conductivity so dual material gate has better performances .

Gain = gm/gd

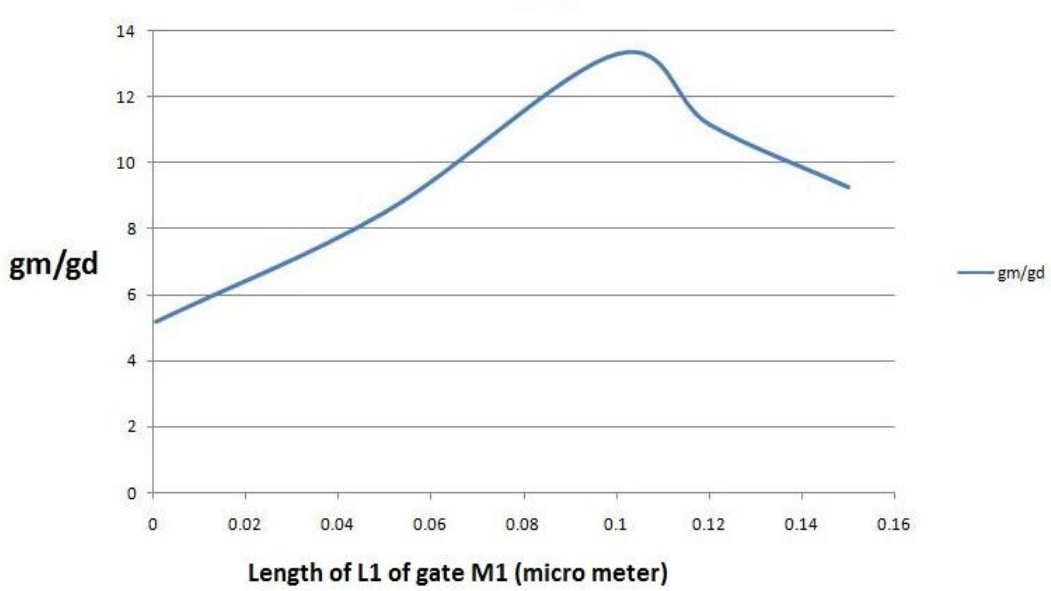


Figure 26: Gain versus length L1 of gate M1

It can be observed from above graph voltage gain is increases as the MOSFET approaches to dual material gate and gain is maximum at the L1/L2 is equal to

unity .so above graph demonstrate that the optimum ratio of channel length is unity .

Effect of Work function Difference when the total Channel Length L is fixed:

When the ratio of L1/L2 is kept fixed and equal to unity, the influence work function difference between metal one(M1) and metal tow (M2) is investigated. Andhowitchanges the electrical characteristics of the dual material gate SOI MOSFET. here we onlychanged work function of metal one(M1) and The work function of metal M2 is held constant and equal to 4.4 e v.

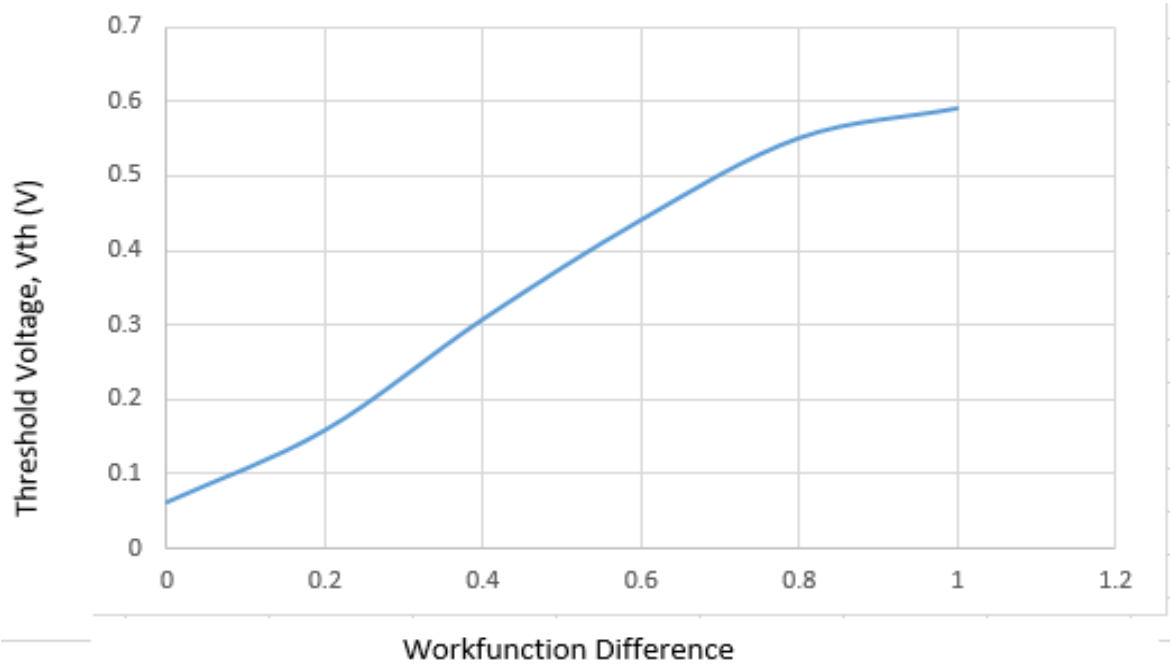


Figure 27: Threshold voltage versus work function difference

Above graph indicates that when the work function difference is high threshold voltage increases here we kept ratio of L1 and L2 at unity. So we conclude that high work function difference cause large threshold voltage which is not desirable for sub micron SOI MOSFET.

3.3 Conclusion:

Dual material gate MOSFET is proposed to reduce the short channel effect In a single material gate according to the simulation result MOSFET with different work function in the gate provide better control over the channel and decreases the short channel effect And also the results showed that dual material gate MOSFEThas smaller trans conductance and higher drain conductance compared to that of single material gate.

Also the simulation results show that the optimum ratio of L1 and L2 is unity, and optimum work function difference is equal to 0.4 e.v for a fully depleted dual material gate MOSFET.

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