DESIGN AND ANALYSIS OF EFFICIENT PHASE LOCKED LOOP

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Bachelor of Technology

By

MALOTHU DILIP KUMMAR NAIK

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Department of Electronics and Communication Engineering

National Institute Of Technology

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Under the Guidance of

Prof. D. P. ACHARYA

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CERTIFICATE

This is to certify that the thesis entitled, **"Design and Analysis of an Efficient Phase Locked Loop "** submitted by **Malothu Dilip Kumar Naik** in partial fulfillment of the requirements for the award of Bachelor of Technology Degree in Electronics & Communication Engineering at the National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

Date:

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Acknowledgement

This undertaking is by a long shot the most noteworthy accomplishment in my life and it would be unthinkable without individuals (particularly my family) who upheld me and had faith in me.

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MALOTHU DILIP KUMAR NAIK

ROLL No: 111EC0171

Dedicated to my Parents

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Abstract

Phase Locked Loop is one of the most important component in design of almost all electronic goods . In modern communications PLL circuit has a wide applications in radio, telephone, mobile phone, PCs and other electronics applications. Phase Locked Loops are used for synchronization , synthesis of clock and jitter reduction in mobile or wireless communications. Due to the increment in the rate of the circuit operation, there is a need of a PLL circuit with quicker locking capacity. PLL is designed to operate both for analog and digital signal processing. For demodulating a signal and recovering it to its original input signal, PLL circuit is used. PLL has a wide application in higher frequency ranges (GHz) as they lock the frequency in less span of time. The main theme of the work is to design a Phase Locked Loop. PLL is designed in CADENCE Virtuoso Analog Design Technology using 90nm process Technology (GPDK90). For this a Current Starved Voltage Controlled Oscillator has been taken with which the required frequency is obtained at certain voltage.

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CHAPTER 1

INTRODUCTION

1.1 Provocation

Since its assessment in mid 1930s , where it was utilized as a part of the Synchronization of the level and vertical outputs of TV , it has arrived at a Propelled manifestation of coordinated circuit (IC) . Today discovered uses in numerous different applications. The primary PLL ICs were accessible around 1965; it was assembled utilizing absolutely simple part. Late advances in coordinated circuit outline methods have prompted the improvement of digital PLL which has ended up more efficient and solid. Presently an entire PLL circuit can be incorporated as a piece of a bigger circuit on a solitary chip .

PLL is the heart of the numerous current hardware and also Communication Systems. As of late a lot of research about have directed on the outline of Phase Locked Loop (PLL) [1-3] circuit and still research is going on this subject to improve its application in modern technology. The vast majority of the research have directed to understand a higher lock range PLL with lesser lock time and have decent stage commotion. The most flexible use of PLL is for clock locking and check recuperation in microchip, microcontrollers, microprocessors, and recurrence synthesizers . PLLs are normally used to produce very much timed on-chip checks in digital systems. Present day communication systems utilize Phase Locked Loop (PLL) basically for synchronization, synthesis of clock, skew and jitter lessening [4]. PLLs find wide application in a few cutting edge applications generally ahead of time correspondence and instrumentation frameworks. PLL being a blended sign circuit includes outline challenge at high recurrence.

Phase Locked Loop (PLL) circuit mainly consists of 5 blocks namely

1. Phase Frequency Divider (PFD)
2. Charge Pump (CP)

3. Low Pass Filter (LPF)

4. Voltage Controlled Oscillator (VCO)

5. Frequency Divider

All these component together form PLL circuit . There are many changes being taken in the design of PLL due to its applications . Some of the blocks are added to it and some of them are removed from the loop depending on the requirement. As PLL is used in higher frequency of GHz to lock them very fast , the improvement of the PLL design is increasing rapidly . VCO which is the heart of the PLL circuit has gone through lot of improvement to attain required outcomes . A resistor is added to VCO to decrease its Phase Noise and to increase its locking range.

1.2 Structure of Thesis

In 1.1, the provocation of overall thesis is explained briefly. Chapter 2 explains about the total PLL circuit and the blocks used for designing it. In 2.1, block diagram and the components of PLL are described. The architecture of PLL is described along with explanation of each and every block in 2.2.

In chapter 3, design and synthesis of PLL is explained. The technology that is used to design is explained in 3.1. In 3.2 design procedure and the schematic of every block and their respective symbols are explained.

Chapter 4 explains about simulation results of the PLL and its blocks. 4.1 gives about simulation of VCO with and without resistor. In 4.2 simulation of PFD is explained in detail. 4.3, 4.4 describes the simulations of charge pump and loop filter. Chapter 6 concludes that is theorized in the thesis.

CHAPTER 2

PHASE LOCKED LOOP

2.1 Introduction

Phase Locked Loop [1-3] is a circuit which consists of a circular loop formed by the feedback . PLL is used to lock the frequency and phase of the input signal. PLL circuit main motive is to generate a signal whose phase and frequency matches with the reference signal . The signal is given for locking should have bandwidth with in the lock range of PLL . The input or reference clock is sent to several blocks and is fed back as feedback again at the input of PLL . This feedback loop is continued until the phase and frequency of the signal is locked.

Phase Locked Loop is used in clock synthesis i.e. generation of high clock frequency from multiple low clock frequency . The feedback given is a negative feedback . PLL acts as control system which is used to control working of many electronic devices.

PLL circuit is designed in many based on the requirement for the given component. But mostly there are five components which integrate to from PLL circuit . The block diagram of PLL circuit consisting of these blocks is shown in Fig.1 . They are:-

1. Phase Frequency Detector (P F D)
2. Charge Pump (C P)
3. Low Pass Filter (L P F)
4. Voltage Controlled Oscillator (V C O)
5. Frequency Divider

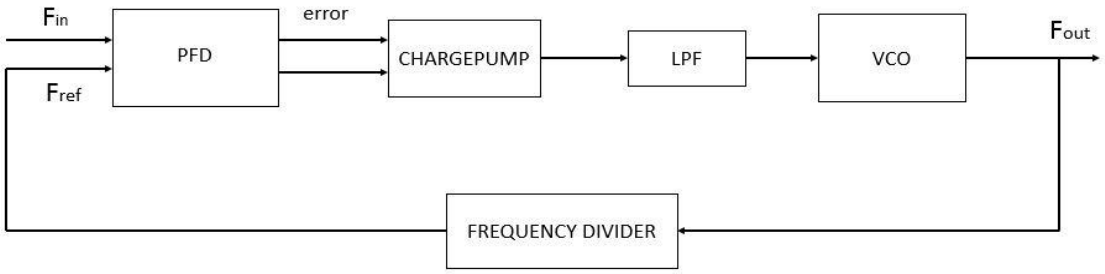

Fig :- 2.1 Block diagram of PLL

An input signal or reference signal is given to Phase Frequency Detector [5-6]. Depending upon the raising edges , PFD generates two signal outputs UP and DOWN . These output signals are sent to Charge Pump [11] which generates both positive and negative current. The output of charge pump is fed to low Pass Filter . LPF allows only the signals with low frequencies blocking the higher frequency terms that are obtained in PFD. Voltage Controlled Oscillator [3],[9-10] is the heart of PLL circuit takes the control voltage from the output LPF. The change in output of VCO depends on the DC control voltage i.e. the output of PFD. Phase and frequency values of VCO increases due to increase in error voltage of PFD by the generation of UP at the output of PFD. In contrast, The frequency and phase of VCO output decreases due to decrease in control voltage obtained at LPF due to generation of DOWN at output of PFD.

2.2 PLL Design

Phase Locked Loop circuits are designed in many ways i.e. depending on their requirement their structure and number of blocks changes . Most commonly used are five to obtain the basic PLL circuit. The design of PLL circuit is shown in Fig. 2.2 . The main blocks of PLL are Phase Frequency Detector, Charge Pump, Low Pass Filter, Voltage Controlled Oscillator and Frequency Divider. A detailed explanation of all the blocks is given below.

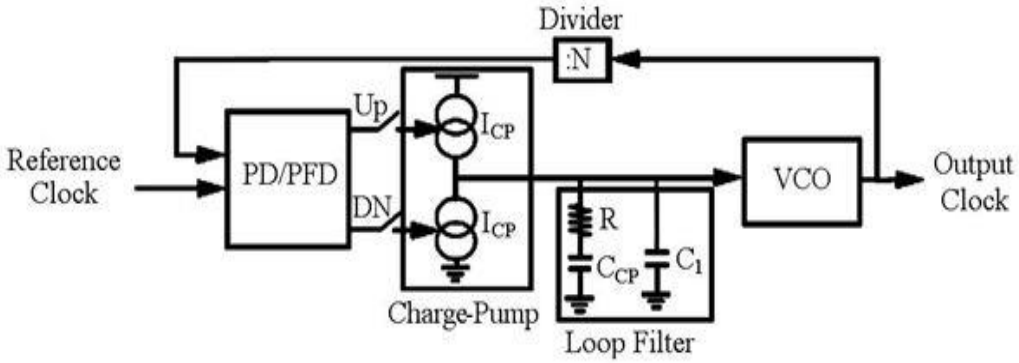

Fig. 2.2 Architecture of PLL Circuit

2.2.1 Phase Frequency Detector

One of main blocks of PLL circuit is "Phase Frequency Detector [5] (P F D)", which is the initial block of PLL circuit. It has two input ports one having input or reference signal whose phase and frequency to be locked is fed to PFD. And the other is the feedback signal that is given by the feedback path. Different types of PFD's are available in the market depending upon their requirement at the particular filed. Some of them are Conventional PFD's, PFD's with N transistors, where n is integer , PFD with variable delay element etc…The circuit design conventional PFD shown in Figure :- 2.3. Depending the change in Phase and frequency PFD generates two signals UP and DOWN. If the feedback signal raising edge is lead by the input signal raising edge then UP is generated at the output. In contrast, if the input signal raising edge is lead by the feedback signal raising edge then DOWN is generated at the output of the PFD. The output of PFD is fed to Charge Pump to continue further process.

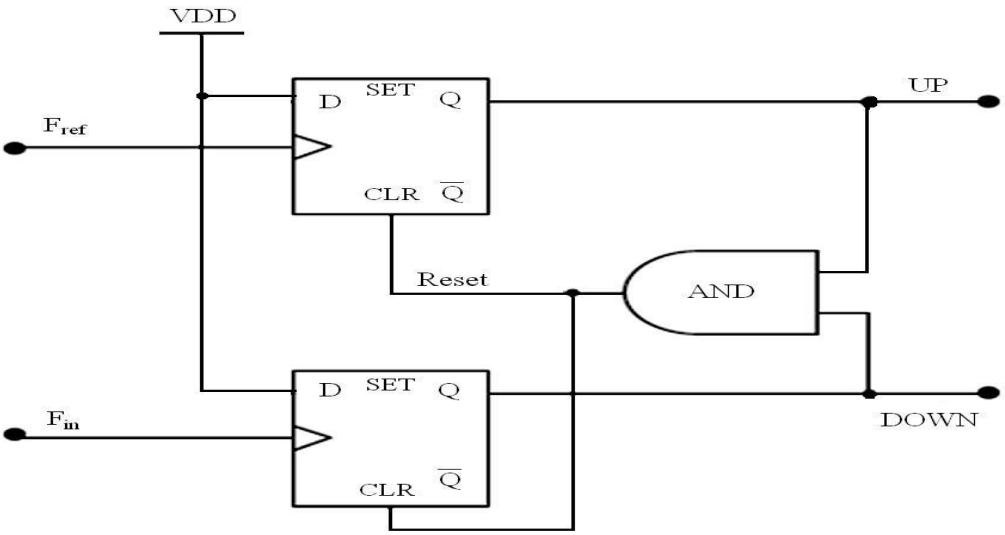

Fig. 2.3 Traditional PFD

2.2.2 Charge Pump

Charge Pump [11] is a circuit that works as DC to DC converter. In PLL it is placed in between PFD and Low Pass Filter. Although it has many applications in present design of PLL circuit, it generates positive and negative currents. So it called as current synthesizer or we can also say that it generates voltage. Depending on the voltage generated in charge pump the output of the VCO changes. It receives two input signals from PFD and converts it to single output value.

Many charge pumps are developed on the requirement. Some of them are Gain-Boosting CP [12], Transmission Gate CP, Ratio current CP [13] etc…All these CP's strive to reduce current mismatch, reference spur and fluctuations in the input of VCO. Their circuit diagrams are shown in Fig. 2.4.

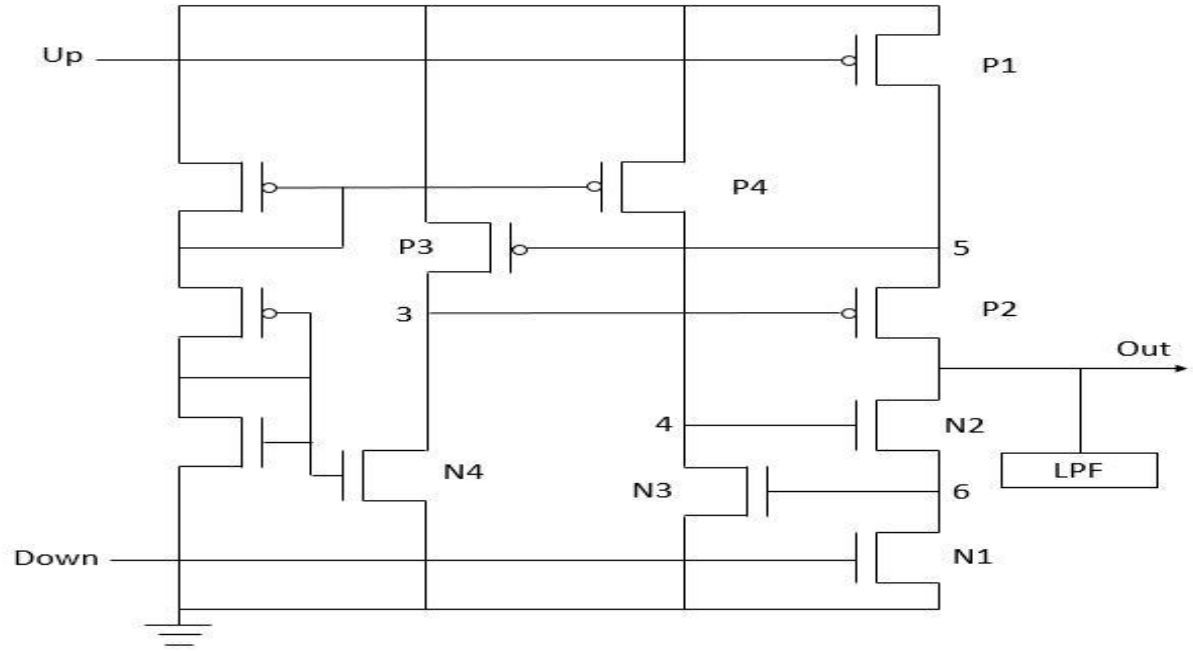

Fig. 2.4a Gain Boosting Charge Pump [12]

The advantage in Gain Boosting charge pump is to reduce the current mismatch which may generate fluctuations in PLL. While ratio current charge pump may suppress the magnitude of reference spur. To obtain this the size of source and drain are changed.

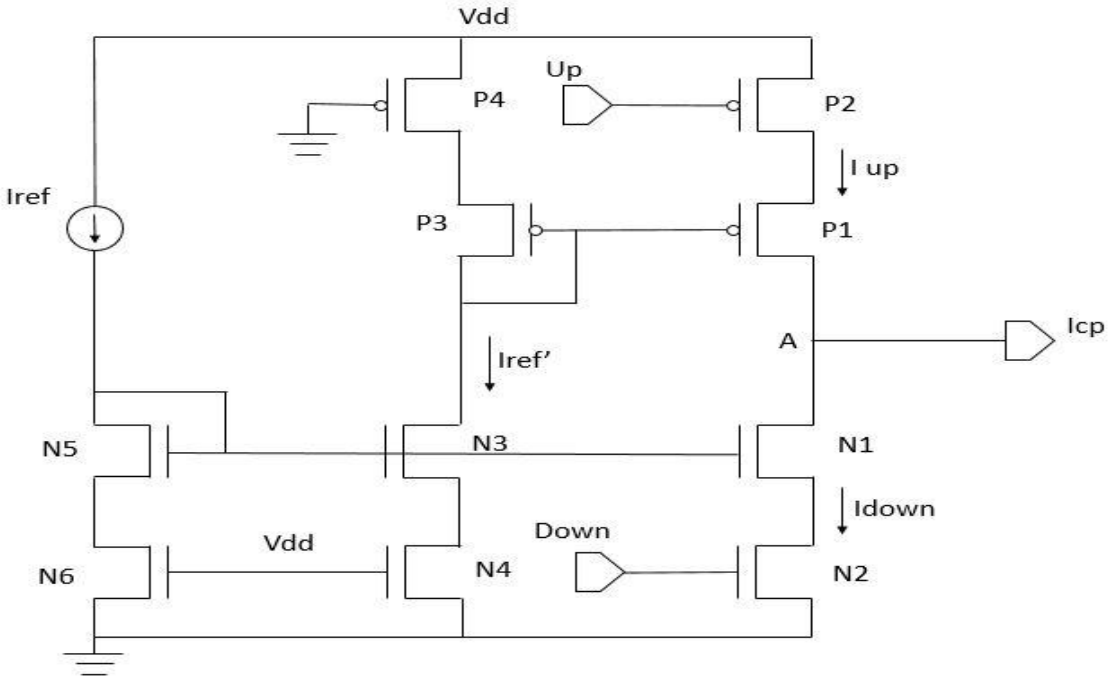

Fig. 2.4b Ratio Current Charge Pump [13]

2.2.3 Low Pass Filter

Low Pass Filter [8] is used to block the high frequency signals from the PFD and allows only low frequency signals. It generates DC voltage by which the output is varied. This DC voltage is used to control the output frequency of the Voltage controlled oscillator. The output of LPF is fed to VCO input and it is given by the equation. The DC voltage of LPF depends on input and reference frequency. If both are same and so they are locked then it maintains constant value. A simple low pass filter circuit is shown in Fig. 2.5.

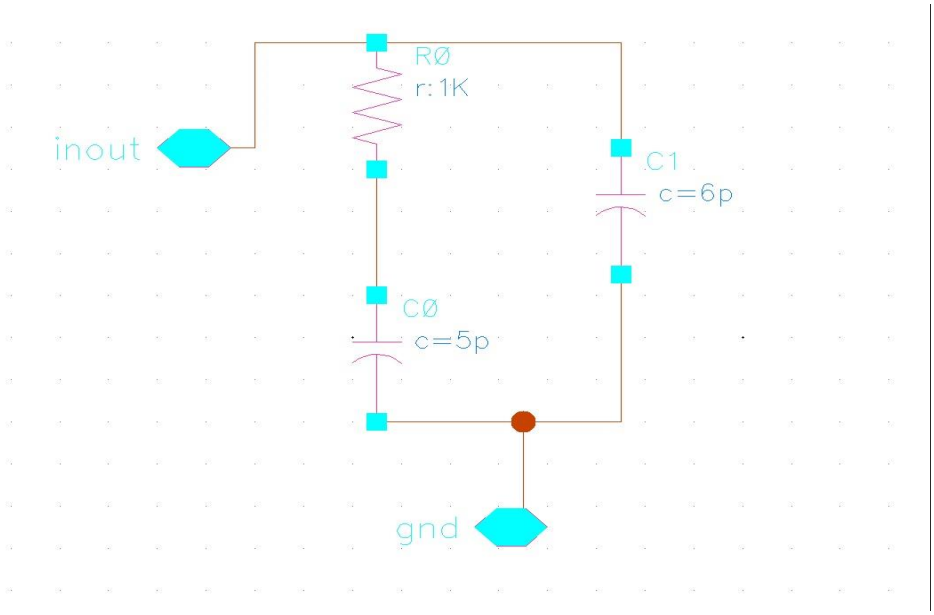

Fig.2.5 Low Pass Filter

2.2.3 Voltage Controlled Oscillator

Voltage Controlled Oscillator [3] is the heart of Phase Locked Loop. It take a DC voltage as input and gives the corresponding frequency. The output voltage of LPF is fed to VCO based on that controlled VCO generates frequency. There are many types of VCO available among them Current Starved Voltage Controlled Oscillator is pretty simple and has great working efficiency. A simple diagram of CSVCO is in Fig. 2.5

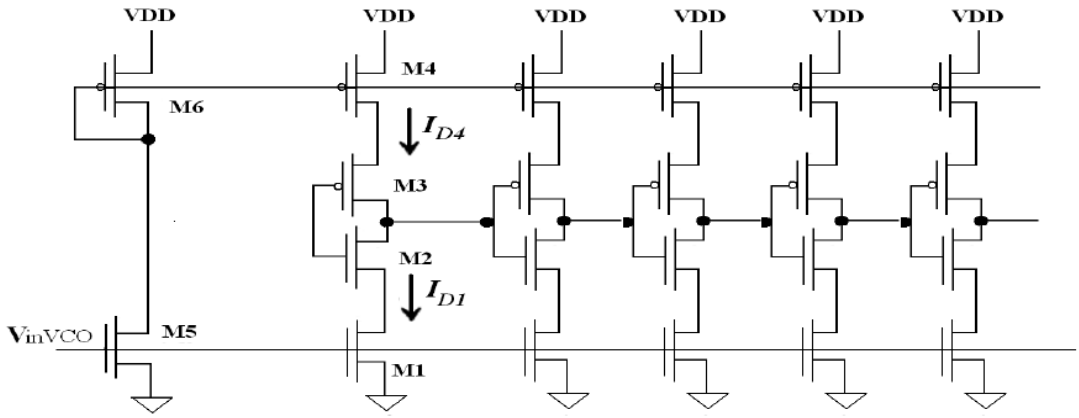

Fig. 2.6 Diagram of 5-stage CSVCO [9-10]

From the figure we can depict that Transistors M2 and M3 act as inverter and M1 and M4 are current sources. M1 and M4 limits current to inverter and then inverter is starved for current. At 1.8V the desired frequency is 1GHz.

2.2.4 Frequency Divider

Frequency Divider [14] is used to reduce the frequency that is obtained from VCO. It forms a closed loop in PLL as it is placed in feedback path. Frequency Divider is a simple Pass transistor based D-Flip flop and it divides a frequency by a factor of two. A simple circuit of D flip flop is shown in Fig. 2.6

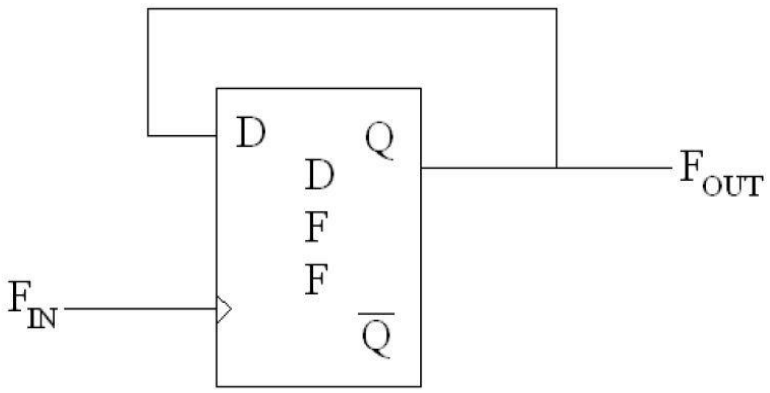

Fig.2.7 Simple D-Flip Flop used for Frequency Divider

CHAPTER 3

DESIGN AND SYNTHESIS OF PLL

3.1 Design Technology

All the circuits are designed in CADENCE Virtuoso Analog Design Environment in GPDK90 library. Their Transient analysis, Power consumptions , Phase noise , PSS all these parameter are checked to find how efficient PLL is working.

3.2 Design Procedure

3.2.1a VCO Design without resistor

VCO is the main part of PLL so precautions should be taken while designing it. VCO designed here is 5-stage current starved VCO. We have to check and implement each and every block or transistors while designing. The propagation delay of all inverter should be verified. The W/L values of transistors should be found. Then W and L values should be found individually. The connections that are made should be verified carefully.

The schematic of CSVCO designed in Cadence is shown in Fig.3.1. At the input of VCO, a controlled voltage between 0.1 to 1.8V range is given to find the frequencies at the respective voltages. W/L values of transistors are taken according to our requirement.

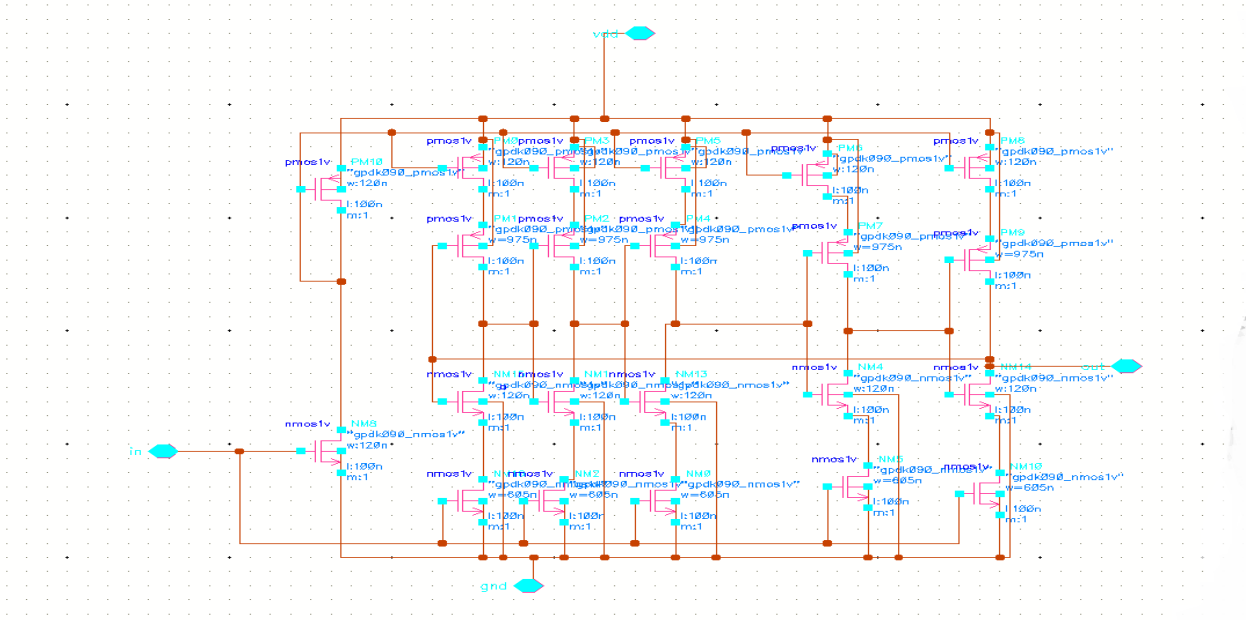

Fig. 3.1 Schematic of 5-stage CSVCO

3.2.1b VCO Design with resistor

VCO designed in Fig. 3.1 has not given some specific requirements in Tuning Range, Phase Noise, PSS, Central frequency, Power consumption. In order to get improvements in these parameters a resistor is added to VCO. This is shown in Fig.3.2. After adding resistor, the efficiency of VCO has increased. Tuning range increased, Phase has reduced and also reduction in average power consumption which are discussed in following chapters.

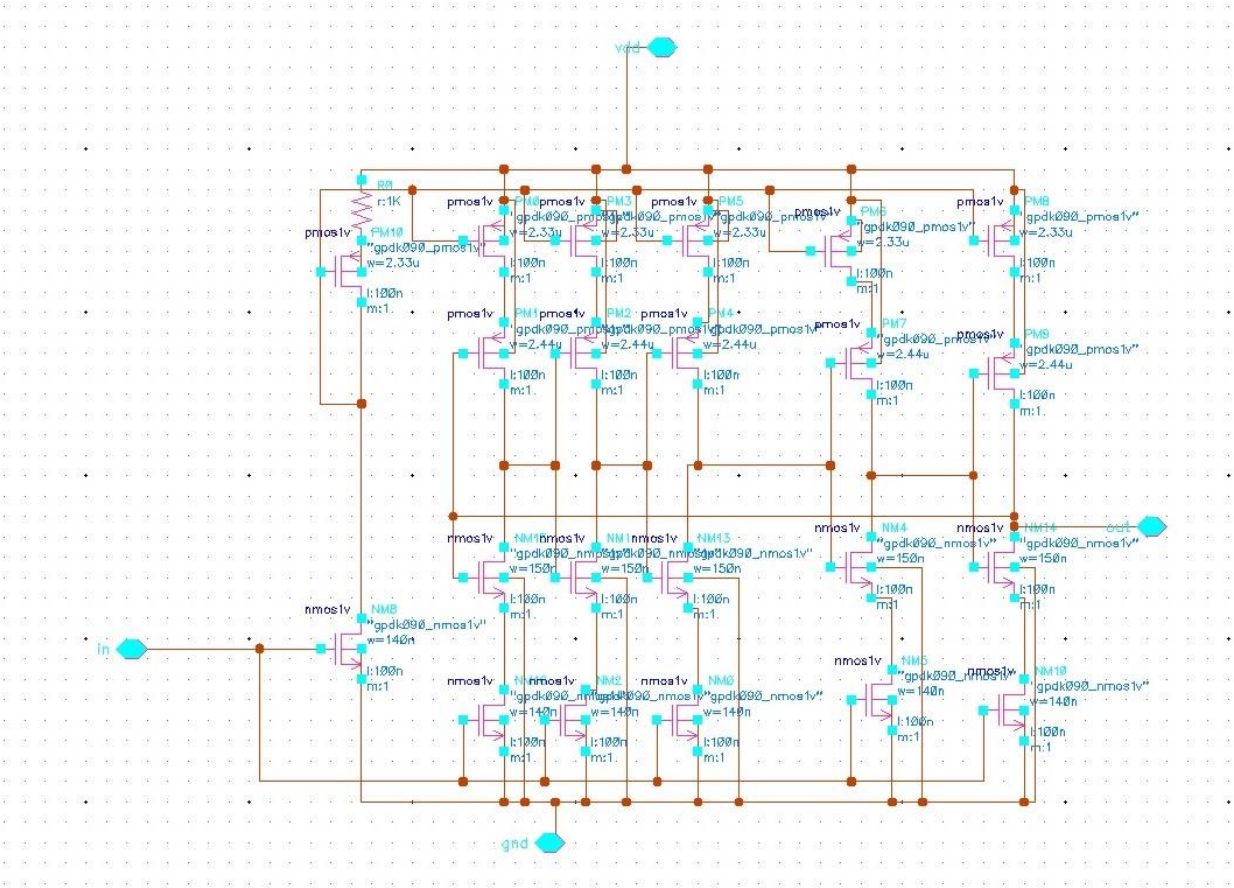

Fig. 3.2 CSVCO with Resistor

3.2.2 Design of Phase Frequency Detector

In design of Phase Frequency Detector, two PFD are connected with a NAND and NOT gate so as to obtain the main block of PFD. The circuit of PFD that is used to get main block of PFD is shown in Fig.3.3.

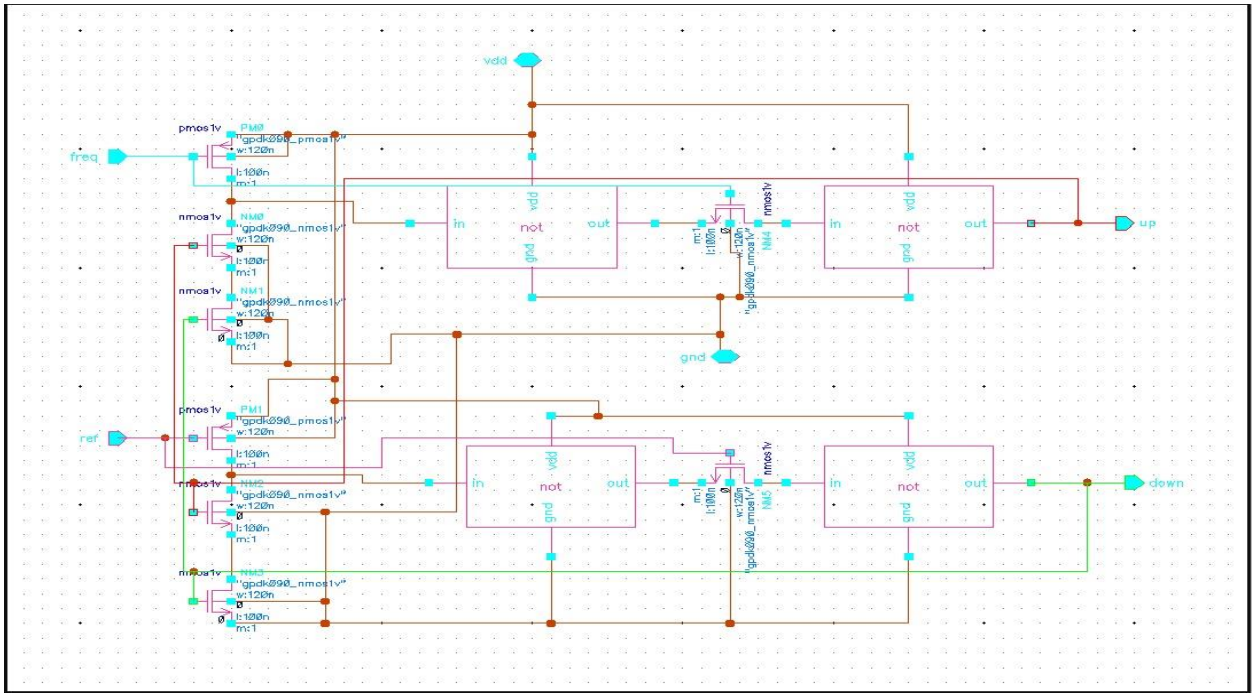

Fig.3.3.Schematic of PFD

The main block of PFD is shown in Fig.3.4. PFD has two inputs input clock and feedback clock are obtained from source and feedback loop. The two outputs UP and DOWN are given to Charge pump.

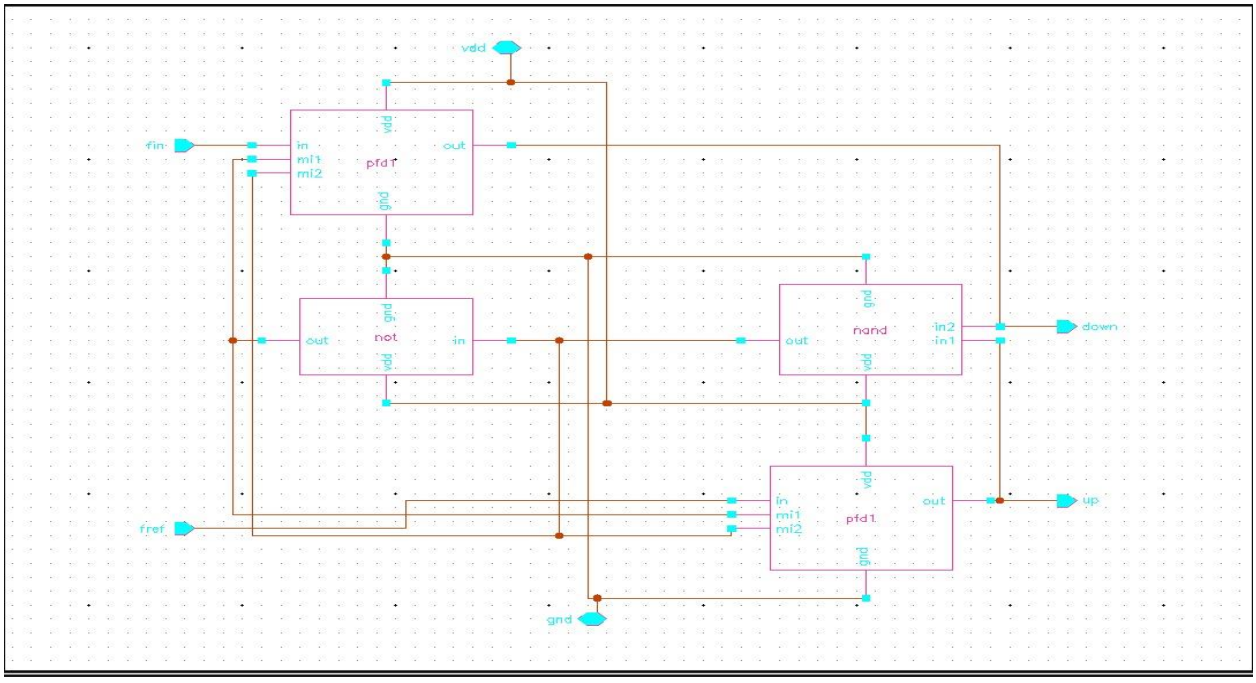

Fig.3.4.Schematic of main PFD block

3.2.3 Design of LPF and Charge Pump

Charge Pump and Loop Filter are circuits used to generate control voltage that is given to VCO to obtain frequency at that voltage. Charge pump converts two outputs of PFD into single output and send it to loop filter. When input clock leads feedback clock then UP is high and at this situation the output of VCO should be high, to increase the value of VCO these circuits are used. Charge pump is also called as current synthesizer because it is used to generate current with positive and negative polarity. Schematic of charge pump is shown in Fig. 3.5

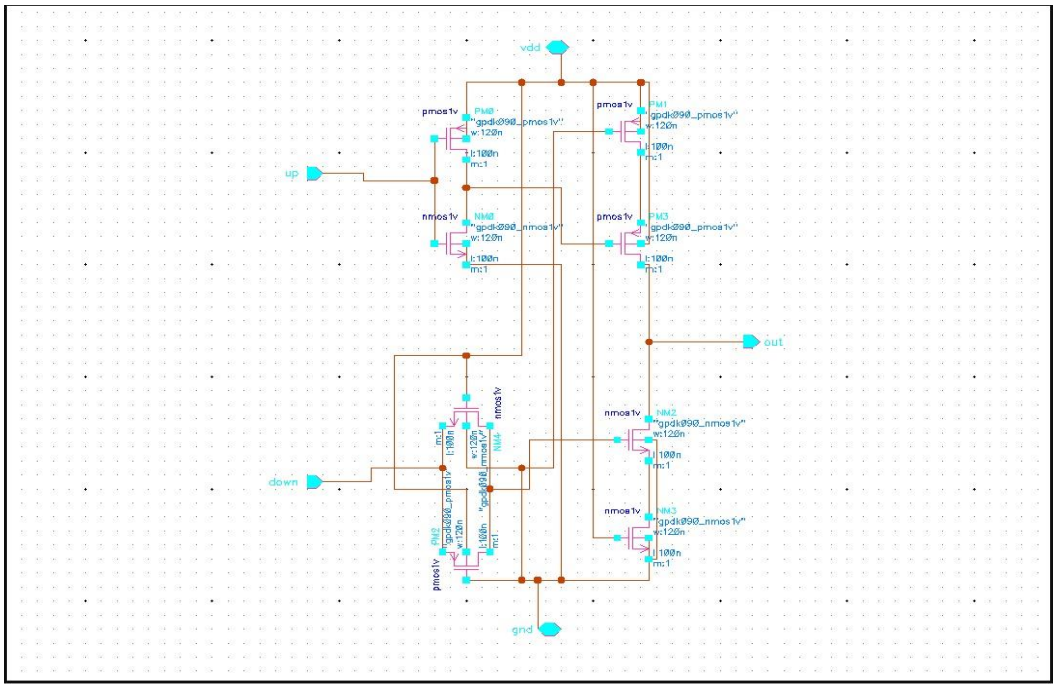

Fig.3.5 Schematic of Charge pump

3.2.4 Frequency Divider

Frequency divider is placed in feedback path which forms a closed loop. It divides the output frequency of VCO by two. The transient results of frequency divider is shown in Fig. 4.9. It depicts a simple D-flip flop which is shown in Fig. 3.6.

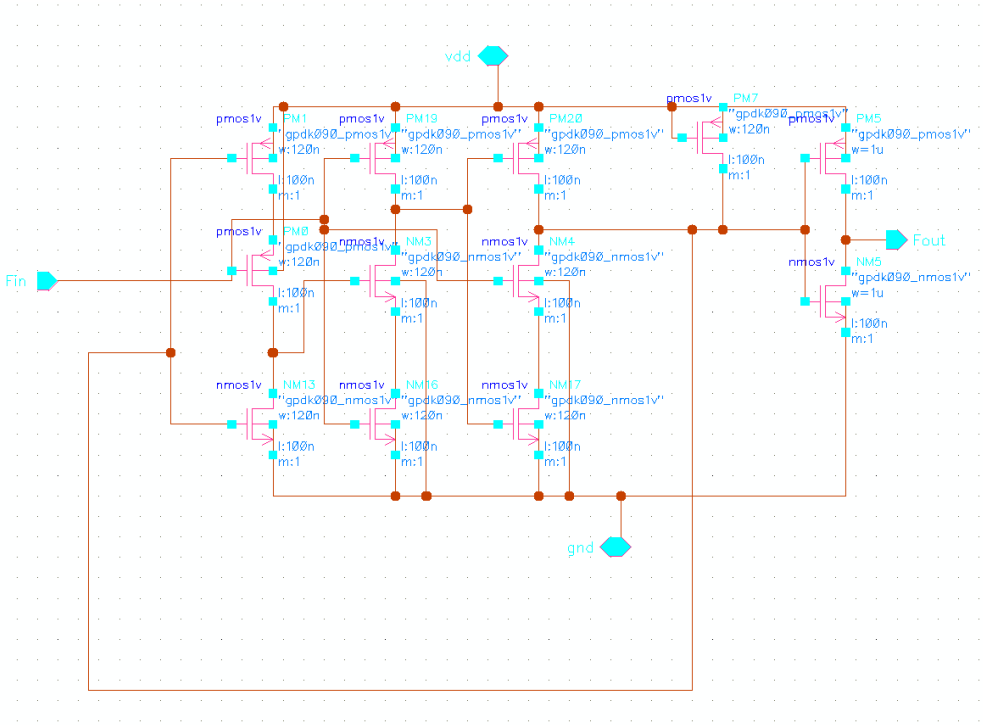

Fig. 3.6 Schematic of Frequency Divider

3.2.5 Design of Phase Locked Loop

All the blocked that are designed above are integrated to form a PLL circuit. The circuit is arranged as shown in Fig. 2.1.

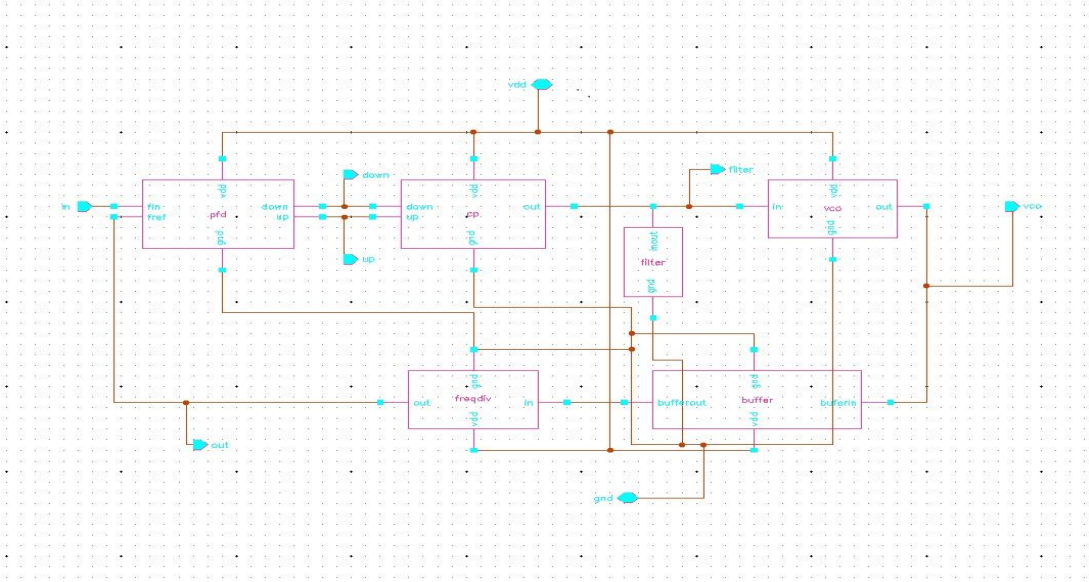

Fig. 3.7 Schematic of PLL circuit

The loop of the PLL is continued until the locking of phase and frequency. The schematic of PLL that is designed in cadence is in Fig. 3.7.

CHAPTER 4

SIMULATION RESULTS AND DISCUSSION

4.1 Voltage Controlled Oscillator

4.1.1 Traditional VCO

The VCO is designed so as obtain the output at the voltage of 0 to 1.8V. So it has a central frequency at 0.9V. Transient analysis of VCO is shown in Fig.4.1.with central frequency of at input voltage 0.9V Calculate the frequency values at every 0.1V and the corresponding frequency values are noted in Table:-1.A graph is drawn for Voltage vs Frequency which is called Tuning Range graph. It is defined as the Linear region obtained when a graph is drawn for voltage and frequency. It can also be calculated by using mathematical formula as

$$Tuning Range = (Higher frequency - lower frequency) \div Central frequency$$

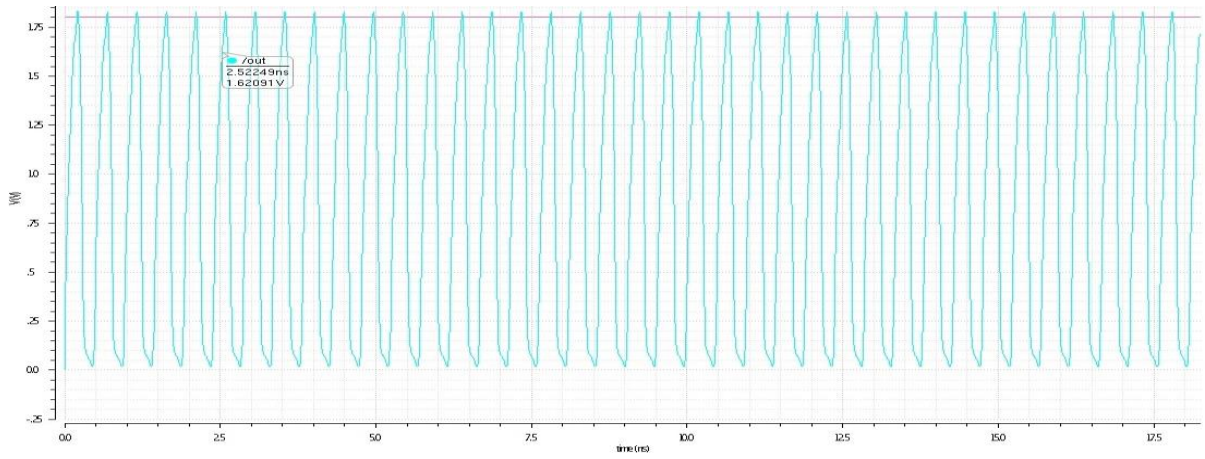

Fig.4.1.VCO output at input voltage VDD/2

Table 1 Oscillating frequency of the VCO for different control voltage

Control voltage (in V)	Frequency (in MHz)
0.1	24
0.2	94.09
0.3	218.6
0.4	357.1
0.5	516.3
0.6	710.9
0.7	928.1
0.8	1155
0.9	1384
1.0	1603
1.2	1992
1.3	2150
1.4	2282
1.5	2393
1.6	2484
1.7	2559
1.8	2620

Tuning range of the VCO is calculated from the graph shown in Fig.4.2. From the values obtained at different controlled voltages

$$Tuning\ Range = \frac{Fmax - Fmin}{Fcentral}$$

Here Fmax=1517.49 MHz, Fmin= 410.82 MHz, Fcentral = 1049.81 MHz

$$Tuning\ Range = \frac{1517.49 - 410.82}{1049.81}$$

$$Tuning\ Range = 1.05$$

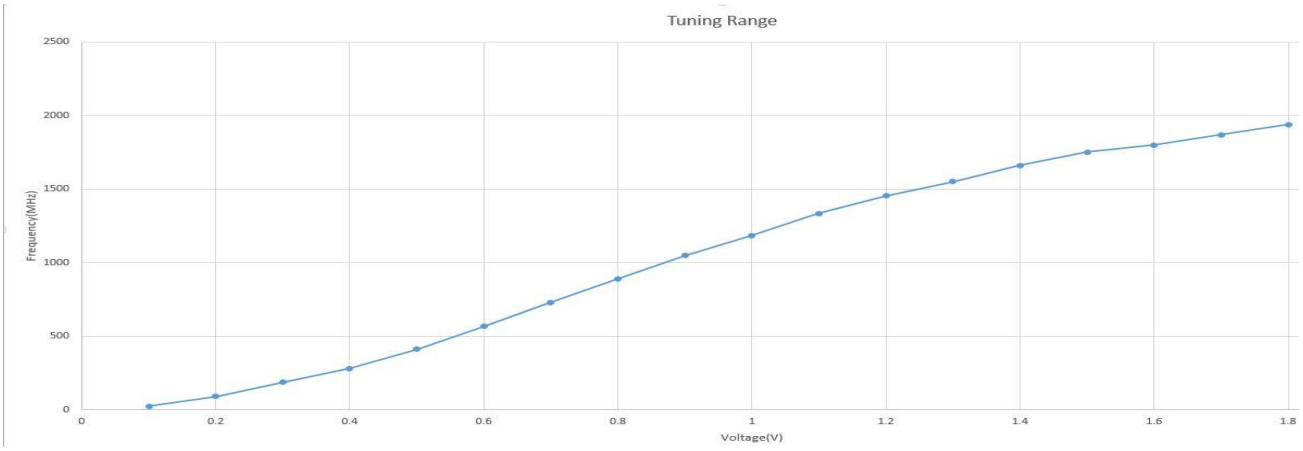

Fig.4.2.Tuning Range of VCO

Phase noise is defined as the frequency domain representation of rapid ,short, random changes or fluctuations in the Phase of signal . It is done after executing the PSS. Pnoise should always be small in negative values. Pnoise of VCO is obtained as -79 dBm/Hz from Fig.4.3. It is calculated at 1 MHz frequency. Average Power is another parameter which determines the efficiency of CSVCO. Average Power can be calculated directly from the calculator of Cadence tools or from the power graph. It is found to be 387.5μwatt All these measurements are tabulated in Table:- 2.

Table.2 All the parameters of Traditional CSVCO

S.No	Parameters	Values
1.	W/L (PMOS)	2.33μ/100n
2.	W/L (NMOS)	150n/100n
3.	Phase noise	-79 dBc/Hz
4.	Power consumed	387.5 μwatt
5.	Central frequency	1.049 GHz
6.	Tuning Range	1.05

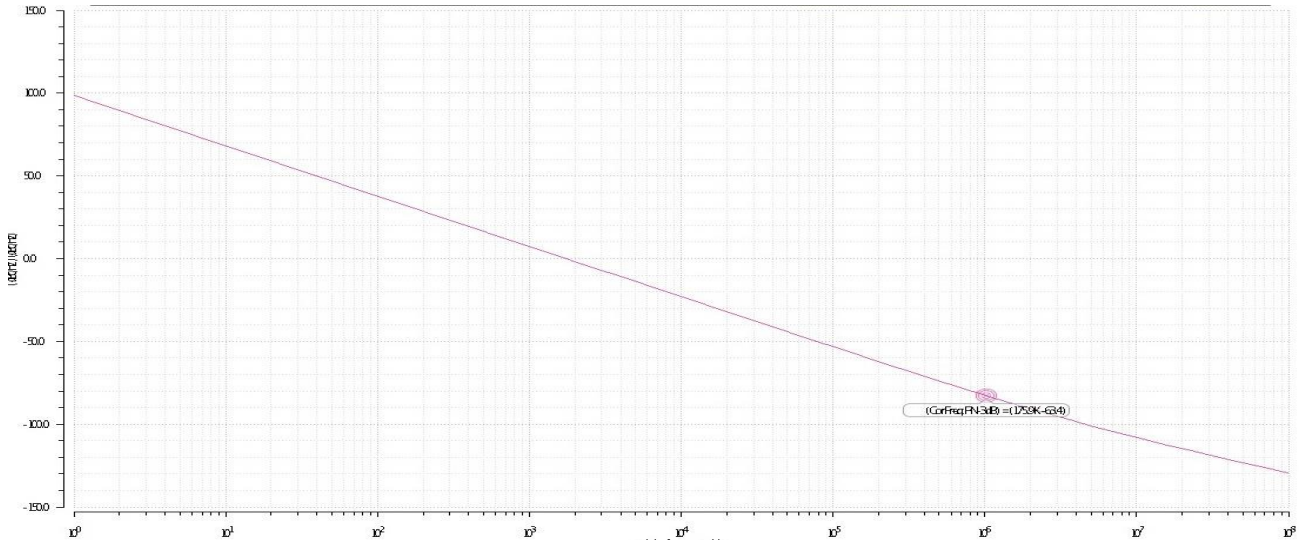

Fig.4.3. Phase noise of Traditional CSVCO

4.1.2 CSVCO with a Resistor

To improve the efficiency of VCO we should get low pnoise, locking range should be increased, tuning range should increase and power consumption should be more. So in order to get these connect a resistor at the required place as shown in Fig.3.Then the value of frequencies at the respective control voltages is shown in Table. 3.

Table. 3 Oscillation frequency of VCO with resistor with different voltage

Voltage (in V)	Frequency (in MHz)
0.1	24
0.2	94.09
0.3	218.6
0.4	357.1
0.5	516.3
0.6	710.9
0.7	928.1
0.8	1155
0.9	1384
1.0	1603
1.2	1992
1.3	2150
1.4	2282
1.5	2393
1.6	2484
1.7	2559
1.8	2620

From Table.3 Tuning range can be obtained as shown in Fig.4.4. It is also calculated by using equation 4.1 and it is 1.39. From Fig.4.4 it is concluded that the locking range of VCO is increased. Here the central frequency is 1.384 GHz.

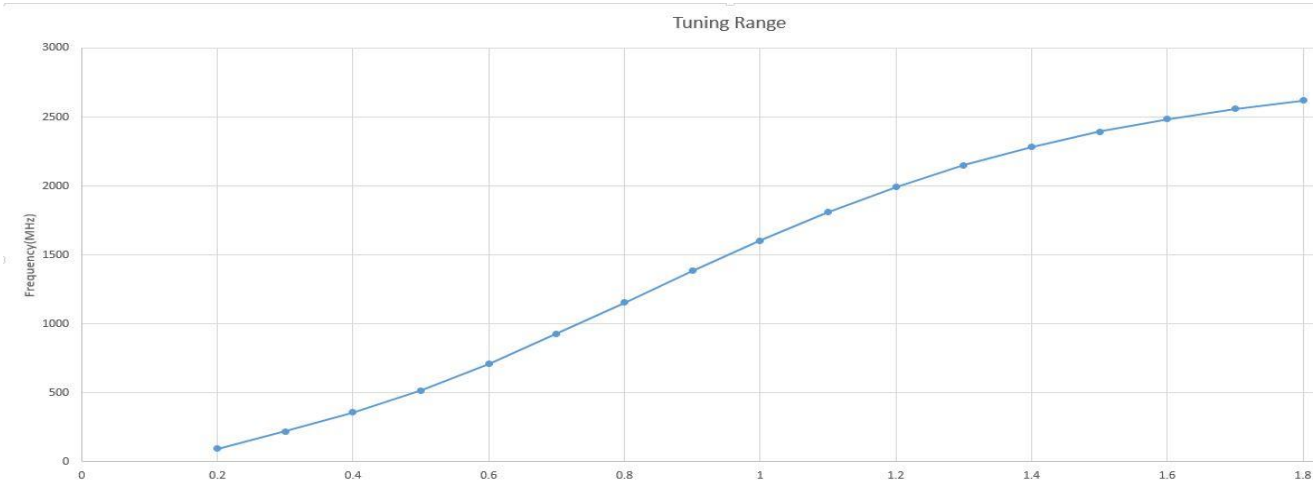

Fig.4.4 Tuning range of CSVCO with resistor

Phase noise is obtained as -81 dBm/Hz from the Fig.4.5. The value of pnoise has reduced from -79 to -81 dBm/Hz which is required for efficient working of VCO.

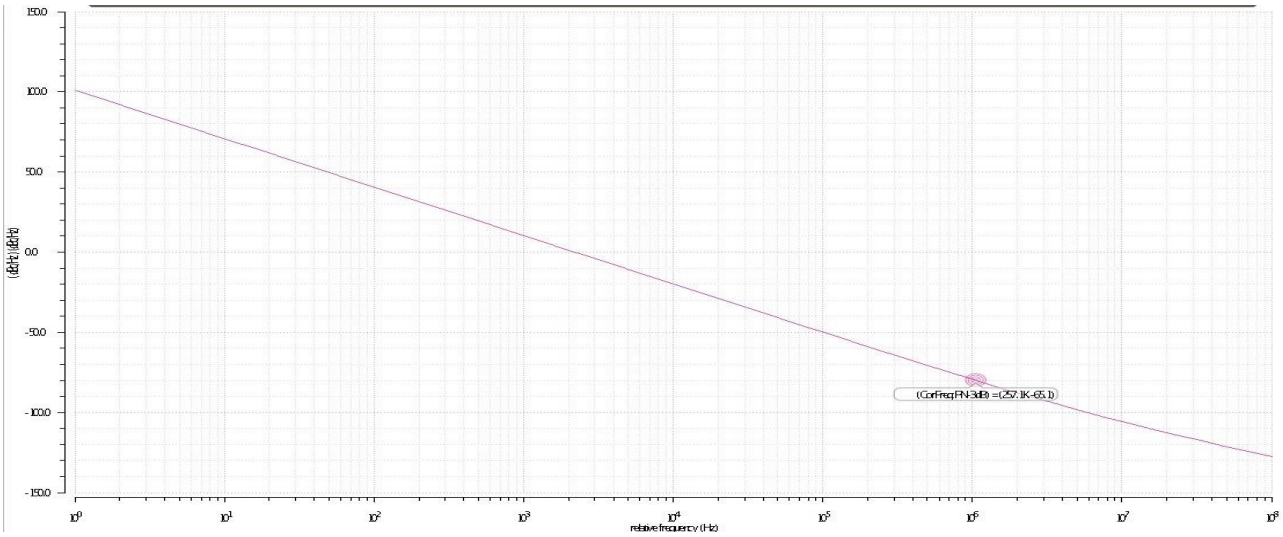

Fig.4.5 Phase noise of CSVCO with Resistor

Power consumed by the VCO is obtained as 455 μwatt from graph drawn in Fig.4.6 or can be calculated from cadence calculator.

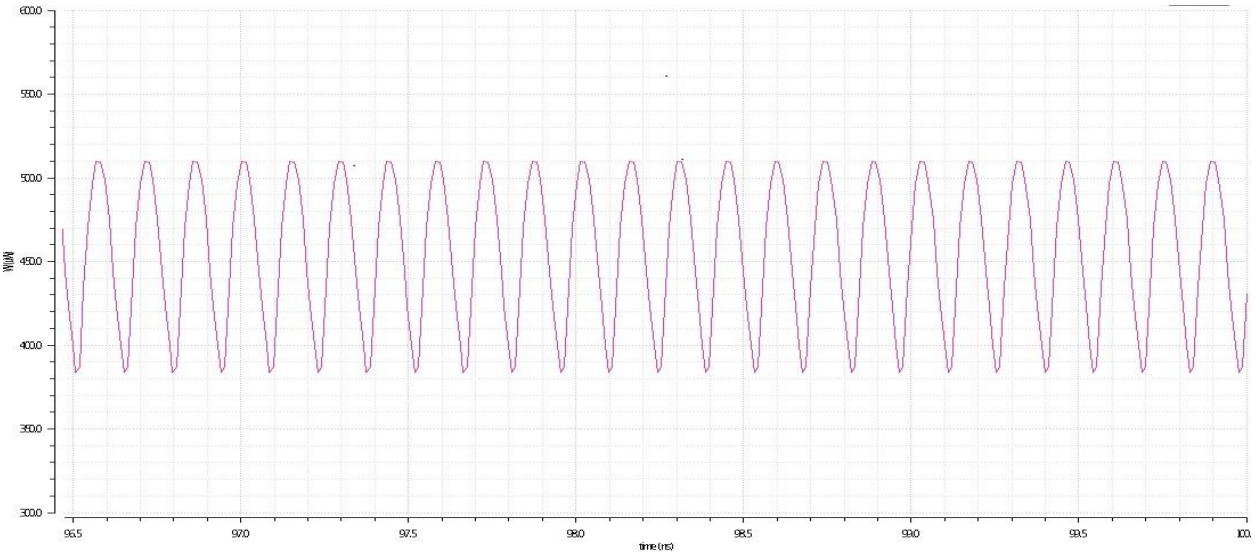

Fig.4.6 Power consumed by VCO with resistor

The values calculated are tabulated in Table.4. From that table it is concluded that there is certain decrease in Pnoise, increase in Tuning range and locking range has increased which is required

Table. 4 All the parameters of CSVCO with resistor

S.No	Parameters	Values
1.	W/L (PMOS)	2.33μ/100n
2.	W/L (NMOS)	140n/100n
3.	Phase noise	-81 dBc/Hz
4.	Power consumed	455 μwatt
5.	Central frequency	1.384 GHz
6.	Tuning Range	1.39

4.2 Simulation of PFD

In order to check the working of PFD, take two Pulse generators in which one is connected to reference port and the other is connected to feedback port. Insert values of pulse generator so the one of the wave is sent with some delay. The transient analysis of PFD is shown in Fig.4.7. The outputs UP and DOWN are obtained according to the input clock signal. If the reference clock raising edge leads feedback raising edge the UP is high. In contrast if feedback raising edge leads reference raising edge then DOWN is high and at last both of them come to reset position.

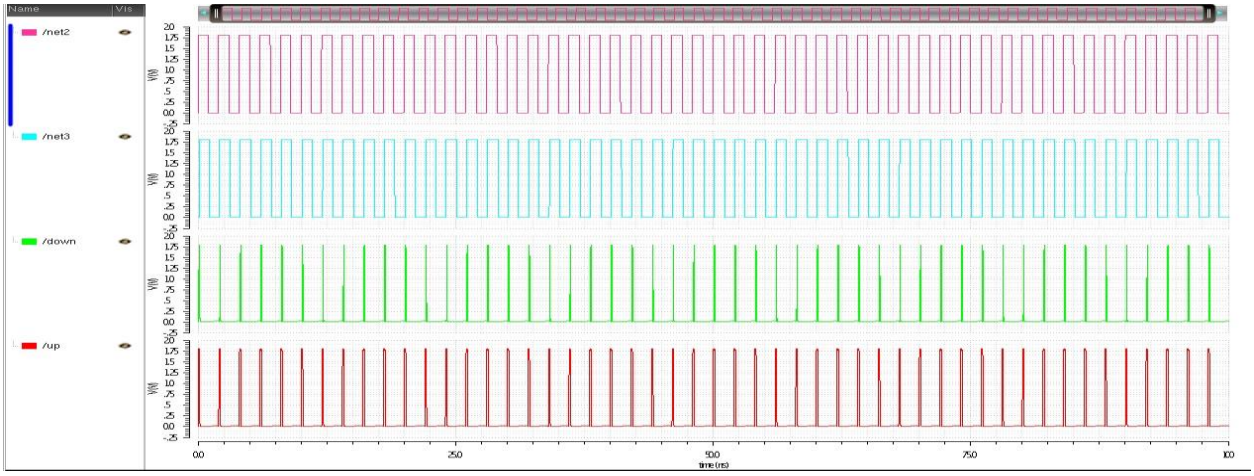

Fig.4.7 Transient analysis of PFD

4.3 Simulation of Charge Pump

Charge Pump is the block used to obtain currents i.e. positive and negative in PLL circuit. Its simulation or transient output depends on the output of PFD. When UP high is then charge pump gives the positive current polarity. On the other hand if DOWN is high then it give current with negative polarity. The simulation is shown in Fig. 4.8

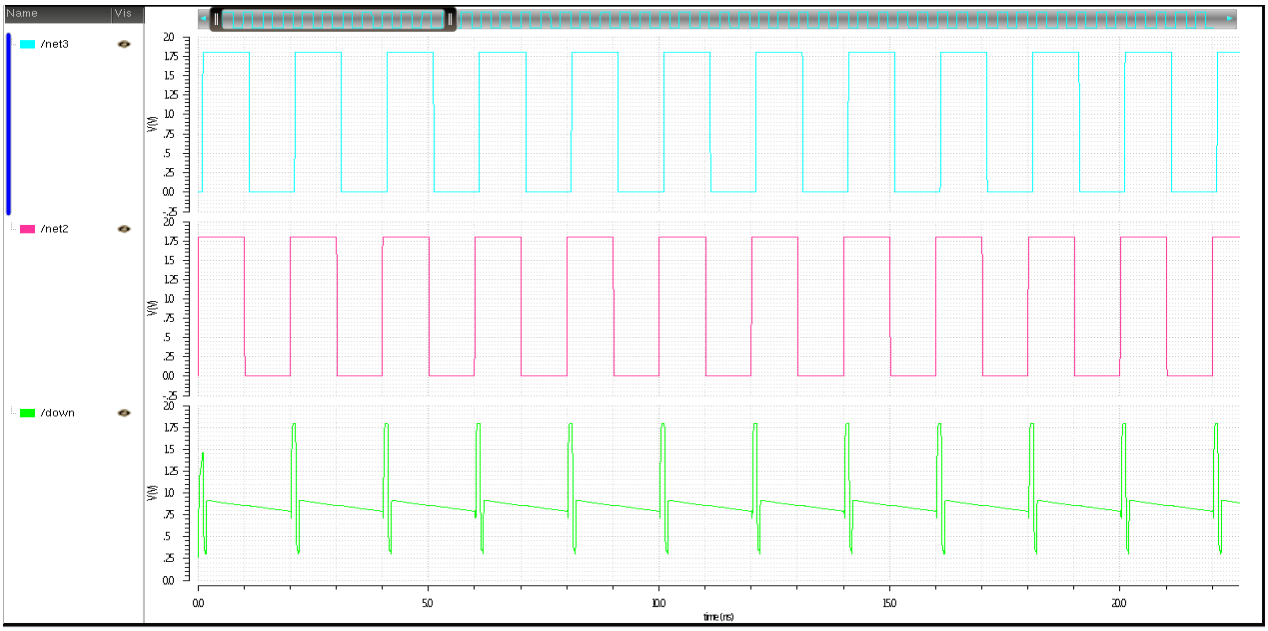

Fig. 4.8 Transient analysis of Charge pump

4.4 Frequency Divider

Frequency Divider is used to divide the output frequency of VCO with two. It forms the closed loop structure of PLL as it is placed in feedback path. Here frequency of 500 MHz frequency is fed to frequency divider and it divides to 250 MHz as shown in Fig.4.9.

Fig. 4.9 Simulation of Frequency Divider

4.5 Phase Locked Loop

Phase Locked Loop circuit is designed by arranging all blocks in specified order. Loop is continued until both the signals are locked. Here in transient analysis signals are locked at 65 micro seconds. So to make it more efficient it is zoomed and shown clearly. Both the inputs i.e. feedback and reference are in same phase and they are locked which is shown in Fig.4.9. Output of VCO along with output of frequency divider are also shown.

Fig. 4.10 Transient analysis PLL circuit

CHAPTER 5

CONCLUSION AND DISCUSSION

Conclusion

- In this thesis Phase Locked Loop is generated with improved locking range. The time at which locking took place is 65 microseconds.
- VCO designed with resistor has better performance when compared to traditional VCO. Tuning range is found to be 1.39 and central frequency is 1.384 GHz.
- Power consumed traditional PLL is 387.5 microwatt while VCO with resistor 455 microwatt. There is a reduction in Phase noise which is advantageous and it reduced from -79 dBc/Hz to -81 dBc/Hz.
- Architecture of PFD, Loop Filter and Charge pump is the main theme on which the PLL locking depends so proper care should be taken in the dimensions of PFD, charge pump and Loop filter which reflects on the perfection of locking.
- Dimensions of transistors reflects on the value of central frequency so care should be taken taking W/L values of transistors.

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