An Optimization of 16×16 SRAM Array for Low Power Applications

A Thesis Submitted in Partial Fulfilment of
the Requirements for the Degree of

Bachelor of Technology
in
Electronics and Instrumentation Engineering

by
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Department of Electronics and Communication Engineering
National Institute of Technology, Rourkela

2015

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Under the guidance of

Prof. Munshi Nurul Islam

by

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2015

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CERTIFICATE

This is to certify that the thesis entitled "***An Optimization of 16×16 SRAM Array for Low Power Applications***" submitted by Soumen Mohapatra (111EI0142) in partial fulfillment of the requirements for the award of Bachelor of Technology Degree during the session 20112015 in Electronics and Instrumentation Engineering at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Diploma/Degree.

Prof. Munshi Nurul Islam

Department of E C E

National Institute of Technology, Rourkela

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I am also thankful to Research Scholars and M. Tech. students for their co-operation in usage of laboratories and helping me to know the basic of Cadence Software.

SOUMEN MOHAPATRA

111EI0142

ABSTRACT

SRAM being Robust and having less read and write operation time is intended to use as a cache memory which oblige low power utilization. Low power SRAM outline is critical because it takes a vast division of aggregate power and pass on region in superior processors. A SRAM cell must meet the prerequisites for the operation in submicron/nano ranges. The scaling of CMOS innovation has critical effects on SRAM cell – arbitrary variance of electrical qualities and significant leakage current.

The paper introduces the configuration of 16×16 SRAM array design including row decoders/drivers, column circuitry, sense amplifiers, pre charge circuitry and transmission gates utilizing Cadence tools in a unique way and its functionality is analyzed properly.

Keywords: SRAM, Cadence Virtuoso, leakage current

LIST OF FIGURES

1. **CMOS Basic……………………………………………………………………10**

2. **CMOS Read…………………..…………………………………………………..11**

3. **CMOSWrite…………………………………………………………………………..12**

4. **Preharge Circuit…...…………………………………………………………………..14**

5. Voltage Sense Amplifier………………..…………….………………………………..16

6. Current Sense Amplifier………………………..……………………………………….17
7. Current Conveyor
Circuit………...……………………………..……………………….18

8. **3-8 Decoder……………………………………....…………………………………..23**

9. **Modified SRAM Cell Schematic……………………………………………………24**
10. Write Enable
Circuitry……………………………...……………………………25

11. Schematic of 2-4
Decoder……………………………...…………………………….26

12. Schematic of 4-16

Decoder……………………………….…………………………26

13. Schematic of Sense Amplifier and Pre charge…………………………..28
14. SRAM
Array……………………………………..……………………………29

15. I/O Waveform of Conventional
SRAM……………………..………………………..28
16. I/O Waveform of Modified
SRAM………………………………………………….29

17. Power Comparison waveform between Conventional and Modified
SRAM………30

18. Transient analysis of 1×1
SRAM……..……………………………………………….32

19. Transient analysis of 16×16
SRAM……..…………………………………………….33

20. Transient analysis of
Decoder………………………..…………………………….33

CONTENTS

1. Introduction……………………………………………………………….......09 .. ix

2. 6T CELL SRAM Basics…………………………………………………………10

3. 6T SRAM Cell Design Analysis and Its Operation………………………….......11

4. Design Flow…………………………………………………………………........13

5. Pre charge Circuit………………………………………………………………15

6. Sense Amplifier…………………………………………………………………...16

7. Row Decoder and Word line Driver……………………………………………....20

8. Column Circuitry and Column Decoder……………………………….............22

9. Proposed SRAM Modification Using TGL……………………………...…… 26

10. Write Driver Circuit……………………………………………… 27

11. Schematic of Memory Array and Its Per... 28

12.Result and An 32

13. Conclusion………………………………………… 39

14. Reference……………………………………………… 40

1. Introduction

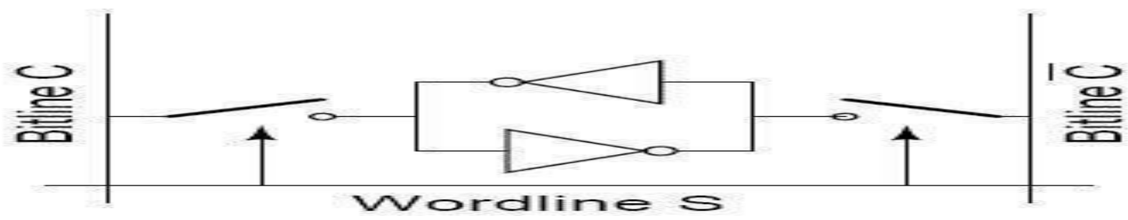
Over the past decades, physical dimension of complementary metal-oxide semiconductor (CMOS) devices have been continuously scaled to meet the requirement of higher speed of operation, and of integrating more number of the devices in a given silicon wafer area. Such and a miniaturization of device size and an increase in number of switching nodes, both dynamic and static power dissipation are increasing at an alarming rate with the technology generation. This is not only a serious problem for portable applications but also for high performance desk top applications since it requires a costly cooling mechanism. Therefore, an appropriate optimization of various circuits is required to reduce power consumptions of an integrated circuits (ICs). Among various components of an IC, memory element consumes a significant fraction of the total power dissipation.

SRAM based Cache memories and System-on-chips are widely used in present days for various applications.

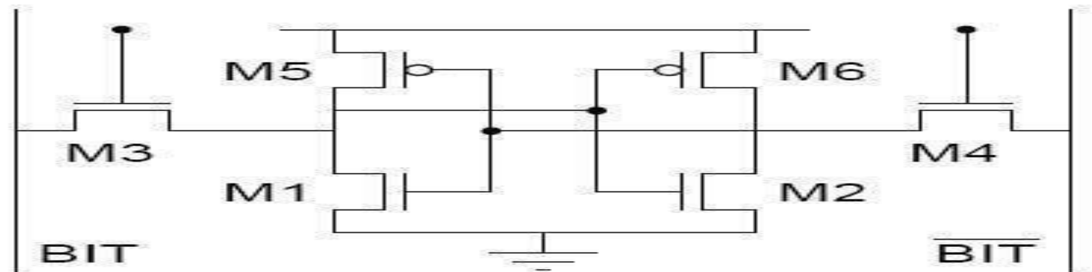
So here we are trying to optimize the cell ratio and improving the pre charge circuitry so that we can achieve our goal To improve the speed of SRAM we use the dynamic logic in the memory periphery design which results in use of lower transistors and speed also. After that the stability of the cell is measured and analyzed thoroughly.

2. CMOS 6T SRAM Cell Basics

Design of SRAM is generally depends on its perfect sizing and its read and write stability i.e. the cell should provide a nondestructive read and fast writing operation. The memory circuit is said to be static if the put away information can be retained uncertainly, the length of the power supply is on, with no requirement for intermittent revive operation. The information stockpiling cell, i.e., the cell having storing capacity of 1bit in the static RAM exhibits, perpetually comprises of a basic lock circuit with two steady working focuses. Contingent upon the saved condition of the two inverter cross coupled circuit where one giving negative of its to the others, the information being held in the memory cell will be translated either as rationale "0" or as rationale '1'. To get to the information contained in the memory cell by means of a bit line, we require at least one switch, which is controlled by the comparing word line

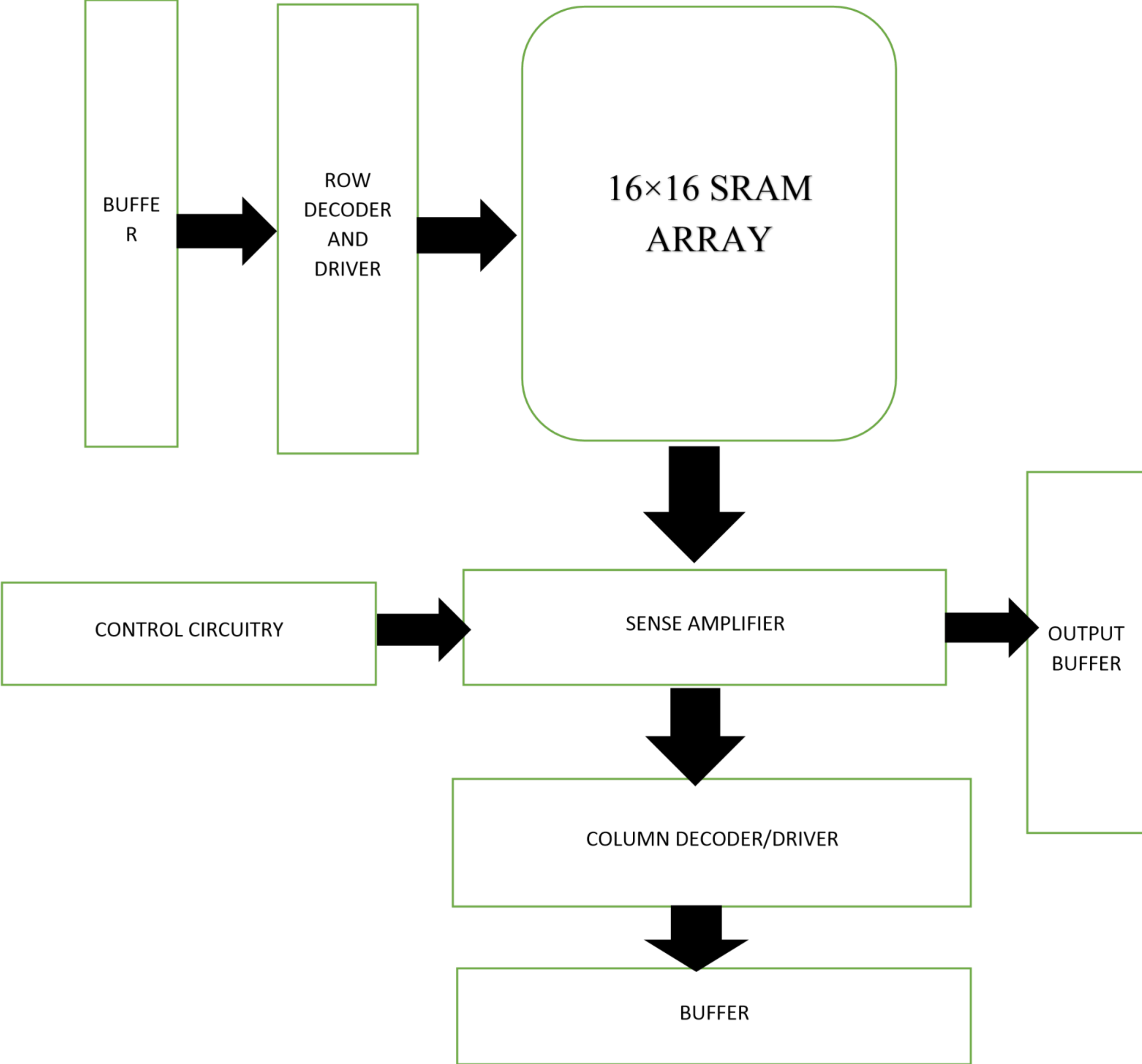


The main reason for using it because of its less static power loss as leakage current in this case is very less. It also has a high noise immunity because of its high noise margin and it could also operate in very low power supply voltage. But it is generally made up of 6T CMOS but not of 4T NMOS design where a high resistive load is used causes always a path to the power supply voltage.



The pass transistors are activated only when we activate the corresponding word line and according to they become activated by making WL=1, then accordingly read and write operation is done. The above fig. is the diagram of basic 6T SRAM cell.

The below Fig. show the basic Memory system where we give in row side and column side 4 input each



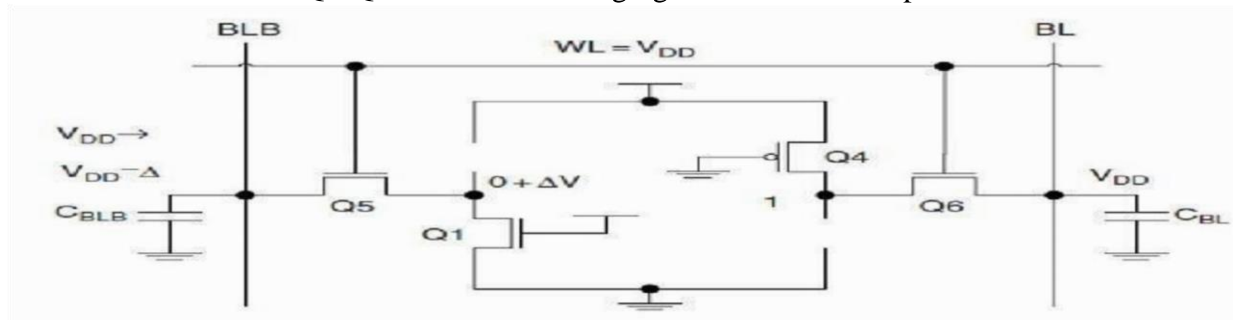
which pass through a buffer then they get decoded and by a driver come into the SRAM array.And using control circuitry we got the output from the output buffer.

3. 6T SRAM Cell Design Analysis and Its Operation

For determination W/L ratios of the transistors, a number of design methods have to be be taken into consideration. The two basic requirements, which find W/L ratios, are that the data during read operation should not destroy the stored data present in the cell and there should be allowed to modify information during write operation.

READ OPERATION

Before launching a read operation, the bit lines are pre charged to VDD. The read operation is started by empowering the word line (WL) and interfacing the pre charged bit lines and bit line bar, to the interior nodes of the cell. Upon read access indicated in the below given figure, the bit line voltage VBL stays at the pre charge level. The integral bit line voltage VBLB is discharged through transistors Q1 and Q5 associated in arrangement. Successfully, transistors Q5 and Q1 act as a voltage divider circuit whose yield is presently no more at zero volt and is associated with the information of inverter Q2-Q4. Estimating of Q1 and Q5 ought to guarantee that inverter circuit Q2-Q4 don't switch bringing on a destructive operation of read.



(Figure: Read Operation of SRAM)

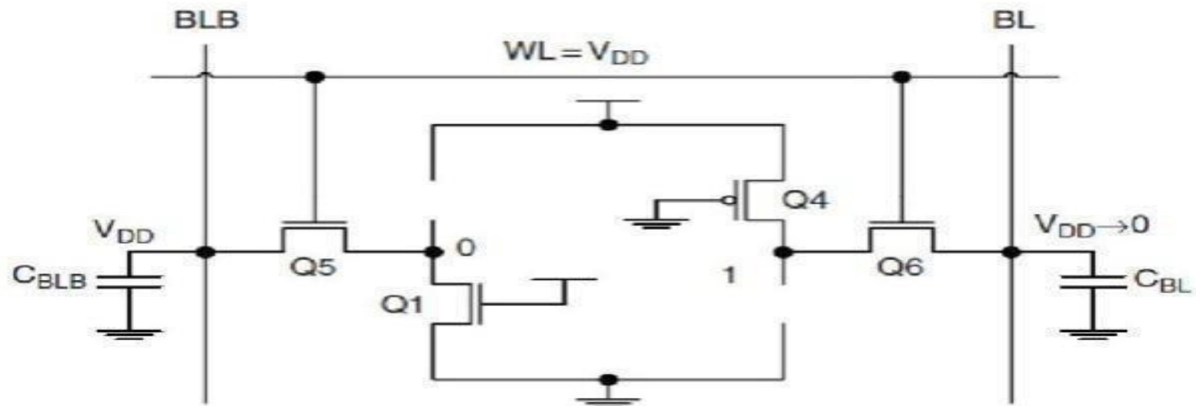
Under considering the situation we find a cell ratio (CR).   CR = (W/L) of Q1 / (W/L) of Q5

It is our requirement to make CR > 1.2 to ensure read stability.

Write Operation

In case of write operation 1 of Bit lines has to go to ground level from the pre charged V_{dd} level via a write driver of Q6. In the event that Q4 and Q6 are perfectly designed so that it wont cause to flip and data is viably over written.

Write margin is availed there to show that up to which it can write which is characterized by base bit-line voltage needed to flip 6T SRAM condition.



(Figure -2 Write Operation of SRAM Cell)

PR =(W/L)of Q4/(W/L)of Q6

It is our requirement to make PR < 1.8 to ensure read stability.

Standby Operation

It is the case happens when the word line is put to be ‘0’ i.e. the case when the pass transistors become deactivated there could be no transfer of data from the bit or bit bar line to inner cell.

4. Design Flow

Cadence is a leading EDA software and semiconductor company which provides different sorts of design and verification tasks that include:

1. Virtuoso Platform

I t is a tool specified for designing full-custom ICs, includes schematic entry, behavioral modeling (VerilogAMS), circuit simulation, physical verification,full custom layout, extraction of circuit etc. Used mainly for analog, mixed-signal, RF designs.

2. Encounter Platform

Tools for creation of digital ICs. This includes floor planning, synthesis, test, and place and route. Typically a digital design begins from Verilog net lists.

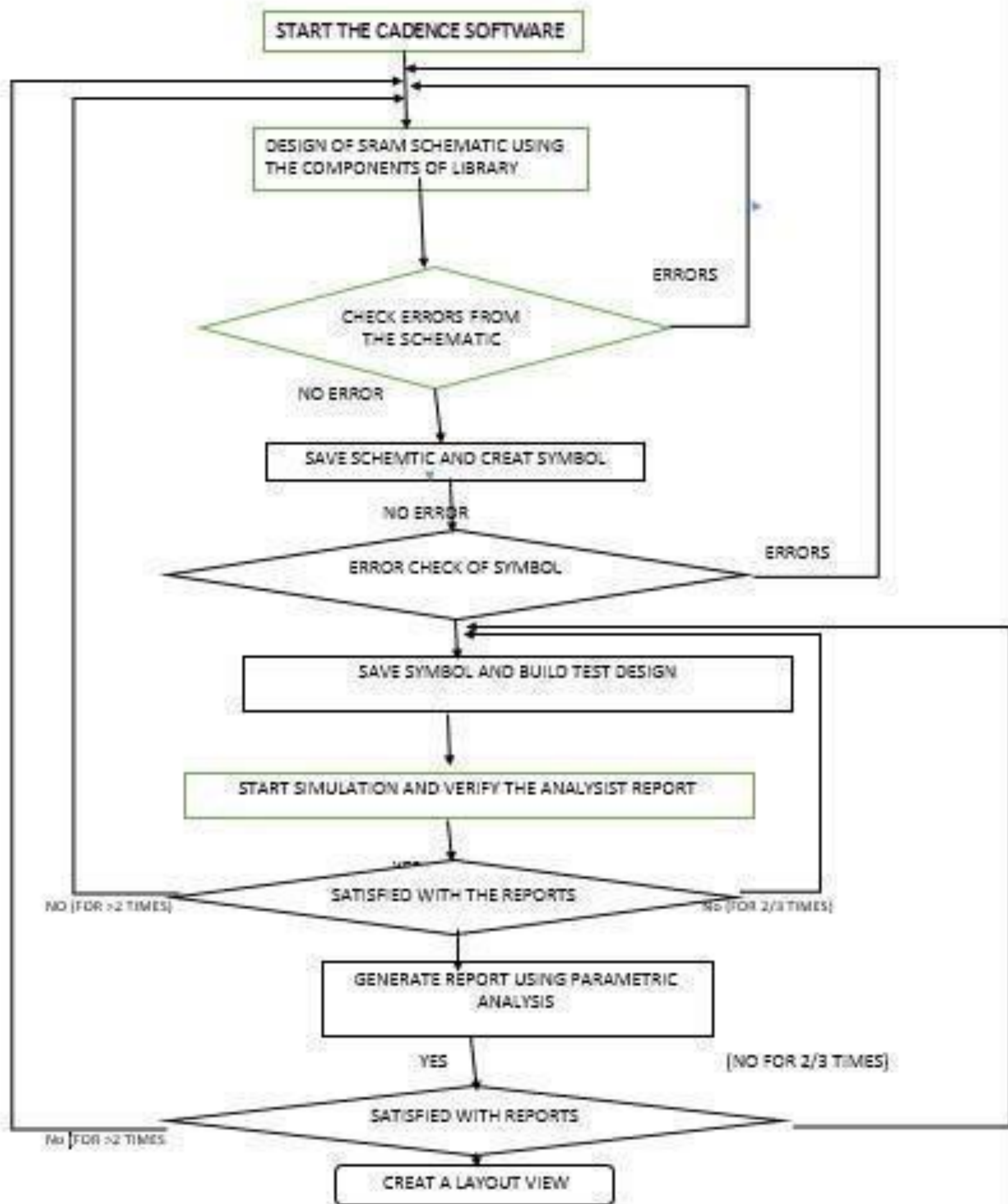
3. Incisive Platform

Tools for simulation and functional verification of RTL including Verilog, VHDL and System. It includes formal verification, formal equivalence checking, hardware acceleration, and emulation.

A SRAM cell of 1×1 is designed and analyzed then, a corresponding symbol is done for it and then a 16×16 array is done by copying this sram cell 256 times and placing it in between word lines and correspondingly bit lines. Finally of the design for the decoders, sense amplifiers, and transmission gates etc are being done using dynamic logic or BIMOS logic so that it will be able to speed up the process.

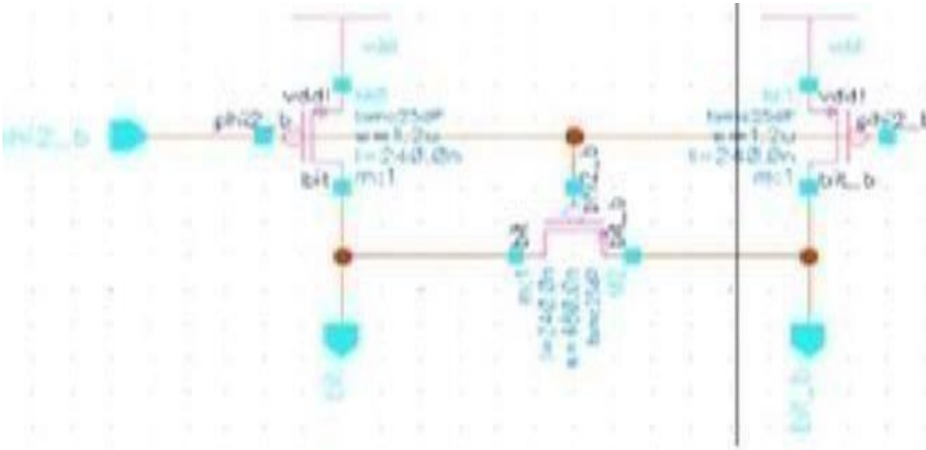
The work on this cadence software is done according to the below flow charts.

The project work is done via Virtuoso platform using gpdk-90 nm technology.The procedure on this cadence software is done according to the below flow charts


START THE CADENCE SOFTWARE
DESIGN OF SRAM SCHEMATIC USING THE COMPONENTS OF LIBRARY
ERRORS
CHECK ERRORS FROM THE SCHEMATIC
NO ERROR
SAVE SCHEMTIC AND CREAT SYMBOL
NO ERROR
ERROR CHECK OF SYMBOL
ERRORS
SAVE SYMBOL AND BUILD TEST DESIGN
START SIMULATION AND VERIFY THE ANALYSIST REPORT
SATISFIED WITH THE REPORTS
GENERATE REPORT USING PARAMETRIC ANALYSIS
YES
(NO FOR 2/3 TIMES)
SATISFIED WITH REPORTS
CREAT A LAYOUT VIEW

5. Pre charge Circuit

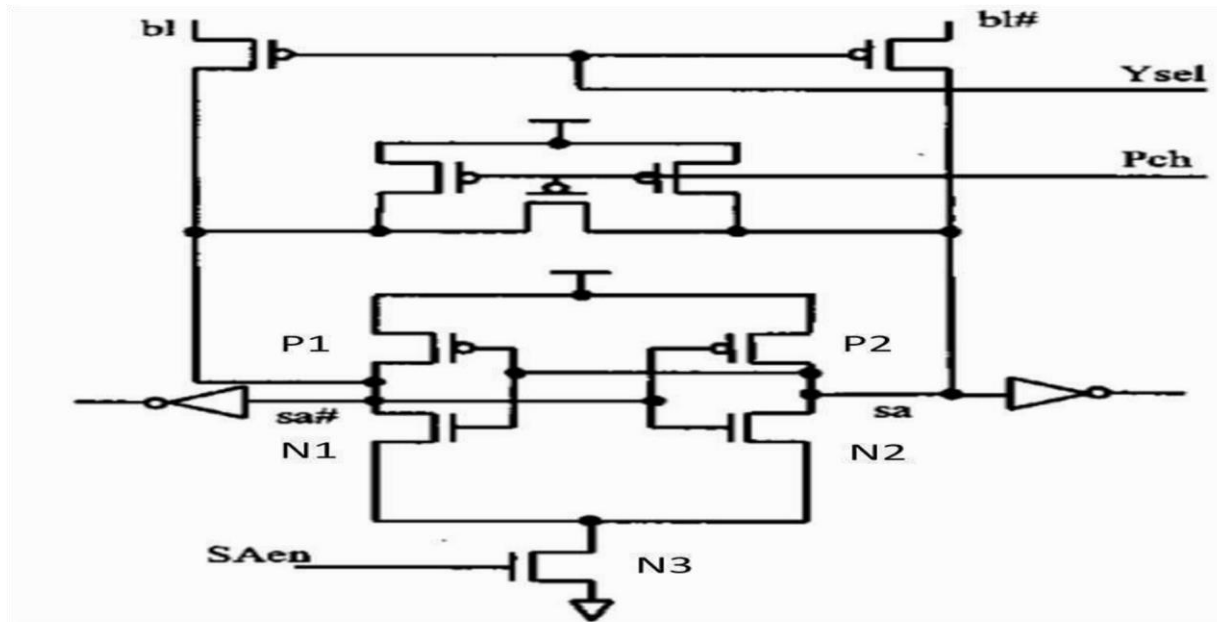
It is used to make the both bit and bit bar line equal i.e. Vdd. The circuit is controlled by a pre charge voltage. When we give phi voltage zero which results in activating the two PMOS gate so that it will be able to allow both the bit lines and bit line bar to go to pre charged state. So that it will help in read operation. A third transistor is placed connecting the bit lines to help equalize the voltage in case of any mismatch between the bit lines.



6. Sense Amplifier

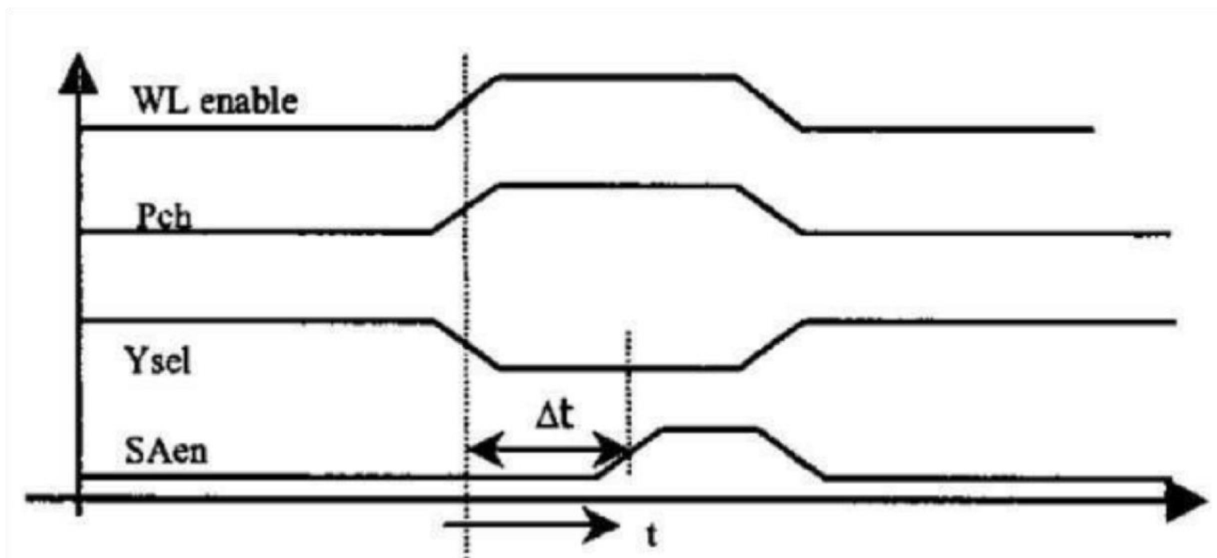
Voltage Sense Amplifier

A voltage sense amplifier detects the differential voltage on the bit-lines and creates a full rail yield. The



circuit is demonstrated in Figure

(Figure 3.1 Voltage Sense Amplifier)



The timing scheme for the voltage sense amplifier is given here

The operation of the circuit is as per the following. At the point when WL is empowered, a voltage differential starts to grow on the bl/bl# pair. At the point when enough differential, contingent upon the innovation and circuit, has added to the sense amp empower (SAEN) is initiated which causes the cross coupled inverters to go into a positive criticism circle and make an interpretation of the differential to full rail yield. The sense intensifier yield hub which interfaces with the bit-line with a lower voltage, for eg sa, is pulled down to 0 while the other yield sa# stays high. At the point when sense intensifier is empowered, NMOS device N1 and N2 go into immersion. The NMOS device N2 which gets full VDD info has a higher current than N1 with a littler voltage as its Vgs. The particular case that leads higher current (N2) pulls its yield voltage lower decreasing the Vgs on alternate NMOS device (N1), which subsequently has littler current coursing through it. This positive input circle proceeds until the yield voltage sa has fallen sufficiently low to bring about the NMOS device N2 to enter direct locale and turn on the PMOS device P1 of the other inverter and reason its yield to be driven high. N1 is in the long run killed, and the cross coupled inverters store the subsequent yield.

Current Sense Amplifier

The current sense amplifier works by sensing the bit cell current specifically. It is not subject to a differential voltage growing over the bit-lines. This helps decrease bit-line pre charge power subsequent to the low going bit-line can be clasped at a higher voltage than would be needed with a voltage sense amplifier. The current sense amplifier comprises of 2 portions one is a current transporting circuit with unity gain current transfer

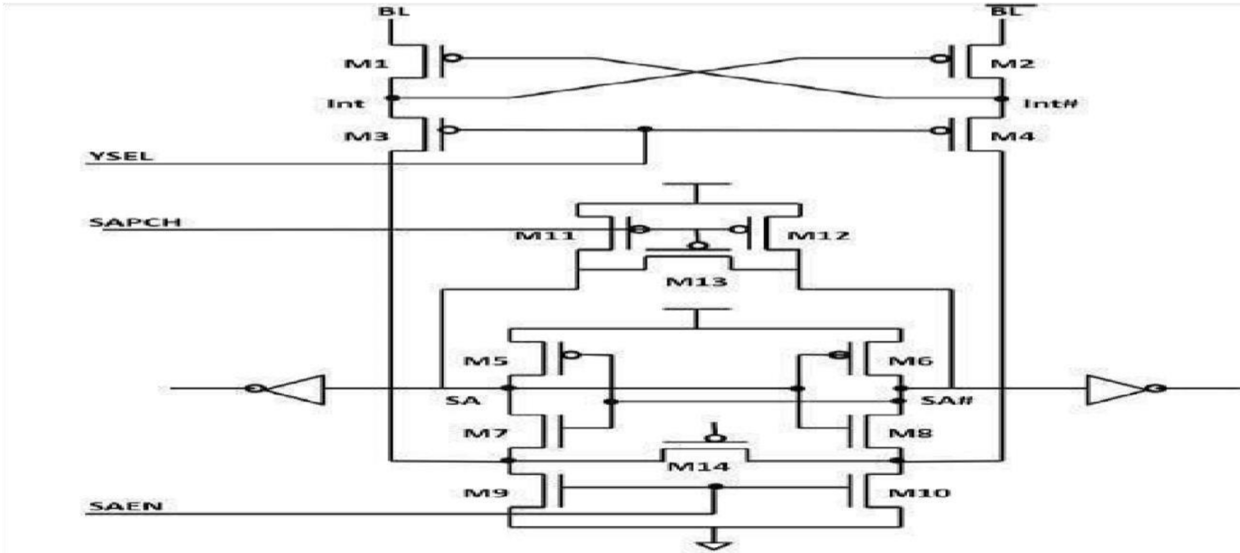
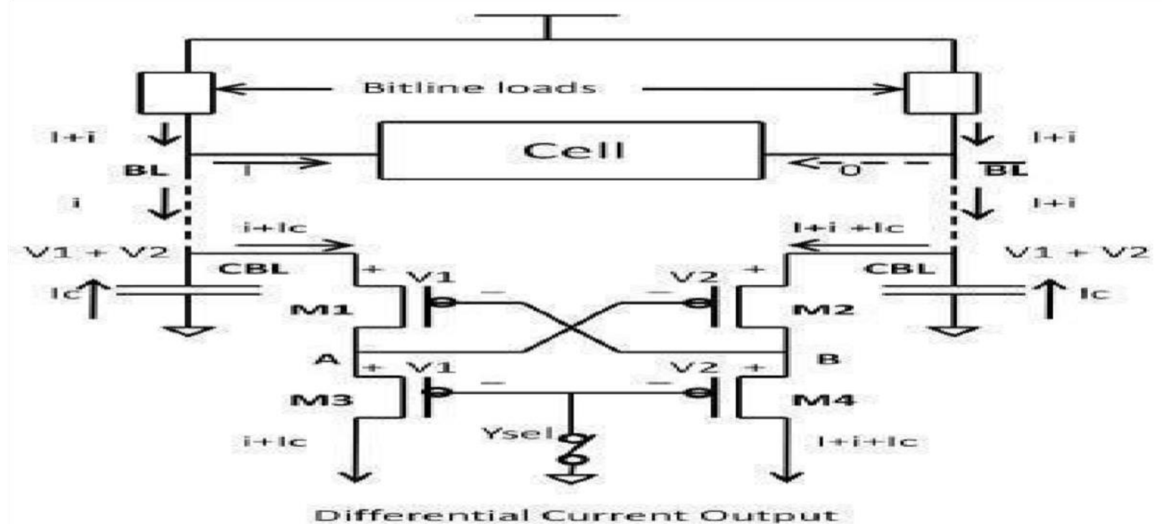


Figure 3.3 Current Sense Amplifier

attributes and another one sensing circuit which detects the current differential. The circuit outline of the current sense amplifier is indicated in Figure

The current transporting circuit or the current conveyor comprises of four similarly estimated PMOS transistors (P1 through P4) with positive feedback. These devices work in immersion. The current conveyor circuit, indicated in above figure works as takes after. The V_{GS} of M1 will be equivalent to V_{GS} of M3, since their currents are break even with, their sizes are measure up to, and both transistors are in immersion. Let this voltage be spoken to by V1. Likewise, the gate-source voltages of M2 and M4 are additionally equivalent, let this be spoken to by V2. At the point when YSEL is grounded, the voltage on BL is given by V1+V2, so is the voltage on BL#. Therefore, the capability of the bit lines will be square with free of the present circulation. This indicates that there over the bit-lines a virtual short circuit is existed. Since the bit line voltages are meet, the bit-line load currents will likewise be level with, and the bit-line capacitor currents. Since the cell draws a present I, the right leg of the present conveyor draws more present than the left leg. The distinction between these two currents will be equivalent to the cell current. The channel current of M3 and M4 are gone to the present conveyor yield which is associated with the present sensing circuit. The differential yield current of the present conveyor is therefore equivalent to the cell-current.

(Current Conveyor Circuit)



Present sense amplifier works in two stages: precharge and assess. Amid the precharge stage, the bitlines are precharged through precharge transistors associated with the bit-lines (not indicated here). The sense amplifier yield hubs SA and SA# are additionally pre charged high through M11 and M12 PMOS transistors. Transistors M11 and M13 are ON amid pre charge, adjusting the inputs and yields of the sensing circuit separately. The working current of the sense amplifier is dictated by the sizes of transistors M5-M8. Toward the end of the pre charge stage, pre charge and adjustment transistors M11-M14 are killed. Amid the assessment stage, YSEL is pulled low and SAEN is pulled high. The cross coupled inverters involving transistors M5-M8 then shape a high increase positive input amplifier. Because of the positive input, the impedance investigating the source terminal of either M7 or M8 is a –R i.e. negative of resistance), which causes M7 and M8 to start sourcing a bit of the distinction current. The distinction current moving through M7 and M8 courses through the little identical capacitance at the drains of M7 and M8, offering ascent to a voltage contrast over the yield hubs of the sense amplifier. The starting direction for the extent of the voltage contrast between the drains of M7 and M8 is given by

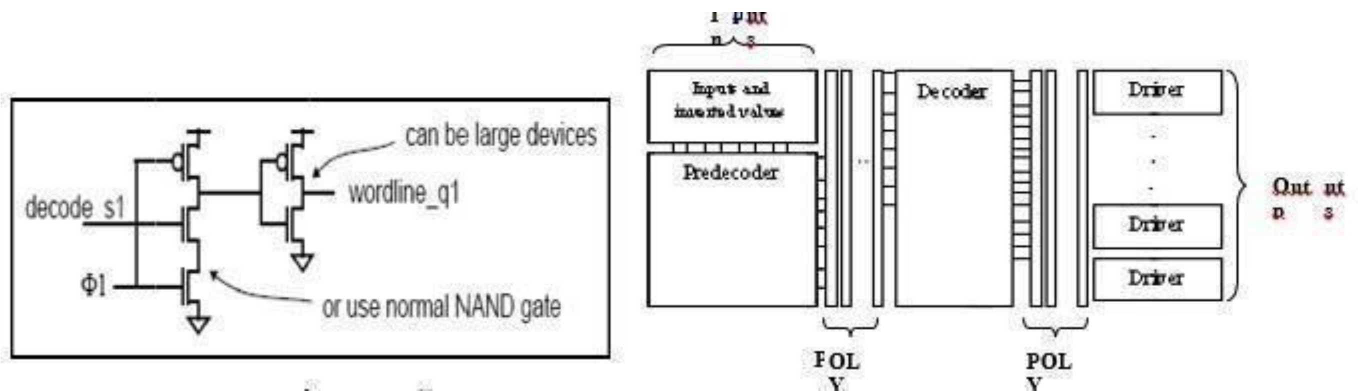
$$D(\Delta V/dt) = 2\Delta I/Cd$$

Where Cd is the aggregate capacitance at the drain node of M7 or M8. This direction is taken after for a short time, and afterward the subsequent differential voltage at the yield of the sense amplifier is quickly opened up by the positive feedback of the cross coupled inverters, driving one yield to zero and keeping the other one high.

The sensing delay is moderately insensitivity to capacitance of bit line as the operation is not reliant on the improvement of a differential voltage over the bit-lines. Not at all like the voltage sense amplifier, the yield nodes are not fixing to the high capacitance bit-lines and have the capacity to react rapidly. The CSA can have lower voltage swing on bit-lines. This is on account of the cross coupled PMOS pair M1 and M2 cuts off the release way to ground for both bit-lines. Assume BL is high and BL# is going low. This reasons nodes Int and A to go high creating M2 to be cut off. Therefore, the way from the low set BL# to ground is cut off, decreasing the voltage swing on it.

7. Row Decoder and Word line Driver

For a n: 2^n decoder, 2^n n input gates need to be constructed. Substantial fan-in gates are the result of substantial decoders. An arrangement stack is shaped by extensive fan-in gates and the decoder is slower. So we instead of CMOS logic use a dynamic logic decoder for overcome this problem. NAND and NOR gates were considered for the decoder configuration. Using delay analysis, it was observed that the NAND gate is quicker than the NOR gate. So we used NOR dynamic logic so that our PMOS transistor number reduces. Then by use of a clock in pre charge or evaluation phase we operate this decoder and select our required word line. The decoder would presumably be speedier if the inverter sizes were changed to be incremental along the whole decoder. The below given block diagram is the block diagram the Row decoder and Word line driver.



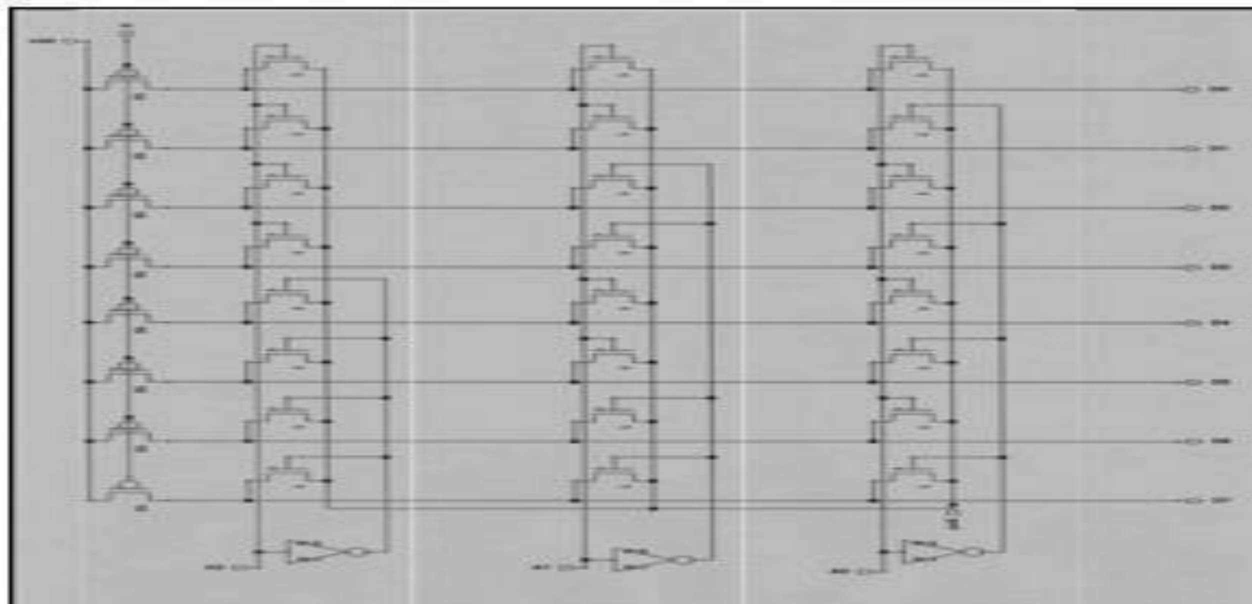
8. Column Circuitry and Column Decoder

Like the above expressed in row decoder and driver in the column circuitry also same formulation method is applied where we give input through the column side which allows to pass through a buffer first because generally the input to the column decoder or driver is ECL based so to convert it into CMOS based for array. Now the decoder if we make in CMOS style then it will occupy more area as well as also little slower due to more number of PMOS presented there also. So we require a dynamic logic or bi-mos circuit to speed up our transient response or read/write operation.

Here we use the dynamic logic for it where we give a clock if it is zero then all the PDN portion will be activated or 1.which is called prechrge condition if we make it one then according to the PDN input the output will be 0 or retained in 1.Advantage of using this design logic is it require very less PMOS and more NMOS devices so speed is increased and the number of transistors also drastically decreases.

And we also use driver circuits CMOS type for giving this decoder output to the SRAM array. The below given figure is the schematic of basic 3-8 decoders using NOR-dynamic logic.

Like this we can design decoder for 4-16 decoder also.



(3-8 dynamic decoder column circuitry)

We have to make the size of the PMOS transistors utilized for pre charging larger little bit.The reason behin doing this is that bigger the PMOS transistor tends to speed up the pre charging

process thus quicker can be decoder. Here it is attainable to fabricate extensive size PMOS transistors.

9. Proposed SRAM Modification Using TGL

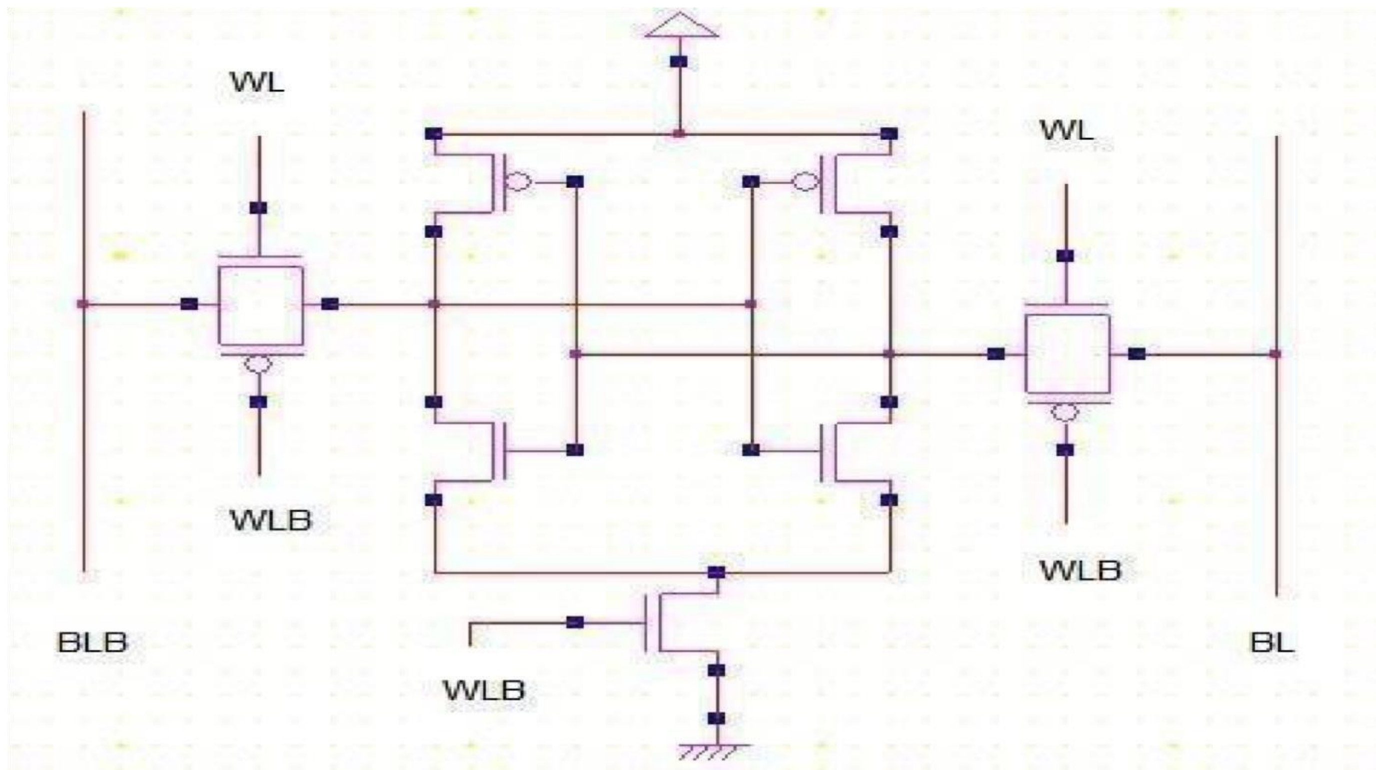
The novel design of SRAM cell is shown in below figure where, we place the transmission gates instead of nmos pass gates this is because of the way that the transmission gates have low voltage drop contrast with pass transistors.

As we know NMOS causes a voltage drop of V_T so not good for pre chrge output as it out of (V_{DD}- V_T) not V_{DD}. So in TGL we have both NMOS and PMOS connected in parallel. So it allows to pass both 1 and 0 in a good way, with no voltage drop occurs. So a tremendous power improvement is happened due to it.

Likewise we have also used an extra NMOS which acts as a switch furthermore it is important to confine a short circuit current when the information is composed in the rudimentary cell.

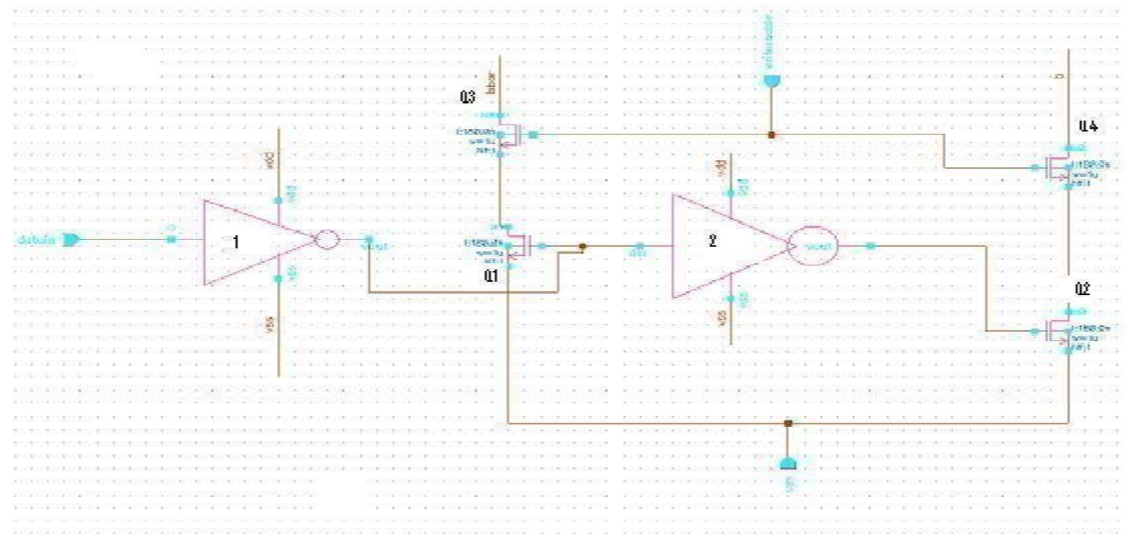
And also the R/W operations of our modified circuit is same as that of customary 6T SRAM.

As we know NMOS give good 0 but not good 1, so here in transmission gate logic both pmos and nmos devices are kept in parallel. So it allows to pass both 1 and 0.



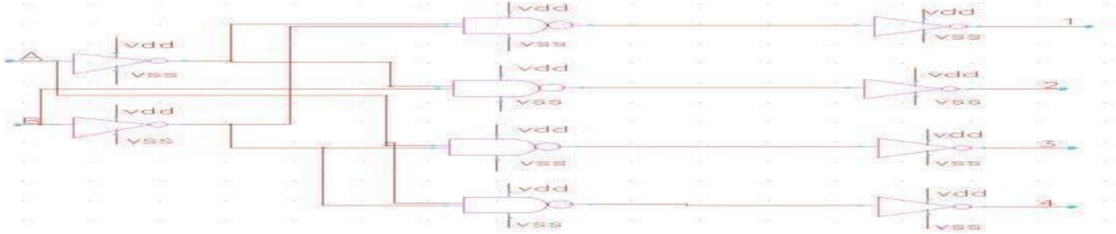
10. Write Driver Circuit

The main intention of using this write driver circuit is to fasten the discharging process of one of the bit lines from the pre charge level to below the write margin of the SRAM cell. Normally, it is activated by the Write-Enable (WE) signal and drives the bit line using full-swing discharge from the pre charge level to ground level. The order in which the word line is activated and the write drivers are activated is not crucial for the correct write operation. It predominantly uses two stacked NMOS transistors to form two pass transistor AND gates using NMOS Q1,Q3 and Q2,Q4 transistors. The sources of NMOS transistors *Q*1 and *Q*2 are grounded. When activated by write enable, the input data enables, through inverters 1 and 2, one of the transistors *Q*1 or *Q*2 and a strong "0"is applied by discharging *bit line* or *bit line bar* from the pre charge level to the zero condition/level.

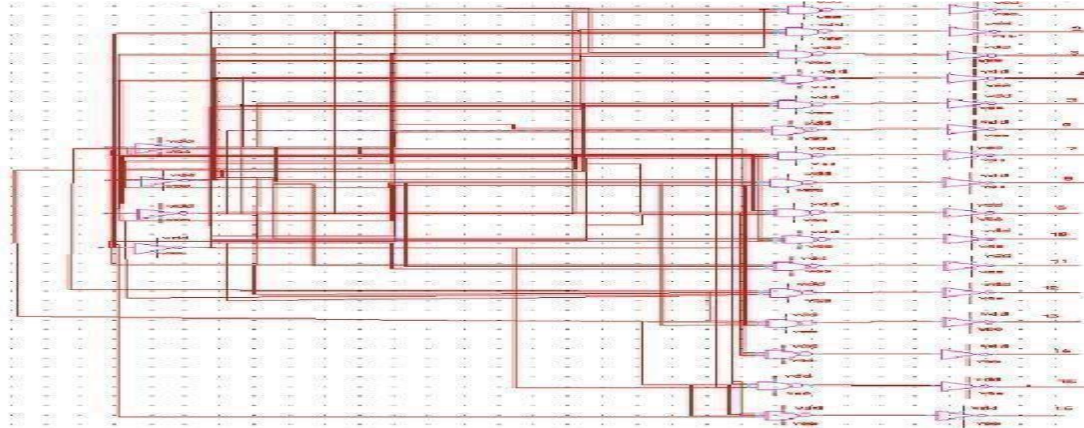


(Schematic of write enable circuit)

11. Schematic of Memory Array and Its Periphery

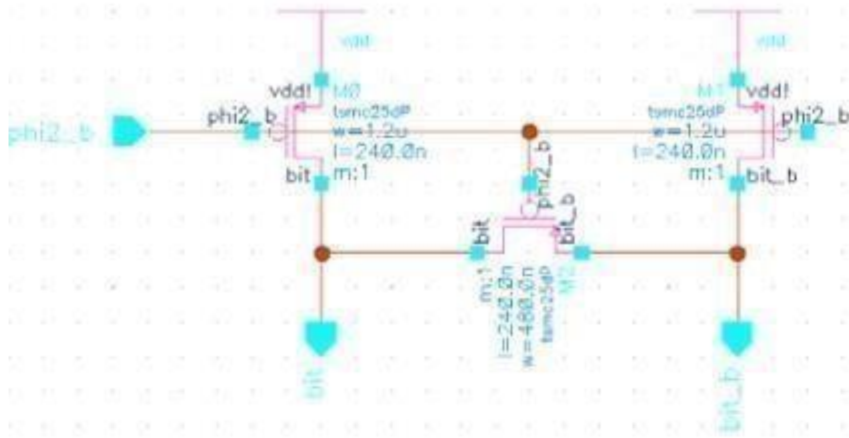


(Schematic of 2-4 decoder)

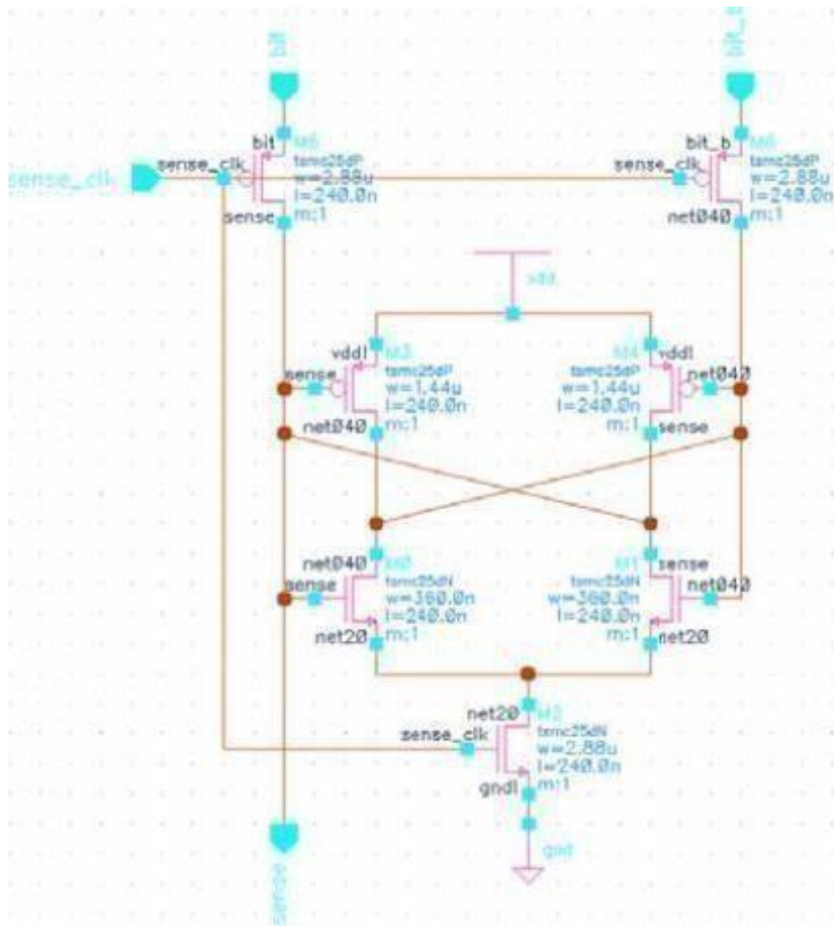


(Schematic of 4-16 decoder)

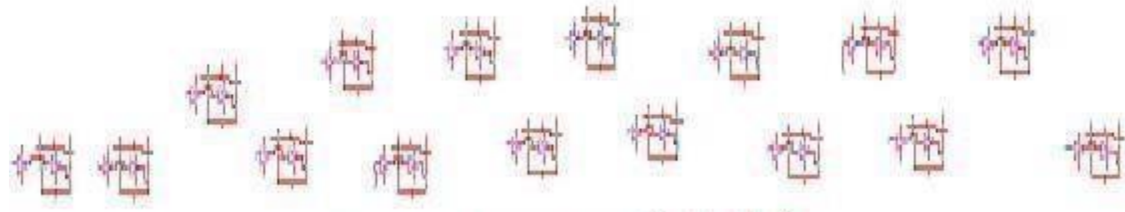
(Schematic of transmission gate)

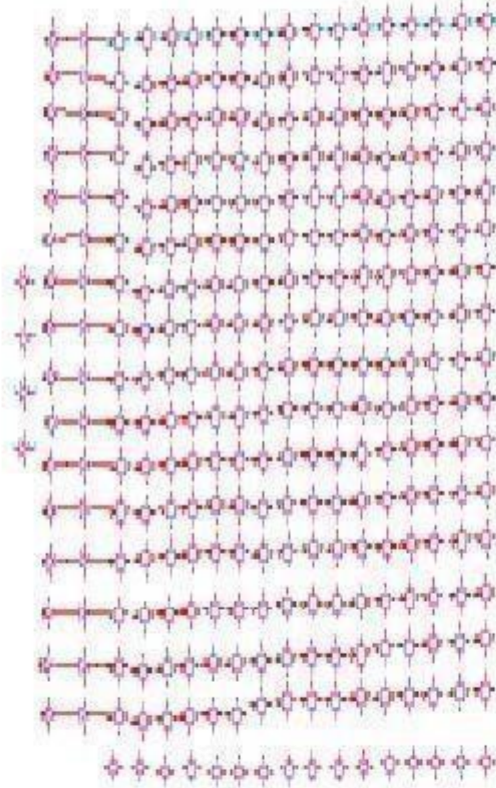


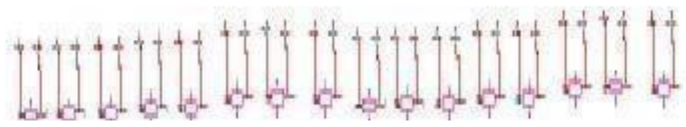
(Schematic of Pre Charge Circuit)



(Schematic of Sense Amplifier)







(SRAM 16×16 SRAM ARRAY)

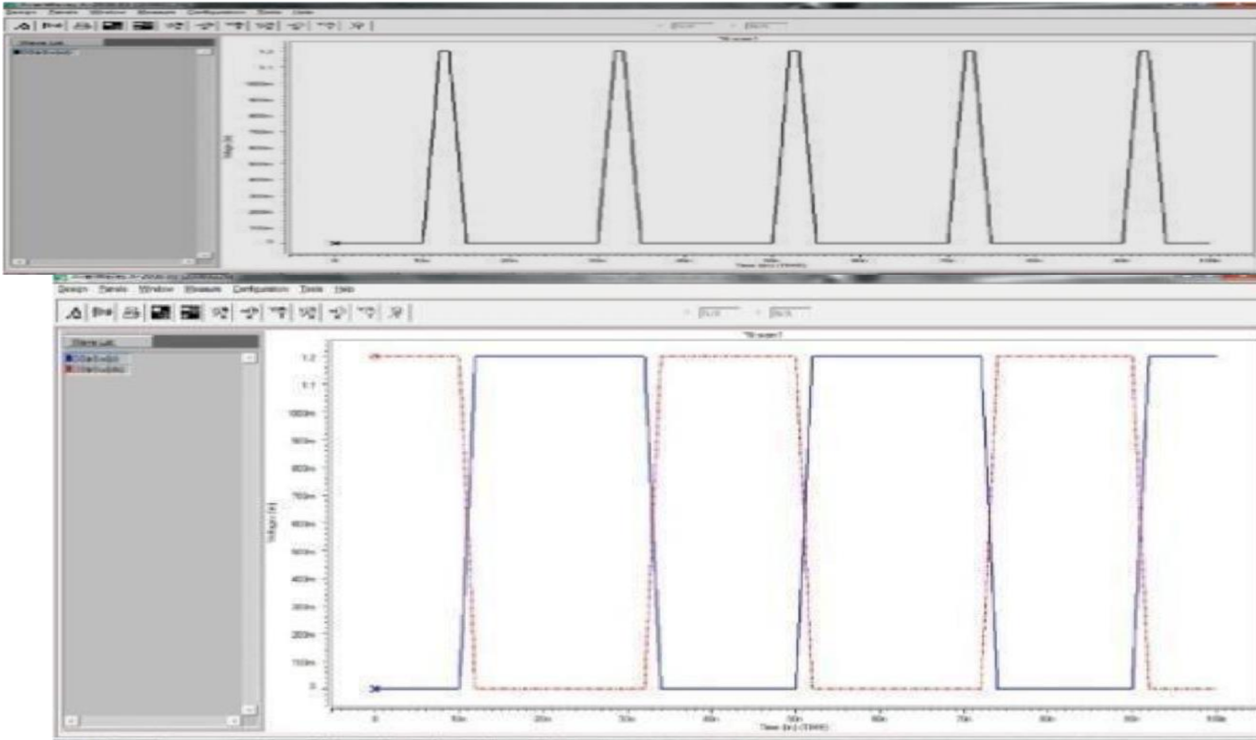
12. Result and Analysis

By analyzing the conventional SRAM cell we got following waveforms

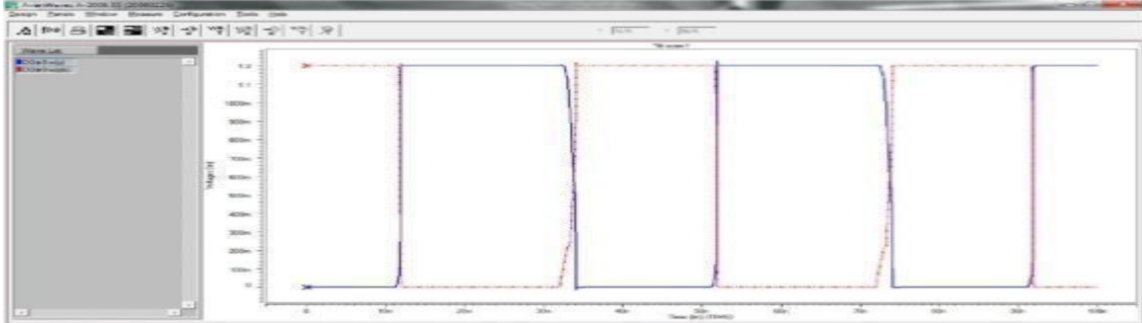
I/O Waveform of Basic 6T SRAM

Input word-line voltage (WL) vs Time.

Input bit-line voltages BL & BLB vs Time.

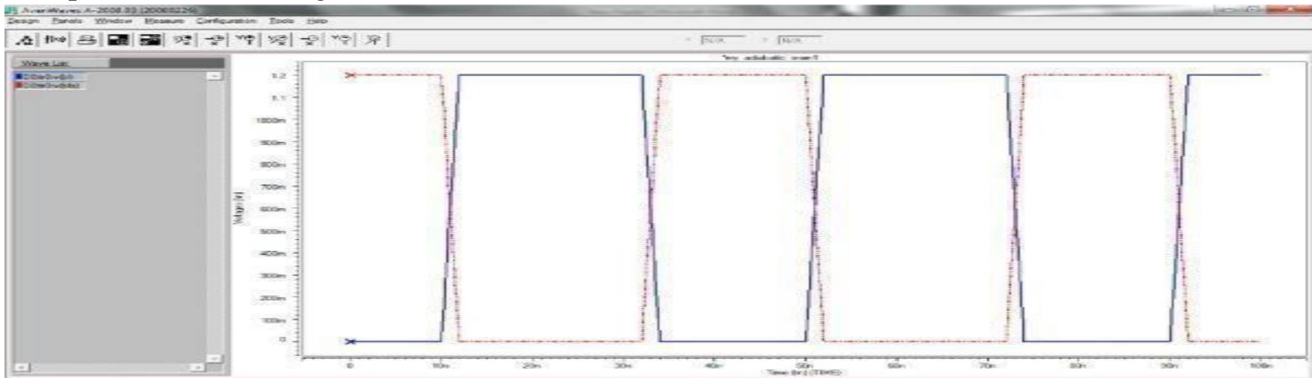


Given below screenshot-3: Shows the output voltages QA and QB

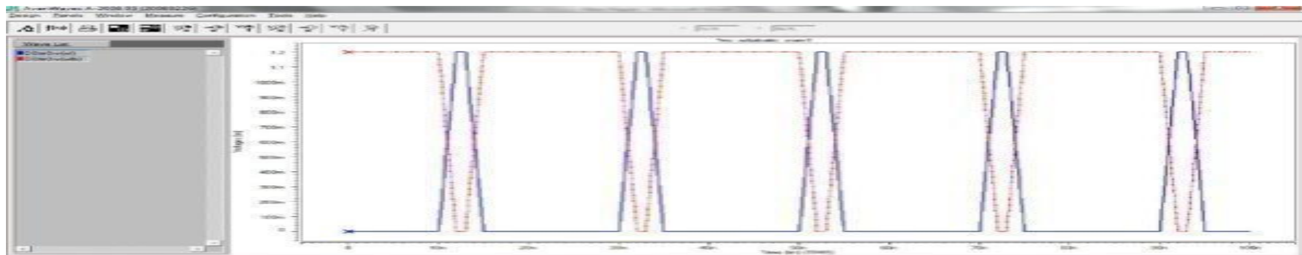


I/O Waveform of Modified SRAM Cell Using TGL

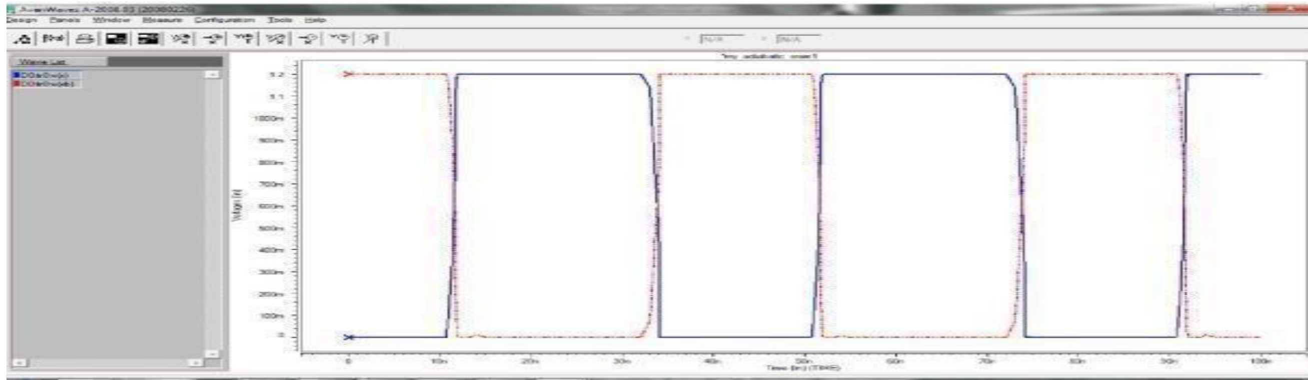
Input word-line voltage WL & WLB vs Time.



Input bit-line voltages BL & BLB vs Time



Output voltages QA and QB vs Time



Power consumption in both conventional and modified SRAM cell and its comparison

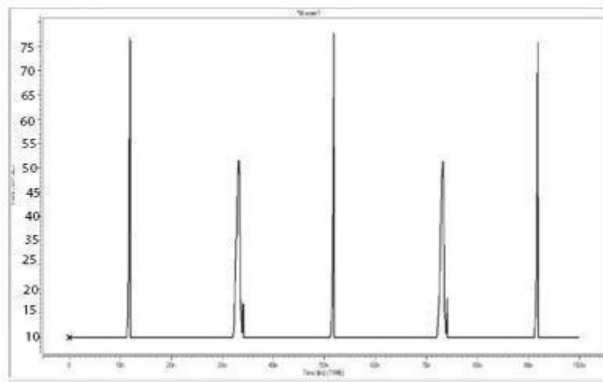
By giving 1.2V dc power supply and 1.2V trapezoidal wave in BL and WL the simulation of both conventional one and modified one is done and I got the above power spectrum and the comparison of their

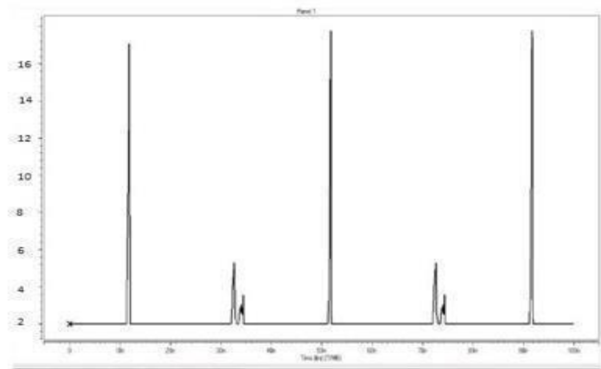
power utilization is expressed below.

CONVENTIONAL SRAM CELL	PRPOSED SRAM CELL
P_{max}= 60 uW	P_{max}= 16uW
P_{min}= 40uW	P_{min} = 3.5uW

From this we see that a lot of power improvement can be done by using this simple method nearly (60% power loss is reduced).

Conventional Cell design **Purposed Cell Design**





Temperature V/s Power Dissipation

Now we varying the temperature from 0 to 80^0 Celsius we see the variation of power w.r.t. the temperature variation. As we increase temperature the career concentration increases so leakage power also increases drastically.

TEMPERATURE (DEG CENT.)	POWER DISSIPATION(uW)
0	56.881
10	58.406
27	64.572
50	78.533
80	92.689

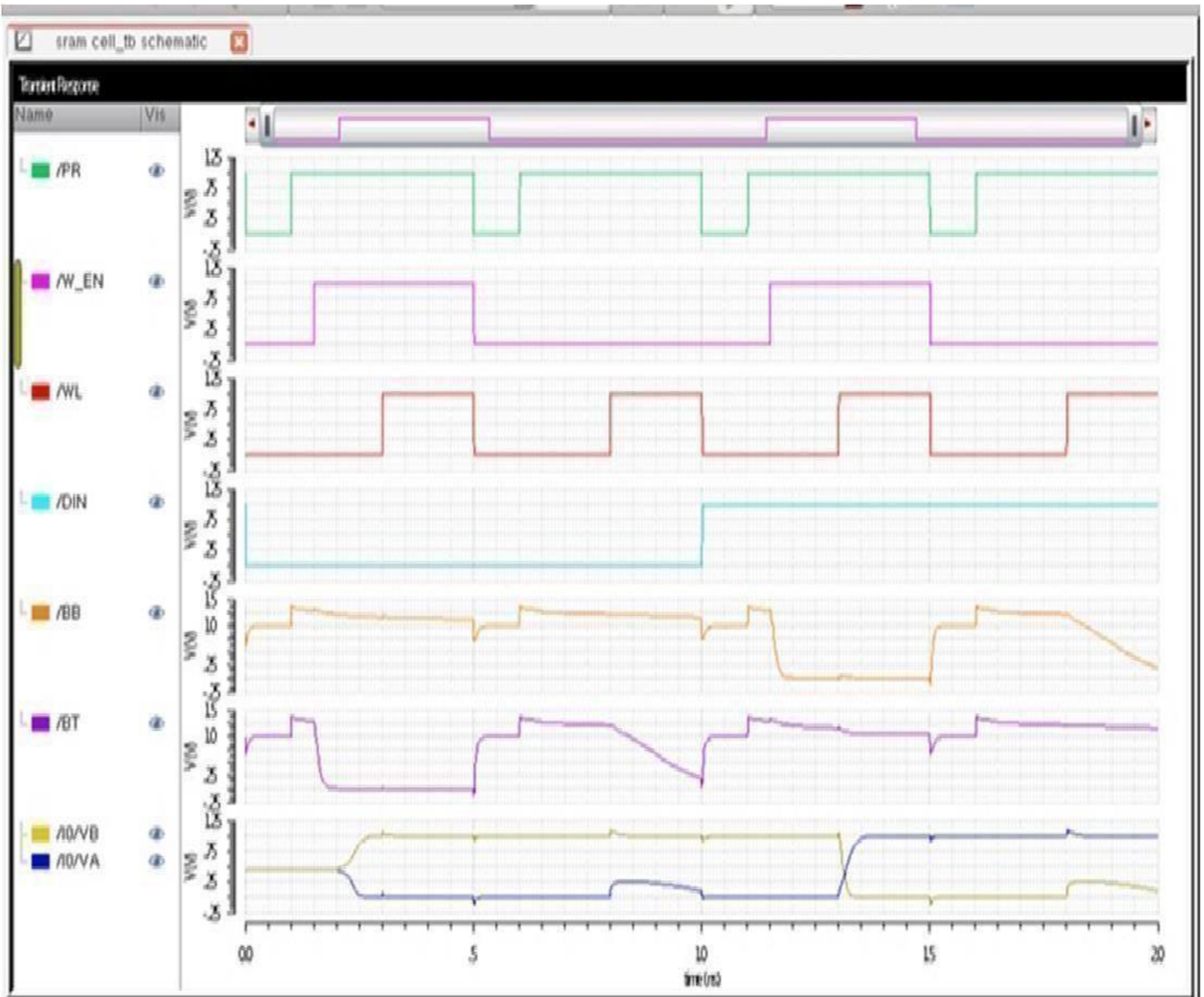
Supply Voltage V/s Power Dissipation

To calculate power supply voltage V_{DD} is changed from 2 to 0and corresponding power dissipation is recored and tabulated . As we increase supply voltage power dissipation also increase as power loss is proportional to voltage square i.e. V_{DD}^2.

SUPPLY VOLTAGE (V)	POWER DISSIPATION(uW)
1	24.14
1.2	34.92
1.4	40.18
1.6	60.34
2	80.63

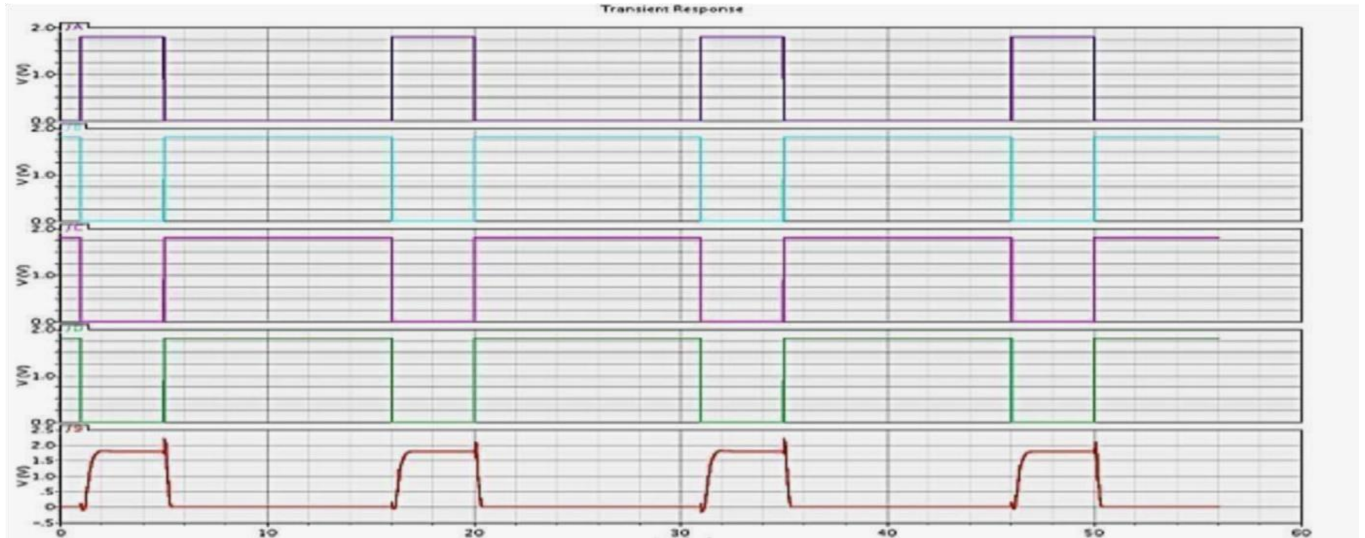
Now varying the input control value we got the following transient analysis of graph with respect to the time for SRAM cell,4-16 decoder and 16×16 SRAM array.

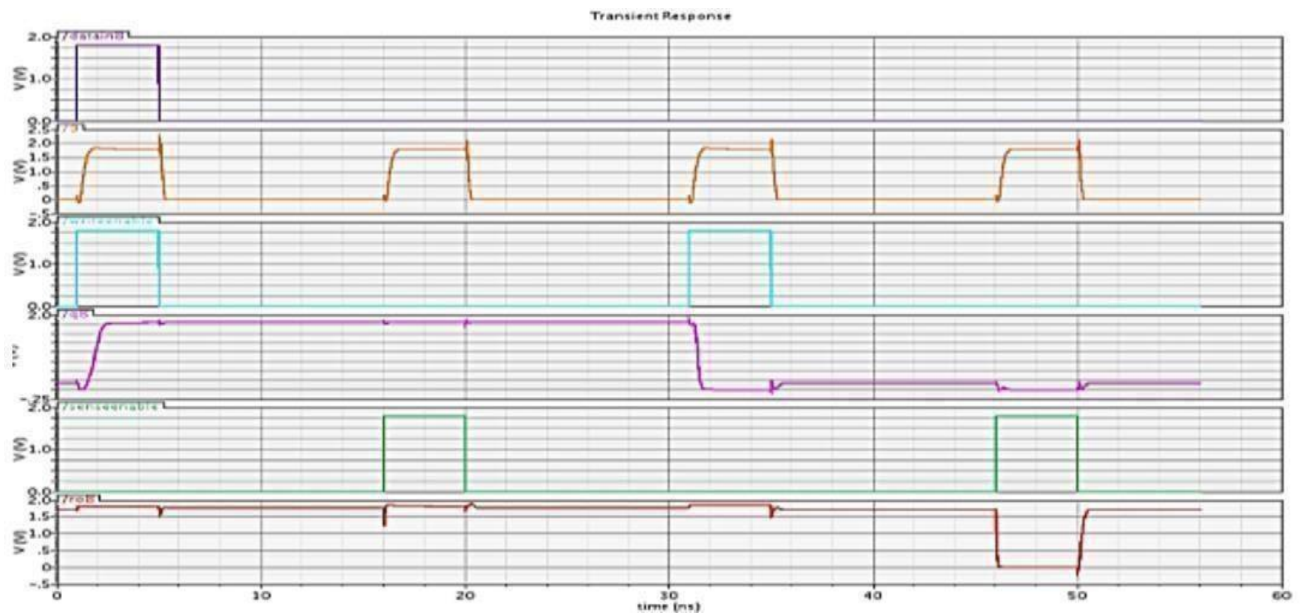
Transient Analysis for SRAM CELL



sram cell_tb schematic
Name
Vis
/PR
/W_EN
/WL
/DIN
/BB
/BT
/I0/VB
/I0/VA
time (ns)

Transient analysis for 4-16 Decoder & SARAM Array





13. CONCLUSION

The works done in this project are summarized as follows:

- In this project, an optimization of 16×16 SRAM memory for low power application had been carried out using simulations. The memory was built using an array of modified CMOS SRAM cell. The replacement of the pass transistor by a transmission gate was done to modify the conventional SRAM cell.
- Impact of temperature and supply voltage on power dissipation of the SRAM cell was also investigated. It was observed that a decrease in temperature and supply voltage results in a significant reduction in power dissipation of the cell.
- Then memory peripheral like column circuitry and row decoders were designed using dynamic logic so that it consume less area and fasten the response also.
- Finally the transient analysis of the memory with the sense amplifier and pre charge circuitry is done to obtain an insight into its stable read and write operation as per the requirement.

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