Subthreshold Modeling and Simulation of Silicon Nanotube Field Effect Transistors (SiNTFETs)

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF

THE REQUIREMENT FOR THE DEGREE OF

Bachelor of Technology in Electronics and Instrumentation
And
Master of Technology in VLSI Design and Embedded Systems

Submitted by
SUNKARA THANDAVA SESHA TALPA SAI
(710EC2122)
to

Department of Electronics and Communication Engineering
National Institute of Technology, Rourkela, India.
June, 2015.

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Under the Supervision of
Prof. Pramod Kumar Tiwari

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Department of Electronics and Communication Engineering, National Institute of Technology, Rourkela

Certificate

This is to certify that the thesis entitled " Subthreshold Modeling and Simulation of Silicon Nanotube Field Effect Transistors (SiNTFETs)" being submitted by Sunkara Thandava Sesha Talpa Sai bearing Roll No. 710EC2122 to the National Institute of Technology, Rourkela, in the Department of Electronics and Communication Engineering is a bonafide work carried out by him under my supervision and guidance. The research reports and the results presented in this dissertation have not been submitted in parts or in full to any other University or Institute.

Place: Rourkela
Date:

Prof. P.K Tiwari
Dept. of ECE
National Institute of Technology
Rourkela-769008

DEDICATED TO MY PARENTS

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Sunkara Thandava Sesha Talpa Sai

Abstract

The MOS technologies with low device geometry and new architectures have accelerated the pace of computational technology. In order to uphold the challenges of scaling in sub 20nm regime and meet the aggressive specifications of ITRS, a novel and non-conventional devices have to intervene. So came the ultimate solution- Silicon Nanotube Field Effect Transistor (SiNTFET) with its unique architecture which enhances the electrical characteristics of the device and the performance.

In this work, an analytical model of surface potential and threshold voltage for SiNTFETs are developed. The two dimensional poisson's equation with a cylindrical coordinate system, has been evaluated to find surface potential. The concentration of the inversion charge has been evaluated in the channel in subthreshold regime using the surface potential equation and the Boltzmann equation. The threshold voltage of the device is stated as the gate voltage for which the calculated inversion charge equals the threshold charge. Assuming this definition, the threshold voltage of the device for different channel lengths is mathematically modeled.

The effect on threshold voltage by the variation of physical parameters is detailed analysed. The physical parameters include gate oxide thickness, tube thickness and core thickness. The effects of DIBL and voltage roll-off are discussed. The model results are verified with the simulation results obtained by using device simulator, ATLAS^{TM}. It is observed that for short channel lengths (<30nm), the model values vary from the simulated data; that is because the quantum mechanical effects are neglected during modeling which are vital in those channel lengths. The objective of the work is to provide a basic model for threshold voltage of the SiNTFET. The electrical characteristics show that device has a potential to set a new technology road map and meet the ULSI applications.

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CHAPTER 1

1 INTRODUCTION

1.1 Semiconductor Devices: A Brief History

'Necessity is the mother of invention'. We humans always desire to make our life more and more comfortable resulting in exploring more new and new things. This burning desire to explore a new world led to the civilization. As the civilization started, people started exploring new places, started exchanging ideas, started questioning and gradually led to the revolution in the Science and Technology. And technology is changing along the lines of materials. We had Stone Age, Bronze Age, Iron Age and so on. Now going through the phase of Silicon Age.

In 1830s Michael Faraday noticed the decrease in resistance of silver sulphide as temperature rises. In 1839 another renowned researcher Edmund Bequerel discovered photovoltaic effect operating principle of solar cell. Both the researchers have explored the intrinsic properties of the semiconductor. In 1870s, German Scientist Karl Braun had noticed that a point-contact semiconductor rectifies alternating current and could replace vaccum tube diode. Amid 1873, researcher W. Smith discovered photoconductivity in selenium. In 1878, acclaimed researcher E.H. Hall found there will be a potential will be developed across a conductor when a perpendicular magnetic field is applied to that of the flow of current named as the Hall Effect. In 1880s, magneto resistance was analysed in solid state by J.J.Thompson.

In 1900, a theoretical physicist, Max Plank originated the idea of quantum theory which was later supported by another renowned theoretical physicist, Albert Einstein by discovery of the law of photoelectric effect. Around 1910, researchers started classifying solid materials as insulators, metals, and "variable conductors" and the term semiconductors' slowly coined. In 1920s, an accomplished physicist Lilienfield is said to be pioneer to propose semiconductor

triode. The theories of energy band models and rectifying junctions were established by 1930s. In 1947 Shockley, Bardeen, and Brattain of Bell Labs invented the first point-contact transistor. The first working transistor came in 1954 and MOS transistor in 1960 by Bell Labs. Later on transistors became ubiquitous in modern electronic systems and modernized the pace of technology.

From that point, there was a continuous progression of the solid state devices. This is followed by SSI, MSI, LSI, VLSI and presently ULSI where devices are of Nano crystalline materials and Nano electronics is ruling the semiconductor technology. The decrease in size of the transistors which is known as scaling and made a tremendous impact, but it has constraints at nanoscale.

1.1.1 Scaling: a review

The 20^{th} century made a start of an epoch in automation, information sharing, industrial electronics and technology. Scaling down of the hand gadgets and computers with every conceivable application; altered the world of communication. It is all because of high speed low power, ultra-small sized semiconductor devices and their implementation by the VLSI design.

It began in 1925 when the view of Lilienfeld's IGFET bore the possibility to supplant the technology of vacuum tube with the lesser sized semiconductor technology [1]. The initial explanation was done 1960 by Atilla and Kahng [2] as the Silicon-based MOSFET. Later in 1958, a researcher from Texas Instruments, Jack Kilby had explained the thought of Integrated Circuits (IC) and a designer from Fairchild Corp, Robert Noyce had designed the first IC (S-R flip lemon) .In the next year, Richard Feynman conveyed his important message, "There is plenty of room at the bottom", referring the small sized devices with high performance [4]. A great visionary ,Gordon Moore, who worked with Fairchild Corp. and also co-founded Intel,

said that the transistor count on the IC doubles for every 2 years. The prescience was precise for over 3 decades as indicated in Fig. 1.1. In 1962, there was a development of the TTL the first logic family [3].Intel in 1972 came up with the first microprocessor with more than 2000 PMOS transistors. Subsequently it used NMOS technology which later discontinued due dynamic power consumption was high during the increase in the transistors per unit area. The introduction of CMOS technology eliminated that problem and made integration at higher levels and now heading towards nanotechnology.

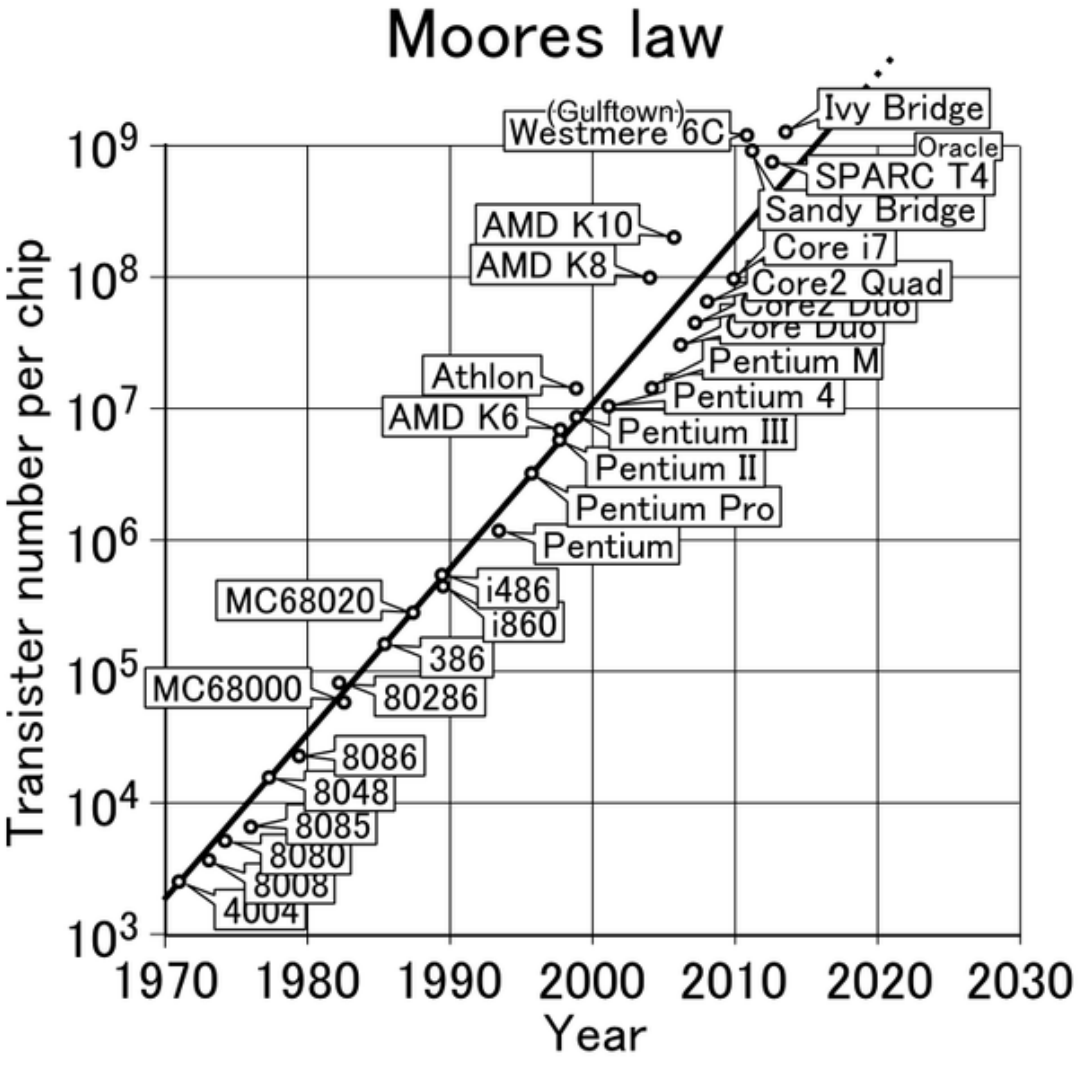


Fig. 1-0-1 Transistor integration illustrating the Moore's Law

The another main advantage of the CMOS technology is it has definite scaling laws. . The International Technology Roadmap for Semiconductor (ITRS) has directed the scaling in terms

of cost and power consumption. In 2014 ITRS committee planned to reorganize ITRS Roadmap to suit the necessities of the present day industries. Fig. 1.2 shows the plan of the ITRS committee and the seven objectives. It is targeting to go beyond CMOS technology like spintronics, memristors, and others. In April 2015, TSMC Taiwan Semiconductor Manufacturing Company announced that 10nm production would begin in 2016.It is still working forward to shrink CMOS. The device engineers could do this because of "scaling". Scaling is explained as the controlled fabrication of device dimensions in such a way that it acquires smaller chip area and maintaining the performance and long channel characteristics. Scaling also reduces the dynamic power through lesser voltages which is a significant in the device performance. In order to avoid SCEs and ensure better electrostatic control the lateral and the vertical dimensions are scaled down by a same factor.

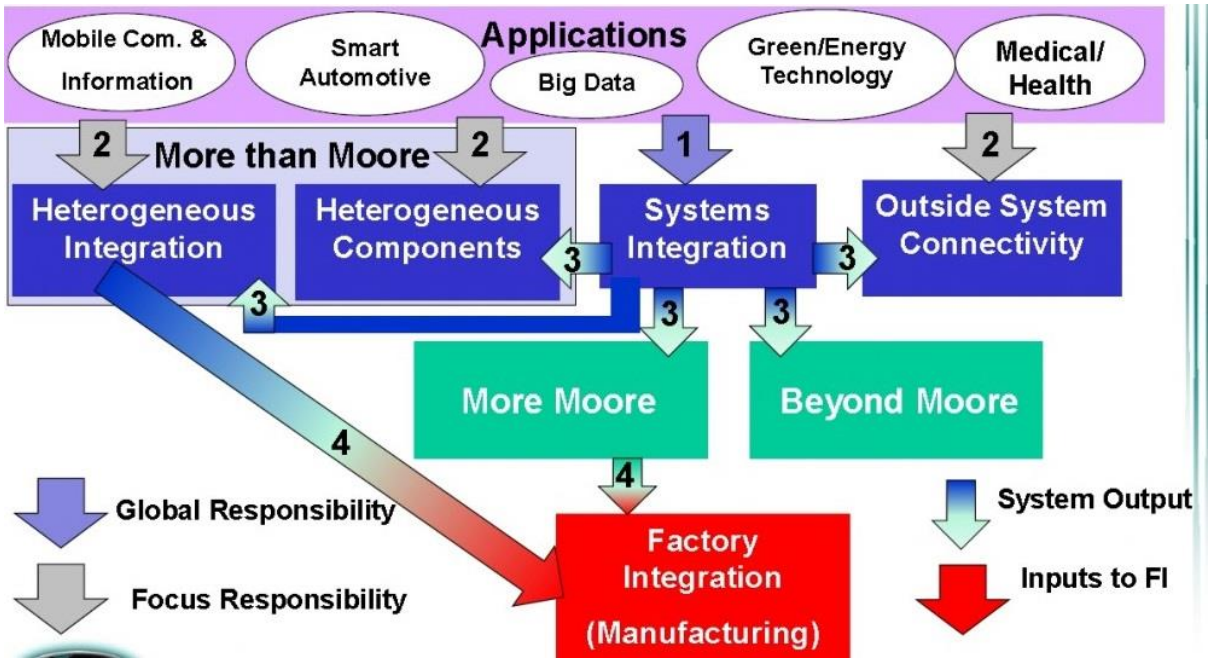


Fig. 1-0-2 ITRS 2.0-anounced by ITRS committee in April 2014

MOSFET is being used in the present monolithic ICs as the basic switching component in the digital logic circuits and also as an amplifier in the analog circuits. This led to a faster and complex chips and incessantly decreasing the unit coast of the IC.

1.2 Challenges in Scaling

Integration of so many billion transistors on an IC is possible due to patterning every minor feature of silicon by optical lithography. As the optical lithography entered to the sub-wavelength regime, interference and diffraction causes image disorder. So, patterning is difficult without proper resolution enhancement techniques.

For getting higher performance and lower threshold voltage gate oxide needs tremendous scaling which results in the increase of tunnelling leakages. The increase in substrate doping can check short channel effects however lessen the current drive by increasing the scattering. The trade-off between SCEs, low current and power consumption is the most important today which the conventional devices fail to achieve. This provides an approach of substitute device structures to continue further scaling of CMOS. The scaling in the MOSFET varies both the vertical and lateral dimensions.

1.2.1 Vertical Scaling

1.2.1.1 Polysilicon Depletion Effect

The Vertical scaling increases the effective thickness of the oxide which results in the degrading the transconductance and capacitance of the gates. The factor which is responsible for the oxide scaling is a thick polysilicon depletion layer during inversion region of the device. The depletion region of the device can't be further lessened because doping confinements as the solid solubility of silicon is fixed at a given temperature. This effect also causes to a shift in threshold voltage and is more apparent at lower doping densities of polysilicon gate. So, the technology forecasts the application of a metal gate to evading these challenges.

1.2.1.2 The Quantum effects

The oxide scaling causes a stronger surface electrical field at the silicon/oxide interface. This makes the potential well which prompts the quantum confinements of the inversion carriers.

This leads to distinct sub-bands for the movement in the perpendicular direction to the interface resulting in change of the peak of inversion charge centroid farther from the interface. This confinement drops inversion charge density for given bias resulting in the increase of the threshold voltage.

1.2.1.3 The Gate Tunnelling

By reducing the thickness of the gate oxide, the power dissipation in the static condition rises and the key reason is the Gate tunnelling. This phenomenon is quantum mechanical where particles tunnel across a barrier where as in classical mechanics it does not exist. Fig. 1.3 shows the band diagram of direct tunnelling in MOS transistor. The high -k dielectrics (viz. HfO_2, $HfSiO_4$, and Si_3N_4) can check gate tunnelling to some extent.

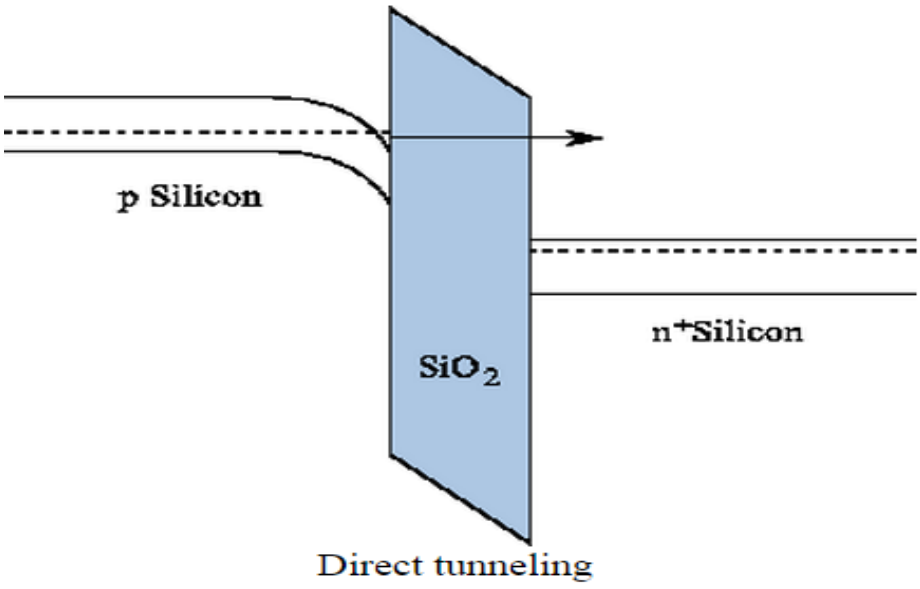


Fig. 1.3: Band Diagram showing electrons tunnel through the whole SiO_2 energy barrier

1.2.2 The Lateral Scaling

1.2.2.1 Threshold voltage roll-off and DIBL

By scaling the lateral dimensions, the depletion width of S/D channel p-n junction becomes substantial in relative to channel length which causes diminishing the gate control over channel. The barrier of the channel also decreases immensely by increasing the scaling of the channel which is known as threshold voltage roll off.

The roll-off of threshold voltage is more prominent when there is a higher drain bias. This is because increment in the drain voltage causes further penetration of drain-induced field into channel which leads to reduction of the potential barrier which is commonly under the control of gate. This is known as drain induced barrier lowering (DIBL) .The decrement of threshold voltage due to DIBL can be analysed by the semi-experimental 'charge sharing' model.

According to that model, the depletion charge in the device can be divided into two parts. The first one is because of the gate control and the second one is by the control of the source and drain. So, this presents a rectification in the maximum depletion charge which is controlled by gate and that determines threshold voltage.

1.2.2.2 Hot Carrier Effect

The hot carriers will cause impact ionization and lead to drain-body current and may even lead to channel breakdown. So this effects the reliability, increasing SCEs and this leads to decrease in threshold voltage and increase in sub-threshold drive current. Fig. 1.4 illustrates impact ionization by the hot carriers in the MOSFET. This leads to degradation of silicon-oxide interface which in long term leads to rapid aging of the device. The breaking of Si-H bond leads to the degradation by releasing hydrogen atom to substrate.

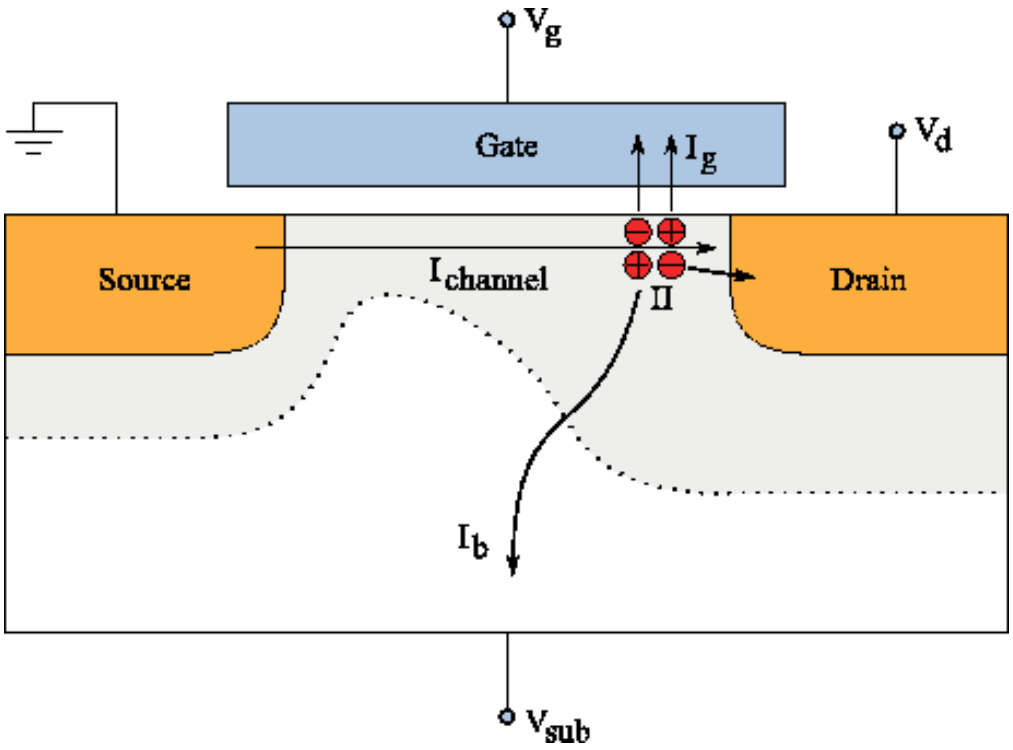


Fig. 1.4: Hot carriers causing impact ionization and generate electron-hole pairs

1.2.2.3 Mobility Degradation

Continuous scaling of MOSFETs also needs to continuous increase in channel doping to decrease the junction electric field and to avoid overlapping of source and drain depletion region in the channel. As device dimensions reduce the lateral field increases, mobility depends as a function of electric field and so velocity saturation occurs. This leads to current saturation. Similarly, as the vertical field increases there will be more scattering of electrons at the surface leading to the decrease in surface mobility.

1.3 Technology Boosters: Scaling Solutions

1.3.1 Channel Engineering

1.3.1.1 Shallow S/D Junction

By bringing down the junction depths of drain/source will decrease the drain coupling to source barrier. But for keeping the sheet resistance same, we need to increase the doping as the S/D junctions get shallow. But we can't keep on increasing the doping density as there is an limit

for the solubility of the dopants. So, decreasing the junction depth leads to rise in series resistance of the channel. Also it is not easy for the technology to make ultra-shallow junction so that it would remain abrupt even after annealing steps which are necessary for activating the dopants and to decrease the resistivity. Because of these abrupt S/D junctions, there is an increment in band to band tunnelling leakage current and degrade the performance of the device.

1.3.1.2 Halo Doping

To decrease the short channel effects, different channel engineering techniques are employed. For digital circuits halo doping is highly crucial. The halo implants effect the in the linear region of current voltage characteristics of the device. The on current for halo-doped regions is higher than the uniformly doped device. In saturation region of the device the output resistance degrades by having a higher drive current in that region compared to uniformly doped device. Halo doping at the drain side causes lower saturation voltage of the device. For shorter channels the halo doping of source and drain overlaps and so leads to increase the average channel doping concentration which causes to increase the threshold voltage.

1.3.1.3 Strain

By applying strain, the mobility of electrons and holes increased which results in the increase of conduction in the channel. The PMOS and NMOS perform differently for different strains. The better of PMOS occurs when there is a compressive strain applied to the channel. The NMOS performs best at tensile strain. The stained-Si CMOS technology has become an important technology node which can maintain higher current drive. These methods compatible with other technology boosters like high k dielectrics or metal gate or multi gate technology.

1.3.1.4 Multi-Material Gate

Multi material gate is one of the best methods to avoid hot carrier effects. Here multiple gates are cascaded which have different work functions. In 1999 Double Material Gate structure has been proposed and later on many other multi material gate devices are developed. The metals are to be arranged such that the metal (screen gate) near the drain (M2) should be having the lower work function and at the source side (control gate) with a higher work function. Due to this the lateral electric field and the velocity of electron increases at the interface in the channel. So overall there is an increase in the gate transport efficiency. Any variation in the drain voltage will not highly effect the potential distribution in the channel because the lower work function metal will take the voltage drop across it leading to maintain the same minimum surface potential. The ratio of the screen gate and control gate are design parameters for the designers for getting the optimum performance. Fig. 1.5 shows dual metal structure.

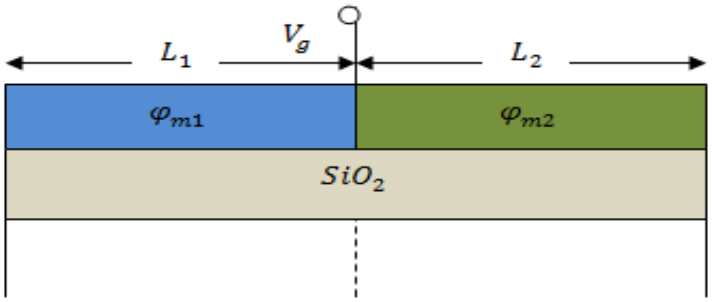


Fig. 1.5.Dual Metal Gate structure

1.3.2 Gate Engineering

1.3.2.1 High-k dielectric

The materials with higher dielectric constants than silicon diode are considered as high-k dielectrics. This is one of the widely used techniques for scaling down the devices. As the oxide thickness comes below 2nm, the gate tunnelling effects becomes significant. So we need to

increase the thickness in such a way that the gate capacitance won't be disturbed. So this introduces higher dielectric constant materials to replace conventional silicon dioxide and thereby decreasing the leakage currents.

1.3.2.2 Metal Gate

In the beginning it is expected that poly-Si or the high-k dielectric gate stack can improve the gate leakage current. But further analysis and the experiments showed that there is a significant decrease in the mobility in comparison to metal gate technology. This is because the work function varies according to the gate dielectric and leads to variation in band alignments.

1.3.2.3 Multiple Gate

A multi gate device indicates a MOSFET with more than one gate. These multiple gates are controlled by single electrode or each one independently. Multiple gate gives additional advantages of controlling the channel more effectively and designing the device according to the necessity. In Planar Double Gate MOSFETs, the drain, source and channel is sandwiched between two gates. This is fabricated by layer by layer preventing the difficulties of lithographic techniques which occur in non-planar devices. But the problem in manufacturing the device is it is difficult to obtain a good self-alignment of the two gates. Tri-gate FINFET is formed by the oxide layer over a SOI wafer comprising the silicon layer and etching the oxide and silicon layers and forms a mesa by a mask. Now the portion of mesa by second mask and fin will form. This will result in forming a dielectric layer over the fin. The tri gate improved the manufacturability and the cost. It also decreases the fringing capacitance of the device. Fig. 1.6 shows the technology progress through multiple gates in MOSFETs.

Ultra-Thin body SOI MOSFETs have an advantage of very low off current the body is adequately thin. The body doping can be eliminated and the random dopant fluctuations can be avoided. The SOI technology gives advantages of low parasitic capacitance which is because

there is isolation from bulk silicon. This decreases the power consumption and so increasing the performance. There is no significant effect of temperature because of no doping and need of tapping in the body or well. The SOI wafers are being widely used in silicon photonics because the design enables internal reflection of the electromagnetic waves.

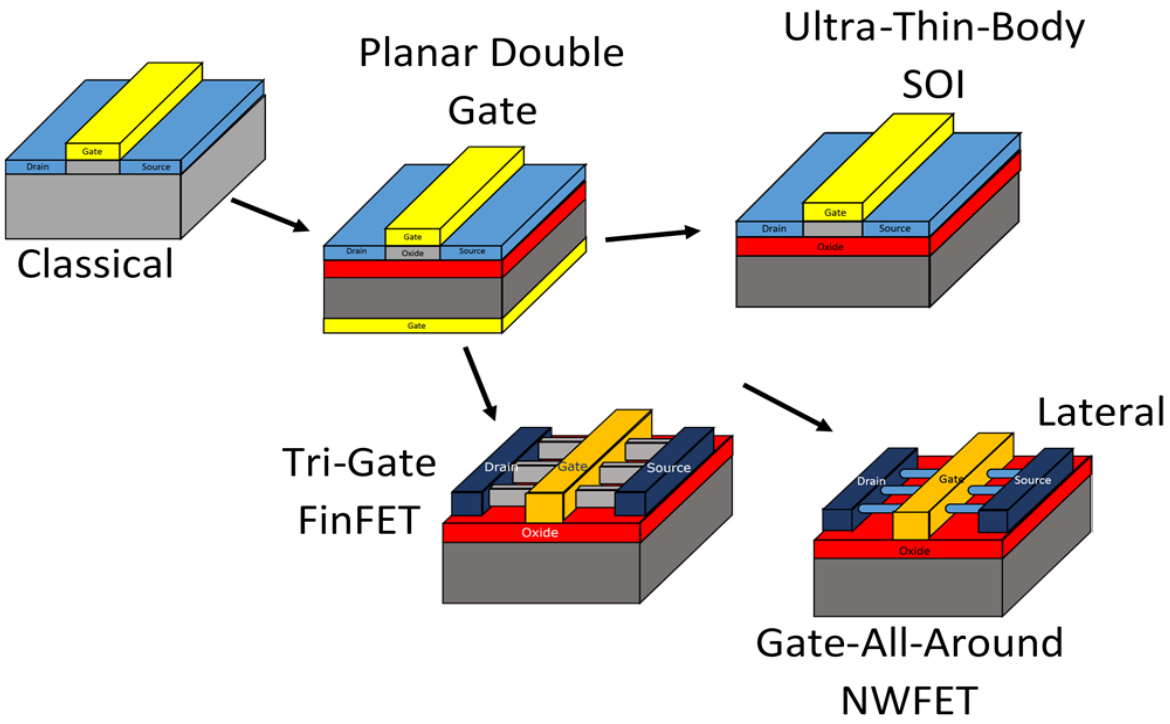


Fig. 1.6 MOSFET Technology progress through multiple gates.

Gate all around nano wire FETs surround the gate material surrounds the channel from all directions. It shows lower characteristic lengths the device and the capability of further scaling. The GAA nano wire transistor shows better short channel effects and better confinement of the electric field than existing devices. Now, the present technology came up with further advanced device with better switching performance and gave the hope for further scaling in sub

manometer regime and the best electrostatic charge control in the channel, that is -Silicon Nanotube FETs which will be detailed dealt in the thesis.

1.4 Thesis Organization.

In this chapter we have reviewed the history, technical terminology of the semiconductor devices and introduced the advance device SiNTFET.

Chapter 2: It presents a detailed literature review of Silicon Nano Tube Field Effect Transistors (SiNTFETs). At the end it explains the problem statement of the project.

Chapter 3: It presents the basic details of a device simulator ATLAS and at the end it presents the structure of the device.

Chapter 4: It presents the analytical modeling of the surface potential and the results are explained and verified with the device simulation results.

Chapter 5: The threshold voltage for SiNTFETs has been modeled. The results and discussions are completely elaborated and compared with the simulation results.

Chapter 6: It discusses the idea of modelling the cylindrical capacitances in SiNTFET.

Chapter 7: It gives the conclusion and suggests the future work that can be done.

CHAPTER 2

2 LITERATURE REVIEW

2.1 Fabrication of SiNTFET

The fabrication steps of SiNTFET has been patented by Tekleab *et.al* [5] in 2012. The Silicon nanotubular FET include a tubular inner gate named as core and outer gate as shell. They are separated by the silicon channel which is grown epitaxial. The source and drain are separated by spacers which covers the inner and outer gates. The strategy for fabricating the device comprises:-forming a cylindrical shaped silicon layer. Then form the outer gate which covers the silicon layer and placed in between bottom and top spacer. Then grow the epitaxial layer on the top spacer next to Si layer. Then etch the inner part of cylinder and forms a hollow cylinder. Then fabricate the inner spacer which exists at the bottom of inner cylinder. Then fill the hollow portion of the inner gate and put a side wall adjacent to inner gate .For making contacts, a deep trench is required to access the outer gate and drain.

2.2 Previous works on SiNTFET

In 2012, Fahad and Hussain [6] have compared various electrical characteristics of Silicon Nanotube FET with the silicon nano wire FET. They concluded that the architecture of SiNTFET gives the additional advantage. They have did the mathematical calculations the and simulations considering the transport models of semi classical which also includes the effects of quantum confinements for comparing between the SiNTFET and GAA FET. They concluded that for a same off current values the 20nm device of NWFET and SiNTFET the current drive of nanotube FET is 13 times of that of the nanowire FET while keeping the thickness of SiNTFET of 10nm and NWFET of 20nm diameter. They also conclude that

SiNTFET has area benefits and it uses only 11% of NWFET contact area for same output current. They found that nanotube's enhancement in the current drive while maintaining low leakage current and higher subthreshold swing. Fig. 2.1 shows that for a 10nm thickness of the channel in SiNTFET current drive is10 times of the GAA nanowire explained in their paper.

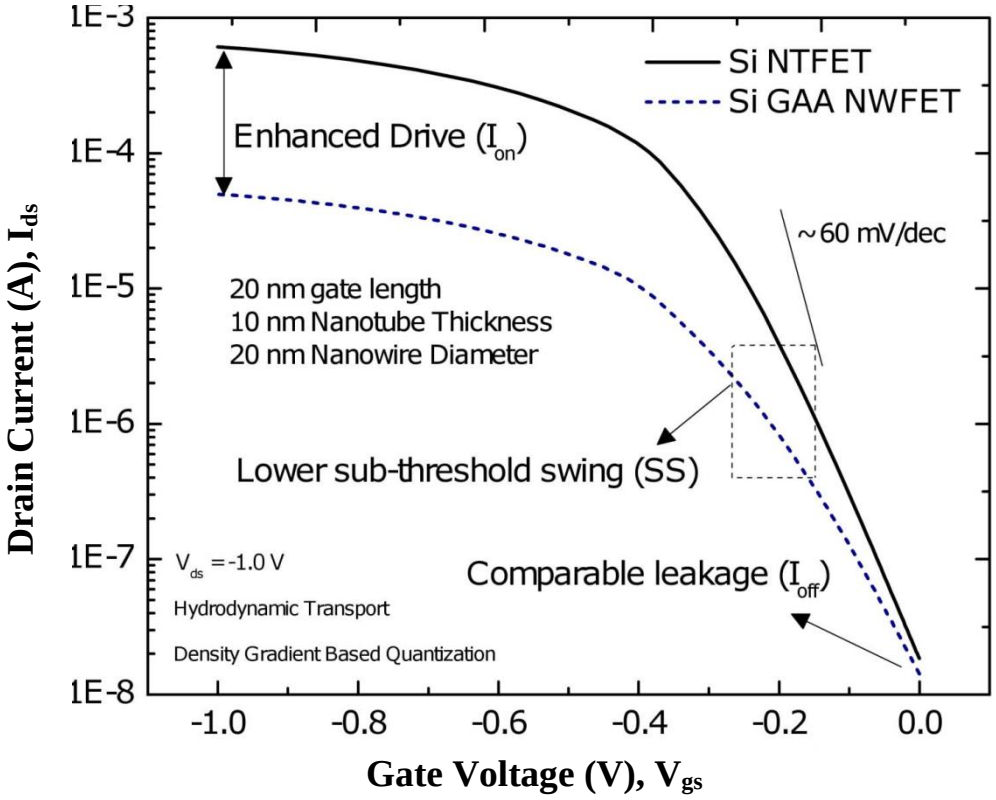


Fig. 2.1 Comparison of electrical characteristics of SiNTFET and GAA[]

Fahad *et.al* [7] explained how the architecture of SiNTFET gives the advantage by the quantum mechanical simulation study. The core-shell gates make a volume inversion in the channel. They have compared the carrier concentration of the nanotube with nanowire transistor. It is observed that the volume inversion takes place and controllability of the gate. They analysed the short channel effects in SiNTFETs which are minimal when compared with the NWFET. They have done the band gap analysis for the device and compared the planar silicon MOSFET. They have shown the scaling benefits of the device in comparison to others. They have detailed listed the drive current, subthreshold slope, DIBL and on -off current ratio for various devices

for comparison. Table 2.1 shows a comparative study of different devices given in his paper with all the references.

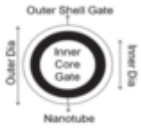
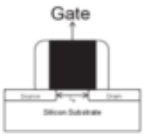
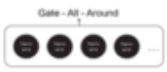
Device Type	N	N	N	N	P	N/P
Gate Length, L_g	20 nm	350 nm	32 nm	40 nm	800 nm	35 nm/25 nm
Gate Structure	Inner Core/Outer Shell 	2 x GAA Nanowire FET 	Planar MOSFET 	Tri-Gate 	500 x GAA nanowire FET 	1xGAA 
V_{dd}	1.0 V	1.2 V	1.0 V	1.1 V	-1.0 V	1/1.2 V
Normalization	Ave. Circumference	Diameter	Width	(2 x Height) + Width	-	Circumference
Drive current, I_{ds}	2.56 mA/µm	2.4 mA/µm	1.62 mA/µm	1.4 mA/µm	4 mA	0.825 mA/µm 0.950 mA/µm
Sub-threshold slope (SS)	72 mV/dec	60 mV/dec	< 100 mV/dec	76 mV/V	61 mV/dec	85 mV/dec 85 mV/dec
DIBL	63.15 mV/V	6 mV/V	~ 210 mV/V	89 mV/V	-	65 mV/V 105 mV/V
I_{on}/I_{off}	$>10^5$	$>10^6$	$>10^5$	$\sim 10^4$	-	~2E5/~2E5

Table 2.1 Comparing electrical characteristics of different FETs

The mathematical calculations say that for a same effective area for drive current, a single SiNTFET is equivalent to 44 NWFETs showing the area advantages. The current ratios explain that a SiNTFET is equal to 56 NWFETs put all together. They further explained that NWFET use a noble metal as a catalyst where as SiNTFET can be grown by selective epitaxy from the silicon material. This method has an advantage that it prevents any type of electrical shorts and protects from charge trapping. So, there will be little contamination in the device fabrication.

In 2014, Tekleab [8] analysed the Device performance of SiNTFET. As gate is completely covering the device it helps to provide full electrostatic controllability in the channel. He

concluded that for a same diameter of SiNTFET and NWFET, nanotube gives twice the drain current. The paper listed the advantages of SiNTFET as the best structure for short channel control. The charge carriers are highly confined by the architecture of the device. By the engineering techniques the tube thickness, depleted transistor performance can be realized. The multiple threshold voltage characteristics can be realized because of the two gates and they can be controlled individually. This adds an advantage to the designers as low and high performance ICs can be realized uniformly processed FETs. The device architecture makes it easy to apply stress which can be Drain/Source regions for increasing the carrier mobility. The device gives better short channel effects even when the diameter of the device is increased by keeping constant tube thickness; but in GAA MOSFETs the by increasing the channel thickness the SCE becomes significant.

The electrical properties are analysed by the 3D simulations. The doping in the channel region is decreased to avoid random dopant fluctuation which occurs during the fabrication of the device by molecular beam epitaxial growth of the channel. In SiNTFET peak of the carrier concentration in near the centre of the channel which shows the very high control of the inner and outer gates. The GAA showed a Vt roll of 150mV from 45nm to 14nm where as SiNTFET showed only 50mV. The subthreshold slope characteristics degraded for GAA for shorter channel lengths where as SiNTFET showed less than 80mV/Dec even at 14nm and showed that it is better than GAA by 5%.For same off current values, the on current of SiNTFET is 2.3 times the GAA. They also analysed the diameter dependence on subthreshold slope and on-off current ratio. The important results given by him are shown in Fig.2.2 which compare electrical characteristics GAA FET and SiNTFET for same diameters.

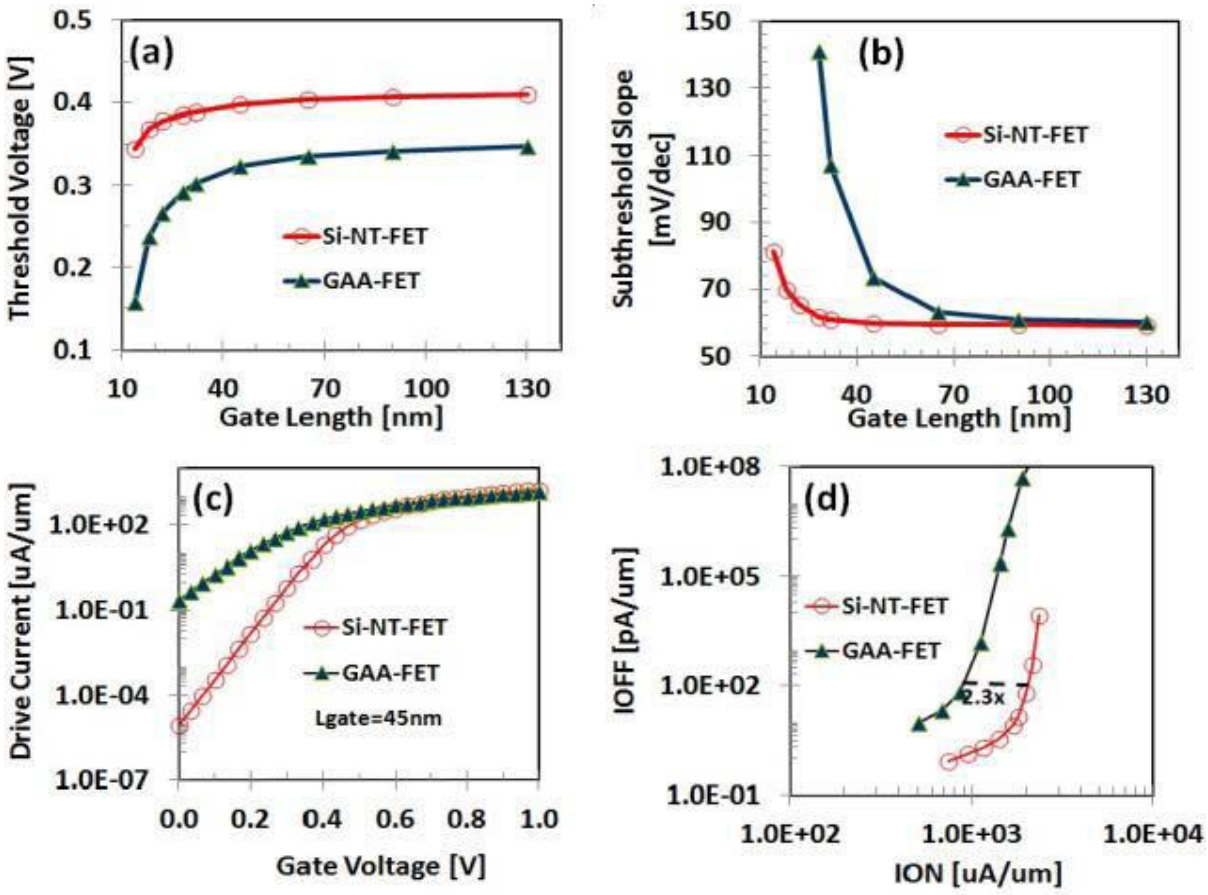


Fig.2.2 Comparison of electrical characteristics between SiNTFET and GAA

2.3 Device Structure

Analogous to the conventional MOSFETs, the device has Source, Drain, channel, gate oxide, extension, gate and spacers. The inner gate acts like a pillar for whole structure. Without the inner gate or core and replacing it by the silicon gives the structure of Silicon Nanowire MOSFET. Over the inner gate the gate oxide is surrounded and over which the channel and extension regions are formed. The channel is once again surrounded by the gate oxide and then the gate. The source, drain and the extension regions are highly doped to decrease the series resistance whereas the channel is lightly doped to decrease random dopant fluctuation. The device and its 2D cross section along the channel is shown in Fig.2.3. The tubular structure is shown in Fig.2.4 by removing the gate oxides and gates.

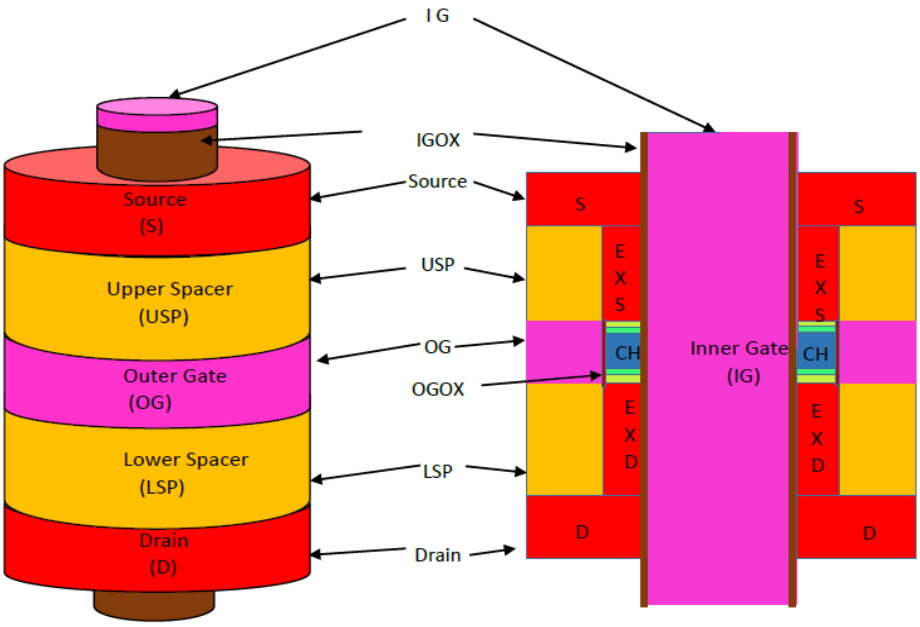


Fig.2.3 SiNT structure showing the components and its 2D cross section

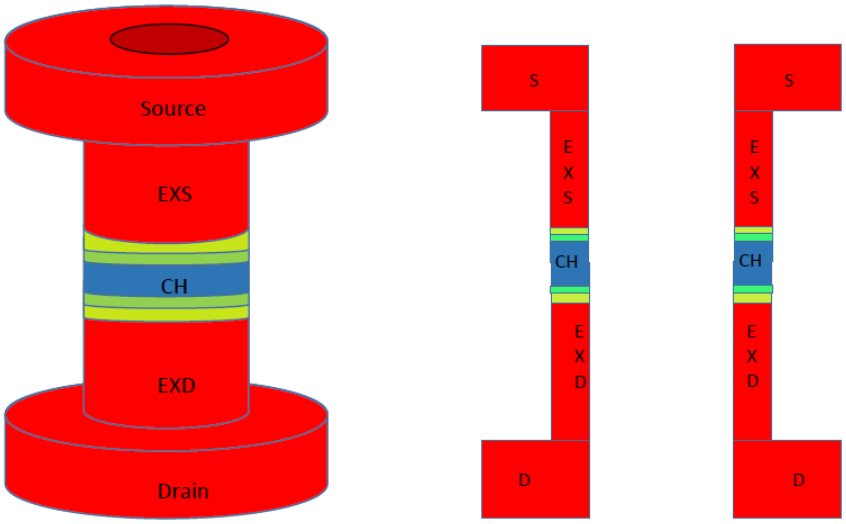


Fig.2.4.The tubular structure of SiNT and its 2D cross section

2.4 Problem Statement

As the title of the project suggests, the 2-D analytical model for surface potential and threshold voltage of SiNTFET has to be developed and to be verified with the device simulation data from ATLAS^{TM}. The capacitance model has to be developed for including the quantum effects for shorter channel lengths.

CHAPTER 3

3 DEVICE SIMULATION

3.1 **ATLAS- a brief overview**

The device simulator used for the work is ATLAS [9]. It is a device simulator frame work. It numerically evaluates the behaviour of a semiconductor device alone or with several other physical parameters. It evaluates the device characteristics by solving the device physics equations that explain the charge distribution and conduction mechanisms. So, the real devices are being presented in the simulator as a virtual device and we analyse their characteristics.

It provides a diverse set of physical models like Fermi Dirac statistics, advanced mobility models etc. It has fully integrated capabilities. It has an interactive run time environment known as DECKBUOLD. For analysis and graphics it has TONYPLOT. It has process simulators known as ATHENA and SSUPREM3. It uses very powerful and sophisticated numerical techniques during the solving and making initial strategies.

The users have to specify the following for the device simulation:

1. Physical structure

2. The models to be used

3. The bias conditions of the device.

The ATLAS inputs and outputs are shown in Fig.3.1

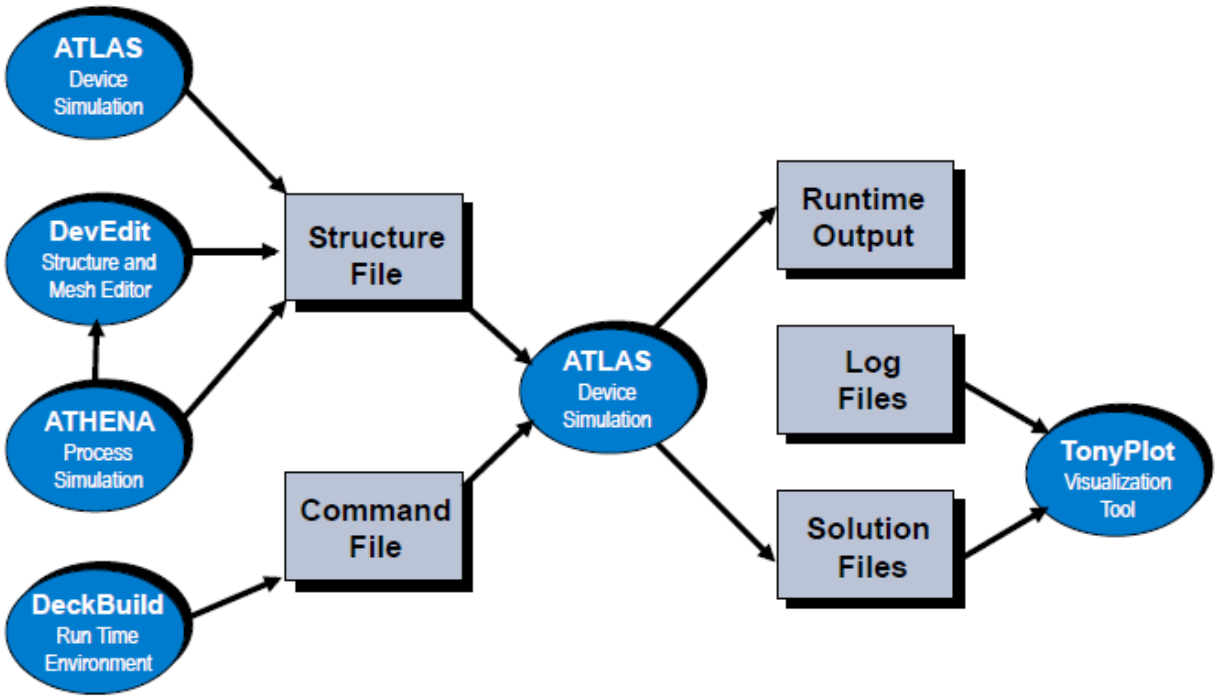


Fig. 3.1 ATLAS inputs and outputs

3.2 ATLAS programming with Illustration

The ATLAS programming is simple and systematic. We start with the command go atlas. We define the mesh whether it is a 2D or 3D with a multiple factor for the mesh. The elements in the input desk can be categorized into five smaller groups.

1. Structure needs to be properly defined. Structure specification includes defining MESH, REGION, ELECTRODE, DOPING of the device. Mesh is the smallest entity where the evaluation of the device equation occurs at every node. Dense meshing causes will result in higher number if nodes, so taking much time for evaluation and greater accuracy. But lightly meshing can give result faster but accuracy decreases. So, the user has to intelligently plan his meshing definitions so as to optimize time and accuracy. The code given below explains this.

```
go atlas
mesh three.d space.mult=4.0 cylindrical

#code for 30nm channel dense mesh

#radius
r.m l=0      spac=0.001
r.m l=0.005   spac=0.001
r.m l=0.007   spac=0.001
r.m l=0.008   spac=0.001
r.m l=0.016   spac=0.001
r.m l=0.017   spac=0.001
r.m l=0.019   spac=0.001
r.m l=0.020   spac=0.001
#angle
a.m l=0.0    spac=3.0
a.m l=360.0  spac=3.0
#z-axis
z.m l=-0.01001    spac=0.001
z.m l=-0.01     spac=0.001
z.m l=-0.002    spac=0.001
z.m l=0.00      spac=0.001
z.m l=0.001    spac=0.001
z.m l=0.019     spac=0.001
z.m l=0.0195    spac=0.001
z.m l=0.029     spac=0.001
z.m l=0.0295      spac=0.001
z.m l=0.030     spac=0.001
z.m l=0.0305       spac=0.001
z.m l=0.0400      spac=0.001
z.m l=0.04001     spac=0.001
#region
region num=1 material=sio2     a.min=0.0   a.max=360.0  r.min=0.005  r.max=0.007  z.min=0.00     z.max=0.03
region num=2 material=silicon   a.min=0.0   a.max=360.0  r.min=0.007  r.max=0.017  z.min=-0.01 z.max=0.00
region num=3 material=silicon    a.min=0.0   a.max=360.0 r.min=0.007  r.max=0.017  z.min=0.00  z.max=0.03
region num=4 material=silicon    a.min=0.0   a.max=360.0 r.min=0.007  r.max=0.017  z.min=0.03  z.max=0.04
region num=5 material=sio2      a.min=0.0   a.max=360.0 r.min=0.017  r.max=0.019  z.min=0.00     z.max=0.03
#electrode
electrode name=source r.min=0.007      r.max=0.017   z.min=-0.01001  z.max=-0.01000
electrode name=gate   r.min=0         r.max=0.005   z.min=0.00   z.max=0.03
electrode name=gate1  r.min=0.019      r.max=0.020   z.min=0.00   z.max=0.03
electrode name=drain  r.min=0.007      r.max=0.017   z.min=0.04   z.max=0.04001
#doping
doping   uniform conc=1e20  n.type direction=z r.min=0.007 r.max=0.017 z.min=-0.01 z.max=0.00
doping   uniform conc=1e20  n.type direction=z r.min=0.007 r.max=0.017 z.min=0.03 z.max=0.04
doping   uniform conc=1e15  p.type direction=z r.min=0.007 r.max=0.017 z.min=0.00 z.max=0.03
```

2. The material models need to be defined. It includes MATERIAL, MODELS,

CONTACTS, INTERFACE definitions.

3. The numerical models that are used in the solving the equations are needed to be specified.

The above steps are illustrated by the code given.

```
#contact
contact  name=source neutral
contact  name=drain
contact  name=gate workfunction=4.7
contact  name=gate1 workfunction=4.7  common=gate
#
models srh conmob fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \
      boltzman print temperature=300
#
mobility  bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200 \
      taun.cvt=0.125 taup.cvt=0.0317 gamn.cvt=2.5 gamp.cvt=2.2 \
      mu0n.cvt=52.2 mu0p.cvt=44.9 mu1n.cvt=43.4 mu1p.cvt=29 mumaxn.cvt=1417 \
      mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 csn.cvt=3.43e+20 \
      csp.cvt=6.1e+20 alphn.cvt=0.68 alphp.cvt=0.71 betan.cvt=2 betap.cvt=2 \
      pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 delp.cvt=2.0546e+14
#
method    newton itlimit=5 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1 \
      tol.time=0.005 dt.min=1e-25
```

4. The solutions are to be specified specifically. The statements used for the solution specification are LOG, SOLVE, LOAD and SAVE.

```
solve init
solve vdrain=.001
solve vgate=.001
solve vdrain=0 vstep=0.05 vfinal=.1 name=drain
log outf=new30_high.log
solve vgate=0  vstep=0.01 vfinal=0.5 name=gate
tonyplot new30_high.log
output     e.field j.electron j.hole j.conduc j.total ex.field ey.field \
      e.mobility h.mobility e.temp h.temp con.band qfn j.disp photogen impact\
save      outf=new30_high.str
```

5. Finally to analyse the results obtained we use the commands EXTRACT, TONYPLOT to obtain the specific value and the device structure respectively.

```
tonyplot3d new30_high.str

extract name="vt"
(xintercept(maxslope(curve(abs(v."gate"),abs(i."dr
ain")))) \
      - abs(ave(v."drain"))/2.0)
quit
```

After completing the input desk we conclude by writing quit.

3.3 Sources of Error in Device Simulation

Sometimes, there might be errors during simulation because of the user or the simulator. The simulator might not know enough physics required for the device or because of its dependence on the empirically fitted models. There might be mesh induced errors as there is an upper limit to the maximum number of nodes permitted by the simulator or inaccurate material or model parameters which are to be handled after the other errors are resolved. User has to make sure that there sufficient mesh density at the high field regions and there are no obtuse triangles in the current path or the high electric field areas. So, user need to take care of all these conditions during simulation.

3.4 The simulation structure of SiNTFET

The 3 D simulation structure is shown in Fig.3.2. The cross section of the device is shown in Fig.3.3. Table 3.1 shows the values of different parameters considered in the device simulation. These values are the same for the device modelling (dealt in the next chapters) unless it is stated the varying parameter.

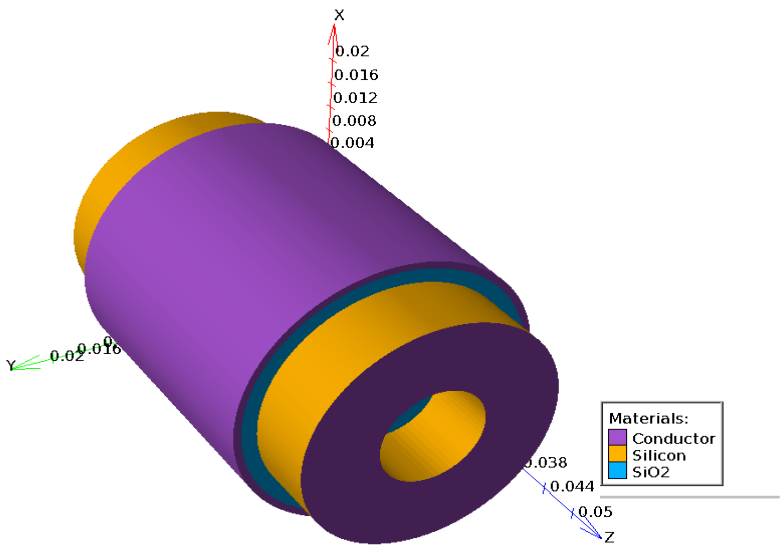


Fig.3.2 The 3D simulation structure of SiNTFET

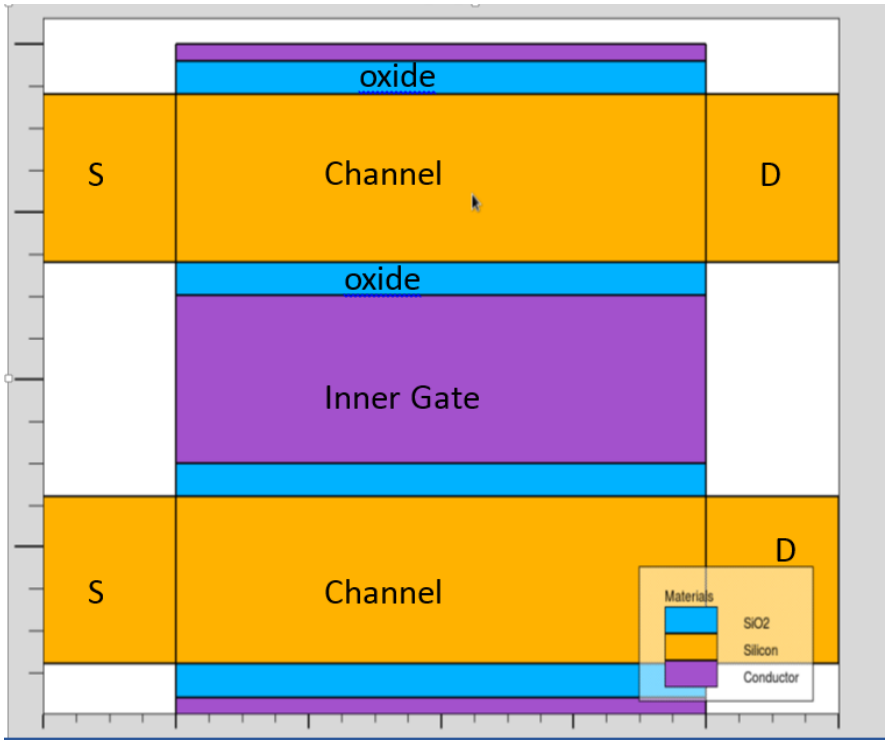


Fig.3.3 The 2D cross section along the channel of SiNTFET

Table 3.1: Device dimensions and parameters used for simulations.

Symbol	Parameter	Value
ε_{ox}	Permittivity of silicon oxide	$3.97 \times 8.85 \times 10^{-14}$ F/m
ε_{si}	Permittivity of silicon	$11.8 \times 8.85 \times 10^{-14}$ F/m
t_{si}	Channel thickness	10nm
t_{ox}	Oxide thickness	2nm
t_c	Core radius	5nm
L	Channel length	30nm
V_t	Thermal voltage	0.0258V
V_G	Gate to Source Voltage	0.1V
V_{DS}	Drain to Source Voltage	0.1V
ϕ_M	Metal Work Function	4.7eV
N_a	Acceptor ion concentration	10^{15} cm^{-3}
N_d	Donor ion concentration	10^{20} cm^{-3}
n_i	Intrinsic ion concentration	1.45×10^{10} cm^{-3}

CHAPTER 4

4 SURFACE POTENTIAL MODELING

Modeling means considering the device physics of the device and analytically modelling the electrical characteristics of the device. Here the modeling results are compared with the simulation results done by the device simulator, ATLAS.

4.1 Surface Potential

The 3 D view of the SiNT FET considered of the model is shown in the Fig 4.1. The 2-D cross sectional view for the device is shown in Fig. 4.2 Here the inner and outer gate oxide thickness are same though the effective thickness won't be. As their physical oxide thickness are same I call it Symmetrical Nanotube FETs. Though the modeling of unsymmetrical device exactly the same procedure as the below it is unnecessary to repeat it. And even modeling symmetrical device will seem like as if a unsymmetrical device is being modeled which is because the of difference in the effective oxide thickness.

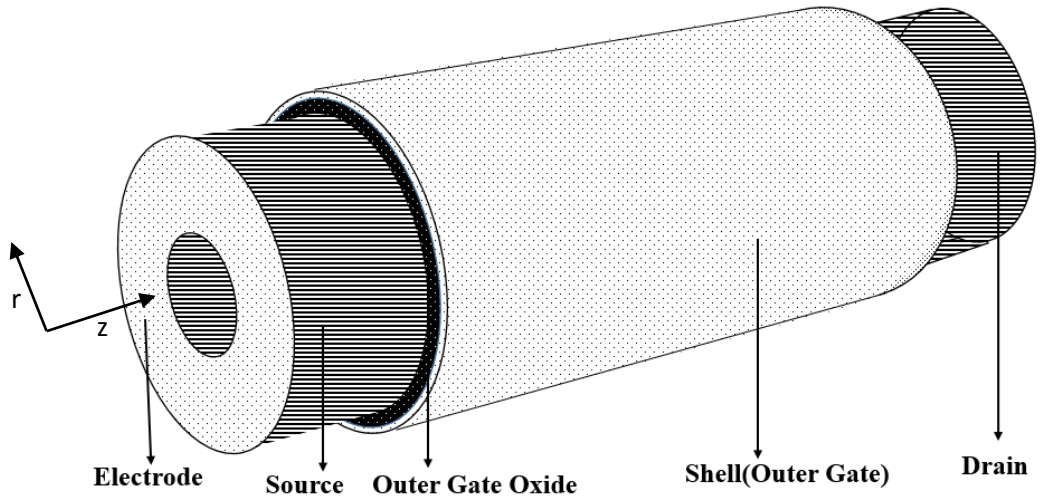


Fig. 4.1 The 3 D structure of SiNT FET

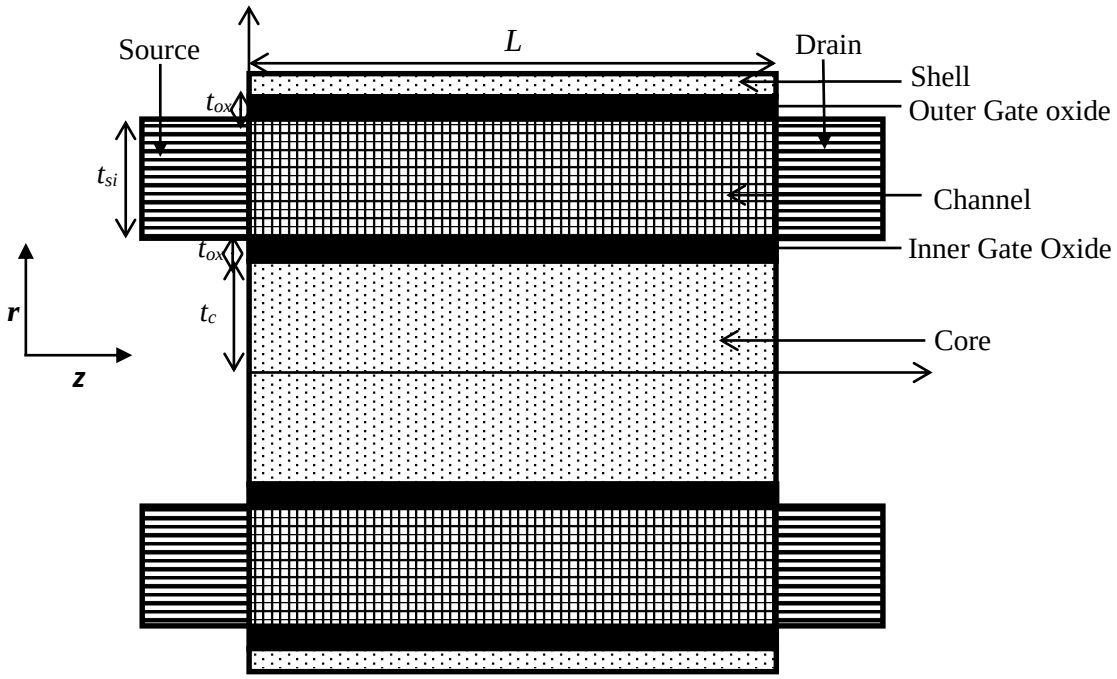


Fig. 4.2 The 2 D cross section view of the device

In the channel region, potential function is obtained by evaluating the solution of the 3-D poisson's equation in cylindrical coordinates given by

$$\frac{1}{r}\frac{d}{dr}\left[r\frac{d}{dr}(\psi(r,z,\theta))\right]+\frac{d^2\psi(r,z,\theta)}{dz^2}+\frac{d^2\psi(r,z,\theta)}{d\theta^2}=\frac{qN_A}{\varepsilon_{Si}}$$

As there is a circular symmetry about z axis, there will be no variation of the surface potential in the θ axis. So, the equation becomes a 2-D and can be rewritten as:

$$\frac{1}{r}\frac{d}{dr}\left[r\frac{d}{dr}(\psi(r,z))\right]+\frac{d^2\psi(r,z)}{dz^2}=\frac{qN_A}{\varepsilon_{Si}} \quad (1)$$

The distribution of the potential is assumed to be quadratic equation. So, the equation is given by:

$$\psi(r,z)=A_0(z)+A_1(z)r+A_2(z)r^2 \quad (2)$$

where $A_0(z)$, $A_1(z)$, $A_2(z)$ are dependent of z only and are evaluated by their boundary conditions.

The device boundary conditions are given by the following equations

The potential inner surface is $\psi(t_c + t_{ox}, z) = \psi_{s1}(z)$ (3)

The $\psi_{s1}(z)$ is the inner surface potential.

The outer surface potential is $\psi(t_c + t_{ox} + t_{si,} z) = \psi_{s2}(z)$ (4)

The $\psi_{s2}(z)$ is the inner surface potential.

As there is continuous electric flux from inner gate oxide to the channel, it is given by

$$\varepsilon_{si} \left. \frac{d\psi(r,z)}{dr} \right|_{r=t_1+t_c} = \varepsilon_{ox} \frac{\psi_{s1}(z) - (V_G - V_{fb})}{t_1} \quad (5)$$

$V_{fb} = \phi_M - (\chi_{si} + \frac{E_g}{2q} + V_t \ln(\frac{N_a}{n_i}))$ is the flat band voltage.

and $$t_1 = t_c \ln\left(1 + \frac{t_{ox1}}{t_c}\right) \text{ [10]} \quad (6)$$

The t_1 is called effective thickness of the oxide. This is can be simply understood by assuming keeping the parallel plate capacitance instead of cylindrical capacitance with a thickness of t_1 .As there is continuous electric flux from outer gate oxide to the channel, it is given by

$$\varepsilon_{si} \left. \frac{d\psi(r,z)}{dr} \right|_{r=t_{ox}+t_c+t_{si}} = \varepsilon_{ox} \frac{-\psi_{s1}(z) + (V_G - V_{fb})}{t_2} \quad (7)$$

and $t_2 = (t_c + t_{ox} + t_{si}) \ln\left(1 + \frac{t_{ox}}{t_c + t_{ox} + t_{si}}\right)$ (8)

The Surface potential at the source is given by

$$\psi(r,0) = V_{bi} \quad (9)$$

where the built in voltage is V_{bi}

$V_{bi} = V_t \log\left(\frac{N_d N_a}{n_i^2}\right)$ and V_t is the thermal voltage. We assume the temperature is 300K.

The Surface potential at drain is given by

$$\psi(r,L) = V_{bi} + V_{DS} \quad (10)$$

The boundary conditions listed above in the equations (3), (4), (5) and (7) give the values of the coefficients of the quadratic equation.

$$A_0(z) = \psi_{s1}\left[1 - \varepsilon_r \frac{(t_1 + t_c)(2t_{si} + t_1 + t_c)}{2t_1 t_{si}}\right] - \psi_{s2}\left[\varepsilon_r \frac{(t_1 + t_c)^2}{2t_2 t_{si}}\right] + \varepsilon_r\left[\frac{(V_G - V_{fb})(t_1 + t_c)(2t_{si}t_2 + t_1 t_2 + t_c t_2 + t_1^2 + t_c t_1)}{2t_1 t_2 t_{si}}\right] \quad (11)$$

$$A_0(z) = -\psi_{s1}\left[\varepsilon_r \frac{(t_1 + t_c + t_{si})^2}{2t_1 t_{si}}\right] + \psi_{s2}\left[1 - \varepsilon_r \frac{(t_1 + t_c + t_{si})(t_1 + t_c - t_{si})}{2t_2 t_{si}}\right] + \varepsilon_r\left[\frac{(V_G - V_{fb})(t_1 + t_c + t_{si})(t_{si}t_2 + t_1 t_2 + t_c t_2 + t_1^2 + t_c t_1 - t_1 t_{si})}{2t_1 t_2 t_{si}}\right] \quad (12)$$

$$A_1(z) = -\frac{\varepsilon_r}{t_{si}}\left(\frac{(t_1 + t_c + t_{si})(V_G - V_{fb} - \psi_{s1})}{t_1} + \frac{(t_1 + t_c)(V_G - V_{fb} - \psi_{s2})}{t_2}\right) \quad (13)$$

$$A_2(z) = \frac{\varepsilon_r}{2t_{si}}\left(\frac{(V_G - V_{fb} - \psi_{s1})}{t_1} + \frac{(V_G - V_{fb} - \psi_{s2})}{t_2}\right) \quad (14)$$

The equations (11) and(12) are the representation of the same coefficient in two different ways. So, this gives the relation of the $\psi_1(z)$ and $\psi_{s2}(z)$.

$$\psi_2(z) = \gamma\psi_1(z) + \frac{\varepsilon_r t_{si}(t_1 - t_2)(V_G - V_{fb})}{2t_1 t_2\left[1 + \frac{\varepsilon_r t_{si}}{2t_2}\right]} \tag{15}$$

Where $\gamma = \frac{\left[1 + \frac{\varepsilon_r t_{si}}{2t_1}\right]}{\left[1 + \frac{\varepsilon_r t_{si}}{2t_2}\right]}$ and $\varepsilon_r = \frac{\varepsilon_{ox}}{\varepsilon_{si}}$

By equations (11), (13), (14),(15) obtained above, the distribution of potential in the channel is :

$$\psi(r,z) = \psi_{s1}(z)[1 - \varepsilon_r(a - br + cr^2)] + (V_G - V_{fb})\varepsilon_r[n - pr + qr^2] \tag{16}$$

Where,

$$a = \left(\frac{(t_1 + t_c)(2t_{si} + t_1 + t_c)}{2t_1 t_{si}} + \frac{\gamma(t_1 + t_c)^2}{2t_2 t_{si}}\right) \tag{17}$$

$$b = \frac{(t_{si} + t_1 + t_c)}{t_1 t_{si}} + \gamma\frac{(t_1 + t_c)}{t_2 t_{si}} \tag{18}$$

$$c = \frac{1}{2t_{si}t_1} + \frac{\gamma}{2t_{si}t_2} \tag{19}$$

$$n = \left[\frac{(t_1 + t_c)(2t_{si}t_2 + t_1t_2 + t_ct_2 + t_1^{\,2} + t_ct_1)}{2t_1t_2t_{si}}\right] - \left[\varepsilon_r \frac{t_{si}[t_1 - t_2](t_1 + t_2)^2}{4t_1t_2\left[1 + \frac{\varepsilon_r t_{si}}{2t_2}\right]t_2t_{si}}\right] \tag{20}$$

$$p = \frac{t_{si} + t_1 + t_c}{t_1 t_{si}} + \frac{t_1 + t_c}{t_2 t_{si}} - \left[\varepsilon_r \frac{t_{si}[t_1 - t_2](t_1 + t_c)}{2t_1 t_2 \left[1 + \frac{\varepsilon_r t_{si}}{2t_2} \right] t_2 t_{si}} \right] \tag{21}$$

$$q = \frac{t_1 + t_2}{2t_{si} t_1 t_2} - \left[\varepsilon_r \frac{t_{si}[t_1 - t_2]}{4t_1 t_2 \left[1 + \frac{\varepsilon_r t_{si}}{2t_2} \right] t_2 t_{si}} \right] \tag{22}$$

As poisson equation is applicable everywhere in the channel. So finding at $r = t_c + t_1$ gives:

$$\frac{d^2 \psi_{s1}(z)}{dz^2} - \psi_{s1}(z) \frac{Y_1}{X_1} = \frac{qN_A}{\varepsilon_{si}} + (V_G - V_{fb}) \frac{Z_1}{X_1} \tag{23}$$

where

$$X_1 = 1 - \varepsilon_r [a - b(t_1 + t_c) + (t_1 + t_c)^2] \tag{24}$$

$$Y_1 = \varepsilon_r \frac{b}{t_1 + t_c} - 4kc \tag{25}$$

$$Z_1 = \varepsilon_r \frac{p}{t_1 + t_c} - 4kq \tag{26}$$

The equation (23) is non-homogenous 2nd order partial differential equation.For simplification and writing in the typical form

$$\frac{d^2 \psi_{s1}(z)}{dz^2} - \alpha_1 \psi_{s1}(z) = \beta_1 \tag{27}$$

Where $\alpha_1 = \frac{Y_1}{X_1}$ and $\beta_1 = \frac{qN_A}{\varepsilon_{si}} + (V_G - V_{fb}) \frac{Z_1}{X_1}$

The solution of this partial differential equation is given as:

$$\psi_{s1}(z) = C_{11}e^{\sqrt{\alpha_1}z} + C_{12}e^{-\sqrt{\alpha_1}z} - \frac{\beta_1}{\alpha_1} \tag{28}$$

The constants C_{11} and C_{12} are to be evaluated by solving the boundary conditions (9) and (10) which show the end potential at drain and source. So, evaluating gives:

$$C_{11} = \frac{-(V_{bi} - \sigma_1)e^{-\sqrt{\alpha_1}L} + (V_{DS} + V_{bi} - \sigma_1)}{2\sinh(\sqrt{\alpha_1}L)} \tag{29}$$

$$C_{12} = \frac{(V_{bi} - \sigma_1)e^{\sqrt{\alpha_1}L} - (V_{DS} + V_{bi} - \sigma_1)}{2\sinh(\sqrt{\alpha_1}L)} \tag{30}$$

Where $\sigma_1 = -\frac{\beta_1}{\alpha_1}$

Substituting the equations (29) and (30) in (28) gives the expression for inner surface potential, given as

$$\psi_{s1}(z) = \frac{(V_{bi} - \sigma_1)\sinh(\sqrt{\alpha_1}(L-z) + (V_{DS} + V_{bi} - \sigma_1)\sinh(\sqrt{\alpha_1}z)}{\sinh(\sqrt{\alpha_1}L)} \tag{31}$$

In the same way as above, solving the poisson's equation at $r = t_c + t_1 + t_{si}$ gives:

$$\frac{d^2\psi_{s2}(z)}{dz^2} - \psi_{s2}(z)\frac{Y_2}{X_2} = \frac{qN_A}{\varepsilon_{si}} + (V_G - V_{fb})\frac{Z_2}{X_2} \tag{32}$$

Where,

$$X_2 = \frac{X_1}{\gamma}$$

$$Y_2 = \frac{Y_1}{\gamma}$$

$$Z_2 = Z_1 - \frac{\varepsilon_r}{2\gamma} \frac{t_{si}[t_1 - t_2]Y_1}{t_1 t_2 \left[1 + \frac{\varepsilon_r t_{si}}{2t_2}\right]}$$

The equation (32) is can be typically be expressed as

$$\frac{d^2\psi_{s2}(z)}{dz^2} - \alpha_2 \psi_{s2}(z) = \beta_2 \tag{33}$$

Where $\alpha_2 = \frac{Y_2}{X_2}$

$$\beta_2 = \frac{qN_A}{\varepsilon_{si}} + (V_G - V_{fb})\frac{Z_2}{X_2}$$

$$\psi_{s2}(z) = C_{21}e^{\sqrt{\alpha_2}z} + C_{22}e^{-\sqrt{\alpha_2}z} - \frac{\beta_2}{\alpha_2} \tag{34}$$

The constants C_{21} and C_{22} are to be evaluated by solving the boundary conditions (9) and (10) which show the end potential at drain and source. So, evaluating gives:

$$C_{21} = \frac{-(V_{bi} - \sigma_2)e^{-\sqrt{\alpha_2}L} + (V_{DS} + V_{bi} - \sigma_2)}{2\sinh(\sqrt{\alpha_2}L)} \tag{35}$$

$$C_{22} = \frac{(V_{bi} - \sigma_2)e^{\sqrt{\alpha_2}L} - (V_{DS} + V_{bi} - \sigma_2)}{2\sinh(\sqrt{\alpha_2}L)} \tag{36}$$

where $\sigma_2 = -\frac{\beta_2}{\alpha_2}$.

Substituting the equations (35) and (36) in (34) gives the expression for outer surface potential, given as

$$\psi_{s2}(z) = \frac{(V_{bi} - \sigma_2)\sinh(\sqrt{\alpha_2}(L - z) + (V_{DS} + V_{bi} - \sigma_2)\sinh(\sqrt{\alpha_2}z)}{\sinh(\sqrt{\alpha_2}L)} \tag{37}$$

So, the inner and outer surface potential functions are evaluated and are verified by the simulation results.

4.2 Results and Discussion

The mathematical model values and the simulation values are plotted in the graph for comparison. Fig. 4.3 shows the inner and outer channel potential.

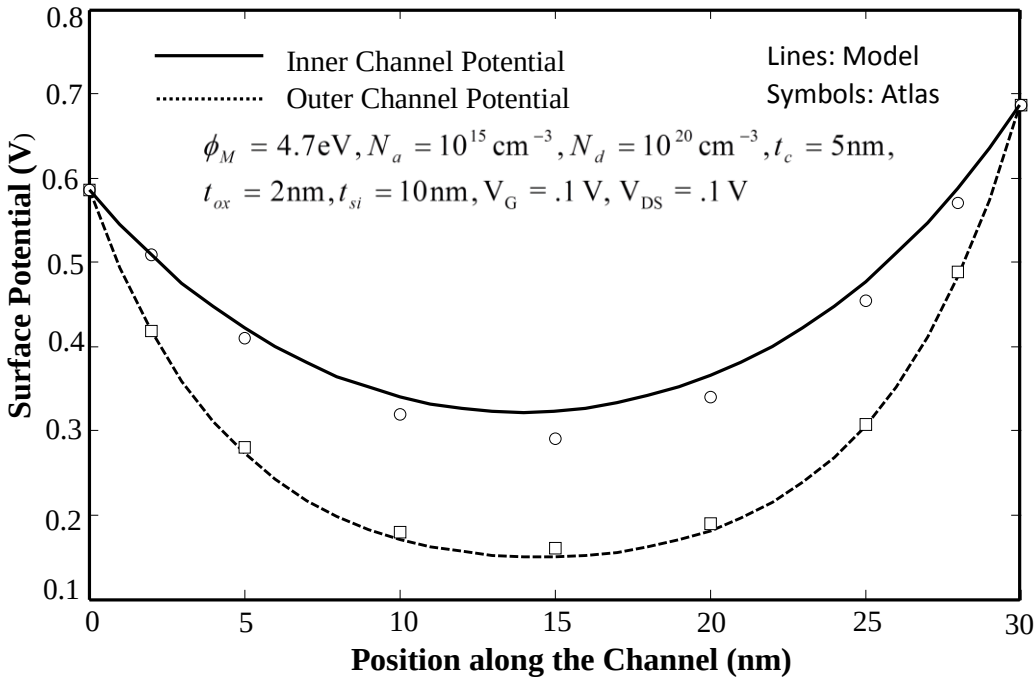


Fig. 4.3 Comparison of the inner and outer channel potentials

It is noted that the inner surface potential is higher than the outer surface for the given conditions. So, this has less barrier height than the outer surface and will determine the threshold voltage of the device and will be discussed in the next chapter.

The Fig. 4.4 shows the variation in the potential distribution in the channel by altering the gate and drain voltages.

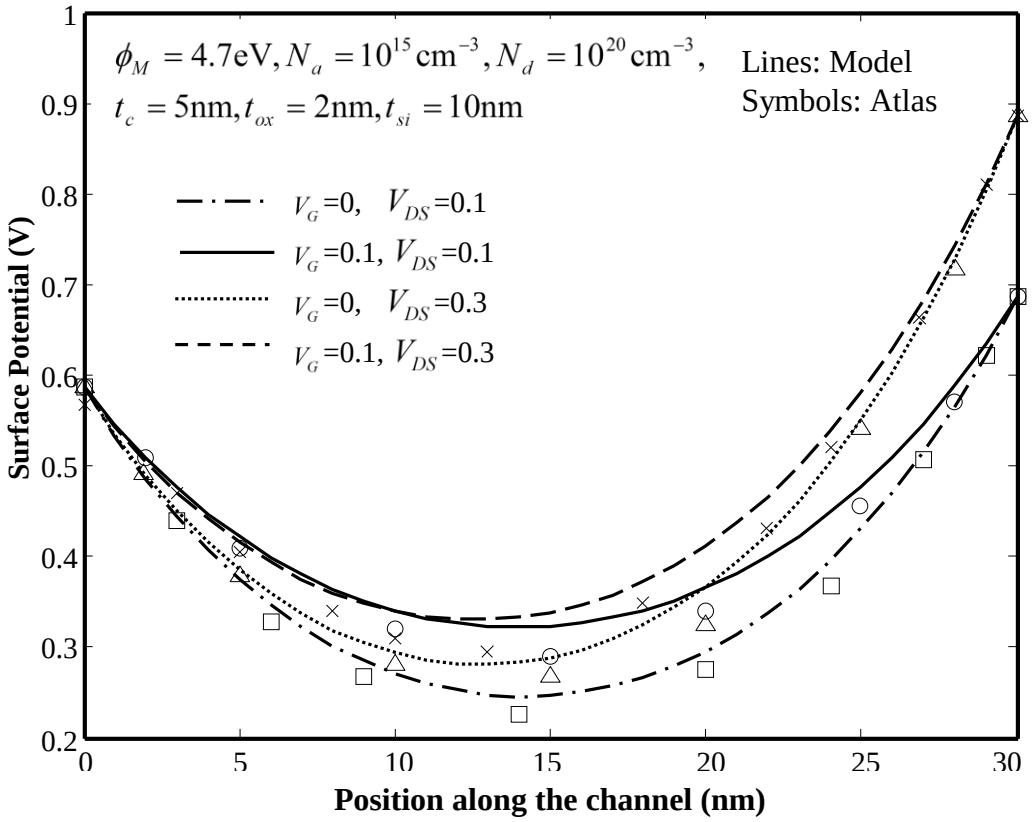


Fig.4.4 Variation of potential distribution of inner surface for variation in the gate and drain voltages.

From Fig.4.4, it is observed that minimum surface potential decreases with lowering of the gate voltage. This increases the source barrier height which causes to increment in the threshold voltage of the nanotube. The increase in drain voltage from .1V to .3V has increased the minimum surface potential resulting in the decrease of the barrier height and also decreasing the threshold voltage.

CHAPTER 5

5 THRESHOLD VOLTAGE MODELING

This chapter is a continuation of the previous chapter. Instead of having one lengthy chapter, it is divided into two to seem the things simpler. In the last chapter the surface potential of the device had been modeled. It was observed that the inner surface potential of the device dominates the outer surface potential in determining the threshold voltage of the device.

5.1 Threshold Voltage

The procedure for finding threshold voltage includes calculation of sub threshold current found at the virtual cathode potential. The minimum surface potential, $z_{\min}$ has to be evaluated .It is found by slope of the inner channel potential function is zero.

$$\frac{d\psi_{s1}(z)}{dz} = 0 \tag{38}$$

So, evaluating gives the above equation gives

$$z_{\min} = \frac{\ln[\frac{C_{12}}{C_{11}}]}{2\sqrt{\alpha}_1} \tag{39}$$

Replacing the value of $z_{\min}$ in (31), results in

$$\psi_{s1\min} = 2\sqrt{C_{11}C_{12}} + \sigma_1 \tag{40}$$

Replacing the above in the original potential distribution function (16)

$$\psi_{vc}(r) = [2\sqrt{C_{11}C_{12}} + \sigma_1][1 - \varepsilon_r(a - br + cr^2)] + (V_G - V_{fb})\varepsilon_r[n - pr + qr^2] \tag{41}$$

In a device, due to the applied gate voltage, then inversion charge will accumulate. The total inversion charge in the channel Q_{inv} is expressed as-

$$Q_{inv} = q\frac{n_i^{\,2}}{N_a}\int_{z=0}^{L}\int_{r=t_c+t_{ox}}^{t_c+t_{ox}+t_{si}} \exp\left[\frac{\psi_{vc}(r)}{V_t}\right] 2\pi r\,dr\,dz \tag{42}$$

Finding the integral of the above equation will be too lengthy and complex because integrating this give the error functions and imaginary function and make the modelling complex. This is generally escaped in MOS device modeling because of its non-analytical characteristics .The doping in the channel was willing made lighter to avoid random dopant fluctuations and this is similar to the DGMOSFET with undoped channel. So, the we consider effective path of conduction [10].The effective conductive path can be written as [11-13]:

$$r = r_{eff} = t_c + t_{ox} + \left(\frac{t_{si}}{4}\right)_{eff} \tag{43}$$

And $\left(\frac{t_{si}}{4}\right)_{eff}$ is the effective distance of the conductive path from the inner gate oxide in this cylindrical device which is evaluated similar to equation (6).

So, this gives the total inversion charge at virtual cathode is calculated as:

$$Q_{inv} = q\frac{n_i^{\,2}}{N_a}\int_{z=0}^{L}\int_{r=t_c+t_{ox}}^{t_c+t_{ox}+t_{si}} \exp\left[\frac{\psi_{vc}(r)\big|_{r=r_{eff}}}{V_t}\right] 2\pi r\,dr\,dz \tag{44}$$

The evaluation of this integral gives the below equation:

$$\psi_{vc}(r)\big|_{r=t_c+t_{ox}+\frac{t_{si}}{4}} = V_t \ln\left[\frac{Q_{inv}N_a}{\pi q n_i^{\,2} t_{si}(2t_c+2t_{ox}+t_{si})L}\right] \tag{45}$$

The threshold voltage value for long channel (100nm) is obtained from simulation and is equated to modeled value by varying the Q_{inv}.This value of Q_{inv} becomes the Q_{TH} of the device. So, using equations (41) and (45) the quadratic expression for $V_G - V_{fb}$ is obtained. At, threshold condition, $V_G = V_{TH}$, threshold voltage of the device. So, substituting in the equation and solving for it gives a quadratic equation:

$$\left(k_1 {k_2}^2 - {k_4}^2\right)\left(V_{TH} - V_{fb}\right)^2 + \left({k_1}^2 k_6 + 2k_7 k_2\right)\left(V_{TH} - V_{fb}\right) + \left({k_1}^2 k_8 - {k_7}^2\right) = 0 \tag{46}$$

$$k_1 = \frac{1 - \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{si} t_1}\left[\left(t_c + t_1\right)\left(t_c + t_1 + t_c\right) - \left(2t_c + 2t_1 + t_{si}\right) r_{eff} + {r_{eff}}^2\right]}{\sinh(\sqrt{\alpha_1} L)} \tag{47}$$

$$k_2 = 2\left(\frac{\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}}\left[3 - \frac{t_c}{t_c + 2t_1 + t_{si}}\right]}{\alpha_1}\right)^2 \left(\cosh(\sqrt{\alpha_1} L) - 1\right) \tag{48}$$

$$k_3 = 1 - \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{si} t_1}\left[\left(t_c + t_1\right)\left(t_c + t_1 + t_c\right) - \left(2t_c + 2t_1 + t_{si}\right) r_{eff} + {r_{eff}}^2\right] \tag{49}$$

$$k_4 = 1 + k_3\left[\frac{\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}}\left[3 - \frac{t_c}{t_c + 2t_1 + t_{si}}\right]}{\alpha_1} - 1\right] \tag{50}$$

$$k_5 = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}}\left[3 - \frac{t_c}{t_c + 2t_1 + t_{si}}\right] \tag{51}$$

$$k_6 = -\left(\frac{4qN_a k_5}{\varepsilon_{si} {\alpha_1}^2} + \frac{2k_5\left(2V_{bi} + V_{DS}\right)}{\alpha_1}\right)\left(\cosh(\sqrt{\alpha_1} L) - 1\right) \tag{52}$$

$$k_7 = V_t \ln\left[\frac{Q_{inv}N_a}{\pi q n_i^2 t_{si}(2t_c+2t_{ox}+t_{si})L}\right] + \frac{qN_a k_3}{\varepsilon_{si}\alpha_1} \tag{53}$$

$$k_8 = \left[\left(2V_{bi}^2+2V_{bi}V_{DS}\right)\left(\cosh(\sqrt{\alpha_1}L)-1\right)-V_{DS}^2\right] + \left(2V_{bi}+V_{DS}\right)\frac{qN_a}{\varepsilon_{si}\alpha_1}\left[\cosh(\sqrt{\alpha_1}L)-1\right]$$

(54)

Solving the quadratic polynomial of Eq. (46) gives V_{TH} represented by:

$$V_{TH} = V_{fb} + \left(\frac{-\left(k_1^2k_6+2k_7k_2\right)+\sqrt{\left(k_1^2k_6+2k_7k_2\right)^2-4\left(k_1k_2^2-k_4^2\right)\left(k_1^2k_8-k_7^2\right)}}{2\left(k_1k_2^2-k_4^2\right)}\right) \tag{55}$$

5.2 Results and Discussion

In this section, the results of surface potential and threshold voltage as a function of channel length are obtained from theoretical models and are compared with the numerical simulation results performed in ATLAS™. The threshold voltage is extracted from constant current method. In constant current method, the threshold voltage is defined as the value of gate voltage at which drain current equal $I_d = \frac{W}{L}\times 10^{-7}$ A [14]. Here, L is the length of the device and W is the effective width of the channel which is evaluated by:

$$W = 2\pi R_{eff} \tag{56}$$

$$R_{eff} = \frac{\int_{R_1}^{R_2}\left(2\pi dr\right)r}{\pi\left(R_2^2-R_1^2\right)} \tag{57}$$

$$R_1 = t_c + t_{ox}$$

$$R_2 = t_c + t_{ox} + t_{si}$$

Fig.5.1 shows the variation of threshold voltage as a function of the channel length which is in good agreement with the simulation results for the long channels. It is observed that threshold voltage roll off for SiNTFETs is very less compared to other semiconductor devices. It shows the better controllabity of the charge in the device. The model values slightly differ from from the simulation values for short channel lengths of less than 30nm because we have not considered the quantum effects which are vital in those channel lengths.

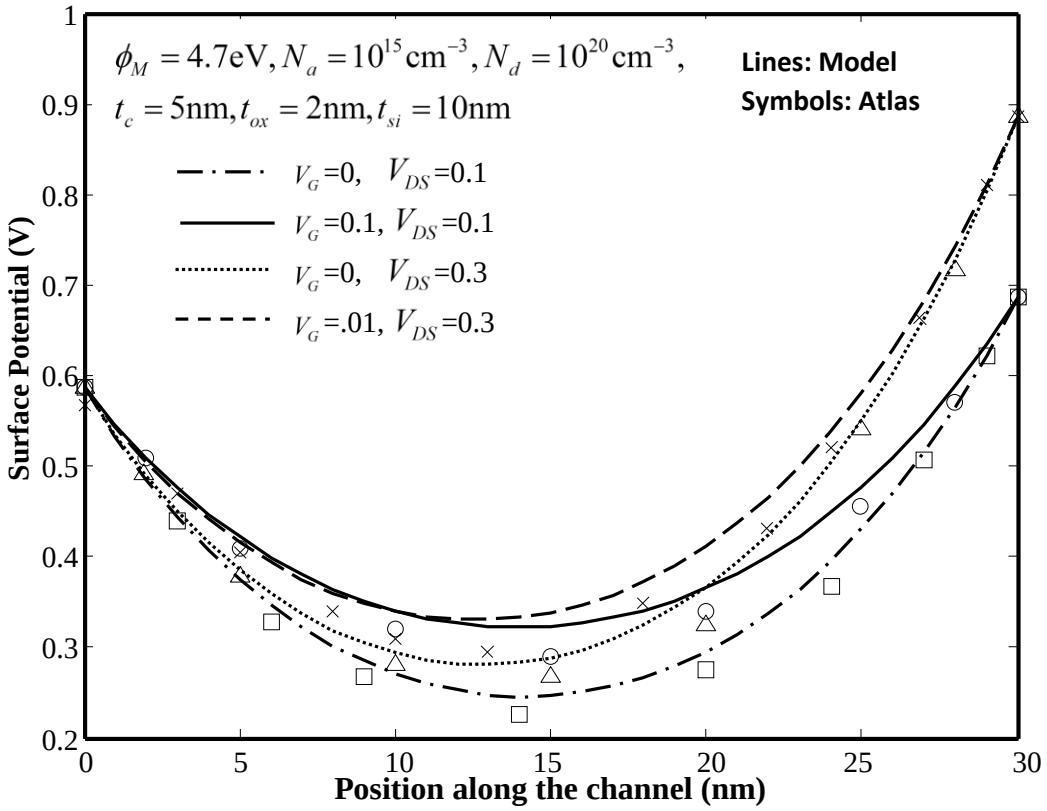


Fig.5.1 Inner channel surface potential along the channel length for varying gate and drain voltages

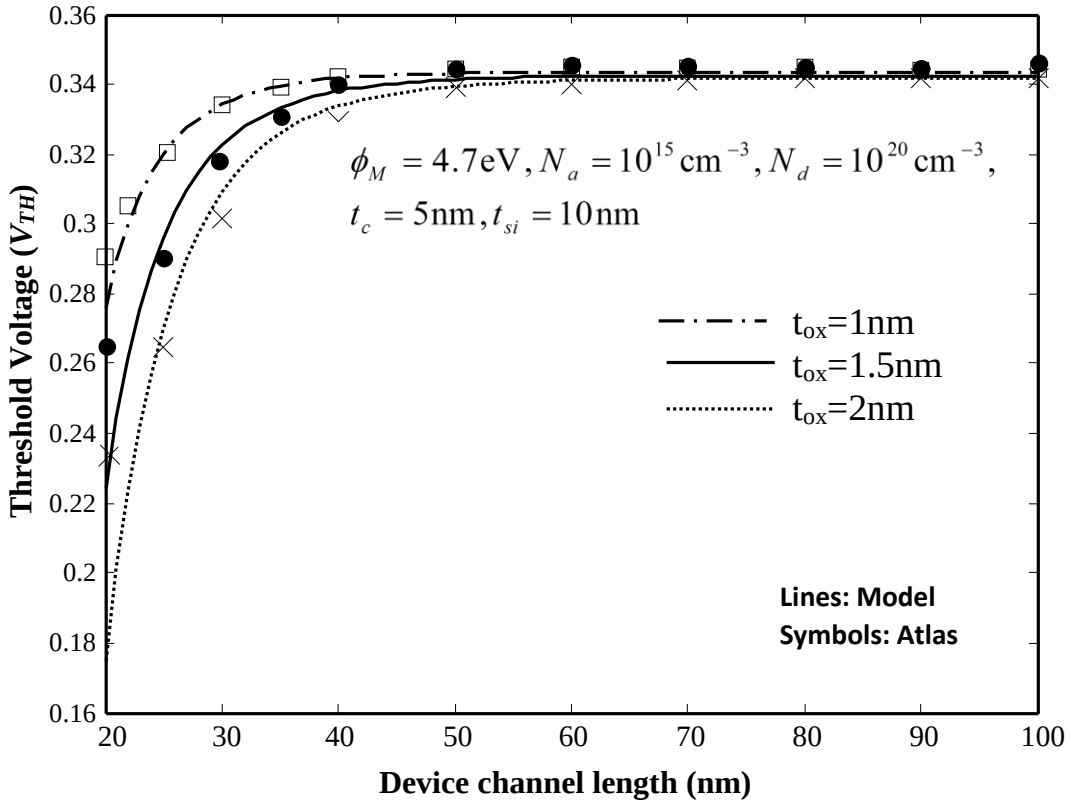


Fig.5.2 Threshold voltage versus channel length for varying oxide thickness.

Fig.5.2 plots threshold voltage as a function of channel length for different oxide thickness. As the oxide thickness decreases the threshold voltage of the device increases. It is noted that as oxide thickness decreases SCE also decreases as gate can more effectively control the charge in the channel. As the oxide thickness of the device increases the roll of the threshold voltage increases. This is because the more thick oxide makes the loss of control by the gate in shorter channel lengths and conduction happens by the external applied drain voltages and so for lower values of gate voltage there is conduction and DIBL is prominent.

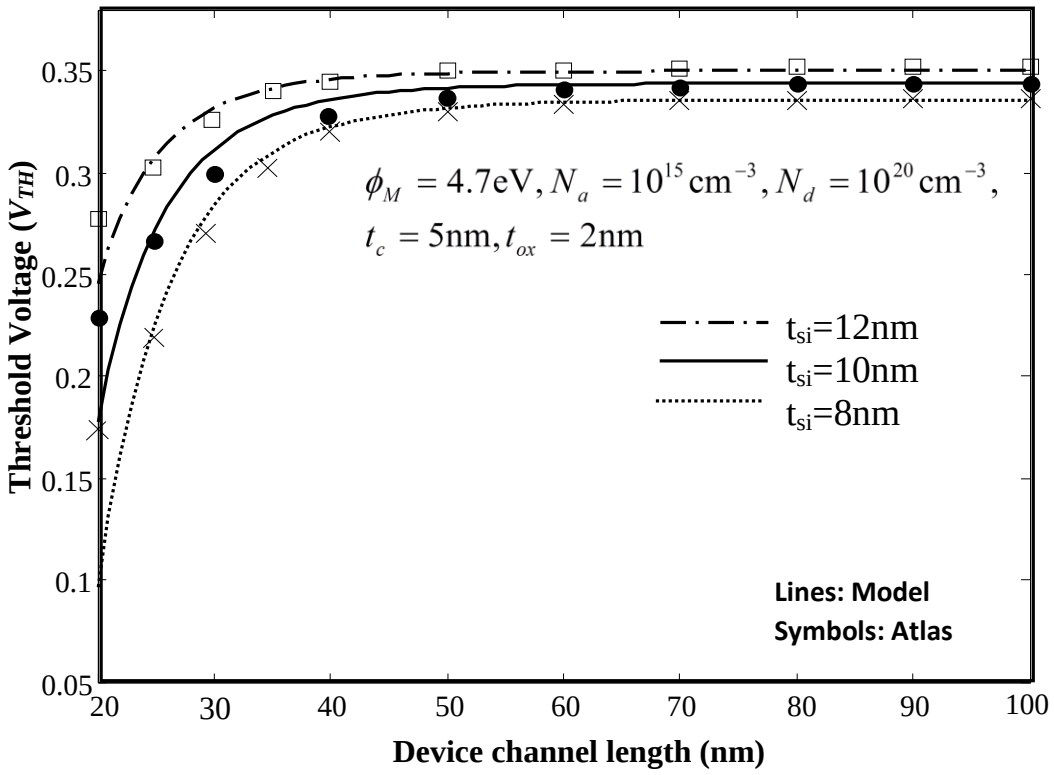


Fig.5.3 Threshold voltage versus channel length for varying silicon thickness.

Fig.5.3 plots threshold voltage as a function of channel length for different channel thickness. As the channel thickness increases, the threshold voltage decreases because there will be more inversion charge to turn on the device. The more the inversion charge the overall current in the tube increases. So, lesser gate voltage can trigger the conduction in the channel resulting in the decrease of the threshold voltage. [15].

Fig. 5.4 plots threshold voltage verses channel length for different core diameters. As the diameter increases threshold voltage decreases. For the doping concentrations this can also be interpreted as greater the diameter of the device, the control of gate per unit area increases. So, as the gate control increases, there is greater electrostatic controllability in the device resulting in decreasing the threshold voltage.

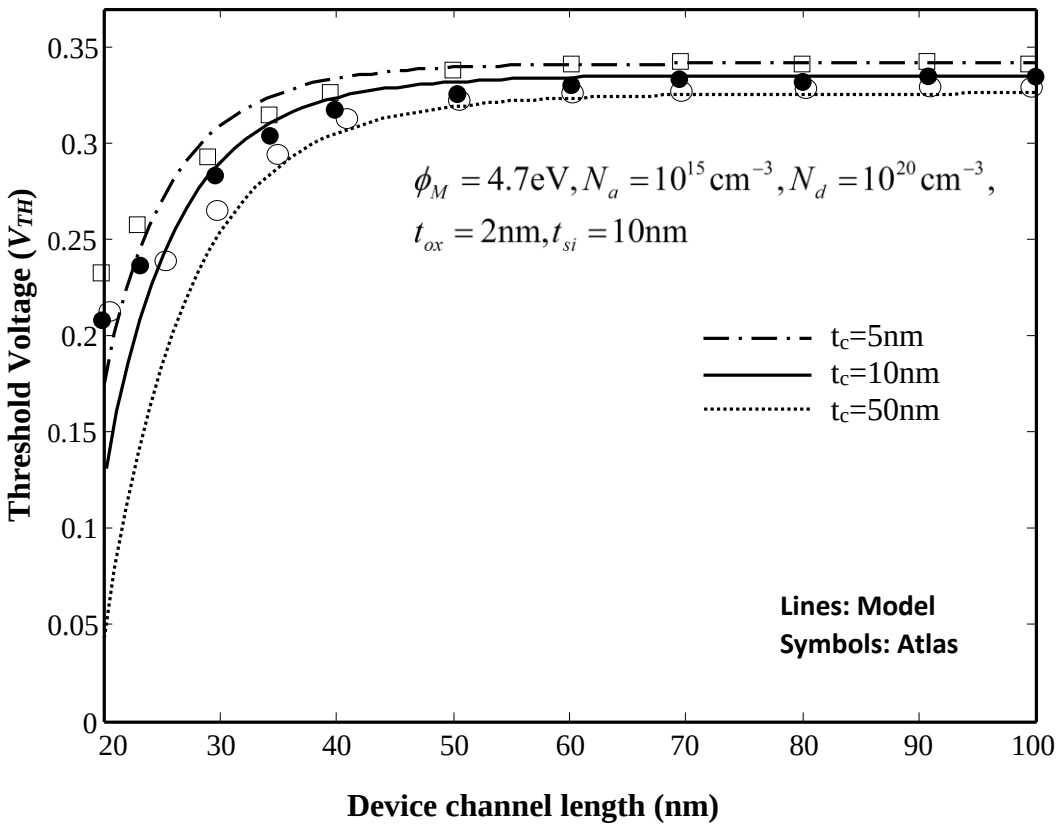


Fig.5.4 Threshold Voltage verses channel length for varying core thickness

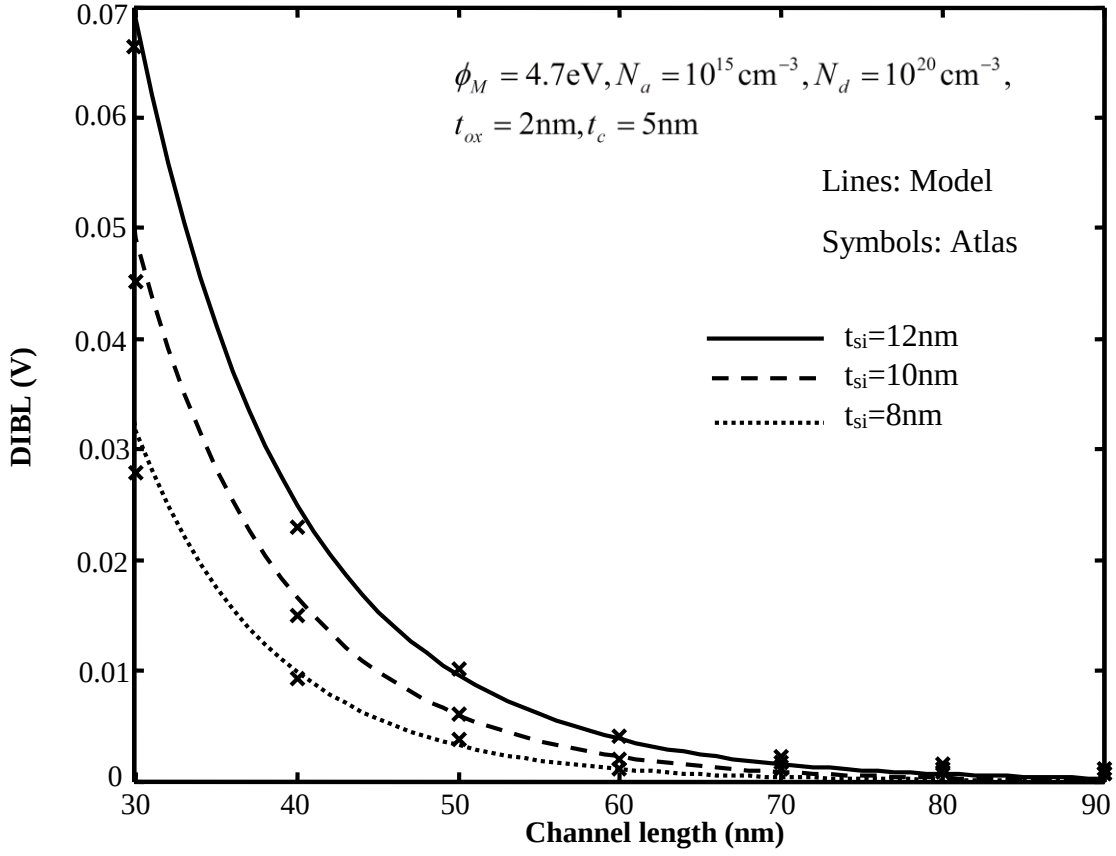


Fig.5.5 Threshold Voltage verses DIBL for varying channel thickness

Fig.5.5 explains the DIBL characteristics of the device by the variation tube thickness of the devices. The DIBL is defined as-

$$DIBL = -\frac{V_{TH}^{high} - V_{TH}^{low}}{V_{DS}^{high} - V_{DS}^{low}}$$

Here the higher drain voltage at which the threshold voltage is evaluated is 1.1V and lower is 0.1V. The drain voltage of 1.1V is too high during the modeling for the short channel devices without including quantum effects. So, this results in the significant deviation of model value from the simulation for shorter channel lengths. But, it is to be observed that the DIBL values are too low where compared with other MOS devices at those channel lengths which credited for its enhanced controllability of charge in the device.

CHAPTER 6

6 MODELING FRINGE CAPACITANCES

In this chapter I present you my idea of modeling the cylindrical capacitances. Modeling capacitances in the cylindrical devices has to be done in cylindrical coordinates. For device like GAA nanowire FETs, SiNTFETs modelling capacitances will help to understand the devices in short channel lengths. Here I attempted to model the fringe capacitances of SiNTFETs. Before going into modeling the cylindrical capacitances of nanotube we will see the different methods used in the modelling different types of capacitances in the model. In order to decrease the fringe effects high-k dielectrics and spacers are used which are taken in consideration during modeling.

6.1 Methods Used

For understanding the modeling the capacitance in cylindrical coordinates, one needs to understand modelling fringe capacitances in 2D Cartesian coordinates. For that the reference papers are-[16-18]. Understanding these papers completely and how the model is developed will be helpful for modeling the device. The fringe capacitance is divided into 3 components and are modeled. The Fig.6.1 shows the convention of capacitances taken by Suzuki[16] and Fig. 6.2 shows the convention of Jagadesh Kumar[17] are followed in this thesis . The bottom Capacitance is modeled by using Jagadesh kumar model [17] top Capacitance by Suzuki model [16] and side capacitance by Kamachouchi model by [18].

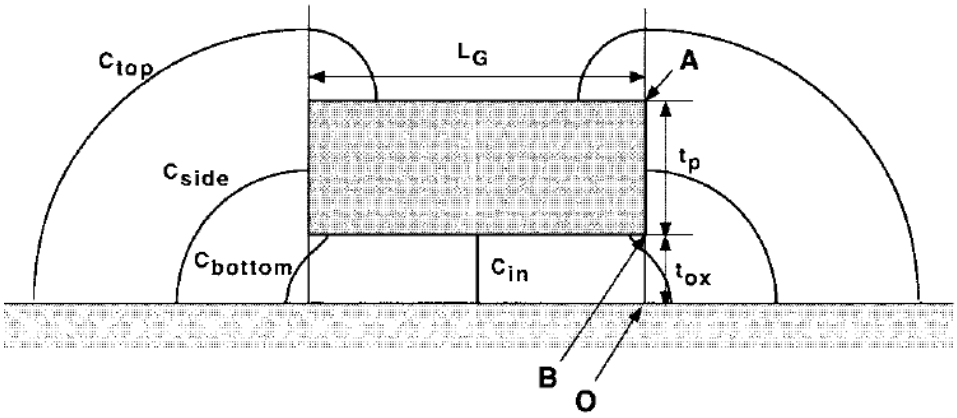


Fig.6.1 Various Capacitance components.

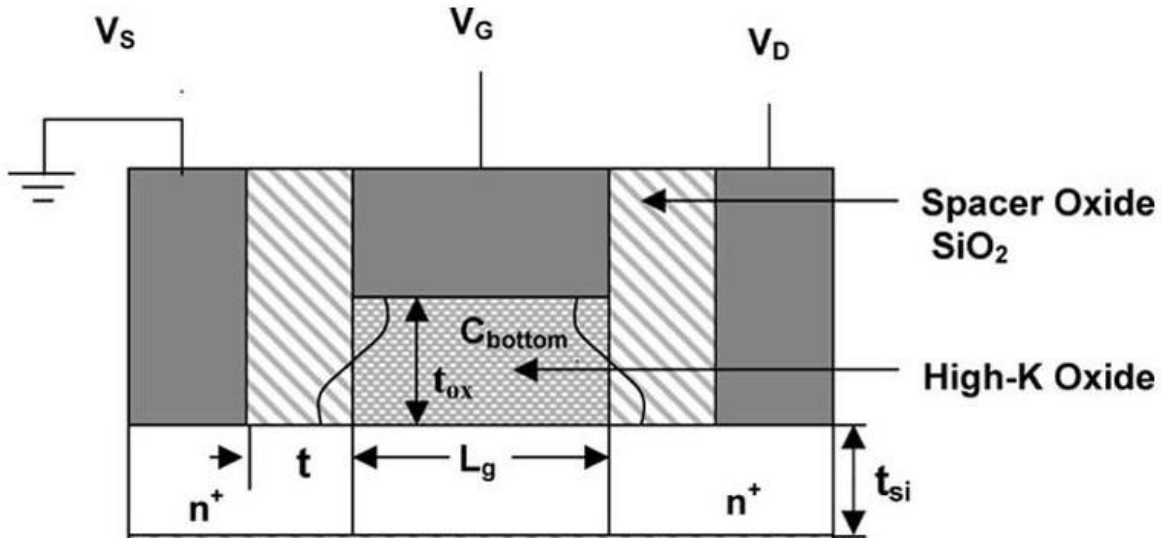


Fig.6.2 Cross sectional view including a spacer

6.2 Modeling capacitances in SiNTFET

6.2.1 Idea of modeling

As we have found the equivalent thickness of the oxide in cylindrical coordinates for writing the electrical flux equations, similarly assume that the parallel place capacitance of same length of same length of the cylindrical capacitance is replacing in such a way that total charge in the system would not change. The concentric cylinders form the capacitance and we get a relation between the distance between the plates and ratio of the radius of the cylindrical capacitance.

In the method to find the threshold voltage of the device by inversion charge method, we need to find the total charge obtained by the fringe capacitances.

6.2.2 Modeling Results

So, evaluating the capacitance values similar to the reference papers given above and making necessary transformation gives the values of different capacitances and symbols have their own meaning as convention.

$$C_{bottom} = \frac{b-a}{\ln\frac{b}{a}}(0.613)\varepsilon_{eff}$$

$$C_{side} = \frac{b-a}{\ln\frac{b}{a}}\varepsilon_{eff}\ \ln(a^1)$$

$$C_{top} = \frac{b-a}{\ln\frac{b}{a}}.2\varepsilon_{eff}\ \ln[1+\frac{L_G}{t_{ox}+t_p}]$$

where

$$a^1 = 2k\sqrt{k^2-1}+2k^2-1)$$

$$k = 1+\frac{t_{ge}}{t_{ox}}$$

$$a = t_c + t_{ox} + t_{si}$$

$$b = t_c + 2t_{ox} + t_{si}$$

$$\varepsilon_{eff} = \frac{\varepsilon_{ox}\varepsilon^1_{sp}}{\varepsilon_{ox}-\varepsilon^1_{sp}}\ln(\frac{\varepsilon_{ox}}{\varepsilon^1_{sp}})$$

$$\varepsilon^1_{sp} = (1+\frac{t_{ox}}{L_g})\varepsilon_{sp}$$

The total capacitances C_{total} is the summation of all the 3 components. The product of the total capacitance and the V_p gives the charge because of fringe capacitance.

$V_p = V_{bi} - V_G + V_{fb}$ for the source region

$V_p = V_{bi} - V_G + V_{fb} + V_{DS}$ for the drain region.

For further analysis of the device we can find the potential due to the charged capacitance at distance z from it. The charge density is given as: $\sigma = \frac{C_{total} V_p}{\pi\left(b^2 - a^2\right)t}$ where t is the length of the device.

So potential given by:

$$V(z) = .\frac{1}{2}\int_{y=0}^{t}\int_{r=a}^{b}\frac{\sigma.2.\pi r dr dz}{4\pi\varepsilon_{si}\sqrt{(z+y)^2 + r^2}}$$

$$V(z) = \frac{\sigma}{4\varepsilon_{si}}\{\frac{z+t}{2}\{\sqrt{(z+t)^2+b^2} - \sqrt{(z+t)^2+a^2}\}\} - \frac{z}{2}\{\sqrt{z^2+b^2} - \sqrt{z^2+a^2}\} +$$

$$\{\frac{b^2}{2}\sinh^{-1}[\frac{z+t}{b}] - \frac{a^2}{2}\sinh^{-1}[\frac{z+t}{a}]\} - \{\frac{b^2}{2}\sinh^{-1}[\frac{z}{b}] - \frac{a^2}{2}\sinh^{-1}[\frac{z}{a}]\}$$

$$V(L-z) = \frac{\sigma}{4\varepsilon_{si}}\{\frac{L-z+t}{2}\{\sqrt{(L-z+t)^2+b^2} - \sqrt{(L-z+t)^2+a^2}\}\} - \frac{L-z}{2}\{\sqrt{(L-z)^2+b^2} - \sqrt{(L-z)^2+a^2}\} +$$

$$\{\frac{b^2}{2}\sinh^{-1}[\frac{L-z+t}{b}] - \frac{a^2}{2}\sinh^{-1}[\frac{L-z+t}{a}]\} - \{\frac{b^2}{2}\sinh^{-1}[\frac{L-z}{b}] - \frac{a^2}{2}\sinh^{-1}[\frac{L-z}{a}]\}$$

In this way we can model the cylindrical fringe capacitances. The modeled results are not verified with the simulation but the objective of this chapter is to give a first-hand information of modelling the fringe capacitances in SiNTFETs.

CHAPTER 7

7 CONCLUSION

7.1 The Outcome

The work explains threshold voltage model of SINTFET and model results has been verified with the simulation results obtained by device simulation software ATLAS. Modeling the threshold voltage by inversion charge method without following the conventional method of saying the threshold voltage is the value of gate voltage at which minimum surface potential equals twice the Fermi potential because conduction in the channel begins starts before that gate voltage. The model results does not exactly match the simulation results for shorter channel lengths (<30nm) because in those lengths, quantum effects are significant to be considered.

After analysing the electrical characteristics of SiNTFET and comparing those with other types of FETs, it shows tremendous improvement. Its unique architecture enables to have a volume inversion and better electrostatic control by the gate. The both inner and outer gate can control the device performance and can have multiple threshold voltages and this characteristic can be productively used in designing circuits. The low threshold voltage, higher immunity at short channel lengths assures fulfilling the ITRS objectives. This device seems to be a promising for the upcoming research as it shows a tremendous potential to meet the demands of ULSI applications and pave a new path in the technology world.

7.2 Scope for Future Work

The idea of SiNTFETs has recently emerged. There is a wide scope for work in this area.The present work gives the first hand information of the threshold voltage modeling of the device and dealing the 3D device modelling in cylindrical coordinates with the existing knowledge on 2D modelling.

The work can be extended by including the quantum effects at short channel lengths (<30nm) which are very vital. The perfect capacitance modeling for the device can be explored.

The analysis of digital and analog characteristics can be analysed. Modeling for super-threshold parameters like the drain current, resistances, transconductance can be done. An extensive frequency analysis for the device can be done for finding the optimum range of operation for maximum outputs. The physics of the device can further be explored and can give the idea for still better devices that can revolutionize the technology.

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