Adiabatic Logic Design for Low Power VLSI Applications

A Thesis submitted in partial fulfilment of the requirements for the degree of

Bachelor of Technology in Electronics and Instrumentation Engineering

BY

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111EI0259

2014-2015

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ACKNOWLEDGEMENT

On the submission of my thesis report on "*Adiabatic Logic Design for Low Power VLSI Applications*", "I would like to extend my gratitude and sincere thanks to my supervisor Prof. Munshi Nurul Islam, Department of Electronics and Communication Engineering for his constant motivation and support during the course of our work in the last one year. I truly appreciate and value his esteemed guidance and encouragement from the beginning to the end of this thesis. I am indebted to him for having helped me shape the problem and providing insights towards the solution. "

I want to thank Prof. A.K Swain for providing the resources for my project. Again I appreciate the effort of Prof. U.C Pati, Prof. D.P Acharya, Prof. S.K Behera, Prof. A.K Sahoo, Prof. U.K Sahoo, Prof. S.K Behera, Prof. S. Sarkar, Prof. S. Kar for providing a solid background for our studies and research thereafter. They have been great sources of inspiration to me and I thank them from the bottom of my heart.

Above all, I would like to thank all my friends whose direct and indirect support helped me to complete my project in time. The thesis would have been impossible without their perpetual moral support.

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CONTENTS

ABSTRACT

A conventional CMOS logic circuit design approach depends upon charging the output capacitive nodes to the supply voltage V_{DD} or discharging it to the ground. This is one of the most used methods in VLSI designs. There are various techniques to design low power circuits both at system level as well as at circuit level to reduce power consumption. One of the major source of power dissipation is the charging and discharging of capacitor. Every time when a capacitor is discharged to ground, an amount of energy = ½ CV^2 stored in the capacitor is lost. We can reduce this power dissipation by restoring this energy to the source instead of discharging to the ground. Another way of reducing the power dissipation is to design the circuit in such a way that the charging of the capacitive node takes place very slowly. It has been observed that by charging the capacitor slowly, the energy require is lesser than faster charging method. Adiabatic circuits use the above two methods viz. slow charging of capacitor and discharging, and recycling of charge to minimize the power consumed. Several Adiabatic designs have been designed and tested in this paper. Most of them achieve significant power savings in comparison to conventional CMOS designs. The major drawbacks of these circuits include complex design for achieving simple operations, requirement of multiple clocks and requirement of complimentary input signals for controlling the charging and discharging process. The Current work is based on an existing adiabatic logic style known as PFAL (Positive Feedback Adiabatic Logic) and ECRL (Energy Efficient Charge Recovery Logic) which are simple and doesn't require complimentary signals or complex clocking.

A simulative investigation on the proposed 1-bit full adder has been implemented with the proposed technique and hence compared with standard CMOS, Positive Feedback Adiabatic Logic (PFAL), Static Energy Recovery Full Adder (SERF), 8T Full Adder and 9T Full Adder respectively. We compared all the designs and achieved a significant power saving to the extent of 40% in case of proposed technique as compared to CMOS logic in 50 to 200MHz transition frequency range. Later in this paper I have implemented the carry look-ahead adder based on adiabatic logic and got a faster response up to 100ps as compared to Full adder counterpart. A comparative result has also been shown by a graph which represents the least power dissipation of proposed technique. In this paper all circuits are analysed in terms of power using 90nm technology and simulated using cadence virtuoso and Tanner EDA.

2. INTRODUCTION

In the last few decades due to the ever growing demand for portable and small sized devices, integrated circuits require electronic circuit design methods to implement integrated circuits with low power consumption. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems.

If we want a design for low-power consumption to be successful, it is important to have a thorough understanding of the sources of power dissipation, the factors that affect them, and the methodologies and techniques that are available to achieve optimal results. Therefore, this thesis starts with the sources of power dissipation in a integrated circuit. We present —we believe— the most important low-power methodologies and power optimization techniques available. Low-power design can be applied on various different levels, such as the architectural level, the gate level, and the technology level. Apart from that, also a number of alternative logic-design styles are presented to report on their characteristics regarding power consumption. This chapter could as well be utilized by others as a quick study in the field of low-power/power-aware design.

Passive losses due to leakage currents are in focus with on-going shrinking of microelectronic circuits. Power-gating does not supply power to the inactive circuits from the power supply. Uncritical paths within a complex system can be equipped with higher V_{th} devices, allowing for a trade-off of speed for passive losses. Apart from these circuit level methods to reduce leakage losses also new transistor models are presented to minimize leakage losses in circuits.

Adiabatic Logic technique is one of the best circuit design methods to reduce energy consumption in different operations. Analysis on the gate level suggests a major cut-down of losses in adiabatic logic as compared to static CMOS. Out of a large numbers of adiabatic topologies only a few satisfy our requirements , as those are compatible to a static CMOS design flow and robust with respect to P-V-T variation and apply a manageable number of clocked power supplies that can be generated in an energy efficient manner.

3.Sources of Power Dissipation

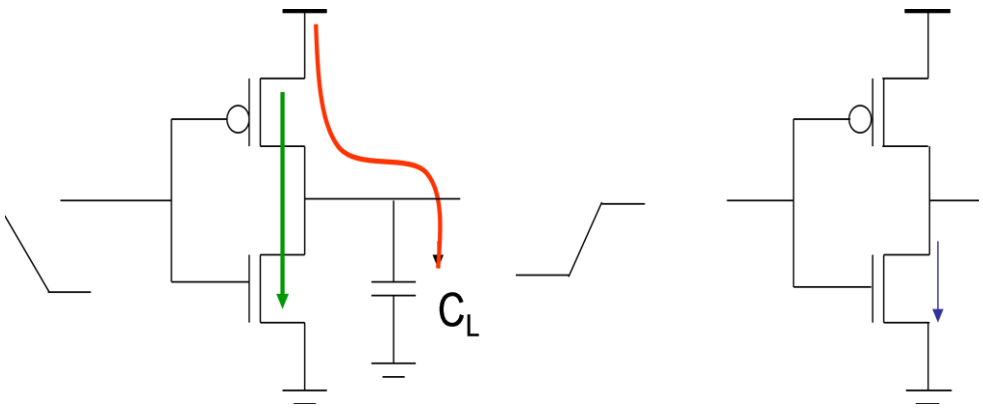
The three major sources of power dissipation in CMOS circuits is expressed using the equation given below

$$P_{total} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

$$P_{total} = \alpha . V . V_{DD} \quad F_{CLK} C_{load} + I_{SC} V_{DD} + I_{leakage} V_{DD} \quad (2)$$

In equation (2), the first term represents power dissipation due to transistor switching. V is the voltage swing, C_{load} is the load capacitance and F_{CLK} is the switching frequency of the clock. The factor α is the activity factor which represents the fraction of the circuit that is switching. In most cases the voltage swing for V is almost same as the supply voltage V_{DD}, in such cases the term V is replaced with V_{DD}.

The second term in the equation represents short-circuits power dissipation which is the power dissipation in the CMOS when both PMOS and CMOS are ON simultaneously. When both transistors are ON a current value of I_{SC} flows from the supply voltage to the ground and it is known as short-circuit current I_{SC}. Apart from these two terms viz. the switching power and short-circuit power, there is always present the power loss due to leakage currents. Leakage currents depend upon various fabrication technologies related factors like threshold voltage V_{th} , device dimensions, substrate-injection etc. In previous years a major contribution to the power dissipation was due to the switching but we have managed it effectively by reducing the switching frequency. Now a days the main focus in on minimization of leakage loss in the circuits, a various numbers of circuit design techniques are proposed and we are going to discuss some of them.



3.1 The Charging Process in Adiabatic Logic Compared to Static CMOS

The energy dissipation due to switching of a simple CMOS inverter as shown in Fig.1 is observed. The capacitor C at the output of the gate is the input capacitance of the following gates. Whether the PMOS or NMOS will be ON is dependent upon the input signal. If the input voltage level changes from 1 to 0, energy is transferred from the voltage source to charge the output capacitor to the supply voltage V_{DD}. A charge of $Q = CV_{DD}$ is taken from the voltage source, an energy quantum of

$$E(V_{DD}) = QV_{DD} = CV_{DD}^2 \qquad (3)$$

is taken from the voltage source. The energy stored on the capacitor at the voltage V_{DD} is equal to

$$E_c = \tfrac{1}{2}CV_{DD}^2 \qquad (4)$$

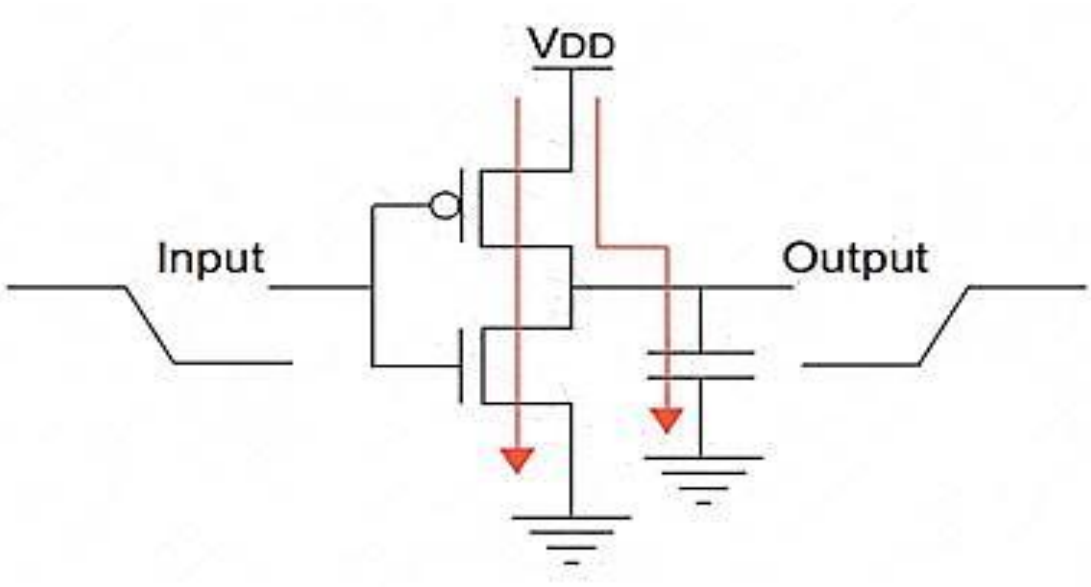


Fig.1

The energy dissipated in the circuit is equal to the difference between the energy transferred from the sources and the energy stored in the circuit. Now if the input level changes from 0 to 1, in steady state condition the NMOS channel become ON and the

PMOS is OFF. Charge stored on the output capacitance is then dissipated to the ground via the NMOS. The energy dissipation due to the switching of input level is given as

$$E_{CMOS} = ½\ \alpha C V_{DD}^2 \qquad (5)$$

Where α is the switching probability of the circuit, as there is no power loss in the circuit if no switching occurs in static CMOS (except leakage losses). Different approaches are used to reduce the energy dissipation in static CMOS. Number of transistor used for a certain operation can be reduced by following different algorithm, on structural and on circuit level. We can also reduce the capacitive load value C but it is dependent on the technology being used and intrinsic device capacitance. But we can reduce the writing capacitance value by choosing the proper architecture model and a well-designed layout. Voltage supply reduction is one of the easiest and most effective method to reduce power consumption, where as it slows the performance of the circuit.

In contrast to the above method Adiabatic Logic doesn't suddenly switches from 0 to V_{DD} (and vice versa), but a voltage ramp is used to charge and recover the energy from the output of the circuit. The principle of operation of an adiabatic gate is presented for a buffer gate in the Efficient Charge Recovery Logic (ECRL) in Fig.2. The gate consists of two cross coupled PMOS devices that are used to store the information. Two NMOS devices are used to construct the logic function. Four-phase power clock signals drives the cascade gates. Input signal for the ECRL gate are shifted by 90 degree with respect to the applied power clock signal.

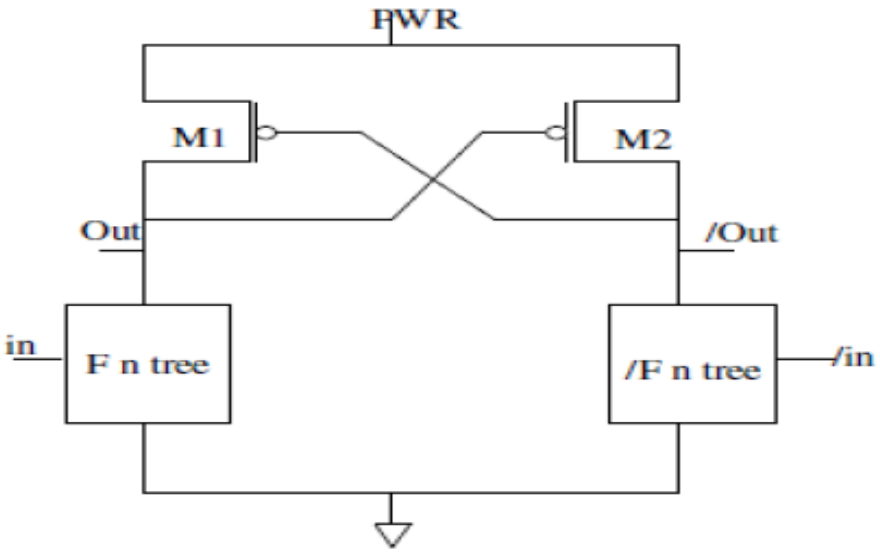


Fig.2

To calculate the energy consumption when charging a capacitance adiabatically, the equivalent circuit in Fig.3 for an adiabatic gate is used.

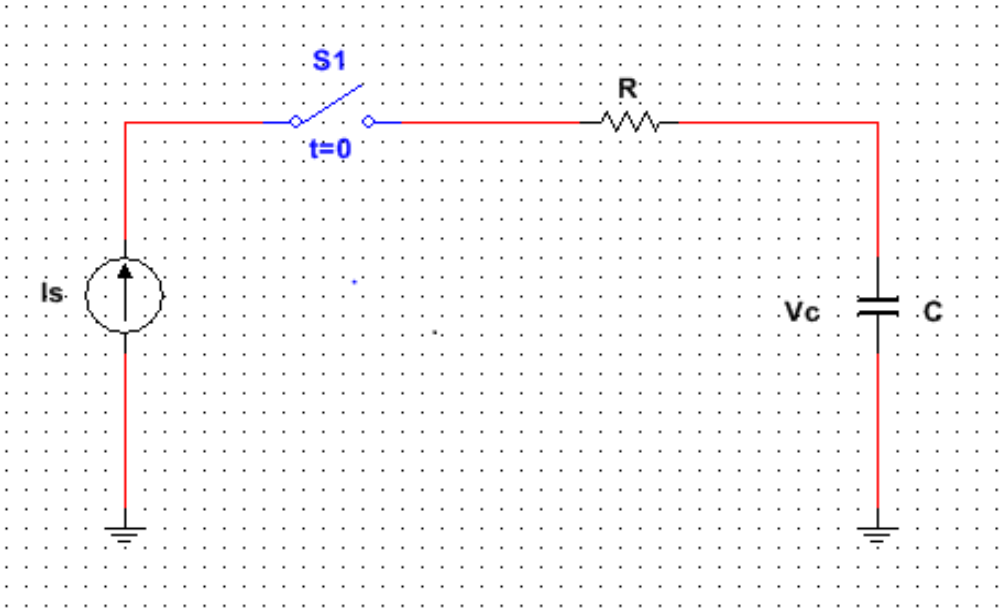


Fig.3 (Equivalent circuit to determine the losses by adiabatically loading a capacitance)

R is the resistance offered by the charging path, which is the combination of the on-resistance of transistor in the charging path and the sheet resistance of the signal line. We have assumed R to be constant for the power calculations. A voltage value is increased gradually as a ramp function from value 0 to 1,the voltage increment should be slow enough so that $v_c\ (t)$ is able to follow signal v(t) instantly, so $v_c\ (t) = v(t)$. The current flowing through the circuit can be calculated as

$$i(t) = C\frac{dv(t)}{dt} = C\frac{V_{DD}}{T} \qquad (6)$$

The energy required for the charging event can be calculated by taking integral of P(t) over a time interval of T.

$$E = \int_0^T p(t)dt = \int_0^T v(t).i(t)dt = \int_0^T (v_R\ (t) + v_C\ (t)).i(t)dt \qquad (7)$$

The second term in the integral $\int_0^T v_C\ (t).i(t)dt$ over one clock cycle will be zero, as there is no power dissipation through the capacitance. Substituting the voltage $v_R\ (t)$ with i(t).R results in

$$E = \int_0^T R\frac{C^2V_{DD}^2}{T^2}\ dt = \frac{RC}{T}CV_{DD}^2 \qquad (8)$$

As same amount of energy is needed in the recovery process, total amount of power consumed will be

$$E_{AL}=2\frac{RC}{T}CV_{DD}^2 \qquad (9)$$

From equation (9) we observe that T is dependent upon E_{AL},which concludes that operating speed of the circuit is dependent on the power dissipation of the circuit. As the value of T increases power dissipation in the circuit decreases, thus low-power can be designed by slower charging and discharging method. The power consumption can be further reduced by reducing the value of supply voltage and/or the load capacitance. In adiabatic logic the power dissipation is also dependent on the size of the transistor. In static CMOS, during one cycle the gate output will be either constant or it will switch from the former value. The activity factor α can expressed as $T> 4\frac{RC}{\alpha}$, which implies that applications with a moderate to high activity factor are suitable for adiabatic logic operations. For other cases static CMOS design is more helpful, as the steady state losses are minimum as long as there is no leakage loss in the circuit.

3.2 Energy Saving Factor

The energy saving factor (ESF) for a circuit can be defined as the ration between the energy dissipation by its static CMOS model and its adiabatic logic counterpart. It is a comparison of how much energy is dissipated by the static CMOS design as compared to adiabatic logic design. ESF compares the losses due to a single gate in the circuit. To calculate ESF we have to consider the supply voltage in static CMOS and power clock generation in adiabatic logic. The losses due to parasitic capacitance have also to be considered. A general definition of ESF is

$$ESF = \frac{\sum_{CMOS} E}{\sum_{AL} E} \qquad (10)$$

The entire energy dissipation fractions under consideration have to be summed up. We have to specify whether the EFS is being used for comparison on gate level or system level. .

4.Low Power Design techniques

Different approaches are followed for a low power design whether It be circuit-based approach or an architectural approach, in higher level programming is used to optimize the power loss. In most of the cases a combination of these methods are used for circuit design. At the circuit level the major task is to minimize any one of the components of equation (2). In the following paragraphs we have focused on different methods which are useful to minimize the losses in a design.

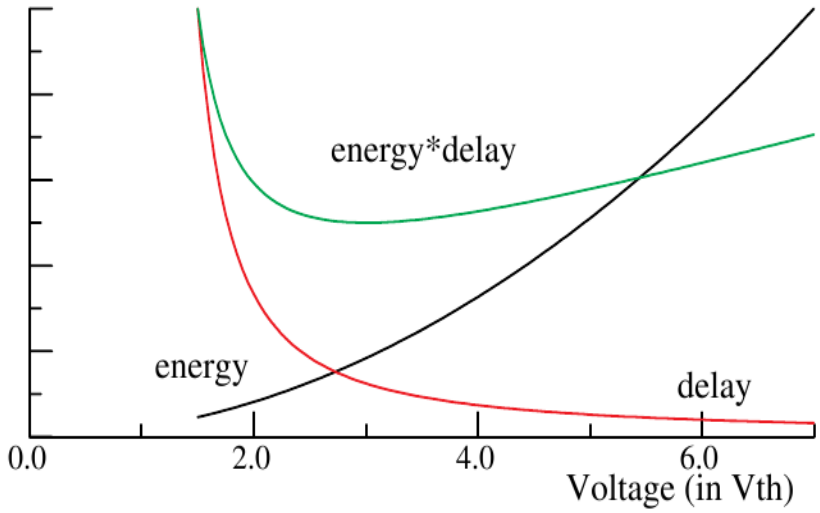


Fig.5

We know that the energy required for a operation can be reduced by decreasing the supply voltage. However due to constant threshold voltage and device capacitance the circuit performance will be slower. We know that delay is related to the threshold voltage and output capacitance as

$$t_d = \mathrm{k}\frac{CV}{(V-V_{th})^2} \qquad (11)$$

Figure.5 shows the plot of energy-per-operation, delay and energy-delay as the supply voltage is varied. At high voltages, reducing the supply voltage effectively reduces the energy with a small change in delay. At voltage level similar to threshold level a small

change in supply voltage affects the delay time with small reduction in energy. At $V_{DD} = V_{th}$ a minima is observed, at theses points changing the supply voltage does not greatly affect the energy-delay product and it is suitable to exchange energy for a small increment in delay. At a voltage level from V_{DD}= 1.5Vth to V_{DD} = 6V_{th} there is a factor of 8 variation of energy that can be traded for delay without affecting the energy-delay product [3].

4.1.1 Transistor Sizing

The reduction in size of the circuit can also save energy by a large magnitude. As the gate capacitance depends upon the size of transistor, by scaling down the transistor size also scales down the gate capacitance which ensures a reduction in power consumption, but the current drive of the logic gates are also affected by decreasing the size which can be a major source in slowing down the operation.

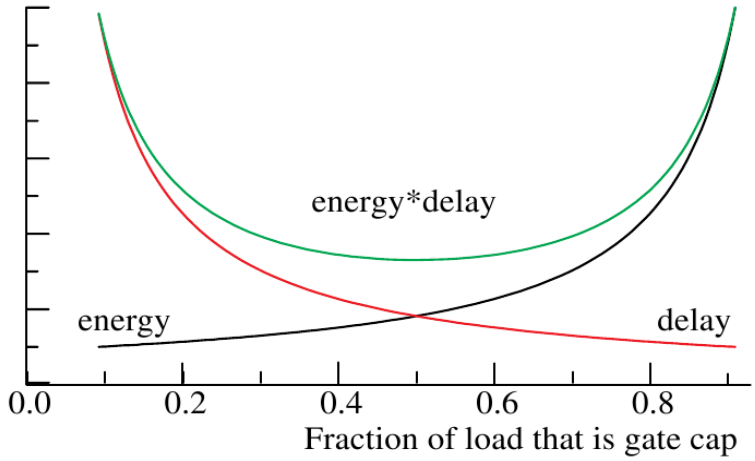


Fig.6 (Energy, delay VS transistor width)

Fig.6 shows the delay, energy, Energy-delay product of a single stage in the inverter chain as a function of the transistor's capacitance contribution to the total load. The load of the transistor will be the load capacitance of the following transistors in the chain for small sized transistor whereas for large sized transistors the gate capacitance will be taken into account. The major portion of energy consumed is due to the switching of the load capacitance in case of small sized device, for such devices the delay is proportional to the inverse of the width, hence we can improve the energy delay product by increasing the transistor width. In case of large sized devices the energy delay product is greatly affected by the self-loading due to gate terminal. So we can say that decreasing the size of the devices improves the energy delay product. The transistor is said to be in optimum operating point when the loading due to next phase is similar to self-loading. For more complex design this method is very effective. The transistors in the critical path should be sized accordingly. Using small sized device will lead to a low power design but it won't be energy efficient design.

4.1.2 Technology Scaling

We can also improve the energy-delay product by using a more advanced technology for circuit design. In case of ideal scaling technique all voltages and linear dimensions values are scaled down by a factor of ϒ (<1). Since electric field in the devices and wires remains constant, the device current and wire capacitances also scale as, since the voltages also scale by, the switching energy for each transition (CV^2) scales as Υ^3 . The delay time also improves by a factor ϒ ($t_d \approx \frac{CV}{i}$) for each logic gate. The energy-delay product decreases byΥ^4. For a scaling factor of 0.7 the device will give same performance at $0.7^4 \approx 0.25$ of the previous power consumption. But in case of ideal scaling, the threshold voltage V_{th} does not scale in with the supply voltage. The threshold voltage scaling is limited by static power dissipation due to leakage current through the OFF transistor. In case of constant voltage scaling, the capacitance is reduced and it improves both the energy and delay by a factor of ϒ, so the energy-delay product scales asΥ^2.

4.1.3 Active power Reduction

There are two methods of reducing active power or dynamic power in VLSI design. They are

a. Activity Reduction

Power consumption in the circuit is proportional to the switching frequency of the circuit and also on the load capacitance. This is valid for every signal path present in a system, whether it is a clock signal, a data pin, or an address line. Hence we can reduce the power consumption by reducing the number of transition occurring. So a correct choice of the number representation can have a great impact on the switching activity. Significant power saving can be achieved by using a gray code as minimum changes occur in gray code as compared to BCD or any other representation. Many such coding techniques have been reported that results in different power savings.

To reduce activity in synchronous logic clock gating is used. Clock gating is done by a control signal applied to a logic block; when some particular blocks are not in use clock signal is not supplied to them, this helps in reducing the clock signal activity and thus decrease the power consumption. Since power lost due to clock signal activity is substantially high this method saves a considerable amount of energy. This technique can be also be used to other signals which contributes to high power dissipation.

b. Supply voltage reduction

As we know power is related quadratically to the supply voltage, substantial power savings can be achieved by reducing the supply voltage. There are two ways to employ supply voltage reduction without compromising performance characteristics: static and dynamic.

The circuit will provide maximum performance at highest supply voltage for dynamic supply voltage scaling. When energy saving is more important than performance

then low voltage is supplied to the circuit requirement is low, substantial power reduction can be achieved by this method by trading of a lower percentage of the performance. The frequency and supply voltage can be tweaked according to the performance requirement. A mobile microprocessor for example may detect peaks in performance requirement and accordingly adjust supply voltage and frequency to deliver the necessary throughput, this contributes to a great level of power saving.

4.1.4 Leakage Reduction

Leakage components of current are always present in CMOS circuit even if the no switching activity is present. This is a major contributor in power dissipation for small sized device. In current days technologies the leakage current is a major source of power dissipation. The methods to reduce power dissipation due to leakage current are given.

a. Stacking technique

This method is used to reduce the standby leakage power. It uses the fact that and "off" transistor stack has an order of magnitude lower sub-threshold leakage than the individual transistors. To exploit stack effect in standby mode, the logic block needs to be placed in a state where all stacked transistors are turned off. This can be done manually; however, future design tool developments may automate this process. A 1.5X to 2.5X reduction has been reported using this technique.

b. Supply gating

Supply gating or "sleep transistor" is an effective method used to reduce both active and standby leakage power. It follows the same concept as clock gating technique, a high threshold value transistor is used in gating the power supply. The power supply is not provided to the logic blocks which are in OFF mode. We can scale down the leakage current by a factor of up to 1000 by using this method. There are several limitations to this method. The high threshold value transistor decreases the performance of the circuit. Again the virtual supply rails tend to decrease the noise immunity level. We need to design a local power grid for the supply rails so that the logic states won't change when the virtual supplies fail.

c. System and architecture level power reduction

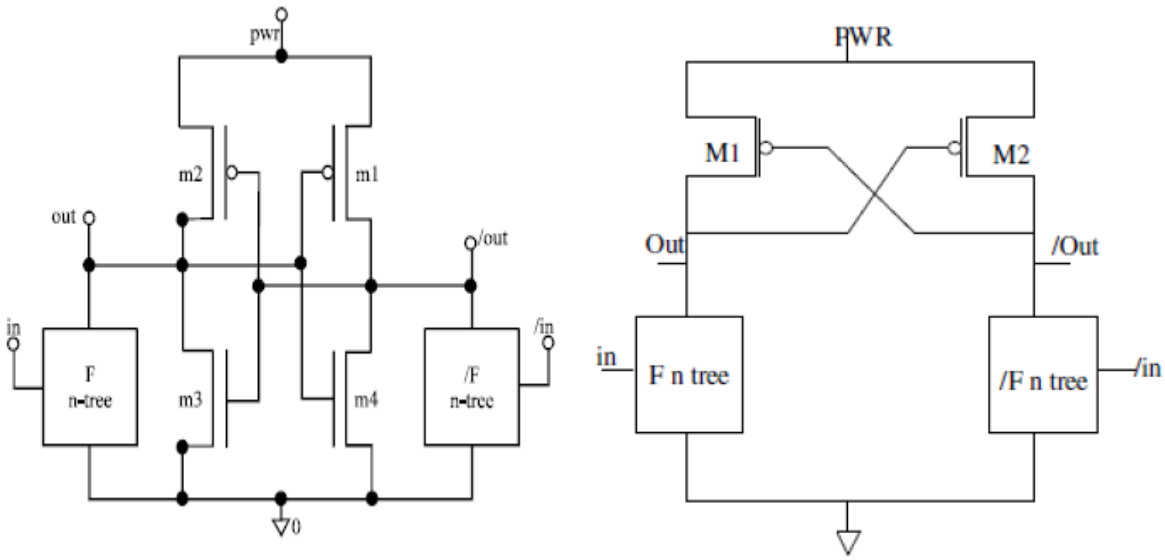
The above mentioned circuit design methods of power reduction try to minimize any one or more components of power dissipation as shown by equation(2).There are power reduction methods adopted at system level where along with the above mentioned circuit design methods, system power dissipation is reduced by careful design of algorithms and data encoding[9].Though software does not consume energy, the storage and execution of the software by the underlying hardware consumes energy .Execution of software involves power dissipation for computation, storage and communication. The energy requirement for storage is less compared to that required for execution. The power reduction in software level is done by compiling the optimized codes .

4.2 An Adiabatic System

Two main parts of an adiabatic system are (i) Digital core design made up of adiabatic gates and the power-clock signal generator. We have used two adiabatic families in this paper. The most important aspect of the adiabatic system is clock-signal generation, High saving factors can be achieved by an optimal generation of four-phase power-clock.

Two adiabatic logic families are discussed in the current paper, one is Positive Feedback Adiabatic Logic (PFAL) and the other is the Efficient Charge Recovery Logic (ECRL). Both operate in the same four-phase power-clock supply. PFAL is designed by the cross coupling of two inverters, which is the latch element. They store the output state when the input signal gradually decreases. A cross coupled PMOS pair is used in case of ECRL based on Cathode Voltage Switch Logic (CVSL). PFAL and ECRL use logic block constructed from NMOS. Logic blocks are connected from the power clock Φ to the output nodes for PFAL and from the output to Ground for ECRL.

An inverter circuit designed using PFAL and ECRL are shown below. Logic blocks are used for complex circuit design instead of transistors.



(a) (b)

Fig.4 (Inverter circuits in PFAL (a) and ECRL (b) Family)

Adiabatic Logic Families

4.2.1 Positive Feedback Adiabatic Logic Family

PFAL is a dual-rail logic family constructed using a pair of cross coupled inverters. The voltage is supplied using power-clock instead of static DC supply. This logic is constructed using NMOS devices which are attached between the power-clock and the output. Complementary inputs are given to these NMOS transistors; this produces a low resistance between the power-clock and the asserted output. The non-asserted path is given a high impendence. When the voltage difference between these two points is substantially high then only the operation is performed. Using this technique we can recover the outputs by using reverse-flowing data, thus we can decrease the power loss due to leakage. PFAL shows the best properties among the MOSFET only logic families.

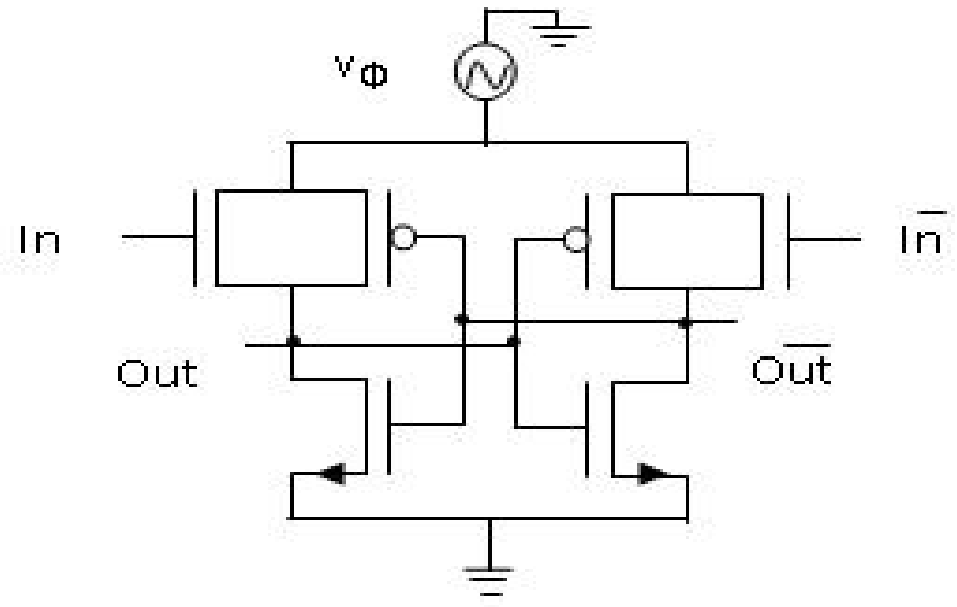


FIG.5 (Positive Feedback Adiabatic Logic)

4.2.2 ECRL-Efficient Charge Recovery Logic

Efficient Charge–Recovery Logic (ECRL) is a cross-coupled PMOS transistors. It is constructed by using two cross-coupled transistors *M1* and *M2* and two NMOS transistors. To recover the power supply from the output and restore it an AC power supply is used at the gates. The clock generator always drives a constant load capacitance irrespective of the change in input level.

Full output swing is obtained because of the cross-couple PMOS transistors in both pre charge and recovers phases. The circuit suffers from non-adiabatic loss in pre-charge and recover phase due to the threshold voltage of the PMOS but due to the threshold voltage of the PMOS transistors. That is, to say, ECRL always pumps charge on the output with a full swing.

$$E_{ECRL} = CV_{th}{}^{2}/2$$

Thus, from Equation it is clear that the power consumption of the circuits depends on the load capacitance and not on the operating frequency.

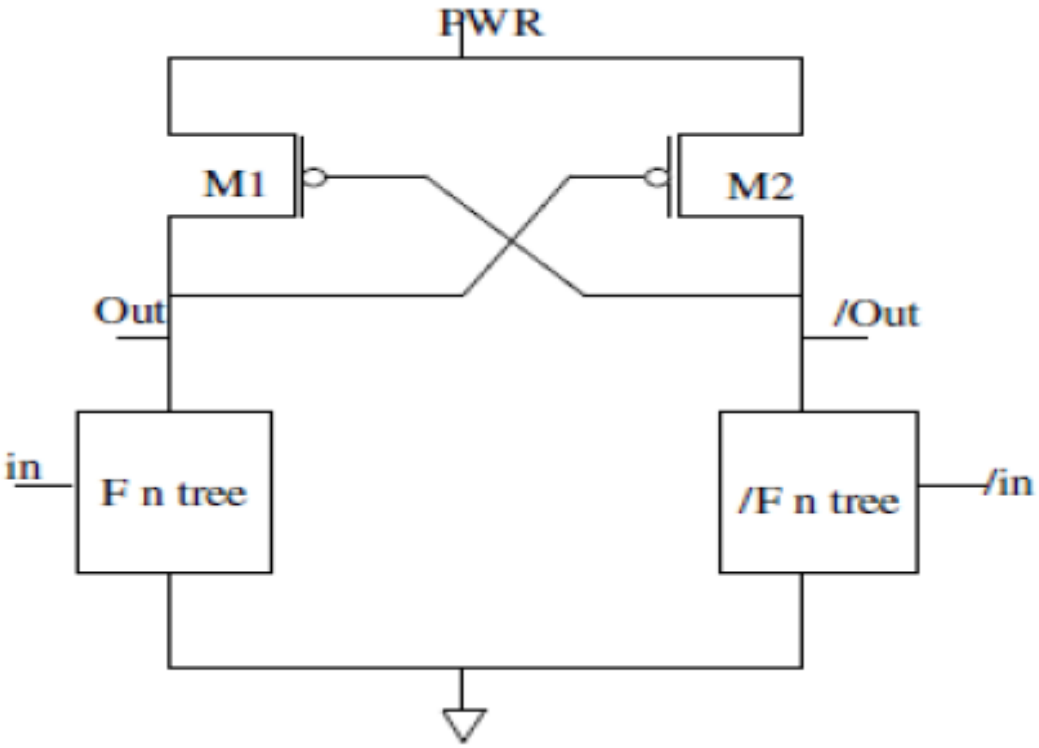


FIG.6 (Positive Feedback Adiabatic Logic)

4.3 FULL ADDER CIRCUIT DESIGN

a.Full adder circuit design using static CMOS

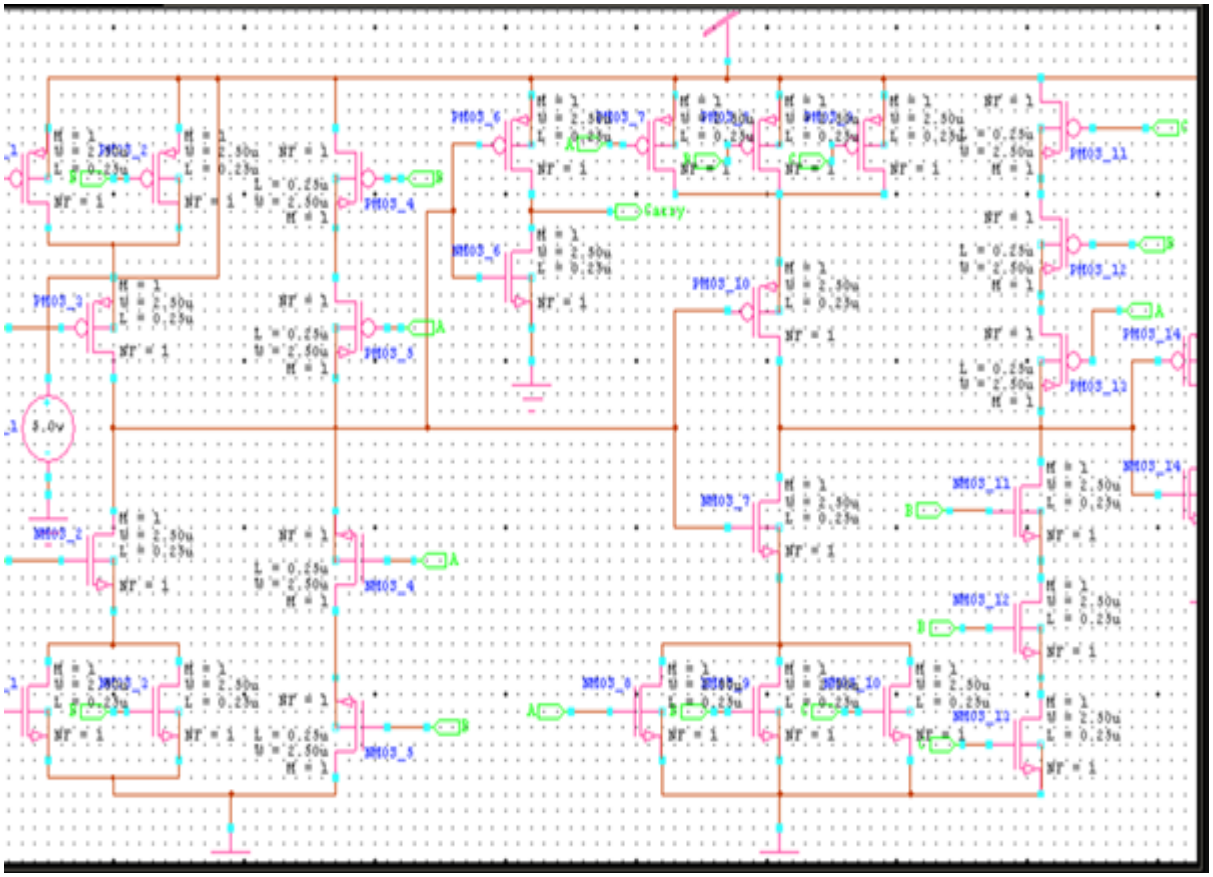


FIG.7(Full adder circuit design using static CMOS)

b.Static Energy Recovery Full adder (SERF)

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation mechanism results in faster XOR and XNOR outputs and also it balances the output delays from the SUM and CARRY output. This leads to less spurious SUM and Carry signals. The output capacitance is also minimized as no inverter is connected at the output stage. If the output suffers from threshold voltage loss then signal drivers can be used to reduce the degradation. The generated outputs using the driver will have same rise and fall time. This ensures better performance characteristics like faster speed, low power dissipation and driving capabilities of the circuit. If a driver is used at the output then the output voltage will have same voltage level as the supplied voltage. The circuit diagram of static energy recovery adder is shown in figure.

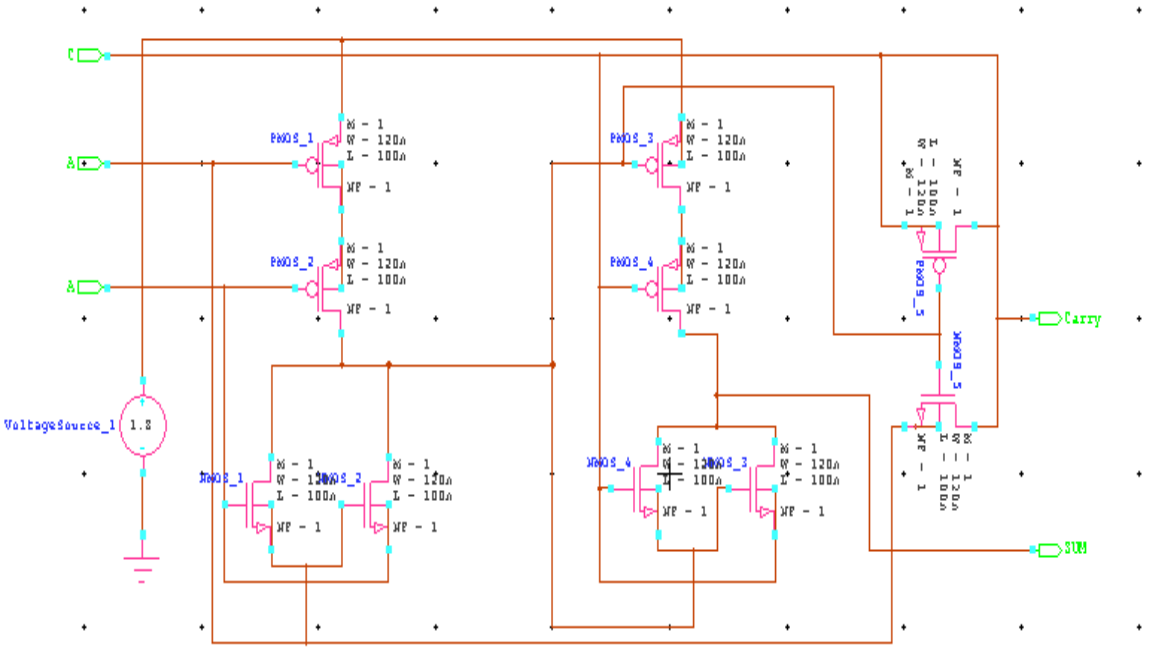


Fig.8(Schematic of SERF)

c.8T full adder

In this circuit sum output is obtained by cascade XOR of three inputs and C_{OUT} module is implemented using 2T multiplexer. Sum and Carry outputs pass through two delay stages

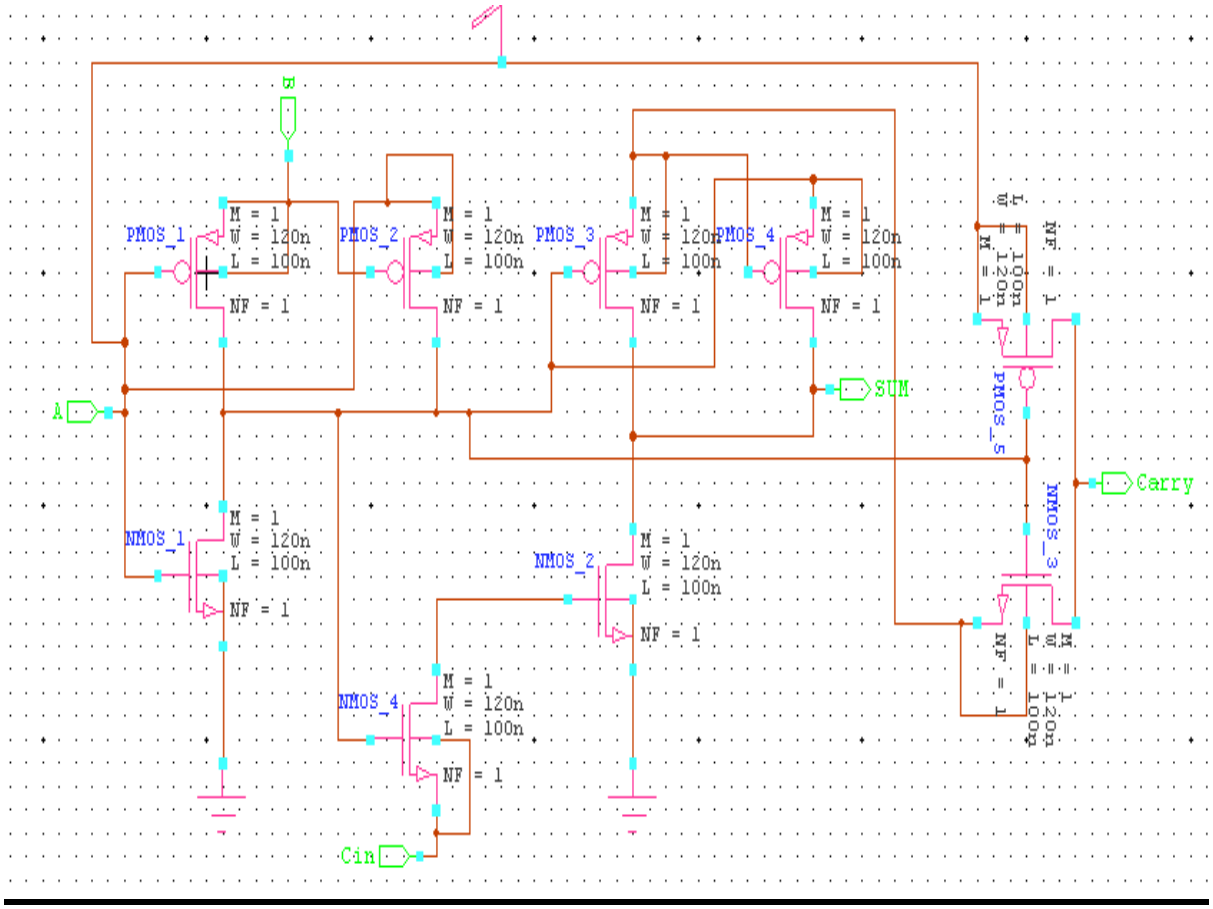


Fig.9(Schematic of 8T Full Adder)

d.9T full adder

The SUM output can be obtained from XOR and XNOR operations between inputs B and C_{IN} . To implement XOR function an inverter is connected at the output of first stage XNOR gate. Finally the Sum is implemented by transferring these output levels through 2T multiplexer. Input to PMOS transistor M6 is XOR of B and C_{IN} while to NMOS M7, input is XNOR of B and C_{IN}. The input signal A controls the 2T multiplexer. C_{OUT} is obtained by using another 2T multiplexer which is controlled by output of first stage XNOR gate and passes either A or Cin accordingly. The circuit ensures improvement in power consumption and temperature sustainability because it operates in super threshold region.

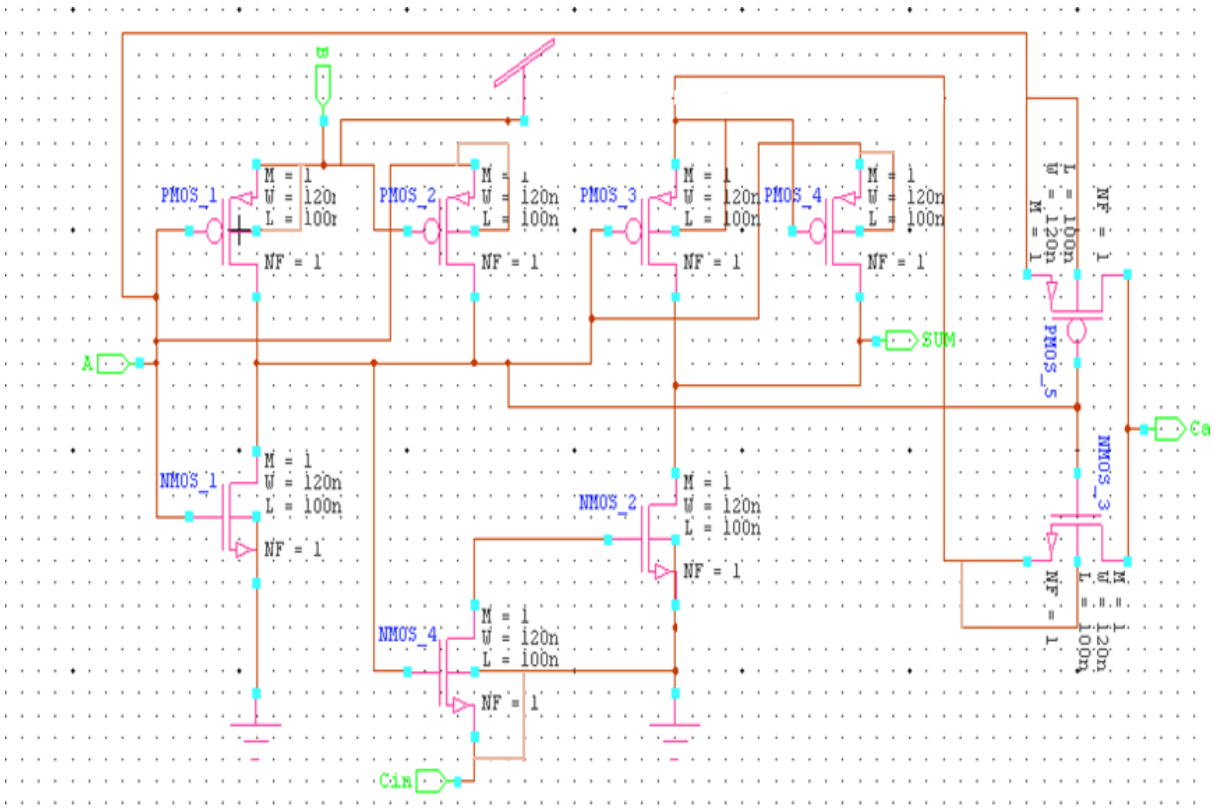


Fig.10(Schematic of 9T Full Adder)

4.3.1 RESULTS

1. Power dissipation comparison between Full Adder using static CMOS, SERF and CPAL

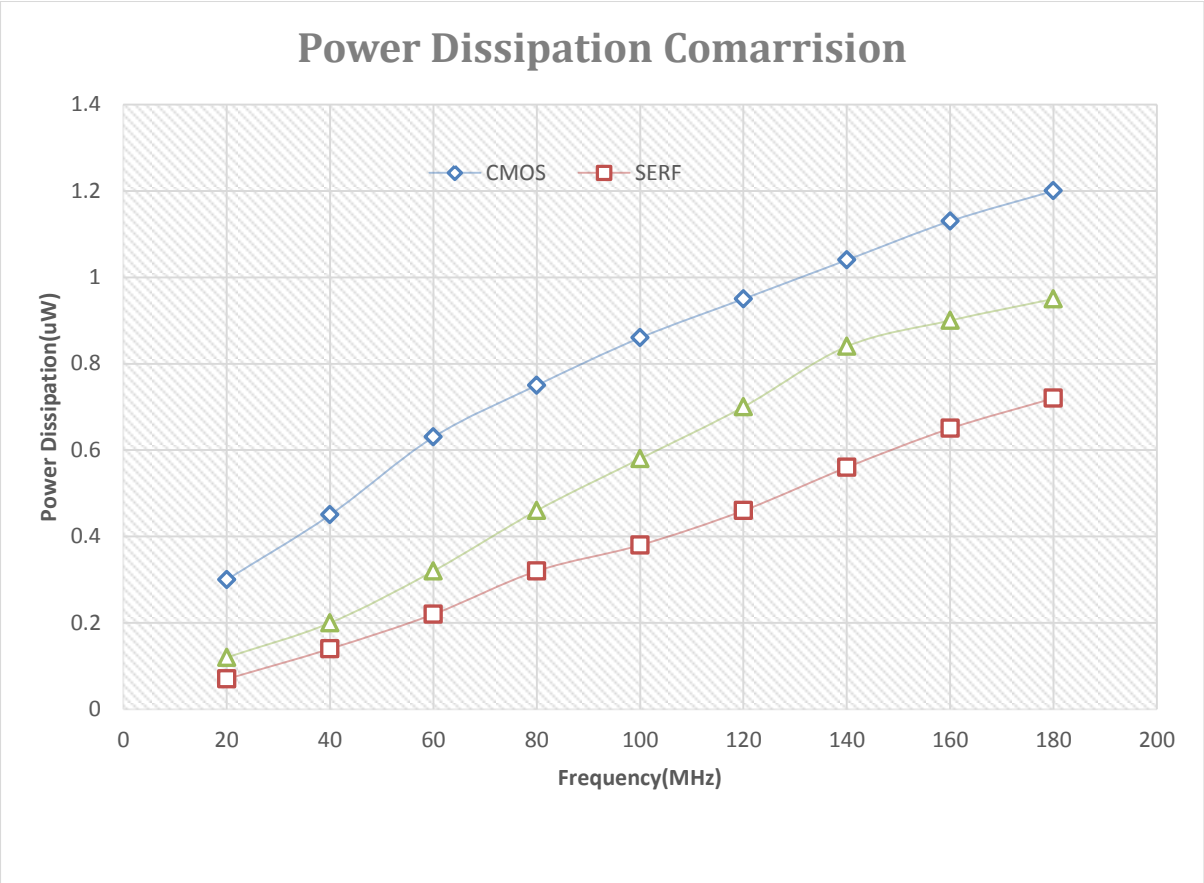


Fig.10(Comparison of power using different methods)

2. Power dissipation comparison between 8T and 9T adiabatic full adder

Power Dissipation:-

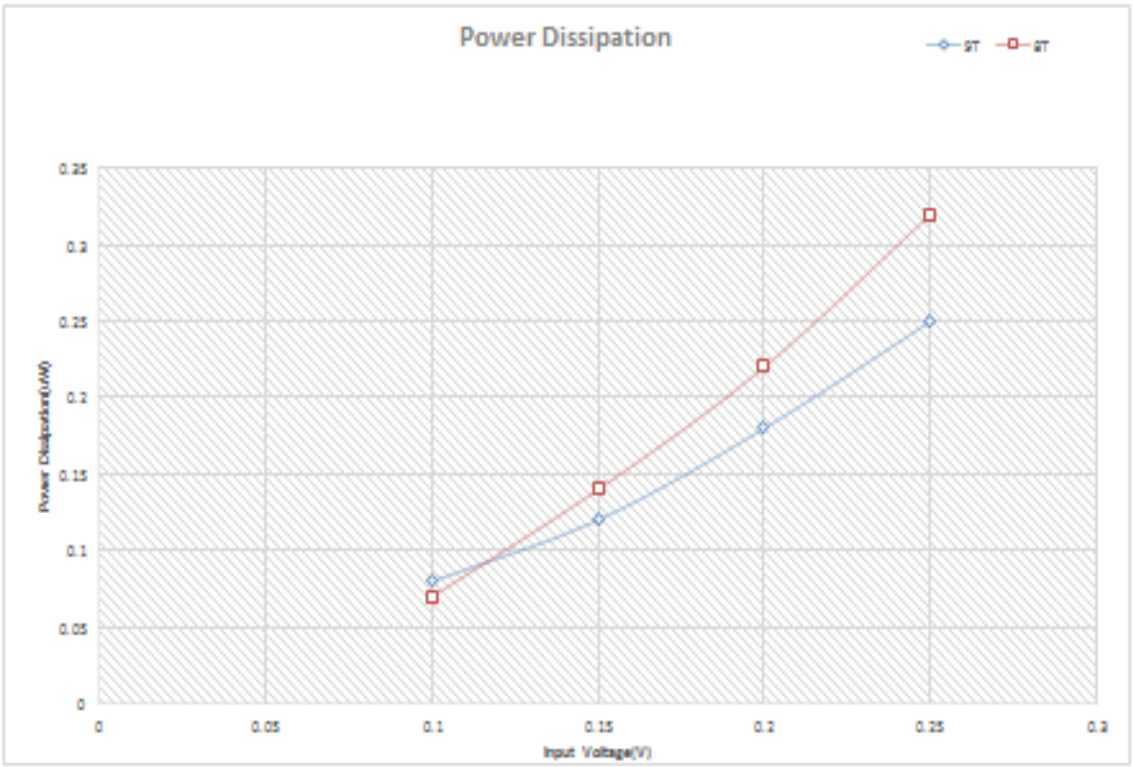


Fig.11(Power dissipation 8T VS 9T Full Adder)

3. Noise Performance of 8T and 9T adiabatic full Adder

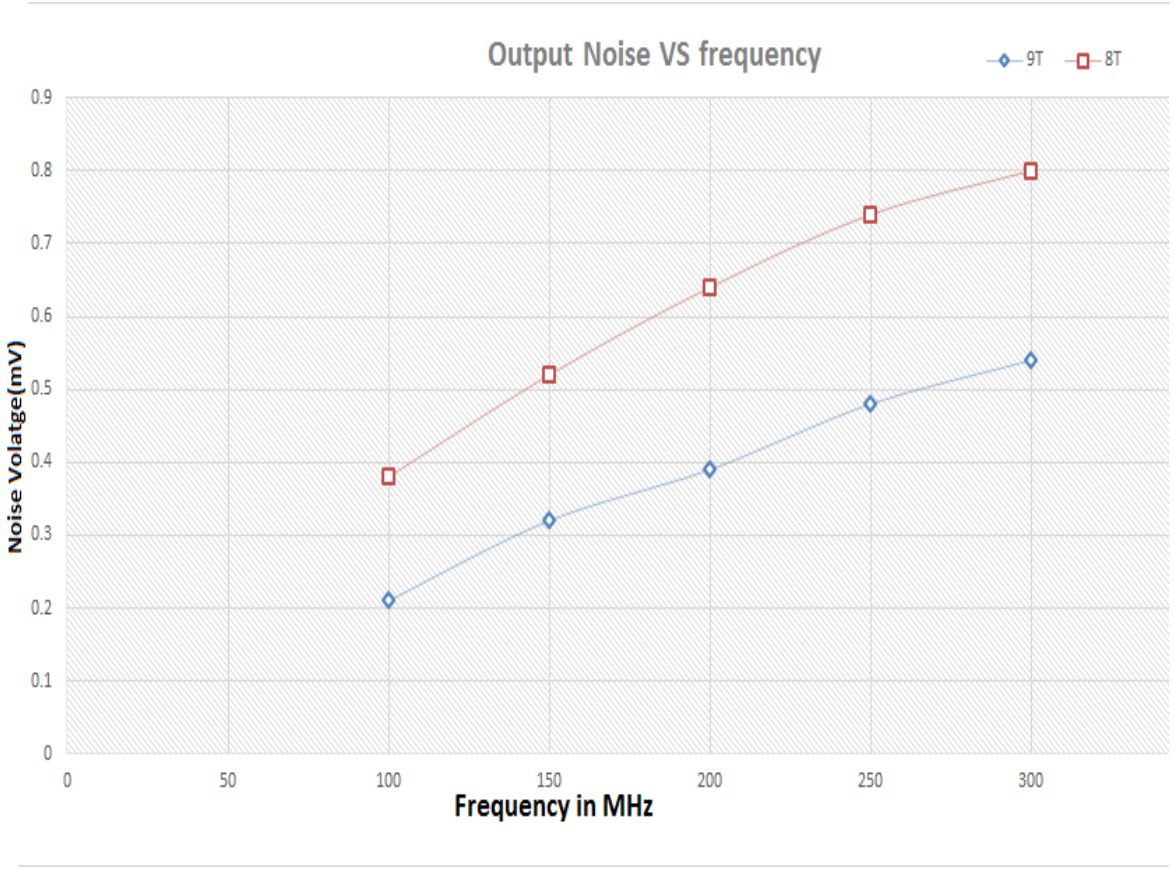


Fig.12(Noise performance of 8T VS 9T Full Adder)

5. Design and Implementation of Low Power 4-bit Carry-look Ahead Adder Using Static CMOS Logic and Adiabatic Logic

Carry look-ahead-adder is used to reduce the computation time for binary addition. The computation is a two step process; two intermediate values known as carry propagator and carry generator are calculated from the input signals. If the adder has two inputs a_i and b_i, then P_i and G_i can be written as follows.

$$P_i = a_i \text{ xor } b_i$$

$$G_i = a_i \text{ and } b_i$$

Using c_i as the carry input, the sum and carry output can be written as follows.

$$S_i = c_i(\text{xor})\ a_i(\text{xor})b_i$$

$$c_{i+1} = G_i\ or\ (P_i\ and\ c_i)$$

Expanding the c_i , the c_{i+1} can be generated as a function of inputs and c_0 .

The functional block carries two 4-bit inputs and 3 carry outputs as shown in the figure 7. The c_{in} and 3 carry outputs have been used to generate 4-bit sum output. From the above equation we know that XOR, AND gates and Carry Propagator & Generator circuits are used.

A. Inverter design

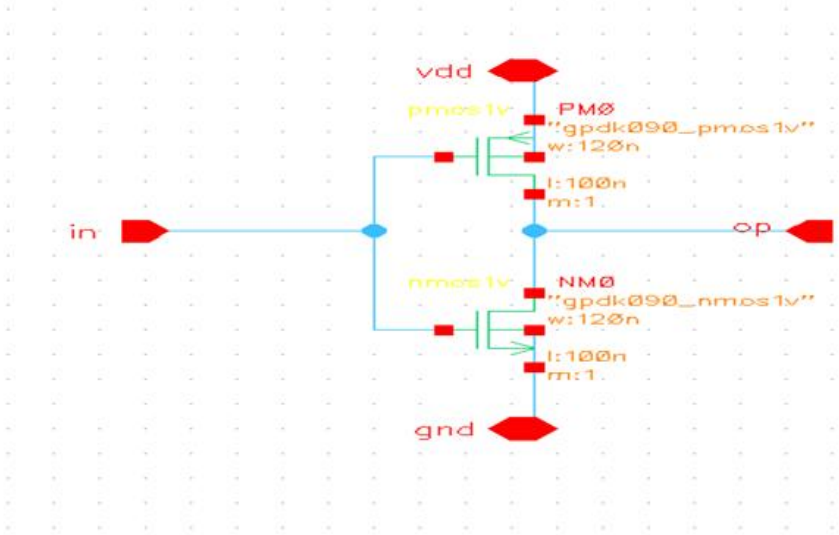


Fig.13(Inverter Schematic Diagram)

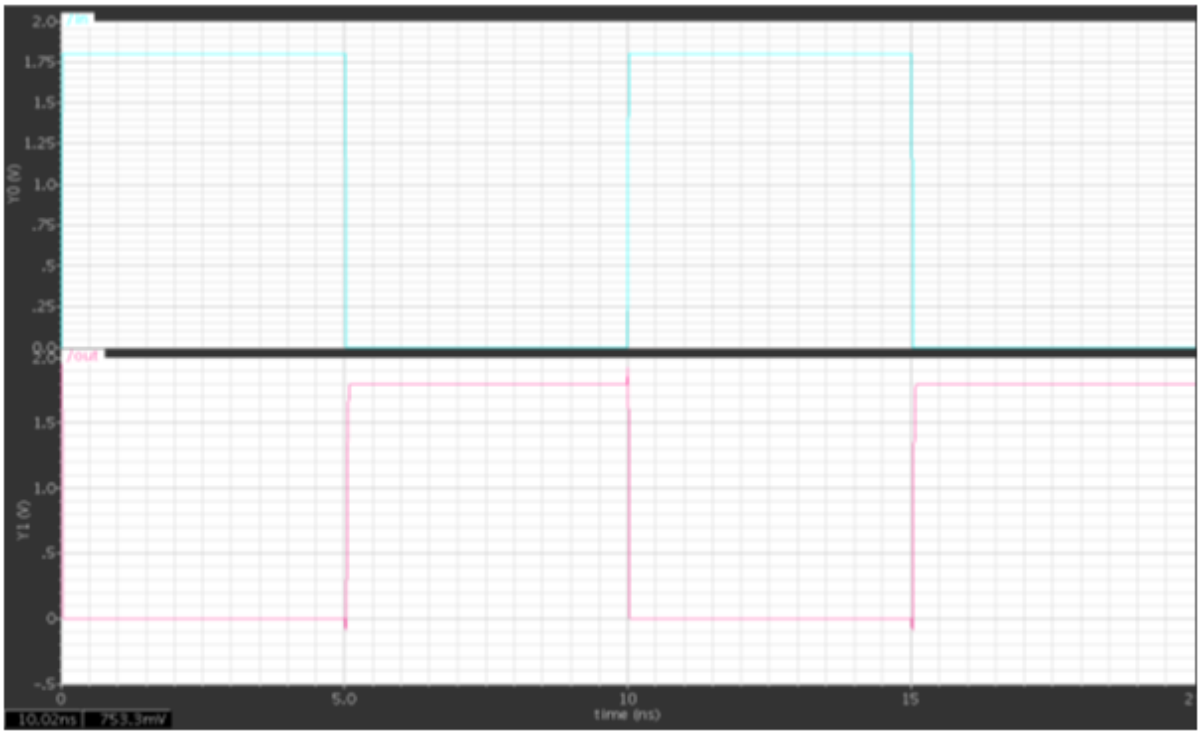


Fig.14(Inverter Output)

B. AND gate Design

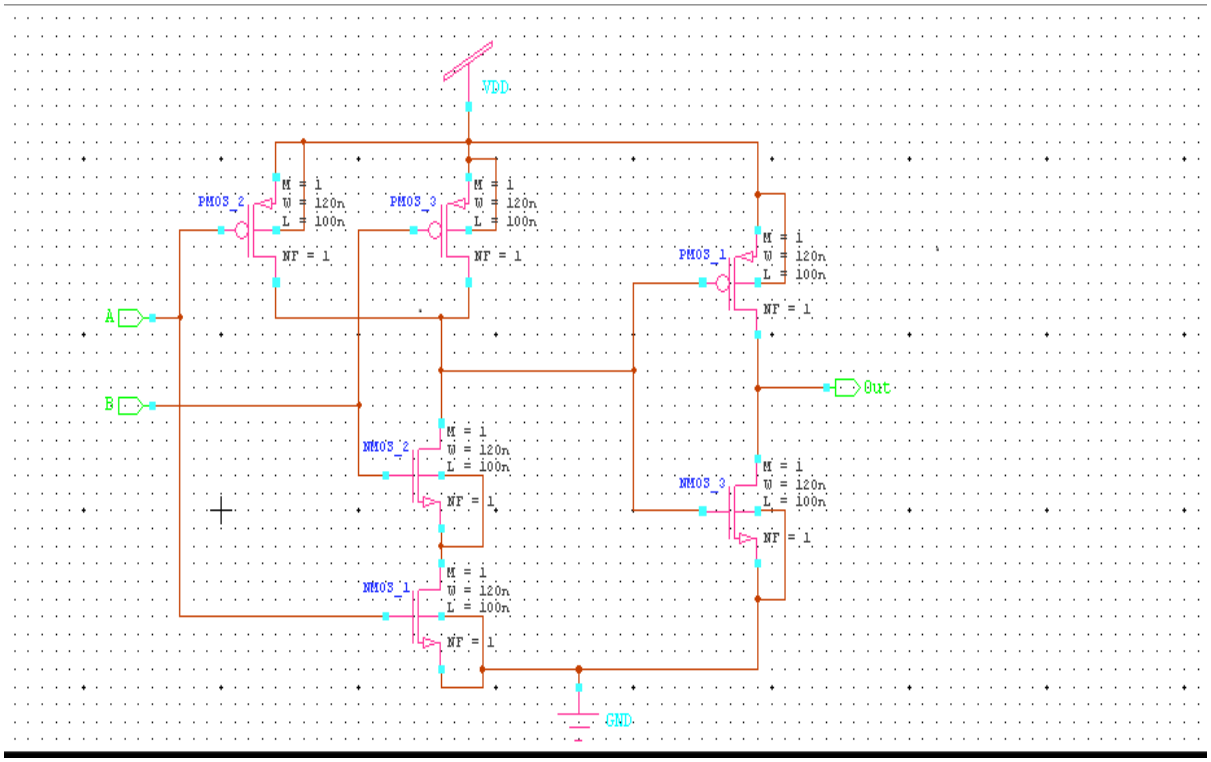


Fig.15 (Schematic of AND gate using static CMOS)

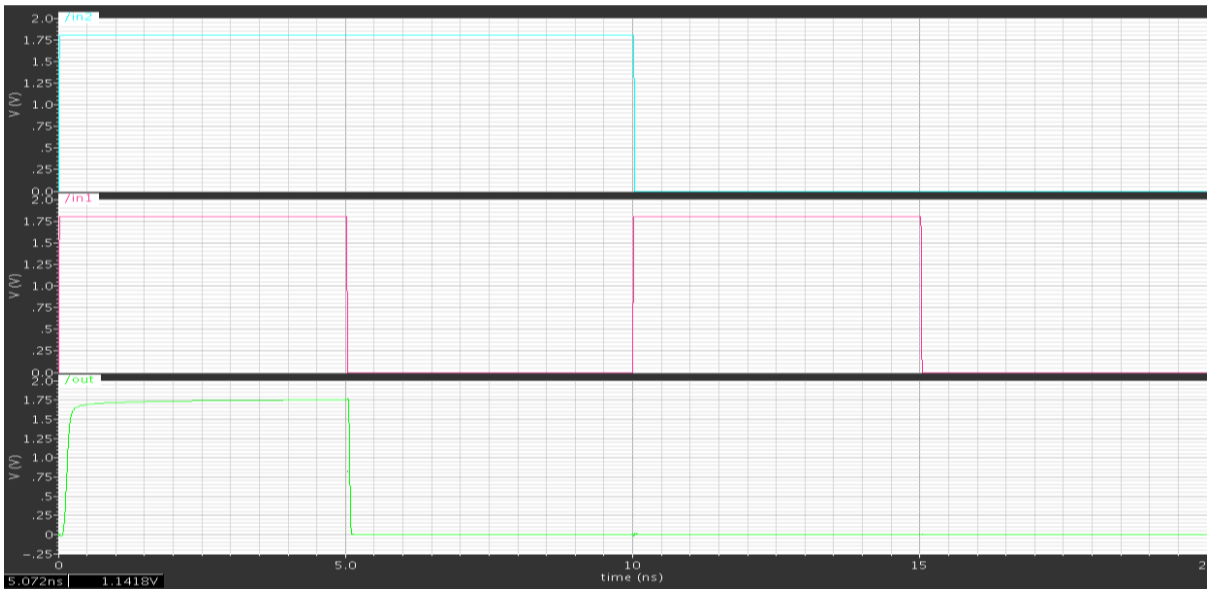


Fig.16(AND Logic Output)

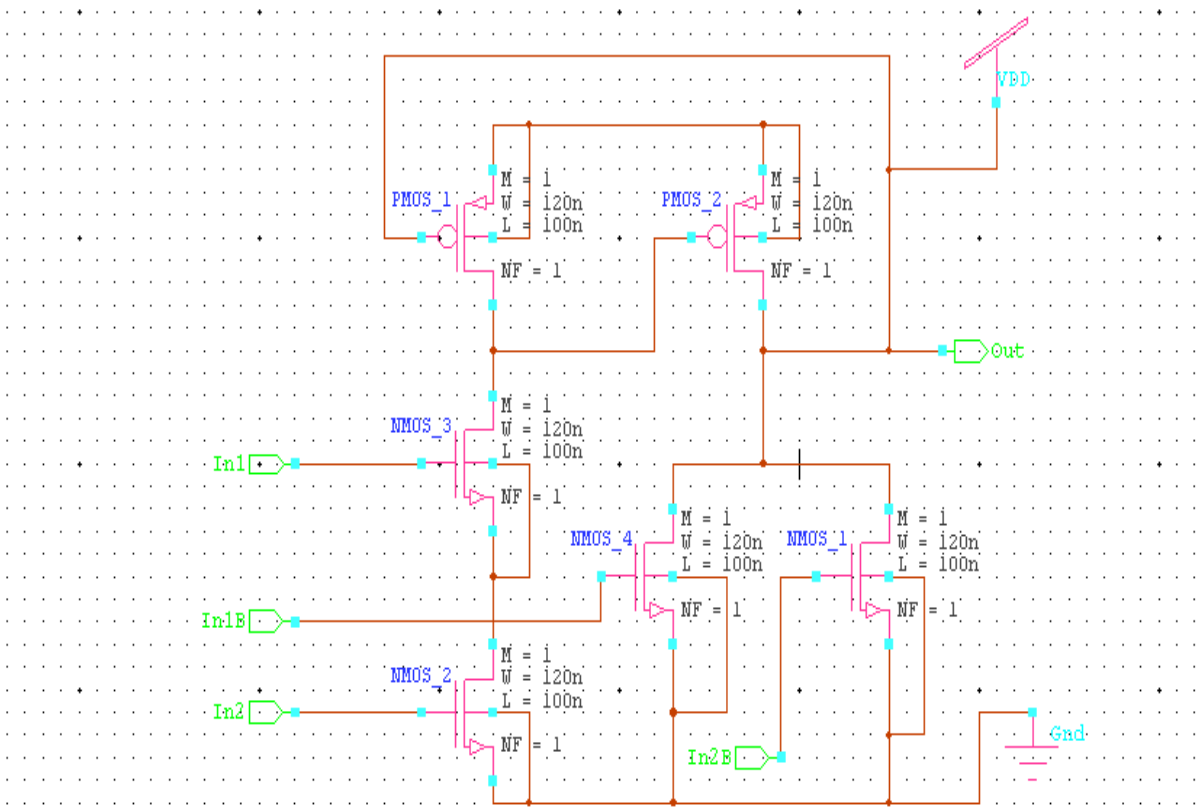


Fig.17(Schematic of AND gate using Adiabatic Logic)

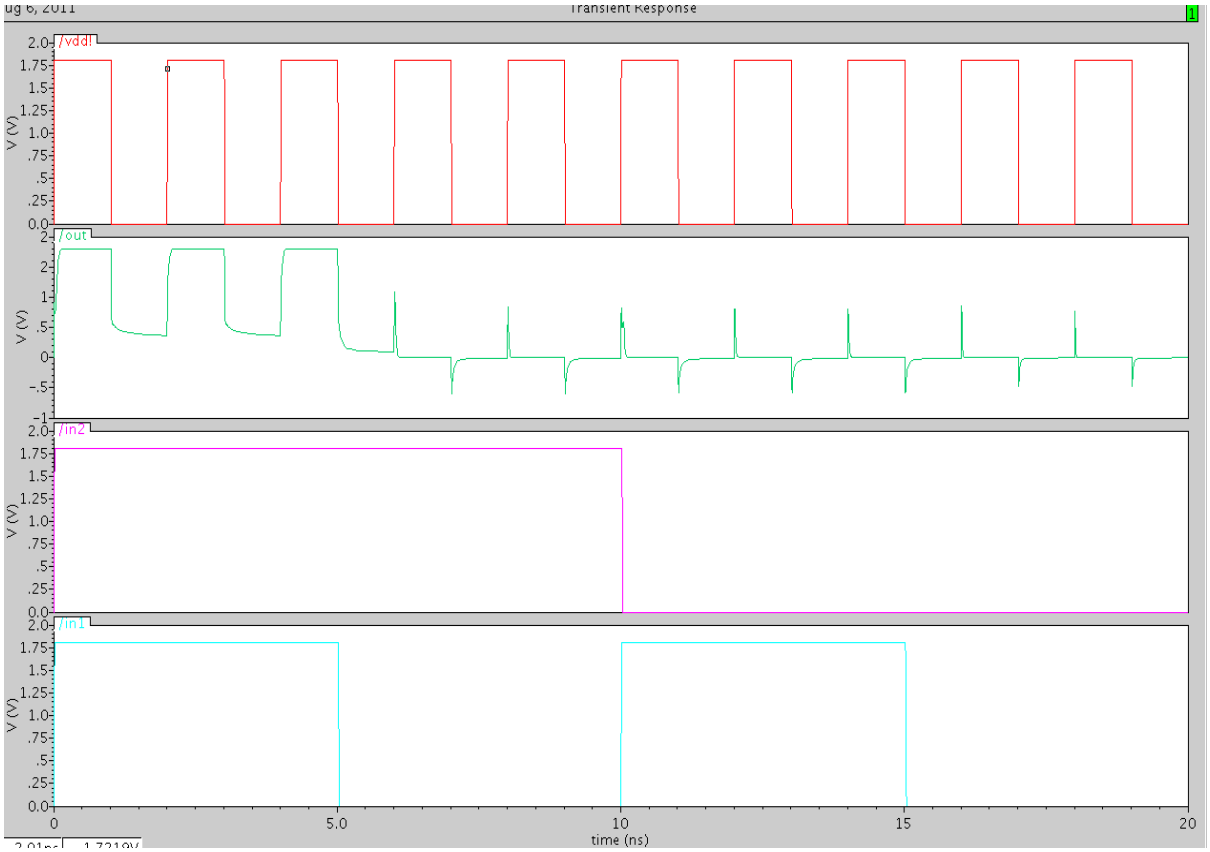


Fig.18(OUTPUT)

C. XOR gate design

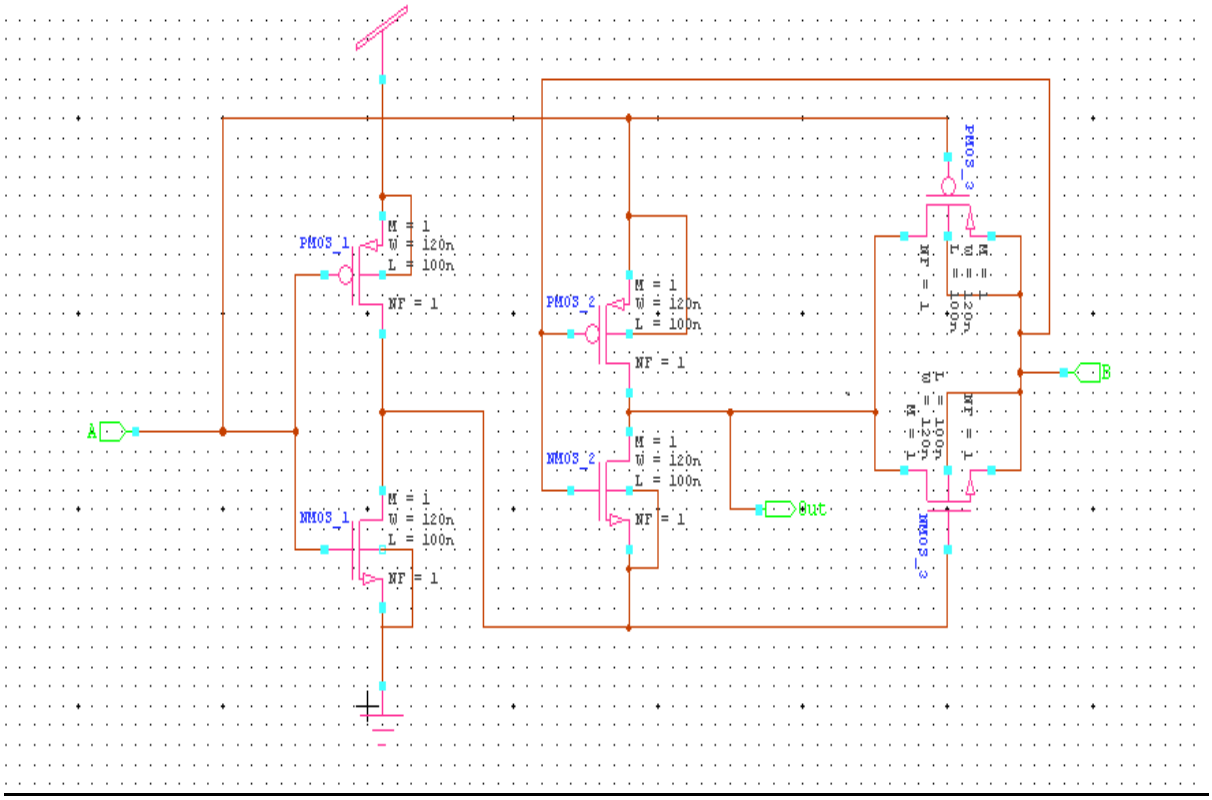


Fig.19 (Schematic of XOR gate using Static CMOS)

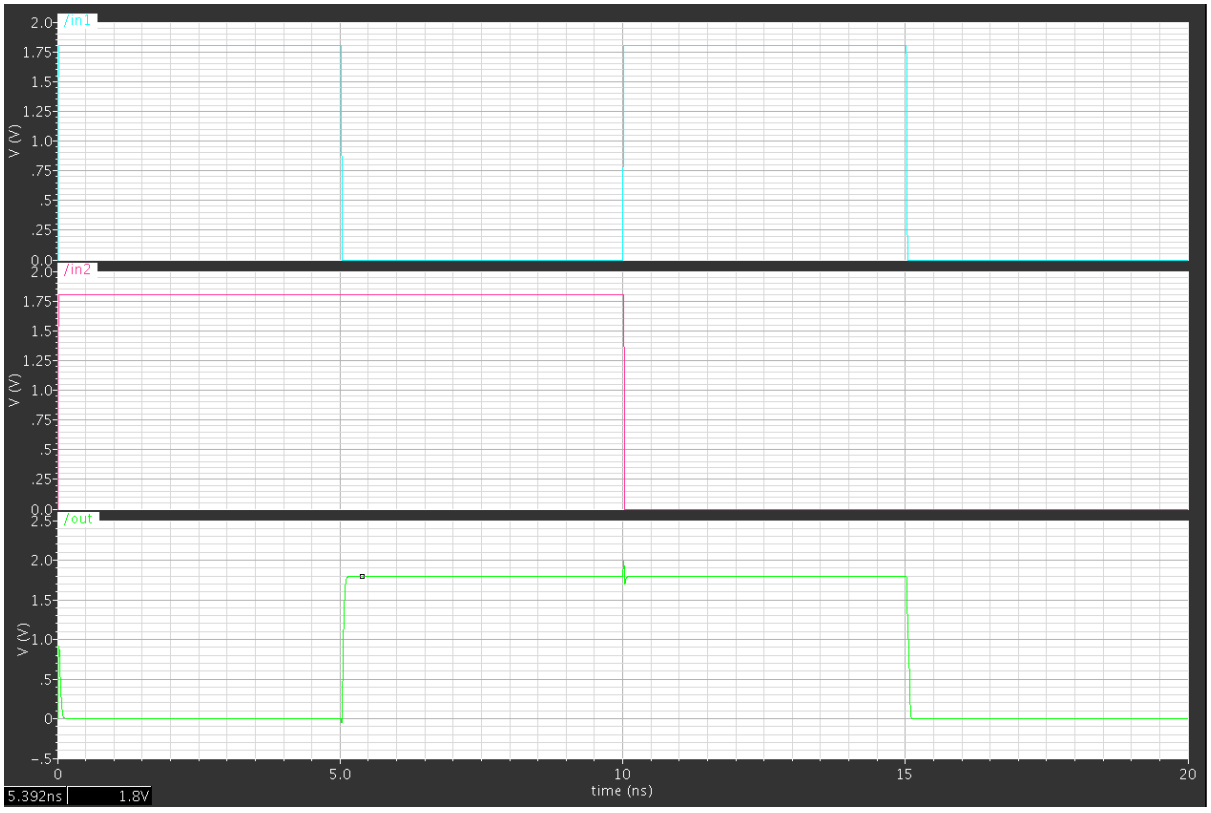


Fig.20(OUTPUT)

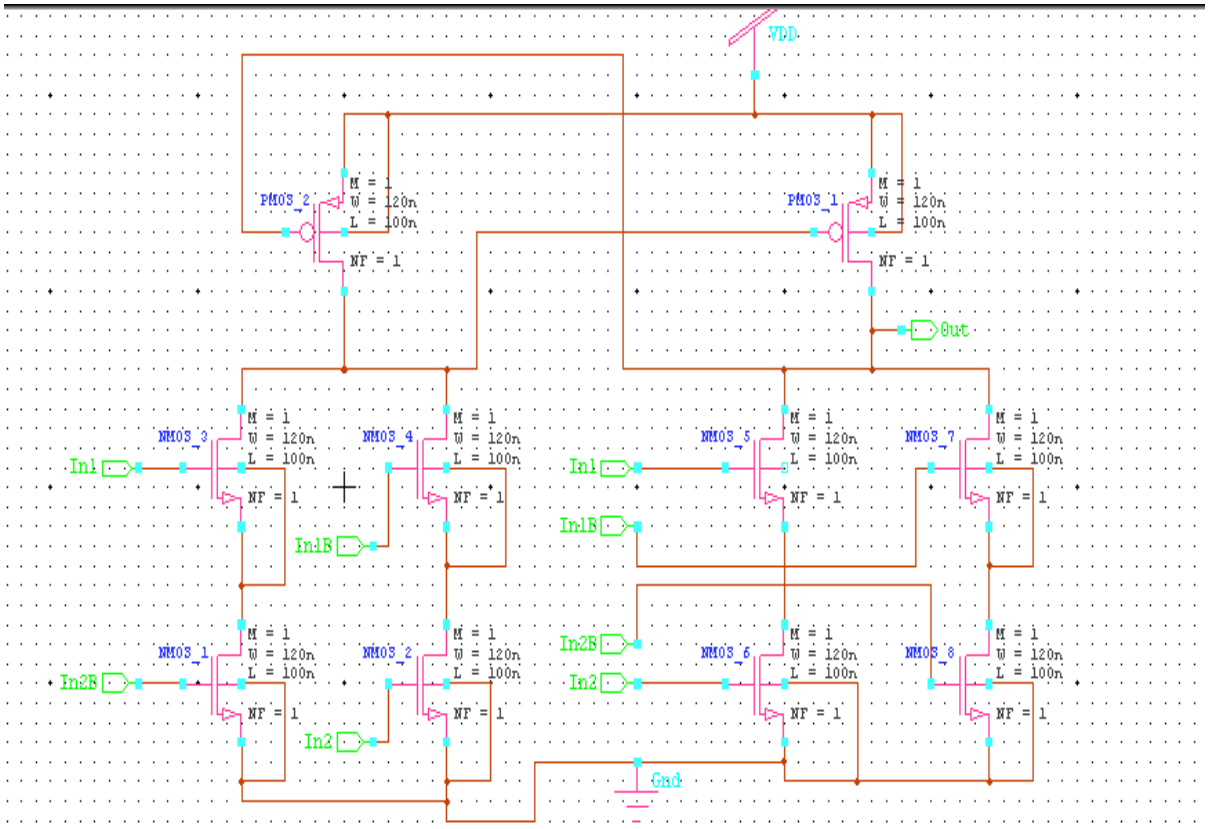


Fig.21(Schematic of XOR gate using adiabatic logic)

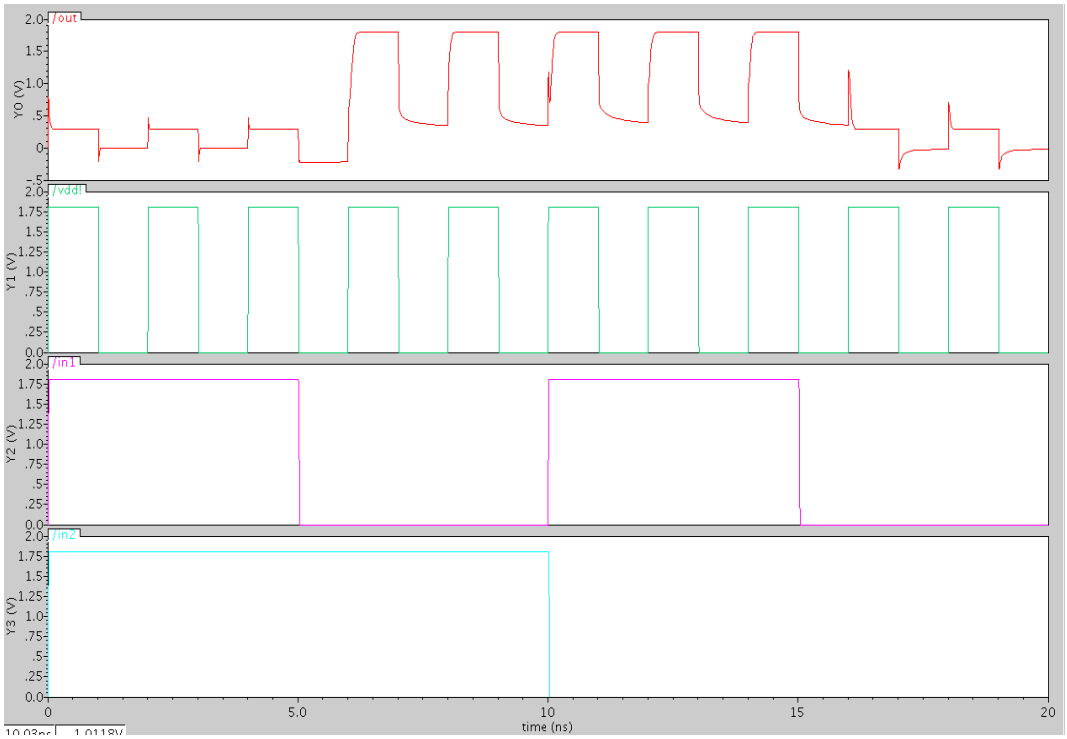


Fig.22(OUTPUT)

D. Propagator and Generator

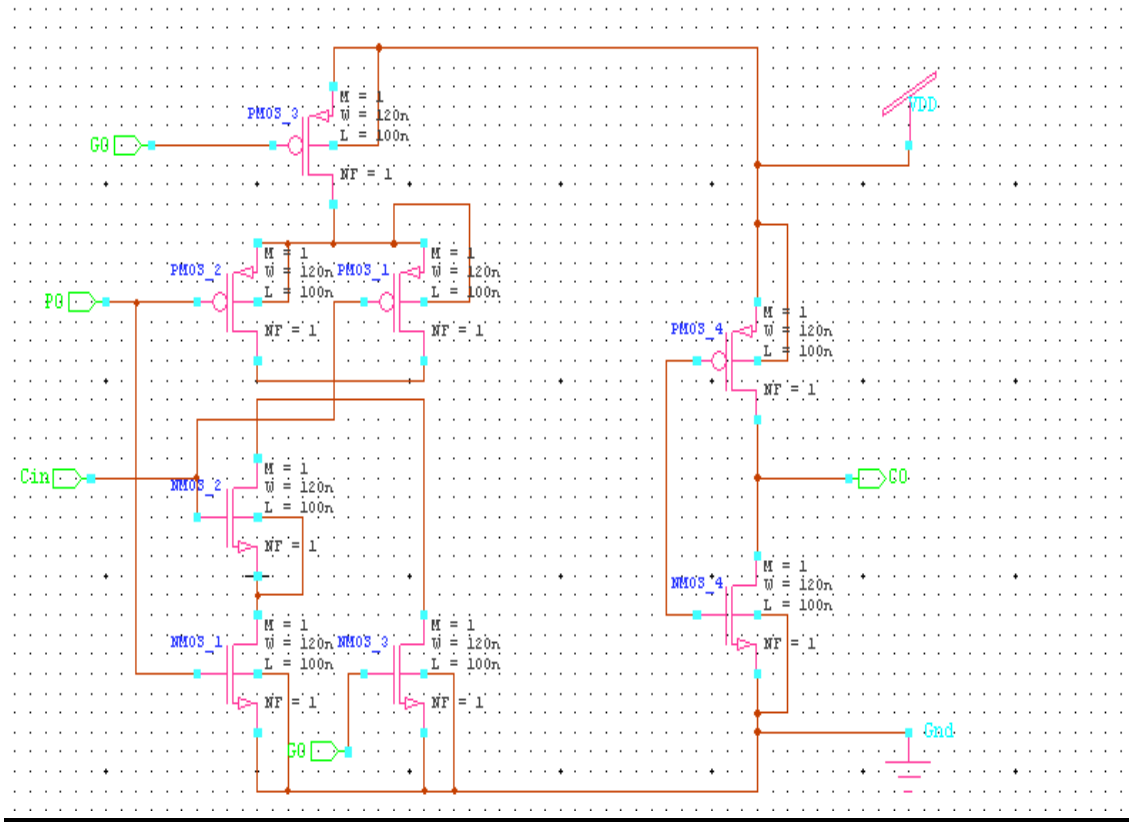


Fig.23(Schematic diagram of carry propagator)

E. 4-bit carry Look-Ahead adder

Carry look ahead adder depends on two things that have been .

(i) ¨ Calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the right.
(ii) Combining these calculated values to be able to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right.

Supposing that groups of 4 digits are chosen. Then the sequence of events goes something like this:

(i) All 1-bit adders calculate their results. Simultaneously, the look ahead units perform their calculations.
(ii) Suppose that a carry arises in a particular group. Within at most 3 gate delays, that carry will emerge at the left-hand end of the group and start propagating through the group to its left.
(iii) If that carry is going to propagate all the way through the next group, the look ahead unit will already have deduced this. Accordingly, before the carry emerges from the next group the look ahead unit is immediately (within 1 gate delay) able to tell the next group to the left that it is going to receive a carry - and, at the same time, to tell the next look ahead unit to the left that a carry is on its way.

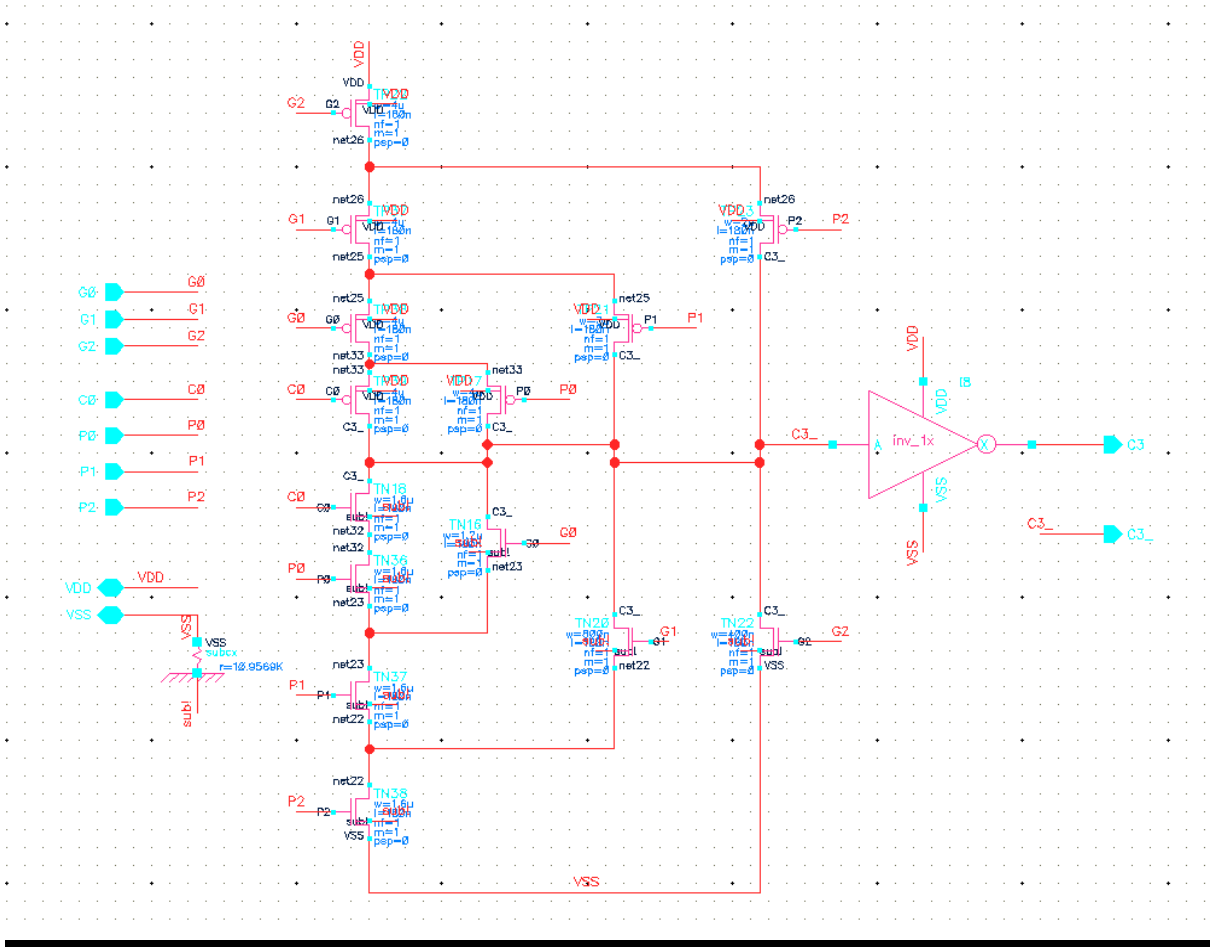


Fig.24(Schematic Diagram of CLA)

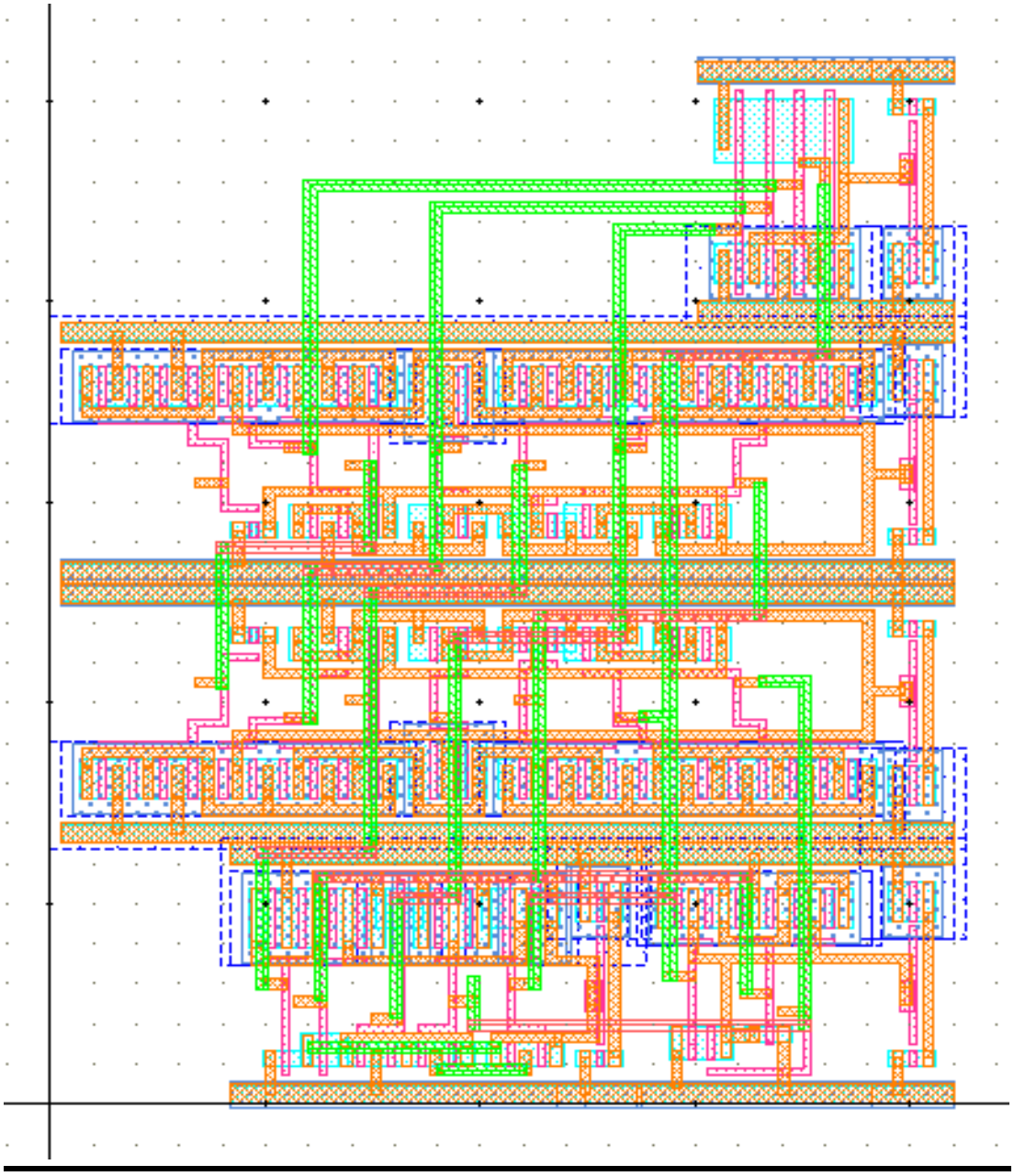


Fig.25(Layout design of CLA)

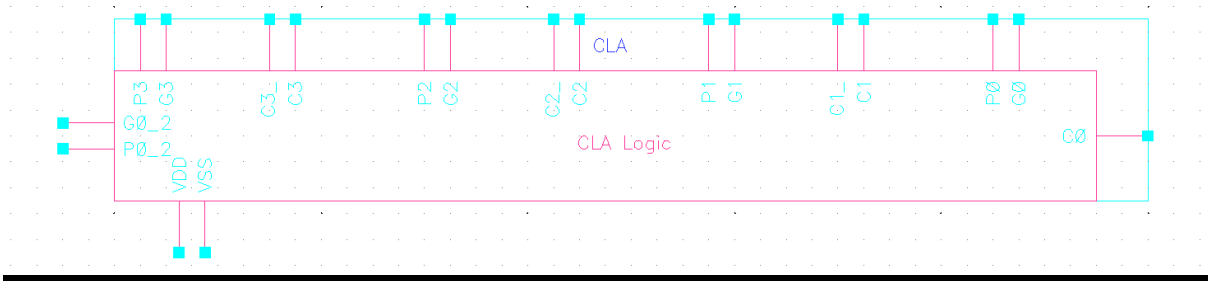


Fig.26(CLA design Block)

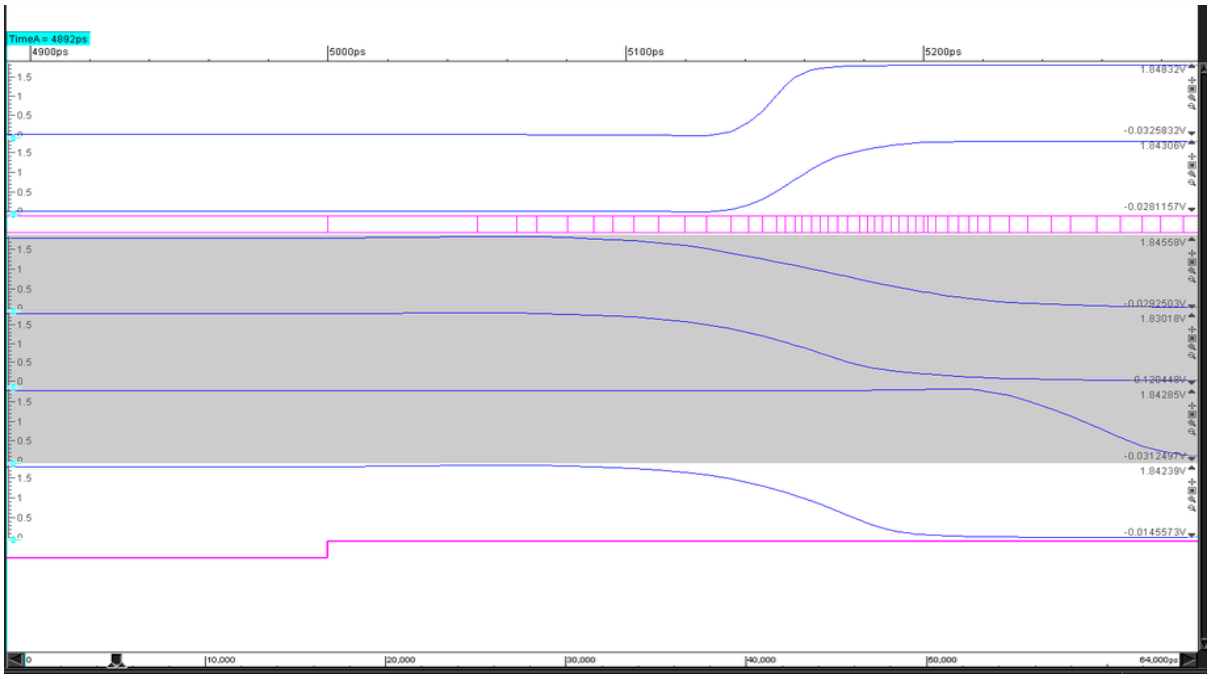


Fig.27(Output delay comparison of CLA and Full Adder)

5.1 RESULTS

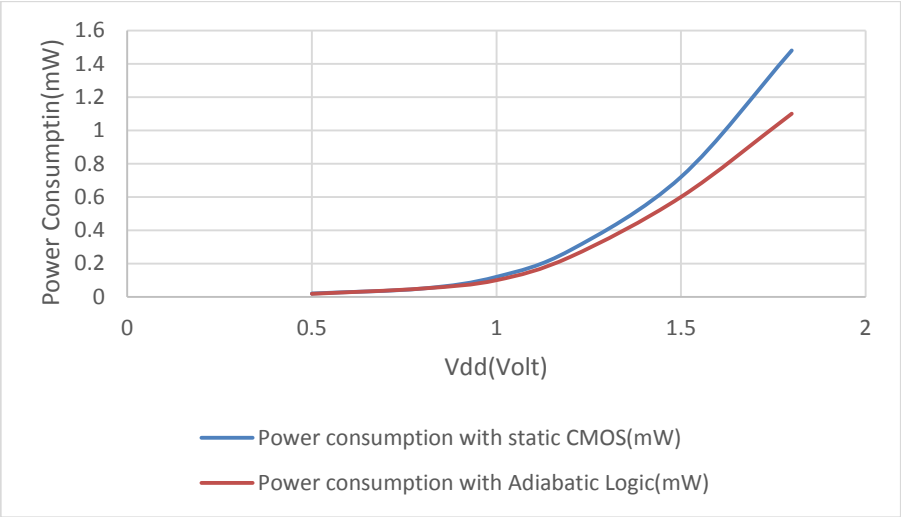


Fig.28(Power consumption comparison between static CLA and adiabatic CLA by varying Vdd)

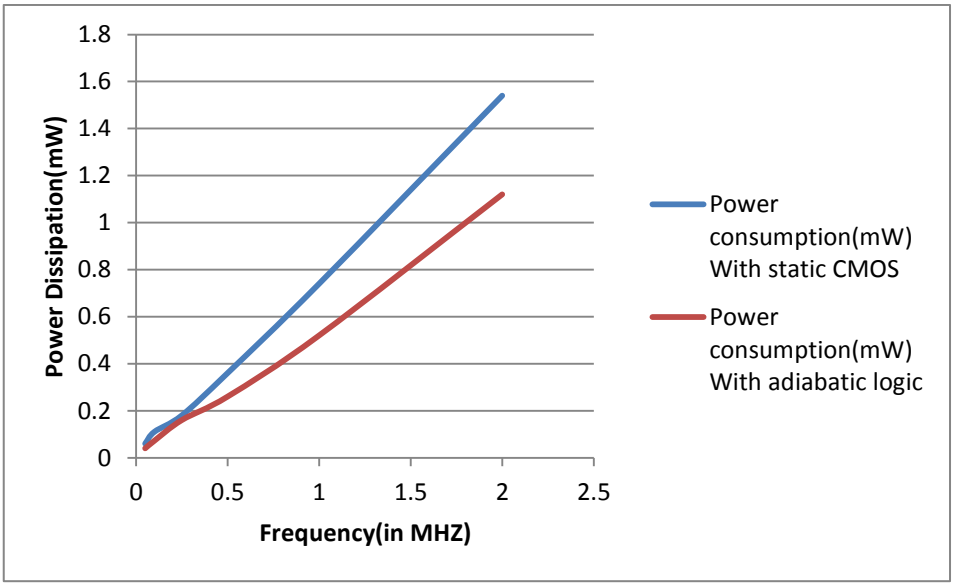


Fig.29(Power consumption comparison between static CLA and adiabatic CLA by varying clock frequency)

6. CONCLUSION

The main idea of this project is to introduce the design of high performance and power efficient full adder design using multiplexer based pass transistor logic. In the current work, the full adder design is implemented by different logics like SERF, PFAL, and ECRL etc. Further the design is implemented using pass transistor logic combined with other logic. The number of transistors required for realizing mixed CMOS design of full adder is less than the number of transistors required in realizing the design of full adder using CMOS transistors independently. So, the required logic can be realized within an optimized area which performs faster when compared to the conventional static CMOS full adder design.

From the output results I found out around 40% less energy conversion in adiabatic logic design as compared to the static CMOS design counterpart. In the second half of the thesis carry look-ahead adder is designed using adiabatic logic which ensured faster operation than the full adder design.

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