UNDER WATER ACOUSTIC MODEM DESIGN

Thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology
In
Electronics and Communication Engineering

By

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NATIONAL INSTITUTE OF TECHNOLOGY

ROURKELA

CERTIFICATE

This is to certify that the work on the thesis **Underwater Acoustic Modem Design** by **Sakuntala Sahoo** and **Priyanka Priyadarsini Swain** is a record of original research work carried out under my supervision and guidance for the partial fulfillment of the requirements for the degree of **Bachelor in Technology** in the department of **Electronics and Communication** Engineering, **National Institute of Technology, Rourkela**.

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ABSTRACT

We present a reconfigurable modem for underwater acoustic communication, using BPSK modulation with coherent detection. The modem is capable of throughput up to 16 kbps in the 1-2 MHz band, while being a flexible platform for deployment in a variety of scenarios, with real-time parameters to optimize communication with respect to channel conditions. In order to maximize the flexibility the system was implemented on an FPGA, so that the implementation can be changed during operation. The transmitter was designed mainly for compactness, using a digital direct synthesizer and IP CORE generator technique to generate the output signal. Phase synchronization technique is adopted for the recovery of transmitted data at the receiver section.

CONTENTS

Chapter1

Introduction

Small, dense, wireless sensor networks are beginning to revolutionize our understanding of the physical world by providing fine resolution sampling of the surrounding environment which could provide significant benefits to mankind. Underwater wireless communication systems have experienced a large development and increasing interest among the scientific community in the last recent decades. But as compared to the advances in airborne wireless communications, this development is almost negligible. Advanced underwater communication networks leads to improvised divers and submarine communications , UAV (underwater automatic vehicle) navigation and control [5], and under water robotics. An efficient Underwater sensor network will provide a promising solution for exploring and observing the aqueous environments which operate under the following constraints:

- Unmanned underwater exploration: Underwater conditions are not suitable for human exploration. Unpredictable underwater activities, High water pressure, and the vast size of underwater areas are major reasons for unmanned exploration.
- Localized and precise knowledge acquisition: Localized exploration is more useful and precise than remote exploration because underwater environmental conditions are typically variable in time and localized at each venue .We may not be able to acquire adequate knowledge about physical events using SONAR or other remote sensing technology.

The evolution of digital electronics, however, as well as an improved understanding of the physical properties of the underwater channel and the associated design trade-offs, have propelled the development of efficient systems for both academic and practical use. Advanced modulation schemes and equalisation algorithms, made possible by the availability of cheap processing power, brought underwater communications closer to their radio counterparts, and have fostered research into underwater networks for commercial and scientific applications.

1.1:THESIS STATEMENT:

This thesis describes the design of a short-range underwater acoustic modem starting with the The modem provides bit rates of up to 40 kbps.The major contributions of this thesis are:

- The design of a novel acoustic analog transceiver using a field programmable gate array (FPGA) implementation .
- Binary Phase shift keying (BPSK) based digital transceiver that provides comparable power consumption to other underwater digital transceiver designs.
- A linear programming model that optimizes for energy consumption and cost on a linear underwater network.
- Implementation of IP CORE generator to optimize the system and to operate more efficiently

1.2: THESIS ORGANIZATION:

- Chapter 2 :It describes the various applications of wireless under water communication
- Chapter 3 : The effect of the underwater environment on RF, optical and acoustic waves for UWC is described in this chapter.
- Chapter 4 : It describes about the architecture of UWA modem and details about the transmitter design.
- Chapter 5: Implementation of each module of Transmitter using IP core generator and FDA Tool is discussed and the integrated system of these modules is defined in this chapter. Simulation Results of the Transmitter section is also given in this chapter
- Chapter 6 : It describes about the Receiver section of UWA modem.
- Chapter 7 : Problem faced ,conclusion and Future work are given.

Chapter 2
Motivating Applications

A few applications are described in this chapter that motivates the need for a low-cost underwater acoustic modem, including applications involving exploration of Oceans and marine life to support the biodiversity, Underwater information collection for ocean mapping, Disaster prevention and assistance by measuring seismic activity, Environmental protection by monitoring pollution, Military applications. We describe the application and its socio-scientific impact and describe how a low-cost underwater acoustic modem can improve the application for further scientific advancement. We are summarizing the common requirements of these applications.

2.1. Oceans and marine life exploration :

From the ecological and economic point of view **,**the marine life exploration has a great importance. Unfortunately, they are under stress due to increasing temperature and acidity of the oceans,and heightened incidence of disease. Because of the complexity of the marine ecosystems, there is an incomplete understanding of the processes that collectively determine their structure, function and dynamics. Fundamental efforts to understand this ecosystems is on the basis of observing the environmental factors such as water temperature, salinity and bio-optical variables. The ability to perform real-time, adaptive ecological experiments would represent a significant advance in ecological sensing.As underwater cabling requires extensive environmental permitting and canbe damaged easily, a wireless network implementation is preferable.

2.2. Ocean mapping : The surface area of the Earth is dominated by the ocean basins. Ocean crust is the most dynamic part of the Earth-encompassing 70% of Earth's surface area.Using advanced under water communication we can locate the under water mountains,trenches, mid-ocean ridges**.**The ocean floor mapping will help in navigation,locating the marine habitats,also beneficial for many industries.

2.3. Disaster prevention : Disaster prevention and assistance by measuring seismic activity, tsunamis scan andwarning, study the effects of submarine earthquakes.

2.4. Military applications : Military applications by improving the coastal surveillance, defense systems, intrusion detection systems and submarine communications.

2.6.Summary : This chapter described a few applications that motivate the need for a low-cost underwater modem, including applications involving defence,controlling environmental parameters and disaster prevention.A low-cost underwater modem requires :

- low data rates
- moderate transmission ranges (< 500m)
- shallow deployment depths (< 100 m)

Chapter 3
Comparison or RF, Optical and Acoustic Underwater Communication

Present underwater communication systems involve the transmission of information in the form of radio frequency (RF) waves, optical waves, or acoustic waves. Each of these techniques has advantages and limitations. This chapter explores the effect of the underwater environment on RF, optical and acoustic waves.

3.1 Radio Frequency Waves:

Radio frequency waves are electromagnetic waves in the frequency band below 300GHz. An electromagnetic wave is a having a frequency within the electromagnetic spectrum as shown in (Figure 3.1) and propagated as a periodic disturbance of the electromagnetic field when an electric charge oscillates or accelerates . Due to the highly conducting nature of salt water, many underwater RF systems have been developed. The effect of conductivity, wavelength on RF waves is discussed in this section.

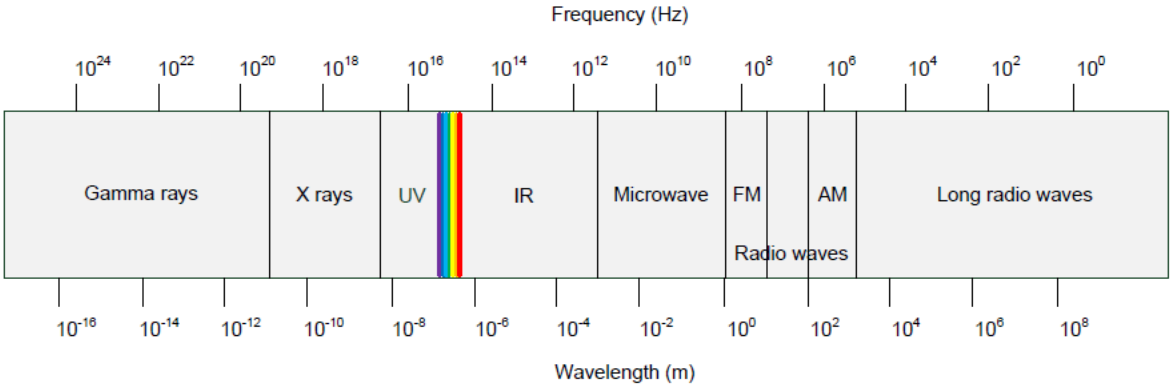


Fig-3.1 Electromagnetic Spectrum

3.1.1 Conductivity:

Pure water is an insulator, but in its natural state, water contains dissolved salts and other matter, so it behaves like a partial conductor. The water's conductivity increases, the attenuation of radio signals becomes more. Propagating waves continually cycle energy between the electric and magnetic fields, hence conduction leads to strong attenuation of electromagnetic propagating waves . Sea water has a high salt content and thus high conductivity(2-8 Siemens/meter (S/m)) .Average conductivity of sea water is 4 S/m whereas conductivity of fresh water is in the order of

a few mS/m .With the increase in conductivity and increase in frequency, Attenuation of radio waves in water increases. It can be calculated from the following formula.

$$\alpha = 0.0173\sqrt{f\sigma}$$

Where f is the frequency in Hertz, σ is the conductivity in S/m and α is attenuation in dB/meter,. Figure 3.2 shows attenuation as a function of frequency for sea water (4S/m) and freshwater.

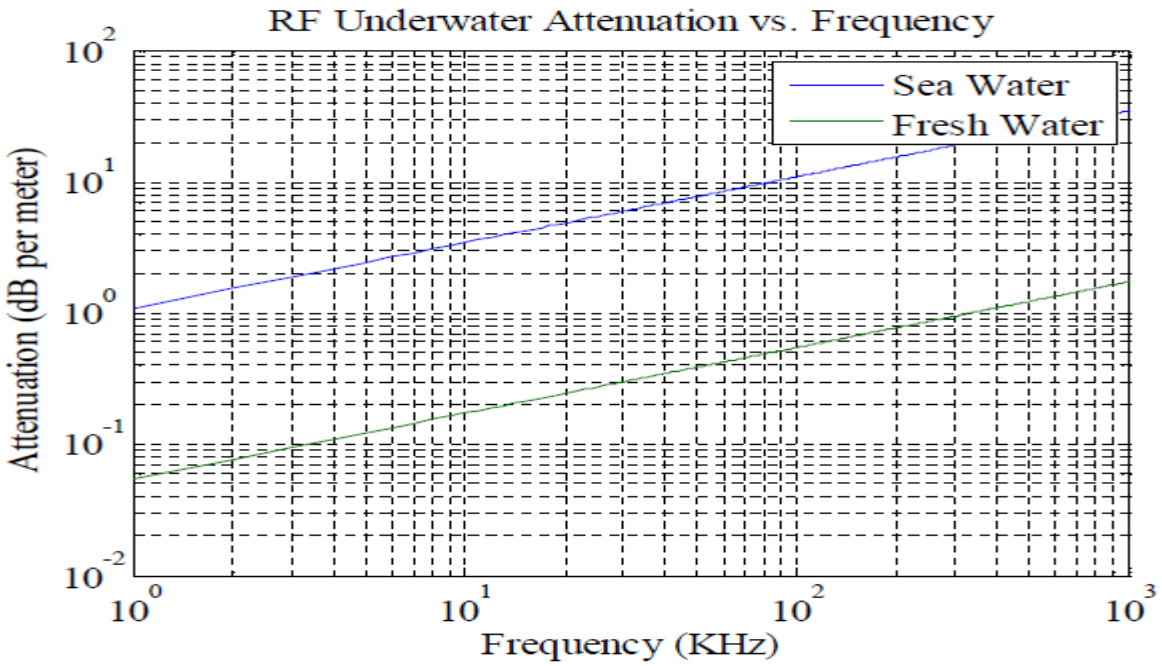


Figure 3.2: **RF Attenuation vs. Frequency in Fresh and Sea Water**

3.1.2 Wavelength: Wavelength in water is calculated from the following formula.

$$\lambda = 1000\sqrt{10/(f\sigma)}$$

Where f is the frequency in Hz, and σ is the conductivity in S/m. Figure 3.3 plots wavelength vs frequency in air, sea water (with conductivity 4 S/m), and fresh water (with conductivity 0.01 S/m).A signal's wavelength in air is considerably reduced underwater (especially in saltwater) .

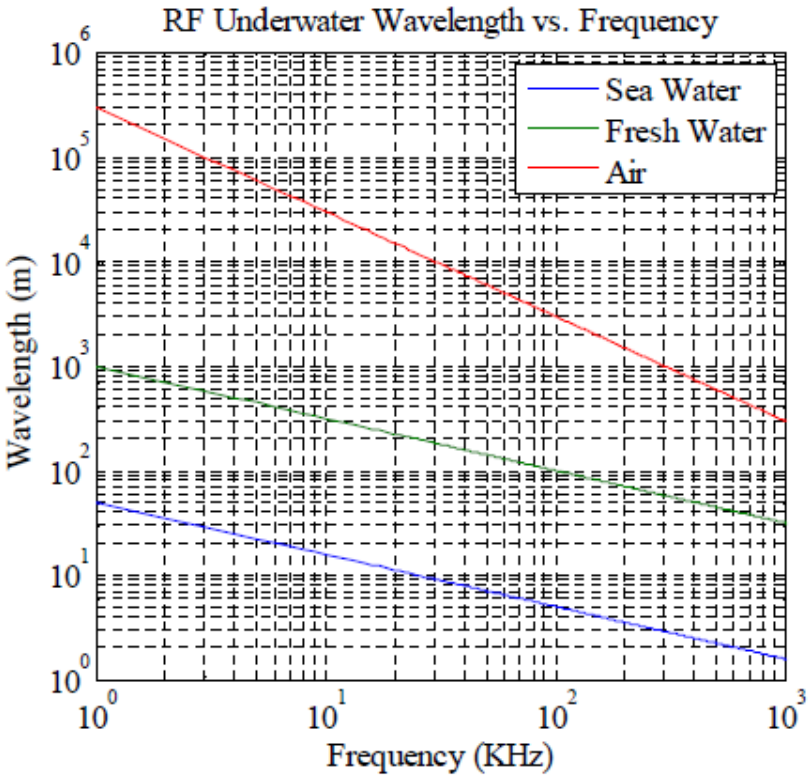


Figure 3.3: **RF Wavelength vs. Frequency in Sea Water, Fresh Water, and Air**

Table 3.1, shows the possible rates and ranges of the Wireless Fibre Systems RF modems in both sea and fresh water and their potential applications.

Table 3.1: Rates, Ranges, and Uses of Wireless Fibre Systems RF Modems

Range	**< 1m**	**10m**	**50m**	**200m**	**2km**	**10km**
RF (Sea Water)	100 Mbps	100 Kbps	6 Kbps	100 bps	1 bps	1 bps
RF (Fresh Water)	100 Mbps	1 Mbps	100 Kbps	1 Kbps	10 bps	1 bps
Applications	-AUV docking -Wireless connectors	-AUV data download -Diver Comm	-Networking -Diver Comm	-Networking -AUV Control -Diver Comm	-Deep water Telemetry	-Deep water Telemetry

3.2 Optical Waves:

Optical waves are EM waves having wavelengths between 400nm and 700nm . Due to their very short wavelength, high frequency, and high spee,optical waves offer the possibility for very high speed communication under water (up to 1Gbps). However, optical waves used as wireless communication carriers are generally limited to very short distances because of severe water absorption at the optical frequency band and strong backscatter from suspended particles . The section discusses the basic physics of optical waves underwater.

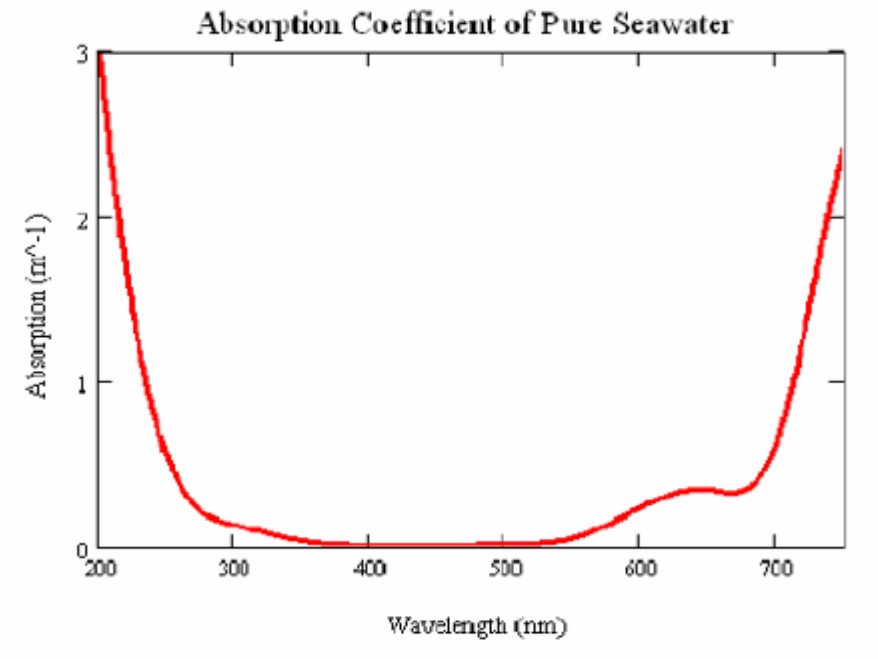


Fig-3.4

3.3 Acoustic Waves:

Acoustic waves are caused from variations of pressure in a medium. Due to the greater density of water, the velocity is 4-5 times faster in water than in air but 5 times slower than electromagnetic waves . Acoustic waves have been widely used in underwater communication systems due to the relatively low attenuation of sound in water. However, acoustic waves can be affected by absorption loss, severe multipath, spreading loss, and ambient noise which is discussed in this section.

3.3.1 Absorption Loss:

The absorption of acoustic waves in sea water depends on the temperature,salinity, and acidity of the sea water as well as the frequency of the sound wave.The absorptive loss for acoustic wave propagation can be expressed as e^(α(f)d) .
Where d is the propagation distance and α(f) is the absorption coefficient of frequency f.

$$\alpha(f) = \frac{A_1 P_1 f_1 f^2}{f_1^2 + f^2} + \frac{A_2 P_2 f_2 f^2}{f_2^2 + f^2} + A_3 P_3 f^2$$

Since α(f) increases with frequency, high frequency waves will be considerably attenuated within a short distance as compared to low frequency acoustic waves .

3.3.2 Spreading Loss :

The energy radiated from an omni-directional source spreads spherically. Since all the energy is not directed in a single direction ,so there is much loss of energy. This is called spreading loss. The spreading loss is independent of frequency. In deep water, the power loss caused by spreading is proportional to the square of the distance. In shallow water, sound is bounded by the surface and the sea floor resulting in cylindrical spreading. In this case, sound power loss increases linearly with the distance from the source.

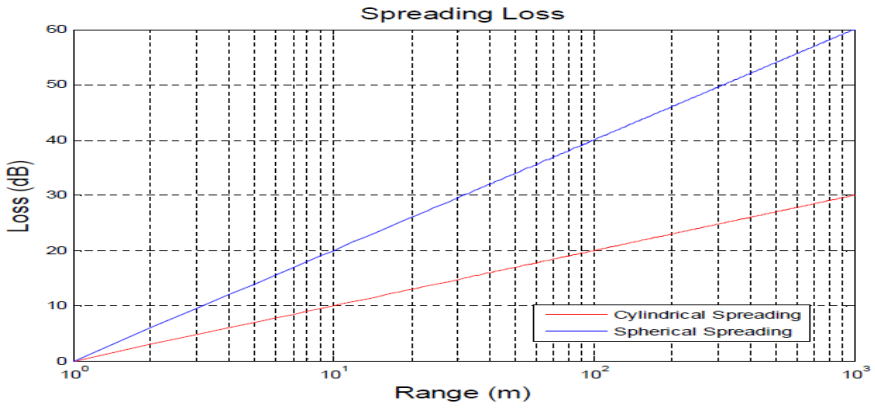


Fig-3.5

3.3.3 Noise:

Ambient noise is defined as the noise associated with the background generated by unidentified sources.Underwater sound is generated by a variety of natural and man-made sources including breaking waves, rain, marinelife, bubbles, surface-ships, and military sonars. The primary source of ambient noise can be categorized by the frequency of sound. In the frequency range of 20-500 Hz, ambient noise is primarily generated by distant shipping, in the range 500-100,000 Hz ambient noise is mostly due to spray and bubbles associated with breaking waves.

3.3.4 Multipath

There exist multiple paths from the transmitter to receiver. Two fundamental mechanisms of multipath formation are reflection at the boundaries (bottom, surface and any objects in the water), and ray bending .Multipath due to reflections of the surface and bottom is common in shallow waters whereas multipath due to ray bending is common in deep waters. Understanding of these mechanisms is based on the theory and models of sound propagation.

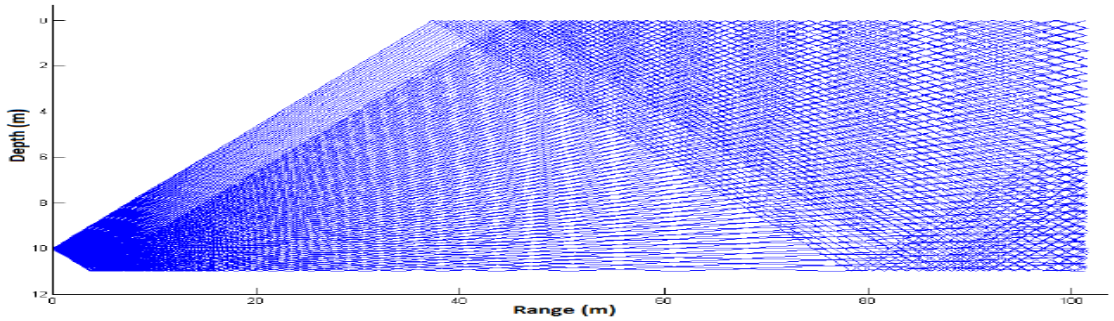


Fig-3.6

Table 3.2: Comparison or RF, optical and acoustic communication underwater

	RF	**Optical**	**Acoustic**
Wave speed (m/s)	$\sim$ 3E8	$\sim$ 3E8	$\sim$ 1.5E3
Data rate	$<$ 10 Mbps	$<$1 Gbps	$<$ 100 Kbps
Effective range	$\sim$ 1-100 m	$\sim$ 1-100 m	$\sim$ km
Power Loss	$\sim$ 28 dB/1km/100MHz	$\propto$ turbidity	$>$ 0.1 dB/m/Hz
Frequency Band	$\sim$ MHz	$\sim 10^{14} - 10^{15}$ Hz	$\sim$ kHz
Major hurdles	power limited	environment limited	bandwidth limited interference-limited

3.4 Summary

In this chapter the effect of the underwater environment on RF,optical and acoustic waves is discussed. Table 3.2 summarizes and compares the characteristics of radio, optical, and acoustic communication underwater. All three physical wave fields have their own advantages and limitations for acting as an underwater wireless communications carrier.

Chapter 4

System Design Of UWA Modem

4.1 System Architecture

Figure 4.1 shows the block diagram of the underwater communication system . The system can be divided in three domains i.e. Digital domain ,Interfacing Domain and Analog domain as shown.

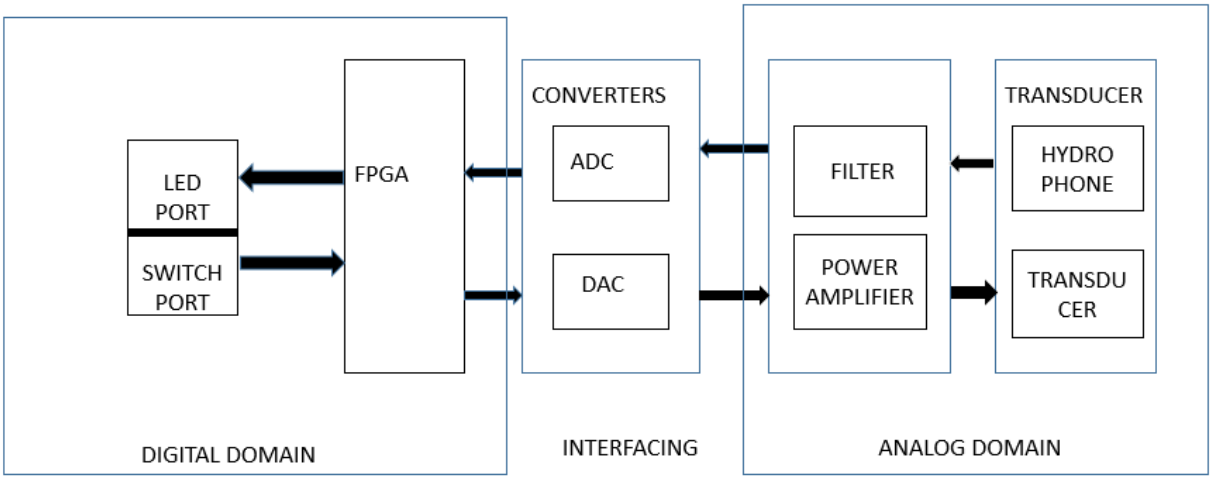


Fig 4.1 (representative block diagram of UWA modem)

From the switch port we are sending the signal which is processed in the fpga and converted to analog signal using the Digital to analog converter then it is amplified before feeding to the transducer. Then the electrical signal is converted to sound signal and transmitted through the aquatic channel. Now the transmitted signal is received by the hydrophone and it is filtered to remove the noise ,then it is converted to digital signal for further processing in fpga and retrival of the sent data and sent to led port.

4.2. TRANSMITTER DESIGN:

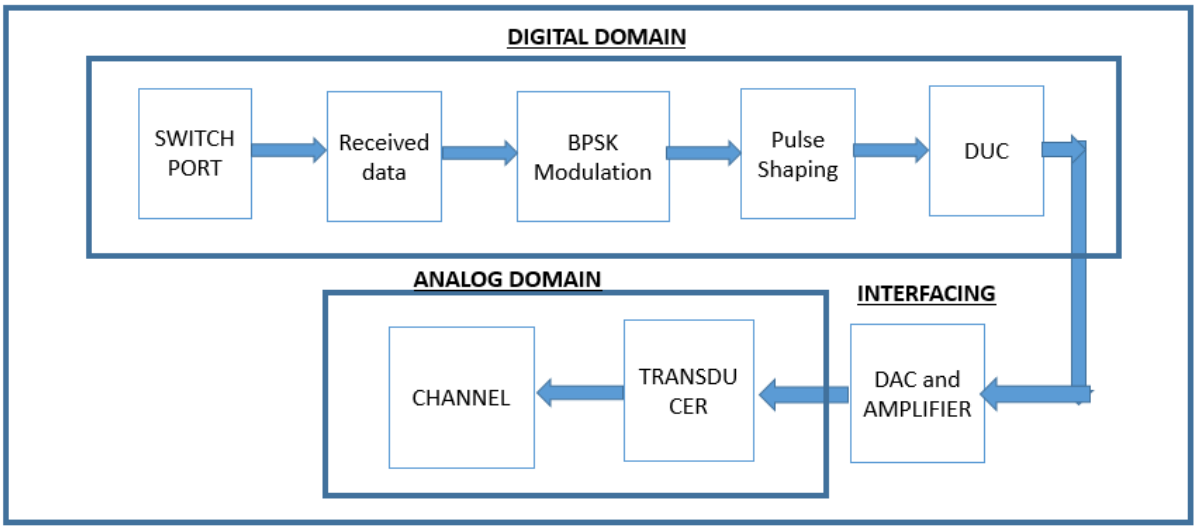


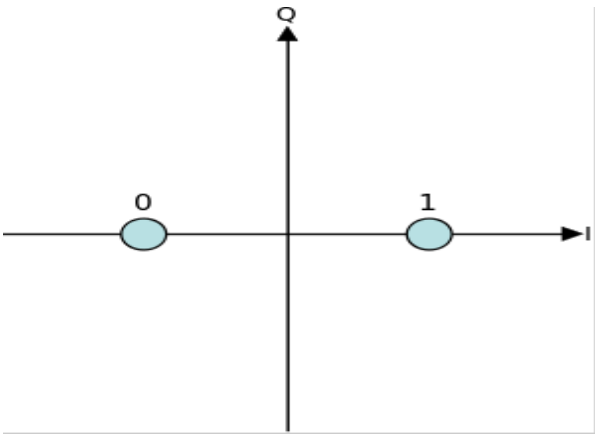
FIG-4.2.1 (Block diagram of transmitter)

4.2.1 Data Transmition:

Data is given from the switch port of the fpga.The data rate is 500 bps . The width of each input data is 1bit. Now the data is processed in the next modules for further processing.

4.2.2 Digital Modulation:

various modulation schemes have been implemented in existing commercial and research modems. These schemes all attempt to combat the performance limitations induced by the underwater acoustic channel while at the same time improving the bandwidth efficiency and bit rate as much as possible. This section describes the characteristics of some of these schemes and reasons for our selection of the use of BPSK for our modem design.BPSK is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180°. This modulation is the most robust of all the PSKs since it has the improved ber curve as shown in fig(4.2.2b).As our application requires low data rate ,BPSK is chosen as the suitable modulation scheme. The bpsk modulation is done by writing a vhdl code in which '1' is represented by "0110" and '0' is represented by "1001" i.e. the 1's complement of '0110'. So the hamming distance between the two bits is now increased and the probability of corruption of data by noise is less.



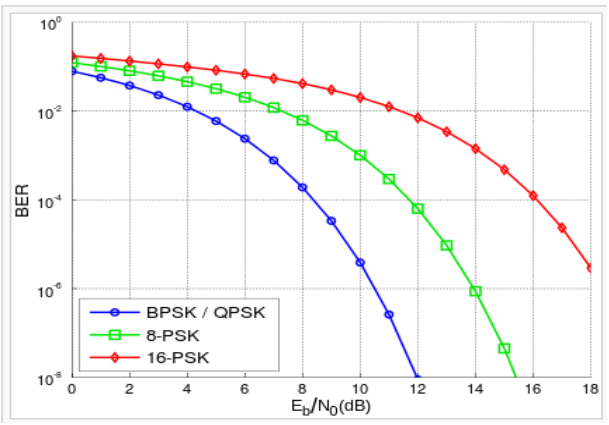


Fig-4.2.2a (Constellation diagram of BPSK) **Fig-4.2.2b**

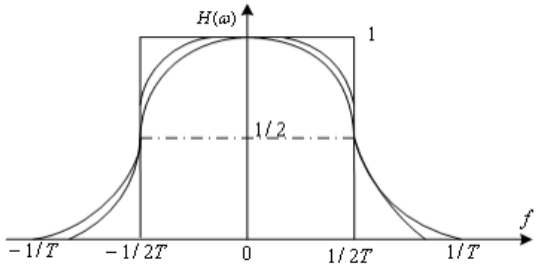
4.2.3 Pulse Shaping:

In **pulse shaping** the waveform of transmitted pulses are changed to make the transmitted signal better suited to the communication channel by limiting the effective transmission bandwidth. Pulse shaping is used for the removal of Inter symbol interference. When we are transmitting a rectangular pulse through a channel , the bandwidth of received signal is reduced because of the band limiting nature of the channel. So in time domain the received pulse is expanded and leads to ISI. There are different techniques for pulse shaping e.g. using sinc filter RRC filter and Gaussian filter .. etc.We have implemented RRC filter for the pulse shaping purpose. The pulse shaped signal is given by the following equation.

$$H(f)=\begin{cases} T & \left(0 \le |f| \le \frac{1-\beta}{2T}\right) \\ \frac{T}{2}\left\{1+\cos\left[\frac{\pi T}{\beta}\left(|f|-\frac{1-\beta}{2T}\right)\right]\right. & \left(\frac{1-\beta}{2T} \le |f| \le \frac{1+\beta}{2T}\right) \\ 0 & \left(|f| > \frac{1+\beta}{2T}\right) \end{cases}$$

$$h(t)=\frac{\sin \pi t/T}{\pi t/T}\,\frac{\cos \pi\beta t/T}{1-(4\beta^2 t^2/T^2)}$$

Frequency response and pulse response of rrc filter is given in the following figures.



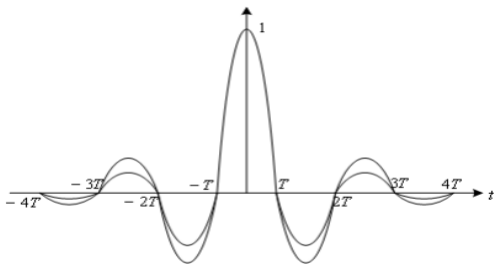


Fig-4.2.3a Fig-4.2.3b

4.2.4 DUC (Digital Up Converter):

The Digital Up Converter (DUC) is the most fundamental building blocks in wireless communication systems for converting the sample rate of signals. when a signal is translated from baseband to intermediate frequency (IF) band Digital up conversion is required. DUCs typically include frequency shifting using mixers, in addition to sampling rate conversion.

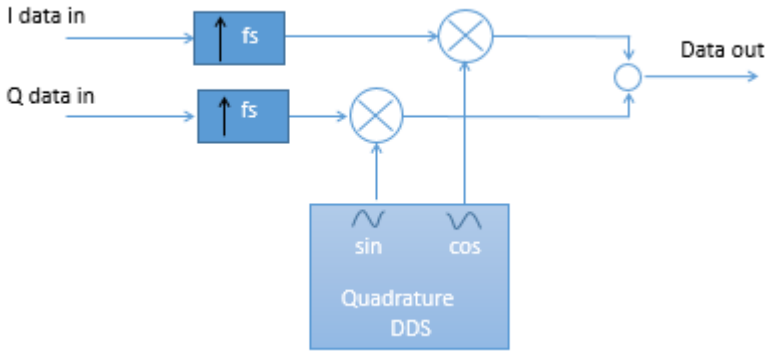


Fig-4.2.4 (Block diagram of DUC)

For digital up conversion , the data should be upsampled first then it is passed through the lowpass filter to remove the image frequencies. Then the baseband signal is transformed to bandpass signal using mixer and direct digital synthesizer.

4.2.4.1: Interpolation :

Interpolation is otherwise known as upsampling. It is performed on a sequence of samples to produce an approximation of the sequence which can be obtained by sampling the signal at a higher rate. The interpolation factor is defined as the ratio of the output rate to the input rate.

L=output rate / input rate

Interpolators can be implemented by using FIR filter or CIC filter. If the conversion ratio is low then using FIR filter is used for interpolation. For high conversion ratio, implementation of CIC filter is efficient as it requires less number of computations. Then the output of interpolator is passed through lowpass filter to remove the image frequency.

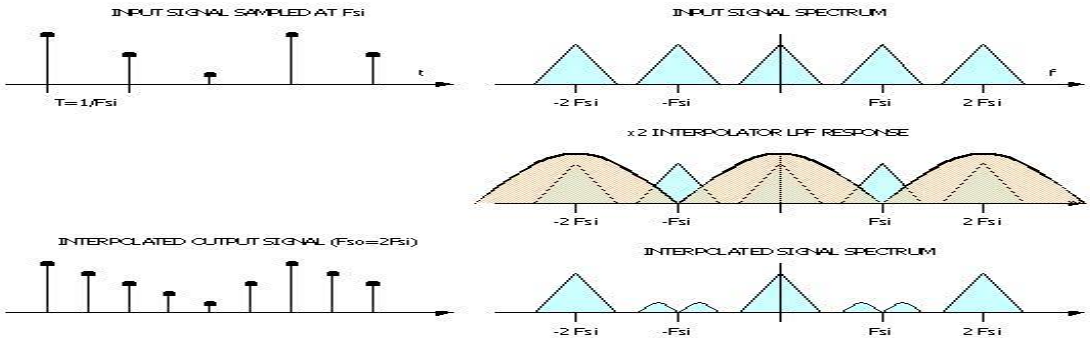


Fig-4.2.4.1

4.2.4.2 Frequency Translation:

To shift the up-sampled baseband data to passband , the baseband data is mixed with a carrier signal of higher frequency using a mixer and DDS(Direct Digital Synthesizer). DDS is used for generation of sine and cosine wave of higher frequency. Then the output of mixer is passed through lowpass filter to remove the undesired heterodyned frequency.

4.3. DAC(Digital to Analog Conversion) and Power amplifier

DAC is used to convert the digital signal to analog signal before transmitting it through the channel. Then the analog signal is amplified to increase the power of the signal.The DAC used in our system has 8-bit resolution , operational frequency range is upto 30MHz.

4.4. Transducer

Piezoelectric materials like ceramic,polymers and composites are mainly used for designing Underwater transducers.There are two types of ultrasonic transducers .One is Projector which converts the electrical energy into ultrasonic sound and other one is Hydrophone which converts the ultrasonic sound into electrical energy. There are Transducers of different architecture (spherical and piston type.. etc).Piezoelectric ultrasound transducers generate high frequency.The piston type transducers project the sound in one direction. So for the high directional property we are using a piston type transducer that works at frequency in 1MHz range.

Fig-4.4(Ultrasonic Projector)

Chapter 5

Implementation Of Transmitter

5.1 Software used:

ISE 14.7 and MATLAB 13a are used for designing the different modules of the system for processing of the data,that will be discussed in details in next chapter.

Hardware used :

a. **NEXYS 4,AIRTEX 7** board is used because of the following specifications.

- 15,850 logic slices
- 15850 * four 6-input LUTs
- 15850 * 8 flip-flops
- fast block RAM : 4,860 Kbits
- 240 DSP slices
- Internal clock speeds upto 450MHz

b. **DIGILENT PMOD DA1** :
Digital To Analog Module Converter Board having two AD7303 8-bit D/A converter in one package.

- Low power, single supply operation. Voltage range for operation :2.7 V to 5.5 V supply and consumes typically 15 mW at 5.5 V.
- Internal or external reference capability.
- High speed operation with clock rates up to 30 MHz.

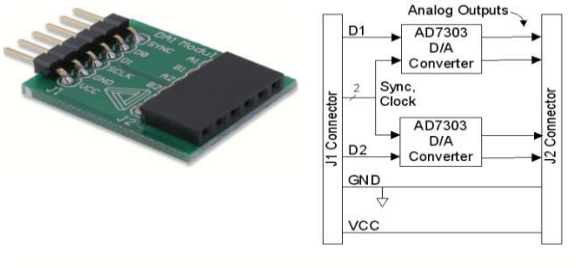


Fig-5.1

5.2: IMPLEMENTATION OF EACH MODULE OF TRANSMITTER:

We are using IP CORE GENERATOR (Xilinx)technique for the implementation of filters and different module like DDS. FDA TOOL of MATLAB 13a is used for designing the filters and generation of coefficient file which will be used in IP Core generation of filters.

5.2.1: Transmitted data and BPSK Modulation:

1 bit Data is transmitted from the switch port of nexys 4 board at a rate of 500bps and it is modulated as described in the section 4.2.2. A small VHDL code is written for the implementation of BPSK Modulation. Now the data rate is changed to 4 kbps.

5.2.2: RRC Pulse shaping :

Both FDA Tool and IP Core generator are used for the implementation of RRC pulse shaping filter as described below. For designing a filter, the important parameters like filter length,filter coefficients,total number of required logic elements should be known to reduce the complexity of system. FDA Tool of matlab provides a Graphical User Interface (GUI) used to set filter specifications and visualize the filter responses. Now the coefficient file(.coe) is generated which will be used in generating the IP of filter. The use of FDA Tool is described below.

- Open FDA Tool.
- Set the parameters (Response type, Filter Order, Frequency and Magnitude specification)
- Click on Analysis tab which has options for different filter responses. e.g. (Magnituderesponse, Phase Response, Group Delay and Phase delay,Impulse Response,Step response,Polezeroplot,Filter information.

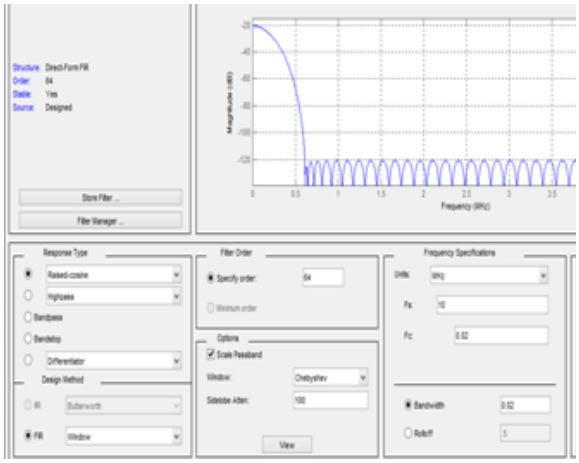


Fig-5.2.2a

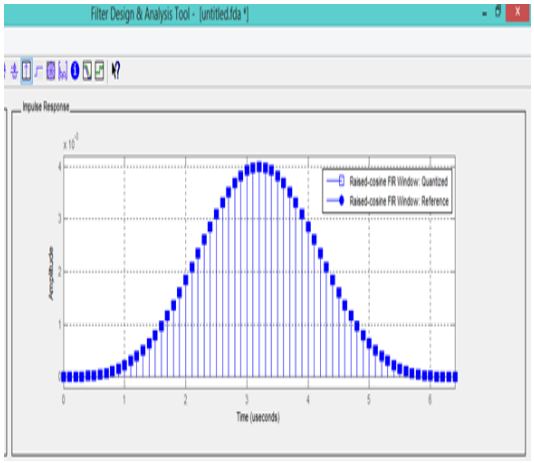


Fig-5.2.2b

5.2.2.1: Generation of Co-efficient file

Step1 :Edit>convert structure (Direct Fir)
Step2 :Filter arithmetic > (Fixed point , Fullprecision)>Word length
Step3 : Target > GENERATE COE FILE

Once the coefficient file is generated ,then Using ISE 14.7 the IP for RRC pulse shaping is generated using FIR filter.

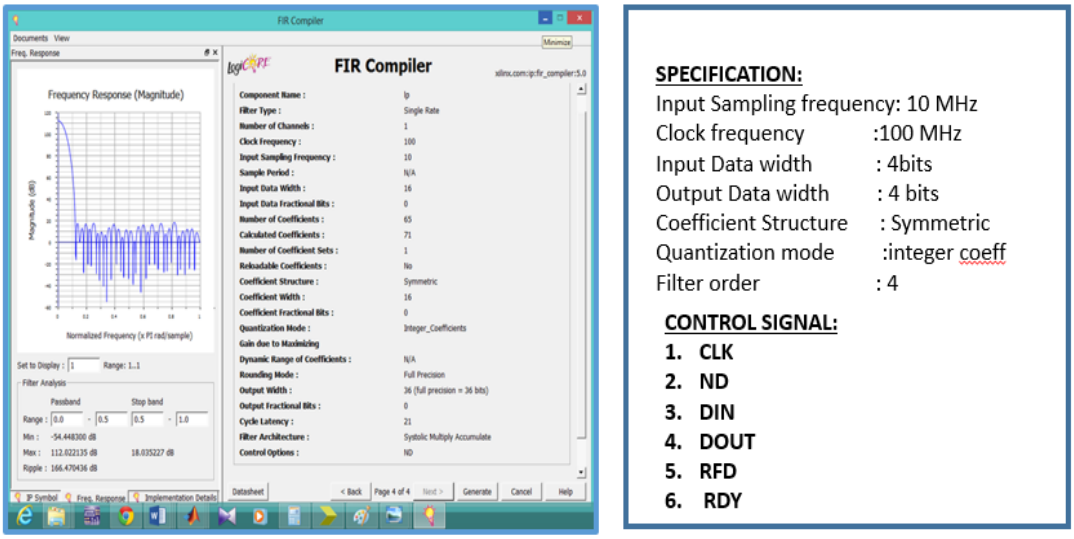


Fig-5.2.2b (IP for RRC filter)

5.2.3 : INTERPOLATION OF PULSE SHAPED SIGNAL

The IP is generated for interpolation filter by following the same same procedure as desribed in the previous section **.** Here we are using a multirate filter for interpolation with a conversion ratio 2. So we are inserting 2 intepolated samples inbetween two given samples.So now the data rate is 40 kbps (<100kbps for acoustic modem). The magnitude and impule response obtained from FDA tool is shown in fig -5.2.3a.

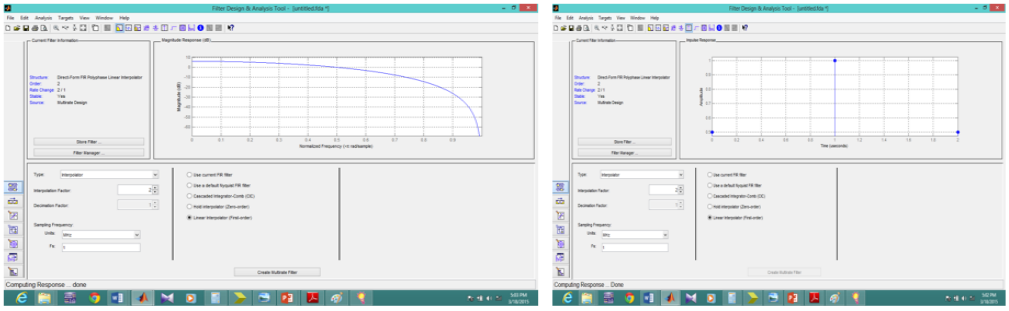


Fig-5.2.3a

5.2.4: IMPLEMENTATION OF LOW PASS FILTER :

Following the same steps the IP for low pass filter for removing the image frequencies is generated.

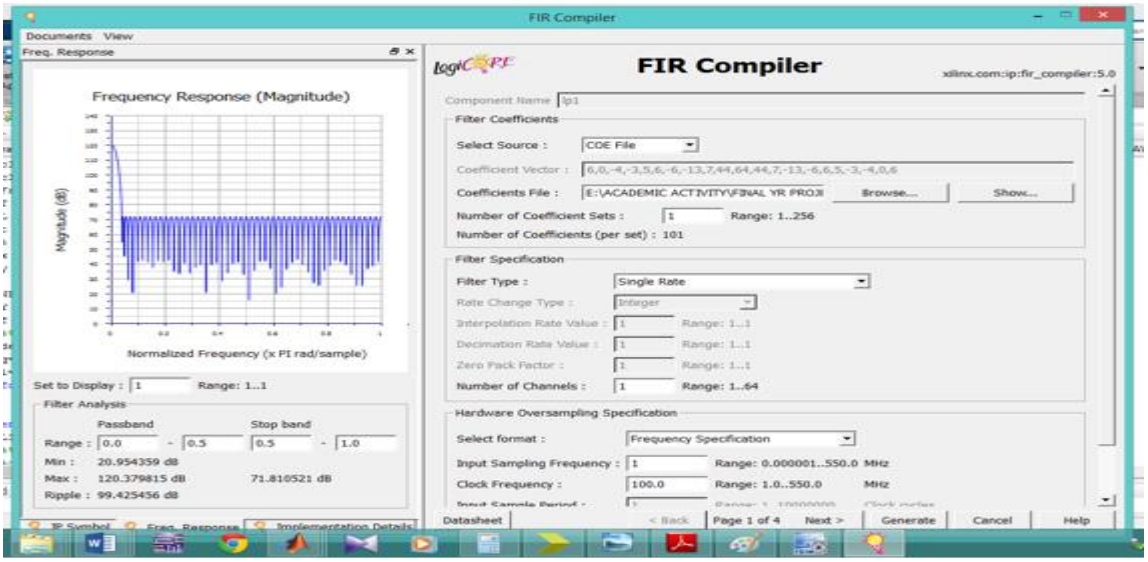


Fig-5.2.4

5.2.5 : IMPLEMENTATION OF DIRECT DIGITAL SYNTHESIZER(DDC):

DDS is used for generating signals(sine,cosine) of high frequency which is used in modulation as carrier frequency. The two basic components of DDS are phase generator and sine or cosine look up table. The integrator (D1 and A1) calculates a phase slope that is mapped to a sinusoid by the lookup table (T1). The quantizer Q1, accepts the high-precision phase angle and generates a lower precision representation of the angle denoted as in the figure. This value is presented to the address port which performs the mapping from phase-space to time.

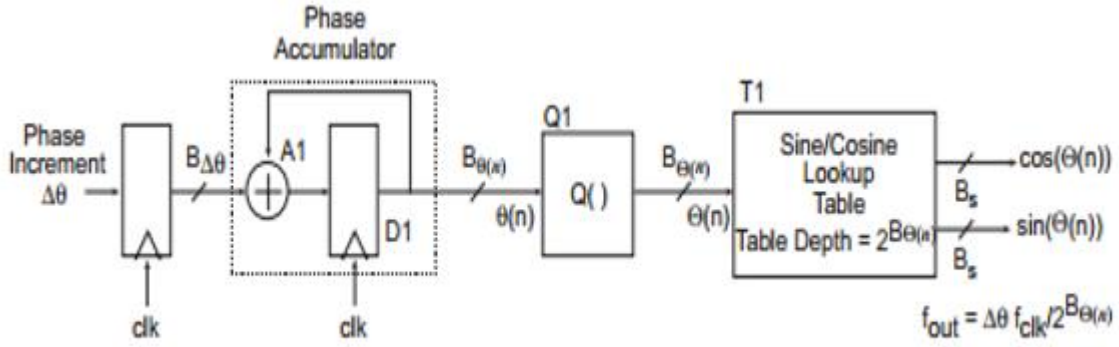


Fig-5.2.5a

Here phase increment is the input to the DDS ip .The output frequency is calculated using the following formulae.

Fout = Fclk . Δθ / 2^(Bθ(n))

Where Fout is the outputfrequency, Fclk is clock frequency of fpga, Δθ is phase increment as input and Bθ(n) is the phase width i.e. the number of bits.

In our system Fclk=100 MHz,B=12 bits, Δθ = 40 . The Fout is nearly 1MHz.

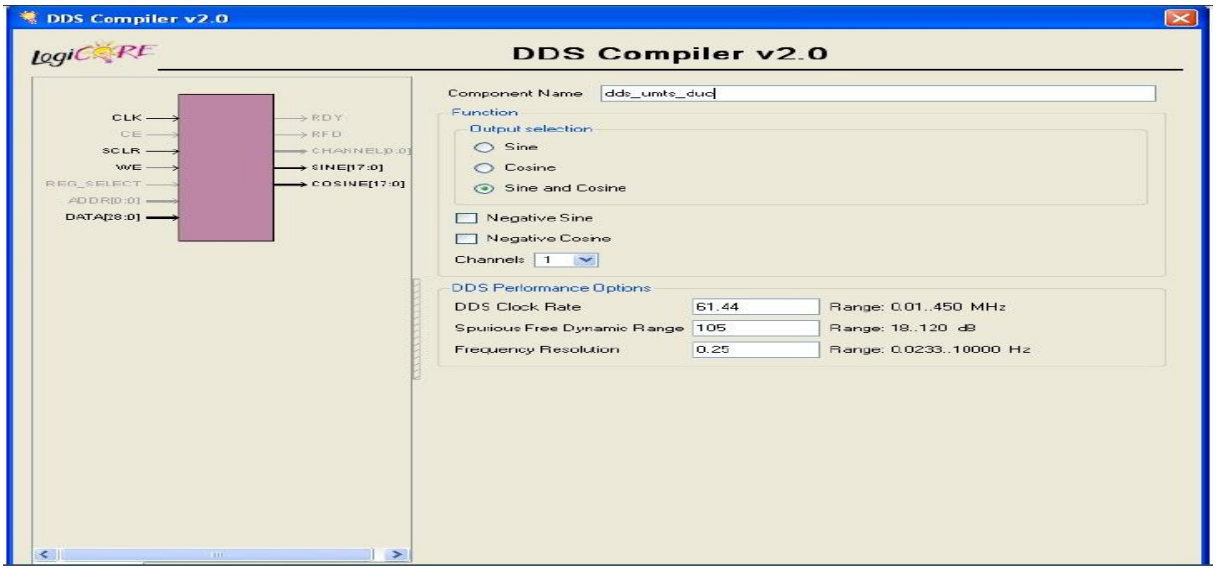


Fig-5.2.5a

5.2.6:IMPLEMENTATION OF MIXER:

Mixer is a complex multipler which generaates the heterodyned frequncies given into its input i.e. (f1 + f2) and (f1-f2).

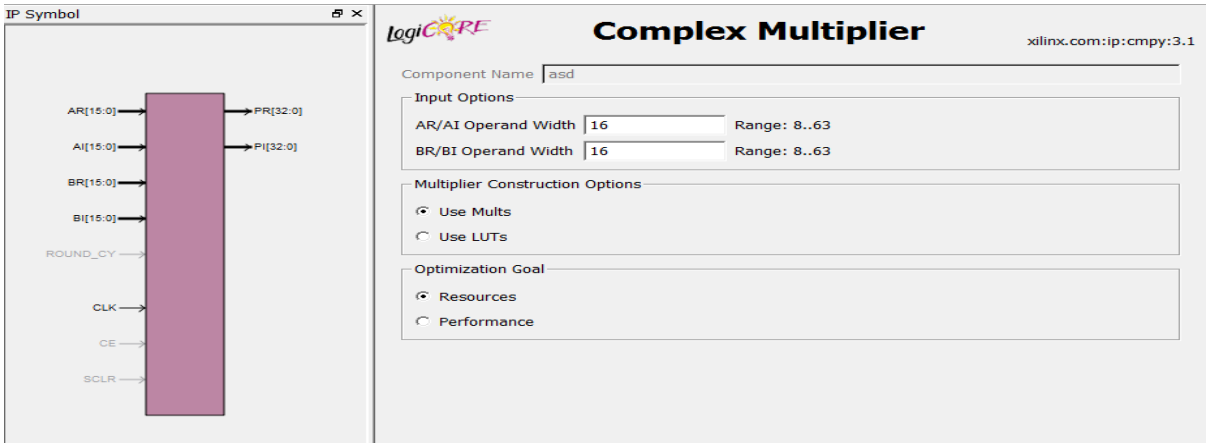


Fig-5.2.6

5.2.7: IMPLEMENTATION OF DAC:

Digilent PMOD DA1 module is used for DAC. The following figure shows interfacing signals for controlling the Digital to analog conversion. The state machine given below describes the controlled operation of DAC.

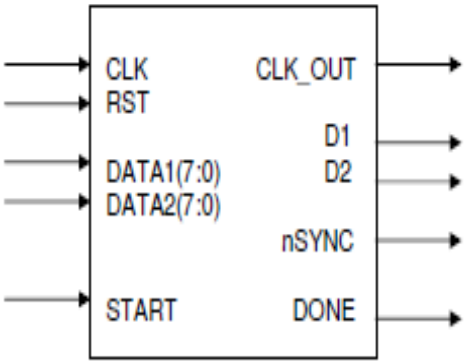


Fig-5.2.7a

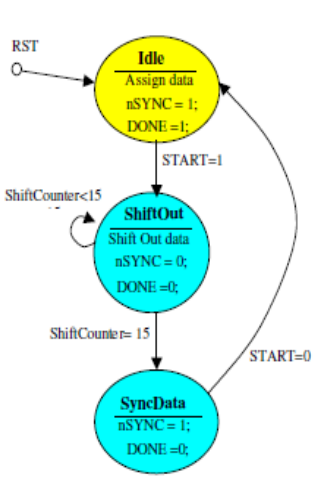


Fig-5.2.7b

The following figure shows the out put of DAC when a digital ramp signal is given to it.

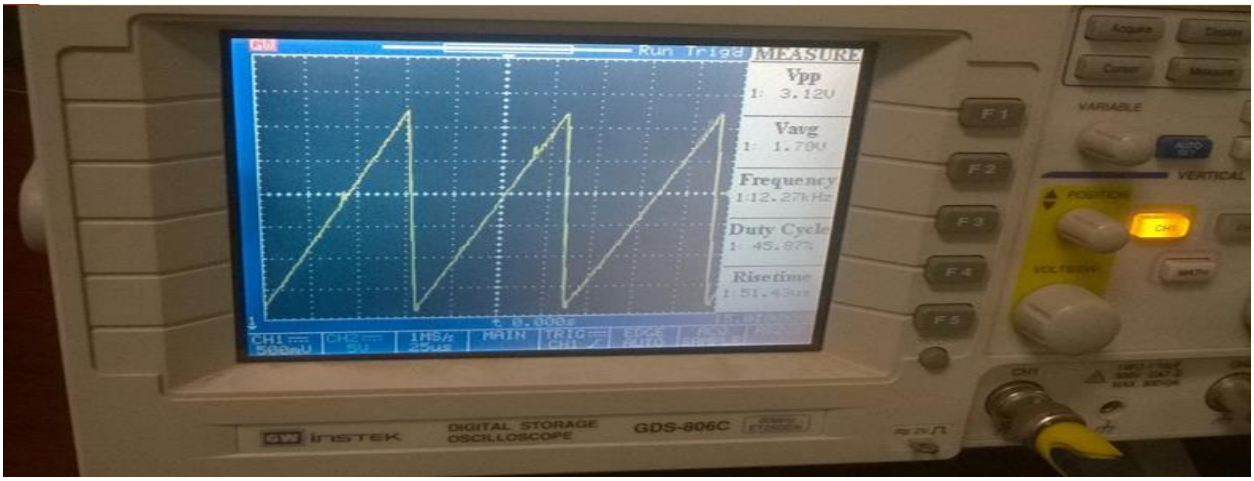


Fig-5.2.7c

5.3. INTEGRATION OF EACH MODULE OF TRANSMITTER

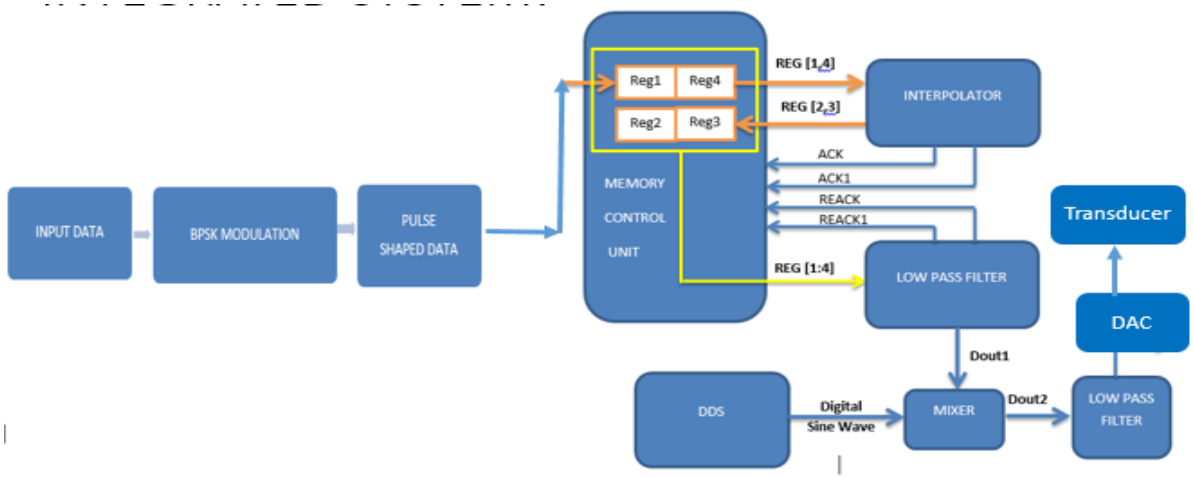


Fig-5.3(Integrated system)

The system is designed for under water communication with low data rate . The frequency of the input data is in the range of 16 kHz whereas the elementary blocks in the FPGA work at far higher frequencies in the range of 100 MHz. This high frequency of the system is set for fast operation the calculations and all operations without losing any data bits in the input. In the current implementation only the Digital Up-Converter is being generated. An extra memory blocks are designed to facilitate the synchronization between the processes of different modules.

- A stream of Data bit is given as input to the system. The frequency set is as low as 500Hz and the data is to be transmitted. The incoming data is bpsk modulated and pulse shaped then fed to interpolator. Two samples of RRC filtered data are stored in the registers 1 and 4. The registers are cleared after the interpolated output is fed to the Low Pass Filter.
- A memory unit consisting of four registers is designed. The register size is equivalent to the size of the data bits. The first and fourth registers were used to store the incoming data bits. This second and third registers store the output data of the interpolator. The arrangement of the registers for storing such specific data in the above defined specific manner is controlled by the memory control unit.
- The interpolator outputs the interpolated data between the two signals of a symbol. It generates two signals between the input signals. The frequency of the interpolator is set very high to mitigate any data loss. By various methods discussed for interpolating data using interpolation filters, we can easily generate the interpolated signals. Thus it helps in up-sampling of the data.
- Since the interpolator outputs only the interpolated data between the two input signals, so there is need to store both the input and output signals to sequentially feed into the low pass filter. The low pass filter smoothens the data thereby removing any unwanted image

frequencies of the signals. The four inputs from the registers are taken as the input for the low pass filter and the output is generated.

- This output is mixed with the DDS output with the help of a mixer to generate a frequency shifted output. The frequency shifts here from the baseband frequency to the intermediate frequency since the data would be transmitted over a long distance. The output from the DDS is a sine wave which is fed to the mixer. The mixer actually multiplies the output of the DDS with the output of the Low pass filter in the previous state.
- In the next stage the output is fed to the low pass filter for removing the presence of any image frequencies after the mixer stage. This signal generated from the low pass filter is further fed into a Digital-to-analog Converter (DAC). The final output of the system is analog . Then post DAC operations are done to remove undesired frequencies and fed to transducer which converts the electrical signal into sound signal which can be transmitted through the aquatic channel with less attenuation.

5.4. RESULTS :

5.4.1 Output of RRC Filter : The input to the RRC filter is of width 4 bit The order of RRC filter is 4. Each BPSK Modulated symbol is now represented by 4 samples. So the bit rate is now 8 kbps. The test bench of ISE 14.7 simulator is plotted in matlab.

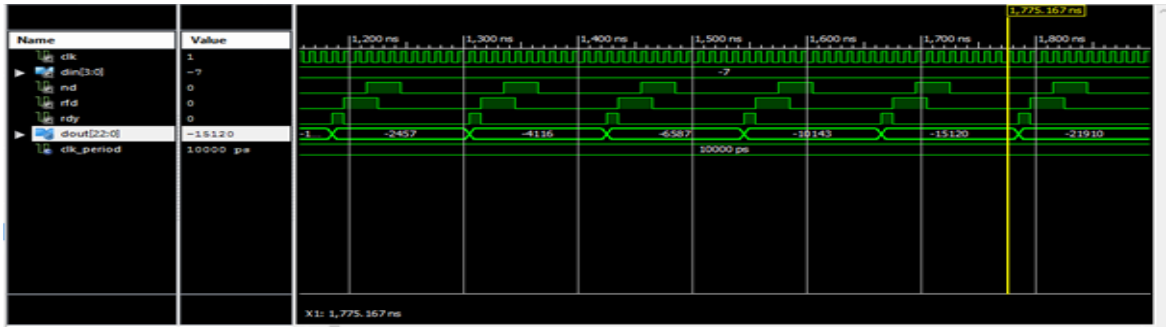


Fig 5.4a (Test bench of RRC filter implementation)

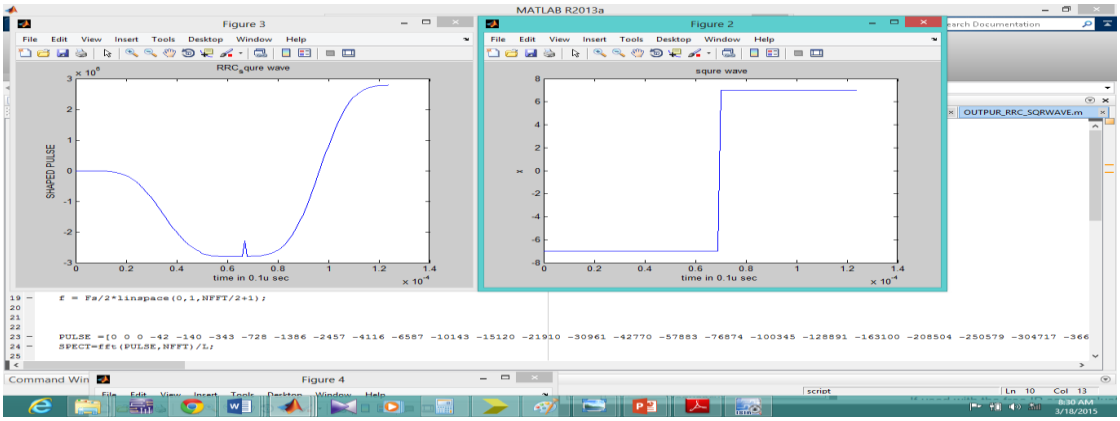


Fig 5.4b(Testbench output plotted in MATLAB)

5.4.2: OUTPUT OF INTERPOLATOR:

The output of RRC filter is given to the interpolator. The conversion ratio is 2 .So interpolator inserts two samples in between the two given input samples. So now the bit rate of input data is changed to 16 kbps.

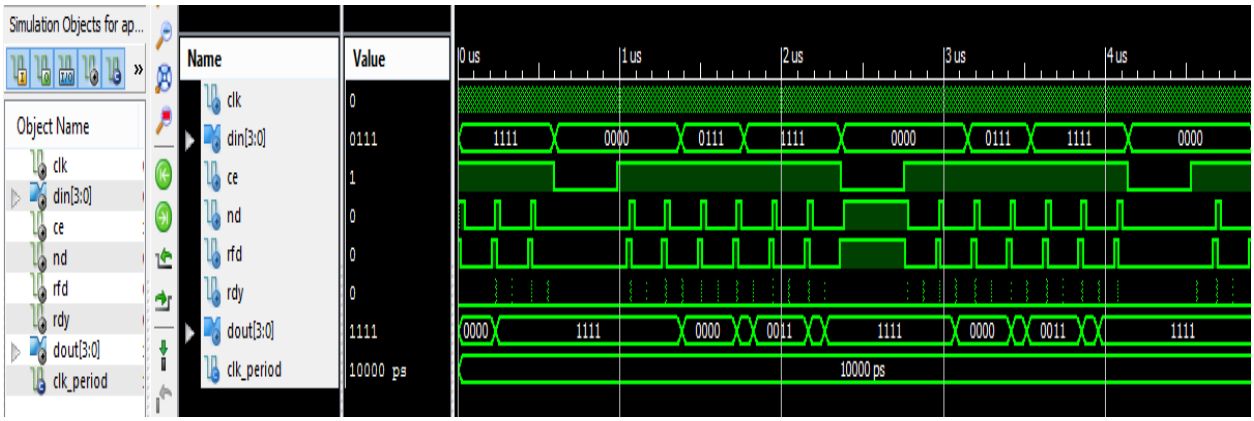


Fig 5.4c

5.4.3: OUTPUT OF LOWPASS:

To remove the image frequency the interpolated data is now passed through LOWPASS filter. The cutoff frequency of the designed filter is 20 KHz.To crosscheck the operation of lowpass filter IP a 20 KHz signal is given in the input and the output of test bench is plotted in matlab. The spectrum analysis done by Matlab shows that the filter is working properly.

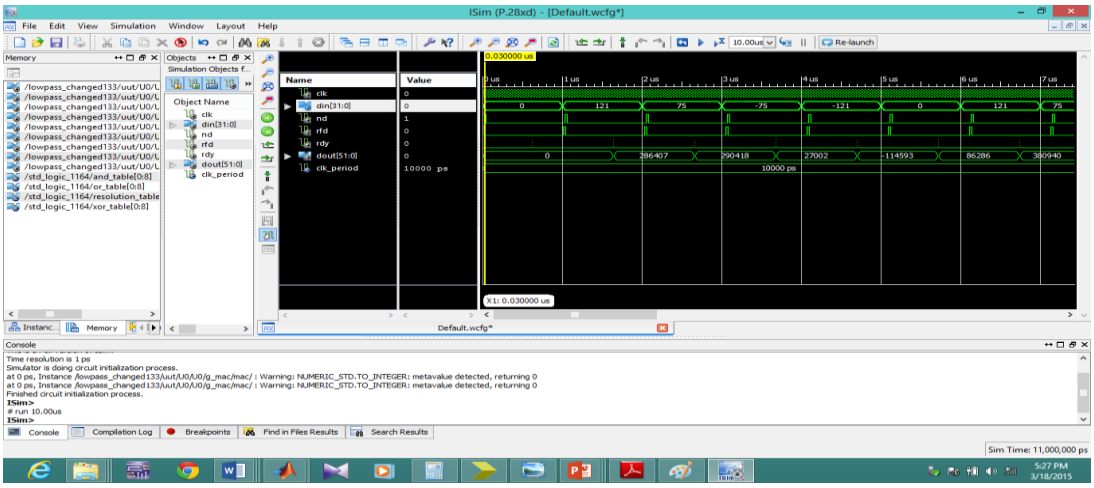


Fig 5.4d (Test bench of low pass filter)

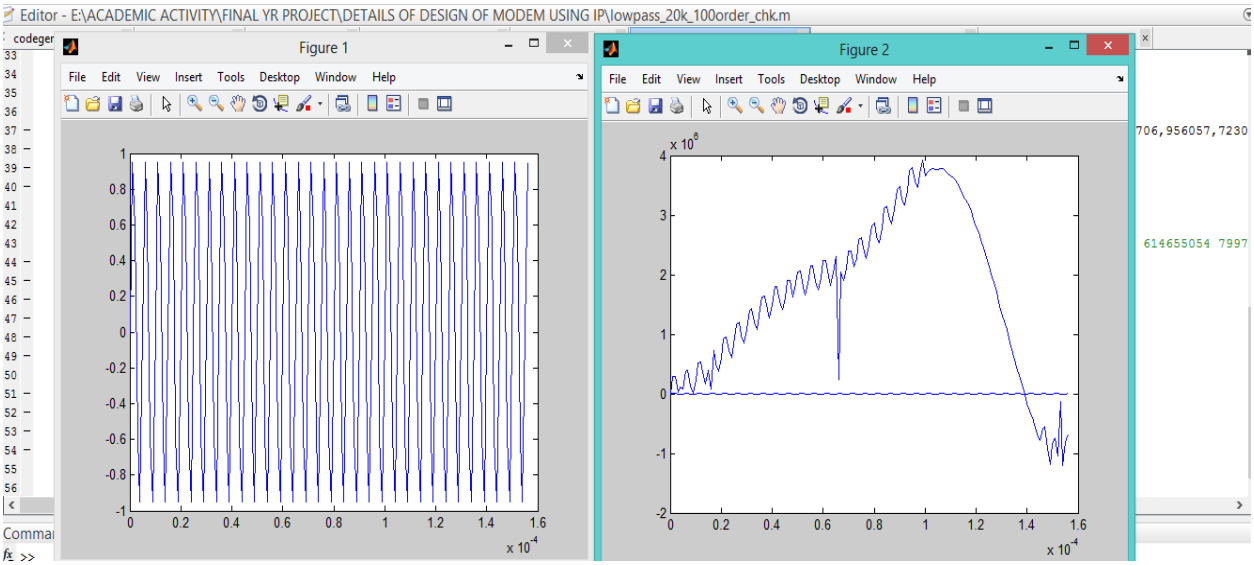


Fig 5.4e (input signal 20KHz)

Fig 5.4f(output signal of filter)

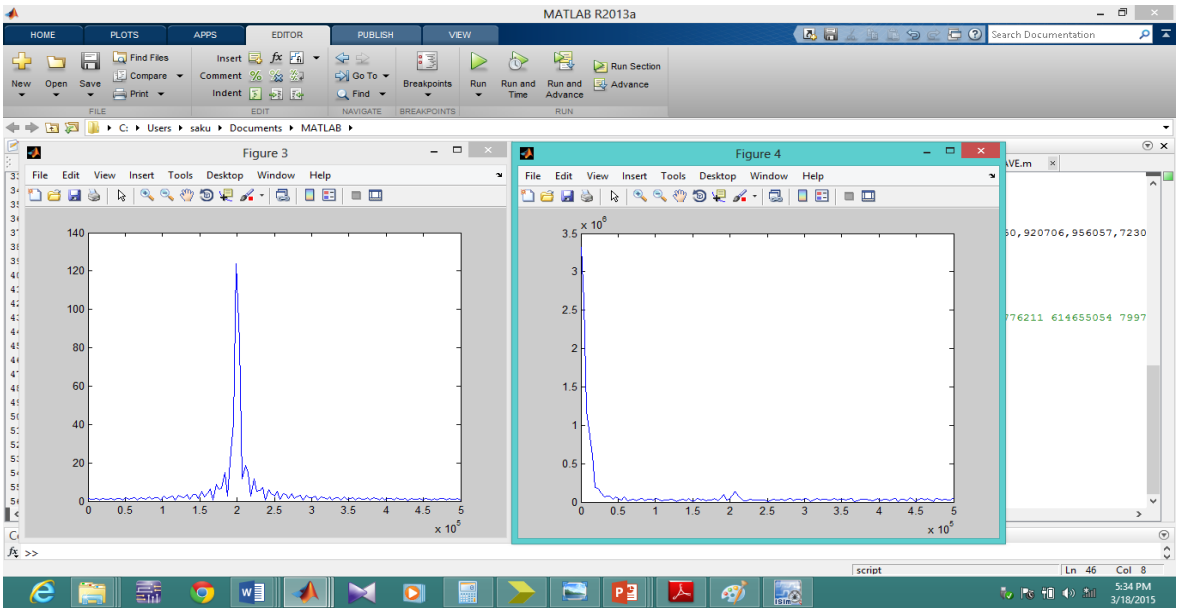


Fig 5.4g (spectrum of input signal)

Fig 5.4h(Spectrum of output signal)

5.4.4: OUTPUT OF DIRECT DIGITAL DYNTHESIZER:

DDS is generating a sine wave of frequency nearly equal to 1MHz.

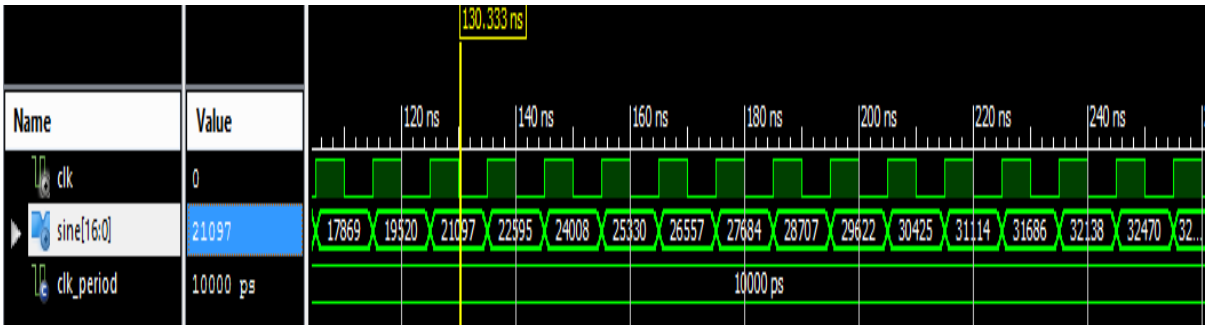


Fig-5.4.4

5.4.5: OUTPUT OF DAC:

For testing the module a ramp signal(digital) is given to the input of DAC.The following Output is obtained.

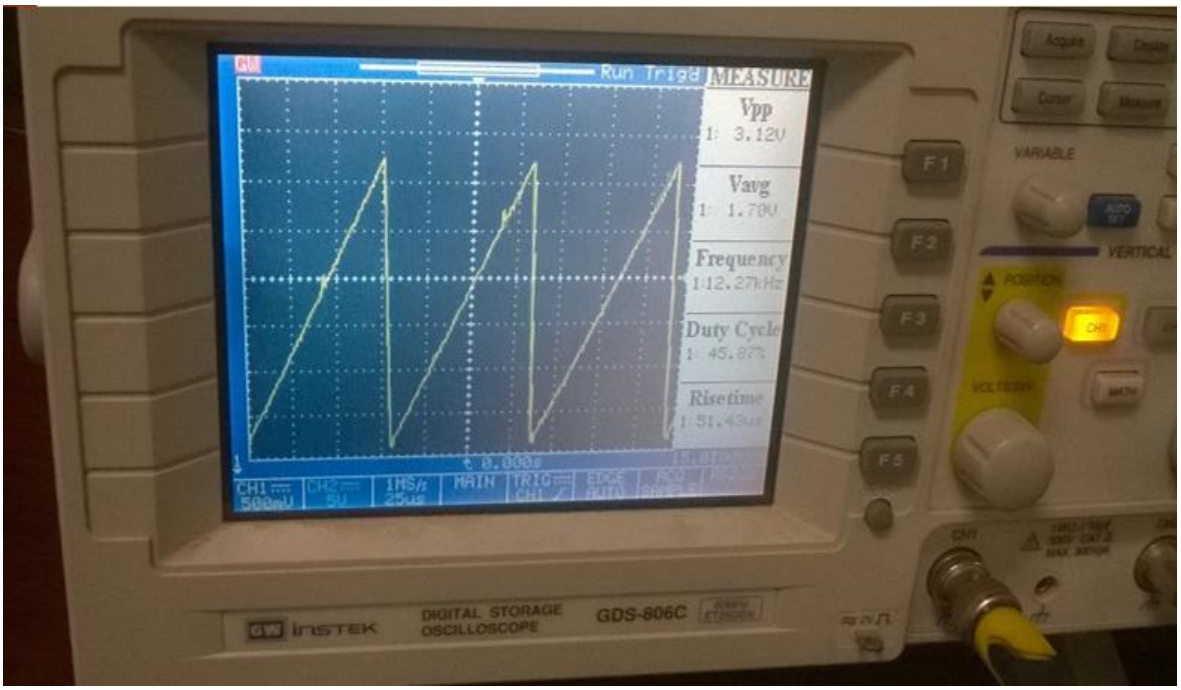


Fig-5.4.5

5.4.6: OUTPUT OF INTEGRATED SYSTEM:

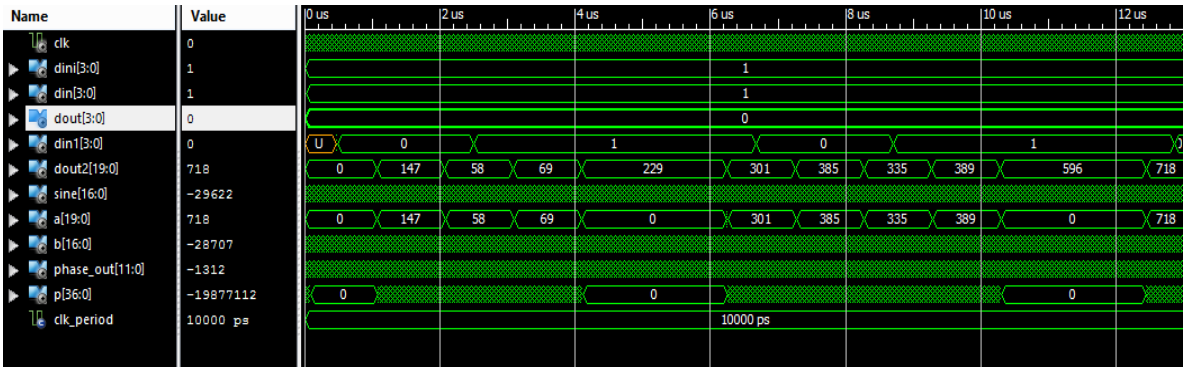


Fig-5.4.6

In the above test bench p represents the final output of integrated system which will be fed to DAC and then to Transducer.

5.4.7: OUTPUT OF TRANSDUCER:

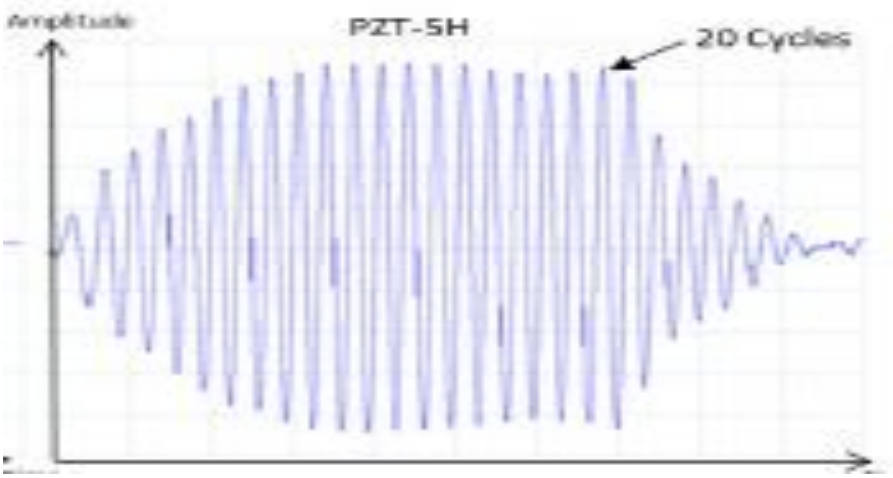


Fig-5.4.7

5.5. SUMMARY:

The transmitter is designed using for successful transmission of 16 kbps of data using a higly directional piston type ultrasonic transducer through water using a bandwidth of 1-2 MHz .The data is bpsk modulated to reduce the complexity of system and ISI is removed by the implementation of RRC pulse shaping.

Chapter 6

Design of Receiver

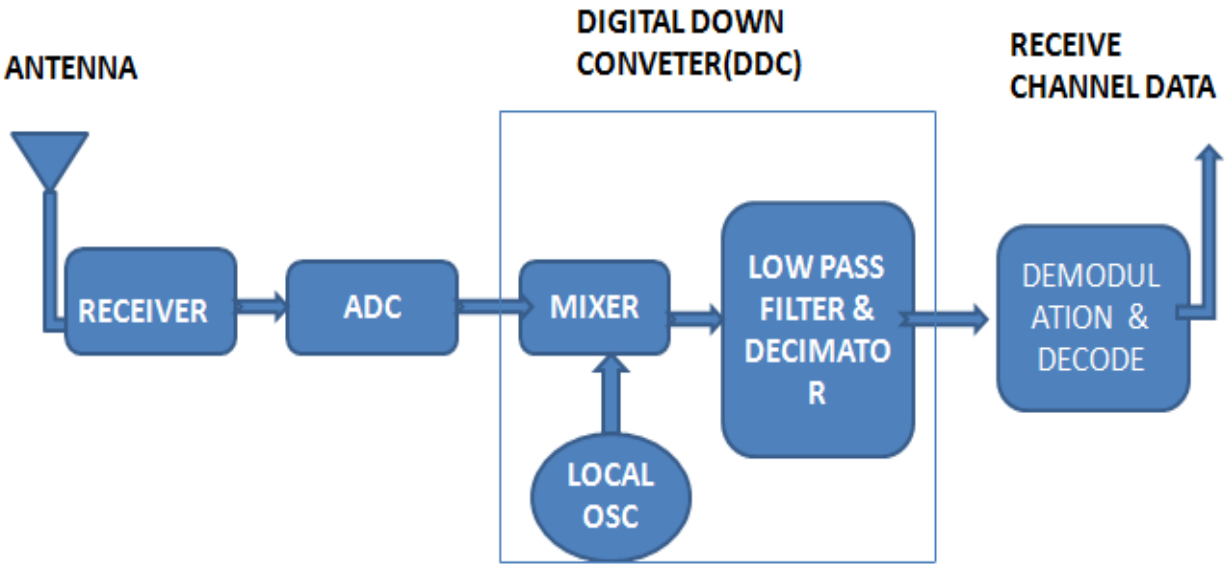


FIG 6.1 (Block diagram of receiver of UWA modem)

DESCRIPTION OF DIFFERENT PART OF RECEIVER:

6.1.ADC (ANALOG TO DIGITAL CONVETER) :

- Hardware Used: Xilinx Spartan 3E Starter Kit by Linear Technology Ltd.
- Onboard ADC (LTC 1407A)
- Software Used: Xilinx ISE 14.2
- Testing Technology: Chipscope Pro
- Successive Approximation (SAR) methods followed for ADC

6.1.1. ONBOARD ADC (LTC 1407A):

ADCs (Analog to Digital Convertor) are of different sorts. The one utilized for our motivation is the Successive Approximation Type ADC (SAR-ADC), where the fundamental segments incorporate a DAC (advanced to simple convertor), a clock, a comparator and a SAR register for putting away the estimations of the computerized information which comes after the comparator contrasts the estimations of the DAC and the simple data and yields a "1" or a "0" contingent upon the condition. A portion of the remarkable highlights of the locally available ADC are:

- 3Msps (3 Mega Hertz testing rate) Sampling: The locally available ADC has two concurrent differential inputs. The inspecting rate is isolated into two channels of 1.5 Msps each.
- 3V Single Supply Operation: It takes its inputs from a supply of 3V DC.
- ±1.25V Differential Input Range: The interval scope of the ADC is 2.5 V (±1.25V). The data voltage reach can be set by changing the increase parameters.
- 3-Wire Serial Interface: It corresponds with the outside information or the outer world through serial media or serial transport (SPI if there should arise an occurrence of LTC 1407A). This makes correspondence simple and basic.

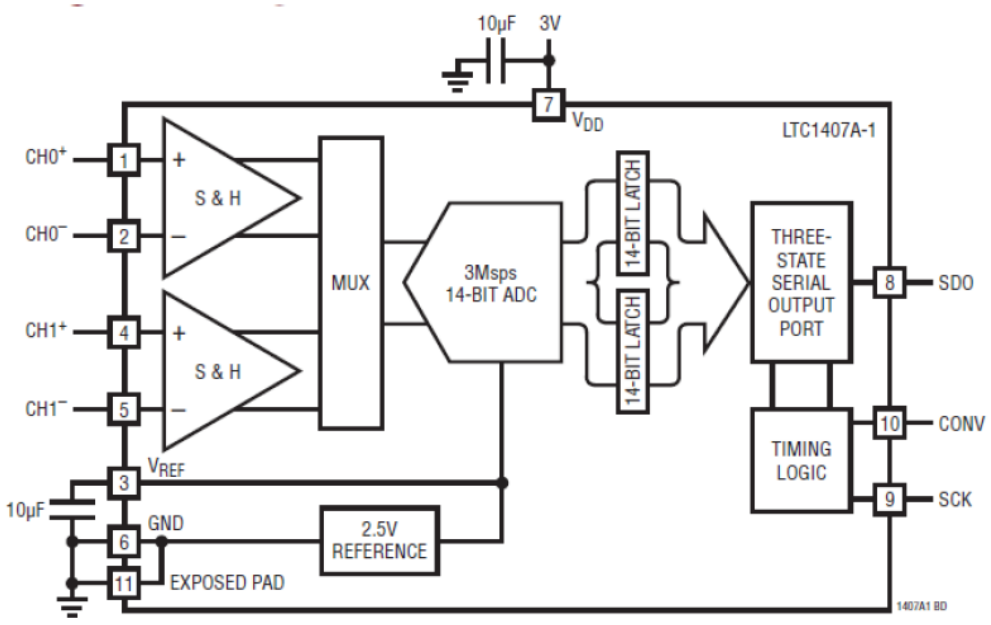


Fig 6.1.1 (CIRCUIT DAIGRAM OF LTC 1407A)

6.1.2:SUCCESSIVE APPROXIMATION ADC:

VIN is approximated as a static esteem in an example and hold (S/H) circuit the progressive close estimation register (SAR) is a counter that augmentations every clock as long as it is empowered by the comparator the yield of the SAR is nourished to a DAC that creates a voltage for correlation with VIN at the point when the yield of the DAC = VIN the estimation of SAR is the computerized representation of VIN.

Fig 6.1.2 (BLOCK DAIGRAM OF SAR-ADC)

6.1.3. PROGRAMABLE PREAMPLIFIER:

The LTC6912-1 gives two free rearranging intensifiers with programmable increase. The motivation behind the enhancer is proportional the approaching voltage on VINA or VINB so it augments the change scope of the ADC, specifically 1.65 ±1.25V. The LTC6912 is a group of double channel, low clamor, digitally programmable addition intensifiers (PGA). The increases for both channels are autonomously programmable utilizing a 3-wire SPI interface to choose voltage additions of 0, -1, -2, -5, -10, -20, -50 and -100. A half-supply reference, produced inside at the AGND pin, backings single power supply applications.

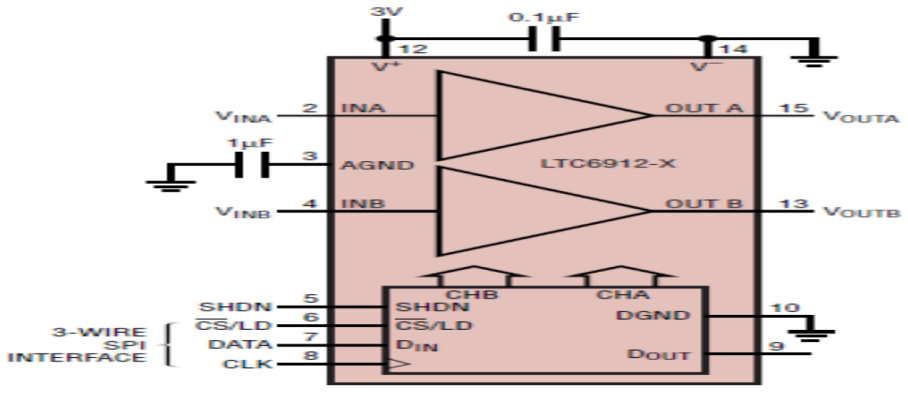


Fig 6.1.3

6.1.3a FPGA AND PREAMPLIFIER INTERFACE:

Various interface signals are used for the interfacing of the amplifier with the FPGA. The amplifier uses the SPI bus for communicating with the FPGA, and this SPI bus is shared among a variety of other peripheral devices like the ADC, DAC the Platform Flash. The other interface signal to those devices must be suitably disabled so that proper interaction of the bus with the pre-amplifier takes place. Some of the SPI signals controlling the working of pre-amplifier are mentioned below:-

o **SPI_MOSI:** This is Master output and slave input signal found in T4 pin of Spartan 3E board**.** It is directed from the FPGA to the ADC. It transmits serial data. Preamplifiers mainly sets the gain and based on this gain setting the analog to digital conversion start and it is also responsible for input range.

- **AMP_CS:** This signal directed from FPGA to amplifier and found at N7 pin of FPGA Spartan 3E board. AMP_CS is a chip select signal of active low and when it becomes high the amplifies gain set.

- **SPI_SCK:** U16 Pin of FPGA Spartan 3E board is SPI_SCK signal and also directed from FPGA to Amplifier. According to this clock setting the amplifier gain setting is done. It sends serially one bit at a time at every rising edge of SPI_SCK.

- **AMP_SHDN :** P7 pin of FPGA Spartan 3E Board is AMP_SHDN Signal. This a active high shutdown and reset signal directed from FPGA to Amplifier .

- **AMP_DOUT:** E18 Pin of FPGA Spartan 3E board is AMP_DOUT. This one signal which is directed from Amplifier to FPGA. This signal just echo or copy the previous amplifier setting gain values to present value.

6.1.4.WORKING OF ADC:

ADC output is 14 bit data which give the 2's complement of input Volt. The input values of ADC depend on the gain of the Pre-amplifier. For voltage range of .4V to 2.9V maximum gain range is -1.Conversion formula is given below:

$$D[13:0] = GAIN*[(V_{IN} - 1.65V)/1.25]*8192$$

D [13:0] is the 14bits output value which we obtain by doing 2's complement of input voltage value. SPI_MISO brings the output from ADC to FPGA.

GAIN is the pre-amplifier gain set before.1.65V is the reference voltage and we get this by doing voltage divider circuit. Range of ADC is 1.25 V and OUTPUT is so divided by 1.25V,then scaled by 8192. In case of this ADC Voltage is parallel sampled so both the input is simultaneously processed.

6.1.5.INTERFACE BETWEEN ADC AND FPGA:

- **AD_CONV:** P11 pin of FPGA board is AD_CONV. This a active high shutdown and reset signals .This is a internal signal of FPGA Spartan 3E Board which have to make high to start the conversion. For ADC functionally this it directed form FPGA to ADC to start the conversion.
- **SPI_MISO:** Pin N10 of FPGA board is responsible for this signal. This signal is the serial data output from adc to FPGA and this SPI_MOSI is a signal from FPGA to ADC.
- **SPI_SCK** : It is the signal from adc to FPGA and played avital role in conversion.

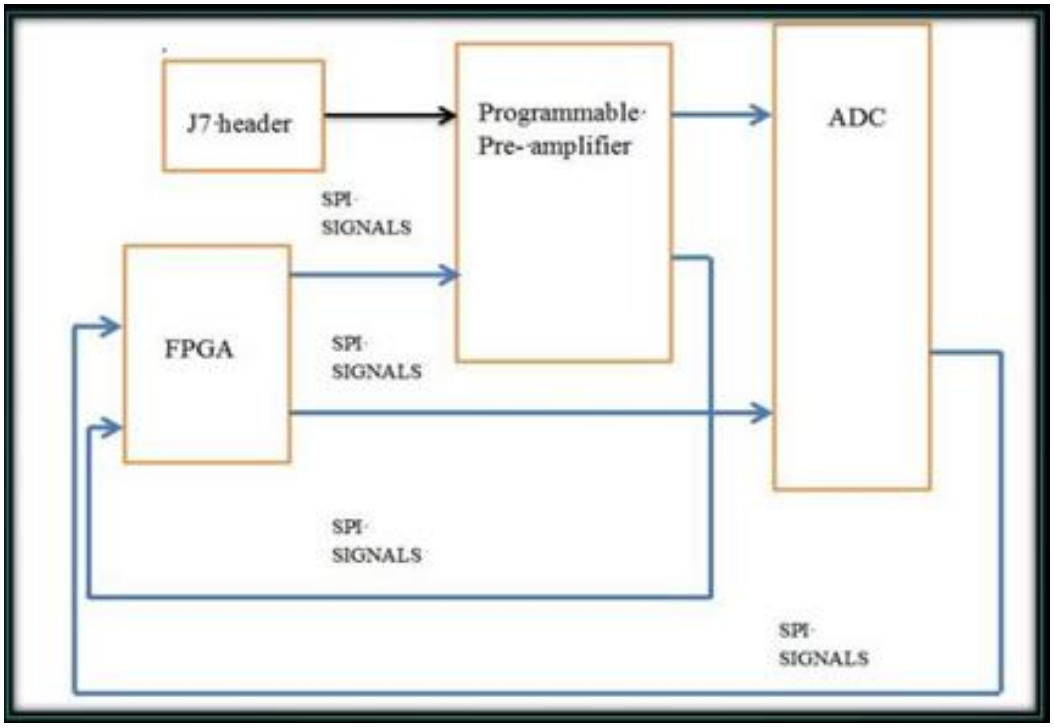


Fig-6.1.5

6.1.6.OUTPUT OF VHDL CODE FOR ADC IMPLEMENTATION:

I. ADC RTL DAIGRAM

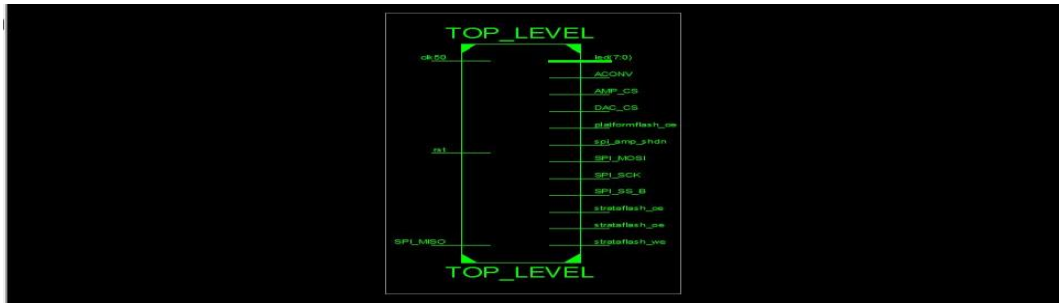


Fig-6.1.6a

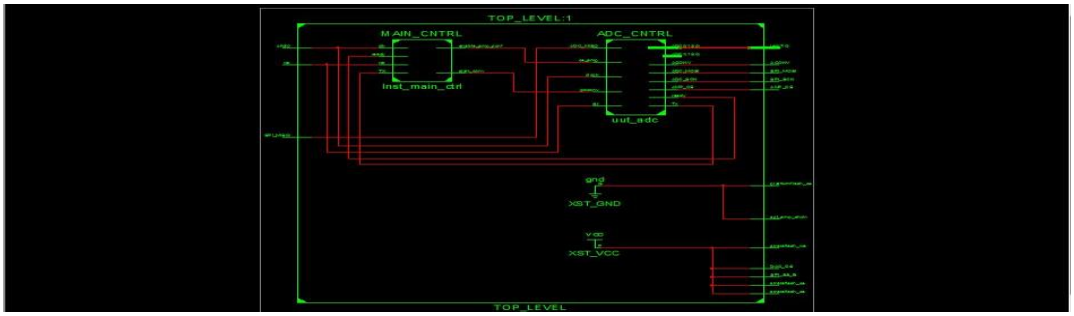


Fig-6.1.6b

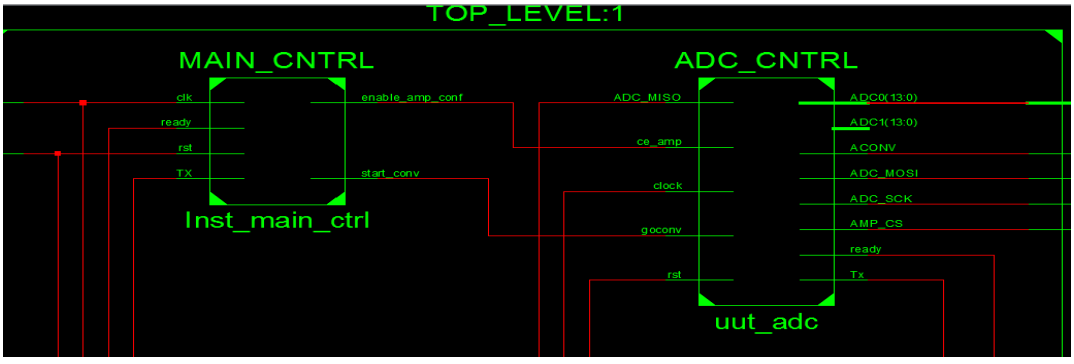


Fig-6.1.6c

6.1.7: CHIPSCOPE PRO SETTING:

- Make connection of all the ADC Channel within the DATA PORT.
- Connect "clk_buff" within CLOCK PORT.
- Connect "rst" within TRIGGER PORT.

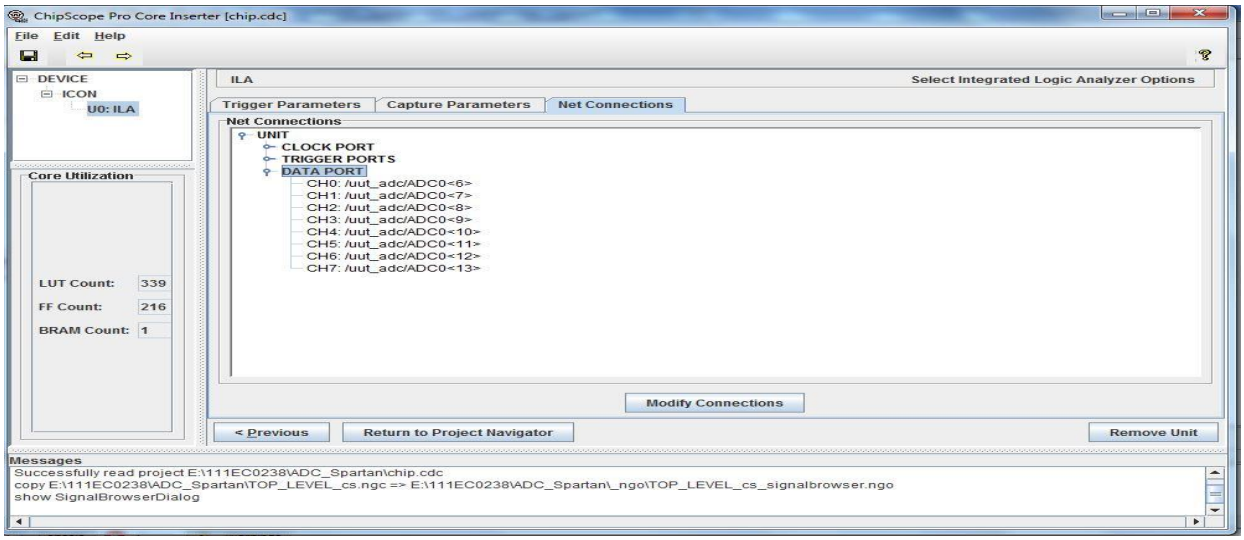


Fig-6.1.7

6.1.7a OUTPUT FOR ANALOG INPUT 0V

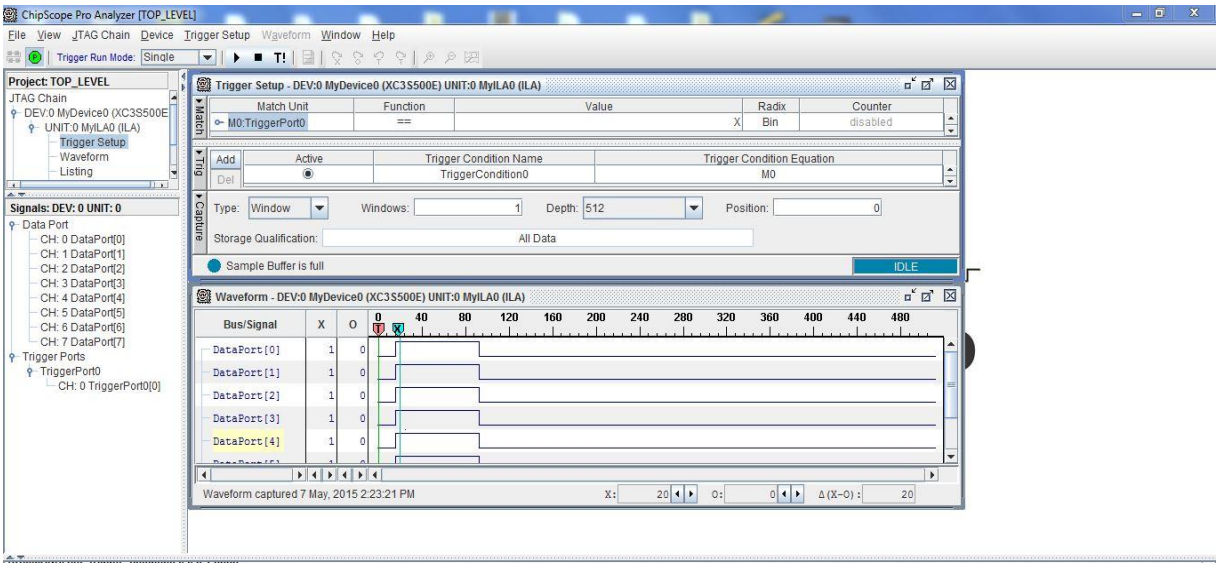


Fig-6.1.7a

6.1.7b For analog input .64V

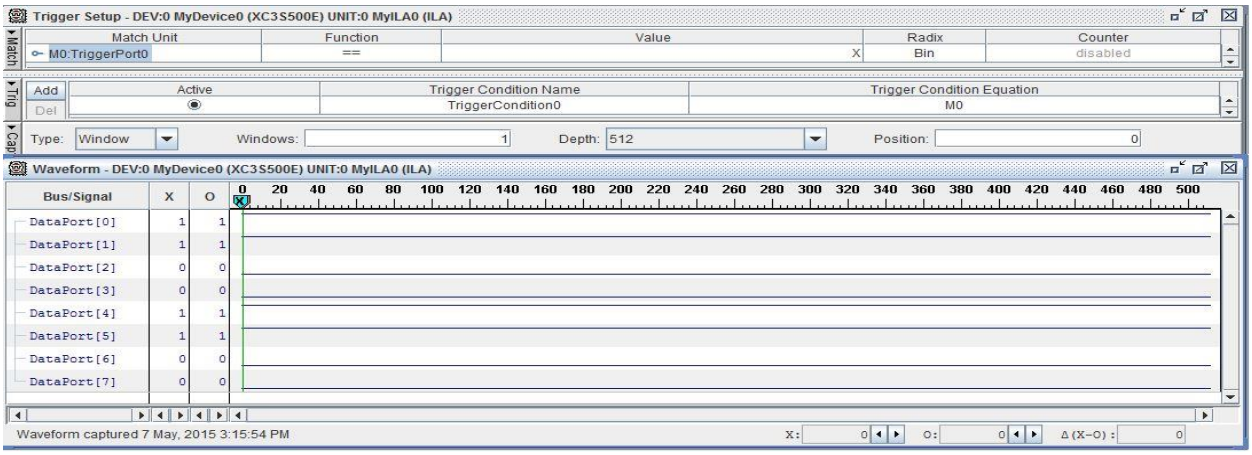


Fig-6.1.7b

6.1.7c For analog input .88V

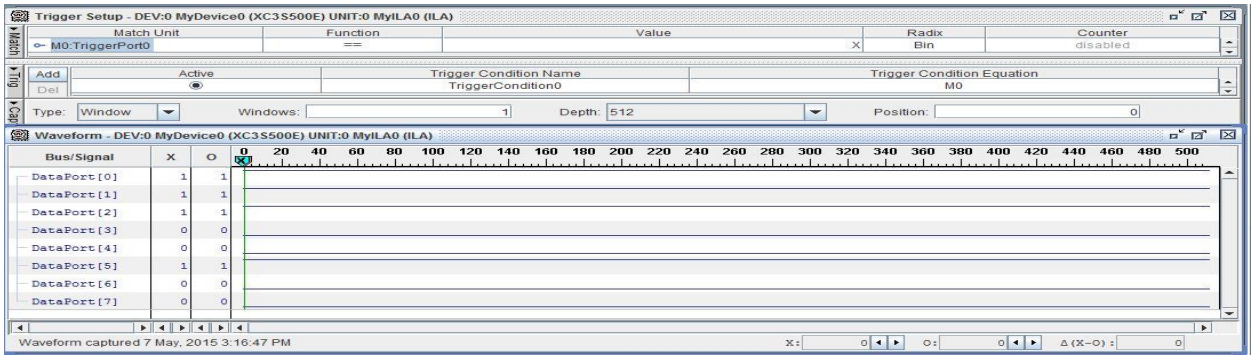


Fig-6.1.7c

6.1.7.d For analog input 1.22V

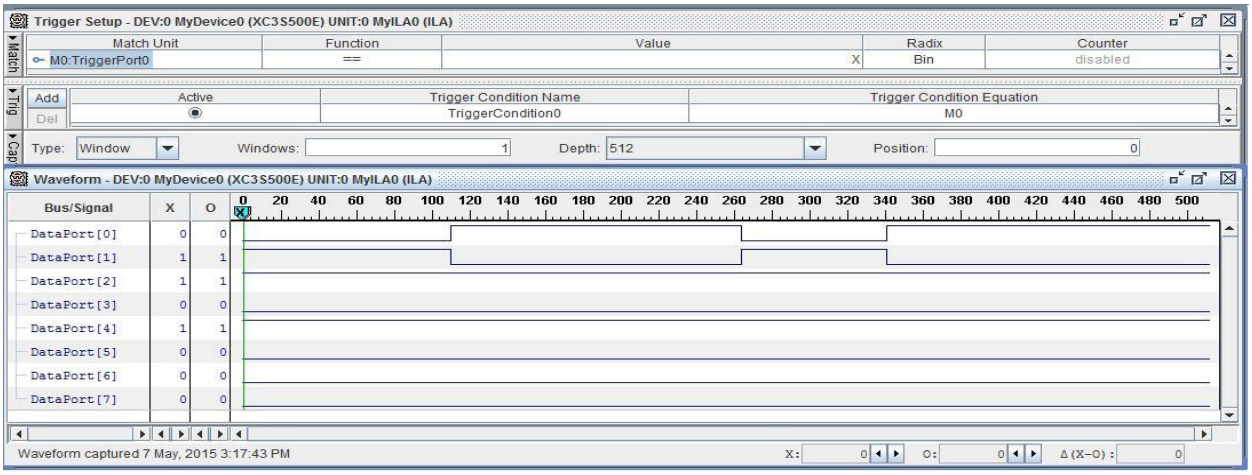


Fig-6.1.7d

6.2. DDC(Digital Down Converter):

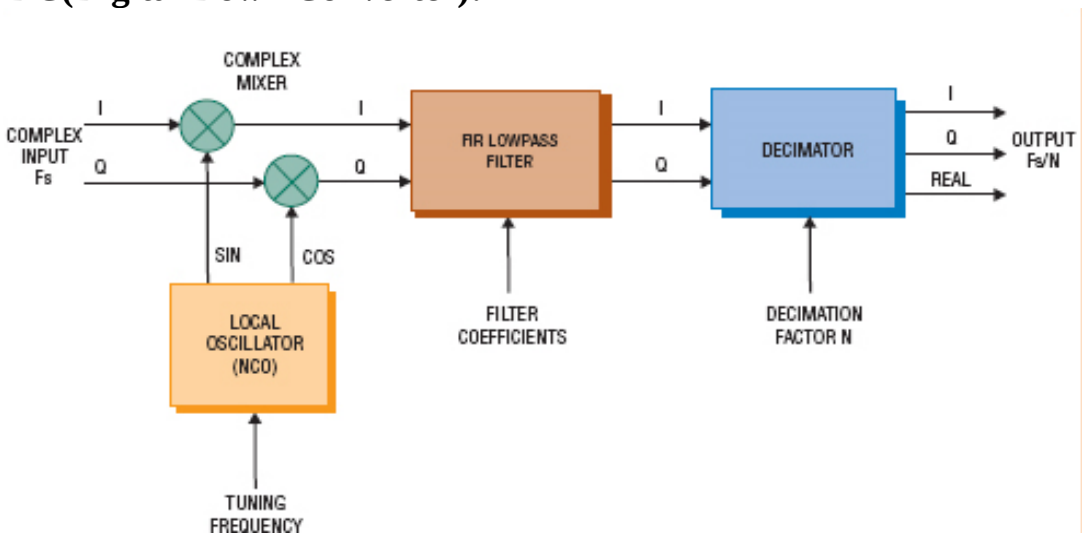


Fig-6.2

6.2.1 Synchronization:

The synchronization process of the receiver have to be receive the data and locked the signal either its frequency or phase. Many control mechanism used to bring out the correct phase and frequency.

We do synchronization in these following level:

- Carrier Recovery
- Symbol Time Recovery
- Frame synchronization

6.2.1a Carrier Recovery :

It is done to avoid carrier phase/frequency error present in receive signals. Reason of carrier phase/frequency error are the use of local oscillator in case of up and down conversion and modulation and demodulation, repeater used in up-down conversion and due to the Doppler effect. In case of coherent detection local oscillators frequency and phase is matched with the received signals.

6.2.1b Symbol Time Recovery

This is done to synchronies the sampling clock with receive frequency and phase. The symbol time error is introduce in communication because of not sampling at maximum eye opening and it reduce the noise margin and introduce ISI.

6.2.1c Frame synchronization

In case of receive signals the process of making alignment of frame that means making identification of distinct bit of frequency is called frame synchronization.

Here we assume that frequency is already known to receiver so we have to do **phase synchronization.**

6.3. Phase Synchronization

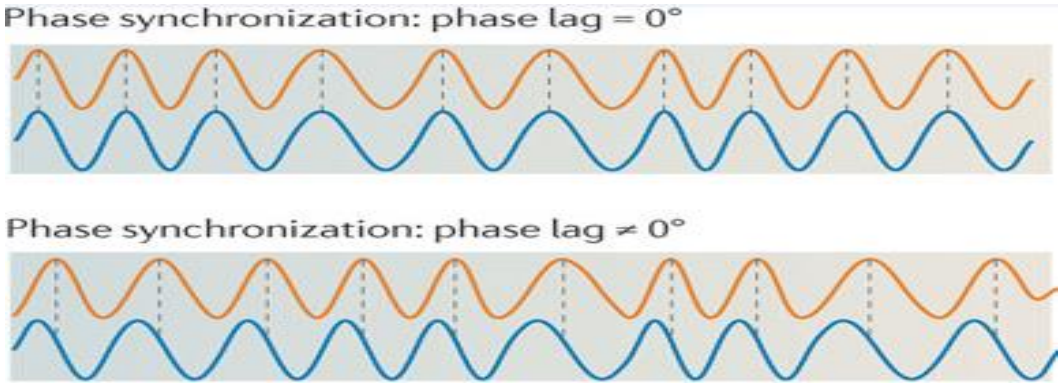


Fig-6.3

6.3.1 Output Of Phase Synchronization:

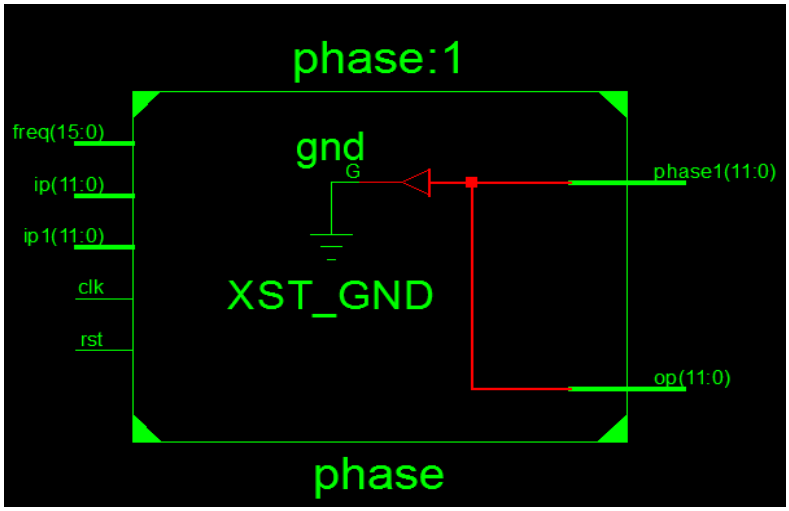


Fig-6.3.1

6.3.2.Test Bench Output:

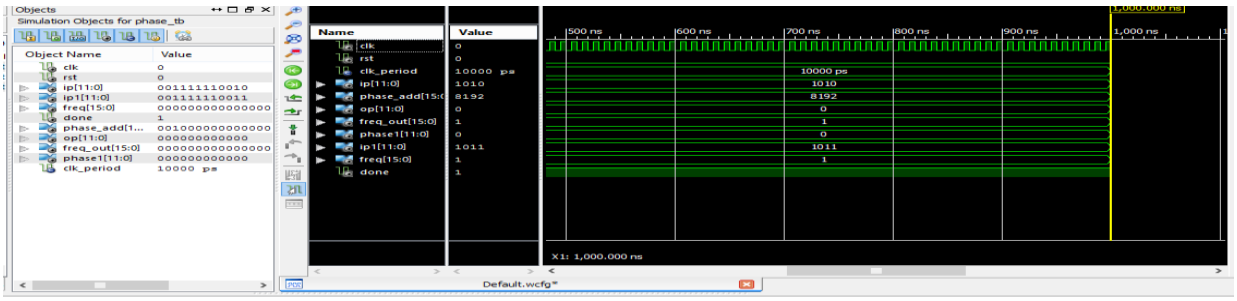


Fig-6.3.2

6.4.LOW PASS FILTER :

A low pass filter always passes signal of interest ,it passes signals which is lower than a cutoff frequency and does not passes or attenuates the higher range frequencies. The filter design and setting of parameters like filter coefficient determine the amount of attenuation. Aliasing is a process when the digital signals appear to have a different frequencies than the original analog signals. To avoid alising effect we also use low pass filter.

6.4.1.RTL Model of Lowpass Filter:

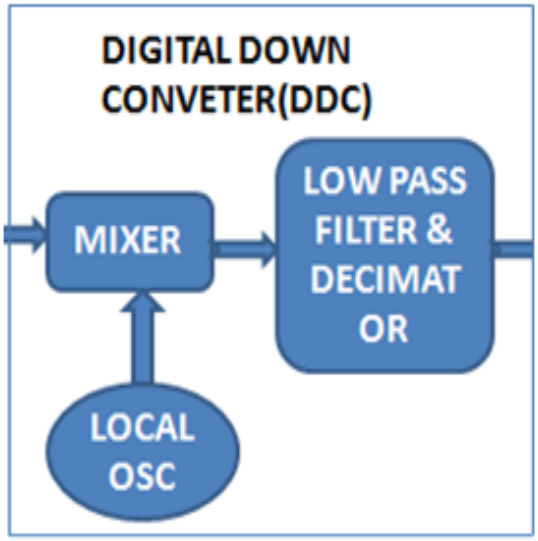


Fig-6.4.1a

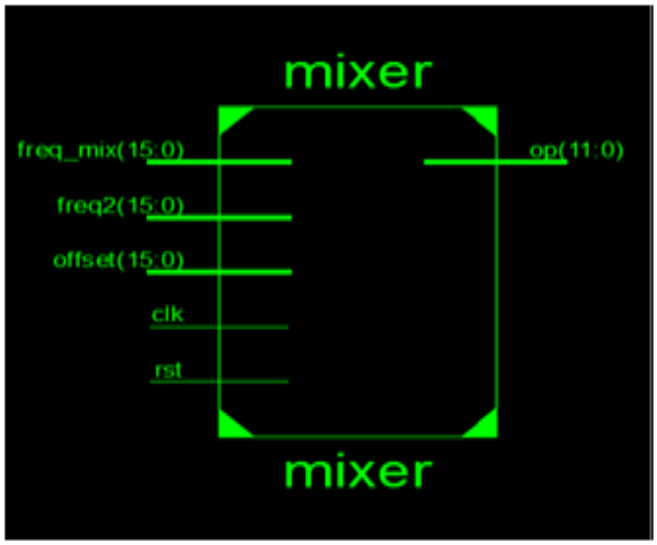


Fig-6.4.1b

6.4.2.OUTPUT OF LOWPASS FILTER:

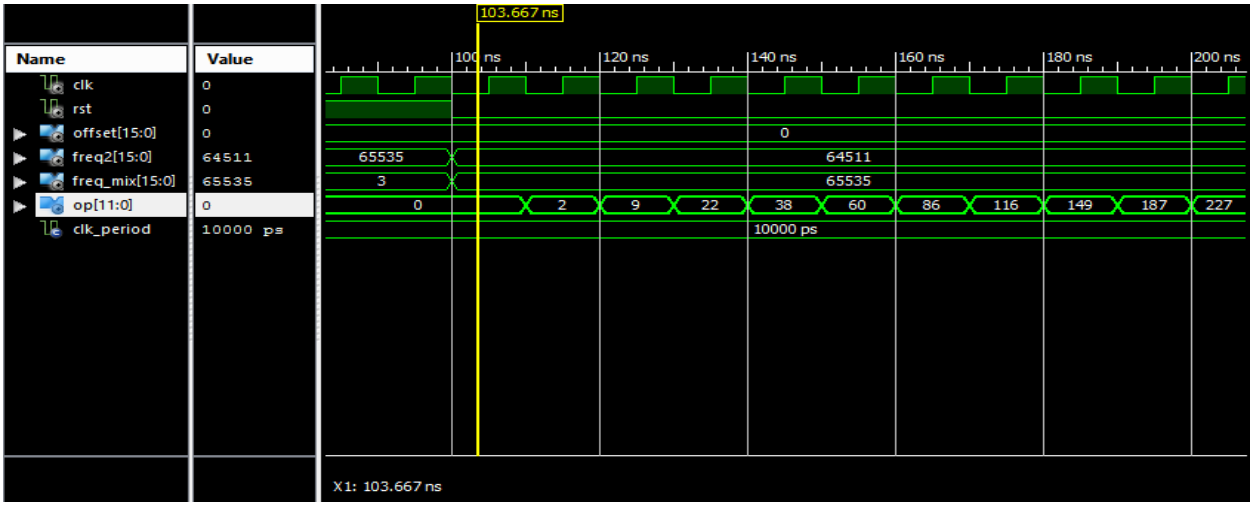


Fig-6.4.2a

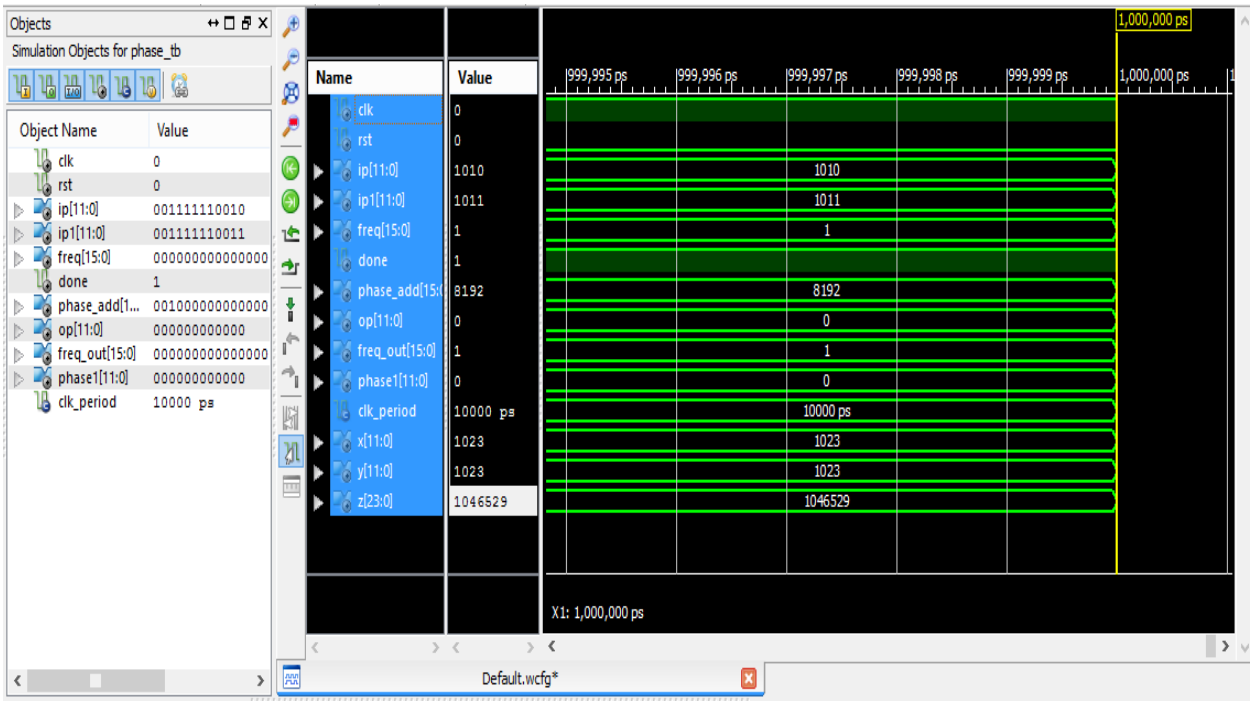


Fig-6.4.2b

6.5 DEMODULATION (BPSK) :

In case of BPSK ,the signals are fixed in amplitude but the phase vary according to the message signal. For one data level it has one constant phase and for other level its phase reverse by 180 degree out of phase .A BPSK signal define like this

$$V_{bpsk}(t) = b(t)\,(2P)^{(1/2)}\,\cos(2\pi f_c t) \quad 0 \le t \le T$$

where b(t) = +1 or -1, fc is stands the carrier frequency, and *T* is bit duration means time taken by 1 bit to transfer. P represents power level of BPSK signal. In case of receiver BPSK demodulation is done in which first we have to detect the message bit in rate at which it is send before interpolator so that we can only detect the message signal and avoid reluctances bits .Then we can compare the message bit whether it is 1 or -1 and according to that we receive actual message signals.

In case of BPSK demodulation coherent detection is used in which both phase and frequency known to the receiver ,then signal get multiplied with a local oscillator having same phase and frequency as receive bit. Then the value pass through a integrator and compare with a threshold value. If the received bit and threshold value is nearly same then it detect 1 ,otherwise 0.After receiving 1 and 0 we can decode it to a bit stream which is actual message bit which the transmitter transmit.

6.5.1.RTL DAIGRAM OF BPSK-DEMODULATION:

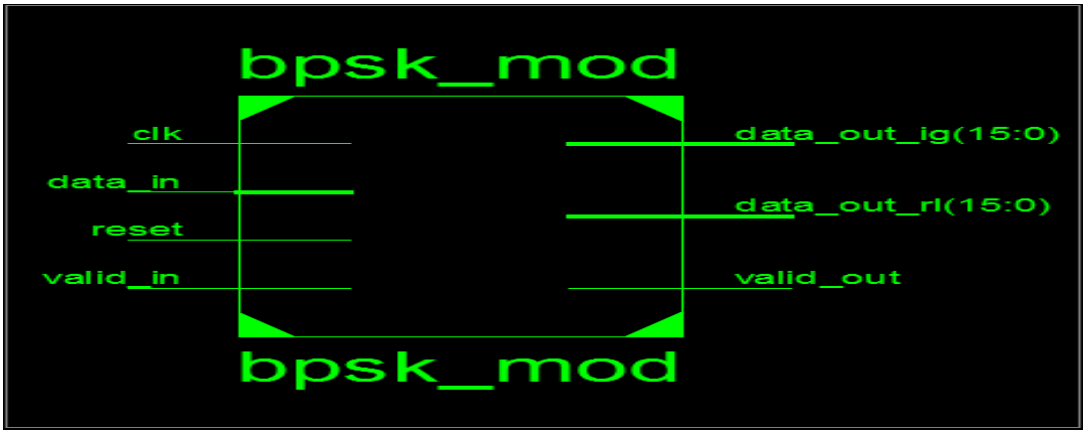


Fig-6.5.1

Here the Data_in is the input signal whether it will be 1 or 0 according to what ever received. When Valid_in is 0 the output is 0.Demodulation starts when the valid_in is 1.When valid_in 1 ,then for message bit 1 one stream of data decoded and for 0 another stream of data decoded. In that case when we receive the data valid_out is 1.

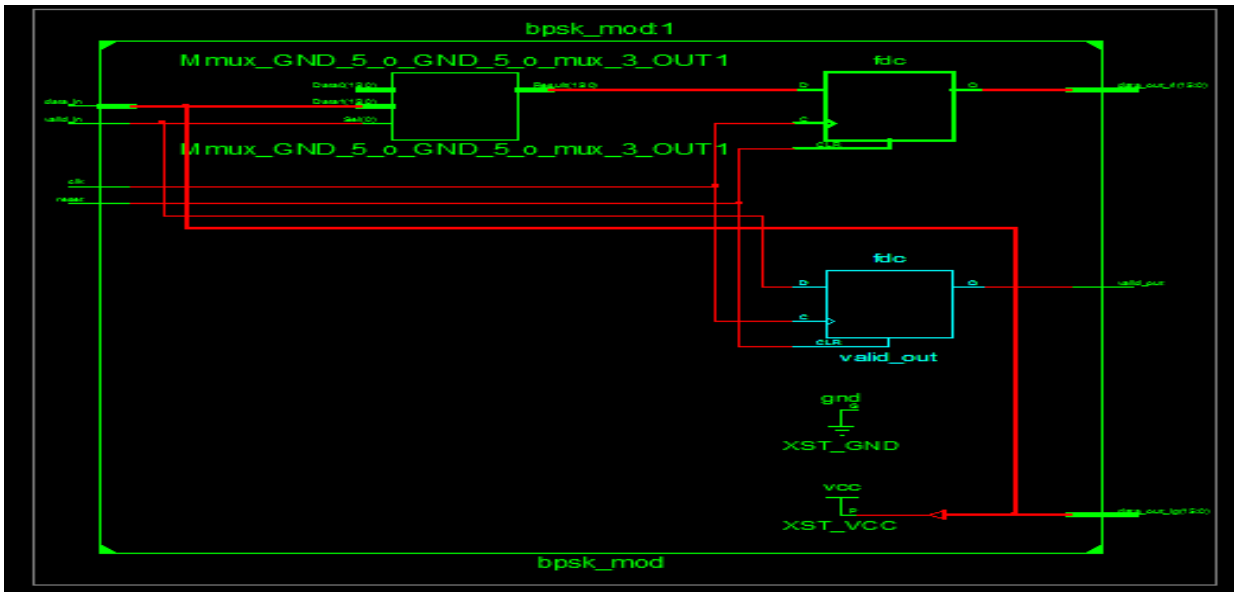


Fig-6.5.1b

6.5.2.TEST BENCH OUTPUT OF BPSK DEMODULATION:

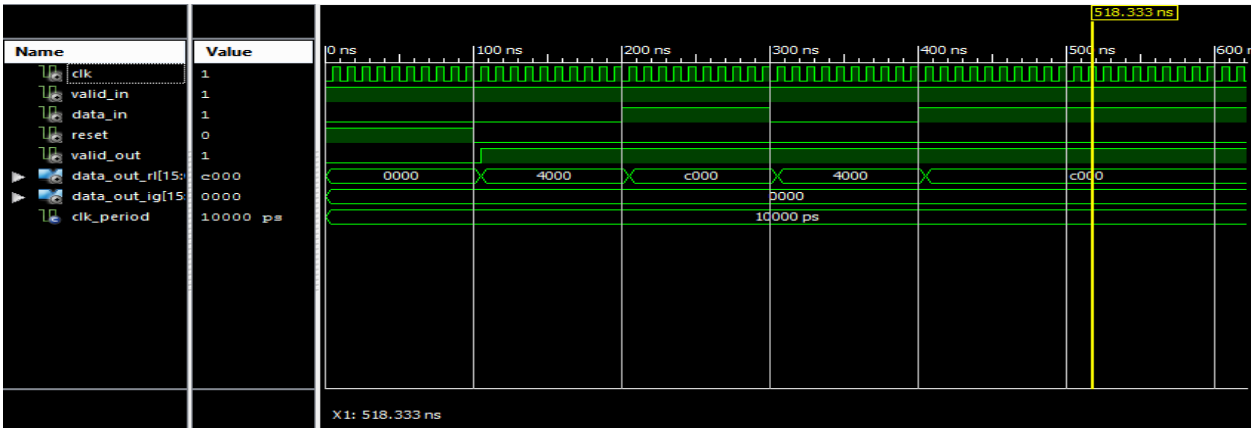


Fig-6.5.2

Chapter 7
Problem Faced,Conclusion And Future Work

7.1 PROBLEM FACED:

7.1.1 Speed of Operation: The operating speed of the system is desired to be high without compromising on the data integrity. Initially we took the input data to be as high as 1MHz. With such a high data rate we had difficulty to maintain the data output without data losses. Since the processing time of the filters exceeded the input frequency, there were frequent data losses. Even large storage units were not of much help either. Since referring to other standards we came to know that we need to keep the system frequency much higher than the input frequency for smooth operation. In this way the filters would take very less processing time than the input frequency. Also the design requires minimum number of storage units.

7.1.2 Placement of a Storage Unit:

The method which we are following requires a storage unit of four registers. The placement of these registers was a matter of concern, since there must not be any data loss. Placing all the registers after the interpolator resulted in data loss. Placing two registers before the interpolator for storing input values and two registers after the interpolator resulted in difficulty in low pass filter for accessing the data. So with the memory unit we had to design the control unit for storing the data. The input data were stored in the first and the fourth registers. The output of the interpolator was stored in second and third registers. The storage technique was controlled using the rdy signal from the interpolator and the low pass filter and their respective acknowledgement bits (ack, ack1, reack, reack1).

7.1.3 Clock Synchronization:

During the operation we had problem in synchronizing the different blocks of the system with the system clock. Several times it happened that, the clock ticks were missed which resulted in introduction of additional counters i.e. extra hardware. We had to take the system frequency as the multiple of the input frequency. We had to include multiple processes in the VHDL Code to synchronize all the blocks.

7.2.CONCLUSION:

From this thesis, we can draw the following conclusions:

- The modem is highly reconfigurable, parametrisable , and extensible of interest to designers.
- The use of an FPGA is the main factor for the flexibility of the modem.
- BPSK modulation is used for low-complexity implementation, while improvement in the BER performance can be achieved by using better modulation scheme and error controlling algorithms.
- Inter symbol interference is mitigated by limiting the bandwidth of transmitted signal using pulse shaping technique.
- Phase synchronization method is adopted for the detection of the signal.

Different modules of the underwater communication system are designed using MATLAB and ISE Project Navigator . VHDL codes are written to control and synchronize the operation between the modules.

7.3.FUTURE WORK:

- **Implementation of FSK Instead Of BPSK:**
  FSK has a better ber performance as compared to bpsk.For achieving high data rate and better ber performance FSK can be implemented instead of BPSK.

- **Implementation of Equalization And Channel Coding:**
  An advanced UWA modem can be designed by implementing different algorithms for channel equalization and error control coding can be implemented for the retrieving the transmitted data from the corrupted data.

- **Optimization of Digital Filters And Analog Circuits:**
  By using more optimized digital filters the speed of operation can be increased and advanced signal processing may lead to successful implementation of under water communication with high data rate.

References

[1] Marcos Martins. Ultrasonic wireless broadband communication system for underwater applications.PhD thesis, Universidade do Minho, 2013.

[2] S. Morgera. Multiple terminal acoustic communications system design. IEEE Journal of Oceanic Engineering, 5(3):199–204, July 1980.

[3] Roee Diamant, Arie Feuer, and Lutz Lampe. Choosing the right signal. In Proceedings of the Seventh ACM International Conference on Underwater Networks and Systems - WUWNet ’12, New York, New York, USA, 2012. ACM Press.

[4] J. Catipovic, D. Brady, and S. Etchemendy. Development of underwater acoustic modems and networks.Oceanography, 6:112–119, March 1993.

[5] http://www.xilinx.com

[6] Jurdak, R.; Aguiar, P.; Baldi, P.; Lopes, C.V., "Software Modems for Underwater Sensor Networks," *OCEANS 2007 - Europe* vol., no., pp.1-6,18-21 June 2007

[7] Craig R. Benson, Michael J. Ryan, and Michael R. Frater. Towards robust high data-rate hydro-acoustic modems. In Oceans ’12. IEEE, October 2012.