VIRTUAL FABRICATION OF RECESSED-SOURCE/DRAIN SOI MOSFETs

A thesis submitted in partial fulfillment of the requirements for the award of

Master of Technology

In

VLSI design and Embedded systems

By

SRIKANYA DASARI

Roll no: 213EC2196

Department of Electronics and Communication Engineering
National Institute of Technology
Rourkela, India

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Under the guidance of

Prof. Pramod Kumar Tiwari

Department of Electronics and Communication Engineering
National Institute of Technology
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MAY 2015

DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING,
NATIONAL INSTITUTE OF TECHNOLOGY,
ROURKELA, ODISHA, INDIA-769008.

CERTIFICATE

This is to certify that the thesis report entitled "**Virtual Fabrication of short channel Recessed-Source/Drain SOI MOSFETs**", submitted by **SRIKANYA DASARI** bearing **roll no. 213EC2196** in partial fulfillment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded Systems**" during session 2013-2015 at National Institute of Technology, Rourkela is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela
Date: June, 2015

Prof. P. K. TIWARI
Dept. of E.C.E
National Institute of Technology
Rourkela – 769008

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(***D.Srikanya***)

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LIST OF ACRONYMS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IC	Integrated Circuit
RC	Resistance Capacitor
SCEs	Short Channel Effects
DLBL	Drain Induced Barrier Lowering
HCEs	Hot Carrier Effects
SOI	Silicon On Insulator
PD	Partially Depleted
FD	Fully Depleted
UTB	Ultra-Thin Body
CMOS	Complementary Metal Oxide Semiconductor
SMG	Single Metal Gate
DMG	Dual Metal Gate
SDE	Source Drain Extension
DMDG	Dual Material Double Gate
Re-S/D	Recessed Source/Drain
STI	Shallow Trench Isolation
LOCOS	Local Oxidation Of Silicon

TCAD	Technology Computer Aided Design
VWF	Virtual Wafer Fab
SSF	Standard Structure Format
CVD	Chemical Vapor Deposition
BOX	Buried Oxide
LDD	Lightly Doped Drain
VLSI	Very Large Scale Integration

ABSTRACT

The main objective of using process simulator in the IC fabrication technologies is to obtain the fast and accurate simulation of all critical fabrication steps used in the semiconductor devices. ATHENA process simulator provides an appropriate and suitable platform for simulating processes such as oxidation, lithography, physical etching and deposition, diffusion, ion implantation which are used in the semiconductor industry.

Scaling down of MOSFET device in IC Technology offers excellent features. However, leakage current and short channel effects (SCEs) are to be considered when MOSFETs are scaled to the deep submicron region. A Re-S/D SOI MOSFET with 30nm channel length, and 10nm channel thickness, is virtually fabricated using ATHENA process simulator with reduced short channel effects (SCEs) and low source/drain series resistance. The processing steps, which are required to obtain the structure of the Re-S/D SOI MOSFET, are explained in detail. The electrical characteristics such as drain current (I_{ds}) versus drain to source voltage (V_{DS}) is obtained for different values of V_{GS} and Re-S/D thickness (t_{rsd}). The influence of gate oxide thickness, recessed source/drain thickness on subthreshold swing is observed and analyzed.

Further, performance of the device is improved by a gate engineering technique named dual metal gate technology. This technique is incorporated in the virtual fabrication of single metal gate recessed source/drain SOI MOSFET. The effect of channel length ratio on threshold voltage (V_{th}), surface potential, subthreshold current (I_{sub}) and drain current (I_{ds}) is observed. Also the impact of recessed source/drain thickness (t_{rsd}) on drain current (I_{ds}) is evaluated.

CHAPTER1

1. INTRODUCTION

1.1 Semiconductor devices and a brief history of MOSFET:

From past 125 years an extensive study has been carried out on Semiconductor devices. Till date, there are around 60 major devices having 100 variations relating to them. These devices are constructed from building blocks like metal-semiconductor interface, p-n junction, hetero-junction interface and metal-oxide-semiconductor interface [1]. Metal semiconductor interface is the first semiconductor device studied in 1984. This interface act as either rectifying contact or ohmic contact. The p-n junction is formed between a p-type and n-type semiconductors. Theory of p-n junction acts as the foundation of semiconductor device physics. The interface between two dissimilar semiconductors results in hetero-junction interface. High speed and photonic devices can be formed by using these heterojunctions. The most important building block is the metal-oxide-semiconductor (MOS) structure which is a conjunction of metal-oxide interface and oxide-semiconductor interface. MOSFET (MOS field-effect transistor) can be constructed by using source and drain as two p-n junctions, gate as the MOS structure.

The point contact transistor is the first transistor invented by Bardeen and Bratten in 1947 as shown in Figure 1.1. The two point contacts separated by 50um and made from two strips of gold foil which are pressed over a germanium surface. Followed by the extremely versatile switching device was developed by Ebers in 1952, which is the basic model for thyristor. Next solar cell was developed by Chapin in 1954. To improve the transistor performance, Hetero-junction bipolar transistor was proposed by Kroemer in 1957.

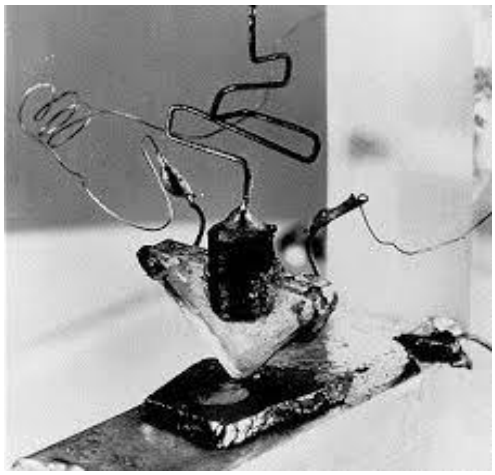

Figure 1.2 Point contact transistor

Figure 1.1 First MOSFET transistor

Further, heavily doped p-n junction negative resistance characteristics are observed by Esaki in 1958 which leads to the discovery of tunnel diode. In 1960, Khang and Atalla reported MOSFET first time which is the most important device for all advanced integrated circuits. This device is developed by utilizing thermally oxidized silicon substrate with 20um thick gate length and200nm thick gate oxide as shown in Fig. 1.2.Top elongated area is the aluminum gate and two key holes are the source and drain contacts. Even though MOSFET technology has been scaled down to submicron region, but the choice of thermally grown silicon dioxide and silicon remains the same. Present days around 90% of the semiconductor device market is consumed by MOSFET and its related integrated circuits.

1.2 Importance of MOSFET Technology scaling:

Scaling down of the MOSFET device in IC Technology offers excellent features such as packaging density and device speed of operation which increase exponentially. Simultaneously, power dissipation decreases exponentially as stated by Moore's. In 1960 Gordon Moore made an experimental observation that the number of transistors on a chip doubles for every 18 months

approximately [2-3] as shown in Figure1.2.When minimum line width is reached a new technology node or technology generation is introduced [4]. Several Technology nodes are 0.18µm, 0.13µm, 90nm, 65nm, 45nm etc. Here the numbers represent the metal line width. Historically, a new

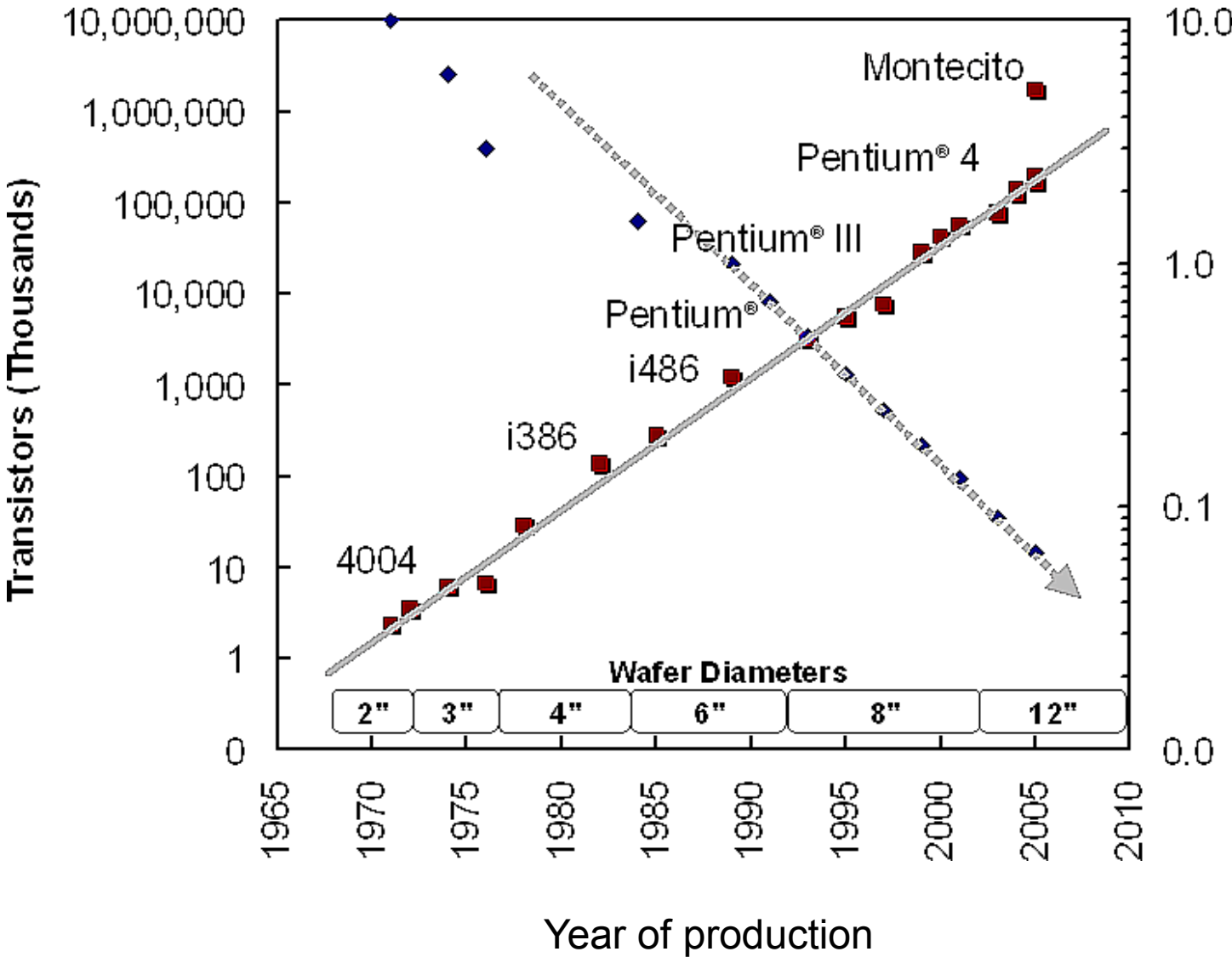

Figure 1.3 Moore's law observation

technology node was introduced in every three years. The cost of an integrated circuit is relatively proportional to the number of chips, since the fabrication cost per semiconductor wafer is comparatively fixed. Hence, smaller IC allows more chips per wafer itself, reducing the price

of an IC. All device dimensions such as channel length, channel thickness, and oxide thickness have to be scaled proportionally with the MOSFET. When device dimensions are scaled by equal factors, which does not alter the channel resistance, but gate capacitance is reduced by the same factor. It reduces the transistor RC delay by a similar factor resulting in fast switching.

1.3 Limitations due to scaling of conventional MOSFETs:

Over with all these advances of MOSFET device scaling, maintaining good performance becomes increasingly difficult over time. In spite of the fact that the electronics industry has benefitted from continuous scaling over the last four decades, the present trends demonstrate that the scaling of the conventional MOSFETs is quickly approaching the end of its valuable life time. However, leakage currents and short channel effects (SCEs) are to be considered when the MOSFETs are scaled to the deep submicron region [5]. At the point when channel length shrivels, the gate control over channel depletion region decreases because of the spread out of charge from the source / drain. During the fabrication process the gate length may scatter, this prompts to the dispersal of device characteristics. The predominating consistency issues related with SCEs are hot-carrier effect and drain-induced-barrier-lowering (DIBL) at increasing drain voltage as well as a shift in threshold voltage and lack of pinch-off with decreasing channel length. Additionally, SCEs also debases the gate voltage gate voltage on drain current, which increases the drain off-current and decreases the sub-threshold slope.

1.3.1 Carrier velocity saturation: When device dimensions are reduced in size, the electric field in the channel increases typically also increases the number of carriers itself called as increased carrier velocity. However, at higher electric fields the linear relation between the electric field and the velocity is violated, when carriers reach its saturation velocity gradually. The increased scattering rate of highly energetic electrons causes this velocity saturation which

leads to increase in the transit time of carriers through the channel. Stronger velocity saturation effects can observe in deep sub-micron regions compared with bulk MOSFETs due to the larger average electron velocity.

1.3.2 Channel length modulation: In MOSFET scaling, channel length modulation is one of the several short channel effects. This effect depicted when drain to source voltage (V_{DS}) is increased beyond the saturated voltage ($V_{DS,Sat}$). This leads to droping of excess voltage (V_{DS} - $V_{DS,\ Sat}$) across a portion of the channel on the right: this portion as shown in Fig 1.4. The carrier velocity is saturated throughout this portion. When the channel length is shortened, velocity saturation effects become stronger and weaken the effective channel length. The carrier's flow achieved through subsurface Instead of flowing in a channel. When drain voltage increases further, excess voltage is dropped near the drain region, then the current control extends to the source, which in turn reduces the length of the effective channel caused to increase the in the channel further as shown in the Figure 1.5. This effect is called channel-length modulation.

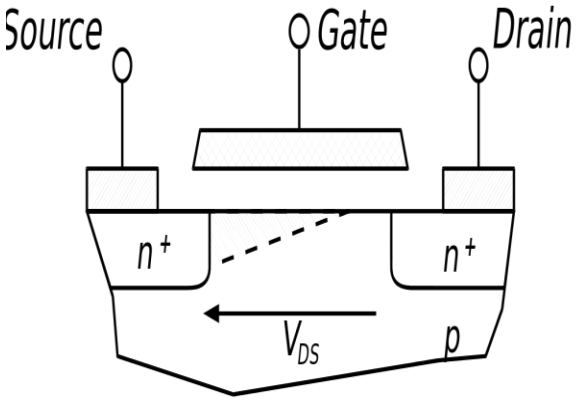

Figure 1.4 Cross section of MOSFET operating in the saturation region

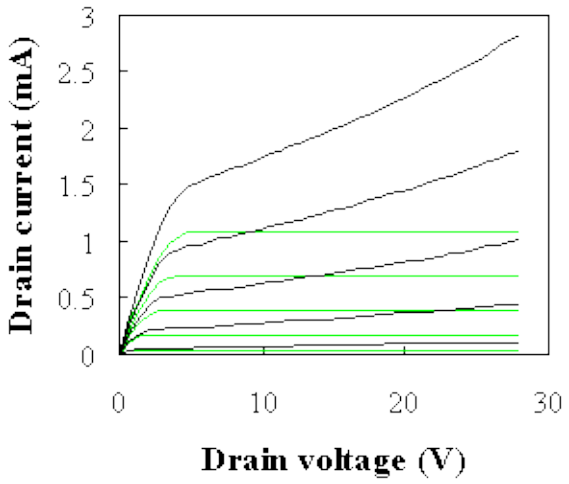

Figure 1.5 Drain current versus drain voltage with and without channel modulation

1.3.4 Sub-threshold Leakage: The electric fields in the device channel are constantly increasing with device shrinking; due to the voltage drops across the gate oxide and the channel are same. This leads to the reliability issues. Consequently, to overcome these issues the supply voltage has been scaled down with more conservative than the device dimensions. Subsequently to maintain good driving capabilities, threshold voltage also decreased. This down-scaling of threshold voltage results in off-state current, which leads to power consumption of an IC in its idle state. In the weak-inversion region (sub-threshold region) the surface potential of the channel is constant and the diffusion of minority carriers leads to the current flow, which depends exponentially on the gate to source voltage.

1.3.4 Punch-through effect: In the presence of parasitic current conduction between the drain and source, the drain current of a MOS transistor may increase. This type of drain current is poorly controlled by gate contact because the path exists far away from the surface. This currently adds to the sub-threshold current resulting in increased power consumption. The potential distribution under the channel determines the actual amount of punch-through current. When the depletion regions around the source and drain extend towards each other lowers the potential barrier between them and carriers easily move from source to drain. This punch-through effect highly depends on the source/drain junction depths and on the applied drain voltage.

1.3.5 Drain induced Barrier lowering: The impact of the drain voltage on the channel region limits the performance of sub-micron MOS devices. This is somewhat related to punch-through effect, sometimes it is noted as "subsurface DIBL". The height of the potential barrier between source and channel regions is because of drift and diffusion currents balance in the weak inversion region. If high drain voltage is applied when the gate voltage is lower than the

threshold voltage leads to decrease in the potential barrier height as indicated in Figure 1.6, resulting increased drain current. Drain voltage also controls the drain voltage. Height of the barrier lowers because of this drain voltage, hence it is called as a drain induced barrier lowering.

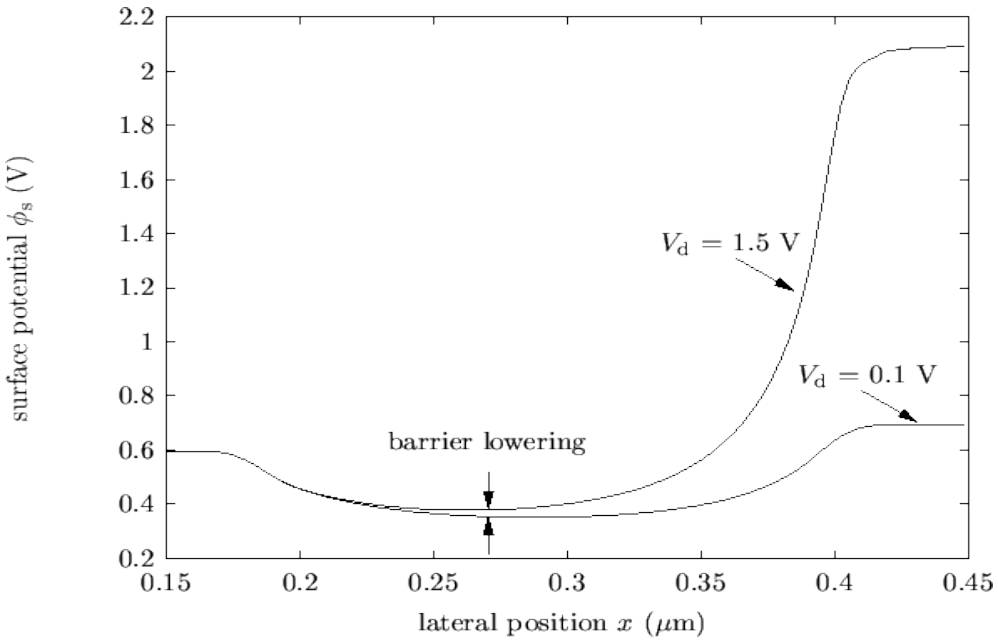

Figure 1.6 Surface potential of device for different VDS values

1.3.6 Hot carrier effects (HCEs), Impact ionization: When MOS transistor is operated in pinch-off, all carriers are flowing with saturation velocity that can introduce parasitic effects near the channel towards the drain side termed as hot Carrier Effects. These carriers have enough energy to create new electron-hole pairs by impact ionization. Impact ionization is non-equilibrium process, the carriers in the conduction band or valanced band becomes highly energetic and collide with electrons in the valance band and excite those electrons into the conduction band by external electric fields. The generated carriers may be collected either by drain or may inject into the gate oxide layer which leads to hot carrier effects. Hot carriers change the threshold voltage and also create traps at the silicon oxide interface which leads to sub-threshold swing degradation. This deterioration effects limit the lifetime of transistor.

1.4 SOI devices:

To continue the miniaturization of microelectronic devices, there are several manufacturing strategies are employed; SOI technology implementation is one of them. SOI technology refers to silicon on insulator technology, which uses silicon-insulator-silicon substrate is used in place of the silicon substrate while manufacturing semiconductor devices. SOI technology has several benefits over the bulk MOSFET technology in terms of 1) It exhibits lower parasitic capacitance because of isolation from substrate; 2) improves power consumption; 3) Reduced temperature dependency; 4) Provides better wafer utilization; 5) Reduced leakage currents. In SOI MOSFET semiconductor layer such as germanium or silicon, this is sandwitched between the gate oxide layer and buried oxide layer. There are two types of SOI MOSFET devices: Partially depleted (PD) SOI MOSFET and fully depleted (FD) SOI MOSFET.

1.4.1 Partially depleted SOI MOSFET: In PDSOI MOSFET the sandwiched film, i.e. channel layer between the gate oxide and buried oxide is large, so that the depletion region can't cover the whole channel region as shown in Fig. 1.7. Hence, some extent, this partially depleted SOI MOSFET devices act as bulk MOSFET devices. Of course, there are a few advantages compared with bulk MOSFET devices.

1.4.2 Fully depleted SOI MOSFET: In PDSOI MOSFET the sandwiched film, i.e. channel layer between the gate oxide and buried oxide is very thin, so that the depletion region easily covers the whole film as shown in Fig. 1.8. FD SOI MOSFET devices have high switching speeds compared with bulk MOSFET because of increases in inverse charges. Other limitations such as higher sub-threshold swing, threshold voltage roll-off can be overcome by using FD SOI MOSFET devices because drain and source electric fields are not interfering with each other due to buried oxide.

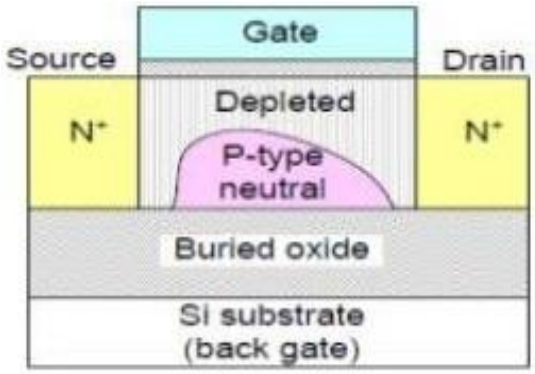

Figure 1.7 Partially depleted (PD) SOI MOSFET

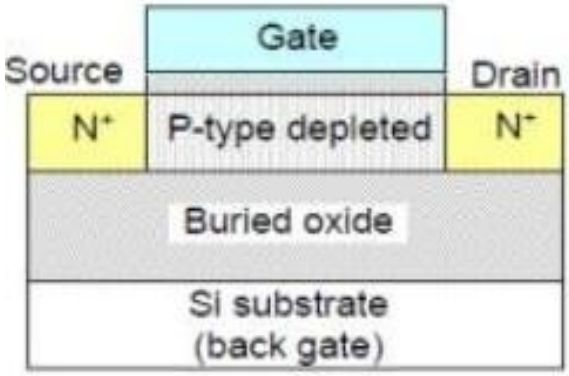

Figure 1.8 Fully depleted (FD) SOI MOSFET

1.5. Limitations of conventional SOI MOSFETs:

These conventional SOI-MOSFET devices come with some device related fabrication problems such as Lattice heating, Kink effect and Sub threshold slope. Above certain drain voltage kink is observed in the SOI MOSFET output characteristics, which is characterized as the kink effect. SOI MOSFET devices are thermally insulated from the substrate by buried oxide layer; leads to a substantial increment in temperature which affects the output. This effect is called lattice heating. Conventional SOI MOSFET devices also exhibit short channel effects. Hence, the control over these short channel effects can be controlled by FD (fully depleted) UTB (ultra thin body) SOI MOSFET with the buried oxide layer. The major problem with this FD UTB SOI MOSFET is showing very high series resistance which in turn degrades the system performance.

1.6 Recessed source/drain SOI MOSFET:

To overcome the above all limitations, microelectronic industry needs a new device structure. Recessed-Source/Drain (Re-S/D) SOI MOSFET is achieved by extending source and drain regions of FD UTB SOI MOSFET into the buried oxide layer. By increasing thicknesses of source/drain regions of FD UTB SOI MOSFET overcomes the series resistance problem. In comparison with the conventional SOI MOSFETs, Re-S/D SOI MOSFET devices have one

special property, i.e. it provides coupling between the source/drain regions and the channel region through the buried oxide layer. Figure 1.9 shows the cross sectional view of n-type Re-S/D SOI MOSFET.

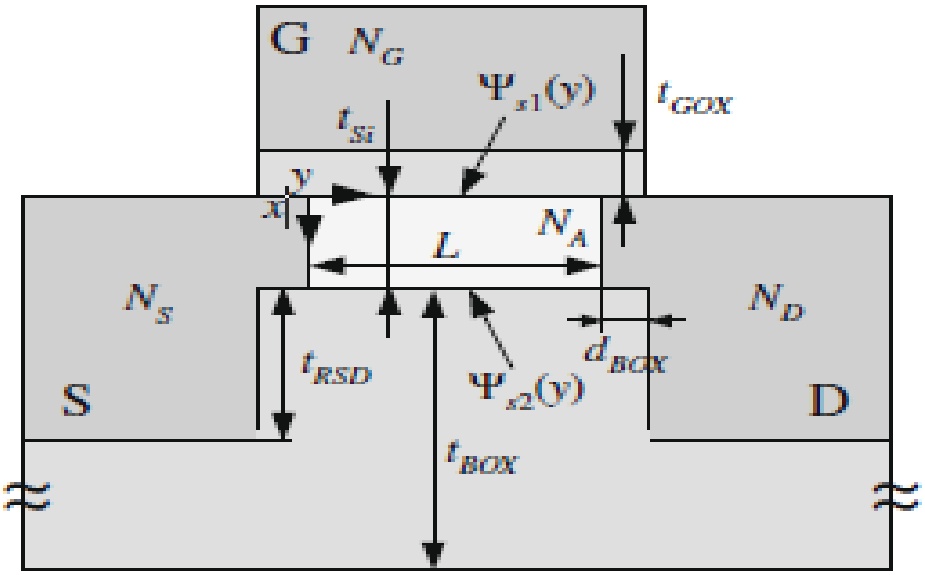

Figure 1.7 Cross sectional view of recessed source/drain SOI MOSFET

1.7 Thesis Organization:

Chapter 2 introduces the concept of recessed S/D SOI MOSFET and gives a brief literature review of different SOI MOSFET structures

Chapter 3.summarizes the design methodology of current simulation work and also briefs about ATHENA process simulator and its features, processing steps, necessary models.

Chapter 4 explains the virtual fabrication of recessed-source/drain SOI MOSFET and also gives brief discussion about processing steps and electrical characterization of the device.

Chapter 5 lists the processing steps which are required to construct dual metal gate recessed source/drain SOI MOSFET and also gives performance analysis of virtually fabricated device. Chapter 6concludes the thesis and future scope of work.

CHAPTER 2

2. LITERATURE REVIEW

2.1 Review on SOI devices

In 1996, D. FLANDRE et al. demonstrated opportunities of fully-depleted (FD) silicon-on-insulator (SOI) technology in the field of low-power, low-voltage CMOS circuits [6]. The advantages of FD SOI MOSFET Technology have been investigated both experimentally and theoretically and also realized low power low voltage circuits using this technology. The results of the study demonstrate that this technology provides low threshold voltage about 0.33 V at supply voltage of 1.2 V.

In 2004, Vishwas Jaju et al. explained problems related to SOI technology. Technological development of SOI wafer fabrication have been presented and properties of double gate MOSFET's, advantages and disadvantages of double gate MOSFET's have been explained over bulk CMOS technology [7]. Several methods for SOI wafer fabrication have been discussed. The results of this study concluded that this Double gate SOI MOSFETs exhibits near-ideal sub-threshold slope and short channel immunities. Jagadesh Kumar et al. presented 2-dimensional analytical model for channel surface potential variation in FD (fully depleted) DMG (dual material gate) SOI MOSFET and investigated the short channel effects (SCEs) [8]. The effect of gate metal lengths and their work functions channel and source/drain doping concentrations, Thin silicon layer, gate oxide and buried oxide thicknesses have been explored. Results of his study demonstrated that This device exhibits suppressed short channel effects such as DIBL and hot carrier effect because of step function in the surface potential of the channel region, which provides screening of the drain potential variation by gate.

In 2005, C.G. Ahn et al. successfully fabricated 30nm channel length Recessed S/D SOI MOSFET with the 5nm thick undoped channel [9]. They illustrated the reduction in SDE resistance by extending heavily doped polysilicon source/drain regions deeper into buried oxide. It was found that the proposed device exhibited excellent properties in short channel immunities, Drain-induced barrier lowering (DIBL) and sub threshold slope. G.V. Reddy et al. presented unique features of Dual-Material Double-Gate (DMDG) SOI MOSFET [10]. they have been studied short channel effects of this structure by developing an analytical model which includes the calculation of the electric field, surface potential, drain induced barrier lowering and threshold voltage; and also discussed a model for drain current, drain conductance, trans-conductance and voltage gain. Results of his study concluded that this structure exhibits increased trans-conductance, decreased drain conductance including suppressed short channel effects.

In 2009, Svilicic et al. Presented analytical models for the front gate and back gate potential distribution, short channel threshold voltage and subthreshold swing of the Re-S/D UTB SOI MOSFETs [11]. They investigated the subthreshold phenomenon of the device. The results of proposed models are in good agreement with 2D numerical device simulator results for different material and geometric parameters.

In 2012, SAPNA et al. virtually fabricated 35nm channel length fully depleted SOI MOSFET with 6nm thick SOI layer using the ATHENA process simulator [12]. The effect of channel doping concentration and SOI layer thickness on the electrical behavior of the device was explored. The results of the study led to the conclusions that threshold voltage decreases with channel doping concentration and good saturation region is obtained in I_d-V_d curve. In addition, threshold voltage and sub threshold swing decreases with decrease in SOI layer thickness. The

on-current driving-capability of a Re-S/D UTB SOI MOSFETs can be further improved by adopting the dual- metal-gate (DMG) structure instead of conventional single-metal-gate structure. In 2013, P.K. Tiwari et al. Presented analytical subthreshold current and subthreshold swing models for a short channel dual-metal-gate (DMG) fully depleted recessed-source/drain (Re-S/D) SOI MOSFET [13-16]. A comparison is drawn between the derived 2-D analytical model results and simulated results obtained from 2-D ATLAS^{TM} from SILVACO. The subthreshold current and subthreshold swing together increase with the decrease in channel length. The SCEs increase with decrease in gate oxide thickness.

2.2 Review on fabrication techniques:

In 2002 Bin Yu, Sunnyvale published a patent on "ultra-thin-body SOI MOS transistors having recessed source and drain regions" [17]. In this patent he invented a method for manufacturing semiconductor-on-insulator integrated circuit having transistor with recessed source and drain regions. And also discussed a method to fabricate semiconductor-on-insulator substrate. Gate, channel with thickness less than 100 A^0 are arranged in between recessed source and drain regions. as per his method substrate is formed by an oxygen implantation process or by bonding and etch-back process. Amorphous semiconductor layer is utilized for recessed source and drain regions, which allow sufficient material for silicidation. Channel is doped with B or BF2 or iridium at rate of 10^{19} cm^{-3} and source and drain regions are doped with As or P or Sb at rate of 10^{20} cm^{-3}. Gate structure includes pair of spacers, gate conductor and gate oxide, where spacers are formed by using Si3N4, SiO2. Thermally grown silicon dioxide is used as gate oxide. Heavily doped polisilicon is used as the gate conductor and it is deposited by chemical vapor deposition. Transistors within the IC are isolated by insulated oxide which is formed by a shallow trench isolation (STI) process or local oxidation of silicon (LOCOS) process.

In 2004, Zhang et al. Fabricated self-aligned recessed-source/drain fully depleted UTB SOI MOSFET [18]. They stated that the series resistance and miller capacitance reduced over UTB SOI MOSFETs when the source and drain regions are extended deeper into the buried oxide. Apart from this, the slight DIBL effect is observed. 20nm channel region is formed by thermal oxidation and etching of 170nm SOI film. Gate stack comprises 4nm thick gate oxide, 150nm thick amorphous silicon and 50nm thick nitride. Source and drain regions are formed by shallow implantation with arsenic impurity. Silicon nitride spacer is used to define the length of the extended source and drain regions.

In 2006, Thean et. al published a patent on "semiconductor fabrication process including recessed source/drain regions in an SOI wafer" [19]. In this patent he discussed a semiconductor fabrication process for semiconductor-on-insulator wafer includes a transistor with shallow source and drain regions desirable for reduced junction capacitance. As per his invention, fabrication process starts with the creation of trench isolation structures in an active layer of SOI wafer. Channel structure is formed by selective etching of an active layer with respect to isolated trenches. Gate dielectric and gate structure are developed on the channel layer. using this gate structure as the mask, exposed portions of the gate dielectric, channel structure and buried oxide layer of SOI wafer are removed by etching. Through this exposed portions, source and drain regions are grown epitaxially from bulk substrate.

Proposed process flow is related to the fabrication of recessed-source/drain SOI MOSFET device. Process steps are very simple and Device performance is enhanced by recessed source/drain regions, which are formed by etch back process of SOI layer. Channel is formed by deposition of thin silicon layer.

CHAPTER 3

3. SIMULATION METHODOLOGY

3.1 Introduction

Simulation is the impersonation of the operation of a physical process. The demonstration of simulating obliges a model; this model gives the key qualities or characteristics or behaviors/functions of the physical system. The model indicates the system itself, though the simulation represents system operation. Simulation of a device uses the standard mathematical models and device models [20]. A simulation of an IC starts with a set of desired specifications. TCAD (Technology Computer Aided Design) is a branch of electronic design automation, that model the semiconductor device fabrication and operation. TCAD design is a combination of process, device and circuit simulation; and modeling tools. The ATHENA process simulator provides physical, numerical and two-dimensional (2-D) simulation models for semiconductor processing. Electrical, thermal, and optical behavior of semiconductor devices is simulated by using ATLAS, which is a two-dimensional and a three-dimensional Device Simulation Framework. ATLAS is frequently used in combination with the process simulator ATHENA. ATHENA provides the physical structure, which is outcome from the processing steps such as ion implantation, physical etching, oxidation, diffusion, and deposition, stress formation, lithography, and silicidation. The resulting physical structure is utilized by the ATLAS device simulator for further electrical characterization of the device. The impact of process parameters on device characteristics are determined by both ATHENA and ATLAS together [21]. ATLAS employed in conjunction with the VWF (virtual wafer fab) interactive tools. VWF is set of several software modules, those are Deckbuild, Devedit, Tonyplot and Maskviews: In which

each one is responsible for some part of a device simulation. They communicate with each other by this process and device simulators. By using Standard Structure Format (SSF), these tools communicate with each other and also with device and process simulators.

3.2 Design flow using ATHENA

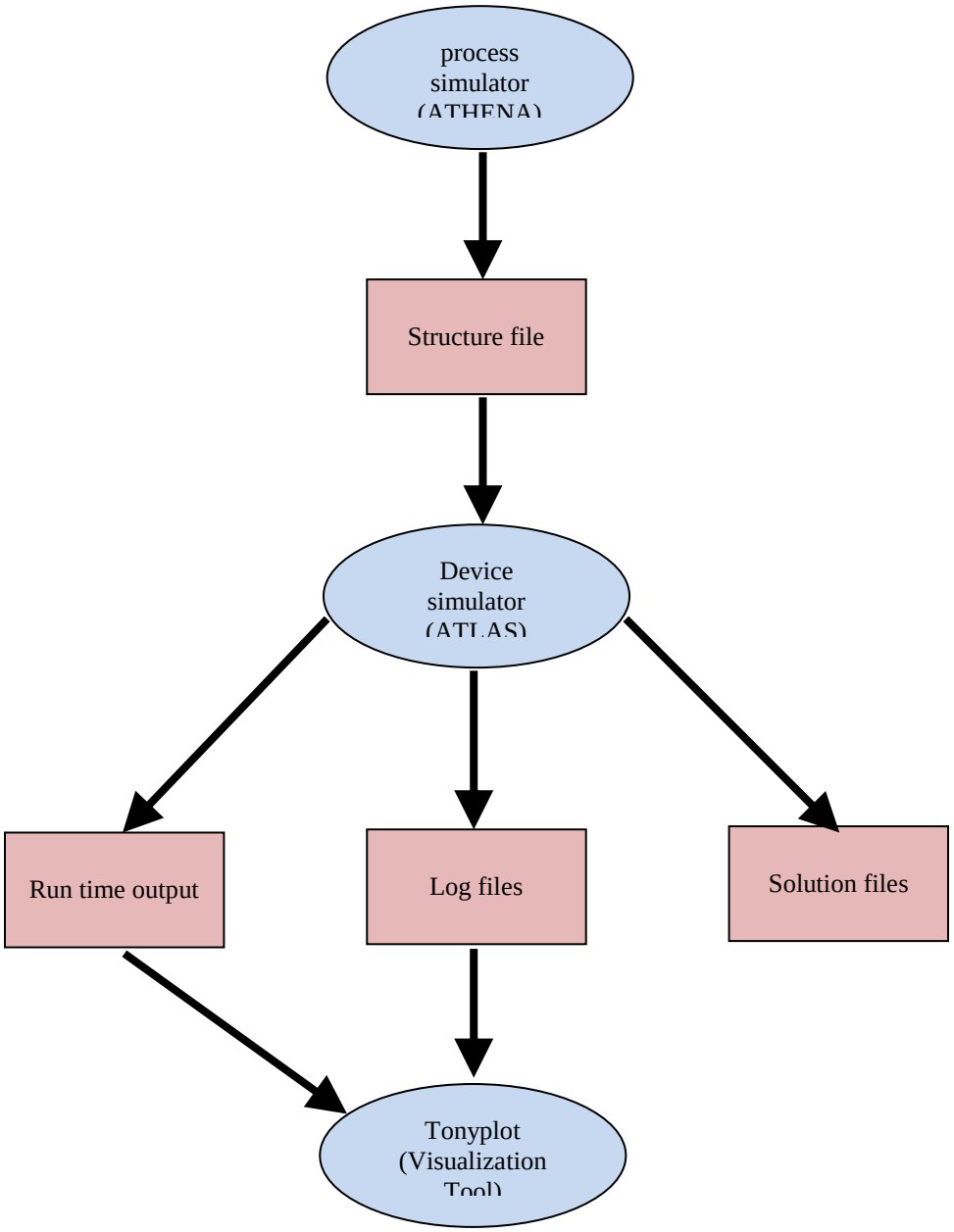

Figure 3.1 Design flow using ATHENA

The main objective of the ATHENA process simulator is to create a device structure by solving a set of system equations, which portray the chemistry and physics of semiconductor processes.

The predicted structure is used by the ATLAS device simulator for further electrical characterization of the device. ATHENA provides an appropriate and suitable platform for simulating processes such as oxidation, lithography, physical etching and deposition, diffusion, ion implantation which are used in the semiconductor industry. Two-dimensional (D) Physically-based process simulator ATHENA offers good features such as - fast and accurate simulation of the device; replacement of costly wafer experiments with simulations; providing advanced simulation environment. Basic operations to create the input file for ATHENA process simulator by using DECKBUILD's Commands.

- Building a fine simulation grid
- Specifying initial substrate
- deposition of layer
- Implementing geometrical etching
- Performing diffusion and ion implantation
- Defining the electrodes
- Saving the structure file

3.2.1 Describing a good simulation grid: Virtual fabrication of any device commenced with defining the initial simulation grid. Specifically, the simulation grid indicates the points where the model equations are resolved. The numbers of points (N_P) in a grid have a direct influence on simulation time and accuracy of the device. Therefore, specification of simulation grid plays a crucial role. So, a fine grid should exist only in the critical areas of the device where ion implantation will occur, where junctions will be formed.

3.2.2 Defining initial substrate: initialize the simulation structure, i.e. initializes the substrate region with its points, triangles, substrate orientation, background concentration with some additional parameters. By specifying Resistivity it can also possible to set background doping.

3.2.3 Performing layer deposition: Layer deposition technique is performed to create multi-layered structures. When shape of the deposited layer is not essential, this deposition technique can be used because it is the simplest deposit and default model. Planar and quasi-planar semiconductor regions use conformal deposition technique instead of the oxidation process, when doping redistribution is negligible. Using Grid Specification parameters, the number of nodes in the deposited layer is controlled.

3.2.4 Performing geometrical etching: Etching alludes to the expulsion of material from the surface of a wafer. The Geometrical etching is the default method. It can also be possible to get any arbitrary shape of geometrical etching by specifying X and Y positions of four arbitrary points. ATHENA etches surface layer within the described polygon, the polygon may consist more than four points. Dry etching is additional choice for geometrical etching, with a specified thickness. The width of the material can be specified by the THICK parameter.

3.2.5 Performing ion implantation and diffusion: Ion implantation is the important method used to directing ions into the semiconductor device structures. Ion implantation process is very important because advanced technologies come up with heavy doses, tilted implants, shallow doping profiles, and other modern methods. The following set of parameters should be specified while performing ion implantation

- Name of the impurity
- Implant energy in KeV
- Ionic dose

• Rotation angle in degrees

• Tilt angle in degrees

Implant energy controls the depth of the implantation i.e. it specifies the distance how far these ions are introduced. It is also possible to control the tilt and rotation angles of the ionic beam. If rotation angle is zero means that the ion beams is in parallel with the simulated surface. If it is 90° rotation means that the ion beam is directed perpendicular to the surface.

Diffusion functionality is similar to Ion Implantation. Diffusion controls the incorporation of impurity atoms into the semiconductor structures. The minimum set of diffusion parameters should be specified while performing diffusion:

• Diffusion Time

• Diffusion Temperature

• Atomic Gas pressure

It is a high temperature process, through this process of diffusion impurity atoms will diffuse into the substrate from high concentration.

3.2.6 Specifying the electrodes: The main objective of process simulator is to generate a device structure, which can be utilized by a device simulator for further electrical characterization. Specification of electrodes done with ATHENA even though ATLAS is capable to specify electrodes. ATHENA can attribute to specify an electrode to metal, silicide, and polysilicon region. Without having a metal region, it can also specify backside electrode placed at the bottom of the structure.

3.2.7 Saving the structure file: After each and every process step, the new structure files are saved by the DECKBUILD history functions mentioned in the "Standard Structure File (SSF) Format". These history files are limited i.e. 50. SSF Format is a universal file format which is

used by a SILVACO simulation program. The ATHENA structure command produces a Standard Structure File, which holds the solution information about mesh, models and other related parameters.

3.3 Brief discussion about models:

3.3.1 Oxidation Models: The oxidation process of semiconductor fabrication technology is used for the generation of gate dielectric regions. This thermal oxidation process step can also be used to create isolation between the regions, space regions and for mask regions which are used in ion implantation. In ATHENA thermal oxidation is modeled with a DIFFUSION statement. Oxidation takes place when the surface of the semiconductor device structures is exposed to an oxidizing ambient.

Table 3-1 Basic Oxidation Models

Type of model	Syntax	Speculation	Recommendation
Vertical (One -dimensional oxidation)	-	Planar	Generally not preferred
Compress model (Two-dimensional oxidation)	Method compress	Non-Planar with linear	Default method, When stress effects are negligible, this model is preferred to determining the shape of the oxide for all types of structures. .
Viscous elastic (Two-dimensional oxidation)	Method viscous	non-Planar with non-linear	This model is recommended, where stress effects are considered

3.3.2 Ion implantation models: Analytical and statistical methods are used by ATHENA to model ion implantation. Analytical models are used by default which is based on the recreation

of implant doping profiles from the computed distribution moments. The final distribution of stopped particles is calculated physically from the statistical technique on the basis of Monte Carlo calculation of ion trajectories.

Table 3-2 Implantation Models

Type of model	Syntax	Speculation	Recommendation
Gaussian implant model	Gauss	Analytical	Generally it is not an adequate because real Gauss Analytical profile is asymmetrical in nature.
Pearson implant model	Pearson	Analytical	This model is recommended, to obtain longitudinal implantation profiles.
Dual Pearson Model.	Pearson	Analytical	This model is recommended, when profiles are heavily affected by channeling
SIMS Verified Dual Pearson (SVDP) Model	Pearson	Analytical	This model is recommended, for B,P, BF2, As extraction
Monto-carlo implant model	Montecarlo	statistical	This model is recommended for non-planar structures and used when channeling is not described by SVDP

3.3.3 Diffusion models: Thermal processes of any device simulation redistribute the dopants because of concentration gradient effects and electric fields. ATHENA diffusion models describe how these implanted dopant profiles are redistributed. During modeling the actual diffusion process the additional effects such as impurity clustering, activation are considered.

Three most basic models are the following:

Table 3-3 Basic Diffusion Models

Type of model	Syntax	Speculation	Recommendation
Ferni model	Method fermi	Equilibrium defects	Recommended for Low concentration lower than $10^{20}cm^{-3}$; Inert ambient and fir low execution time
Two- dimensional model	Method two.dim	Point defect diffusion when dopant diffusion is independent, Transient defect diffusion; Dopant diffusion influenced by point defects;	Recommended for Oxidation Enhanced Diffusion and Implant dose lower than 1E13 cm-2
Fully coupled model	Method full.cpl	Two-way interaction between the dopant diffusion and point defect diffusion.	Recommended when implant dose more than 10^{13} cm^{-3}; Transient Enhanced Diffusion; Co-diffusion (Emitter Push Effect); RTA And for High execution time

These models are extensions of each other; Fermi model is subset of two-dimensional model, which is included in the fully coupled model.

3.3.4 Deposition models: While simulating deposition step using DEPOSIT statement, material and deposited layer thickness must be specified. This layer is deposited by a simple algorithm that illustrates conformal deposition technique which is a default method. The deposited layer is divided into a number of sub-layers which triangulated separately with thicknesses equal to grid spacing. The conformal deposition model produces unity step coverage. Within the ATHENA, ELITE provides set physical deposition models such as CVD deposition model, Dual Directional

Deposition, Planetary Deposition, Unidirectional Deposition, Hemispheric Deposition, Conical Deposition and Monte Carlo Deposition models.

3.3.5 Etch models: While simulating etching process using ETCH statement, material and its thickness must be specified. By default, ATHENA uses geometrical etching technique. Within ATHENA framework ELITE provides a set of Physical etching models such as Isotropic etch model, RIE model, Dopant enhanced etching model, plasma etch model and montecarlo etching model which are correspond to Real fabrication etching techniques

3.4 Device simulation using ATLAS

ATLAS simulations utilize two types of input: a text file with statements, and a structure file, that may be generated from the ATLAS or DEVEDIT or ATHENA. ATLAS creates three sorts of outputs.

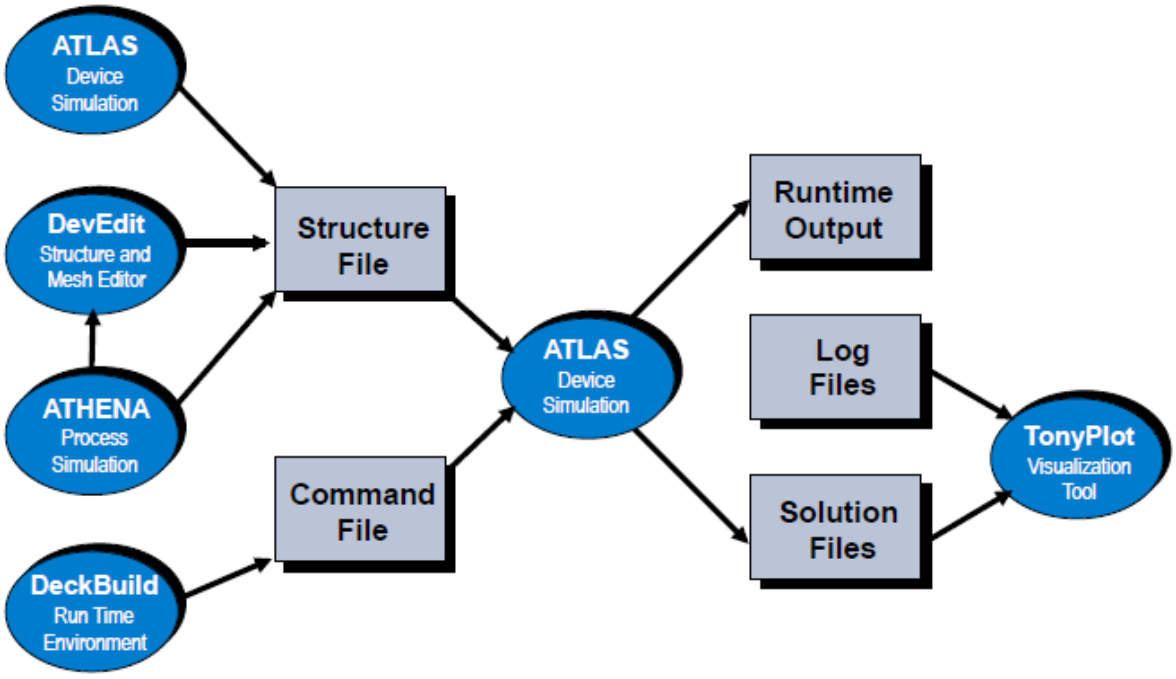

Figure 3.2 Design flow using ATLAS device simulator.

1) run-time output gives information about the simulations, which are running and it will show all warning messages and error messages. 2) Log files store every single terminal currents and voltages from the device analysis. 3) Solution files hold two and three dimensional information about device parameter values and process parameter value

There are five groups of commands, and the sequence of these commands must be in an order

GROUP	STATEMENTS
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Models Specification	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

3.4.1 Interface ATHENA: The structure which is generated from the ATHENA loads all the information about mesh, regions, electrodes and DOPING of the structure. This is done by the statement

3.4.2 Defining Material Parameters and Models: After defining the mesh, geometry, and doping profiles, ATLAS defines some physical models during the device simulation for

electrical characterization of the devices. These actions are achieved by using MODEL statements including MODELS, MOBILITY, IMPACT, and MATERIAL. ATLAS provides five groups of physical models.

- Mobility Models
- Recombination Models
- Carrier Statistics model
- Impact ionization models
- Tunneling models

These models inform Atlas to include some essential semiconductor physics in order to accomplish most exact simulation results.

3.4.3 Defining numerical Methods: Numerical methods are required to calculate the solutions to semiconductor device problems. This can be done by using Method statement. Different situations demand different solution methods. Basically there are 3 types of solutions.

1. De-coupled technique
2. Fully-coupled technique
3. Block

De-coupled technique such as Gummel method, which solve for every unknown while maintaining the other variables as constant and repeating the same process till a stable solution is attained. Fully coupled technique uses the Newton method, which solve for all the system unknowns together and Block methods solve few equations by fully coupled, and remaining by de-coupled.

3.4.4 Obtaining Solutions: ATLAS calculates all types of solutions such as AC, DC and also transient analysis. ATLAS calculates each electrode current by defining voltages on electrodes in

the device. It also calculates internal quantities, such as carrier concentrations and electric fields throughout the device. In all device simulations all electrodes start with zero bias. By stepping these electrode biases from initial equilibrium, complete Solutions are obtained.LOG and SAVE statements are used to save results.

3.4.5 Interpreting The Results: RUN-TIME OUTPUT - This run-time output holds the run-time messages generated by ATLAS. These messages usually include significant values obtained from the simulation. When simulation fails, this run-time output stores all error and warning messages.

LOG FILES - Stores the DC, AC small signal and transient characteristics for a sequence of SOLVE statements. To visualize the device characteristics, these are loaded into TONYPLOT.

SOLUTION FILES - Solution files store each and every node physical quantities of the simulation grid of the structure for a single bias point. This solution files can be shown in TONYPLOT to check the internal distributions of all parameters.

CHAPTER 4

4. VIRTUAL FABRICATION OF SHORT CHANNEL RECESSED-SOURCE/DRAIN SOI MOSFETs

4.1 Introduction

This chapter describes process and device simulation results of short-channel Recessed-Source/Drain (Re-S/D) SOI MOSFETs and also presents the virtual fabrication of 30nm short channel Re-S/D SOI MOSFET with reduced short channel effects (SCEs) and low source/drain series resistance. Several processing steps such as oxidation, deposition, etching, ion implantation and lithography which are required to obtain the structure of the Re-S/D SOI MOSFET are explained in detail. The electrical characteristics such as drain current (I_{ds}) versus drain to source voltage ($V_{DS)}$ have been explored for different values of gate to source voltage (V_{GS}). Also variation of drain current (I_{ds}) with the drain to source (V_{DS}) voltage for different values of recessed S/D thickness (t_{rsd}) have been evaluated. Analysis had been carried out to understand the influence of gate oxide thickness and recessed source/drain thickness on sub-threshold swing.

4.2 Device structure in detail

The cross section of n type Re-S/D SOI MOSFET is as shown in Figure 4.1. This structure consists of thin silicon layer (t_{si}) which is sand witched between a very thin layer of gate oxide layer (t_{ox}) and buried oxide layer (t_{box}) where buried oxide layer is mounted on the p-type silicon substrate with thickness (t_{sub}), thickness of Source/drain region (t_{rsd}) is greater than the channel thickness which is extended into the buried oxide region. Both source and drain are

symmetrically and heavily doped with n-type impurity atoms by using pearson implantation method. The channel is lightly doped with p-type impurity atoms using Pearson implantation process. gate is uniformly doped with n-type impurity atoms because poly-silicon is used as a gate instead of metal. The work function of gate depends on the impurity concentration of poly-silicon. the source and drain electrodes are made up of depositing aluminum metal with work functions less than the gate metal. Table 4.1 lists the parameter values which are used for process simulation of Re-S/D SOI MOSFET. The symbols L, t_{Si}, t_{ox}, t_{box} and t_{rsd} represent the gate length, channel thickness, gate oxide thickness buried oxide (BOX) depth and recessed source/drain (Re-S/D) thickness respectively

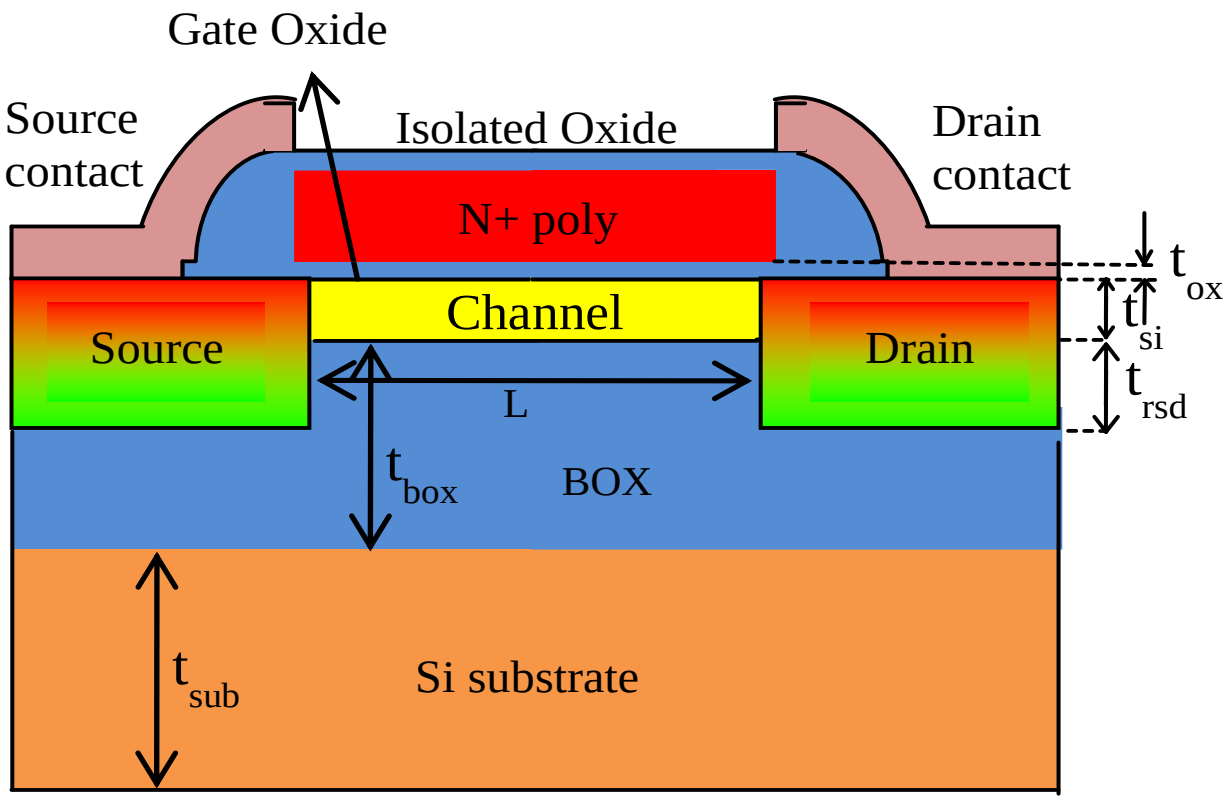

Figure 4.1 Structural view of Recessed source/drain SOI MOSFET

Table 4-1 Device and Process Parameter values for simulation of device under consideration

Serial number	Process/Parameter	value
1	Channel length(L)	30nm
2	Buried oxide thickness(t_{box})	180nm
3	Substrate thickness	400nm
4	Recessed source/drain thickness	30nm
5	Channel implantation	Boron impurity, energy=7KeV, dose= of $3x10^{12}$ cm^{-3}
6	Gate oxide growth	Dry O_2, temp=850^0C, time=3min
7	Poly silicon deposition	Phosphorus conc.=10^{18} cm^{-3}, thickness=40nm
8	Drive in diffusion	In nitrogen, temp=800^0C, time=11min
9	LDD implantation	phosphorus impurity, energy=5KeV, dose= of10^{13} cm^{-3}
10	Source/drain implantation	Arsenic impurity, energy=15KeV, dose= of $5x10^{14}$ cm^{-3}
11	Metal deposition	Aluminum, thickness=20nm

4.3 Device operation:

SOI refers silicon on insulator technology. Thin silicon layer is sand witched between the gate oxide and buried oxide. The recessed source/drain SOI MOSFET provides channel coupling between the extended source/drain regions into the buried oxide and the channel. The coupling

capacitors between the source/drain and channel are increasing while extending source/drain regions into the buried oxide which leads to decrease in series resistance, resulting the current driving capability of the device is increased and also exhibit better short channel immunities such as drain-induced barrier lowering (DIBL) and sub threshold slope.

4.4 Process flow

The process flow of recessed source/drain SOI MOSFET (Re-S/D SOI MOSFET) lists the necessary steps to fabricate and characterize the 30nm channel length Re-S/D SOI MOSFET. By considering a symmetrical MOSFET i.e. the regions from the center of the channel to source and center of the channel to the drain are identical to each other. By using a special facility from ATHENA that half of the structure (region from the center of the channel to source) is fabricated first and then the other half structure (region from the center of the channel to drain) is generated using the command "structure mirror".

- Initialization
- Re-S/D formation
- Oxide growth and etching
- Chanel formation
- Gate oxide growth and highly doped poly silicon gate deposition
- Source and Drain implantation
- Metal deposition and etching
- Mirror imaging the structure
- Electrode specification

Initialization: The process flow of Re-S/D SOI MOSFET commenced with defining the initial simulation grid. P-type <100> SOI wafer with 400nm thick Si substrate, 180nm thick buried

oxide (BOX), 20nm thick SOI layer and background doping of 10^{14} cm^{-3} are considered as shown in Figure 4.2

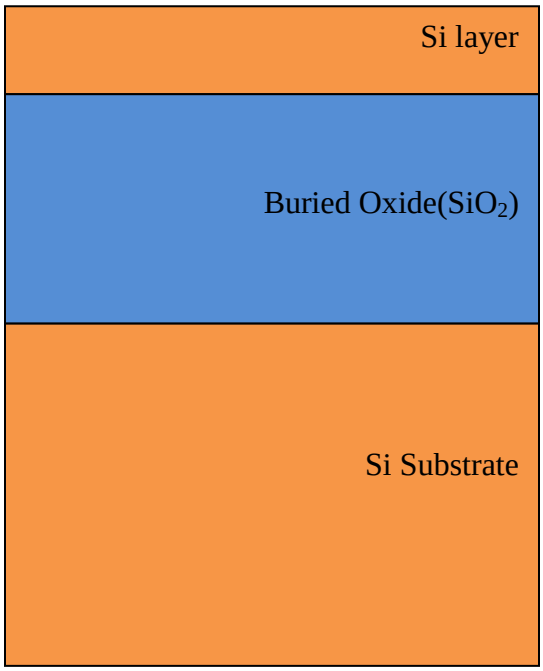

Figure 4.2 SOI wafer

Re-S/D formation: The process of creating Re- S/D above the BOX is as follows: Firstly, SOI layer is etched by using geometrical etching technique as shown in Figure 4.3.1 and then the oxide layer with thickness greater than the silicon layer thickness is deposited using conformal deposition technique as shown in Figure 4.3.2. After that, etching of oxide is carried out to planar structure as shown in Fig 4.3.3. Again, conformal deposition technique is used to deposit Si layer of thickness 20nm which is exposed to perform further processing steps as shown in Figure 4.3.4.

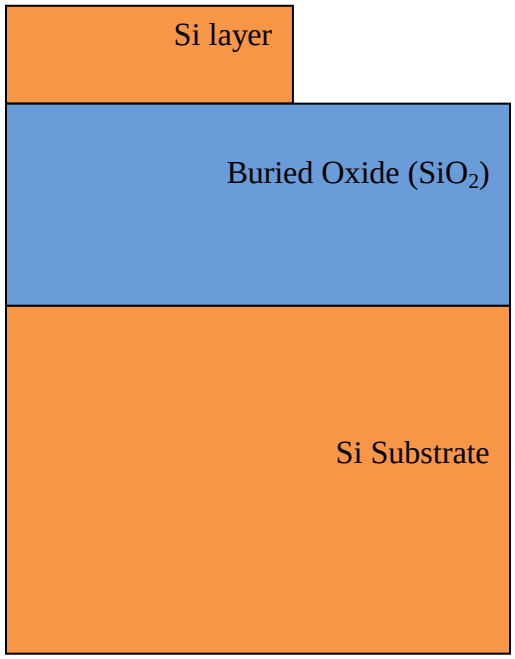

Figure 4.3.1 Etching of silicon

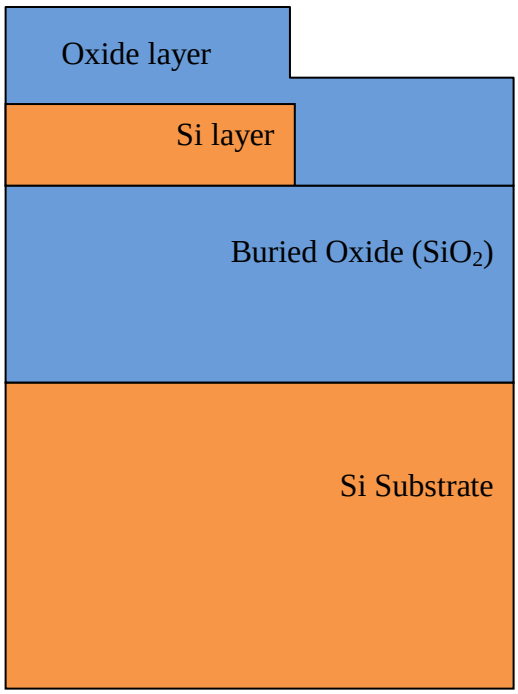

Figure 4.3.2 Deposition of oxide layer

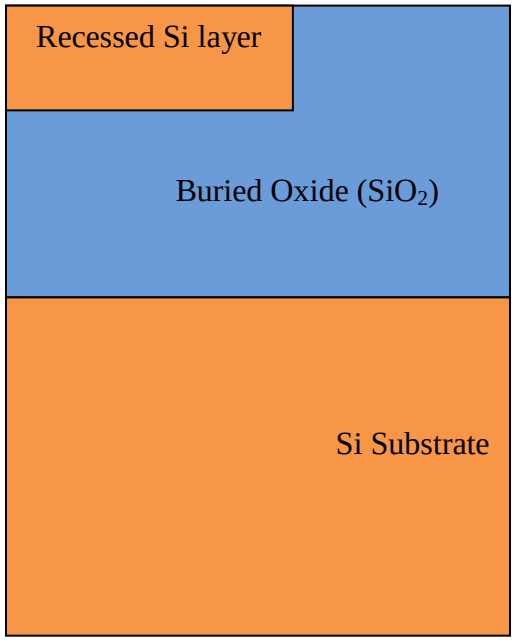

Figure 4.3.3 Planarizing the structure

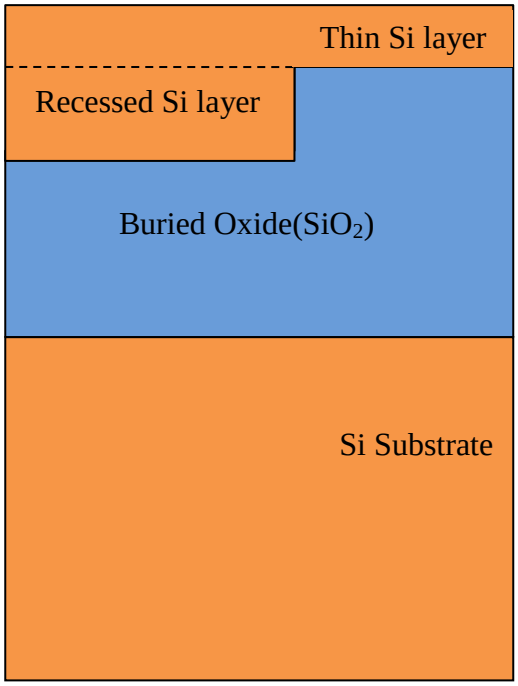

Figure 4.3.4 UTB deposition

Figure 4.3 Re-S/D formation

Oxide growth and etching: Dry oxidation is carried out at 1000^0C for 30 minutes in dry O_2 at 1 atmospheric pressure with the addition of 3% HCl as shown in Figure 4.4.1. Following oxide (SiO_2) growth, the oxide is etched back to a precise thickness to facilitate ion implantation that comes in the next step as shown in Figure 4.4.2. Subsequently, the top Si layer is thinned to 10nm by thermal oxidation process.

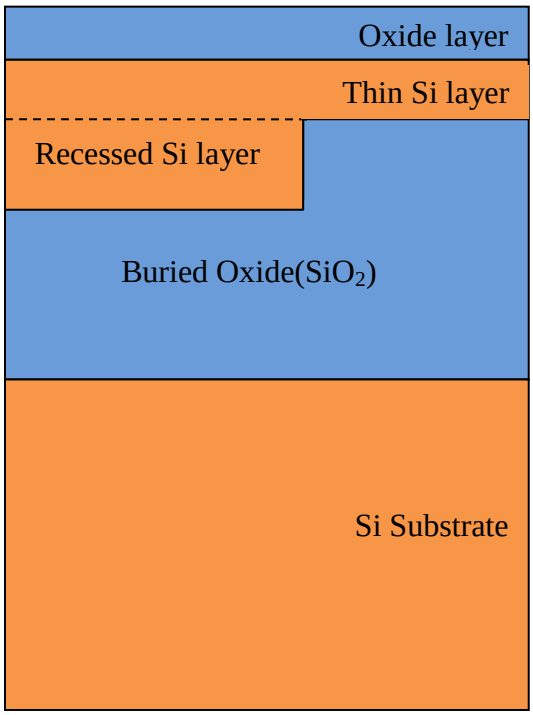

Figure 4.4.1 Oxide growth

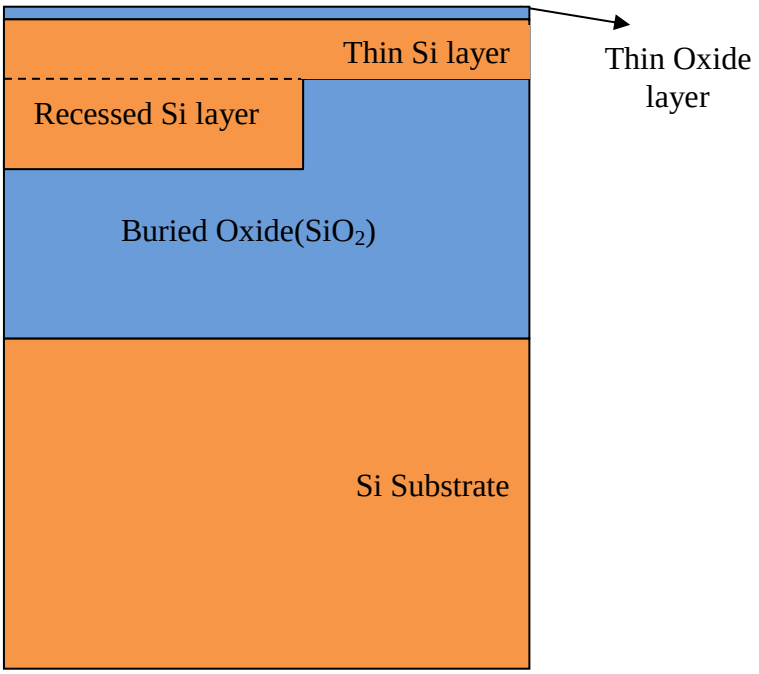

Figure 4.4.2 Etching of oxide

Figure 4.4 Oxide growth and etching

Channel formation: Photo resist barrier is used to mask the S/D region. First photo resist barrier is deposited and part of this layer is etched to create window just above the channel, through which impurity atoms are entered into the surface layer as shown in Figure 4.5.1 Boron ion implantation is carried out at 7KeV of implantation energy with dosage of $3x10^{12}$ cm^{-3} in the channel region as shown in the Figure 4.5.2.

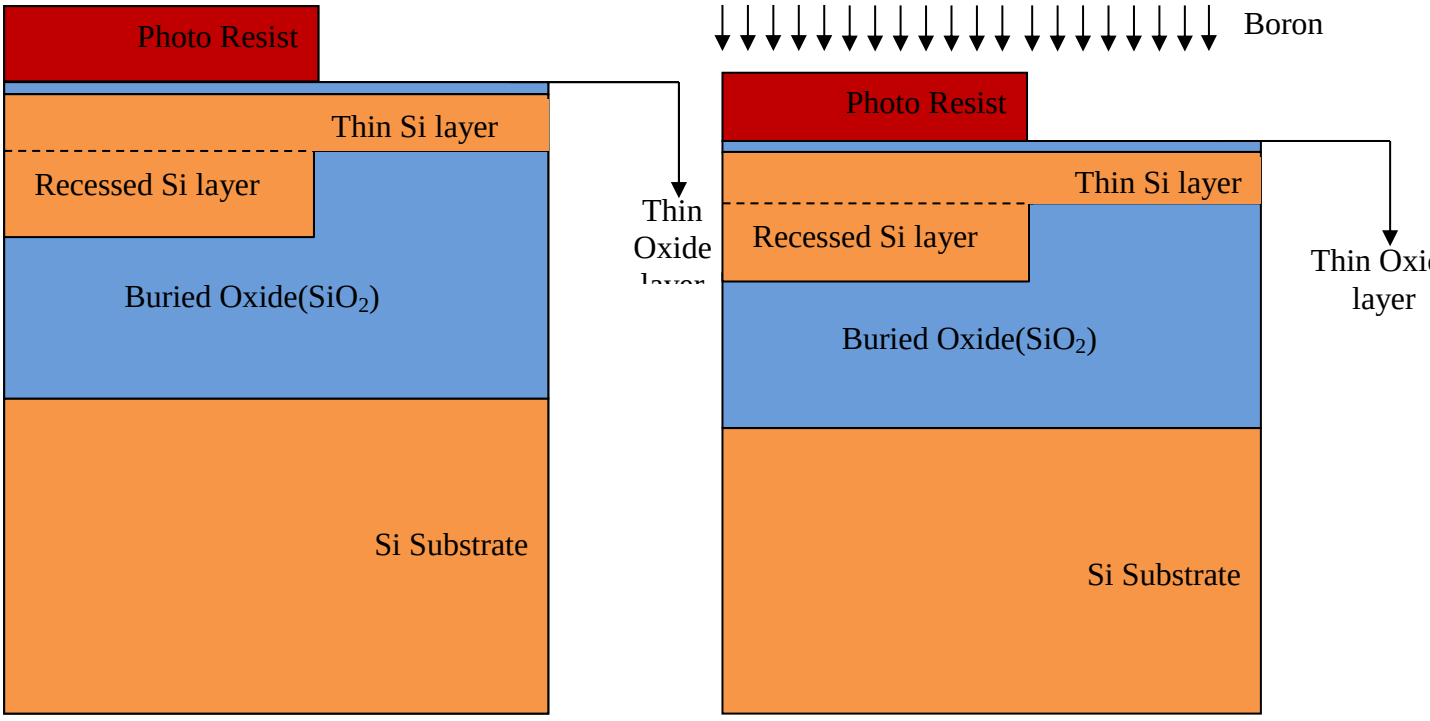

Figure 4.5.1 Masking of S/D region

Figure 4.5.2 Adding boron impurity

Fig. 4.5 channel formation

Gate oxide growth and highly doped poly-silicon gate deposition: Gate oxide (SiO_2) layer is developed by dry oxidation process which is performed at relatively low temperature of 850^0 C for a small time interval of 3 minutes. Heavily doped poly-silicon which is advantageous in terms of its high conductivity is utilized as gate instead of metal. Poly silicon of thickness 40nm is doped with phosphorus of concentration 10^{18} cm^{-3} and deposited with conformal deposition technique as shown in Fig 4.6.1. Further etching of poly-silicon and gate oxide are carried out from x = 0 to 0.03µm on the left side of the gate to make a window for the source implantation which comes in the next step and to define the gate as shown in the Fig 4.6.2. The statements which are defined in the mesh specify a total length of half structure is 0.045µm. Therefore

etching of this poly-silicon indicates half channel length of (0.045 – 0.03) = 0.015µm. Hence the total channel length of this device is 30nm.

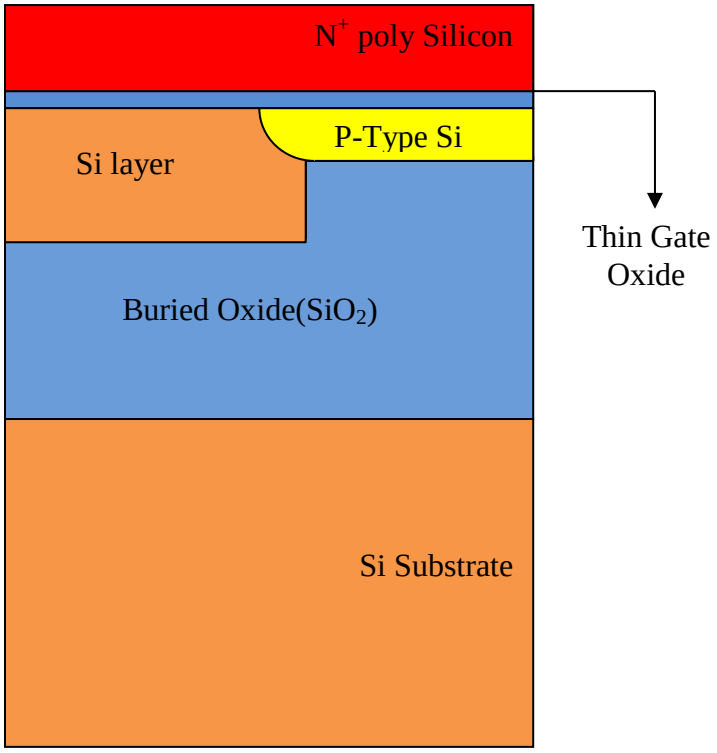

Figure 4.6.1 Gate oxide growth and deposition of highly doped poly silicon

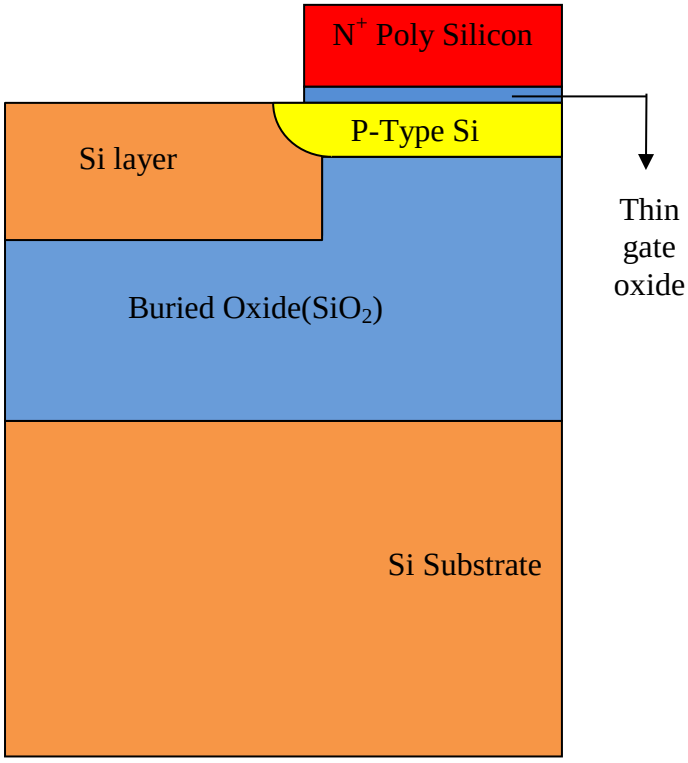

Figure 4.6.2 Etching of polysilicon and oxide

Fig. 4.6 Gate oxide growth and highly doped poly-silicon gate formation

Source and Drain implantation: The next process is the development of source/drain (S/D) using two implantations: phosphorous and arsenic. These implantations are followed by some drive-in diffusion, which are performed at 800^0C in nitrogen for 11 minutes. Wet oxidation is carried out for small interval of time and etched back to provide small thickness of oxide layer above the surface, which is acts as isolated layer between the devices as shown in Figure 4.7.1. If the voltage levels are not scaled simultaneously with the shrinking size of the device, there may be a rise in the electric field in the channel region resulting in hot electron current, in which

electrons approach quickly, scattering into the gate oxide region. To overcome this problem phosphorous implantation is carried out to create a lightly doped drain (LDD) region, which decreases electron energy gradually as electrons approach the drain. Arsenic implantation is carried out with high dosage of $5x10^{14}$ cm^{-3} and the implant energy is 15keV to build the low resistance in the source and drain region as shown in Figure 4.7.2.

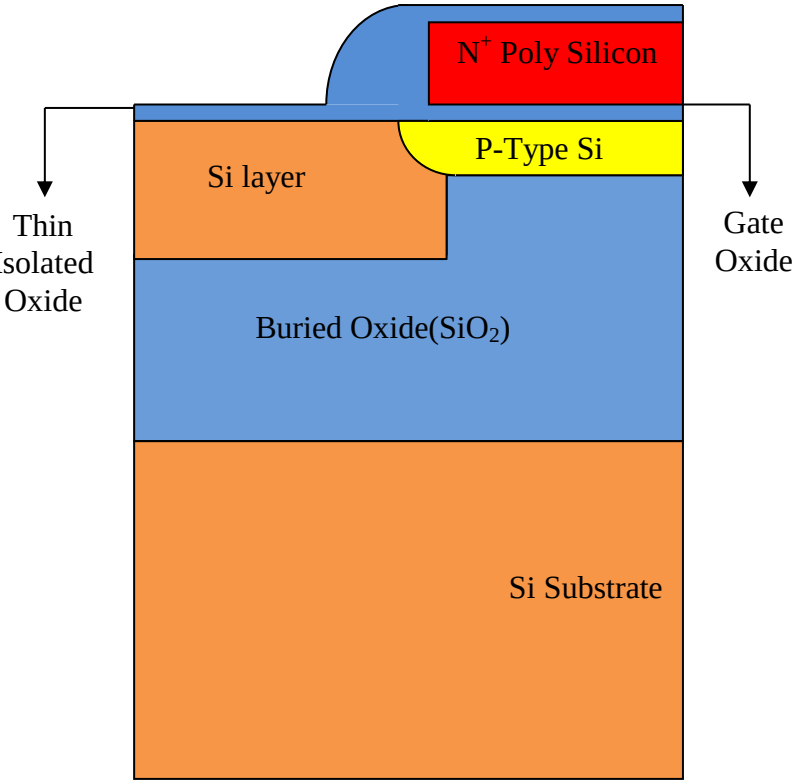

Figure 4.7.1 Field oxide growth

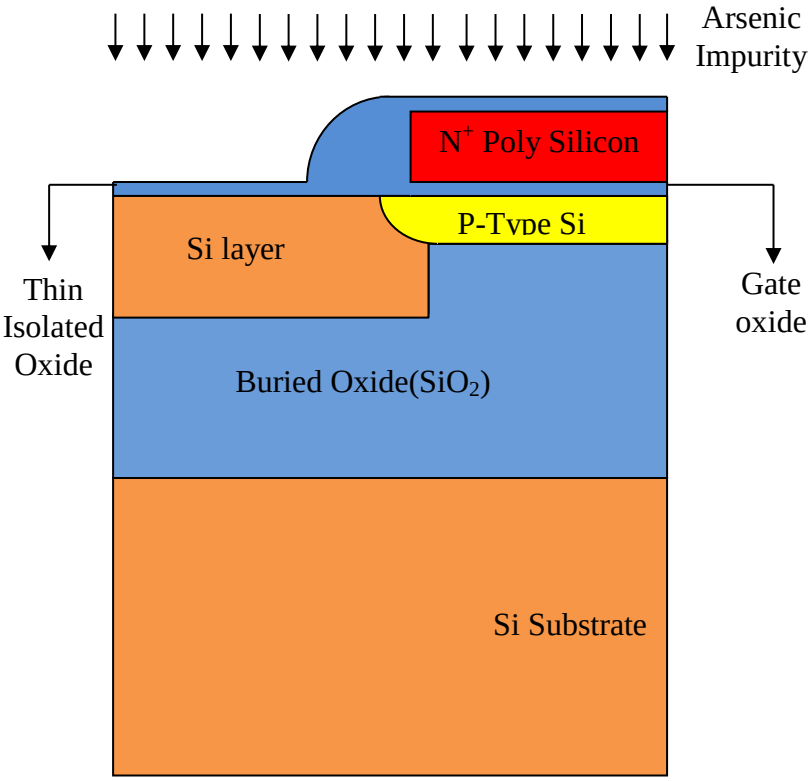

Figure 4.7.2 Adding arsenic impurity

Fig. 4.7 source/drain implantation

Metal deposition and etching: For providing electrical contact to the source/drain, Aluminum (Al) is deposited. Later, oxide on the left side of the device is etched for depositing Al of thickness 20nm and the contact is shaped by etching part of the aluminum on the right side as shown in Figure 4.8. This completes the virtual fabrication of half of the device.

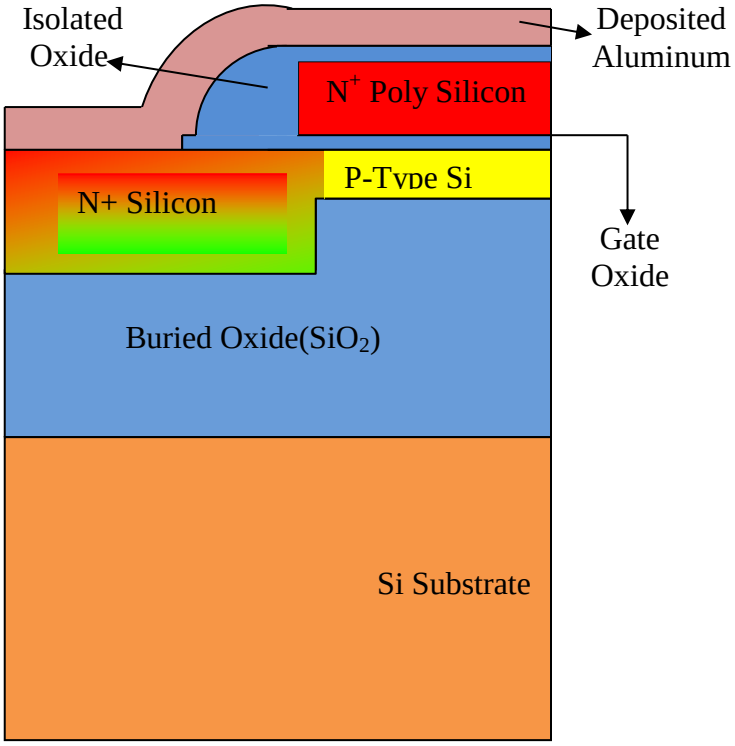

Figure 4.8.1 deposition of aluminum metal

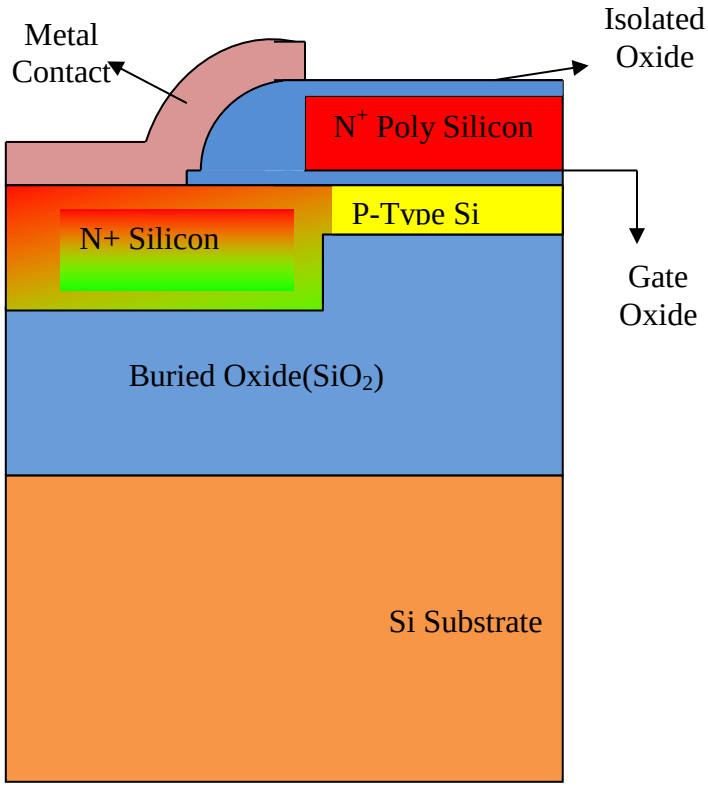

Figure 4.8.2 etching of aluminum

Fig. 4.8 Source and drain metal deposition

Electrode specification and mirror imaging the structure: On mirror imaging the above obtained half structure the full structure of Re-S/D SOI MOSFET is formed. This completes the simulation of other half also. Figure 4.9 shows the schematic of complete structure of Recessed-S/D SOI MOSFET. The next step in the process flow is naming the electrodes. There are four electrodes those are gate, source, drain, and substrate.

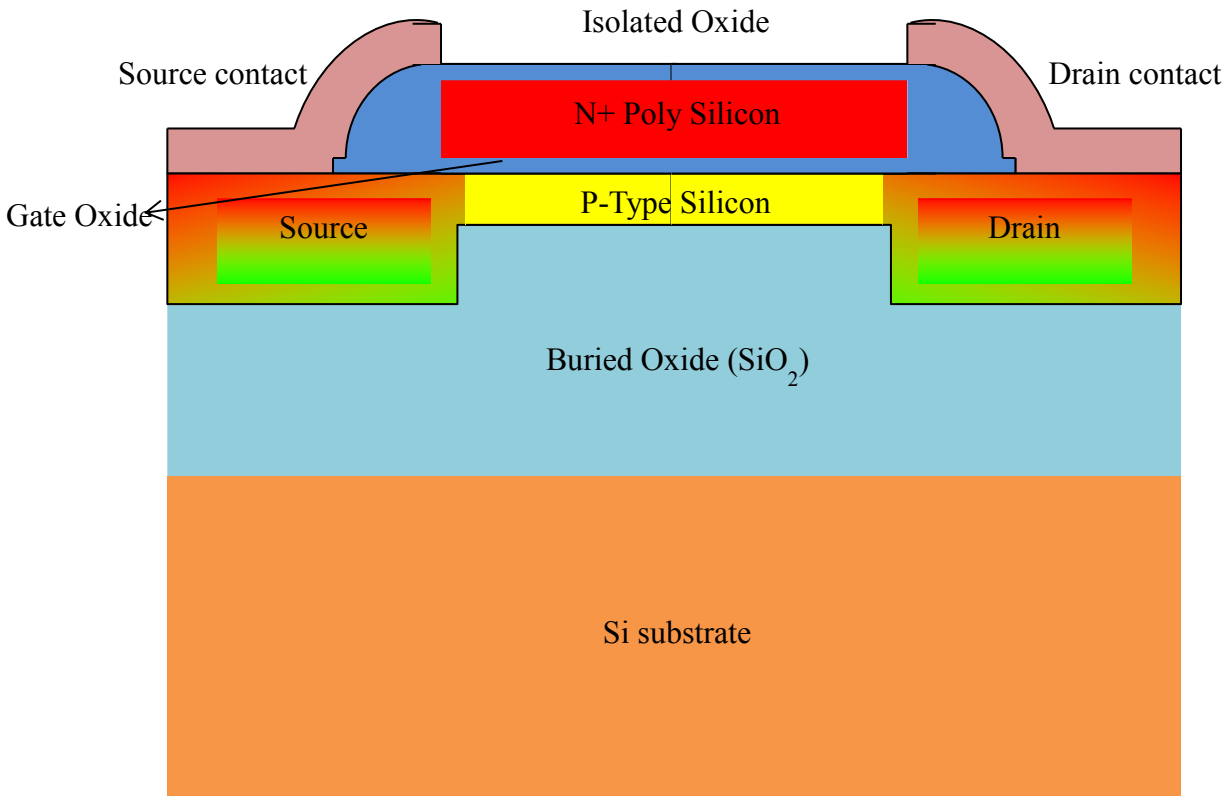

Figure 4.9 Final structure of the Re-S/D SOI MOSFET structure

4.5 Simulation results and discussion

Figure 4.10 shows the variation of net doping in source, channel and drain regions of 45nm channel length Re-S/D SOI MOSFET. The heavily doped n-type source/drain regions are formed by arsenic implantation with an energy of 20 keV and a dosage of $5x10^{13}$ cm-3 . The channel region is doped with boron impurity, with implant energy of 7 keV and a dosage of $5x10^{13}$ cm^{-3}. The ion beam used for both implantations is tilted by 7^0 and rotated by 30^0. The peak concentration in the source/drain regions and channel regions are observed as $5x10^{19}$ cm^{-3}, $3x10^{18}$ cm^{-3} respectively.

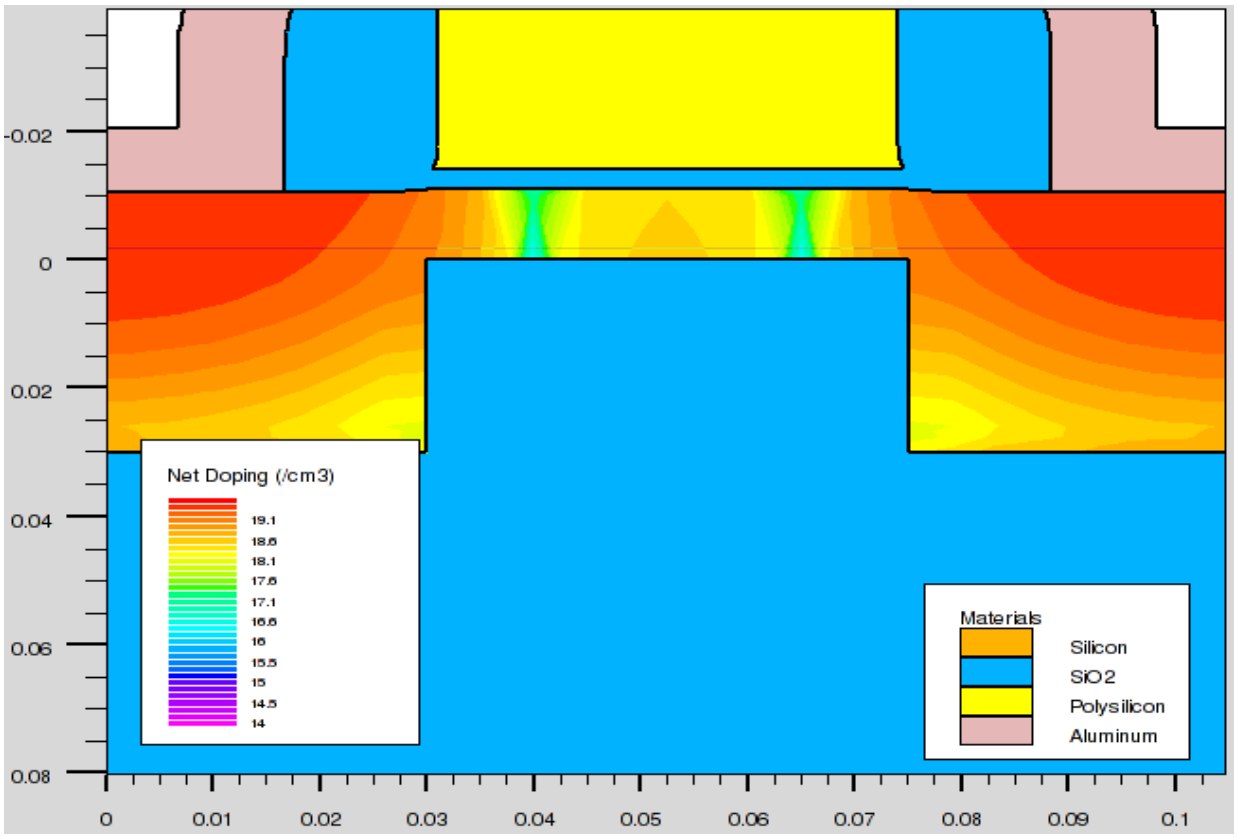

Figure 4.10 Schematic diagram of net doping in source, channel and drain regions of a Re-S/D SOI MOSFET

where, t_{si}=10nm L=45nm L1=30nm t_{ox}=3.2nm t_{box}=200nm t_{rsd}=20nm

Figure 4.11 shows the acceptor and donor doping profile along the cutline taken from source to drain region. The effective channel length of the device becomes 30nm due to lateral penetration of source/drain implantation.

Figure 4.12 shows drain current (I_{ds}) plot with respect to drain to source voltage (V_{DS}) for different gate to source voltages (V_{GS}) considering a step of 0.4V. The drain current (I_{ds}) is found to be increased with drain to source voltage (V_{DS}).

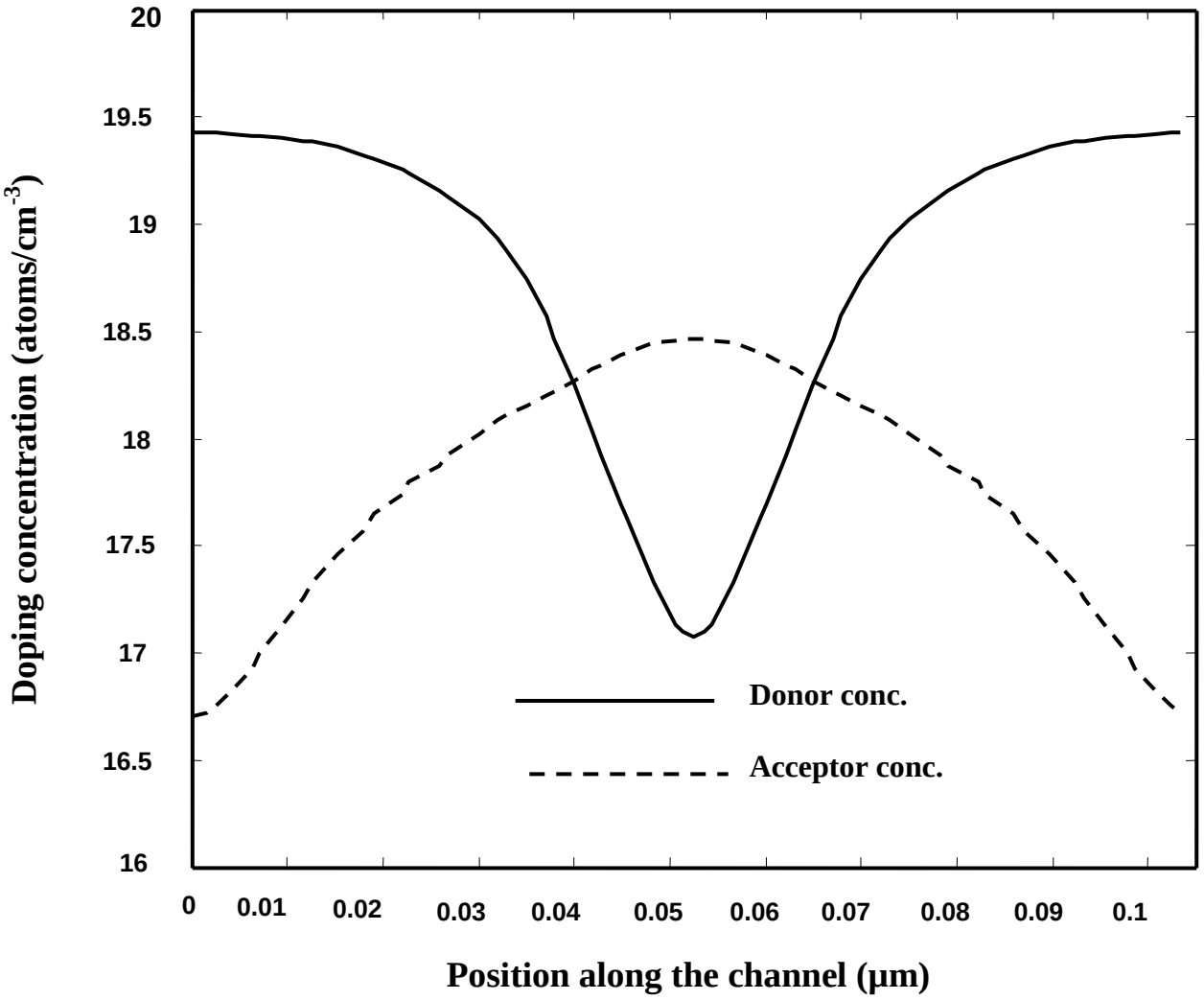

Figure 4.11 Acceptor and donor doping profile along the cutline taken from source to drain where, t_{si}=10nm L=45nm L1=30nm t_{ox}=3.2nm t_{box}=200nm t_{rsd}=20nm

Figure 4.13 shows the effect of recessed source/drain thickness (t_{rsd}) on drain current (I_{ds}) by keeping all other device parameters constant. It also depicts the Ids-VDS characteristics of Re-S/D SOI MOSFET where t_{rsd} varies from 0 to 30nm with step size of 10nm; when t_{rsd}=0nm, the device simply replicates conventional SOI MOSFET. From this figure it is observed that the on-current driving capability of the device increases with recessed-S/D thickness (t_{rsd}).

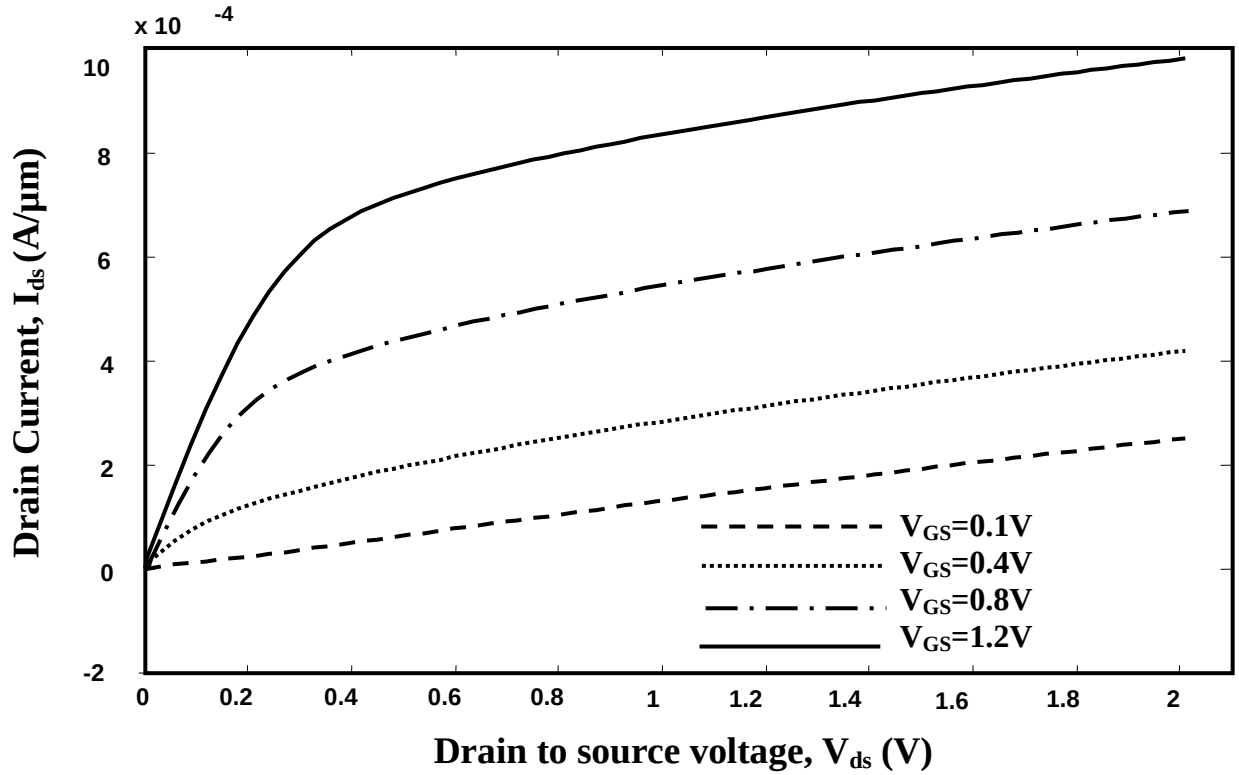

Figure 4.12 Drain current versus Drain to source voltage for different Gate to source values.

where, t_{si}=10nm L=45nm L1=30nm t_{ox}=3.2nm t_{box}=200nm t_{rsd}=20nm

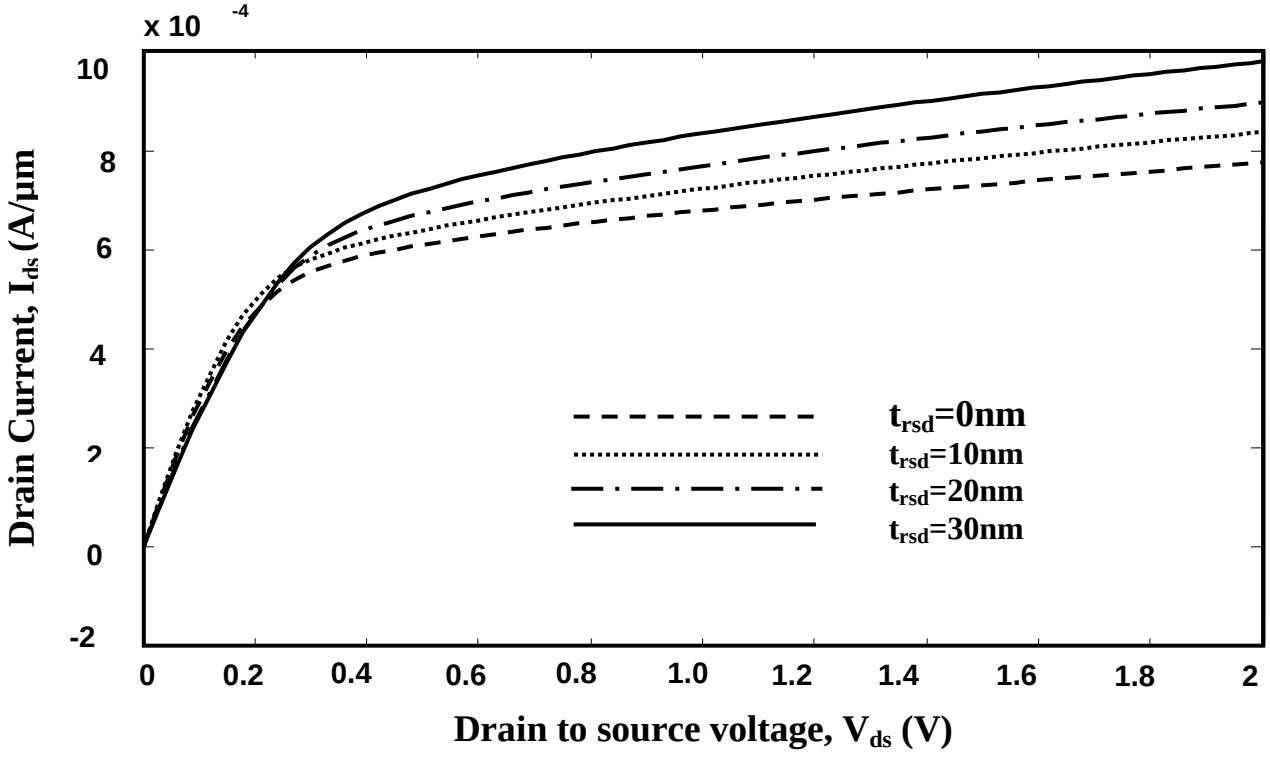

Figure 4.13. Drain current versus Drain to source voltage for different recessed source/drain thicknesses

where, t_{si}=10nm L=30nm t_{ox}=3.2nm t_{box}=200nm t_{rsd}=20nm

Fig 4.14 shows the influence of gate oxide thickness on sub threshold swing. From this figure it is observed that Sub threshold swing of the device gets reduced with the decrease in the gate oxide thickness results in improved the switching characteristics

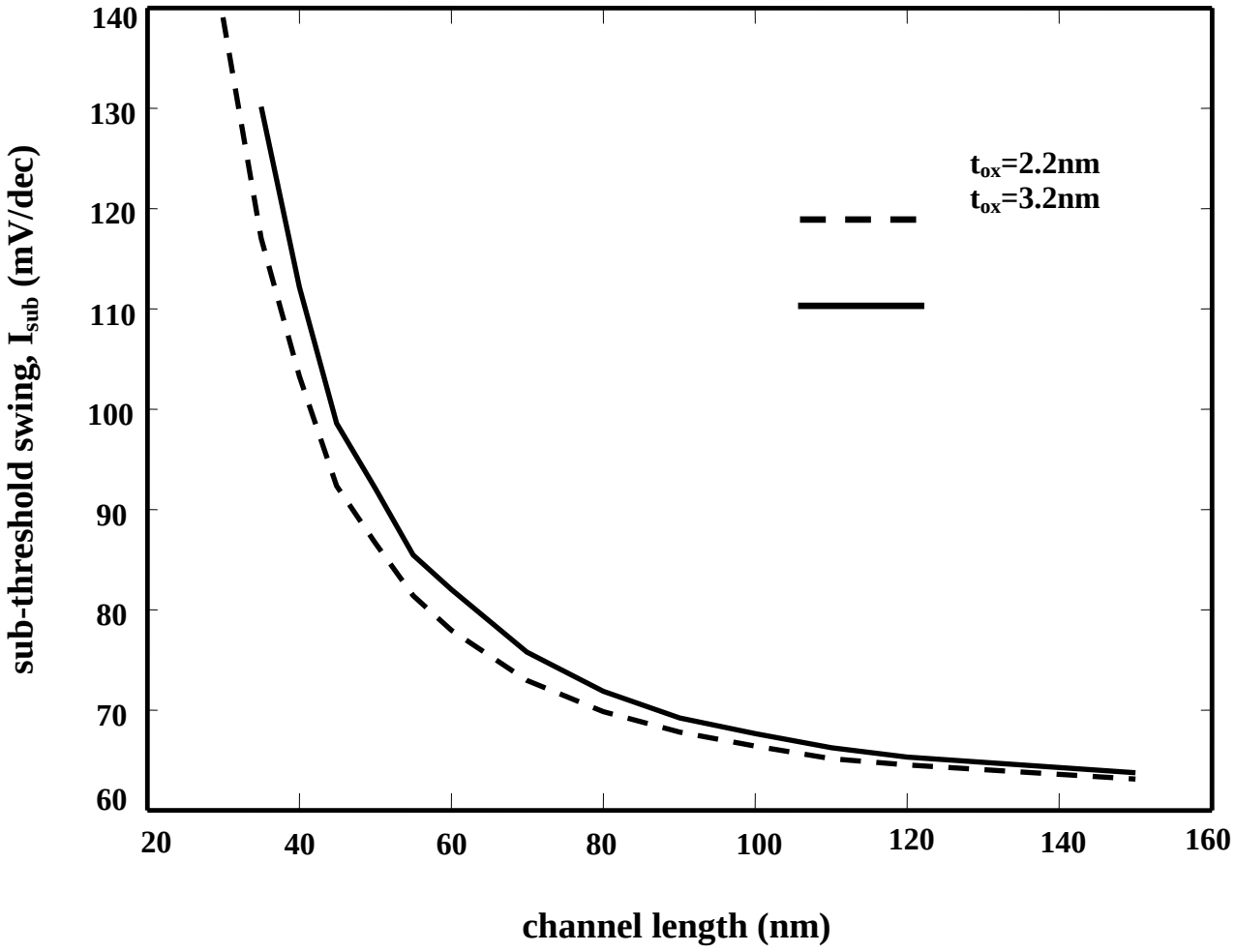

Figure 4.14. Sub threshold swing versus channel length of Re-S/D SOI MOSFET for different oxide thickness values

where, t_{si}=10nm, L=30nm, t_{box}=200nm,t_{rsd}=20nm

Fig 4.15 shows the sub threshold swing variation with the device channel length for different recessed source/drain thicknesses. Higher values of sub threshold swing can be observed with the increasing recessed-S/D. from Figs. 4.13 and 4.15, it is concluded that a trade-off between on-current and sub threshold current.

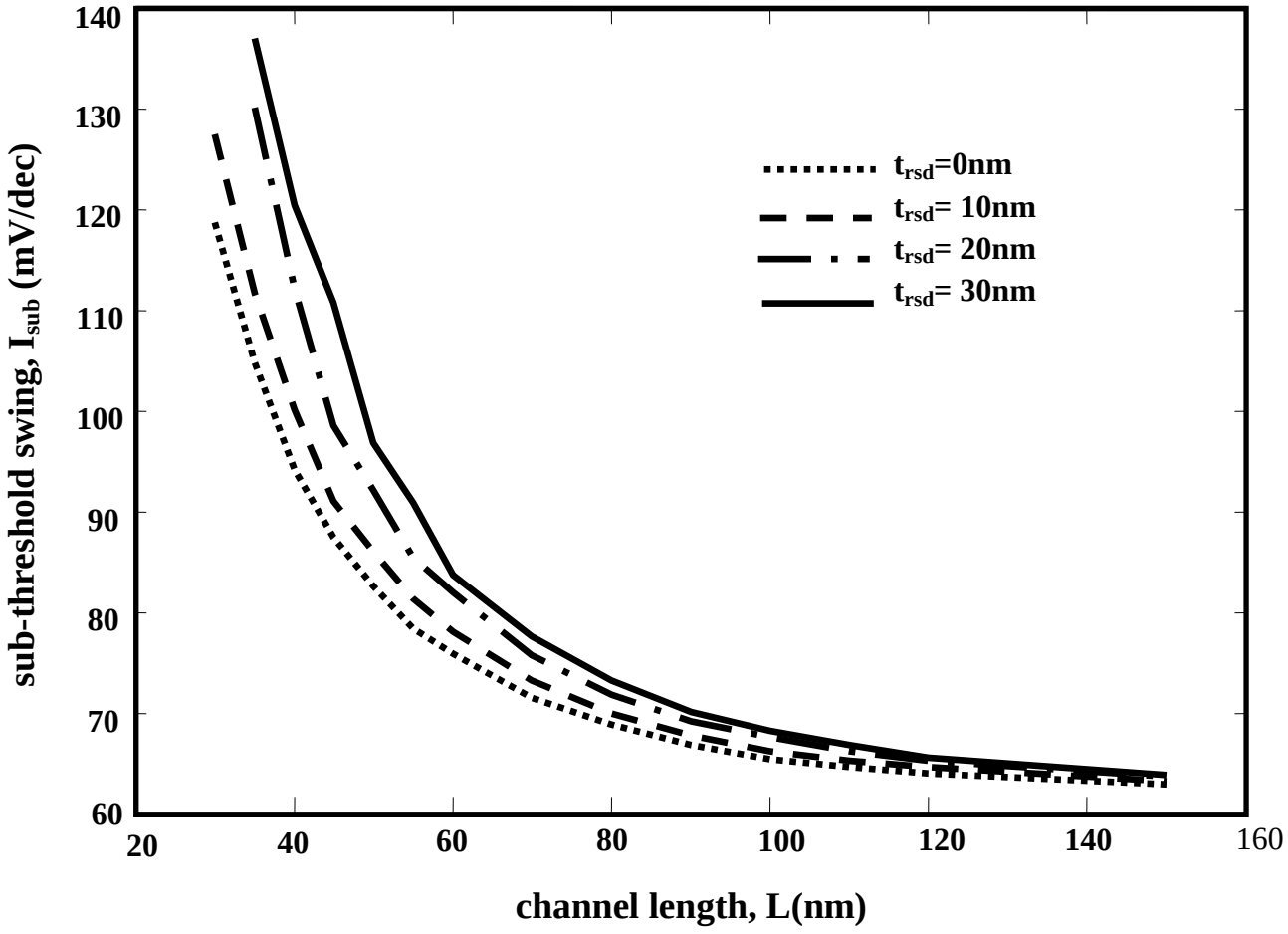

Figure 4.15 Sub threshold swing versus channel length of Re-S/D SOI MOSFET for different recessed souce/darin thickness values

where, t_{si}=10nm, L=30nm, t_{box}=200nm, t_{ox}=20nm

CHAPTER5

5. VIRTUAL FABRICATION OF SHORT CHANNEL DUAL-METAL-GATE RECESSED-SOURCE/DRAIN SOI MOSFETs

5.1 Introduction

This chapter describes process and device simulation results of short channel dual-metal-gate (DMG) Recessed-Source/Drain (Re-S/D) SOI MOSFETs and also presents the virtual fabrication of 45nm short channel Re-S/D SOI MOSFET. Several processing steps such as oxidation, deposition, etching, ion implantation and lithography, which are required to obtain the structure of the DMG Re-S/D SOI MOSFET, are explained in detail. The electrical characteristics such as threshold voltage (V_{th}) versus channel length for different gate length ratios, surface potential along the channel length, subthreshold current (I_{sub}) versus Gate to source voltage (V_{GS}) for different gate length ratios are observed. Also variation of drain current (I_{ds}) with the drain to source (V_{DS}) voltage for different values of recessed S/D thickness (t_{rsd}) and for different gate length ratios have been evaluated

5.2 Device structure and its operation

The cross section of short channel n type DMG Re-S/D SOI MOSFET is as shown in Figure 5.1. This structure consists two metals M1 and M2 with different work functions in place of single metal gate, where work function of M1 (deposited towards the source side) is greater than the other which is deposited towards the drain side. L1 and L2 are the lengths of the metal1 and metal2, where M1 acts as a control gate which is responsible for calculating threshold voltage of the device and M2 acts as screening gate which screens the effect on channel region due to drain

bias. This configuration provides suppressed short channel effects and high trans-conductance due to a step change in the surface potential profile when it is compared with a single metal gate structure. The drain end of the DMG structure have less peak electric field which increases the average electric field under the gate. Resulting in increased device lifetime, ability to increase the drain resistance due to reduction of localized charges, increased gate transport efficiency due to more controllability of gate over the channel conductance.

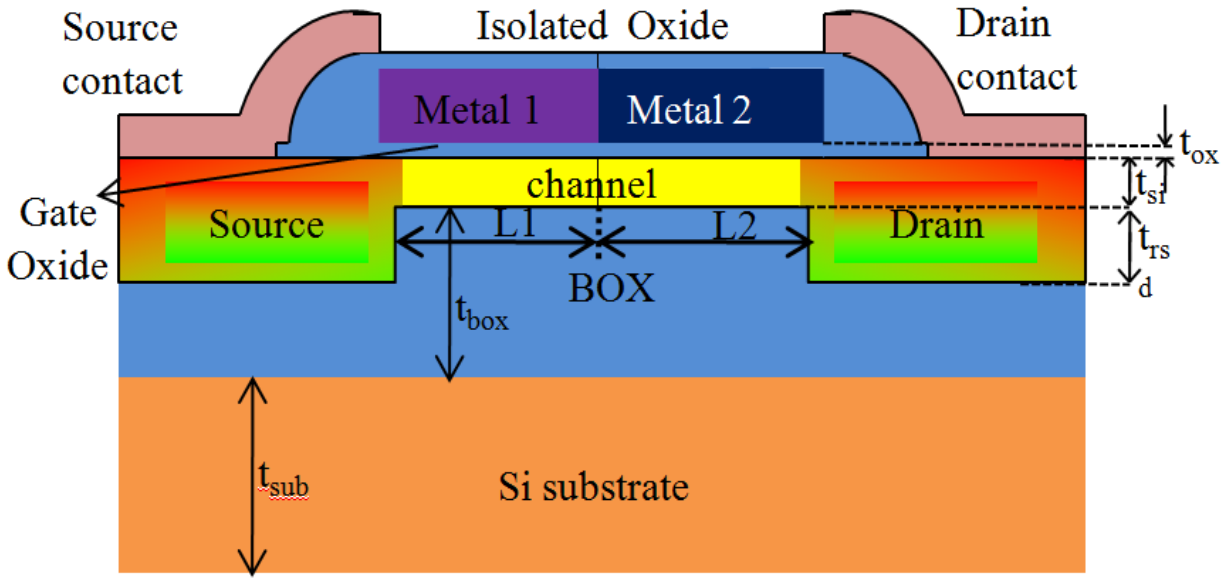

Figure 5.1 Structural view of dual metal gate Recessed-source/drain SOI MOSFET

Table 5-1 Device and process parameter values for simulation of DMG Re-S/D SOI MOSFET

Serial number	Process/Parameter	value
1	Channel length(L)	45nm
2	Buried oxide thickness(tbox)	200nm
3	Substrate thickness	400nm, background doping=10^{14} cm^{-3}

4	Recessed source/drain thickness	30nm
5	Channel implantation	Boron impurity, energy=2KeV, dose of $3x10^{12}$ cm^{-3}
6	Gate oxide growth	Dry O_2, temp=850^0c, time=3min
8	Drive in diffusion	In nitrogen, temp=1000^0c, time=15min
10	Source/drain implantation	Arsenic impurity, energy=25KeV, dose= of $5x10^{14}$ cm^{-3}
11	Metal deposition	Aluminum, thickness=20nm

5.3 Process flow of DMG Re-S/D SOI MOSFET

The process flow of dual metal gate recessed source/drain SOI MOSFET (Re-S/D SOI MOSFET) lists the necessary steps to fabricate and characterize the 45nm channel length Re-S/D SOI MOSFET. This structure have two metals in place of single gate metal, hence it is not a symmetrical device. Processing steps are somewhat differ with single metal gate Re-S/D SOI MOSFET. First four steps are common to the both structures.

- Initialization
- Oxide growth and etching
- Chanel formation
- Gate oxide growth
- Mirror imaging the structure
- Deposition of Metal 1 , Metal2 (Gate metal Deposition)
- Source and Drain implantation

- Metal deposition and etching (s/d contacts)
- Electrode specification

Initialization of the DMG Re-S/D SOI MOSFET commenced with defining the initial simulation grid, type of substrate and background doping. All the parameter values are almost same as the SMG structure. Channel is formed by adding boron impurity through Pearson implantation process. Boron ion implantation is carried out at less implantation energy of 2KeV with dosage of $3x10^{12}$ cm^{-3} in the channel region. Gate oxide is grown by performing dry oxidation at 850^0C for 3 minutes in dry O2 at 1 atmospheric pressure.

Mirror imaging the structure: The next step in the process is gate metal deposition. Because of two metals in the gate, mirror imaging of structure is performed first as shown in the Figure5.2 after that metal deposition will occur.

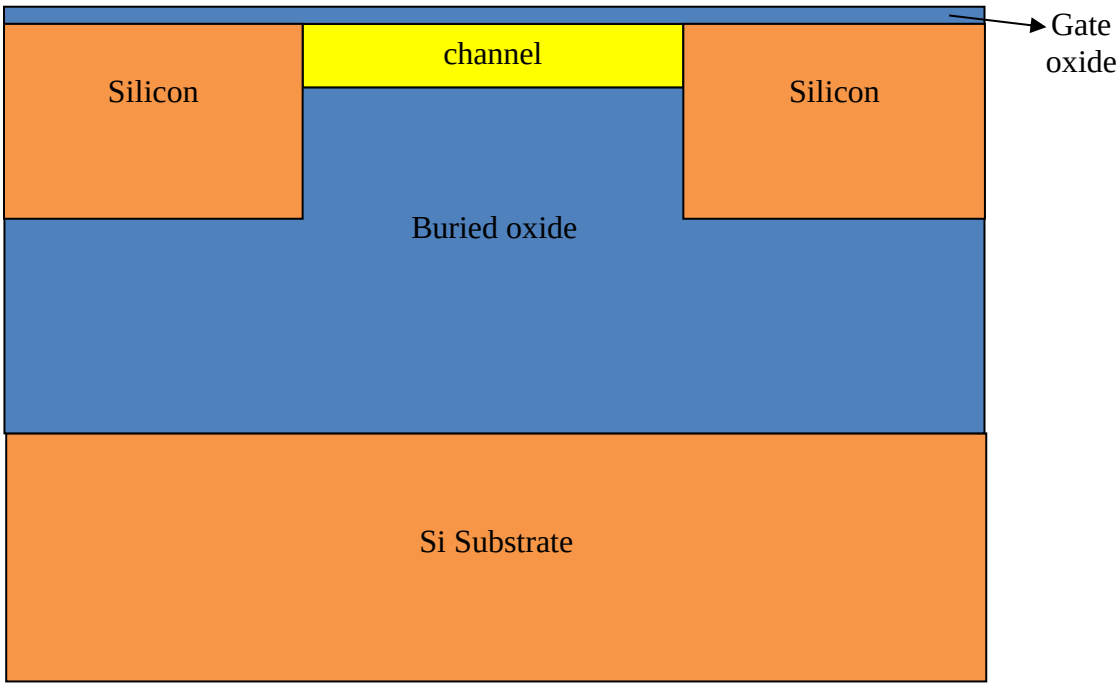

Figure 5.2 Mirror imaging of the structure

Deposition of Metal 1, Metal2 (Gate metal Deposition): The process of creating dual-metal-gate above the thin gate oxide layer as follows: Firstly, Deposition of metal1 is carried out using

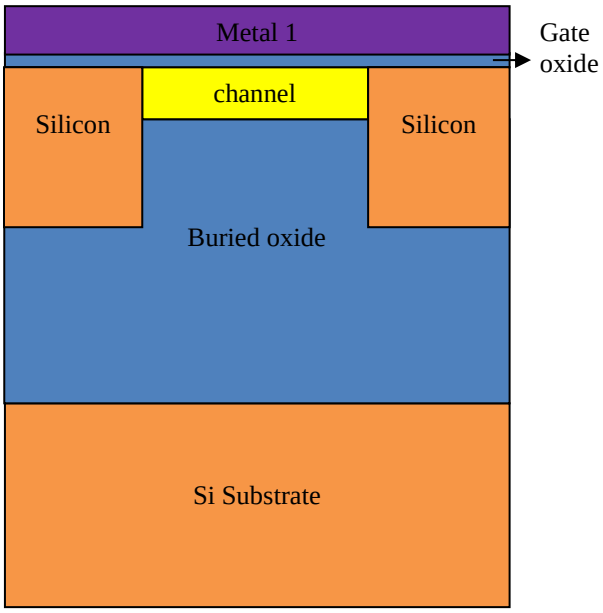

Figure 5.3.1 Deposition of metal1

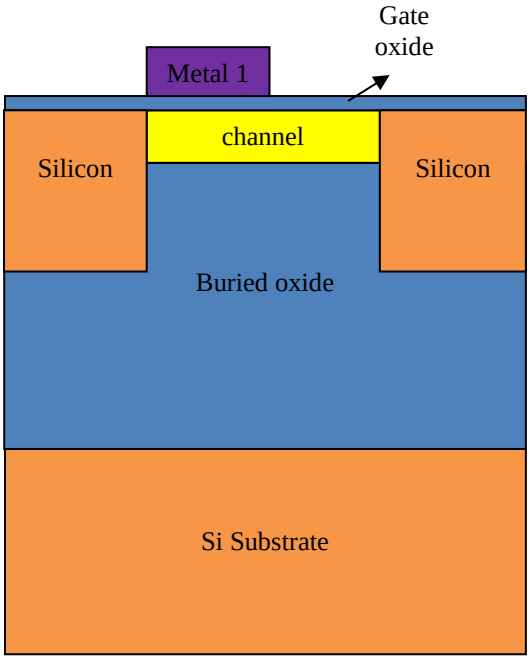

Figure 5.3.2 Etching of metal1

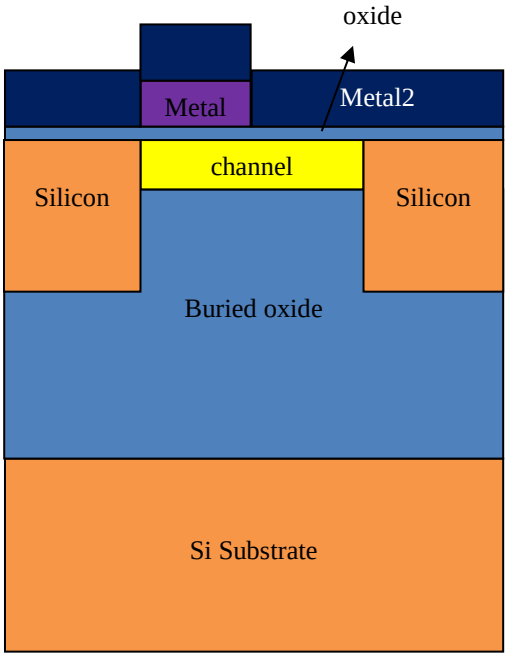

Figure 5.3.3 Deposition of metal2

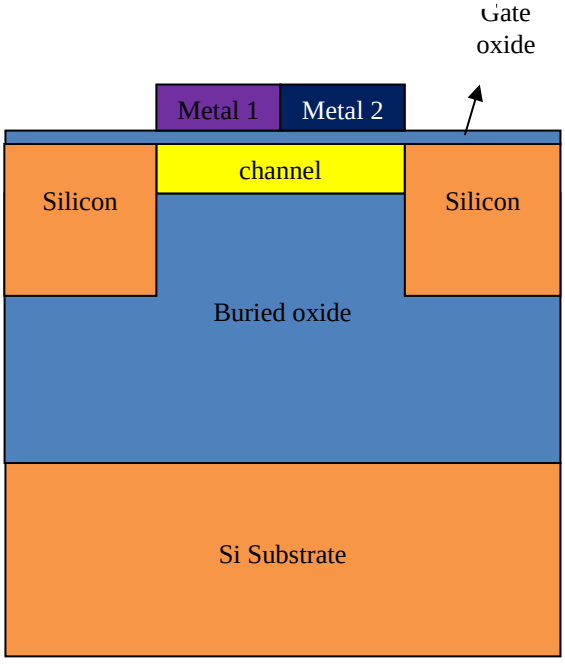

Figure 5.3.4 Etching of metal2

Figure 5.3 Deposition of metal1 and metal2

Conformal deposition technique as shown in Figure 5.3.1 and then metal1 is etched by using geometrical etching technique as shown in Figure 5.3.2 after that, Metal2 layer is deposited using conformal deposition technique as shown in Figure 5.3.3. Again, etching of Metal2 is carried out as shown in Figure 5.3.4

Source and Drain implantation: The next process is the development of source/drain (S/D) implantation. This implantation is followed by field oxidation done with wet oxidation process at 800^0C for 11 minutes. This oxide layer isolates the gate region from the source/drain implantation as shown in the Figure 5.4.1. Arsenic implantation is carried out with high dosage of $5x10^{14}$ cm^{-3} and the implant energy is 25keV to build the low resistance in the source and drain region as shown in Figure 5.4.2.

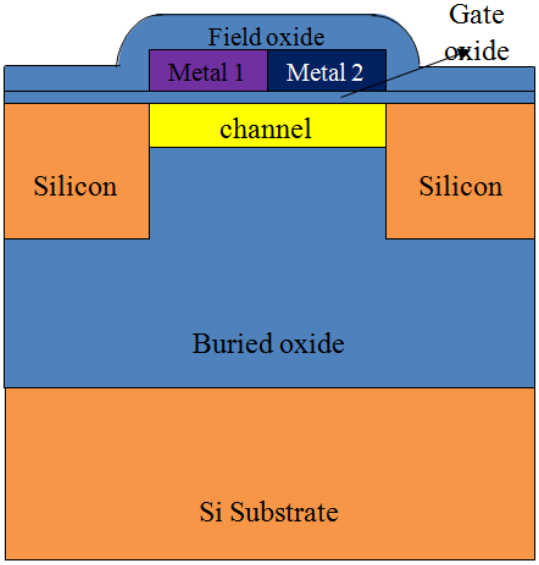

Figure 5.4.1 Field oxide growth

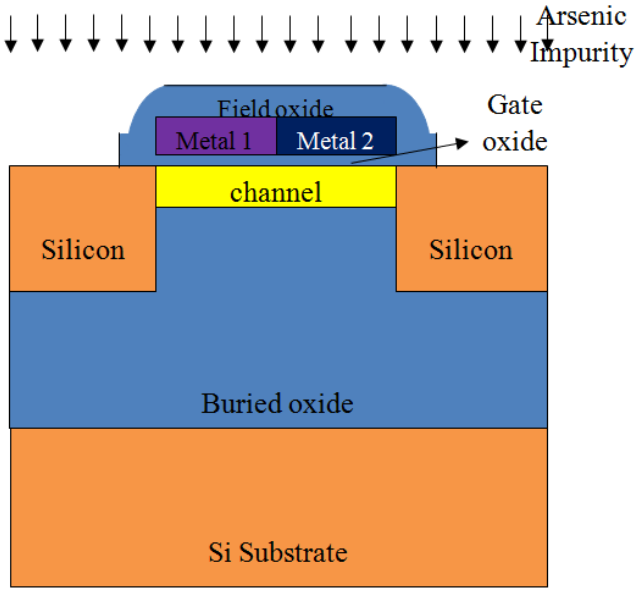

Figure 5.4.2 Adding arsenic impurity

Metal deposition (source/drain contacts) and electrode specification: For providing electrical ontacts to the source/drain, 20nm thick Aluminum (Al) is deposited as shown in Figure 5.7. The

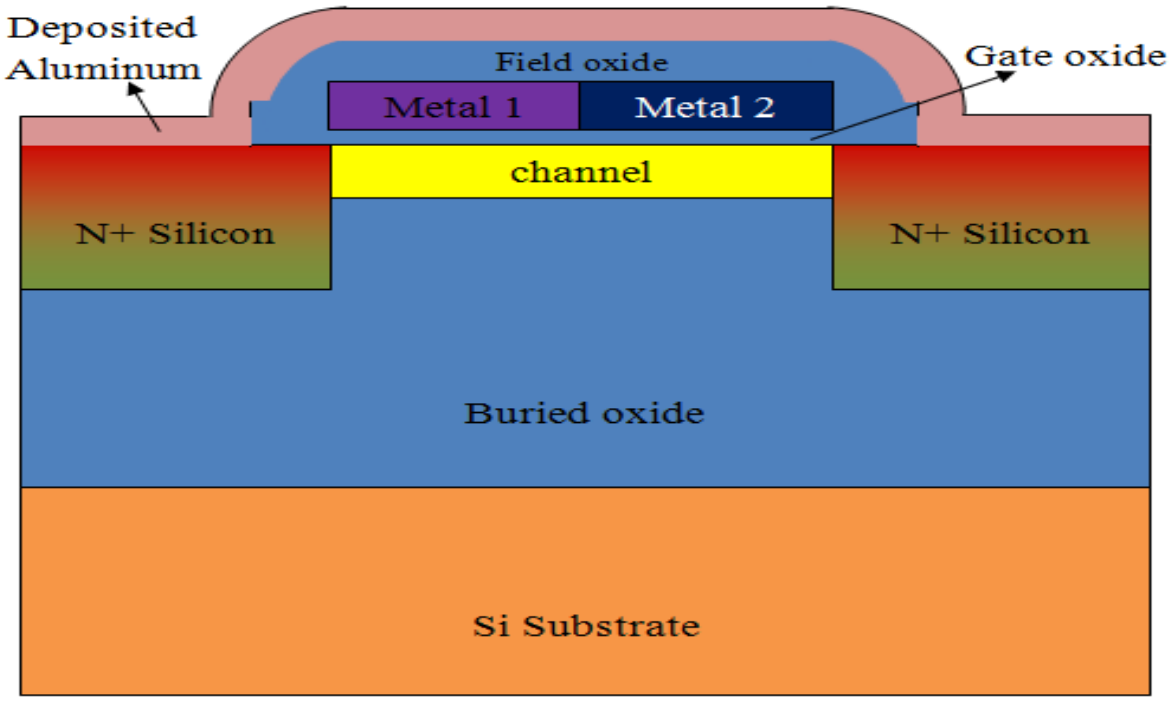

Figure 5.5 Deposition of aluminum metal

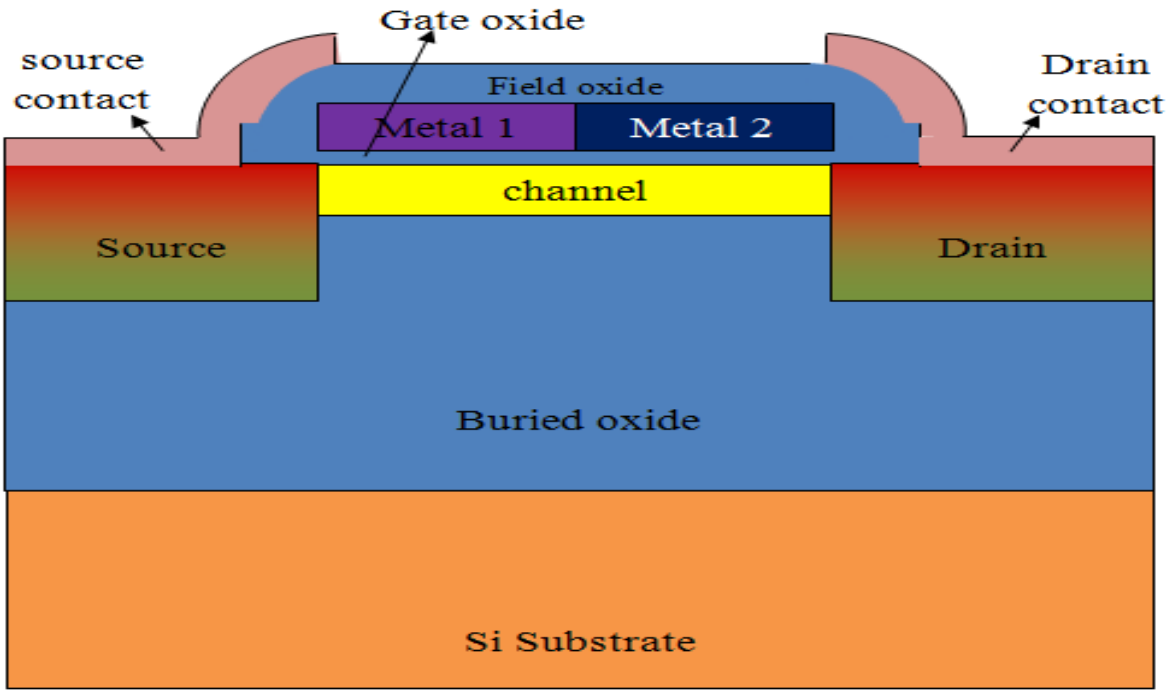

Figure 5.6 Final structure of the DMG Re-S/D SOI MOSFET

Contacts are shaped by etching part of the aluminum at the center of the device. By naming the four electrodes as source, gate, drain and substrate as shown in the Figure 5.8 completes the virtual fabrication of DMG Re-S/D SOI MOSFET.

5.4 Simulation results and discussion

Figure 5.10 shows the acceptor and donor doping profile along the cutline taken from source to drain region. The heavily doped n-type source/drain regions are formed by arsenic implantation with energy of 25 keV and a dosage of $5x10^{14}$ cm^{-3} .

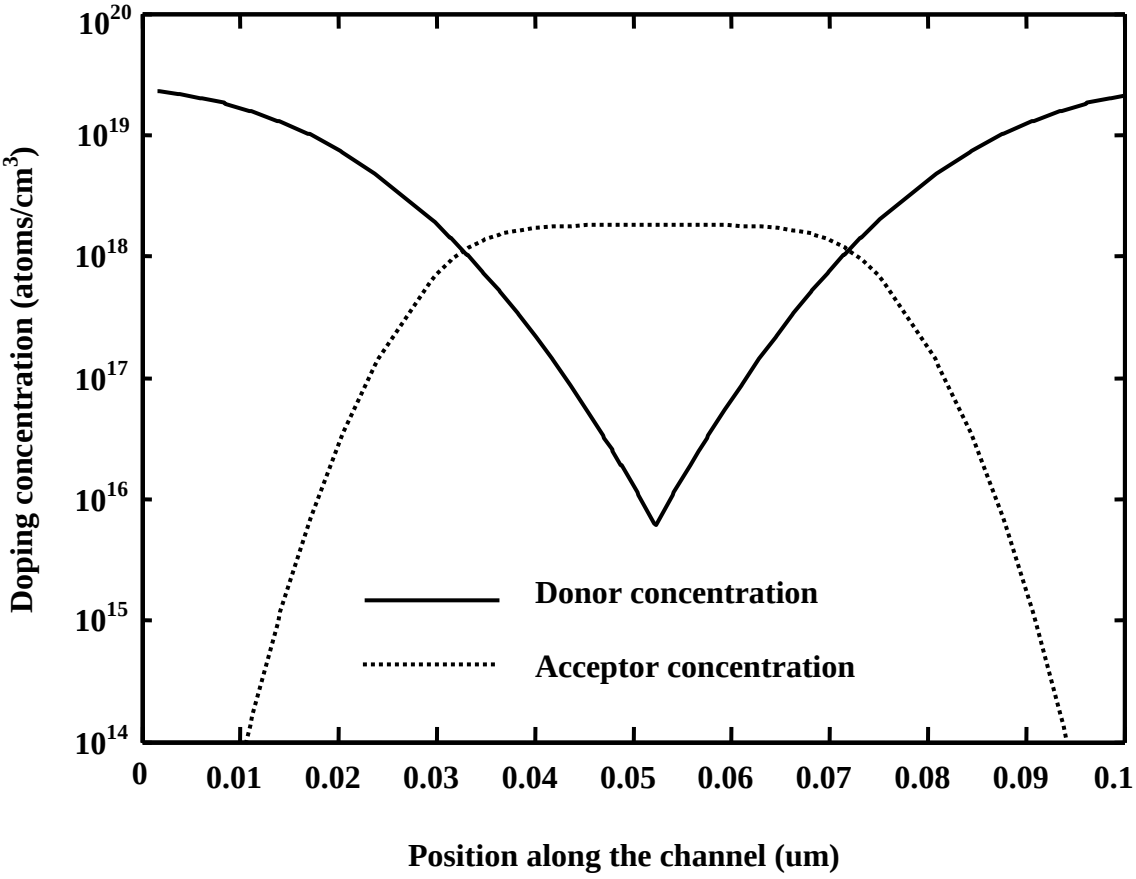

Figure 5.7 Acceptor and donor doping profile along the cutline taken from source to drain of DMG Re-S/D SOI MOSFET

where, t_{si}=8.2nm L=45nm t_{ox}=2.2nm t_{box}=200nm t_{rsd}=30nm

The channel region is doped with boron impurity, with an implant energy of 2 keV and a dosage of $3x10^{12}$ cm^{-3}. The ion beam used for both implantations is tilted by 7^0C and rotated by 30^0C. The peak concentration in the source/drain regions and channel regions are observed as $5x10^{19}$ cm^{-3}, 10^{18} cm^{-3} respectively.

Figure 4.11 shows the front surface potential along the channel. A comparison was drawn between the dual-metal-gate (DMG) Re-S/D SOI MOSFET with different control gate and screen gate lengths ratios, and single metal gate (SMG) Re-S/D SOI MOSFET structures. Work function of M1 is 4.8eV, M2 is 4.6eV and single metal gate work function is 4.8eV. Sudden change in the potential can be observed at the junction of M1 and M2 for the dual-metal-gate

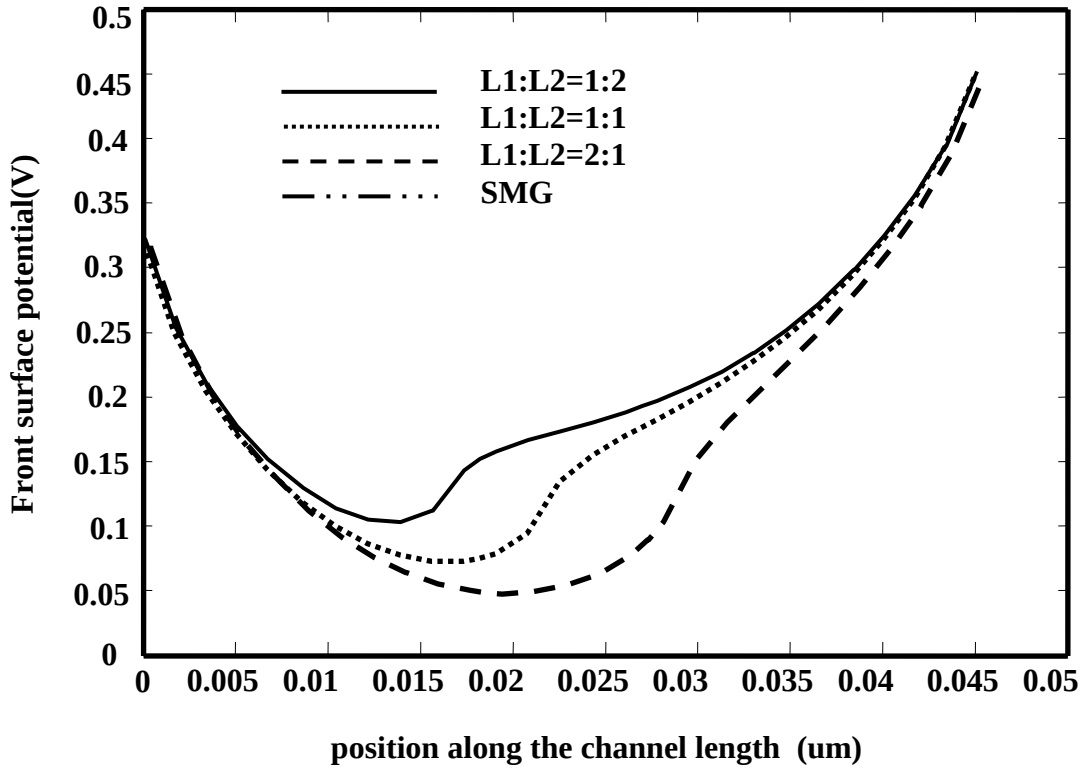

Figure 5.8 Front gate surface potential along the channel for different gate length ratios

Where, t_{si}=8.2nm L=45nm t_{ox}=2.2nm t_{box}=200nm t_{rsd}=30nm

structure because of different work functions. When screening gate length is greater than the control gate, the minimum surface potential of the device is high compared with others and barrier height of the device is less compared with others. While increasing control gate length, the minimum surface potential of the device is moving towards the drain side. From this figure it is also observed that minimum surface potential of the SMG structure is very less because of high work function. Hence, the threshold voltage of the DMG exhibits less value compared to SMG.

Figure 5.12 depicts the variation of threshold voltage of the different device structures along the channel length. Device structure with less control gate length compared with screening gate

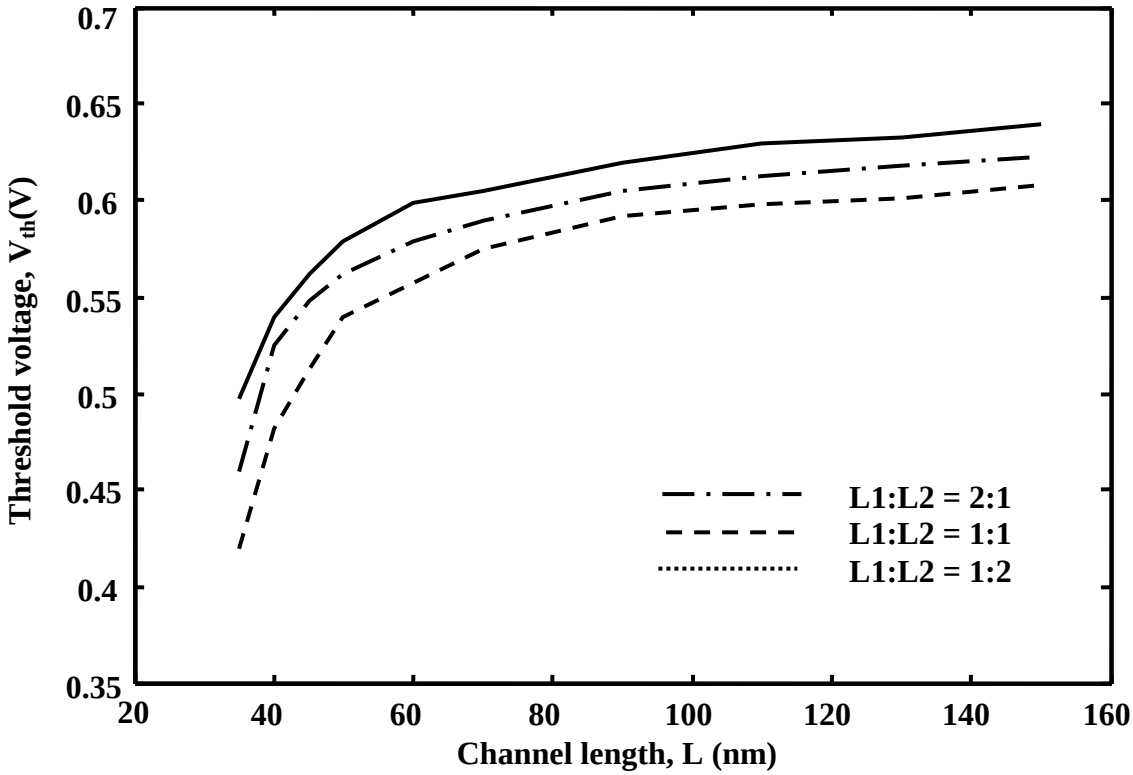

Figure 5.9 Threshold voltage along the channel length for different gate length ratios

Where, t_{si}=8.2nm t_{ox}=2.2nm t_{box}=200nm t_{rsd}=30nm

length exhibits less threshold. Threshold Voltage roll-off is decreasing with increasing control gate length. It is observed that, the device with ratio L1:L2=2:1 exhibits better immunity against short channel effects.

Figure 5.13 shows the variation of gate length ratio on subthreshold current over channel length. When gate lengths ratio is (L1:L2) 2:1, subthreshold current of the device is less compared with other structures. It is also observed that the subthreshold current of the all dual metal gate structures exhibits is higher than the single metal gate structure because of high work function of SMG.

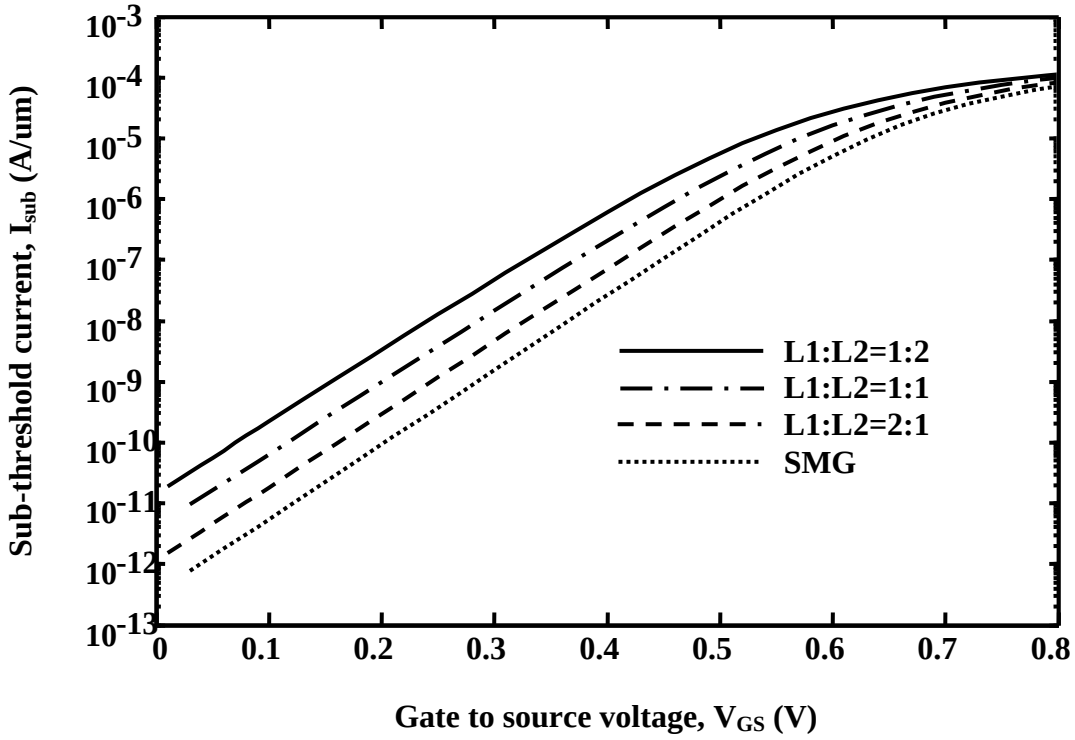

Figure 5.10 Subthreshold current versus Gate to source voltage

Where, t_{si}=8.2nm L=45nm t_{ox}=2.2nm t_{box}=200nm t_{rsd}=30nm

Figure 5.14 shows the drain current (I_{ds}) versus drain to source voltage (V_{DS}) for different gate length ratios of DMG Re-S/D SOI MOSFET, and SMG Re-S/D SOI MOSFET. It is noticed

that, the device with higher screening gate length offers high drain current and a SMG Re-S/D SOI MOSFET have less current. Hence, the current driving capability of the DMG is further improved.

Fig.15 depicts the influence of recessed source/drain thickness on the drain current of DMG Re-S/D SOI MOSFET by keeping L1:L2 ratio as 1:1. It also depicts the Ids-V_{DS} characteristics of Re-S/D SOI MOSFET where t_{rsd} varies from 0 to 30nm with step size of 10nm; when t_{rsd}=0nm, the device simply replicates DMG SOI MOSFET. Implantation energies of the device structures with 30nm, 20nm, 10nm and 0nm are 25KeV, 18KeV, 8KeV and 2Kev respectively. From this figure it is observed that the on-current driving capability of the device increases with recessed-S/D thickness (t_{rsd}).

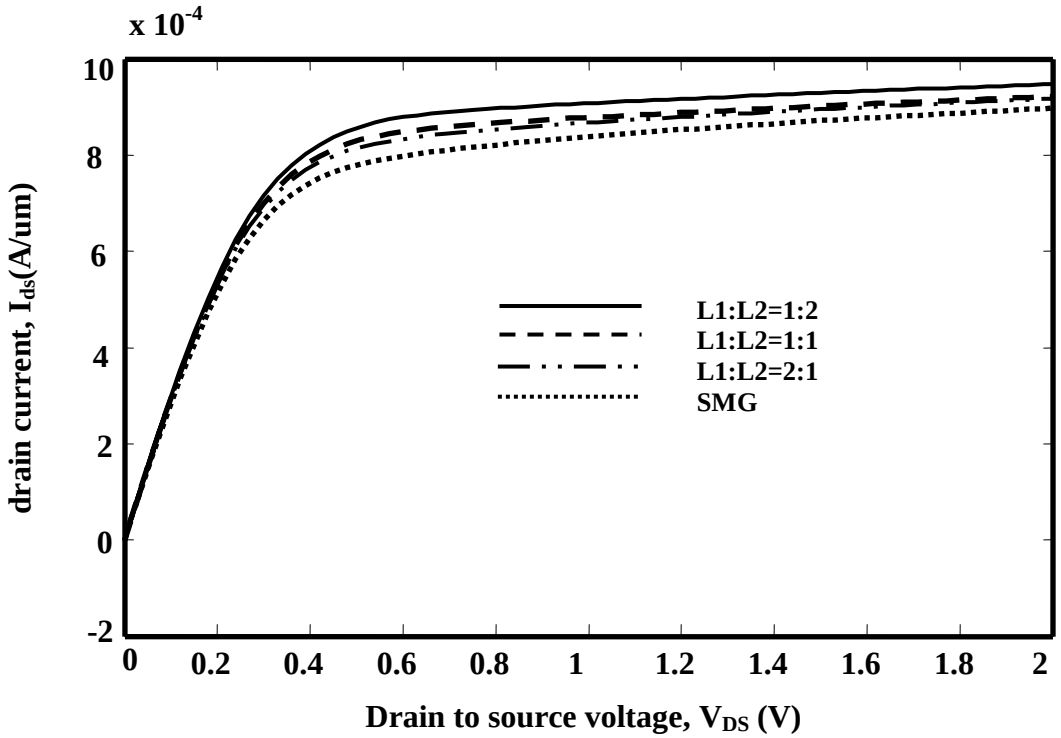

Figure 5.11 Drain current versus Drain to source voltage for different gate length ratios

Where, t_{si}=8.2nm L=45nm t_{ox}=2.2nm t_{box}=200nm t_{rsd}=30nm

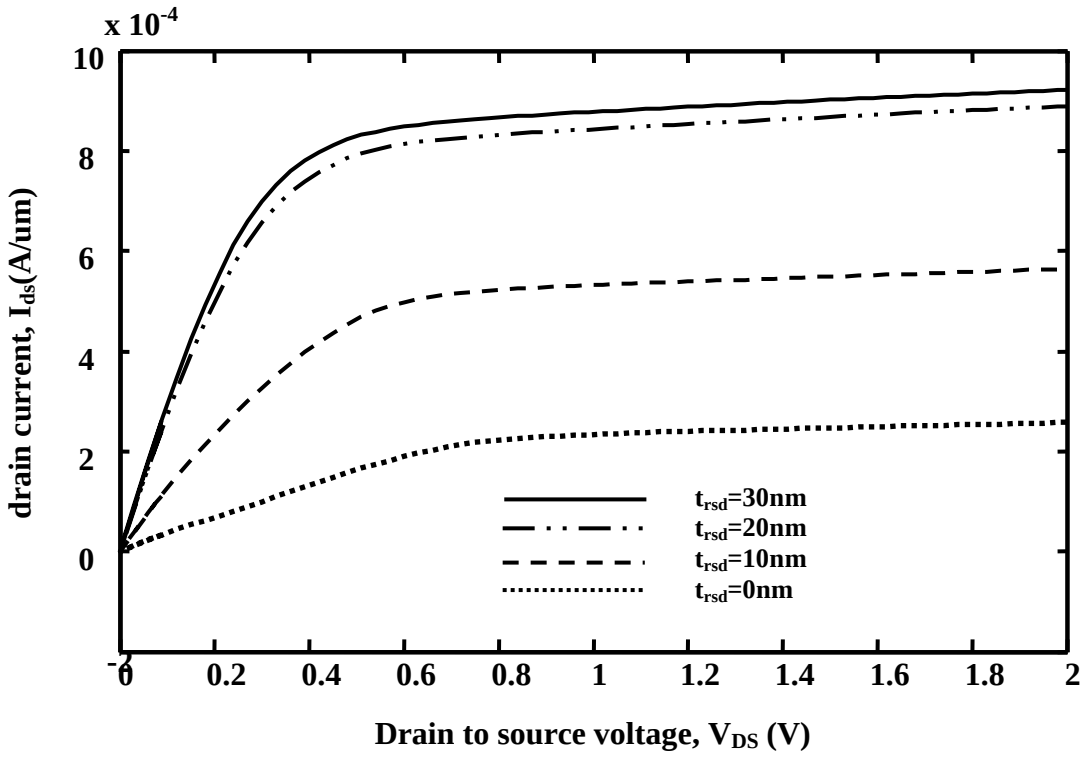

Figure 5.12 Drain current versus Drain to source voltage for different t_{rsd} values

Where, t_{si}=8.2nm L=45nm t_{ox}=2.2nm t_{box}=200nm t_{rsd}=30nm L1:L2=1:1

CHAPTER 6

6. CONCLUSION

6.1 Outcome of the Work

In this Thesis, the virtual fabrication of a recessed-S/D SOI MOSFET with channel length of 30nm and virtual fabrication of dual-metal-gate Re-S/D SOI MOSFET with channel length of 45nm has been done. Several processing steps such as oxidation, deposition, etching, ion implantation and lithography have been utilized in the process of device fabrication. Different process parameters such as gate oxide thickness (t_{ox}), channel thickness have been extracted by process parameter extraction which are 3.2nm and 9nm respectively for SMG structure and 2.2nm and 8nm respectively for DMG structure. The thickness of the Re-S/D (t_{rsd}) is controlled by SOI layer thickness. The electrical characteristics such as drain current (I_{ds}) versus drain to source voltage (V_{DS}) has been explored for different values of gate to source voltage (V_{GS}). Also variation of drain current (I_{ds}) with the drain to source (V_{DS}) voltage for different values of recessed S/D thickness (t_{rsd}) have been evaluated. The drain current (I_{ds}) of the device increased with increasing source/drain penetration in buried oxide(BOX). The threshold voltage and subthreshold current of the DMG Re-S/D MOSFET decreased with increasing control gate length. It is inferred that the current driving capability of the device further improved by incorporating the concept of dual-metal-gate structure.

6.2 Scope for the future work: The present study can be used as reference for virtual fabrication of three-dimensional MOSFET device structures and heterojunction MOSFET devices.

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