SOME STUDIES ON SI-NANOTUBE BASED FETS

A dissertation submitted in partial fulfilment of the requirements for the degree of

MASTER OF TECHNOLOGY
IN
VLSI AND EMBEDDED SYSTEM

by

MUKESH KUMAR
ROLL NO: 213EC2200

to the

Department of Electronics and Communication Engineering
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Under the Supervision of
Prof.(Dr.) P.K.TIWARI

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CERTIFICATE

This is to certify that the thesis report entitled "**Some Studies On Si-nanotube Based FETs**" submitted by **Mukesh Kumar**, bearing **roll no. 213EC2200** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded System**" during session 2013-2015 at National Institute of Technology, Rourkela is an authentic work carried out by his under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela
Date: 20th May, 2015

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Dedicated to my Brother (Kamlesh Kumar)

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MUKESH KUMAR

ABSTRACT

Silicon-nano-tube (SiNT) MOSFETs have been analyzed recently in order to investigate their suitability for future ultra-large scale integration (ULSI) applications. Based on the study so for, it could be safely stated that the SiNT MOSFETs are very promising for future ULSI as they could be scaled down to 22nm gate length and below effectively. The SiNT MOSFET provides ultimate electrostatic controllability to the gates in order to counter the short-channel effects because of its hollow cylindrical shape. In SiNT MOSFETs, two gates, an outer gate and an inner gate, can act independently or together in order to realize the multi-threshold voltage transistors characteristics or high drain current, respectively. The SiNT MOSFET is particularly considered to be unique in the sense that, unlike other MG MOS structures, it provides excellent SCE immunity even when the diameter of the tube is increased as long as the channel thickness is kept same. Subthreshold electrical characteristics of SiNT FET have been studied through device simulation and it has been confirmed that the device outperforms GAA and other MG devices completely. However, in the best of our knowledge, neither analog nor RF performance of the device has been studied till date in order to access its potential in system-on-chip applications. Therefore, we have analyzed the analog as well as the RF characteristics of SiNT FETs using the ATLAS, a 3D device simulator from SILVACO. Besides, the characteristics of SiNT MOSFETs have also been compared with the same of a nanowire based GAA FET to quantify the improvement in the performance.

In this work, Si-nanotube MOSFETs (SiNT FET) with catalytic metal gates are proposed for gas sensing applications. P-channel SiNT FET with palladium (Pd) metal gate is proposed for hydrogen sensing , whereas N-channel SiNT FET with silver (Ag) metal gate can be used for oxygen gas sensing. A simulation based study has been carried out using ATLAS-3D numerical simulator, and it is found that SiNT FETs have more efficiency towards the

hydrogen and oxygen detection than the recently proposed cylindrical gate-all-around (GAA) MOSFETs. Further, effect of variation of the channel length (Lg) and channel thickness (t_{Si}) on the gas sensing sensitivity of the sensors are also studied.

In the presented work, an analysis into the performance of a Dual Material Gate Single Dielectric Si-nanotube Tunnel FET has been done. Numerous simulations were done to determine the influence of work functions of both the gate materials on the electrical characteristics of the device. Comparative study was done between Dual Material Gate device and Single Material Gate device. Parameters like intrinsic capacitances as well as transconducatnce were also determined.

The same analytic approach was extended to Dual Material Gate Hetero Dielectric Si-nanotube Tunnel FET to analyze the improved performance of the device compared to its Single Dielectric Dua Material Gate counterpart .Thus the work presented had all together analyzed attributes of ncorporating Dual Material Gate as well as Hetero Dielectric in Si-nanotube Tunnel FET structures. Extensive simulations for the presented work were performed by using two dimensional device simulator (ATLASTM SILVACO Int.)

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LIST OF ACRONYMS

BOX: Buried Oxide

CMOS: Complementary Metal Oxide Semiconductor

DIBL: Drain Induced Barrier Lowering

HCE: Hot Carrier Effect

ITRS: International Technology Roadmap for Semiconductor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

NWFET: Nano Wire Field Effect Transistor

SCE: Short Channel Effect

SOI: Silicon-on-Insulator

TCAD: Technology Computer-Aided-Design

SD-DMG: Single Dielectric Dual Material Gate

SD-SMG: Single Dielectric Single Material Gate

HD-DMG: Hetero Dielectric Dual Material Gate

HD-SMG: Hetero Dielectric Single Material Gate

TFET: Tunnel Field Effect Transistor

VLSI: Very Large Scale Integration

GAA: Gate-all-around

SiNT FET: Si-nanotube MOSFET

Chapter 1

Introduction

1.1Brief introduction to history of semiconductor device technology

Time has shown that human has achieved more elite life by the use of modern technology. Technology that helps us to understand the need of basic nature and take us even into deep space for exploration and research. Smartphones, pc, laptops etc. has make our life lot easier. And all of these technology are based on semiconductor devices. All these life supporting gadgets are getting smaller and smaller day by day and there power consumption level is also decreasing making them very power efficient.

It's all started in 1925 when great scientist Julius Edgar Lilienfeld (1881-1963) has proposed an element which has a resemblance like todays MOS Transistor for which he has applied for patent in 1930. But the actual device made in 1960 by Kahng and Atilla which they call MOSFET (metal oxide semiconductor field effect transistor)[1-6]. In 1958 first time the idea of integrated circuit(IC) is presented by Jack Kelby at Taxes Instruments and Robert Noyce from the Fairchild Corp. fabricated the first IC (S-R flip flop) as shown in Fig. 1.11. Then came Gordon Moore who is also a co-founder of Intel corp. said that the number of transistors doubles approximately every 18 months which is shown in Fig. 1.1.2. Moore's extrapolation has been correct for three decades. In year 1962 world saw the generation of first logic family and its name as TTL. Then it was it was Intel that introduce first transistor in year 1972 which is made up of two thousand p-MOS transistors[4-6]. Slowly the number of transistor grows exponentially following Moore's law and soon n-MOS has been used to make processors. But they are ruled out due to higher dynamic power dissipation. Then came the CMOS technology which brings tremendous changes in processor manufacturing as well as other semiconductor

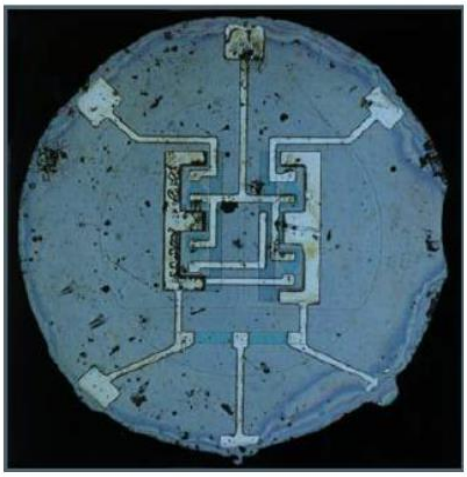


Figure 1.1.1: First IC fabricated by Jay Last's development group at Fairchild Corp. [4]

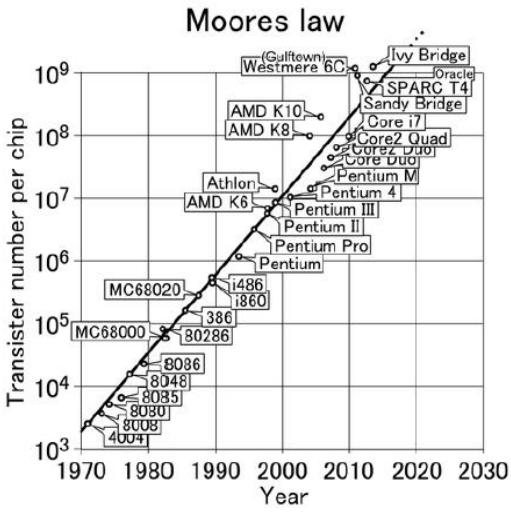


Figure 1.1.2: Transistor Integration on Chip displaying Moore's Law. [5]

Technology. It's possible only because of low power consumption of CMOS and its higher efficiency. With the introduction of CMOS it became easier to fabricate more numbers of chip in a given area so the production of device moves from small scale integration (SSI) to very large scale integration (VLSI). Now the realm of technology is entering the Nano technology.

With CMOS technology it become possible to reduce the device power consumption and it is possible because of the very powerful theory of scaling. With scaling it became possible to

reduce size of device dimensions by reducing basic parts of transistor like channel length, channel thickness etc. scaling also make it possible to reduce the size of voltage supply.

A semiconductor working group which has prepared the road map for the scaling of device and reduction of power consumption called International Technology Roadmap for Semiconductor (ITRS) has prepared a road map which tell us that in year 2013 we will reach to 22 nm technology node where device channel length will be less than 10nm[1-6].

1.2Conventional MOSFET and its shortcoming's

Device with four terminals namely source (S), drain (D), gate (G) and body (B) or substrate as shown in figure 1.2.1 is conventional MOSFET. Using these four terminals MOSFET can be used as electronic switch or it can be used signal amplifier. MOSFET is the basic building block in any integrated circuit. Body terminal is most of the time is tied

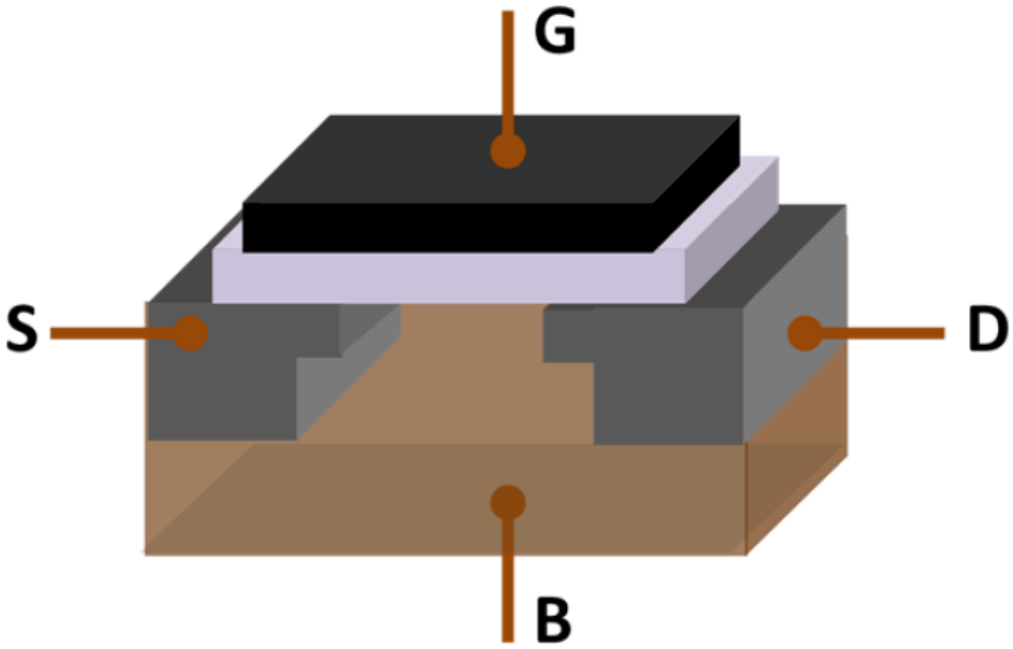


Figure 1.2.1 Cross-sectional view of conventional bulk MOSFET.

with source terminal therefore in representation it appear like three terminal device. Gate terminal is used in electrostatic control of channel[6]. When the gate voltage is applied it will create an inversion layer which provides path to electron flow between source and channel.

There is an oxide layer also present between gate and channel which is called gate oxide. Gate oxide is used to prevent any flow of electron through gate which can generate gate current. Now when gate voltage is applied there will be charge accumulation below gate and after appropriate gate voltage called threshold voltage inversion layer will be strong enough to create path between source and drain through which current will start to flow[6-8].

1.3 Shortcomings of Conventional MOSFET due to scaling

To keep track with Moore's law transistor density inside an integrated circuit must be very high. Therefore size of the MOOSFET must be decrease in order to utilize chip area and power efficiently. So to move from SSI to VLSI the scientists starts decreasing size of the conventional MOSFETs. To decrease the size of MOSFET its channel length must be decreased accordingly but when we start decreasing size we encounters number of short channel effects which results in high power dissipation and demerits of switching properties. Reduced channel length results in higher leakage current which is undesirable also in conventional MOSFET we cannot achieve subthreshold slope (SS) below 60 meV/Dec[22-24]. Reason of this subthreshold slope effect is explained in detail later in this thesis.

1.3.1 Short channel effects

These effects arise channel length of the conventional MOSFET is reduced beyond a certain limit. When the distance between source and drain decreases the control of gate over channel decreases and the resulting effects are called short channel effects.

1.3.1.1 Drain Induced Barrier Lowering (DIBL) and pinch-through

In a long channel device the source and drain are separated by a long distance and therefore only gate has electrostatic control over channel and channel remains independent of drain voltage. When the channel is scale down then channel does not only controlled by gate voltage but also by drain voltages and this is called as drain induced barrier lowering (DIBL). This effect is similar to the pinch-through process. When we apply drain voltages there is a reverse biasing form between drain and the body as in case of n-channel MOSFET. This reverse biasing results in the formation of depletion region between drain and body. If we keep on increasing drain voltage then this depletion region keeps on increasing and it starts penetrating inside the depletion region of source-channel. The penetration of the depletion region of drain into source, this point is called as pinch-through and this will reduced the potential barrier. Similarly in case of DIBL when we apply drain voltage and increase it the potential barrier between source and drain decreases results in increase of drain current. Therefore the threshold voltage of conventional MOSFET not only controlled by gate voltage but also drain voltages[22]. Therefore increase in drain voltage results decrease in threshold voltage of planner MOSFET this is called DIBL.

1.3.1.2 Velocity saturation

With the scaling of the device we required to reduce the channel length which is distance between the drain and source. In case of long channel device the gate has all electrostatic control over channel therefore with increase in the gate voltage the drain current also increases linearly which follows ohms law. We also knows that the movement of electron

is strongly controlled by electric field. Now in case of reduced channel the electric field in the cannel become very strong and under the influence of this strong electric field the velocity of electron become constant and there is no further increase in the velocity is possible for electron. In other words the velocity of electron has reached its saturation value this is called velocity saturation[24]. When electron reach there velocity saturation gate electric field has no control over electrons and even if we increase the gate voltage there is very little change in the drain voltage or there is no change at all. This will affect the transfer characteristics of conventional MOSFET and it will fail to fallow the ohm's law.

1.3.1.3 Surface scattering

Scaling of conventional planer MOSFET leads to the reduction of channel now due to reduced channel the depletion region from source side increases and it extended into the channel. This extension of depletion region in channel leads to control of longitudinal electric field over electrons. The electron mobility depends upon the two electric field components. Due to vertical field component the electrons get accumulated and therefore the mobility of electron decreases[22-27].

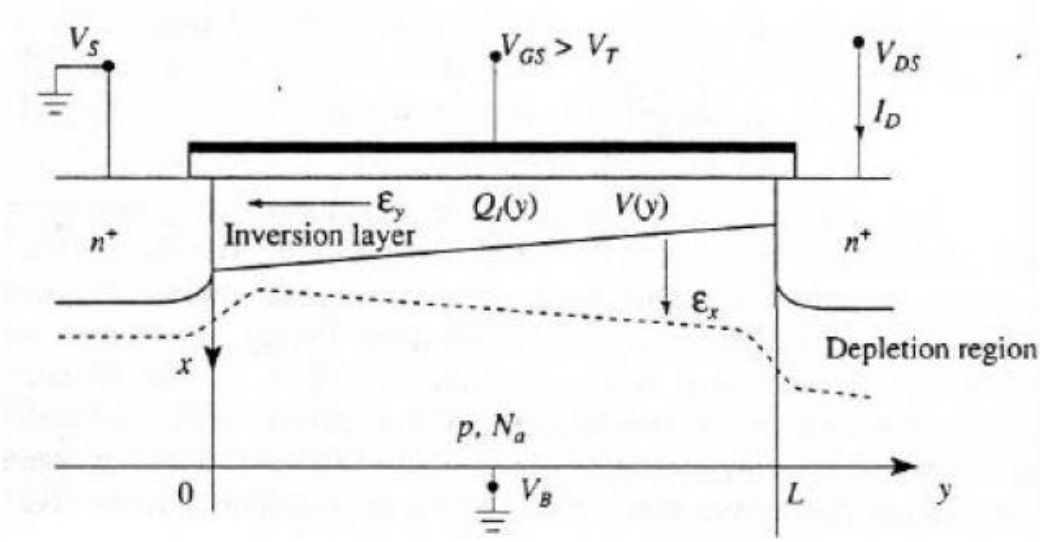


Figure 1.3.1.3.1 Correctional view of conventional MOSFET for surface scattering.

Those electrons which are present parallel to the interface suffers the most reduction in mobility. Now the mobility of electron become electric field dependent therefore in electron in the inversion layer suffers surface scattering. Due to surface scattering the average movement of electron reduces and flow of current also reduces.

1.3.1.4 Impact ionizations

In reduced channel device there is very high electric field present in the small channel and we know that the longitudinal electric field may increase the velocity of the electron very high. And this high speed electron has enough energy that it can strikes the electron present in the silicon atom resulting in the impact ionization. Since the electron moves towards the drain at very high speed it is possible that at the source side there will be huge accumulation of holes takes place. This presence of hole at source side may create some voltage strong enough that electron may starts flowing through substrate[22-27]. Now electron under strong electric field travel at very high velocity and strikes the silicon atom creating electron-hole pairs. This process of generation of electron-hole pair is called impact ionization.

1.3.1.5 Hot carrier injection

Reducing channel length to achieve smaller device dimensions will stats short channel effects and one of these effects are the hot carrier injection effect. Small channel will result in very strong electric field inside the channel. Under the influence of this strong electric field there might be chance that electron may acquires high enough energy and increases its velocity so that electron leaves channel and penetrate into oxide layer. This phenomenon is called oxide tunnelling which is highly undesirable. And the electron that penetrate due to high electric field is hot electron. Now due to these oxide trap electrons

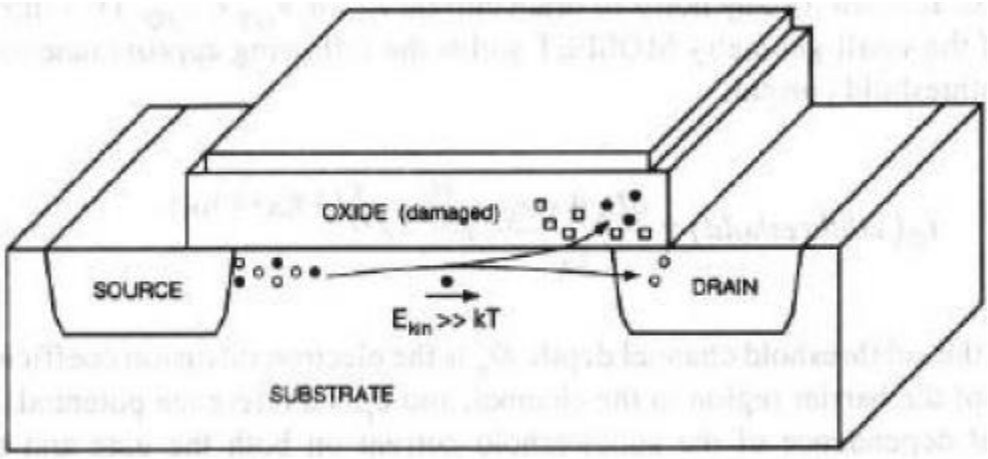


Figure 1.3.1.5.1 MOSFET showing hot carrier injection

threshold voltages changes. It decreases for P-MOS and increases for N-MOS. This strong electric field can be easily achieved by device as the channel length is very small. For example we know that E=V/d, where V is the potential applied and d is the distance in this case its channel length. So if we apply 0.5 v to a device having 10nm channel length we get $E = 5 \times 10^9$ which is very high and very strong electric field. This hot carrier injection problem creates long term reliability problem.We have discussed all the major short channel effects which give us idea that we cannot reduce channel length below certain limit in case of planner conventional MOSFET[22]. Therefore to achieve channel length in nm era there is huge research on non-conventional MOSFET structures. These non-conventional structure has better short channel effects diminutions which will be discuss in next section.

1.5 Evolution of non-conventional MOSFETs

Figure 1.4.1 shows development pf non-conventional MOSFETs from conventional one. In conventional MOSFET gate control the channel from the top only[6]. Gate only gain electrostatic control over surface of channel. Is does not control the deep part of channel

therefore minority carrier flows easily in the depth of channel which contributes to leakage current.

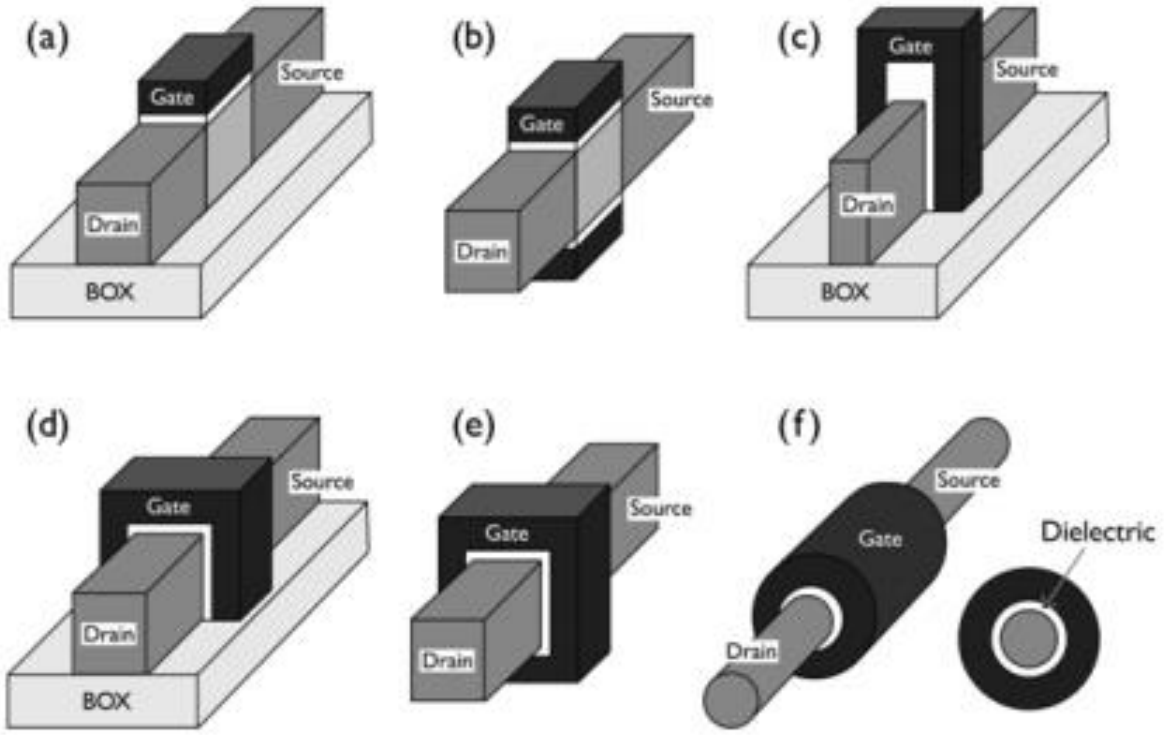


Figure 1.4.1 Cross sectional view of (a) SOI MOSFET, (b) DG MOSFET, (c) FinFET, (d) Tri-Gate MOSGET, (e) Quad-Gate MOSFET and (f) Gate-all-around MOSFET.

Now because of this less control of gate over channel short channel effects occurs. Now we know that if gate has better control over channel the performance of the device is going to be excellent. Thus non-conventional device came into existence which are used using non-planner technology. The first device that came is the silicon-on-insulator (SOI) MOSFET, this device contains an oxide layer above body and below source-channel-drain as shown in figure 1.4.1 (a) this concept helps prevent the DIBL in MOSFET. But in this device gate still only controls from the top and minority carriers are free to flow

in faraway region from surface of channel. Therefore next device came with two gate and called as dual gate (DG) MOSFET as shown in figure 1.4.2 (b). This device has a better control over channel and therefore less leakage current flow in channel. Since DG MOSFET has better control over channel and as a result less leakage current which leads to low power device. After DG MOSFET as shown in figure 1.4.2 (c) one revolutionary idea came that why not take the channel outside the body and place it over the oxide layer along with source and drain, this device is called as FinFET. In FinFET two gates are present on the two sides of channel as shown in figure 1.4.2 (c) and the third gate is present above the channel but the oxide thickness is too high and third gate does not play any role in controlling channel. Now FinFET provides even excellent results and Intel fabricated IC using FinFETs at 22nm technology. Since we are controlling channel using two gate then why not controlling it from three possible sides as shown in figure 1.4.2 (d), called TriGate MOSFET. This is similar to the FinFET but in this case the top gate also controls the channel. Next came the Quad-Gate MOSFET and this MOSFET has four gates as shown in the figure 1.4.2 (e) four gates provides even better electrostatic control of gate and the leakage current reduced to very low level. Trigate and Quad-gate MOSFET has only one problem called corner electric field problem which leads to more parasitic capacitance. And this problem arises due to their rectangular geometry. Therefore to remove corner electric field problem an ground-breaking idea came that changes the world of MOSFET and that is, why not change the geometrical shape of MOSFET from rectangular shape to cylindrical[8-12]. Then came gate-all-around MOSFET or Cylindrical MOSFET or Si-Nanowire MOSFET as shown in figure 1.4.2 (f), in this device the channel is given cylindrical shape along with source and drain, the gate is wrapped around the channel giving it outstanding control over channel and free of corner electric field.

1.5 Thesis organization

Chapter 2: This chapter is a literature review. In this chapter a brief discussion about the past work done by the researcher has been discussed.

Chapter 3: This chapter will compare most of the properties of the Si-nanotube MOSFET (SiNT FET) with Gate-all around (GAA) MOSFET. Also RF characteristics of both device has been compared and it is shown that SiNT FET is better than GAA MOSFET.

Chapter 4: This chapter will use SiNT FET for the gas sensing and compare to the GAA MOSFET for the same application and then the obtained results will be compared to get which device is better in gas sensing applications.

Chapter 5: This chapter will examine the SiNT FET with dual metal gate having single dielectric with tunnelling characteristics.

Chapter 6: This chapter will examine the SiNT FET with dual metal gate having dual dielectric with tunnelling characteristics.

Chapter 7: this chapter will present overall conclusion of thesis work.

Chapter 2

Literature Review

2 INTRODUCTION

In this chapter literature review of important topics and devices has been presented based on the reference papers that has been used as a guidance work.

2.1 Gate-all-around MOSFET (GAA)

GAA MOSFET is a non-conventional MOSFET which has very great interest for researchers. Since this device could be the device of nanotechnology era and GAA has a cylindrical structure therefore this also called as cylindrical MOSFET. The device structure is shown in the figure 2.1.1 and as it is clear from the structure that channel is wrapped around by a gate. Since the channel is wrapped around by gate, gate has very good electrostatic control over channel. And compared to the conventional MOSFET it has less leakage current.

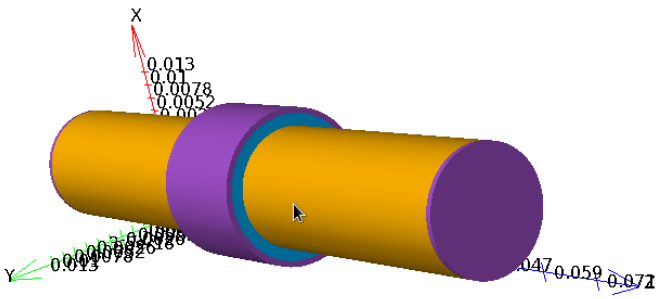


Figure 2.1.1 Simulated structure of GAA

Due to the superior control of gate over channel GAA MOSFET has reduced short channel effects, reduced leakage current and steeper subthreshold slope. It's also a very promising

device for channel length below 10nm. This make GAA a very hopeful device for low power circuits. But the main drawback of this device is that its drain current is very low few micro amperes only there for to generate noticeable amount of drain current we required some kind of array stacking which can generate enough amount of drain current which can derive circuits[9-12].

To avoid drain current problem the Si-nanotube based structure has been considered which give even more promising results.

2.2 Si-nanotube architecture (SiNT FET)

Demand of this world for the low power device leads to the construction of GAA MOSFET which seems very powerful device for the future when channel length is going to be below 10nm. But the problem with the GAA MOSFET is its low drive current therefore to avoid that problem one new device structure came into lime light as shown in figure 2.2.1. This structure is called as Si-nanotube architecture and the device is called as Si-nanotube MOSFET (Si-NT FET).

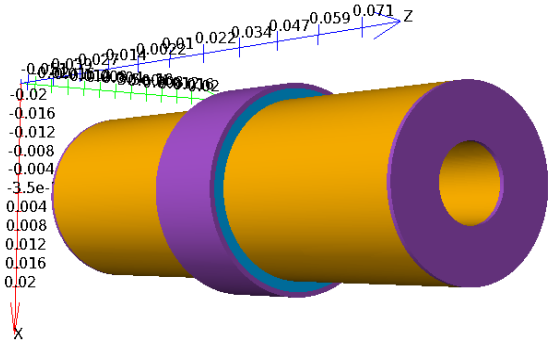


Figure 2.2.1 Simulated structure of SiNT FET

The only structural difference between SiNT FET and GAA is that SiNT FET has one extra gate called the core gate which is present inside the channel. Therefore the channel is placed in between two gates. One present above the channel called outer gate and other present inside the channel called core gate. Since two gates are controlling channel the electrostatically control over channel is more than excellent. Due to two gates and excellent control of channel there is very less leakage current flows in SiNT FET. Because of two gated structure there is formation of volume inversion instead of surface inversion which leads to the reduction of surface scattering. And reduction in surface scattering increases the drive current. It also shows the steeper subthreshold slope and reduction in the short channel effects[9-12]. Therefore the SiNT FET has a better characteristics than GAA MOSFET.

2.3 MOSFET as a gas sensor

With current worlds scenario the study of environment, automobile, industries, and medical facilities required a very efficient gas sensors. Recently MOSFET based gas sensors are of very high demands because of the benefits provided by MOSFETs. MOSFET based gas sensor not only provide small size but also high efficiency towards gas sensing and low cost. The basic principle on which MOSFETs based gas sensor works is that "In the presence of gas its molecules react with the surface of metal and this reaction changes the work function of that metal such metals are called catalytic meta". This shift in work function changes the surface potential which leads to the change in threshold voltage and drain current. Therefore to measure the presence of the gas and it's concentration we can measure any of the parameter i.e. surface potential, threshold voltage or drain current. Detection of the drain current is easier than the threshold voltage detection as it required additional circuits for threshold detection. In previous work it was found that n-channel MOSFET with silver catalytic gate can be used for oxygen sensing and p-channel MOSFET with palladium catalytic gate can be used for

hydrogen sensing[18-21]. Researchers has found that GAA MOSFET has a far better gas sensing efficiency than the conventional MOSFETs.

2.4 Tunnel FET

The demand of small size , low power consuming ,less leakage and low cost semiconductor devices has been increased to follow the ITRS bellow 22nm technology node. To reach technology nodes bellow 22nm, fallow moors law and ITRS scientist has been looking for non-conventional MOSFETS like dual gate MOSFET, trigate MOSFET, FIN FET, Gate-All-Around MOSFETs etc. because conventional MOSFET cannot reach such small size due to increase in leakage current. The current scenario required ultra-low-power devices and this employ reduction in the voltage supply $V_{dd.}$ Till now according to ITRS we has reduces Vdd by using theory of scaling to 0.9 and the projected target is 0.8 by 2015. But further reduction of Vdd is not possible by using scaling theory due to fundamental limit possess by current conduction in conventional MOSFET which thermionic by nature. Therefore subthreshold slope (SS) creates huddles for the further scaling of Vdd. This scaling limit on Vdd is due to kT/q factor value due to which the subthreshold slope cannot go below 60mV/dec.

To answer the challenge presented by subthreshold slope (SS), tunnelling devices like tunnel field effect transistors represents better and promising solution to construct low power devices. Because it is possible to achieve SS below 60 mV/dec[22-28]. the transport of charge carrier in tunnelling device fallow quantum mechanical band-to-band-tunnelling BTBT instead of thermionic mechanism.

2.4.1 Operations of tunnel FET and BTBT

Figure 2.4.1.1 shows the basic structure of tunnel FET, its actually a p-i-n diode which is when operated under reversed biased condition the phenomenon of tunnelling occurs and the drain current due to reverse biasing is called as tunnel current.

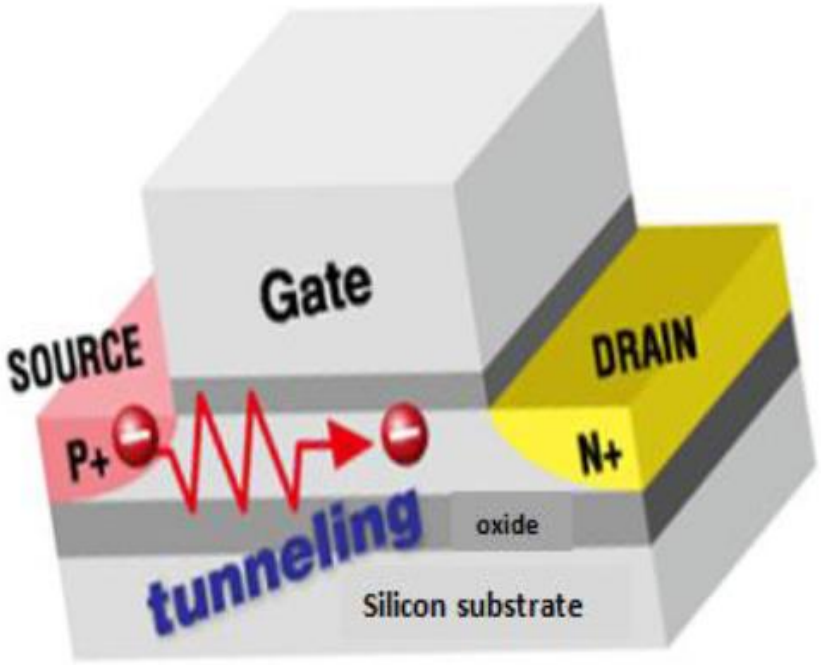


Figure 2.4.1.1 Conventional Tunnel MOSFET

There are two types of tunnel FETs are available n-type and p-type. n-type act like reversed biased p-i-n diode and p-type act like reversed biased n-i-p diode. The structure shown above is a SOI tunnel diode in which the source and drain are highly doped and channel is intrinsic. Here "i" represent intrinsic region.

Figure 2.4.1.2 represents the tunnelling process that occurs inside device when the tunnel FET is in OFF-state there is a significant energy barrier present between the source-channel. When gate voltage is below the threshold voltage the energy barrier between source and channel is very high as shown in figure 2.4.2 (a). at this time there is no tunnelling current flows and leakage current is also very low due to high energy barrier. Therefore we can easily conclude that in tunnel FET leakage current is very low. Now in ON-state when the applied gate voltage is above threshold voltage the valance band of source and conduction band of channel align

and electron in valance band of source find it very easy to move to the conduction band of channel[22]. Now this movement of electron contributes to the tunnelling current.

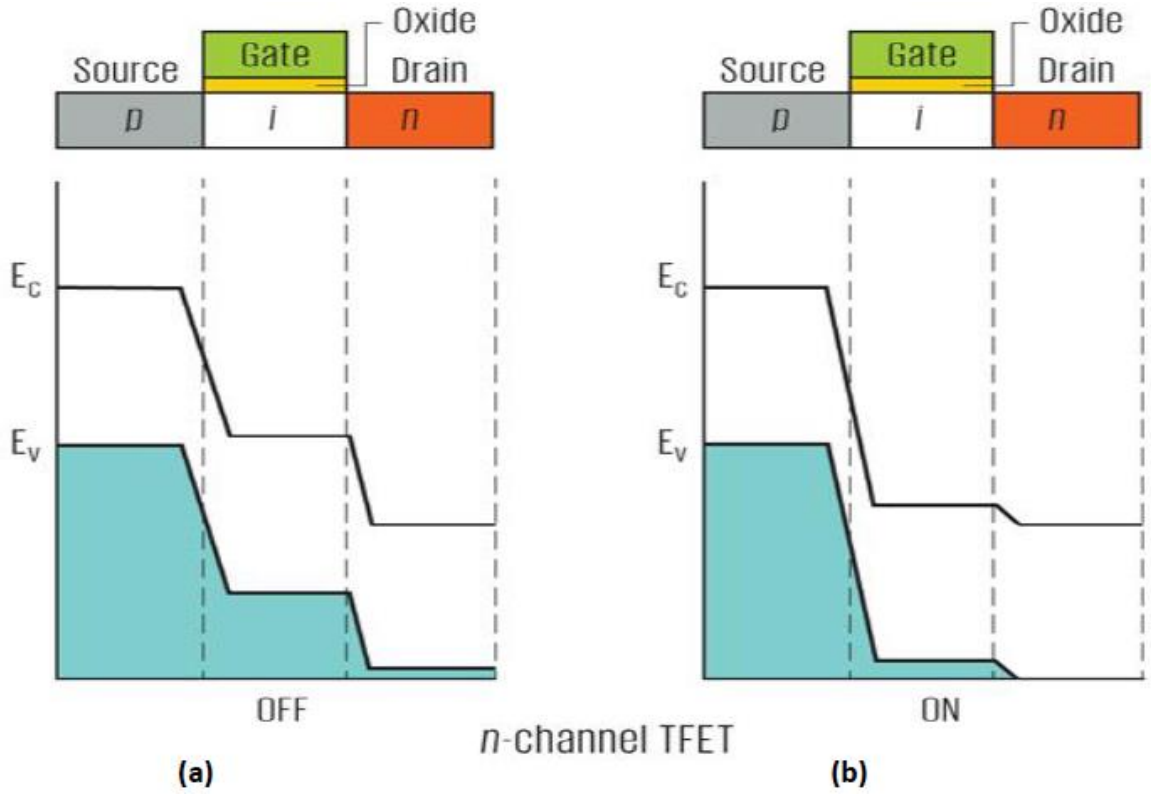


Figure 2.4.1.2 Energy band diagram of SOI MOSFET (a) OFF-state (b) ON-state

2.4.2 Ambipolar nature of Tunnel FET

Ambipolar is a unique phenomenon which happens with the tunnelling FET. The current conduction inside the Tunnel FET took place in both directions such that from source to drain and from drain to source. When the device is reversed biased for positive voltage more than threshold voltage of device the valance band of source is align with channel conduction band and current will flow from source to channel and when we apply negative voltage to the same device, for more negative voltage the valance band of drain get align with conduction band of channel and therefore we get negative drain current as shown in figure 2.4.2.1.

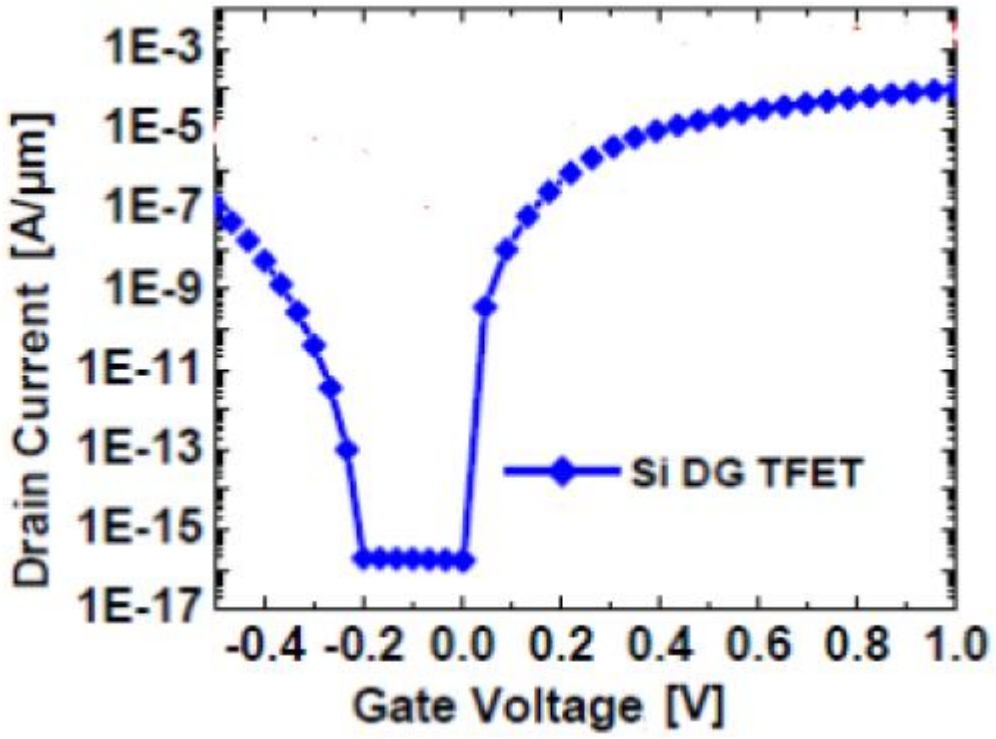


Figure 2.4.2.1 Transfer characteristics showing ambipolar nature for DG-Tunnel FET.

Now this ambipolar nature is not required property of tunnel device therefore to avoid this nature of device the doping level of source-channel- drain is taken in specific order[22]. Source and drain are highly doped and channel is soberly doped and also we can use High-k dielectric to avoid ambipolar nature of device.

2.5 Dual Metal gate Tunnel FET (DMG TFET)

Figure 2.5.1 shows the schematic of dual metal gate tunnel field effect transistor. Its almost similar to the conventional MOSFET but the only difference is that gate is made of two different metals having different work functions. Now by changing this works functions we can get better control over device channel. This type of device has proven to be having higher Ion-Ioff ratio and steeper subthreshold slope.

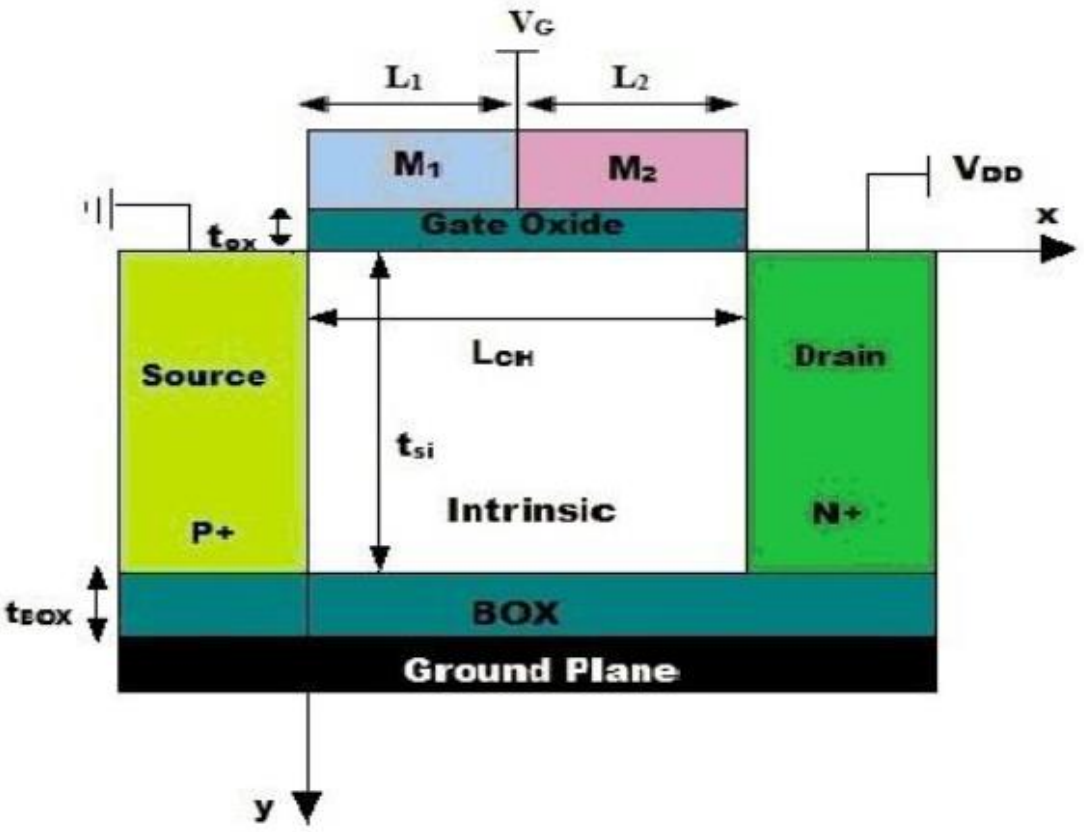


Figure 2.5.1 Cross-sectional view of Dual gate SOI Tunnel field transistor

Various researcher from all over globe has given special attention to the Dual gate metal device because it shows very promising characteristics due to better electrostatic control over gate. Using even high-k dielectric with dual metal prevents penetration of electron to the oxide layer which avoid the hot carrier injection in such device. Moreover the use of high-k give better transfer and output characteristics especially when it is used under tunnelling gate[30].

From this literature survey it is very clear that SiNT FET is a very potential device for future research especially in the era of nanotechnology. And all the points mentioned above in 2.3, 2.4, and 2.5 should be examined using SiNT FET and should be compared with the GAA MOSFET structure.

CHAPTER 3

Analog and radio-frequency performance analysis of silicon-nanotube MOSFETs

3.1 INTRODUCTION

Silicon-nano-tube (SiNT) MOSFETs have been analyzed recently in order to investigate their suitability for future ultra-large scale integration (ULSI) applications. Based on the study so for, it could be safely stated that the SiNT MOSFETs are very promising for future ULSI as they could be scaled down to 22nm gate length and below effectively [11-15]. The SiNT MOSFET provides ultimate electrostatic controllability to the gates in order to counter the short-channel effects because of its hollow cylindrical shape [14-17]. In SiNT MOSFETs, two gates, an outer gate and an inner gate, can act independently or together in order to realize the multi-threshold voltage transistors characteristics or high drain current, respectively [14]. The SiNT MOSFET is particularly considered to be unique in the sense that, unlike other MG MOS structures, it provides excellent SCE immunity even when the diameter of the tube is increased as long as the channel thickness is kept same [14]. Subthreshold electrical characteristics of SiNT FET have been studied through device simulation and it has been confirmed that the device outperforms GAA and other MG devices completely [14]. However, in the best of our knowledge, neither analog nor RF performance of the device has been studied till date in order to access its potential in system-on-chip applications. In the present letter, we have analyzed the analog as well as the RF characteristics of SiNT FETs using the ATLAS, a 3D device simulator from SILVACO [16]. Besides, the characteristics of SiNT MOSFETs have also been compared with the same of a nanowire based GAA FET to quantify the improvement in the performance.

3.2 DEVICE STRUCTURE

A hollow cylindrical structure of SiNT MOSFET with very thin channel is considered with two gates where one is the inner core gate and other is the outer shell gate, as shown in Figure 3.2.1(a). The three dimensional (3D) as well as the cross-section views of the structure is shown in Figure 3.2.1(a), (b) and (c). The core and outer gates are tied together to set the device in the symmetrical mode of operation. The oxide thickness of the both core gate and outer gate is considered to be 2nm.

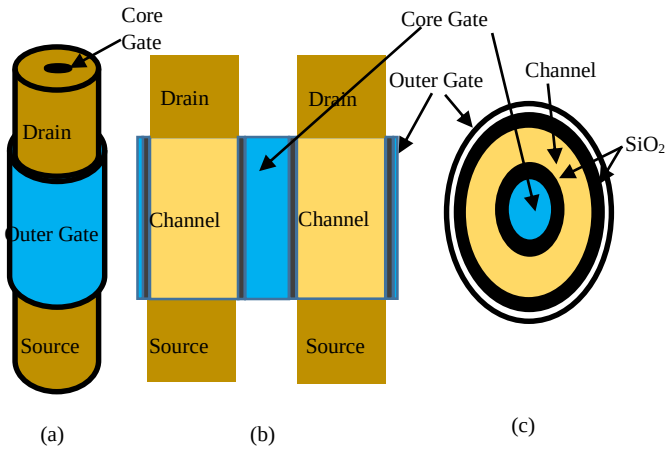


Figure 3.2.1(a) 3D- structure of a SiNT FET. Channel length = 20nm, channel thickness = 10nm, source length= drain length=10nm and inner core gate diameter = 10nm.

(b) Cross-section view of SiNT FET showing position of inner core gate.

(c) Top view of SiNT FET showing position of Sio_2 layer.

The doping concentration in source and drain regions are taken to be $1 \times 10^{20}\,cm^{-3}$(n-type).The channel doping concentration is considered to be $1 \times 10^{15}\,cm^{-3}$ (p-type). The nanowire GAA MOS structure, which has been considered for characteristics comparison, is almost similar to SiNT FET with no inner gate, as shown in Figure3.2.2(a), (b) and (c).

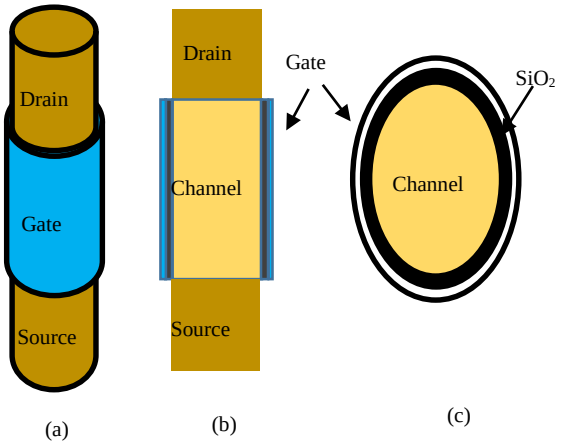


Figure 3.2.2(a) 3D- structure of a GAA FET. Channel length = 20nm, channel thickness = 10nm, source length= drain length=10nm.

(b) Cross-section view of GAA FET.

(c) Top view of GAA FET showing position of Sio_2 layer.

In order to set the same threshold voltage (0.1477 eV) in both devices, the gate work function of SiNT MOSFETs and GAA MOSFETs are considered to be 4.7 eV and 4.639 eV respectively. For devices, channel length and channel thickness are 20 nm and10 nm respectively.

3.3 RESULTS AND DISCUSSION

After applying proper biasing to SiNT FET the drain current I_d is plotted against the gate voltage and the drain voltage in Figurers 3.3.1(a) and (b), respectively. To plot I_d verses gate voltage (V_g), the drain voltage (V_d) is kept constant at 0.1V and gate voltage is vary stepwise in ATLAS Deckbuild window. Similarly, I_d verses V_d is plotted by keeping gate voltage constant at 0.1 V and changing value of drain voltage.

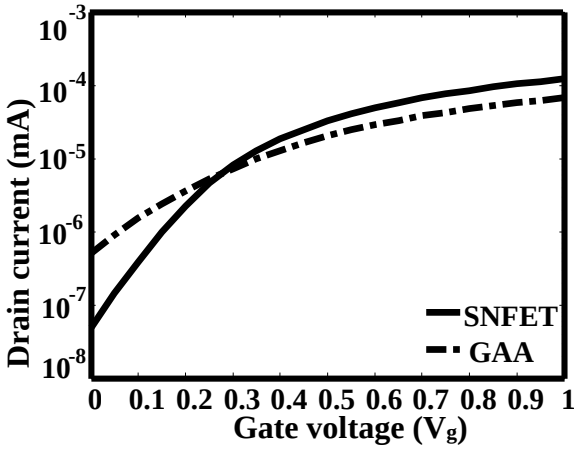


Figure 3.3.1(a) Comparison of transfer ($I_d - V_g$) characteristics of SiNT FET and GAA FET. Where I_d =drain current, V_g = gate voltage and V_d = drain voltage. The device parameters: source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type). Oxide thickness for both outer and inner gate is 2nm, channel length is 20nm and channel thickness is 10nm.

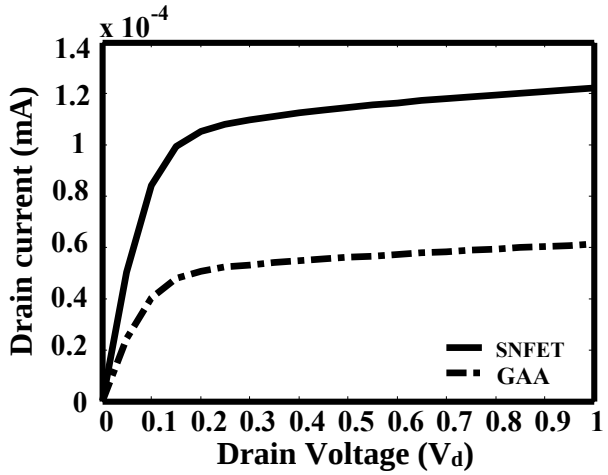


Figure 3.3.1(b) Comparison of drain ($I_d - V_d$) characteristics of SiNT FET and GAA FET. The device parameters: source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type). Oxide thickness for both outer and inner gate is 2nm, channel length is 20nm and channel thickness is 10nm.

In Figure 3.3.1(a) and (b), corresponding data are also included for nanowire GAA MOSFETs for the sake of comparison. It can be noticed that the sub-threshold slope of the SiNT MOSFET is much steeper than that of GAA MOSFET (in Figure 3.3.1 (a)). And, SiNT MOSFET could deliver more drive current compared to the GAA MOSFET of same channel thickness and channel length as shown in figure3.3.1(b) . Thus, the I_{on} of SiNT MOSFET is higher than that of GAA and I_{off} is lower than GAA. It may be attributed to the following facts (i) since the channel region is surrounded by the gates from both sides unlike a GAA MOSFET, the gates are in excellent position to control the channel charges. . This utmost electrostatic control of channel charges is responsible for the improved subthreshold characteristics of SiNT FETs. (ii) the full volume inversion in the channel region causes high carrier mobility in the bulk due to reduced scattering associated with oxide-interface trapped charges and surface roughness. (iii) at the selected channel thickness, the effective cross-sectional area of SiNT FETs is much higher than that of a GAA MOSFETs. The parameter g_m / I_d, which is also called as transconducatnce efficiency, of both SiNT MOSFETs and GAA MOSFETs is plotted against drain current in Figure 3.3.2.

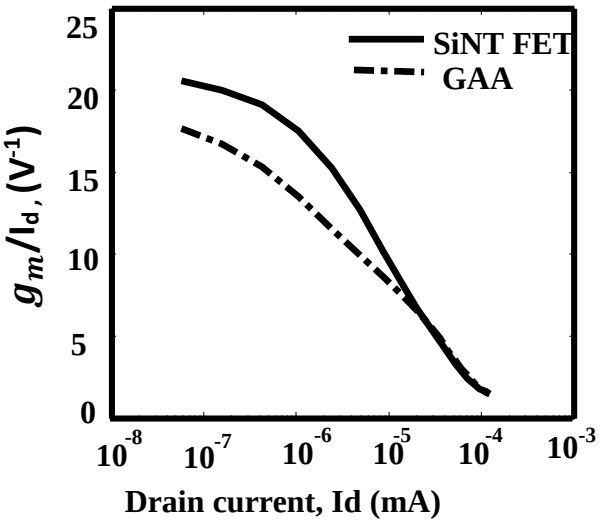


Figure 3.3.2 Comparison of g_m / I_d *vs* I_d of SiNT FET and GAA. Here $V_{ds} = V_{gs}$ = 1V, channel length = 20nm, channel thickness = 10 nm, source length = drain length = 10 nm, $f_i = 1GHz$ and work function = 4.7

eV for SiNT FET and 4.639eV for GAA to match threshold voltage. Source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type).

Here, it is worth mentioning that g_m / I_d ratio is a measure of channel inversion level, a lower value of g_m / I_d indicates a strong inversion in the channel region and vice versa. It can be noted from Figure 3.3.2 that in the weak inversion regime of device operation, since g_m / I_d of SiNT MOSFET is higher than that of GAA, the inversion carriers concentration is lower in case of SiNT FETs compared to the GAA MOSFETs, which is an indication of better subthreshold characteristics in SiNT MOS devices.

The RF performance is mainly characterized by the cut-off frequency (f_T) and the maximum frequency of oscillation (f_{MAX}). The f_T is defined as the frequency at which the short circuit current gain decreases to unity (sometimes called as unity gain frequency). And is given by [17]

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{1}$$

Where g_m is the transconducatnce and C_{gg} is the gate capacitance.

The f_{MAX} is the frequency where power gain become unity (sometimes also called as maximum power gain frequency) and is given by [17]

$$f_{MAX} = \frac{g_m}{2\pi C_{gs}\sqrt{4\left(g_{ds} + g_m \frac{C_{gd}}{C_{gs}}\right)\left(R_s + R_{ch} + R_g\right)}} \tag{2}$$

Where C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitance respectively, g_{ds} is the output conductance, R_S - source resistance, R_{ch} – channel resistance and R_g – gate

resistance. However, in this work f_T and f_{MAX} are determined using H and Y parameters as follows [17]

$$f_T = f_i.|H_{21}| \tag{3}$$

$$f_{MAX} = f_i\left[\frac{|Y_{21} - Y_{12}|^2}{4\left[Re(Y_{11}).Re(Y_{22}) - Re(Y_{21}).Re(Y_{12})\right]}\right]^{\frac{1}{2}} \tag{4}$$

Where f_i is the input signal frequency. The H and Y parameters for both devices have been determined using high frequency simulation at $f_i = 1GHz$. f_T And f_{MAX} obtained from Eqs. (3) And (4), respectively, are presented in Figure 5(a) and 5 (b).

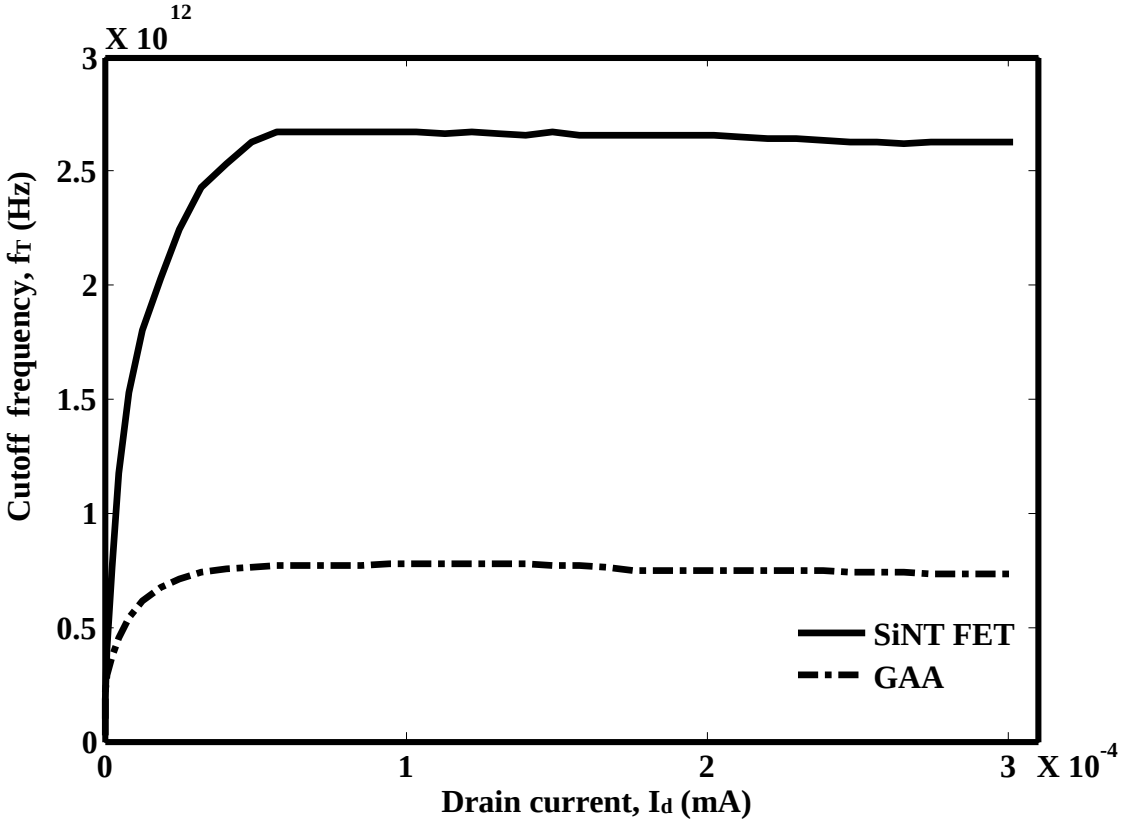


Figure 3.3.3 (a) Comparison of cut-off frequency (f_T) curve of SiNT FET and GAA. Here $V_{ds} = V_{gs}$ = 1V, channel length = 20nm, channel thickness = 10nm, source length = drain length = 10nm, $f_i = 1GHz$ and work function = 4.7 eV for SiNT FET and 4.639eV for GAA to match threshold voltage. . Source and drain doping

concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type).

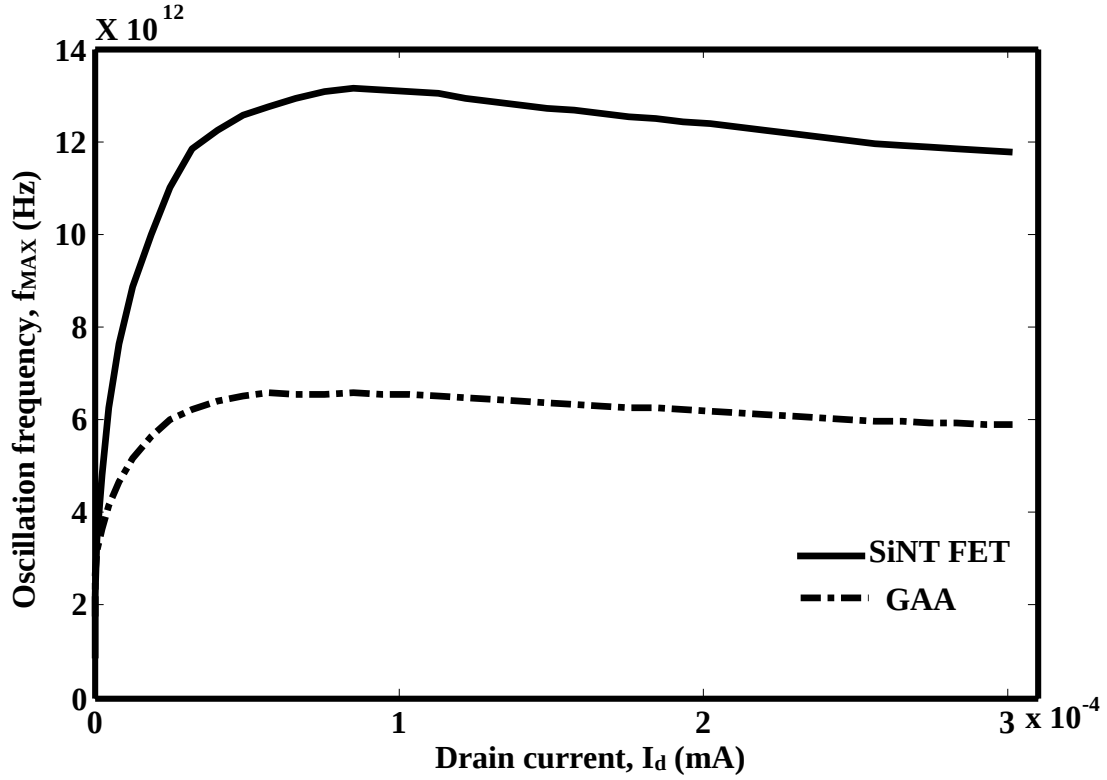


Figure 3.3.3(b) Comparison of maximum frequency of oscillation (f_{MAX}) curve of SiNT FET and GAA. Same data as above is used. . Here $V_{ds} = V_{gs}$ = 1V, channel length = 20nm, channel thickness = 10nm, source length = drain length = 10nm, $f_i = 1GHz$ and work function = 4.7 eV for SiNT FET and 4.639eV for GAA to match threshold voltage. . Source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type).

It could be noticed from the Figure 3.3.3(a) and (b) that SiNT FET has far better RF performance as compared to GAA. Following are the important observations (a) f_T is found to be 2670GHz for SiNT FET and 777GHz for GAA MOSFETs at $I_d = 1\,x\,10^{-4} mA$, which is almost 3.5 times improvement at selected device parameters (b) f_{MAX} is found to be 13082

GHz for the SiNT FET and 6540GHz for the GAA MOSFET at $I_d = 1\,x\,10^{-4} mA$, which is almost two times improvement. This improvement in the RF performance of SiNT FETs may be attributed to the high g_m value offered by the device owing to the better drain current driving capability.

In Figure 3.3.4(a) and 6(b), f_T and f_{MAX} of SiNT FETs are demonstrated for different channel thickness (t) keeping other parameters constant as mentioned in the figure caption.

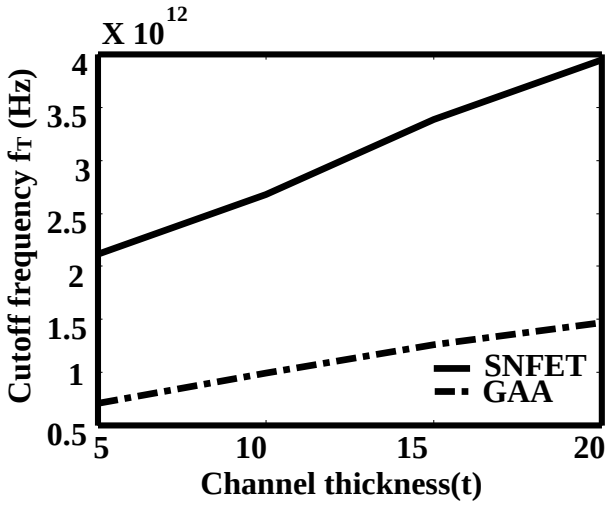


Figure 3.3.4(a) Comparison of cut-off frequency (f_T) vs channel thickness (t) for SiNT FET and GAA. Here $V_{ds} = V_{gs}$ = 1V, channel length = 20nm, channel thickness (t) = 5,10,15,20 nm, source length = Drain length = 10nm and $f_i = 1GHz$ .Source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type).

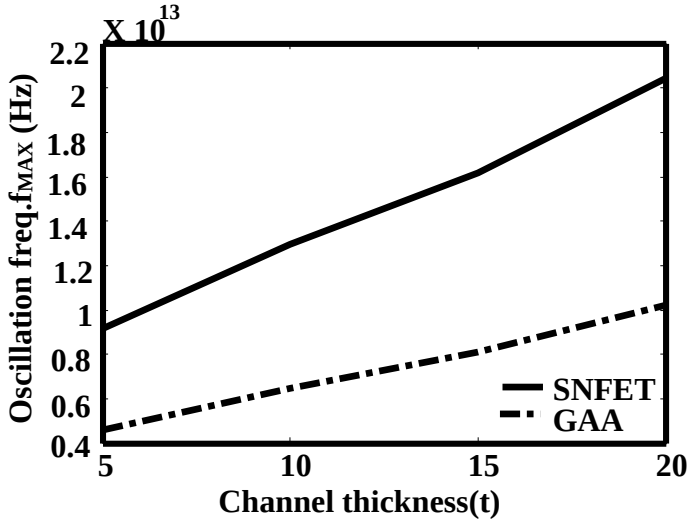


Figure 3.3.4(b) Comparison of maximum frequency of oscillation (f_{MAX}) vs channel thickness (t) for SiNT FET and GAA. Same data as above is used. . Here $V_{ds} = V_{gs}$ = 1V, channel length = 20nm, channel thickness (t) = 5,10,15,20 nm, source length = Drain length = 10nm and $f_i = 1GHz$ .Source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type).

The results are also compared with the same of GAA MOSFETs. In order to fix the threshold voltage of 0.14777 V for both devices under comparison different gate work functions have

Channel thickness,t (nm)		5	10	15	20
Work function(Ø),(eV)	SiNT FET	4.59	4.7	4.793	4.915
	GAA	4.6189	4.7	4.808	4.917

Table 3.3.1 : Channel thickness and there corresponding work functions used for simulation. . Here $V_{ds} = V_{gs}$ = 1V, channel length = 20nm, channel thickness (t) = 5,10,15,20 nm, source length = Drain length = 10nm and $f_i = 1GHz$ .Source and drain doping concentration are be 1 x 10^{20} cm^{-3}(n-type), The channel doping concentration is considered to be 1 x 10^{15} cm^{-3} (p-type).

been selected for both devices at different channel thicknesses, as shown in Table3.3.1.

In Figure 3.3.4 (a) and (b), f_{MAX} and f_T are found to be increased with the increase in the channel thickness. And, for all channel thickness variation SiNT FETs show a superior performance.

3.4 CONCLUSION

The present analog and RF performance study shows that the SiNT FETs can be used in more demanding situation. SiNT FETs offer high drive current and can be considered for high frequency circuit design because of relatively higher f_T and f_{MAX} parameters value, compared to GAA MOSFETs. Thus, SiNT FETs with excellent digital, analog and RF performance are the most worthy candidates for system-on-chip (SoC) design.

CHAPTER 4

Si-Nanotube MOSFETs with catalytic metal gate for gas sensing applications

4.1 INTRODUCTION

Increase in the environmental pollution and industrialisation leads to the emission of various gases and detection of these gases are very important. Therefore gas detecting devices are in very high demands. The gas detection can be done by various electrical or chemical devices but gas detector based on MOSFET's are in high demands. MOSFET based gas detector shows lots of advantages over other gas detectors. Some of these advantages are low cost, low power consumption, small size and there sensitivity are high too. Since MOSFETs are purely semiconductor devices therefore they are made of mainly silicon and hence they are cheap and since few voltages are required to operate these devices there power consumption are low[18]. And in this chapter later it will be shown that there sensitivity are also very high.

In recent years several gas detector has been developed which changes there gate metal work function in the presence of gas. Research in this field has taken two different paths 1) Finding suitable sensitive films for catalytic gate , metal compounds, hydrate salt and organic compound which can serve as catalytic gate[18].

2) Device engineering like changing device structure or using dual metal gate and techniques that will bring more sensitivity towards gas sensing[18].

To create a better gas detector various devices has been taken into account like dual gate metal MOSFET, SOI MOSFET, Nanowire FETs and now Si-nanotube FETs. There has been extensive study done on conventional MOSFET, SOI MOSFET and Nanowire FETs but till now there is no research has been done on SiNT FET as a gas sensor. Therefore in this chapter gas sensitivity of SiNT FET has been examined and it is compared with the Nanowire FETs or Gate-all-around MOSFET (GAA MOSFET).

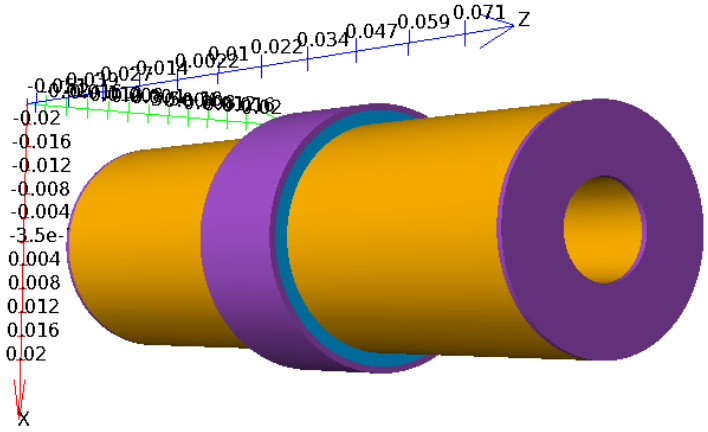
Gas sensitivity for a device will be high if gas will find more area to react such as surface-to-volume ratio should be high and it is well known that GAA MOSFET has more surface area as compared to the conventional MOSFET which results in higher sensitivity of GAA as compared to conventional MOSFET. But due to presence of core gate in SiNT FET its surface to volume ratio is higher than that of GAA MOSFET. Therefore SiNT FET provides more surface to gas for reaction. Therefore late in this chapter it will be shown that SiNT FET has higher gas sensitivity than GAA MOSFET.

Another class of gas detector has been taken into account and these detectors utilizes the catalytic metal gate. The basic property of catalytic metal is that it changes its work function proportional to the presence of gas. Change in the work function leads to change in the surface potential of the device and change in surface potential leads to change in the subthreshold voltages.

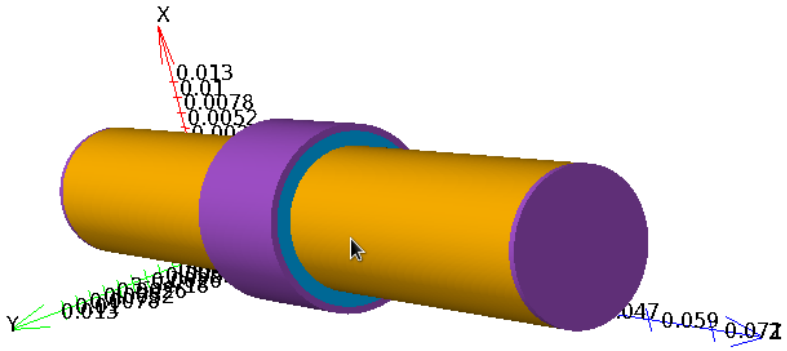
In recent study it is found that p-channel MOSFET with palladium (Pd) as a gate metal can be used for hydrogen sensing and n-channel MOSFET with silver (Ag) metal gate can be used for oxygen sensing. Therefore in this chapter p-channel SiNT FET with palladium metal gate for hydrogen sensing and n-channel SiNT FET with silver metal gate for oxygen sensing has been examined and the result is compared with the GAA MOSFET [18-24].

4.2 DEVICE STRUCTURE

3D Structure of SiNT FET is shown below in figure 4.2.1(a). It's basically a cylindrical structure having two gates. One is outer gate and other gate is called core gate. Channel is bounded between these two gates. Below shown is a Deckbuild generated structure from ATLAS.



(a)



(b)

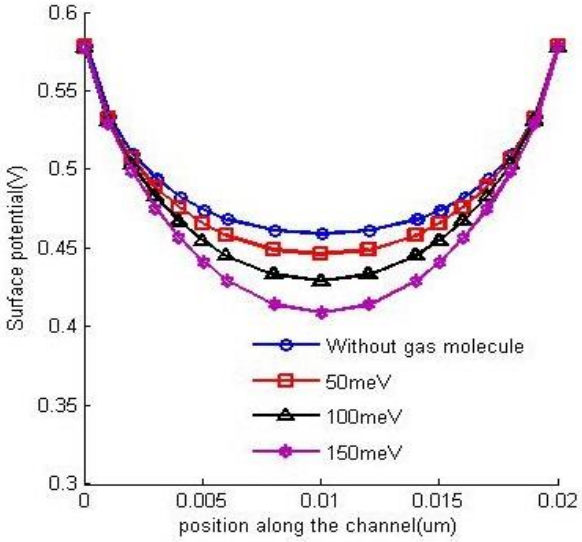
Figure 4.2.1. (a) Simulated structure of SiNT FET. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) =1 × 10^{21} $m^{-3.}$ (b) Simulated structure GAA MOSFET. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) =1 × 10^{21} $m^{-3.}$

The channel length of the device is kept at 20nm, channel thickness is 10nm, oxide thickness is 2nm, channel doping is (N_A) =1 × 10^{21} $m^{-3.}$ Source and Drain doping is kept at N_D=1 × 10^{20} cm^{-3}. SiNT FET is compared with the GAA MOSFET and it is found that SiNT FET has more gas detection sensitivity. The structure of GAA MOSFET is shown in the figure 4.2.1(b). The basic diffrance between two devices is that there is only one gate prasent (outer gate) in GAA MOSFET and in case of SiNT FET one extra inner gate is prasent.

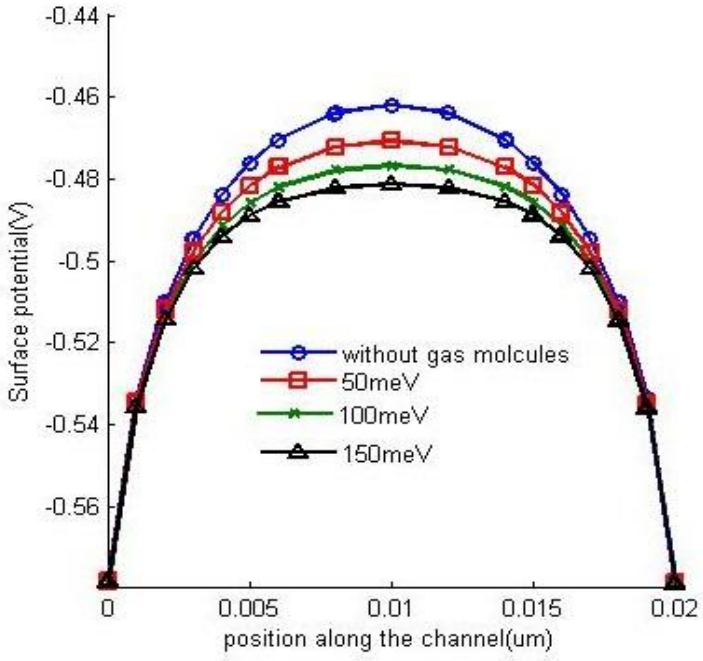
Now due to two gate in SiNT FET the electrostatic control of gate over channel is excelent which leads to very less leakage current. Due to two gate there will be bulk inversion formation which results in reduced surface scattering. Other benifits of SiNT FET over GAA are it has higher drive current ,reduced short channel effects and steeper suthreshold slope. These advancement of SiNT FET over GAA concludes that SiNT FET can give better result than GAA MOSFETs.

4.3 RESULTS AND DISCUSSION

The FET used for gas detection is works like an electrical transducer which transform shift in the work function into change in the output current or threshold voltages changes. Figure 4.3.1(a) and (b) shows the effect of shift in the work function of catalytic metal on surface potential of device. Figure 4.3.1 (a) represents change in the surface potential of n-channel SiNT FET with silver metal gate which is used for oxygen sensing and 4.3.1 (b) shows change of surface potential on p-channel SiNT FET with palladium gate used for detection of hydrogen. Gas molecule presents at the catalytic gate surface starts reacting with metal and this reaction leads to the change of work function which changes the flat-band-voltages due to addition band bending. Now this change in flat-band-voltage results in the change in the surface potential which further changes the threshold voltages of device. Change in threshold



(a)



(b)

Fig4.3.1. (a) Effect of work function change on surface potential of n-channel SiNT FET with Ag metal gate. Device parameters: channel length (L) =20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3.}$ (b) Effect of work function change on surface potential of p-channel SiNT FET with Pd metal gate. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) =1 × 10^{21} $m^{-3.}$

voltages V_{th} changes the drain current. Now by monitoring change in any of these parameter like surface potential, threshold voltage and drain current.

Since the prasence of gas changes the workfunction of catalytic metal gate this change in the work function $\Delta\emptyset_m$ depends upon the metal gate used and the gas prasence and is given by :

$$\Delta\emptyset_m = \text{const} - \left(\frac{RT}{4F}\right) lnP$$

Where T is absolute temperature, R is gas constant, F is Faraday's constant and P is the partial pressure of gas[18]. Since partial pressure depends upon the concentration of gas there fore gas detector can also be used for detection of amount of the gas and that same device can aslo be calebrated to merasure mole fraction of gas in air.

Now for the sake of the simulation of device we will consider that change in the work function will be approximately 50meV, 100meV and 150meV. Since the change in the work function will depends upon the concentration of the gas molecule present. This work is purely based on simulation therefore we will examine change in drain current for above mentioned three work functions. Simulation of both SiNT FET and GAA FET has been done for channel length of 20nm and 50nm and obtained result will be shown later in this chapter.

Figure4.3.2(a) and (b) shows the effect of changing the work function on drain current. Figure 4.3.2 (a) represents change in drain current with change in gate voltages keeping drain voltage at 0.05v for n-channel SiNT FET with silver metal gate having channel length 20nm. It is clear from the plot that there is very minute change in the on current $I_{on.}$ While there is exponential change in the off current $I_{off.}$ Therefore we can easily measure change in I_{off} than change in $I_{on.}$ Similarly, Figure 4.3.2 (b) shows output for p-channel SiNT FET with Pd gate metal having channel length 20nm. Here also it is clear that I_{off} changes more exponentially than the I_{on}.

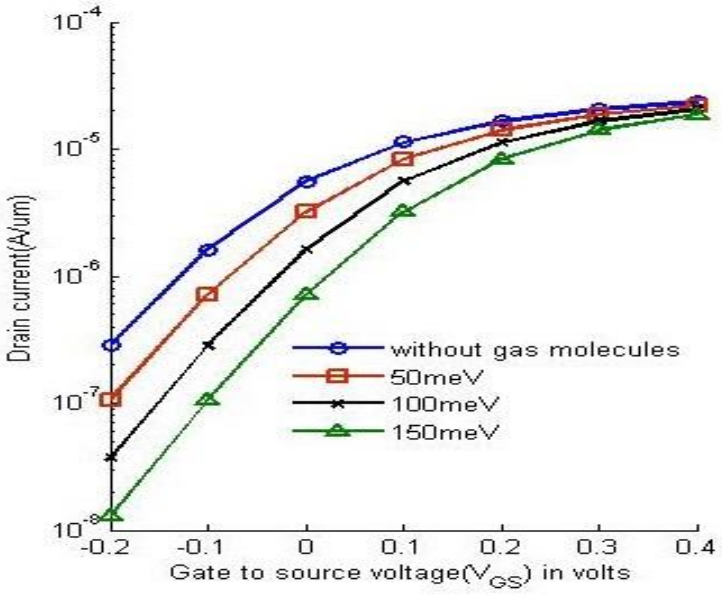


Figure 4.3.2. (a) I_d versus Vgs with and without gas molecules for n-channel SiNT FET with Ag metal gate. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ drain-to-source voltage (Vds) = 0.05 V.

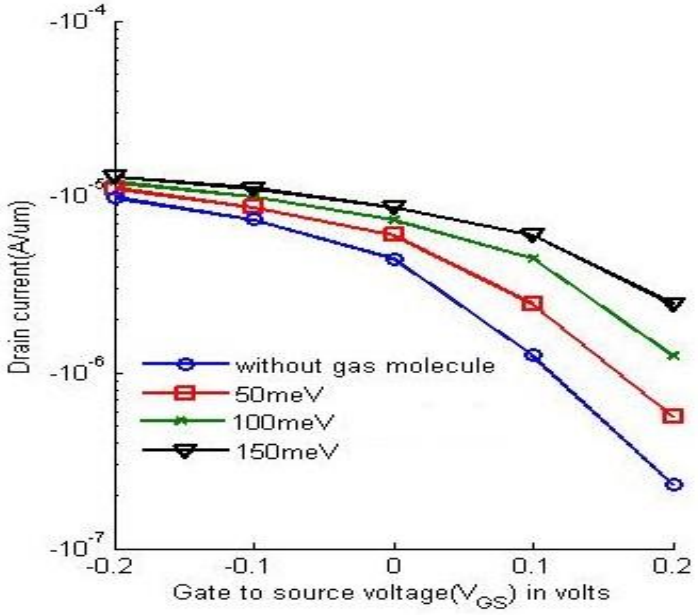


Figure 4.3.2 (b) I_d versus Vgs with and without gas molecules for p-channel SiNT FET with Pd metal gate. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ and drain-to-source voltage (Vds) = 0.05 V.

As it can been seen that I_{off} changes steeper than Ion therefore we can operate these device in subthreshold region. And operating any MOSFET in subthreshold region will result in low power consumption. Therefore using SiNT FET as a gas detector will result in low power consuming device. As we are measuring drain current not threshold voltages therefore there is no need of using any extra circuits to measure V_{th} which will results in low cost also. This high sensitivity of I_{off} can be attributed to the fact that due to shift in catalytic metal work function there will be addition band bending in absence of Fermi level because of reaction of the gas molecule at the surface.

Figure 4.3.3 (a) and (b) shows similar results for the 50nm channel length.

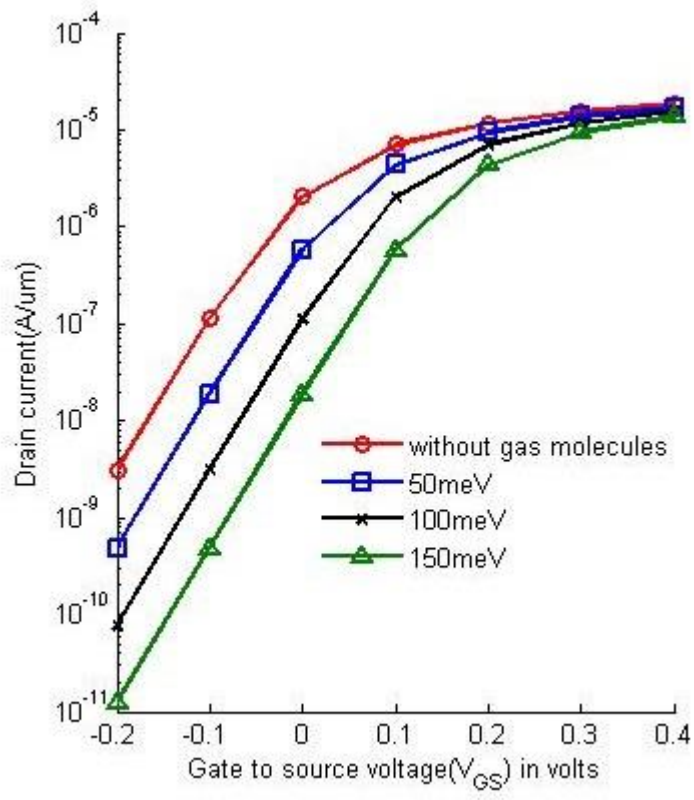


Figure 4.3.3. (a) I_d versus Vgs with and without gas molecules for n-channel SiNT FET with Ag metal gate. Device parameters: channel length (L) = 50 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ drain-to-source voltage (Vds) = 0.05 V.

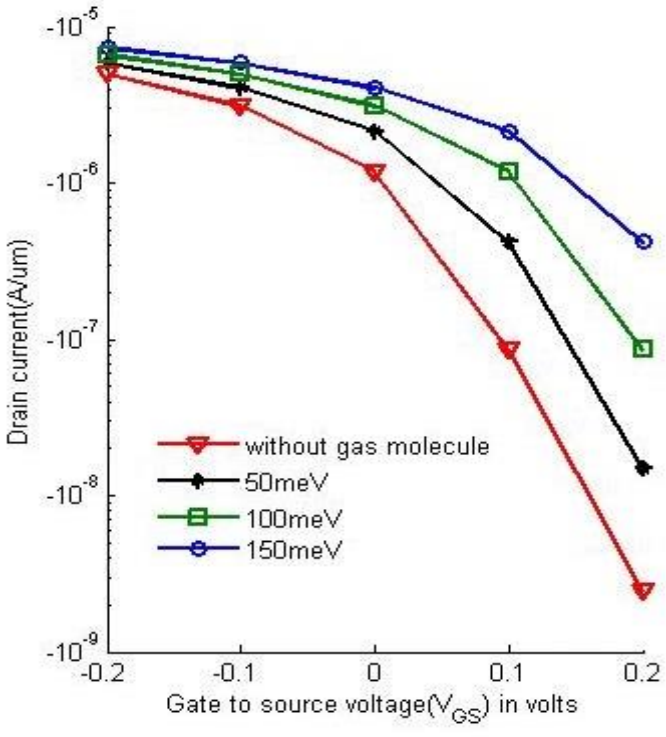


Figure 4.3.3 (b) I_d versus Vgs with and without gas molecules for p-channel SiNT FET with Pd metal gate. Device parameters: channel length (L) = 50 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ and drain-to-source voltage (Vds) = 0.05 V.

In figure 4.3.3 (a) drain characteristics of n-channel SiNT FET with silver catalytic gate for oxygen sensing and as explained earlier similar results are obtained here. I_{off} changes exponentially as compared to I_{on} which can be attributed to the fact that shift in work function results in additional ban bending. Similarly, figure 4.3.3 (b) shows drain characteristics for p-channel SiNT FET with palladium metal gate used for hydrogen sensing. Here also drain curve is obtained for different work functions 50meV, 100meV and 150meV.

Figure 4.3.4(a) and (b) shows the drain characteristics of GAA MOSFET which is compared with the SiNT FET. In previous published paper it is shown that GAA MOSFET has higher gas sensitivity as compared to the conventional MOSFETs. Figure4.3.4 (a)shows drain characteristics for n-channel GAA MOSFET with silver gate for oxygen sensing.4.3.4 (b)

shows drain characteristics for p-channel GAA MOSFET with palladium gate for hydrogen sensing.

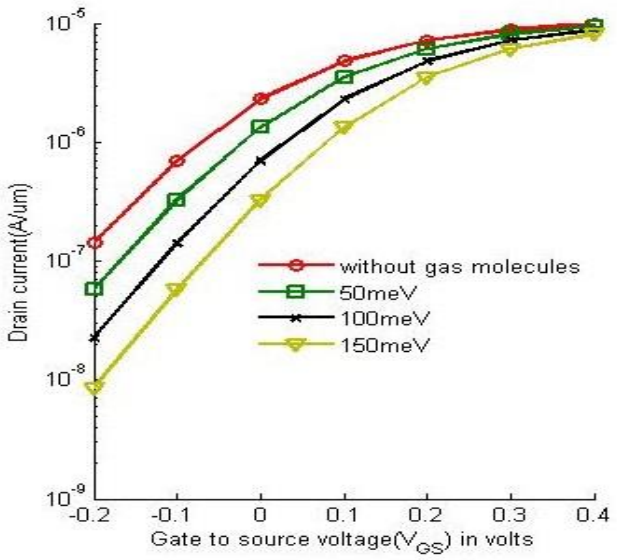


Figure 4.3.4. (a) I_d versus Vgs with and without gas molecules for n-channel GAA MOSFET with Ag metal gate. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ drain-to-source voltage (Vds) = 0.05 V.

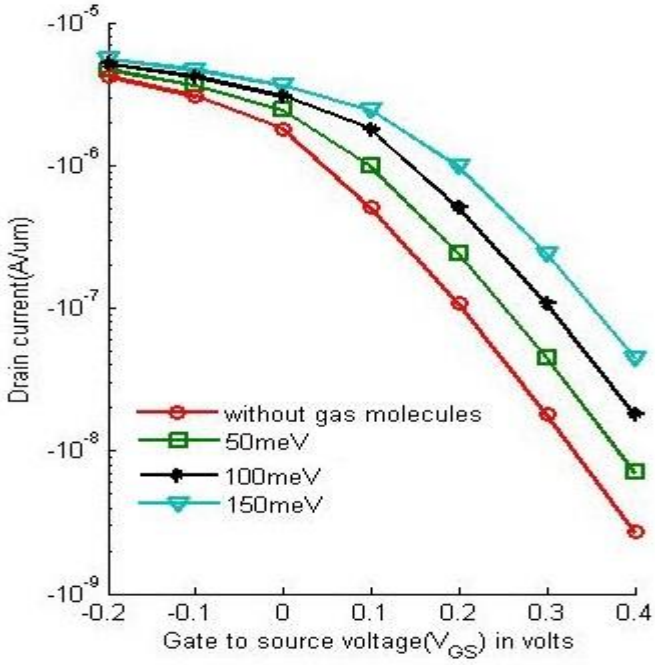


Figure 4.3.4 (b) I_d versus Vgs with and without gas molecules for p-channel GAA MOSFET with Pd metal gate. Device parameters: channel length (L) = 20 nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ and drain-to-source voltage (Vds) = 0.05 V.

Table 4.3.1 shows the sensitivity comparison of n-channel SiNT FET with n-channel GAA MOSFETs. The sensitivity of device is measured by calculating the ratio between I_{off} (without gas molecule) and I_{off} (with gas molecule) and it is found that as channel length increases the sensitivity of device also increases.

Change in work function $\Delta\phi_m$	Channel length=20nm		Channel length=50nm	
	I_{off} (without gas molecule)/I_{off} (with gas molecule)		I_{off} (without gas molecule)/I_{off} (with gas molecule)	
	SiNT FET tsi = 10nm	GAA tsi = 10nm	SiNT FET tsi = 10nm	GAA tsi = 10nm
50meV	2.695	2.452	9.350	6.231
100meV	8.927	6.266	47.537	39.209
150meV	22.109	16.338	280.406	246.65

Table 4.3.1: Shows the sensibility comparison result of n-channel SiNT FET with n-channel GAA MOSFET. Device parameters: channel length (L) = 20 nm and 50nm, radius (R) = 5 nm, oxide thickness (t_{ox}) = 2 nm, channel doping (N_A) = 10^{21} $m^{-3,}$ and drain-to-source voltage (Vds) = 0.05 V.

As it is clear from table higher the concentration of gas higher will be the change in work function and higher will be the sensitivity. For 20nm channel length the sensitivity for SiNT FET is very high as Ioff changes 22.109 times and in case of GAA it only changes by 16.338. But if we increases to channel length to 50nm for 150meV change in work function the Ioff changes 280.406 times for SiNT FET compared to the 246.65 in case of GAA MOSFET. Now this higher sensitivity occurs may be because with increase in channel length the surface area increases and volume to area ratio also increases. And in all case of work function change it is clear from the table that SiNT FET has higher sensitivity compared to GAA MOSFET.

4.4 CONCLUSION

Si-nanotube MOSFETs (SiNT FET) with catalytic metal gates can be used for gas sensing applications. P-channel SiNT FET with palladium (Pd) metal gate is proposed for hydrogen sensing, whereas N-channel SiNT FET with silver (Ag) metal gate can be used for oxygen gas sensing. A simulation based study has been carried out using ATLAS-3D numerical simulator, and it is found that SiNT FETs have more efficiency towards the hydrogen and oxygen detection than the recently proposed cylindrical gate-all-around (GAA) MOSFETs.

CHAPTER 5

Performance analysis of single dielectric dual material gate Si-nanotube tunnel FET

5.1 Introduction

The demand of small size , low power consuming ,less leakage and low cost semiconductor devices has been increased to follow the ITRS bellow 22nm technology node. To reach technology nodes bellow 22nm, fallow moors law and ITRS scientist has been looking for non-conventional MOSFETS like dual gate MOSFET, trigate MOSFET, FIN FET, Gate-All-Around MOSFETs etc. because conventional MOSFET cannot reach such small size due to increase in leakage current. The current scenario required ultra-low-power devices and this employ reduction in the voltage supply $V_{dd.}$ Till now according to ITRS we has reduces Vdd by using theory of scaling to 0.9 and the projected target is 0.8 by 2015. But further reduction of Vdd is not possible by using scaling theory due to fundamental limit possess by current conduction in conventional MOSFET which thermionic by nature. Therefore subthreshold slope (SS) creates huddles for the further scaling of Vdd. This scaling limit on Vdd is due to kT/q factor value due to which the subthreshold slope cannot go below 60mV/dec[22-31].

To answer the challenge presented by subthreshold slope (SS), tunnelling devices like tunnel field effect transistors represents better and promising solution to construct low power devices. Because it is possible to achieve SS below 60 mV/dec. the transport of charge carrier in tunnelling device fallow quantum mechanical band-to-band-tunnelling BTBT instead of thermionic mechanism[22].

This chapter represent the detailed analysis of single dielectric dual metal gate (SD-DMG) Si-nanotube tunnelling FET (SiNT FET) and results obtained has been compared with the single dielectric single metal gate (SD-SMG) Si-nanotube tunnelling FET (SiNT FET). In this chapter we had tried to find the effects of change of work function in tunnelling device at the source side as well as at the drain side. Due to change in the work function there will be changes in the drain characteristics and output characteristics for SD-DMG and that changes are plotted and presented here. Similar analysis has been carried out for SD-SMG and comparisons between the obtained results has be shown later in this chapter. Other analysis

like change in drain current due to change in channel length L_g for SD-DMG and SD-SMG for tunnelling device is also presented. RF analysis for SD-DMG has been done and parameter like transconducatnce and intrinsic capacitance has been found and plotted. All the simulation work of device has been done using 3D device simulator ATLAS from SILVACO.

5.2 Device structure

The structure of the device under consideration is shown in Fig.5.2.1 where p+-intrinsic-n+ silicon regions which form the source-channel-drain is shown it is the cross sectional view of DMG SiNT FET. The structure has been simulated using ATLAS^{TM}, version 5.18.3.R. from Silvaco. Non local BTBT model along with band gap narrowing model have been incorporated in the simulation. In all our simulations, source-channel and drain-channel junctions are considered to be abrupt. The gate oxide spans over the intrinsic silicon channel.

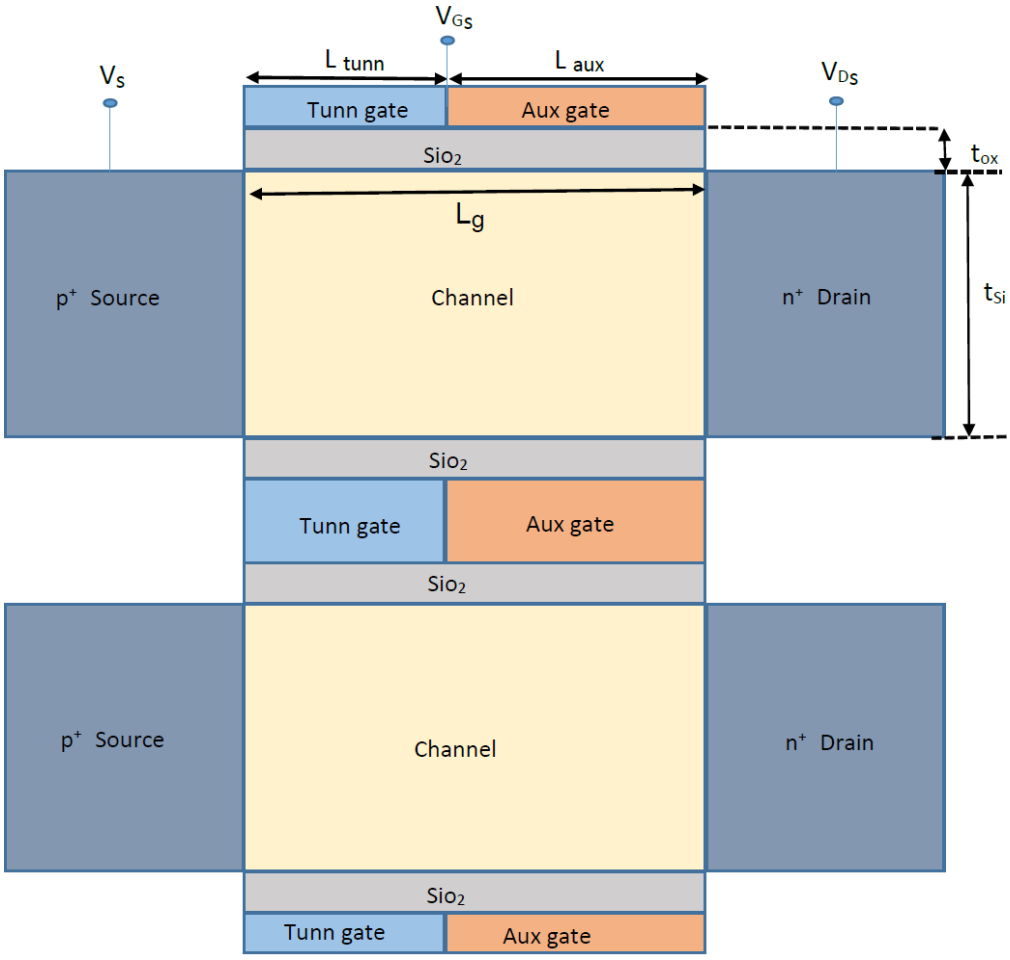


Figure 5.2.1. Cross-sectional view of SD-DMG SiNT FET.

Table 5.2.1: Device parameter taken for the simulation of device

Gate oxide thickness (t_{ox})	2nm
Total channel length (L_g)	50nm
Length of tunnel gate (L_{tunn})	20nm
Length of auxiliary gate (L_{aux})	30nm
Channel thickness (t_{si})	10nm
Source doping	1 x 10^{20} atoms/cm^3 p.type
Channel doping	1 x 10^{16} atoms/cm^3 p.type
Drain doping	5 x 10^{18} atoms/cm^3 n.type

As shown in table 5.2.1 the channel length L_g is consider 50nm which is equal to the summation of tunnel gate length L_{tunn} 20nm and auxiliary gate length L_{aux} 30nm. The oxide thickness t_{ox} is 2nm and channel thickness t_{si} is consider to be 10nm. Source is doped with p+ type and drain with n+ and channel doping is consider moderate.

5.3 Result and discussion

SD-DMG SiNT FET is actually a reverse biased p-i-n diode. Here tunnel device n-type. Initially the barrier height between the sources-channel- drain is sufficiently high so that no current flows in off stage. But when we apply positive voltage to drain and channel after appropriate amount of voltage the energy barrier between valance band of source and conduction band of channel overlaps and thus tunnelling takes place. Now by changing the work function of both tunnelling as well as auxiliary gate modulation of band overlap can be achieved. Therefore we can have electrostatic control over channel.

Fig.5.3.1 shows the energy bands horizontally across the body of the device in the OFF-state with a reverse bias (V_{DS}=1 V) applied across the p-i-n junction without any voltage at the gate. To modulate band overlap between source and channel we fixed work function of tunnel gate φ_{tunn} at 4.0 and changes the work function of auxiliary gate φ_{aux} . The obtained result is shown in Fig. 5.3.1. It is clear from the plot that steepness for the $\varphi_{\text{aux}} = 4.0$ is highest

and least for the $\varphi_{\text{aux}} = 4.8$. Therefore for higher value of φ_{aux} there will be very less amount of leakage current flow.

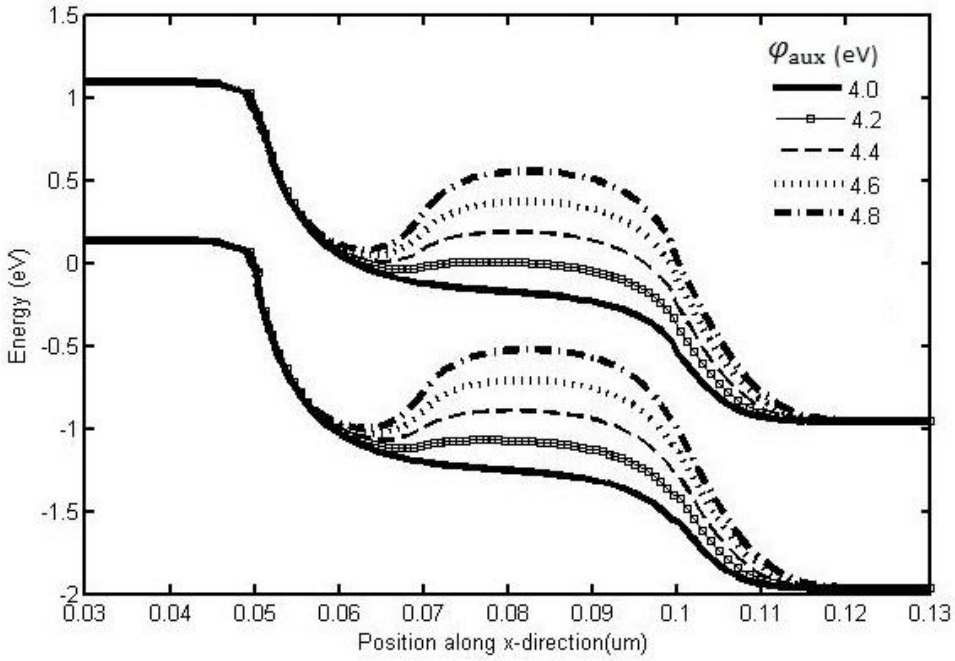


Fig.5.3.1: Schematic of energy band diagram for the OFF state in the SD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0eV, L_{tunn} = 20nm, L_{aux} = 30nm along horizontal cutline with V_{DS} = 1V and V_{GS} = 0V for different φ_{aux} .

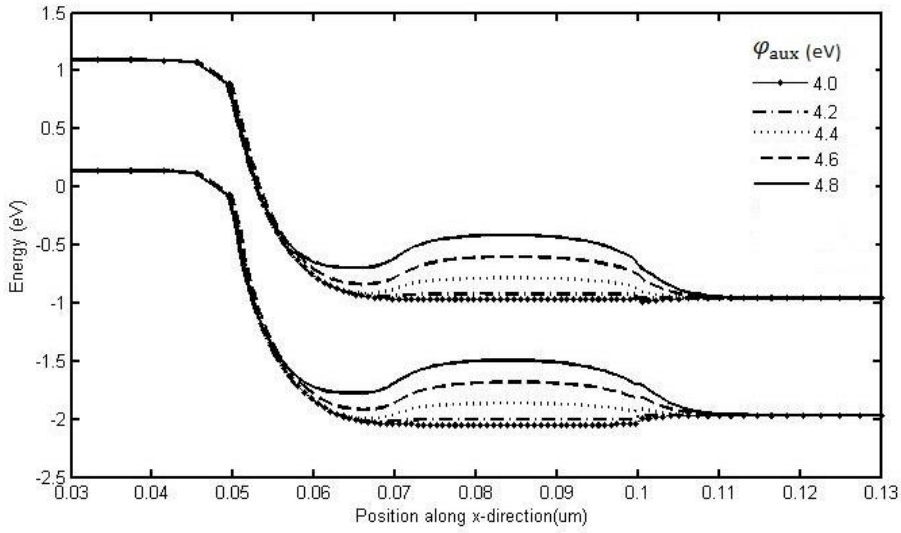


Fig.5.3.2: Band diagram along horizontal cutline for SD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0eV, L_{tunn} = 20 nm, L_{aux}=30nm in ON state with V_{DS} = 1V and V_{GS} = 2V for different φ_{aux}.

Fig. 5.3.2 shows the energy bands horizontally across the body of the device in the ON-state with a reverse bias (V_{DS}=1 V) applied across the p-i-n junction with gate voltage of 2V. To modulate band overlap between source and channel we fixed work function of tunnel gate φ_{tunn} at 4.0 and changes the work function of auxiliary gate φ_{aux} . From figure it is clear that electron will find it easy to flow from valance band of source to the conduction band of channel.

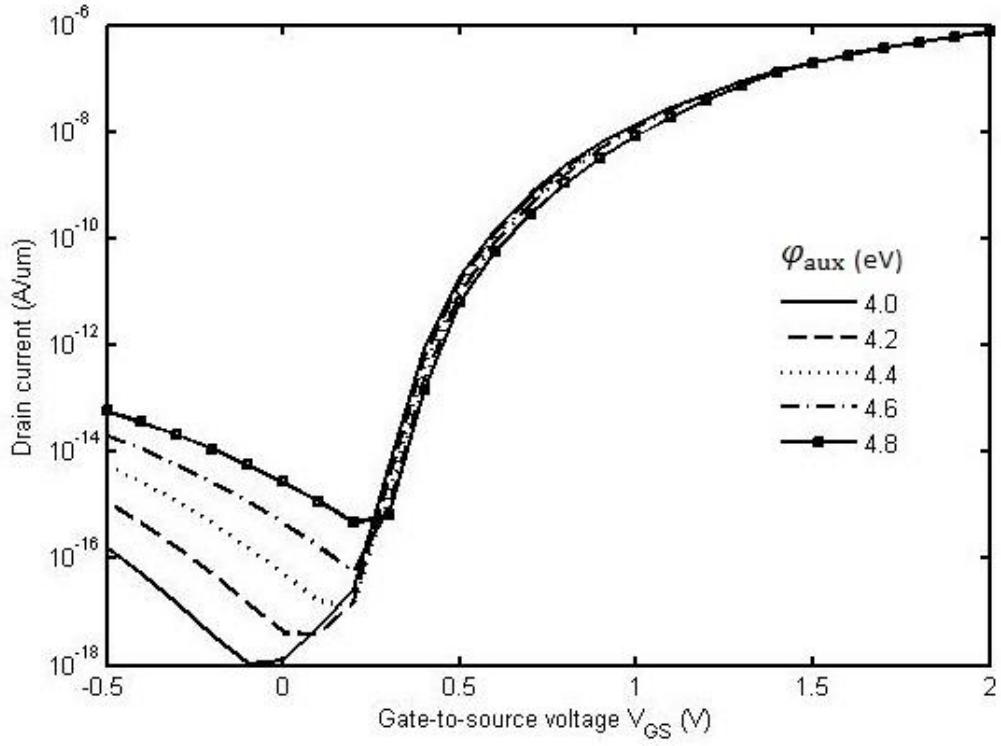


Fig. 5.3.3: Transfer characteristics for SD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, *Ltunn* = 20 nm, *Laux* = 30 nm with *VDS* = 1V for differentφ_{aux}.

Fig. 5.3.3. shows the transfer characteristics which depicts the result obtained from both above figures. As it is clear that leakage current is least for the $\varphi_{\text{aux}} = 4.0$ and it increases more rapidly as φ_{aux} increases and this result can be verify from figure. In figure 5.3.1 it's clear that the energy barrier for 4.0 is highest and lowest for 4.8 for auxiliary gate work function therefore more leakage current for 4.8 than 4.0. Now, in figure 4 I_{on} is highest for the $\varphi_{\text{aux}} = 4.0$ and lowest for $\varphi_{\text{aux}} = 4.8$. which can be explained from figure 3. In figure 5.3.2, ON-state of device the energy barrier for the $\varphi_{\text{aux}} = 4.0$ is lowest and it is highest for $\varphi_{\text{aux}} = 4.8$. Therefore we get lowest leakage current and highest on current for $\varphi_{\text{aux}} = 4.8$.

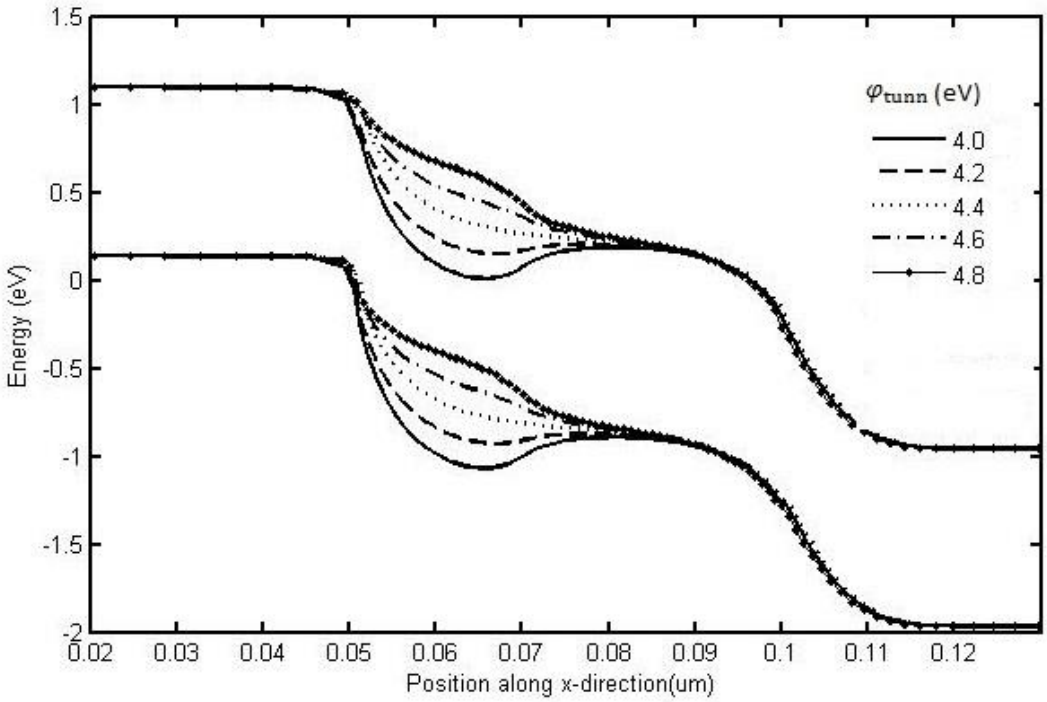


Fig.5.3.4: Band diagram along horizontal cutline for SD-DMG SiNT FET. Device parameter: φ_{aux} = 4.4eV, Ltunn = 20nm, Laux=30nm in OFF state with VDS=1V and VGS=0V for different φ_{tunn}.

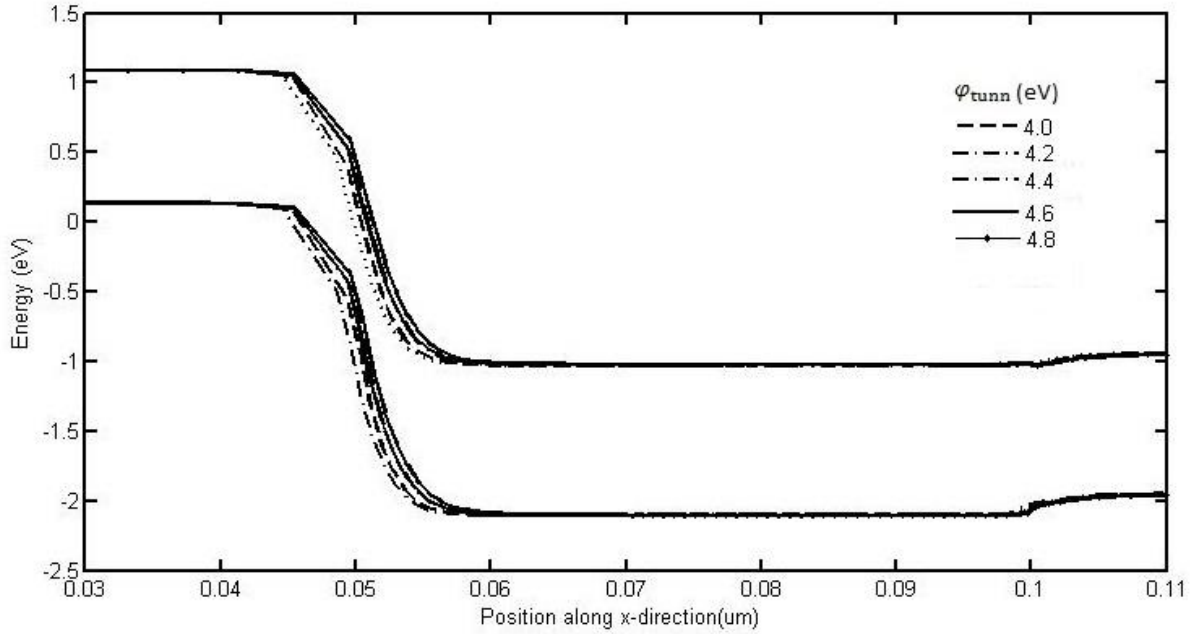


Fig.5.3.5: Band diagram along horizontal cutline for SD-DMG SiNT FET. Device parameter: φ_{aux}=4.4eV, *Ltunn* = 20nm, *Laux*=30 nm in ON state with *VDS* = 1V and *VGS* = 2 V for different φ_{tunn} .

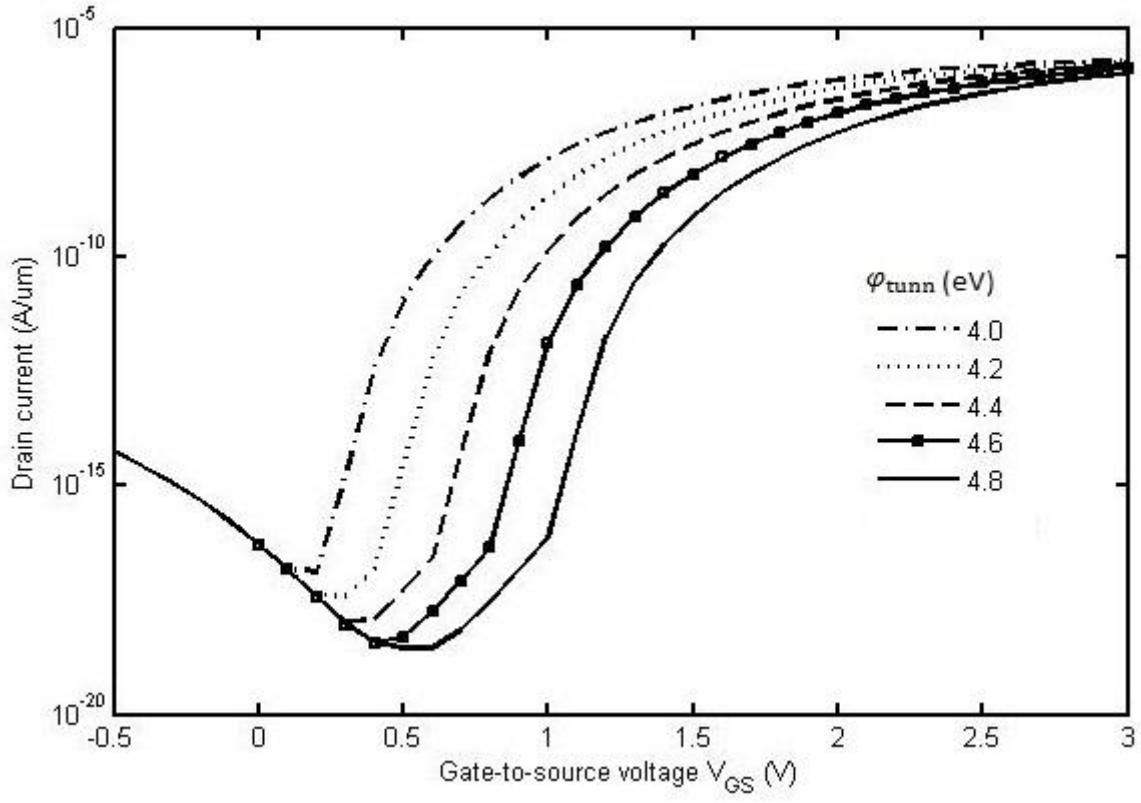


Fig.5.3.6: Transfer characteristics for SD-DMG SiNT FET. Device parameter: φ_{aux}=4.4eV,Ltunn=20nm,Laux=30nm with *VDS*=1V for different φ_{tunn} .

In figure 5.3.4 to 5.3.6 we have done same analysis but this time auxiliary gate work function is fixed at $\varphi_{aux} = 4.4eV$ and tunnel gate work function φ_{tunn} is varied. Since φ_{tunn} is changes from 4.0 to 4.8 and $\varphi_{aux} = 4.4eV$ is fixed therefore the tunnelling width will be high in all cases and there will be very less leakage current flows for all values of φ_{tunn}. It can be observe in figure 5.3.4, the energy barrier width is very high in all cases and therefore very less leakage current will flow. However in on-state $\varphi_{tunn} = 4.0$ gives least value for barrier height. Therefore maximum I_{on} will flow for $\varphi_{tunn} = 4.0$. Now the above mention discussion can be verified from figure 5.3.6.

In figure 5.3.6, which represent transfer characteristic of SD-DMG SiNT FET with varying tunnel gate work function, it's very clear that there is very less leakage current for all values of φ_{tunn} . Figure also shows that I_{on} is highest for $\varphi_{tunn} = 4.0$ which are the production from figure 5.3.4 and 5.3.5. Another interesting result which is shown by transfer characteristics of SD-DMG SINT FET that there is change in threshold voltages with the

change in tunnelling gate work function φ_{tunn}. Now for the optimum performance of device $\varphi_{\text{tunn}} = 4.0$ and $\varphi_{\text{aux}} = 4.4eV$ will be considered.

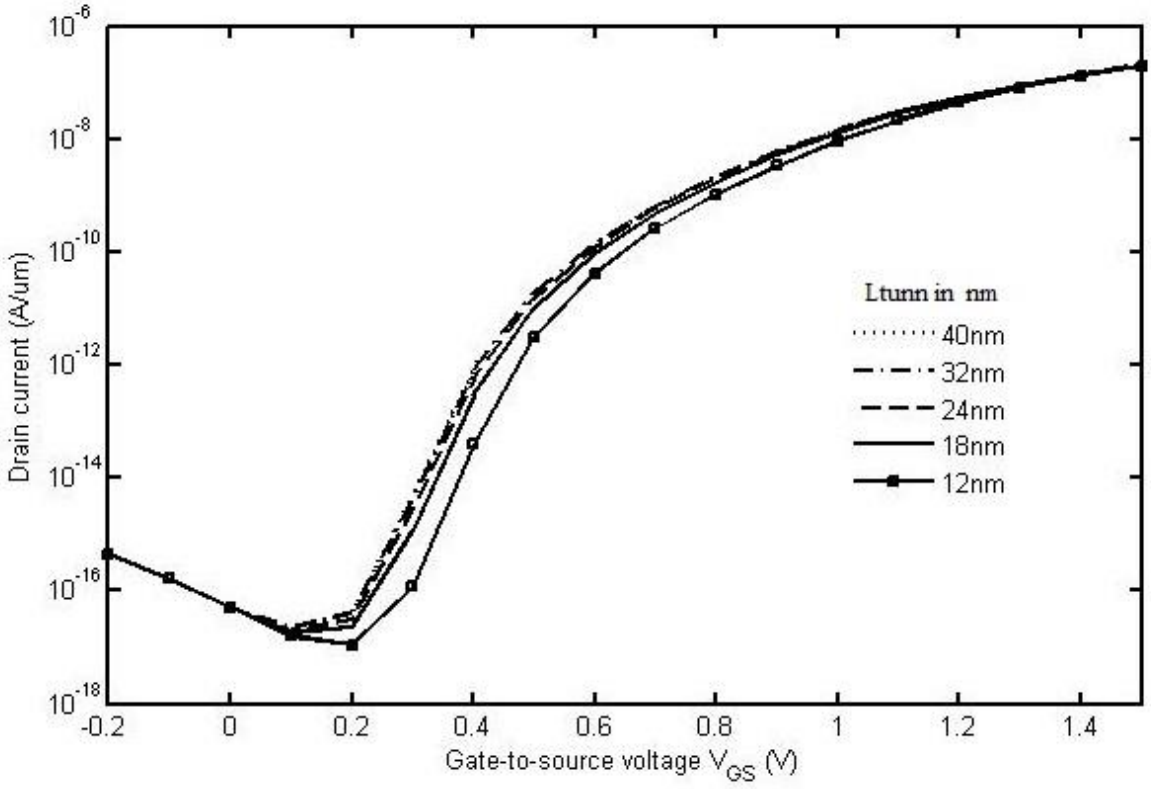


Fig.5.3.7: Transfer characteristics for SD-DMG SiNT FET. Device parameter: φ_{aux}=4.4eV, $\varphi_{\text{aux}} = 4.4eV$ with V_{DS}=1V for different Ltunn.

To check the effect of changing tunnelling length Ltunn on SD-DMG SiNT FET transfer characteristics simulation of device has been done in ATLAS. Figure 5.3.7 shows transfer characteristics for variation in tunnelling length. Ltunn is varied from 12nm to 40nm and it is found that there are slight changes in threshold voltages and very little change in Ion. Leakage current remains same in all cases. While changing from 12nm to 40nm there is reduction in threshold voltages. For Ltunn less than 20nm threshold voltage value is comparatively high and therefore we will consider Ltunn = 20nm for further investigation.

In figure 5.3.8 and 5.3.9 comparison between SD-DMG SiNT FET and SD-SMG SiNT FET has been done. For SD-SMG SiNT FET we have considered two work function for analysis $\varphi_{\text{m}} = 4.0\ and\ 4.4$. In figure 5.3.8 which represents transfer characteristics, shows that SD-DMG SiNT FET and SD-SMG SiNT FET for 4.0 work function has almost similar characteristics. While SD-DMG has lesser leakage current and higher threshold voltage compared to SD-SMG for 4.0 work function.

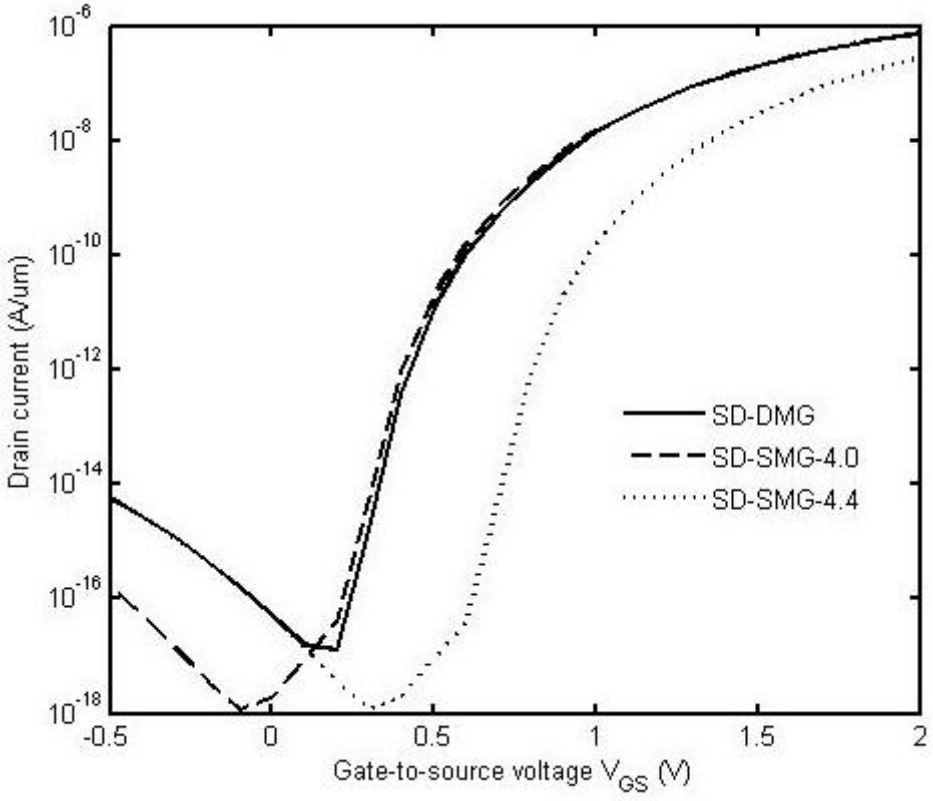


Fig.5.3.8: Transfer characteristics of the SD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and SD-SMG SiNT FET (φ_m = 4.0 eV, 4.4 eV, Lg= 50 nm) at V_{DS} = 1 V.

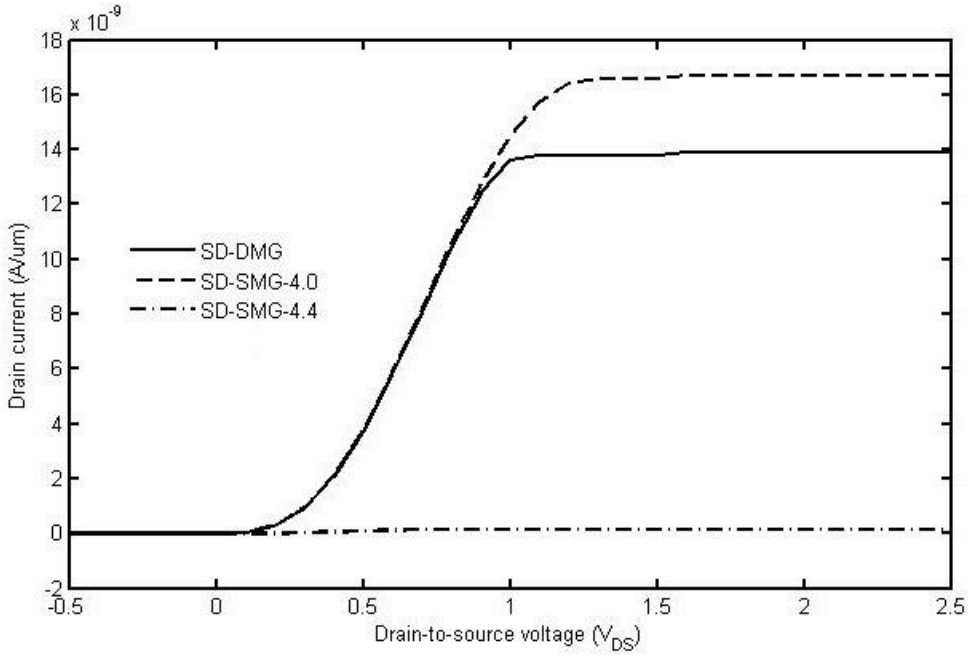


Fig.5.3.9: Output characteristics of the SD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and SD-SMG SiNT FET (φ_m = 4.0 eV, 4.4 eV, Lg= 50 nm) at V_{GS} = 1.8 V.

From figure 5.3.9 it is also clear that SD-SMG SiNT FET having 4.4 work function has lower Ion compared to SD-DMG. It also have higher threshold voltages and leakage current is comparative with SD-DMG. Figure 10 shows that SD-SMG-4.0 has higher Ion than SD-DMG but in case of SD-DMG output saturates at lesser drain voltages compared to SD-SMG-4.0. Also SD-DMG has higher Ion compared withSD-SMG-4.4. Therefore we can conclude that SD-DMG has better characteristics as its output current saturates slightly before SD-SMG-4.0 and it has moderate Ion.

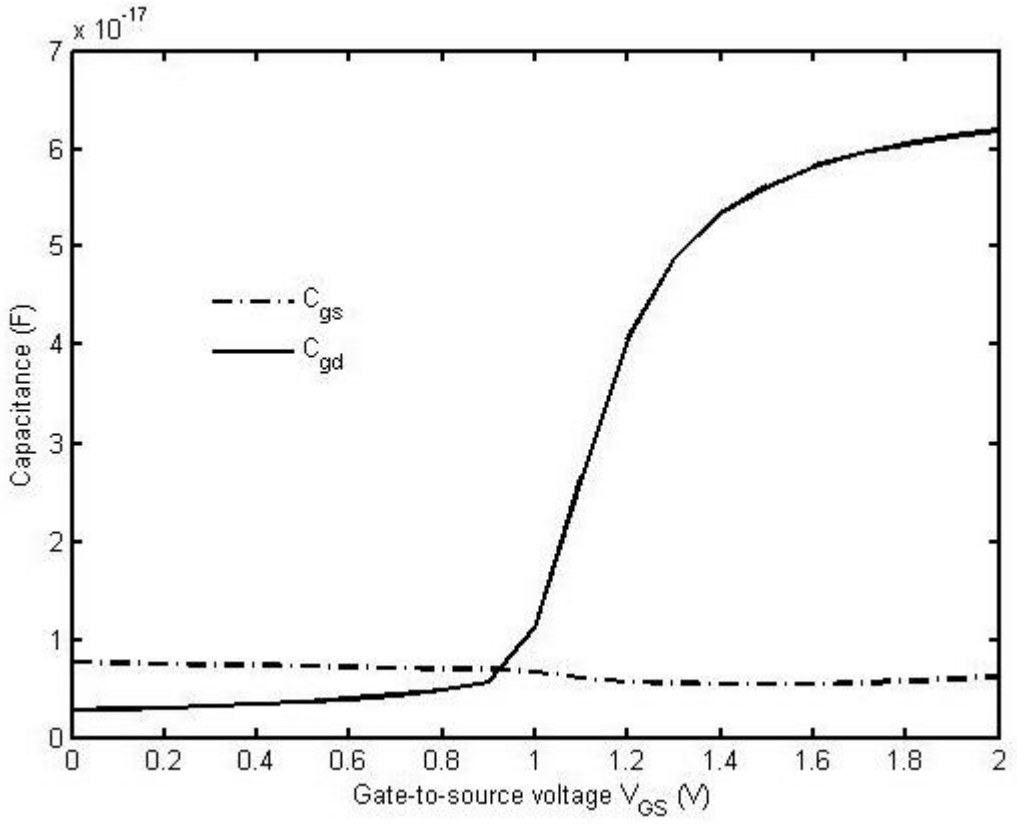


Fig5.3.10. Parasitic capacitances Cgs and Cgd as a function of VGS in SD-DMG SiNT FET. Device parameters: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, Ltunn = 20 nm, and Laux = 30 nm.

Intrinsic capacitance in SD-DMG SiNT FET has been determined so as to model its RF behaviour. Gate-to-source capacitance (Cgs) and gate-to-drain capacitance (Cgd) as a function of V_{GS} is shown in fig. 5.3.10. It can be seen that Cgd is the main factor influencing total gate capacitance (Cgg). Cgs decrease as V_{GS} is increased. Cgd shows a tremendous increase as V_{GS} is increased due to reduction of potential barrier at the drain side.

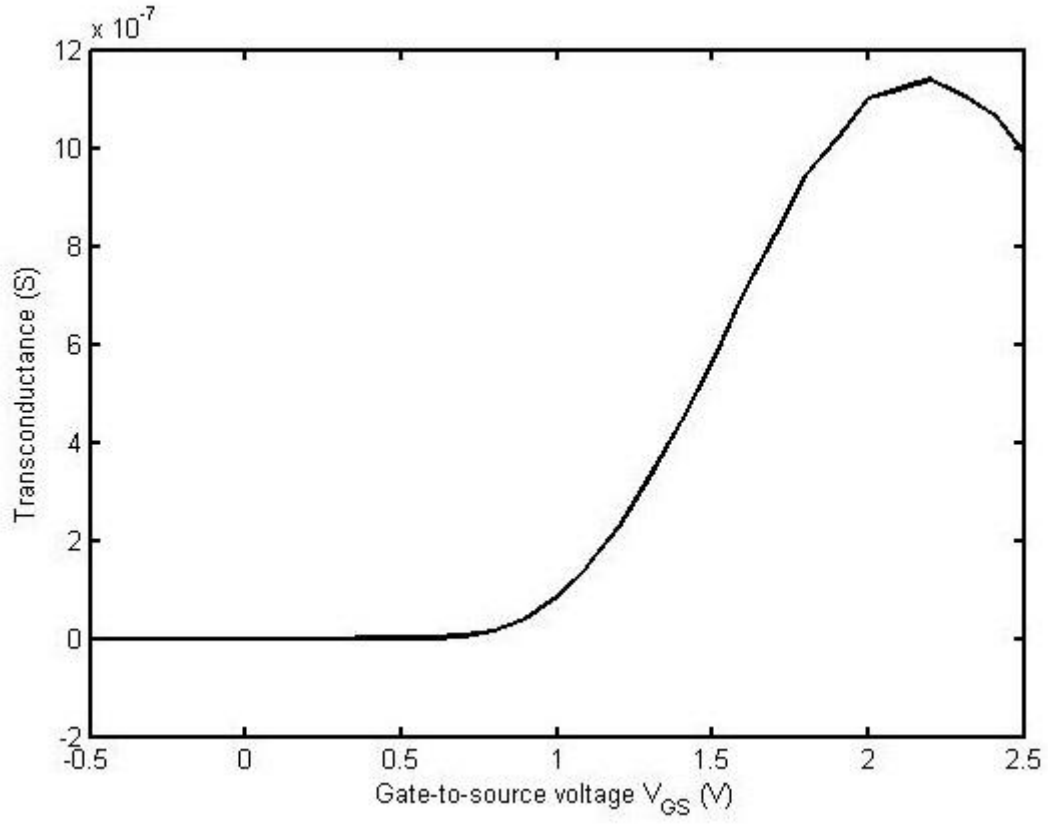


Fig. 5.3.11. Transconducatnce as a function of VGS in SD-DMG SiNT FET. Device parameters: tunn = 4.0 eV, aux = 4.4 eV, Ltunn = 20nm, and Laux = 30 nm.

Fig. 5.3.11 shows the variation of transconducatnce (g_m) with varying V_{GS} for SD-DMG SiNT FET. g_m is in the order of μS comparatively lesser than conventional MOSFET.

5.4 CONCLUSION

In this chapter we find that by changing the work function of tunnel as well as auxiliary gate we can get optimal control on electrostatic field over channel. Effect of change of work function over source and drain side over tunnelling current has been studied. SD-DMG SiNT FET can be optimized to give less leakage current and high on current. Threshold voltage of SD-DMG SiNT FET can be change by changing the work function of tunnelling gate. SD-DMG and SD-SMG has been compared and it is found that SD-DMG has a better transfer and output characteristics. Intrinsic capacitance and transconducatnce has been found and since drain current is low transconducatnce value is low compared to conventional MOSFETs.

CHAPTER 6

Performance analysis of hetero dielectric dual material gate Si-nanotube tunnel FET

6.1 INTRODUCTION

The demand of small size , low power consuming ,less leakage and low cost semiconductor devices has been increased to follow the ITRS bellow 22nm technology node. To reach technology nodes bellow 22nm, fallow moors law and ITRS scientist has been looking for non-conventional MOSFETS like dual gate MOSFET, trigate MOSFET, FIN FET, Gate-All-Around MOSFETs etc. because conventional MOSFET cannot reach such small size due to increase in leakage current. The current scenario required ultra-low-power devices and this employ reduction in the voltage supply $V_{dd.}$ Till now according to ITRS we has reduces Vdd by using theory of scaling to 0.9 and the projected target is 0.8 by 2015. But further reduction of Vdd is not possible by using scaling theory due to fundamental limit possess by current conduction in conventional MOSFET which thermionic by nature. Therefore subthreshold slope (SS) creates huddles for the further scaling of Vdd. This scaling limit on Vdd is due to kT/q factor value due to which the subthreshold slope cannot go below 60mV/dec[22-31].

To answer the challenge presented by subthreshold slope (SS), tunnelling devices like tunnel field effect transistors represents better and promising solution to construct low power devices. Because it is possible to achieve SS below 60 mV/dec. the transport of charge carrier in tunnelling device fallow quantum mechanical band-to-band-tunnelling BTBT instead of thermionic mechanism[22].

Now in previous chapter we had examined SD-DMG SiNT FET and we found that DMG has better property over SMG. Therefore in this chapter detailed analysis is done for hetero dielectric dual metal gate Si-nanotube MOSFET (HD-DMG SiNT FET). Transfer and output characteristics has been plotted for HD-DMG SiNT FET and it is also compared with hetero dielectric single metal gate Si-nanotube MOSFET (HD-SMG SiNT FET). Effect of change in work function on energy barrier over source side and drain side has been studied in detail and optimum values of work function for tunnelling as well as auxiliary gate is found. We also study the outcome of change in tunnelling channel length. To supress ambipolar nature high k dielectric has been used for tunnelling gate side and low k dielectric is used at drain side.

By using such combination of dielectric there is enhancement in I_{on}. Lastly RF characteristics like intrinsic capacitance and transconducatnce is found using ATLAS^{TM} from SILVACO.

6.2 DEVICE STRUCTURE

The structure of the device under consideration is shown in Fig.6.2.1 where p+-intrinsic-n+ silicon regions which form the source-channel-drain is shown it is the cross sectional view of HD-DMG SiNT FET. The structure has been simulated using ATLAS^{TM}, version 5.18.3.R. from Silvaco. Non local BTBT model along with band gap narrowing model have been incorporated in the simulation. In all our simulations, source-channel and drain-channel junctions are considered to be abrupt. The gate oxide spans is under auxiliary gate and Hfo_2 span over tunnelling gate.

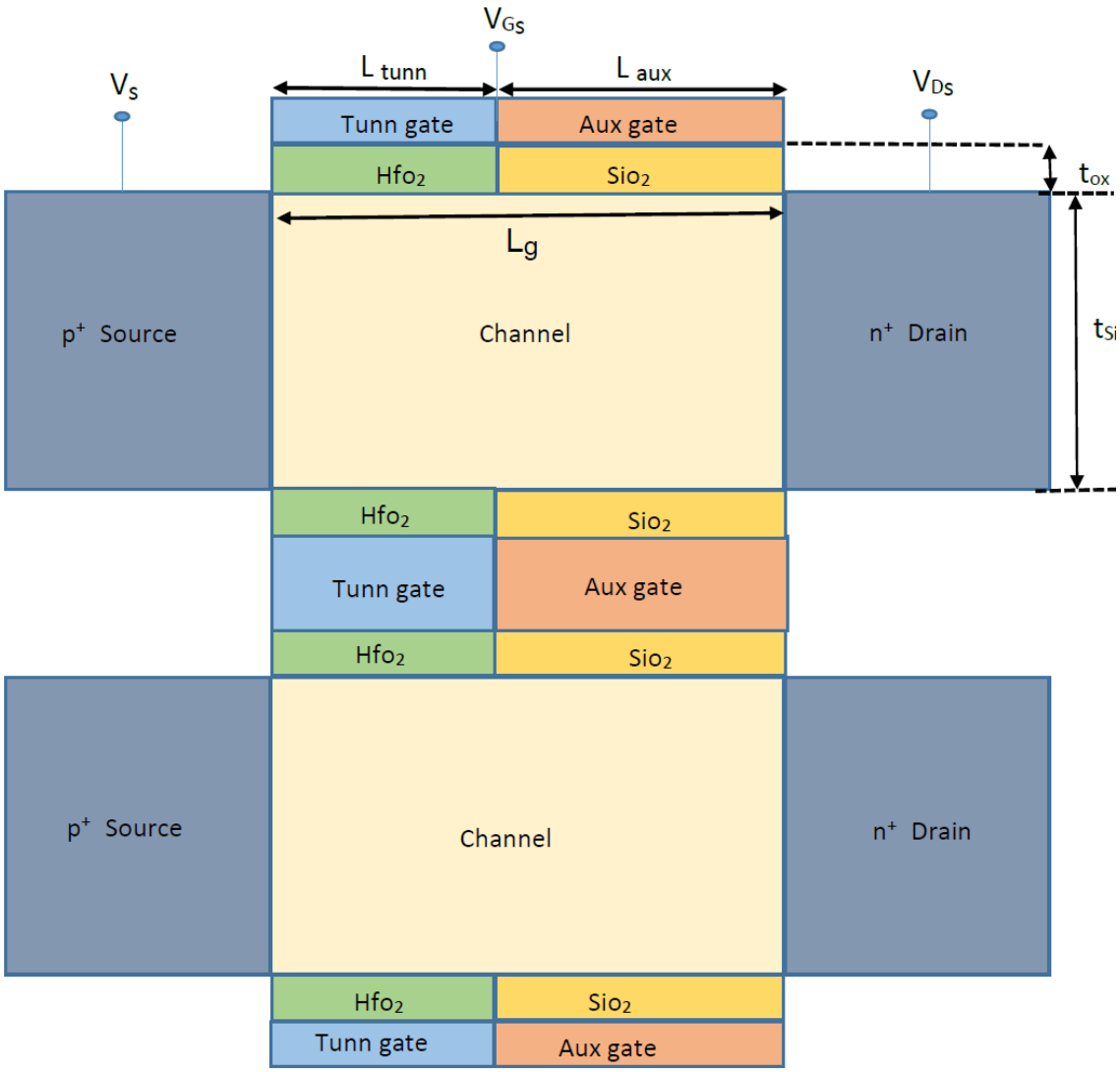


Fig.6.2.1.Cross sectional view of HD-DMG SiNT FET

Table 6.2.1: Device parameter taken for the simulation of device

Gate oxide thickness (t_{ox}) for both dielectrics	2nm
Total channel length (L_g)	50nm
Length of tunnel gate (L_{tunn})	20nm
Length of auxiliary gate (L_{aux})	30nm
Channel thickness (t_{si})	10nm
Source doping	1 x 10^{20} atoms/cm^3 p.type
Channel doping	1 x 10^{16} atoms/cm^3 p.type
Drain doping	5 x 10^{18} atoms/cm^3 n.type

As mentioned in table 6.2.1 the device under consideration has 50nm as total channel length, tunnel gate length is 20nm, auxiliary gate length 30nm. Channel thickness for HD-DMG is 10nm and oxide thickness for both dielectrics are 2nm. Source is doped with p+ 1 x 10^{20} atoms/cm^3 p.type, drain doping is n+ 5 x 10^{18} atoms/cm^3 n.type and channel is moderately doped at 1 x 10^{16} atoms/cm^3 p.type.

6.3 RESULT AND DISCUSSION

HD-DMG SiNT FET is actually a reverse biased p-i-n diode. Here tunnel device is n-type. Initially the barrier height between the sources-channel- drain is sufficiently high so that no current flows in off stage. But when we apply positive voltage to drain and channel after appropriate amount of voltage the energy barrier between valance band of source and conduction band of channel overlaps and thus tunnelling takes place. For better tunnelling behaviour high k dielectric is placed below tunnelling gate towards source side. High k also prevents oxide tunnelling. Now by changing the work function of both tunnelling as well as auxiliary gate modulation of band overlap can be achieved. Therefore we can have electrostatic control over channel.For the simulation we have fixed tunnelling gate work function $\varphi_{\text{tunn}} = 4.0$ and vary auxiliary gate work functionφ_{aux}. Fig.6.3.1 shows the energy bands horizontally across the body of the device in the OFF-state with a reverse bias (V_{DS}=1 V) applied across the p-i-n junction without any voltage at the gate.

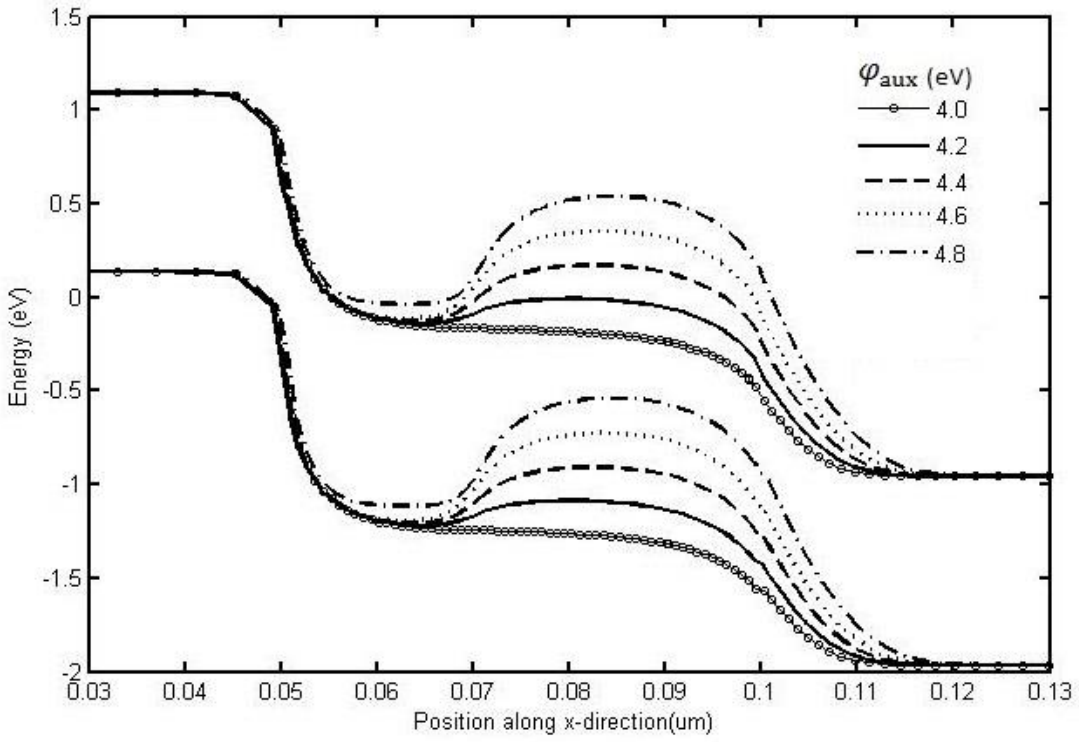


Fig.6.3.1: Schematic of energy band diagram for the OFF state in the HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0eV, L_{tunn} = 20nm, L_{aux} = 30nm along horizontal cutline with V_{DS} = 1V and V_{GS} = 0V for different φ_{aux}.

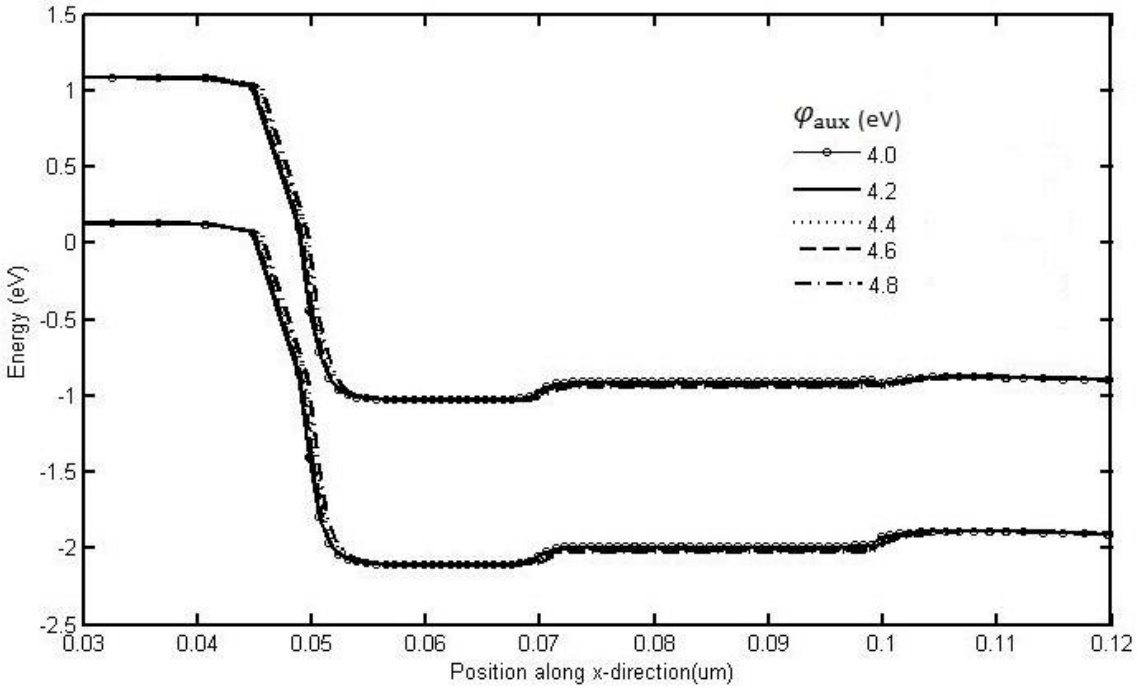


Fig.6.3.2: Band diagram along horizontal cutline for HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0eV, L_{tunn} = 20 nm, L_{aux}=30nm in ON state with V_{DS} = 1V and V_{GS} = 2V for different φ_{aux}.

To modulate band overlap between source and channel we fixed work function of tunnel gate φ_{tunn} at 4.0 and changes the work function of auxiliary gate φ_{aux} . The obtained result is shown in Fig. 6.3.1. It is clear from the plot that steepness for the $\varphi_{\text{aux}} = 4.0$ is highest and least for the $\varphi_{\text{aux}} = 4.8$. Therefore for higher value of φ_{aux} there will be very less amount of leakage current flow. And leakage current keeps on decreasing when φ_{aux} is increased from 4.0 to 4.8.

Fig. 6.3.2 shows the energy bands horizontally across the body of the device in the ON-state with a reverse bias (V_{DS}=1 V) applied across the p-i-n junction with gate voltage of 2V. To modulate band overlap between source and channel we fixed work function of tunnel gate φ_{tunn} at 4.0 and changes the work function of auxiliary gate φ_{aux} . From figure it is clear that electron will find it easy to flow from valance band of source to the conduction band of channel. After application of gate voltage.

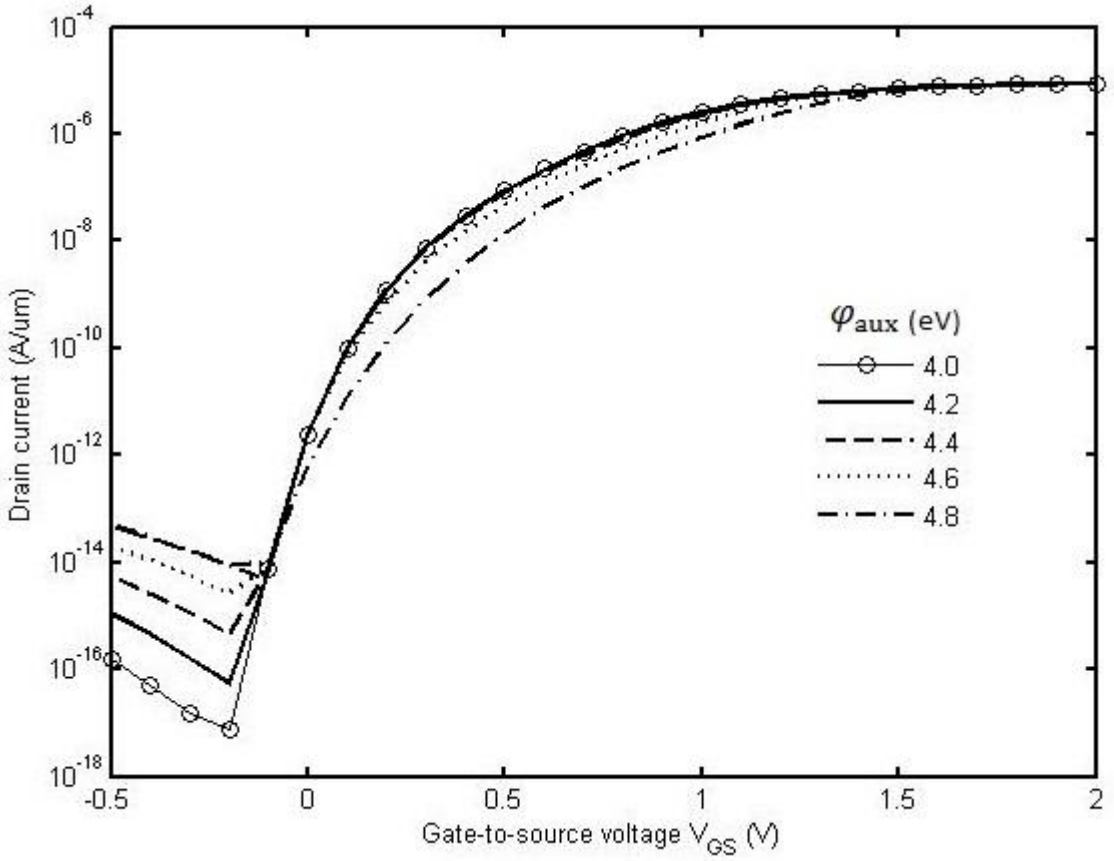


Fig. 6.3.3: Transfer characteristics for HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, *Ltunn* = 20 nm, *Laux* = 30 nm with *VDS* = 1V for differentφ_{aux}.

Fig. 6.3.3. shows the transfer characteristics which depicts the result obtained from both fig. 6.3.1 and fig. 6.3.2. As it is clear that leakage current is least for the $\varphi_{\text{aux}} = 4.0$ and it increases more rapidly as φ_{aux} increases and this result can be verify from figure. In figure 2 it's clear that the energy barrier for 4.0 is highest and lowest for 4.8 for auxiliary gate work function therefore more leakage current for 4.8 than 4.0. Now, in figure 6.3.3 I_{on} is highest for the $\varphi_{\text{aux}} = 4.0$ and lowest for $\varphi_{\text{aux}} = 4.8$.. In figure 6.3.2, ON-state of device the energy barrier for the $\varphi_{\text{aux}} = 4.0$ is lowest and it is highest for $\varphi_{\text{aux}} = 4.8$. Therefore we get lowest leakage current and highest on current for $\varphi_{\text{aux}} = 4.8$.

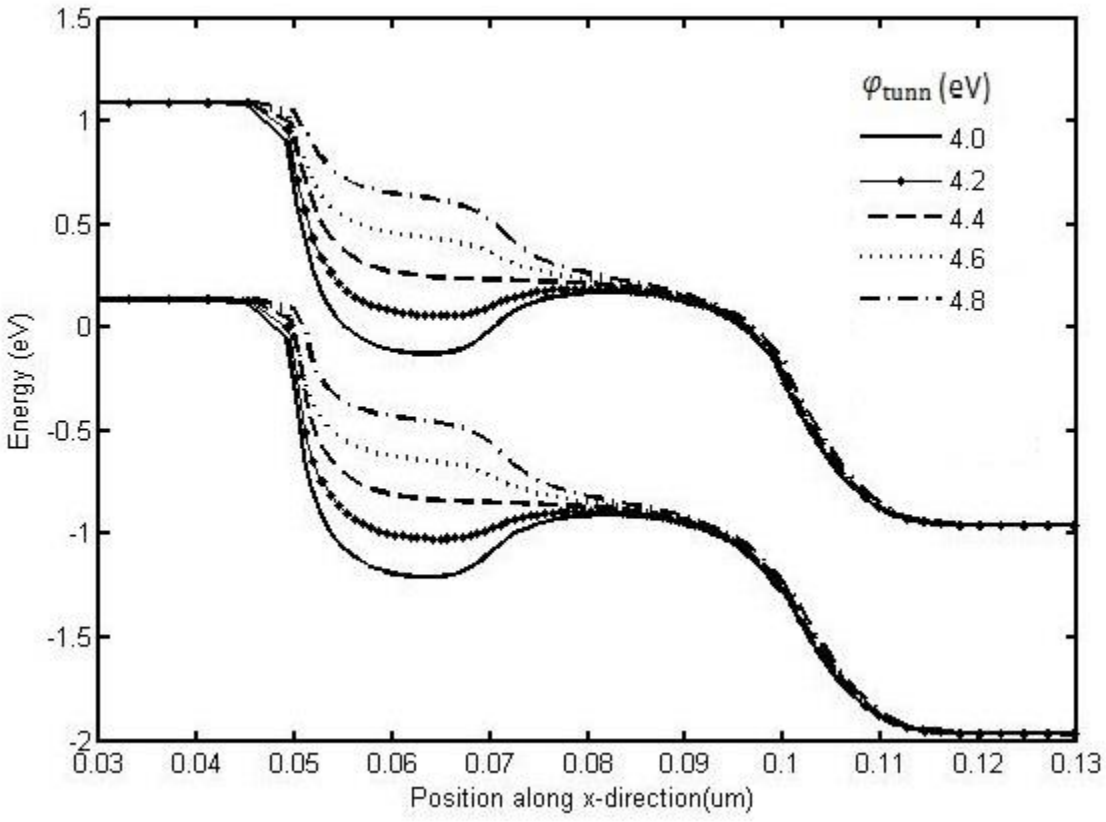


Fig.6.3.4: Band diagram along horizontal cutline for HD-DMG SiNT FET. Device parameter: φ_{aux} = 4.4eV, Ltunn = 20nm, Laux=30nm in OFF state with VDS=1V and VGS=0V for different φ_{tunn}.

In figure 6.3.4 and 6.3.5 we have done same analysis but this time auxiliary gate work function is fixed at $\varphi_{\text{aux}} = 4.4eV$ and tunnel gate work function φ_{tunn} is varied. Since φ_{tunn} is changes from 4.0 to 4.8 and $\varphi_{\text{aux}} = 4.4eV$ is fixed therefore the tunnelling width will be high in all cases and there will be very less leakage current flows for all values of φ_{tunn}.

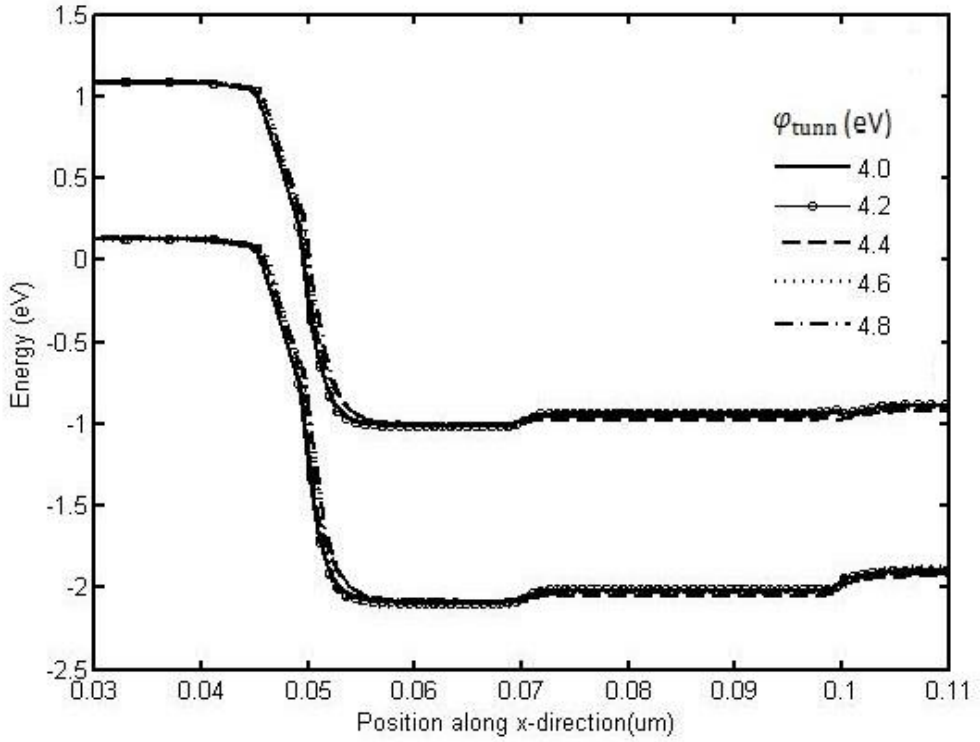


Fig.6.3.5: Band diagram along horizontal cutline for HD-DMG SiNT FET. Device parameter: φ_{aux}=4.4eV, *Ltunn* = 20nm, *Laux*=30 nm in ON state with *VDS* = 1V and *VGS* = 2 V for different φ_{tunn} .

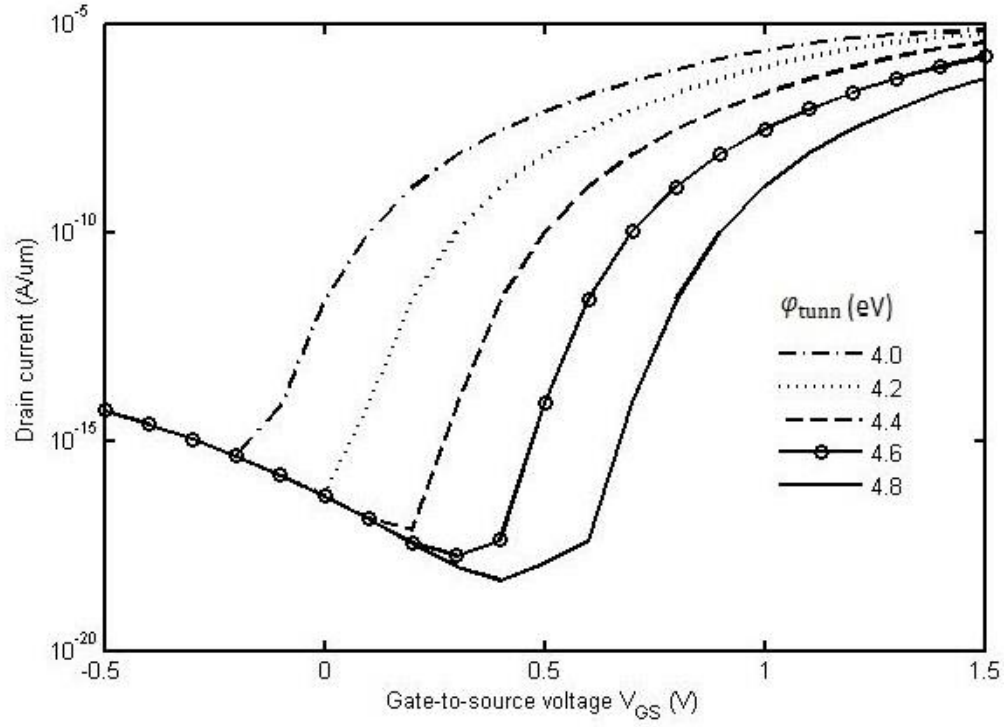


Fig.6.3.6: Transfer characteristics for HD-DMG SiNT FET. Device parameter: φ_{aux}=4.4eV,Ltunn=20nm,Laux=30nm with V_{DS}=1V for different φ_{tunn} .

It can be observe in figure 6.3.5, the energy barrier width is very high in all cases and therefore very less leakage current will flow. However in on-state $\varphi_{\text{tunn}} = 4.0$ gives least value for barrier height. Therefore maximum I_{on} will flow for$\varphi_{\text{tunn}} = 4.0$. Now the above mention discussion can be verified from figure 7.

In figure 6.3.6, which represent transfer characteristic of HD-DMG SiNT FET with varying tunnel gate work function, it's very clear that there is very less leakage current for all values ofφ_{tunn} . Figure also shows that I_{on} is highest for $\varphi_{\text{tunn}} = 4.0$ which are the production from figure 6.3.4and 6.3.5. Another interesting result which is shown by transfer characteristics of HD-DMG SINT FET that there is change in threshold voltages with the change in tunnelling gate work function φ_{tunn}. Now for the optimum performance of device $\varphi_{\text{tunn}} = 4.0$ and $\varphi_{\text{aux}} = 4.4eV$ will be considered.

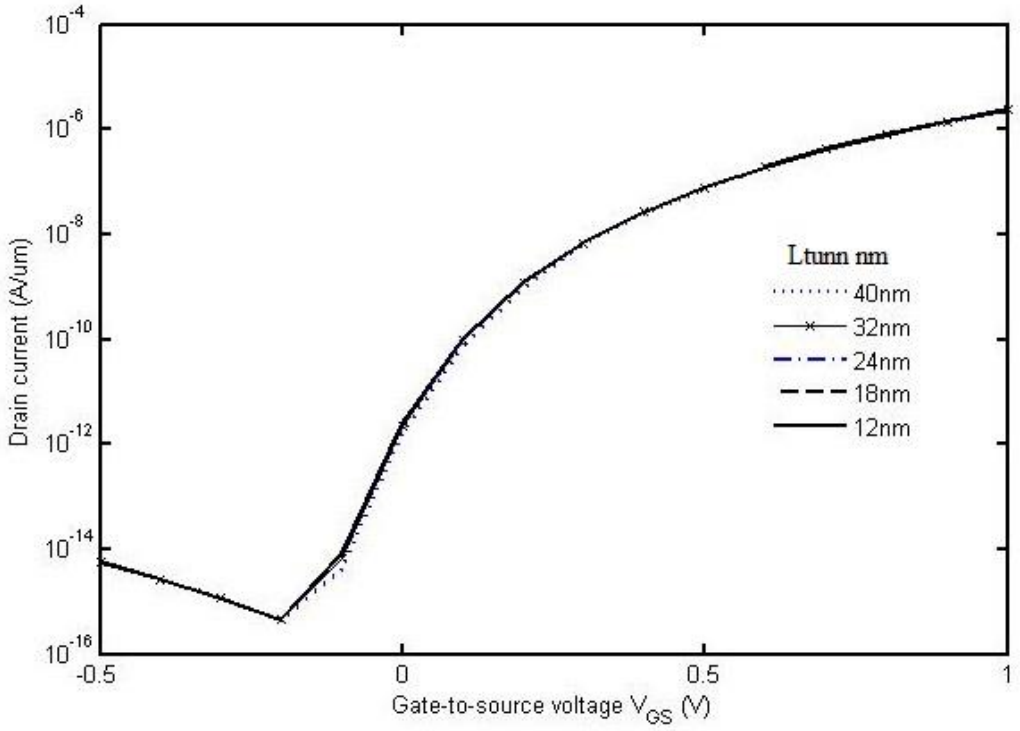


Fig.6.3.7: Transfer characteristics for HD-DMG SiNT FET. Device parameter: φ_{aux}=4.4eV, $\varphi_{\text{aux}} = 4.4eV$ with V_{DS}=1V for different Ltunn.

To check the effect of changing tunnelling length Ltunn on HD-DMG SiNT FET transfer characteristics simulation of device has been done in ATLAS. Figure 6.3.7shows transfer characteristics for variation in tunnelling length. Ltunn is varied from 12nm to 40nm and it is found that there are slight changes in threshold voltages and very little change in Ion. Leakage

current remains same in all cases. While changing from 12nm to 40nm there is reduction in threshold voltages. For Ltunn less than 20nm threshold voltage value is comparatively high and therefore we will consider Ltunn = 20nm for further investigation.

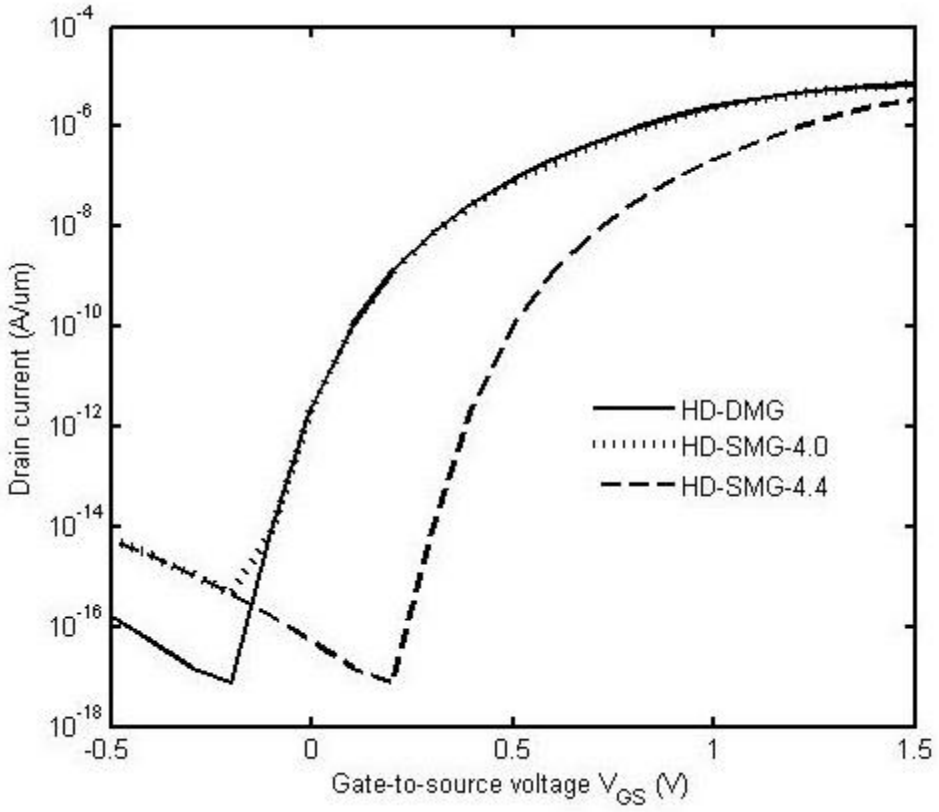


Fig.6.3.8: Transfer characteristics of the HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and HD-SMG SiNT FET (φ_m = 4.0 eV, 4.4 eV, *Lg*= 50 nm) at V_{DS} = 1 V.

In figure 6.3.8 and 6.3.9 comparison between HD-DMG SiNT FET and HD-SMG SiNT FET has been done. For HD-SMG SiNT FET we have considered two work function for analysis$\varphi_m = 4.0\ and\ 4.4$. In figure 6.3.8 which represents transfer characteristics, shows that HD-DMG SiNT FET and HD-SMG SiNT FET for 4.0 work function has almost similar characteristics. While HD-DMG has lesser leakage current and higher threshold voltage compared to HD-SMG for 4.0 work function.

From figure 6.3.8 it is also clear that HD-SMG SiNT FET having 4.4 work function has lower Ion compared to HD-DMG. It also have higher threshold voltages and leakage current is comparative with HD-DMG. Figure 6.3.9 shows that HD-SMG-4.0 has higher Ion than HD-DMG but in case of HD-DMG output saturates at lesser drain voltages compared to HD-SMG-4.0.

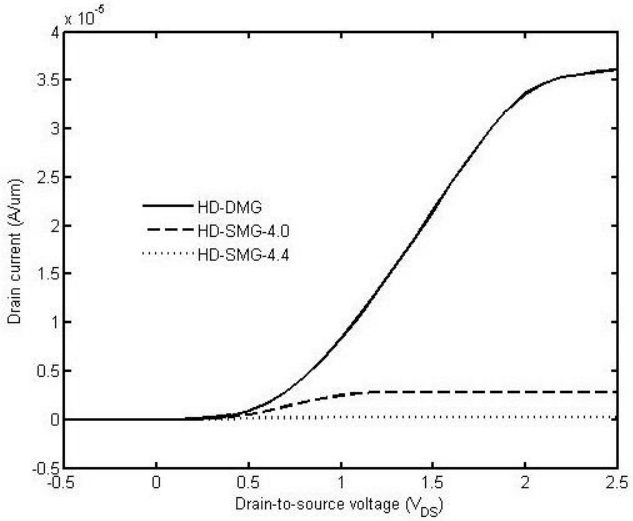


Fig.6.3.9: Output characteristics of the HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and HD-SMG SiNT FET (φ_m = 4.0 eV, 4.4 eV, *Lg*= 50 nm) at V_{GS} = 1.8 V.

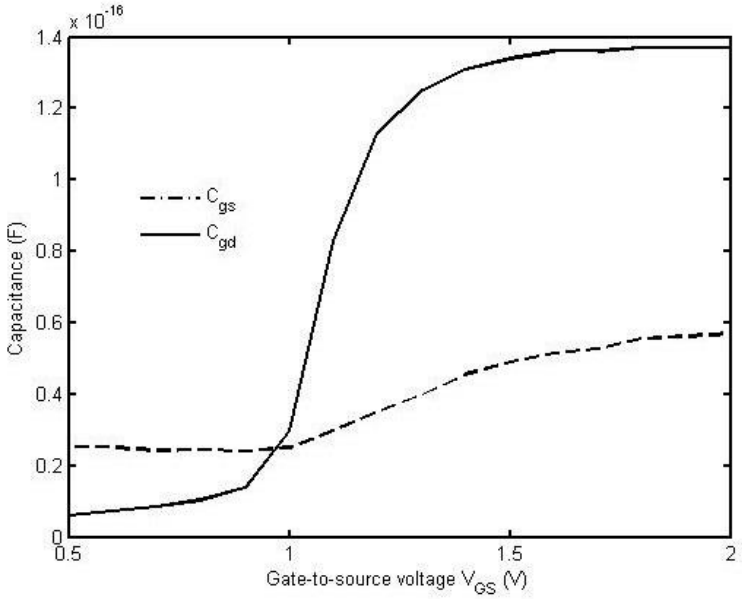


Fig6.3.10. Parasitic capacitances Cgs and Cgd as a function of VGS in HD-DMG SiNT FET. Device parameters: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, Ltunn = 20 nm, and Laux = 30 nm.

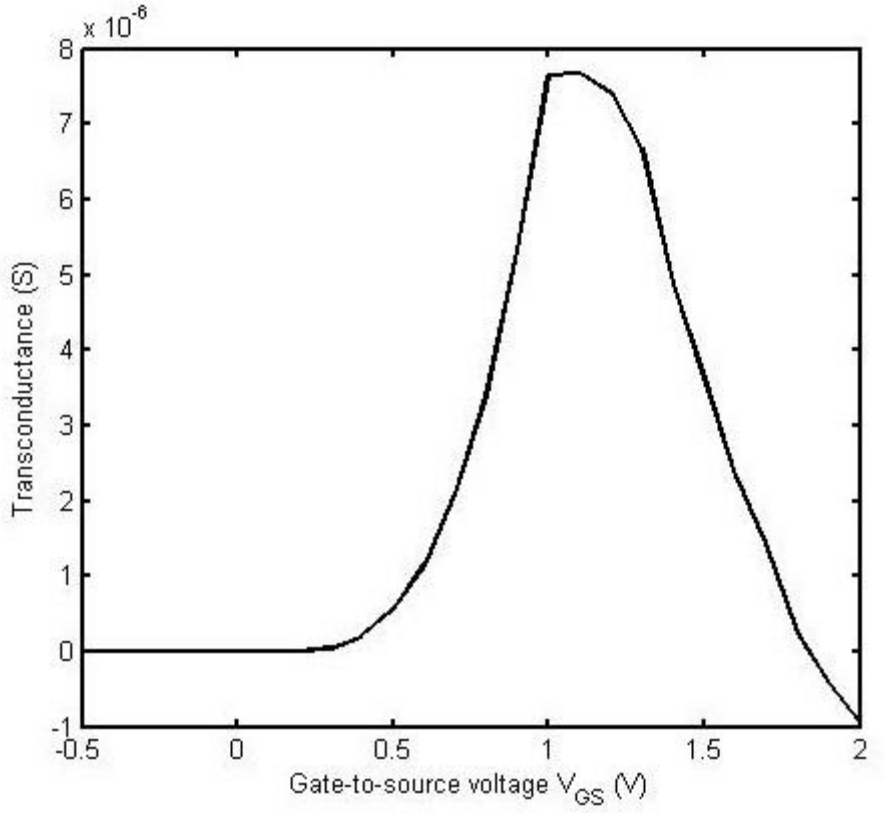


Fig. 6.3.11. Transconducatnce as a function of V_{GS} in HD-DMG SiNT FET. Device parameters: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, Ltunn = 20nm, and Laux = 30 nm.

Also HD-DMG has higher Ion compared with HD-SMG-4.4. Therefore we can conclude that HD-DMG has better characteristics as its output current saturates slightly before HD-SMG-4.0 and it has moderate Ion.

Intrinsic capacitance in HD-DMG SiNT FET has been determined so as to model its RF behaviour. Gate-to-source capacitance (Cgs) and gate-to-drain capacitance (Cgd) as a function of V_{GS} is shown in fig. 6.3.10. It can be seen that Cgd is the main factor influencing total gate capacitance (Cgg). Cgs decrease as V_{GS} is increased. Cgd shows a tremendous increase as V_{GS} is increased due to reduction of potential barrier at the drain side. Fig. 6.3.11 shows the variation of transconducatnce (g_m) with varying V_{GS} for HD-DMG SiNT FET. g_m is in the order of μS comparatively lesser than conventional MOSFET.

6.4 Advantages of HD-DMG over SD-DMG SiNT FET

6.4.1 Higher I_{on} and lower V_{th}

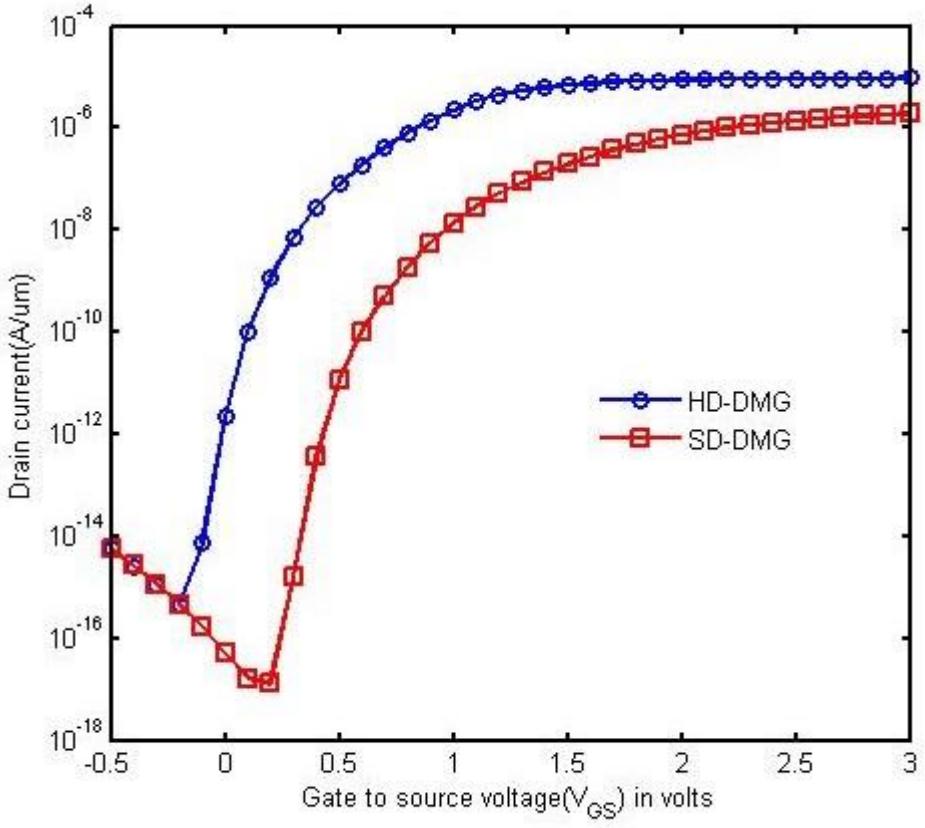


Fig 6.4.1. Transfer characteristics of HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30nm, Ɛox$_{tunn}$=25, Ɛox$_{aux}$=3.9. SD-DMG SiNT FET device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30 nm, Ɛox=3.9 at V_{DS} =1V.

Figure 6.4.1 shows the transfer characteristics of HD-DMG and SD-DMG for SiNT FET. It is clear from the graph that HD-DMG has better characteristics. It has higher on current compared to the SD-DMG and HD-DMG has lower threshold voltages. This lower threshold voltage attributed to the fact that higher k-dielectric has been use at the source channel junction below tunnelling gate. The presence of high-k dielectric will allow band-to band tunnelling to take place at lower voltage therefore HD-DMG has lower threshold value compared to SD-DMG SiNT FET.

6.4.2 Upgrading in output characteristic

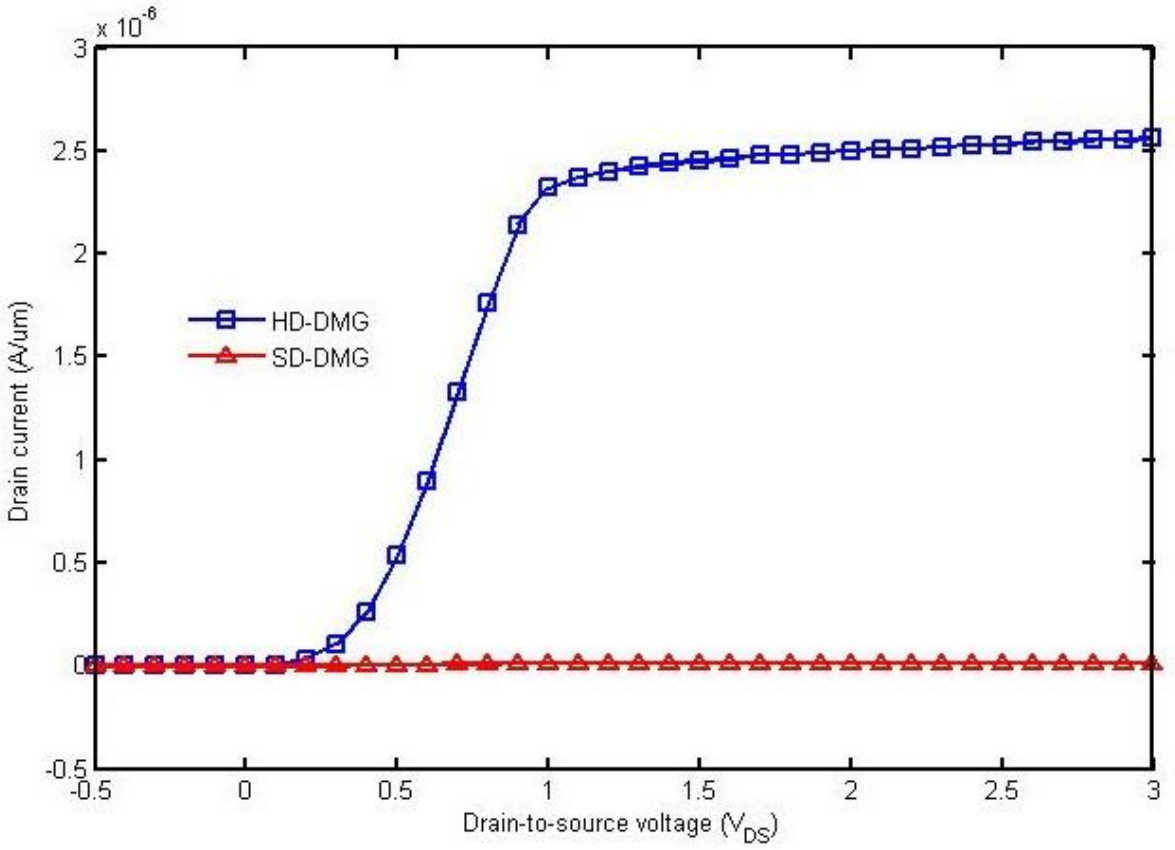


Fig 6.4.2. Output characteristics of HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30nm, Ɛox_{tunn}=25, Ɛox_{aux}=3.9. SD-DMG SiNT FET device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30 nm, Ɛox=3.9 at V_{GS} =1.8V.

The output characteristic shows the significance enhancement in the drain current for HD-DMG as compared to SD-DMG. The order of improvement is very high approximately 1000 time. This improvement is due to the fact that there is high-k dielectric is present below tunnelling gate near source and channel junction. The presence of high-k dielectric will allow band-to band tunnelling to take place at lower voltage which might be the reason for enhanced drain current for HD-DMG SiNT FET.

6.4.3 Intrinsic capacitance and transconducatnce comparison between HD-DMG and SD-DMG SiNT FET.

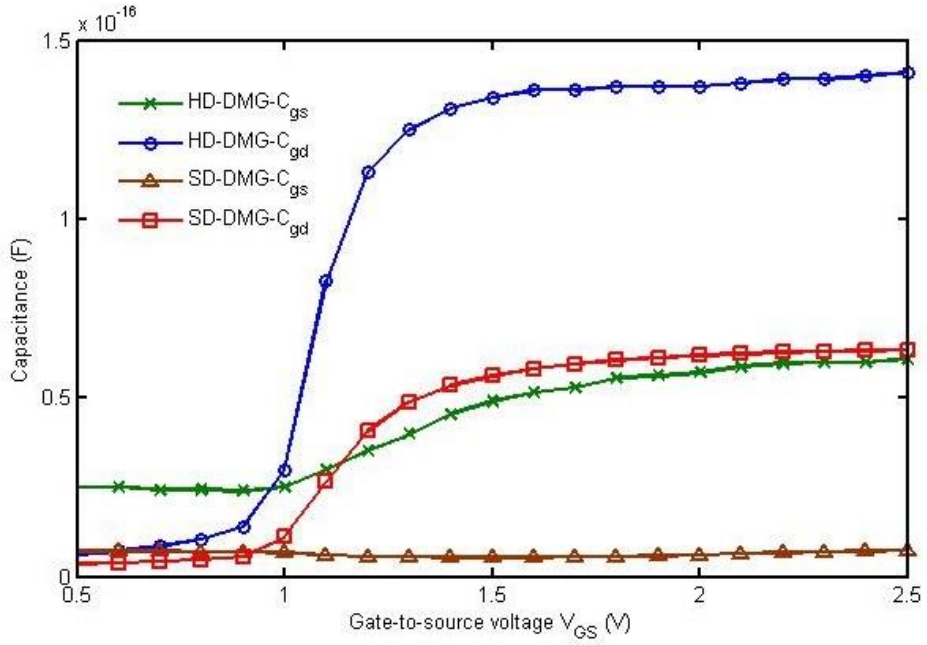


Fig **6.4.3**. Intrinsic capacitance of HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30nm, Ɛox$_{tunn}$=25, Ɛox$_{aux}$=3.9. SD-DMG SiNT FET device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30 nm, Ɛox=3.9 at V_{DS} =1V.

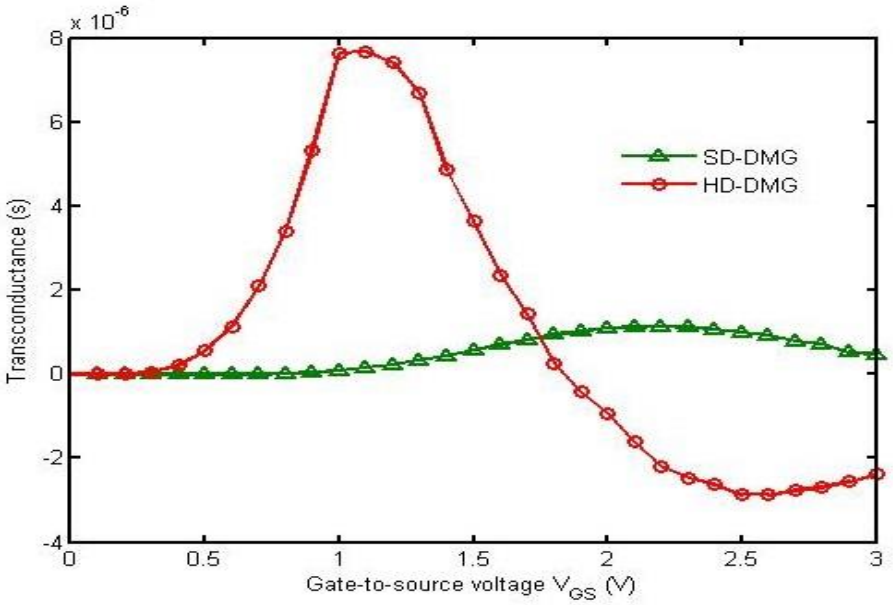


Fig **6.4.3**. Transconducatnce for HD-DMG SiNT FET. Device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30nm, Ɛox$_{tunn}$=25, Ɛox$_{aux}$=3.9. SD-DMG SiNT FET device parameter: φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, *L*tunn = 20 nm, *L*aux = 30 nm, Ɛox=3.9 at V_{DS} =1V.

Figure 6.4.3.1 shows the intrinsic capacitance comparison between HD-DMG SiNT FET and SD-DMG SiNT FET and it is clear from the plot that HD-DMG has higher intrinsic capacitance which are gate-to-source and gat-to-drain. Now this high value of intrinsic capacitance may be attributed to the fact that HD-DMG has high-k dielectric. Higher value of k also results in increase in tunnelling due to increase in gate voltage coupling.

Figure6.4.3.2 shows the transconducatnce cure which is plotted by varying the gate to source voltage and it is clear from this plot that HD-DMG has better transconducatnce value as compared with SD-DMG that will result in improved RF characteristics.

6.5 CONCLUSION

In this chapter we find that by changing the work function of tunnel as well as auxiliary gate we can get optimal control on electrostatic field over channel. Effect of change of work function over source and drain side over tunnelling current has been studied. HD-DMG SiNT FET can be optimized to give less leakage current and high on current. Threshold voltage of HD-DMG SiNT FET can be change by changing the work function of tunnelling gate. HD-DMG and HD-SMG has been compared and it is found that HD-DMG has a better transfer and output characteristics. Intrinsic capacitance and transconducatnce has been found and since drain current is low transconducatnce value is low compared to conventional MOSFETs. Finally the comparisons between HD-DMG SiNT FET and SD-DMG SiNT FET shows that HD-DMG SiNT FET has better performance.

CHAPTER 7

Conclusion

7.1 Overall conclusion

The presented analog and RF performance study in chapter 3 shows that the SiNT FETs can be used in more demanding situation. SiNT FETs offer high drive current and can be considered for high frequency circuit design because of relatively higher f_T and f_{MAX} parameters value, compared to GAA MOSFETs. Thus, SiNT FETs with excellent digital, analog and RF performance are the most worthy candidates for system-on-chip (SoC) design.

In chapter 4 it is found that Si-nanotube MOSFETs (SiNT FET) with catalytic metal gates can be used for gas sensing applications. P-channel SiNT FET with palladium (Pd) metal gate is proposed for hydrogen sensing, whereas N-channel SiNT FET with silver (Ag) metal gate can be used for oxygen gas sensing. A simulation based study using ATLAS-3D numerical simulator shows that SiNT FETs have more efficiency towards the hydrogen and oxygen detection than the recently proposed cylindrical gate-all-around (GAA) MOSFETs.

We also find in chapter 5 and 6 that by changing the work function of tunnel as well as auxiliary gate we can get optimal control on electrostatic field over channel. Effect of change of work function over source and drain side over tunnelling current has been studied. SD-DMG SiNT FET can be optimized to give less leakage current and high on current. Threshold voltage of SD-DMG SiNT FET can be change by changing the work function of tunnelling gate. SD-DMG and SD-SMG has been compared and it is found that SD-DMG has a better transfer and output characteristics. Intrinsic capacitance and transconducatnce has been found and since drain current is low transconducatnce value is low compared to conventional MOSFETs.

In chapter 6 we find that by changing the work function of tunnel as well as auxiliary gate we can get optimal control on electrostatic field over channel. Effect of change of work function

over source and drain side over tunnelling current has been studied. HD-DMG SiNT FET can be optimized to give less leakage current and high on current. Threshold voltage of HD-DMG SiNT FET can be change by changing the work function of tunnelling gate. HD-DMG and HD-SMG has been compared and it is found that HD-DMG has a better transfer and output characteristics. Intrinsic capacitance and transconducatnce has been found and since drain current is low transconducatnce value is low compared to conventional MOSFETs. Finally the comparisons between HD-DMG SiNT FET and SD-DMG SiNT FET shows that HD-DMG SiNT FET has better performance.

Therefore above conclusions prove that SiNT FET is a very promising device for IC integration for short channels devices.

BIBLIOGRAPHY

[1] Yuhua Cheng, Chenming Hu, “MOSFET classification and operation". *MOSFET modeling & BSIM3 user's guide*. Springer. pp. 13. 1999

[2] http://en.wikipedia.org/wiki/MOSFET

[3] U.A.Bakshi, A.P.Godse, “The depletion mode MOSFET”, *Electronic Circuits*. Technical Publications. pp. 8–12, 2007

[4] H. Yan, H S. Choe, S. Nam, Y. Hu, S. Das, J. F. Klemic, J. C. Ellenbogen and C. M. Lieber, “Programmable nanowire circuits for nanoprocessors”, *Lett. Nature*, vol. 470, pp. 240-244, issue 7333, (2011).

[5] M. Li, et al. “Sub-10 nm Gate-All-Around CMOS Nanowire Transistors on Bulk Si Substrate”, Symp. *VLSI Technol., IEEE*, pp. 94–95, (2009).

[6] B. D. Gates, “Nanowires find their place”, *Nature Nanotechnol.*, vol 5, pp. 484–485, (2010).

[7] H. M. Fahad & M. M. Hussain, “Are Nanotube Architectures More Advantageous Than Nanowire Architectures for Field Effect Transistors? “, *Report Sci.*, 2, 475, (2012).

[8] D. Tekleab, “Device Performance of Silicon Nano Tube Field Effect Transistors”, *Electron Dev Letter, IEEE*, vol 35, 5, pp.506-508, (2014).

[9] H. M. Fahad, C. E. Smith, , J. P. Rojas & H. M. Fahad, C. E. Smith, J. P. Rojas & M. M. Hussain, “Silicon Nanotube Field Effect Transistor with Core-Shell Gate Stacks for Enhanced High-Performance Operation and Area Scaling Benefits.”, *Lett., Nano, vol* 11, 4393–4399 (2011).

[10] D. Tekleab, H. H. Tran, J. W. Slight *et al.*, "Silicon nanotube MOSFET," U.S. Patent 0 217 468, Aug. 30 (2012).

[12] ATLAS, A 3D device simulator from SILVACO, Singapore 2014.

[13] N. M. Kumar, B. Sayamal, and C. K. Sarkar, "Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs", Electron Device IEEE. Vol. 57, p820-826, (2010).

[14] R. Gautam, M. Saxena, and R. S. Gupta," Gate-All-Around Nanowire MOSFET With Catalytic Metal Gate For Gas Sensing Applications," IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 12, NO. 6, NOVEMBER 2013.

[15] I. Lundstrom,M. Armgarth, A. Spetz, and F.Winquist, "Gas sensors based on catalytic metal-gate field-effect devices," *Sens. Actuators*, vol. 10,pp. 399–421, Nov. 1986.

[16] K. Tsukada, D. Kiriake, K. Sakai, and T. Kiwa, "Silver gate field effect transistor for oxygen gas sensor," in *Proc. 2nd Int. Conf. Sens. DeviceTechnol. Appl.*, French Riviera, France, Aug. 21–27, 2011, pp. 5–7.

[17] K. Tsukada, M. Kariya, T. Yamaguchi, T. Kiwa, H. Yamada, T. Maehara,T. Yamamoto, and S. Kunitsugu, "Dual gate field effect transistor hydrogen gas sensor with thermal compensation," *Jpn. J. Appl. Phys.*, vol. 49,pp. 024206-1–024206-5, 2010.

[18] Raymond Woo , "Band-to-band Tunneling Transistor Scaling and Design for Low Power Applications", Doctoral Thesis,Department of electrical engg,Stanford University,2009.

[19] James Towfik Teherani, "Band to Band Tunneling in Silicon Diodes and Tunnel Transistors",M.S Thesis,Massachussets Institute of Technology,June 2010

[20] Alan Seabaugh, The Tunneling Transistor,IEEE Spectrum, 30 Sep 2013

[21] Rakhi Narang et al, “Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling”, JOURNAL OFSEMICONDUCTOR TECHNOLOGY ANDSCIENCE, VOL.12, NO.4, DECEMBER, 2012

[22] Peter Matheu, “Investigations of Tunneling for Field Effect Transistors”,Doctoral Thesis, University of California, Berkeley, 2012

[23] Kathy Boucart and Adrian Mihai Ionescu, **“**Double-Gate Tunnel FET With High-K Gate Dielectric”, IEEE Transactions on Electron Devices, VOL 54, NO 7, July 2007.