A Novel Design for Dual Edge Triggered Flip-Flop for High Speed Low Power Application

by

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DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING
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This is to certify that the work in the thesis entitled "**A novel design of low power and high speed dual edge triggered flip-flop"** by **Chandan Maurya** is a record of an original research work carried out by him during 2014 - 2015 under my supervision and guidance in partial fulfilment of the requirements for the award of the degree of Master of Technology in Electronics and Communication Engineering (VLSI Design & Embedded System), National Institute of Technology, Rourkela. Neither this thesis nor any part of it, to the best of my knowledge, has been submitted for any degree or diploma elsewhere.

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Chandan Maurya

28th May 2015

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ABSTRACT

In area of low power VLSI, switching activity of circuit node is of great concerned to reduce dynamic power. Dynamic power is directly proportional to switching activity of nodes. Switching activity vary according to input data pattern thereby for different input data sequence different power dissipation can occur. To achieve same data throughput as in single edged triggered flip-flop (SETFF), dual edged triggered flip-flop (DETFF) is an effective way to decrease power dissipation. DETFF reduces switching activity for same data throughput. In this paper, two different design of DETFF are investigated. The technique used to design DETFF is to generate pulse at every edge of clock to trigger data and/or latch stage of circuit. A conventional and a proposed design of DETFF are surveyed. Proposed DETFF utilized different scheme to generate pulse at every edge of clock. In view of power dissipation there is no considerable improvement but delay has been greatly reduced thereby overall PDP with respect to conventional DETFF

MOTIVATION

Power consumption is as important as performance of VLSI circuits. Battery operated electronics devices are the largest source of wealth for electronics industries. Sequential circuits, finite state machine etc. are the most important part of VLSI circuits. And flip-flops are widely used in such circuits, 30 to 40 % of total power in VLSI circuits are consumed by flip-flops. So to reduce power consumption of circuits flip-flops pull the considerable attention. Most effective way to reduce power is to reduce supply voltage (voltage scaling). But supply voltage cannot be reduced after a certain level because reducing supply voltage can change device working region of operation and also increase delay of operation. Since oxide thickness is reducing with growing technology so voltage must be scale down to save the device from tunnelling and other factors (i.e. DIBL) as discussed in book [23]. Technology have their own limitation, gate length cannot be reduced too much in case of typical MOS otherwise it is very hard to off the MOS for too much small gate length and this is not desirable for digital operation. Many of power reduction technique discussed in [9, 16]. There are several method for PDP optimization [1,14,15,17]. In this thesis, PDP is optimized at circuit level technique. However to optimize the device fully, one must consider optimization at each level. Static power dissipation increase with advanced technology however in case of dynamic power dissipation it's not true.

Literature survey:

- Z Chen, M Johnson, L Wei, and K Roy [25]

Reduction of leakage current using transistor stacking discussed in this paper. In this paper it is described that because of stacking subthreshold current reduces greatly, DIBL effect also reduces that causes further reduction in subthreshold leakage.

- Koichi Nose, Masayuki Hirabayashi, Hiroshi Kawaguchi, Seongsoo Lee, and Takayasu Sakurai [23]

V_{th} hopping is a circuit technique that is used to reduce subthreshold current. A control signal which is sent from a software, guided the voltage supply connected to the body of MOS device that results low v_{th} or high v_{th} required for different operation.

- W.M. Chung, T. Lo, and M. Sachdev [1]

This paper concludes the comparison of different of dual edge triggered flip-flop (DETFF). A detailed description of different DETFF and their comparison give the best DETFF for digital operation.

- A.G.M. Strollo and D. De Caro [5]

Clock gating is a circuit technique used to reduce power consumption of circuit. Clock gating helps to avoid unnecessary switching of circuit node. In this paper it is described that when the input of D-FF is same as the output then a small circuit scheme is used to control the clock of D-FF that control the triggering of D-FF.

- N. Nedovic, M. Aleksic, and V.G. Oklobdzija [11]

Clock time period is very crucial to any sequential circuit. Similarly term setup time and hold time is time limit for input data. Clock period must be greater than propagation delay of device, there are more specification about clock period and data time limitation discussed in this paper.

- For further reading about different type of low power design, low power circuit analysis, timing specifications of CMOS digital circuit following books as given in reference **[9,10,12,13,16,21,23]** can be used.

CONTENT

LIST OF FIGURES

Chapter 1:
Introduction

1.1 *REVIEW OF D FLIP-FLOP*:-

Flip-flop (FF) being a storage element occupies a significant space in digital circuit design such as register, counter and finite state machine. In view of its huge applications, it is important to understand its operation in details obtaining a high level of insight into its various performance metrics such as speed, power dissipation, hold-time, set-up time and area. Thus, there is a significant research effort on FF which revealed various techniques for its performance improvement and optimization [2, 3, 4, 5, 6].

There can be various type of FF, each having advantage/disadvantage over one another. D-FF is among commonly used FFs because of its relatively simple operation. It can be either of static or dynamic type as shown in Fig.1.1.(A) and Fig.1.1.(B) In static flip-flop output data is stored using latch whereas in dynamic flip-flop output is stored by using the node capacitance and thus it needs clock pulse at regular interval to preserve data at appropriate logic level. Static type flip-flop usually utilizes more transistor than dynamic type. Glitches and charge sharing are two drawbacks that happens in dynamic type D-FF, resulting in a different state of the circuit node voltage.

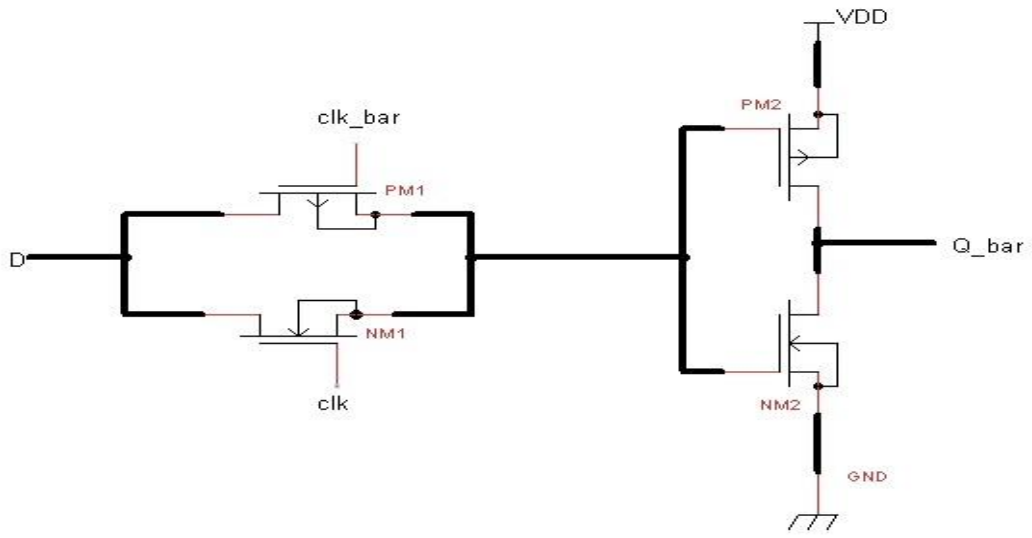


Fig 1.1.(A) Dynamic D-FF

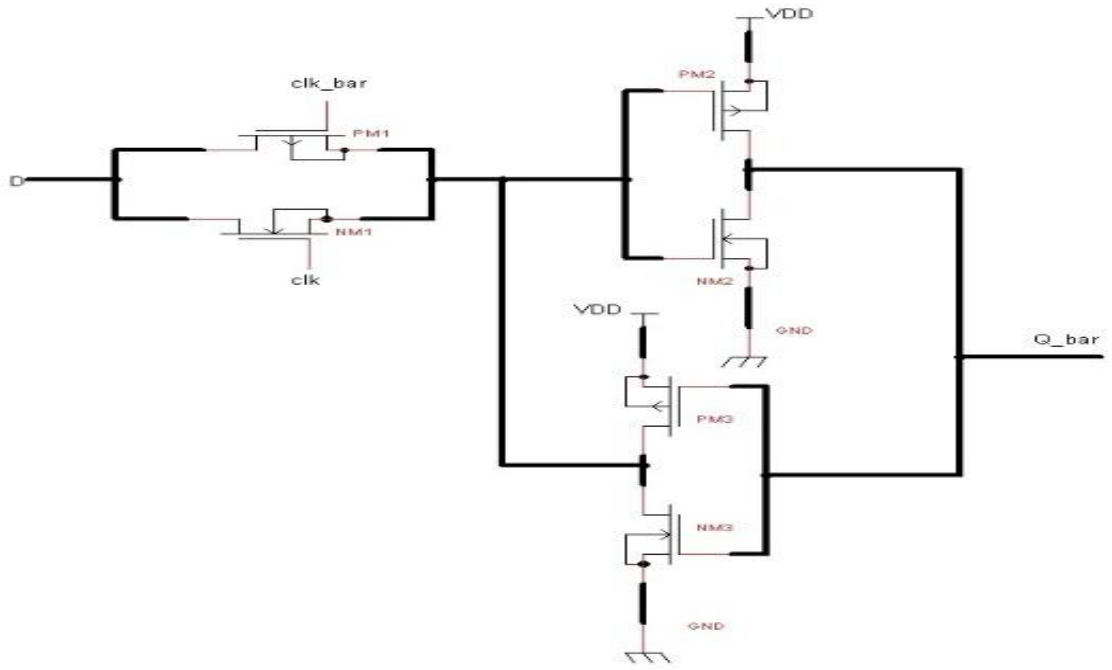


Fig 1.1.(B) Static D-FF

The FF can be either level or edge triggered, and thus can be classified as follows:

1. Positive level triggered flip-flops
2. Negative level triggered flip-flops
3. Positive edge triggered flip-flops
4. Negative edge triggered flip-flops
5. Dual edge triggered flip-flop

1.2 *POSITIVE LEVEL TRIGGERED FLIP-FLOPS:-*

These flip-flops operate when clock is at logic high level, and don't respond to any transition in clock or when clock is at low logic. Fig.1.2 (A) and (B) shown typical example of +ve level triggered static and dynamic type D flip-flop respectively. It is clear that input data is transfer to output when clock is at logic high level.

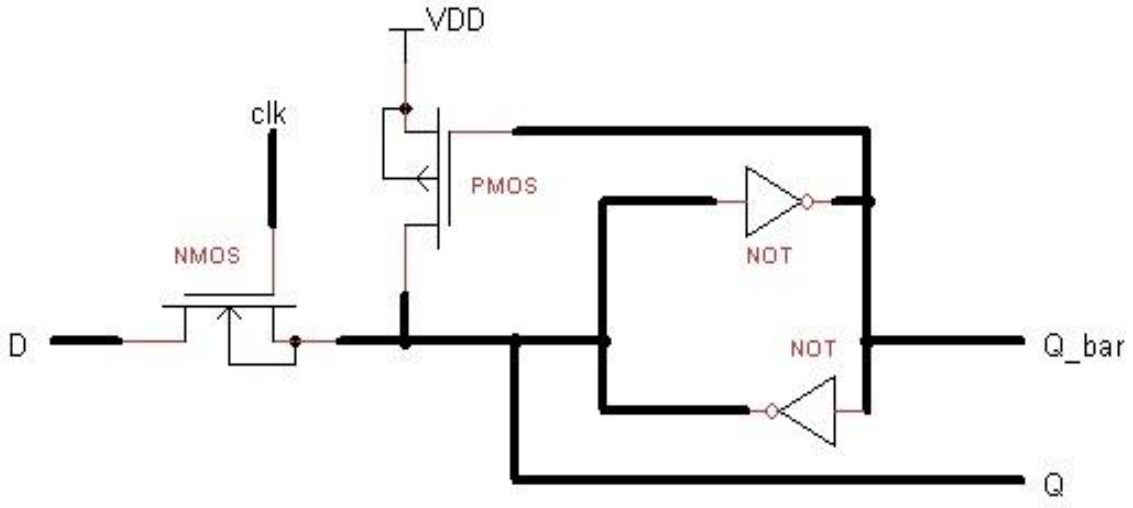


Fig 1.2.(A) +ve level static D-FF

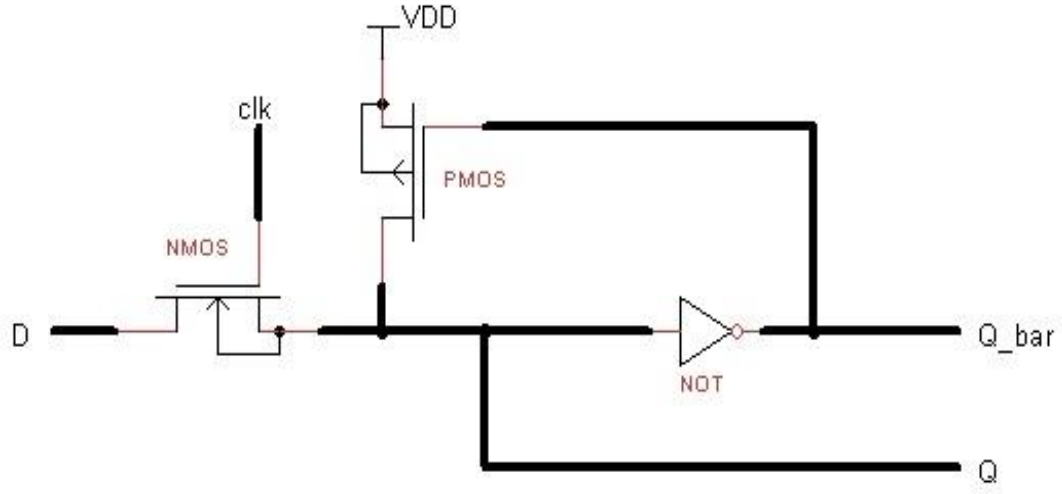


Fig 1.2(B) +ve level dynamic D-FF

1.3 *NEGATIVE LEVEL TRIGGERED FLIP-FLOPS:-*

As name specified, -ve level triggered flip-flops work only at low logic of clock pulse. Circuit schematic of –ve level triggered flip-flops using transmission gate shown in Fig.1.3. (A) and (B). Transmission gate based flip-flops do not need voltage boost circuit mechanism as in Fig.1.2 (A) and (B) which are based on pass transistor.

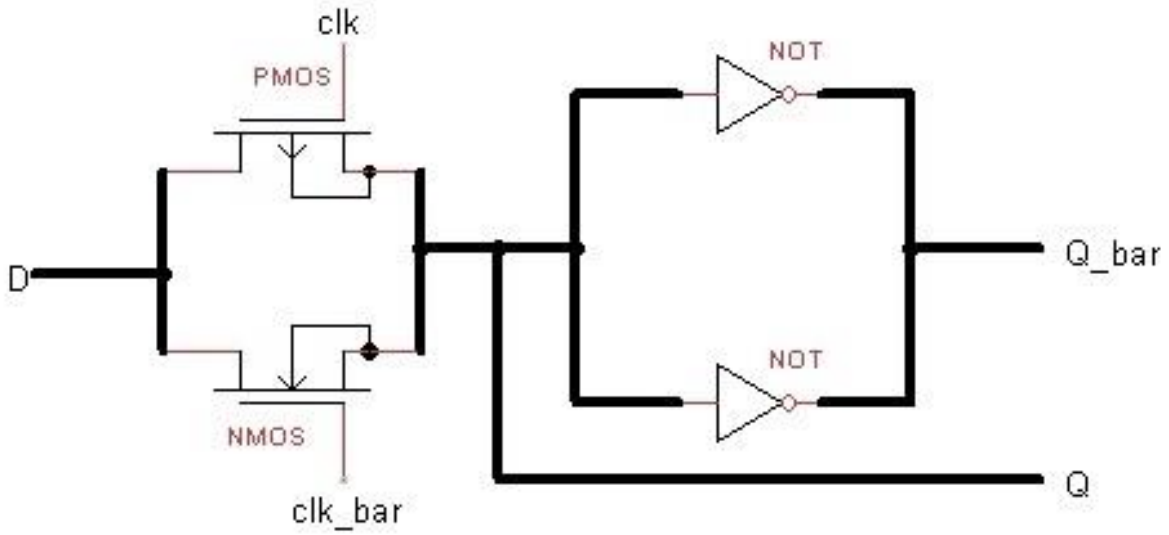


Fig 1.3.(A) –ve level triggered static D-FF

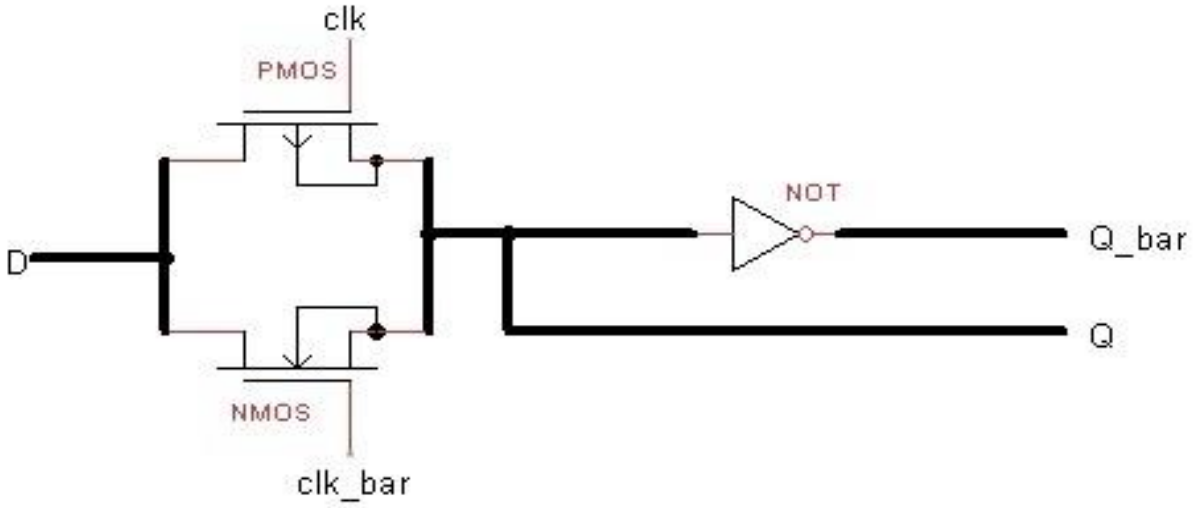


Fig 1.3.(B) –ve level triggered dynamic D-FF

1.4 *POSITIVE EDGE TRIGGERED FLIP-FLOPS:-*

When rising edge of clock is utilized to trigger the flop-flop, such flip-flops comes under category of +ve edge triggered flip-flops. Schematic of +ve edge triggered flip-flop shown in Fig.1.4.(A) and (B).

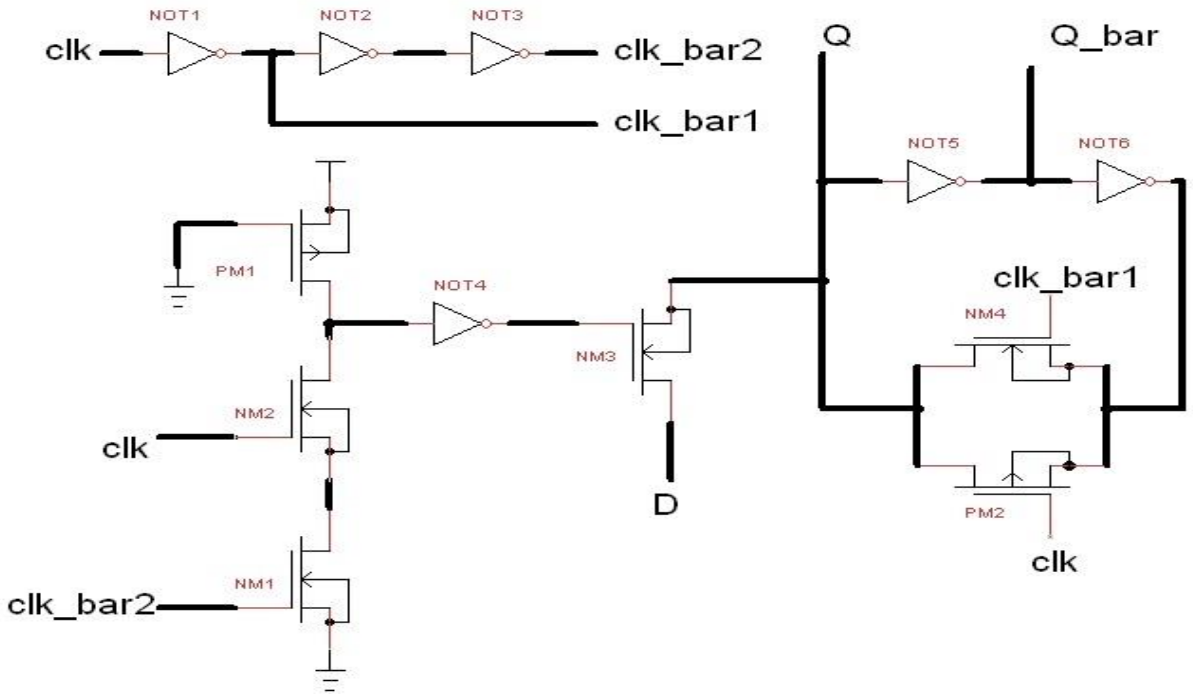


Fig 1.4.(A) +ve edge triggered static D-FF

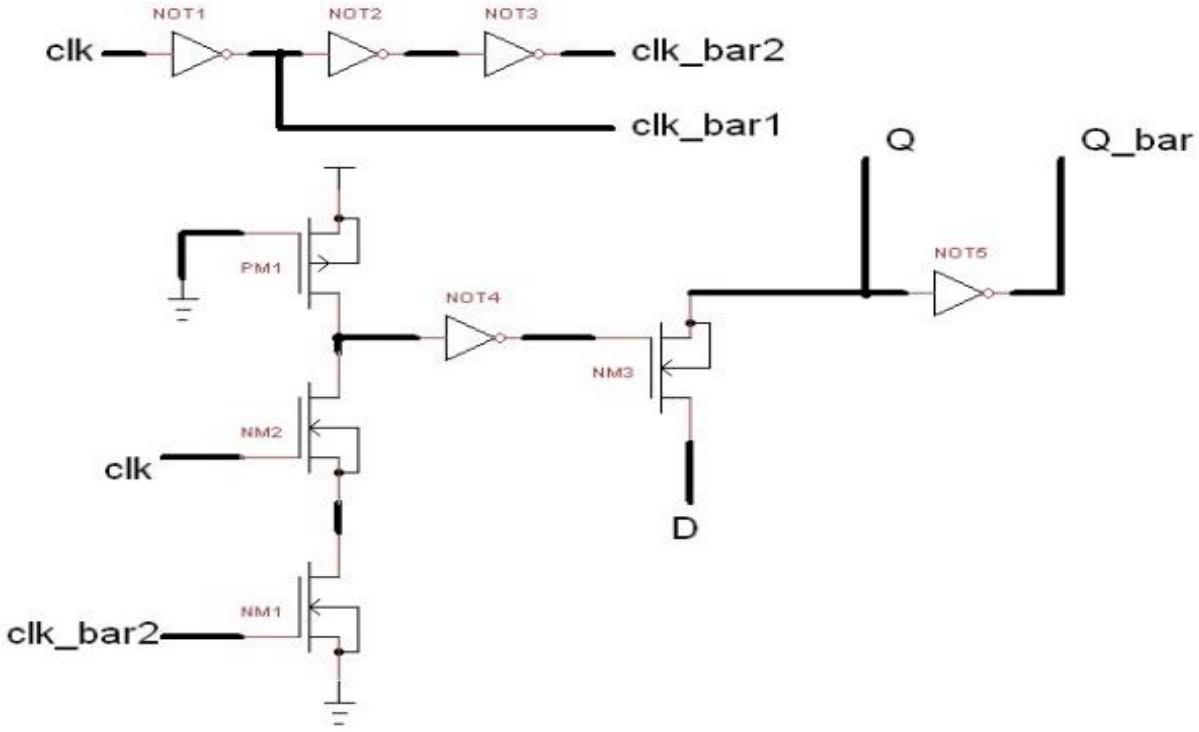


Fig 1.4.(B) +ve edge triggered dynamic D-FF

1.5 *NEGATIVE EDGE TRIGGERED FLIP-FLOPS:-*

In contrast to +ve edge triggered flip-flop, -ve edge triggered flip-flop works on falling edge of clock.

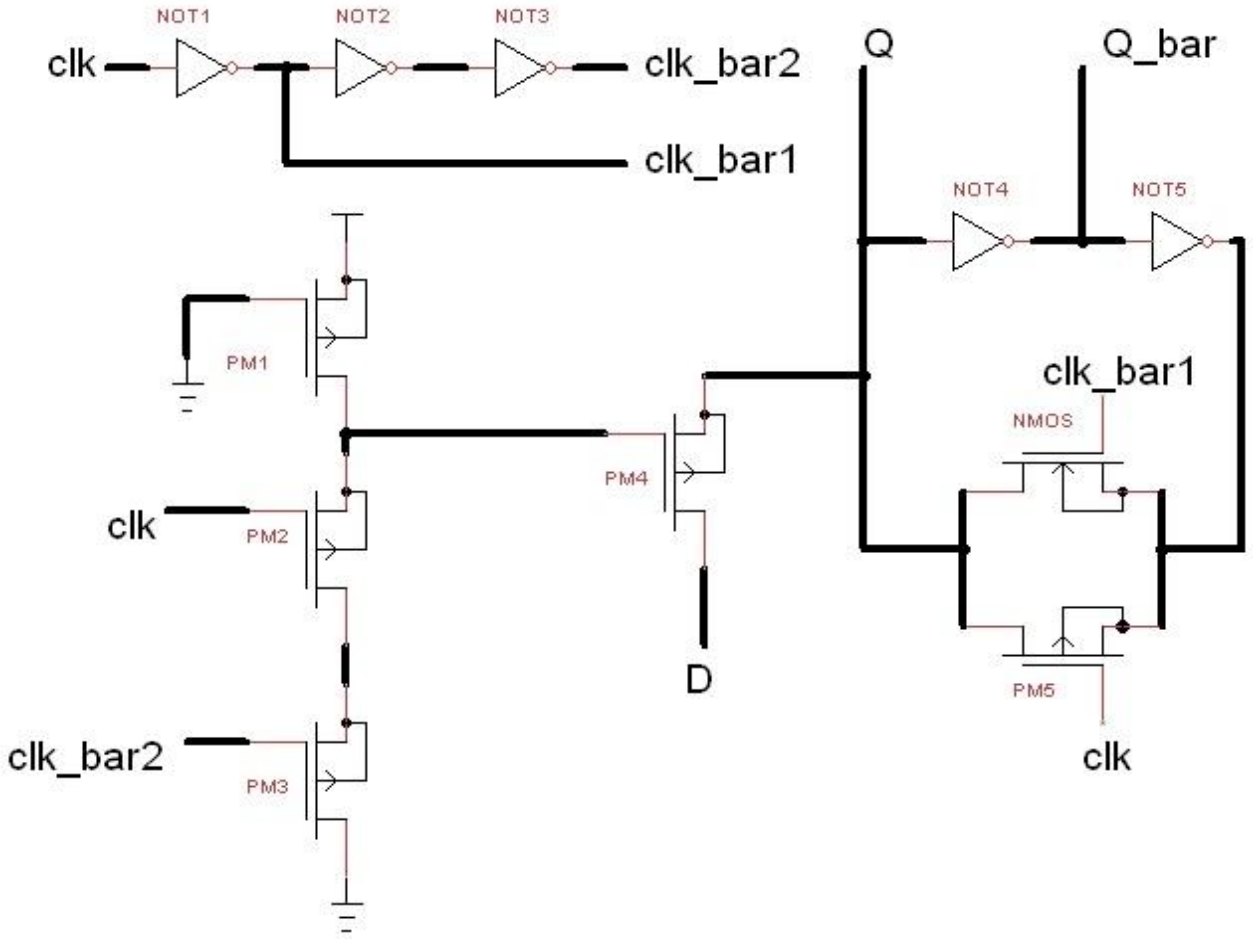


Fig 1.5.(A) -ve edge triggered static D-FF

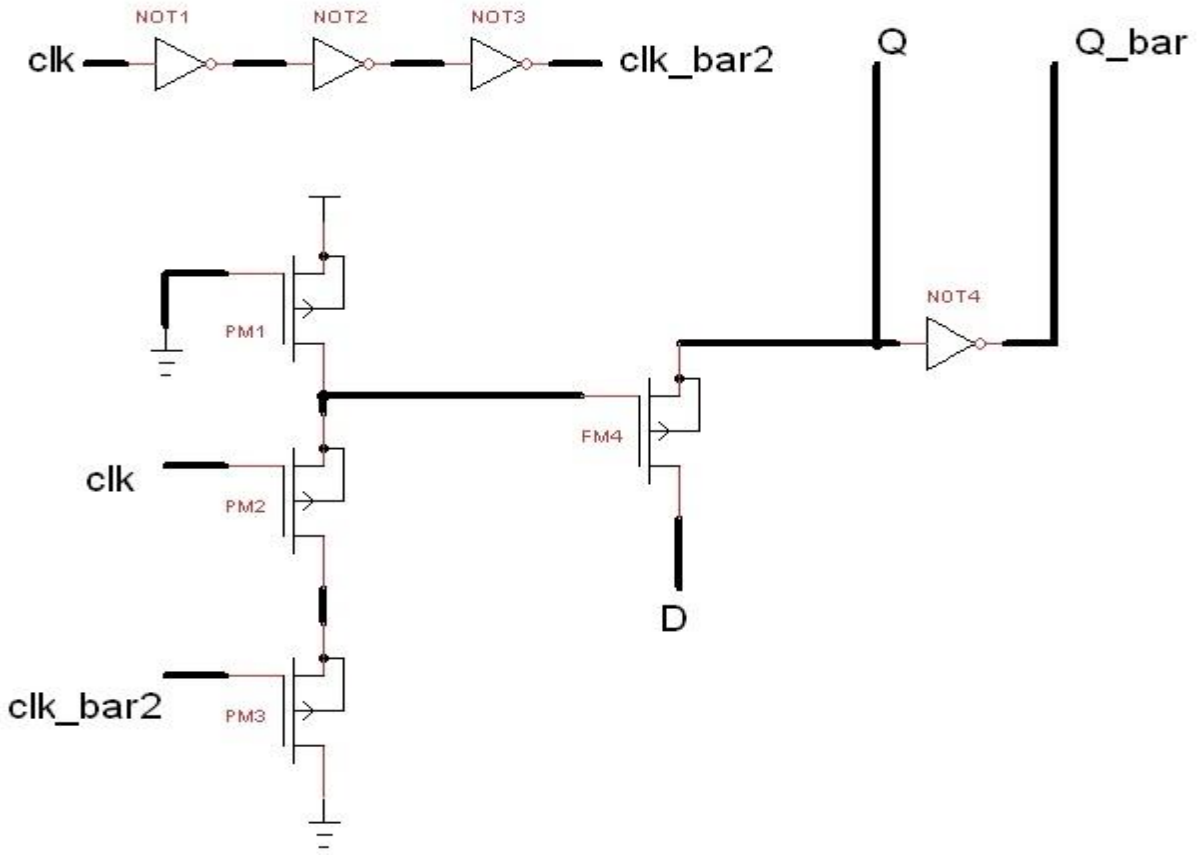


Fig: 1.5.(B) -ve edge triggered static D-FF

1.6 *DUAL EDGE TRIGGERED FLIP-FLOPS:-*

In dual edge triggered flip-flops, both edge of clock is utilizes to sample the input data. Simple Dual edge triggered flip-flop can be made by parallel combination of +ve edge and -ve edge triggered flip-flop as shown in Fig.1.6.(A).

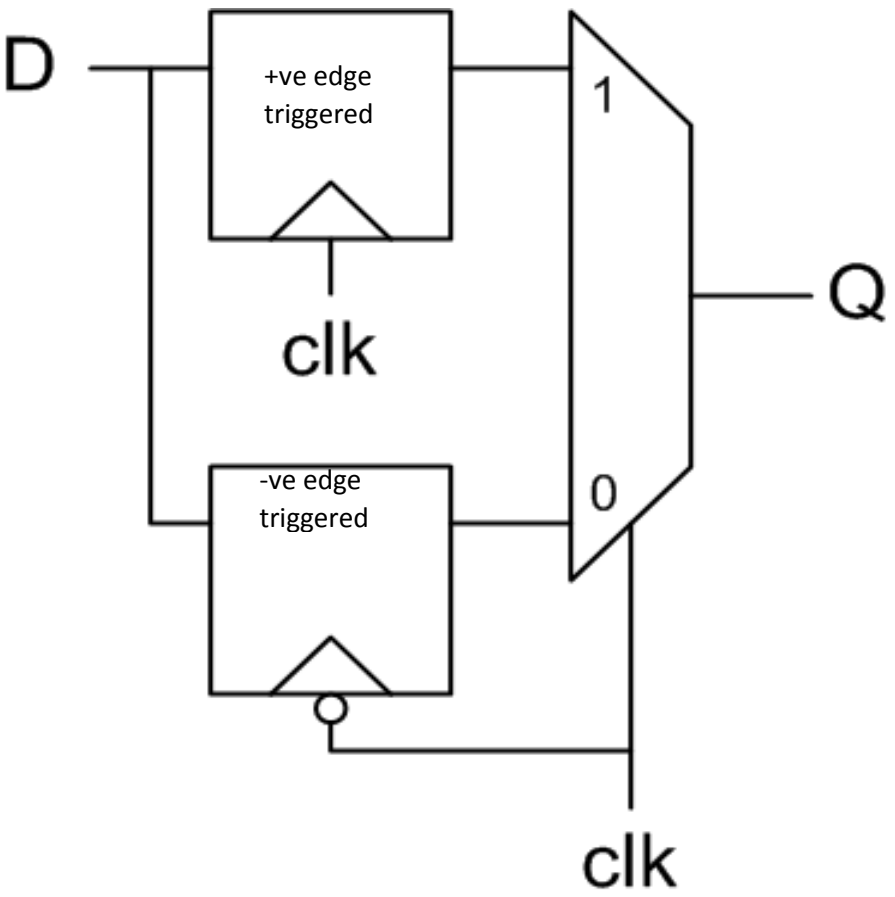


Fig 1.6.(A) Simple configuration for Dual edge triggered D-FF

But structure shown as above is bulky and consumed more power another kind of structure for dual edge triggered D-FF shown in Fig.1.6.(B) this is much efficient design but having less speed than FF shown in Fig.1.6.(A).

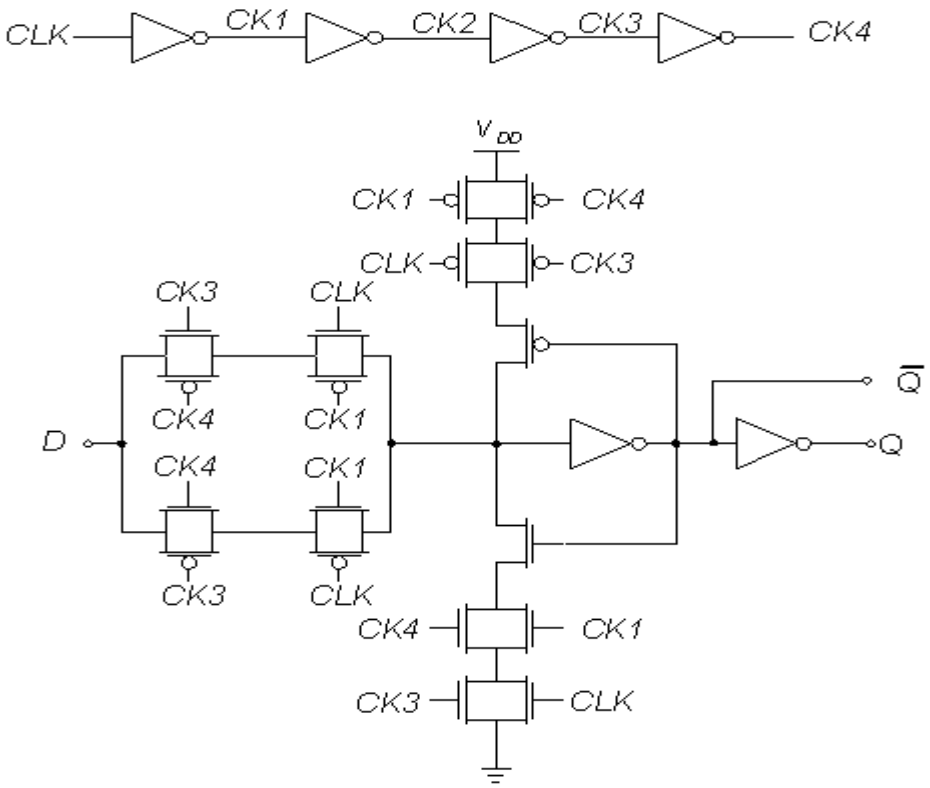


Fig 1.6.(B) Another configuration for dual edge triggered flip-flop

Following Fig.1.6.(C) shows the output for +ve edge triggered flip-flop and dual edge triggered flip-flop for same data sequence and clock pulse.

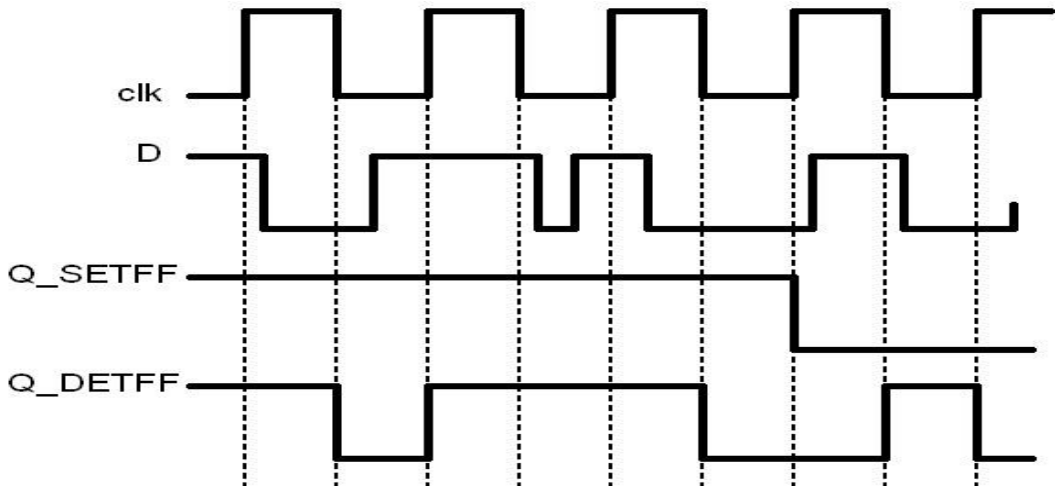


Fig 1.6.(C) output data for single edge triggered flip-flop (SETFF) and dual edge triggered flip-flop (DETFF)

The problem with level triggered flip-flop is that inputs change the outputs many times for single clock pulse and condition can be even worse when output is feedback to the input. Race-around condition is the key disadvantage of level triggered flip-flops. When Level triggered FF work in toggle mode then output changes many times for single clock pulse that is undesirable, this phenomenon known as race-around condition.

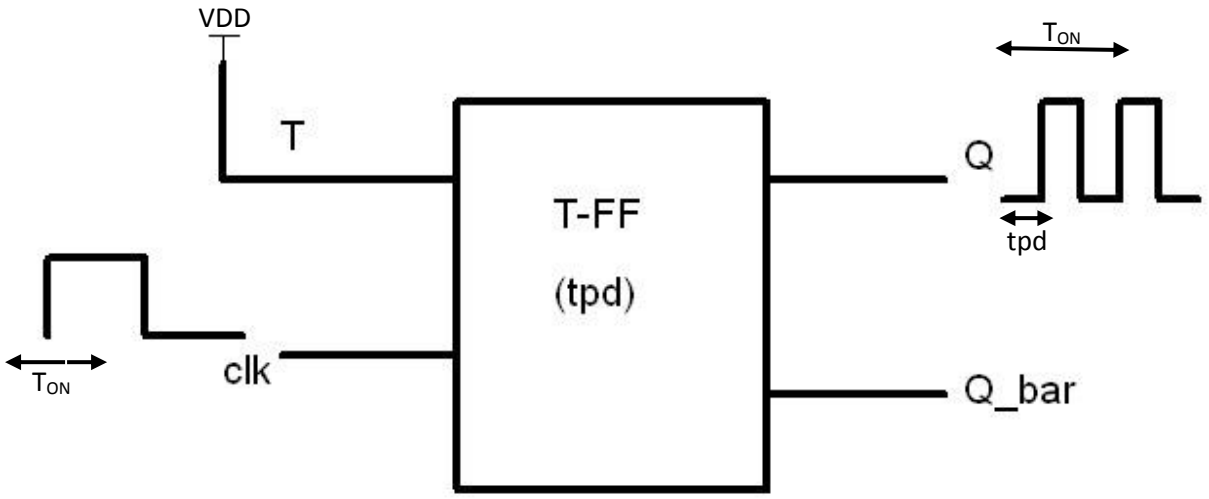


Fig 1.6.(D) race around condition in T-FF

To avoid race-around condition master-slave flip-flop or following clock scheme can be used:

I. ON time of clock pulse (T_{ON}) < Propagation delay (t_{pd}) of +ve level triggered flip-flop but overall $T_{clk} > t_{pd}$
II. OFF time of clock pulse (T_{OFF}) < Propagation delay (t_{pd}) of -ve level triggered flip-flop but overall $T_{clk} > t_{pd}$

Besides arrangement in clock duty cycle, master-slave or edge triggered flip-flops are widely used to avoid race-around condition. In master-slave flip-flop [2], output is taken from slave whereas input signal is fed to its master as shown in Fig.1.6.(E).

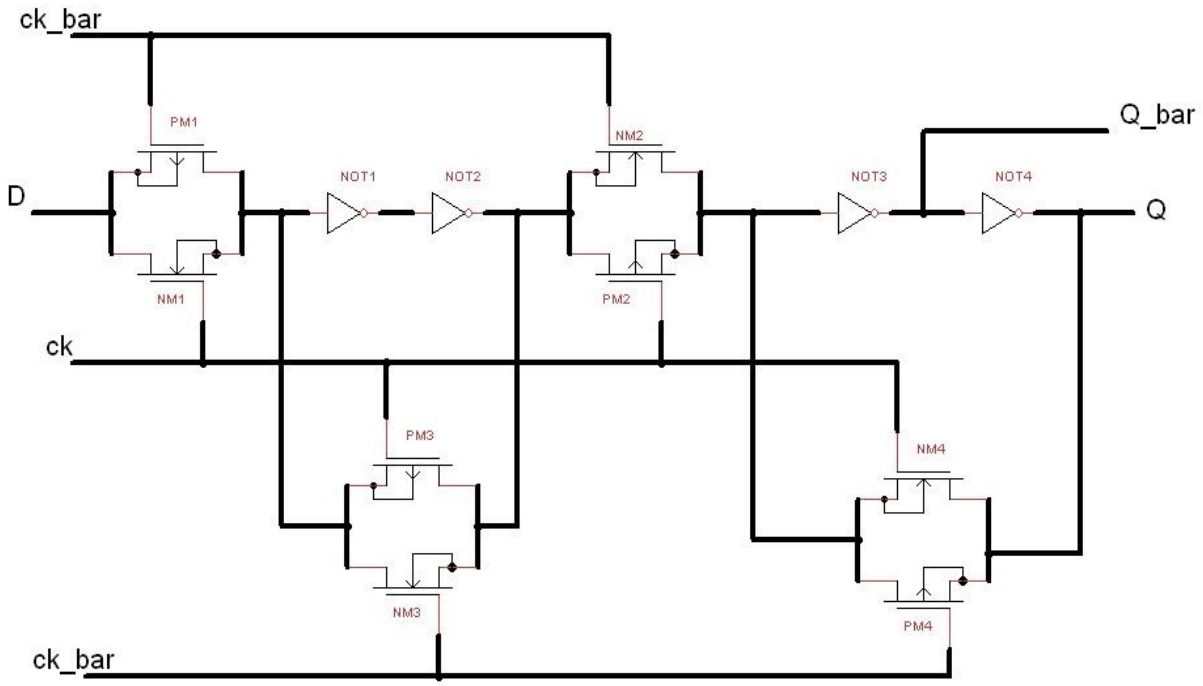


Fig 1.6.(E) Master-slave D-FF

Master and slave is on opposite phase of clock therefore master and slave run alternatively. Master-slave flip-flops require more number of transistor thereby consumed more area and power whereas edge triggered flip-flops are small, fast and consumed less power.

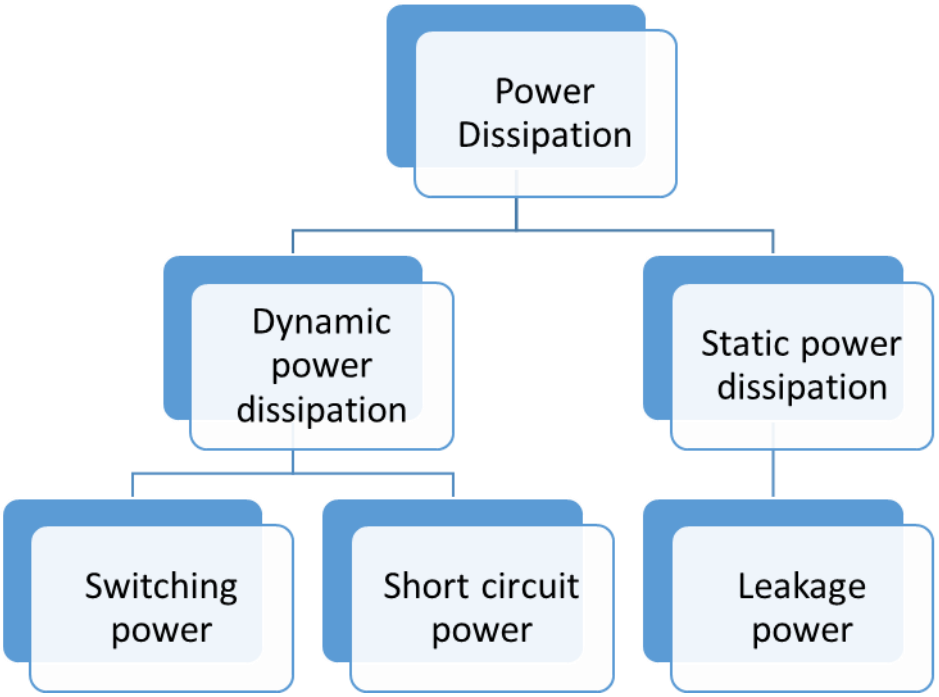
Single edge triggered flip-flops [7], (i.e. positive (+ve)/negative (-ve) edge triggered flip-flops) respond only at level transition of clock it means +ve edge triggered flip-flops work when clock transit from low to high level and – ve edge triggered flip-flops work when clock transit from high to low level. It is noteworthy that in single edge triggered flip-flops (SETFFs), one edge of clock is not utilized for data modification. However, voltage at the internal nodes of circuit changes on the clock edge and thereby resulting in significant switching power consumption during the unutilized clock edge. On the other hand, dual edge triggered flip-flop (DETFF) operates with both edge of clock. To achieve same data throughput DETFF requires half of clock pulse and power consumption is significantly lower in DETFF. For example to send data sequence 1101 SETFF require four clock pulse while DETFF requires only two clock pulse.

In order to integrate more number of functionalities in an Integrated Circuits (ICs) with given area, the devices are reducing in size in an aggressive manner. Such an increase in number of switching nodes, and a miniaturization of device size, both dynamic and static power dissipation are increasing at an alarming rate with the technology generation. This is not only a serious problem for portable application but also for high performance desktop application since it requires a costly cooling mechanism. As In small chip area billion of transistors can be mend but it cost increment in power dissipation through device. Depending upon application for which a device is used power dissipation also differ. Reliability of chip degraded with higher power dissipation. It is tough job to optimize the device for all application in concern of power dissipation. An ideal device has to be fast and must work at low power, but in practical sense delay and power dissipation cannot be reduce simultaneously. There is a compromisation between delay and power for a device. In general both delay and power are inversely proportional to each other for a device, thereby for a device power delay product (PDP) must be as small as possible. To stand in current semiconductor market, a chip must have low PDP. Most of electronic circuit based on MOS device, lots of research have been done to reduce power and delay [8, 9, 10]. Flip-flops are basic components for sequential circuits. Normally 20 to 45 % of total power is dissipated by flip-flops. So FFs needs high attention in design of low PDP system.

Chapter 2: BRIEF INTRODUCTIN OF SOURCES OF POWER DISSIPATION IN SEMICONDUCTOR DEVICES

Portable electronic industries are booming now days. Most of portable electronic devices run on battery for energy that's why energy consumed by device is as important as performance and area of the device. A deep research has been done through recent years in concern of sources of power dissipation in semiconductor devices. There are three source of power dissipation in CMOS digital circuit [16, 23],

1) Switching power dissipation
2) Short circuit power dissipation
3) Leakage power dissipation



Thus

$$\mathbf{P_{Total} = P_{Switching} + P_{Short} + P_{Leakage}}$$

2.1 REVIEW OF LEAKAGE POWER DISSIPATION:

$$P_{Leakage} = I_{Leakage} \times V_{DD}$$

Different type of leakage current illustrated in Fig.2for n-channel MOS.

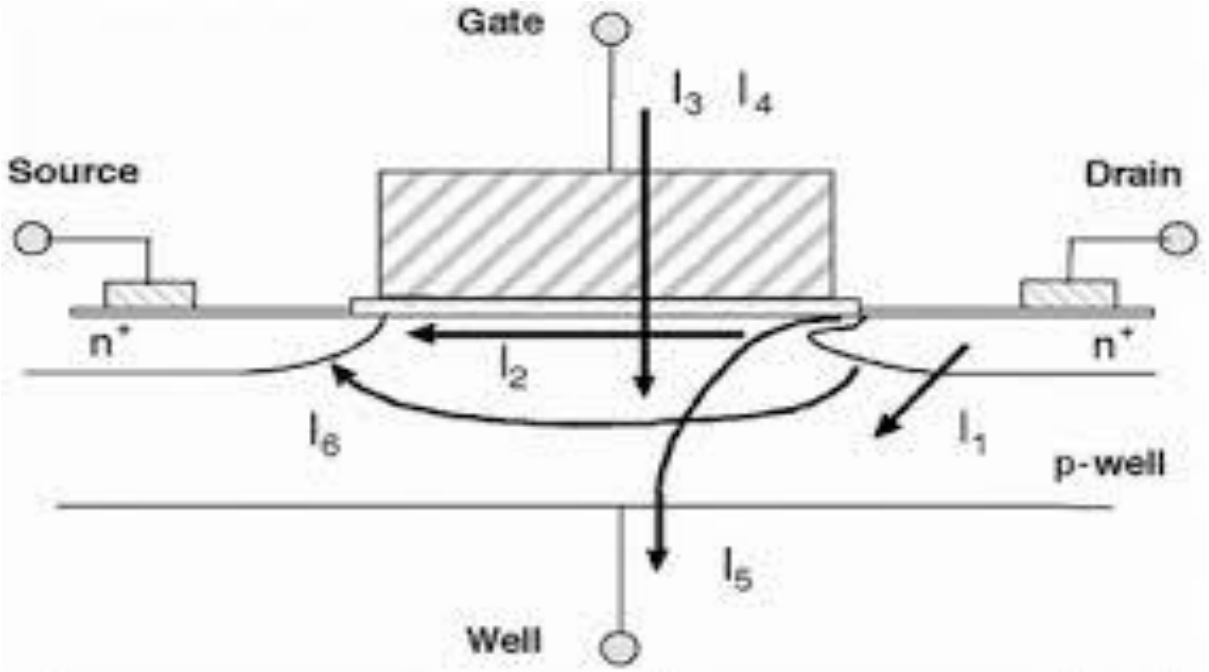


Fig 2.1 Leakage currents in MOS

These currents are:

1. pn junction reverse bias current (I_1)
2. Subthreshold leakage (I_2)
3. Gate tunnelling (I_3)
4. Hot carrier injection (I_4)
5. Gate induced drain leakage (GIDL) (I_5)
6. Punch-through (I_6)

2.1.1 PN JUNCTION REVERSE BIAS CURRENT:-

This current have two main component:

a) Minority carrier diffusion/drift near the edge of the depletion region

b) Electron-hole pair generation in depletion region

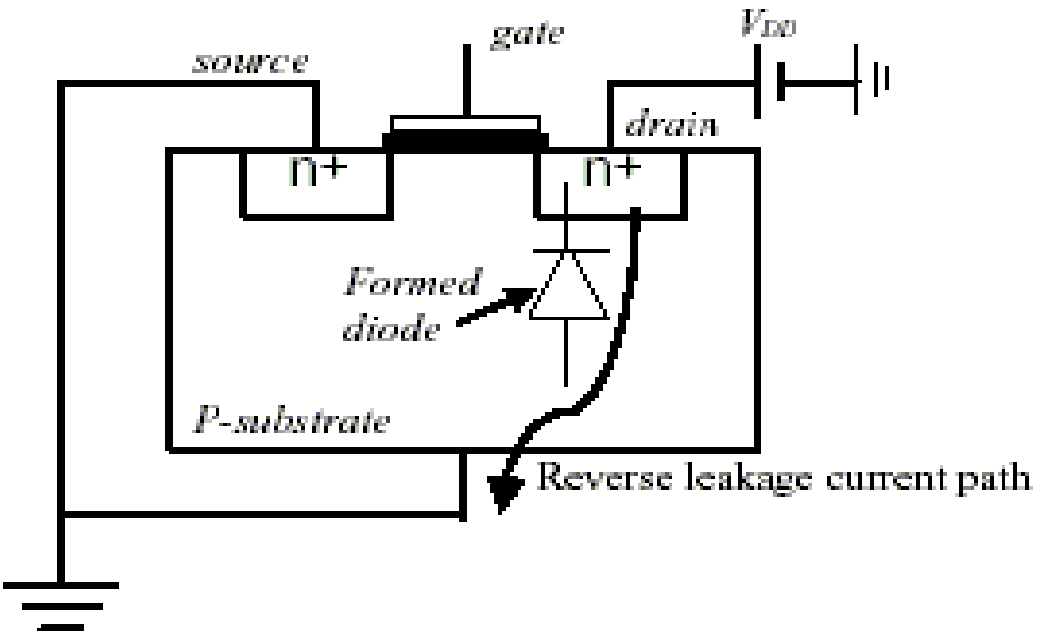


Fig 2.1.1 Junction leakage current

Mathematical expression shows reverse leakage current is strong function of junction area and temperature.

$$I_{reverse} = A.J_s.(e^{\frac{q.V_{bias}}{k.T}} - 1) \quad \text{……(1)}$$

Where,

J_s = reverse saturation current density

A = the junction area

Js is strong function of temperature because p_{n0}, n_{p0} and E_g depends on temperature. This is shown in equation (2), (3) and (4).

$$J_s = q.[\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0}] \quad \text{.....(2)}$$

$$n_{p0} = \frac{n_i^2}{N_A}$$

$$p_{n0} = \frac{n_i^2}{N_D} \quad \text{.....(3)}$$

$$n_i = k'.T^{3/2}[-\frac{E_g}{2kT}]$$

$$E_g = E_{g0} - \frac{\alpha T^2}{\beta + T} \quad \text{.....(4)}$$

Where,

A is the junction area

D_p=diffusion coefficient for hole in n-region

D_n=diffusion coefficient for electron in p-region

L_p=diffusion length of hole in n-region

L_n=diffusion length of electron in p-region

n_{p0}=minority electron concentration in p-region

p_{n0}=minority hole concentration in n-region

n_i=intrinsic carrier concentration

E_g=band gap energy

E_{g0}=band gap energy at absolute zero temp.

2.1.2 SUBTHRESHOLD LEAKAGE (I_2):-

When gate voltage of MOS device is less than threshold voltage, then MOS device is in weak inversion region. In weak inversion region, there is current between source and drain, this is subthreshold leakage current (I_2).

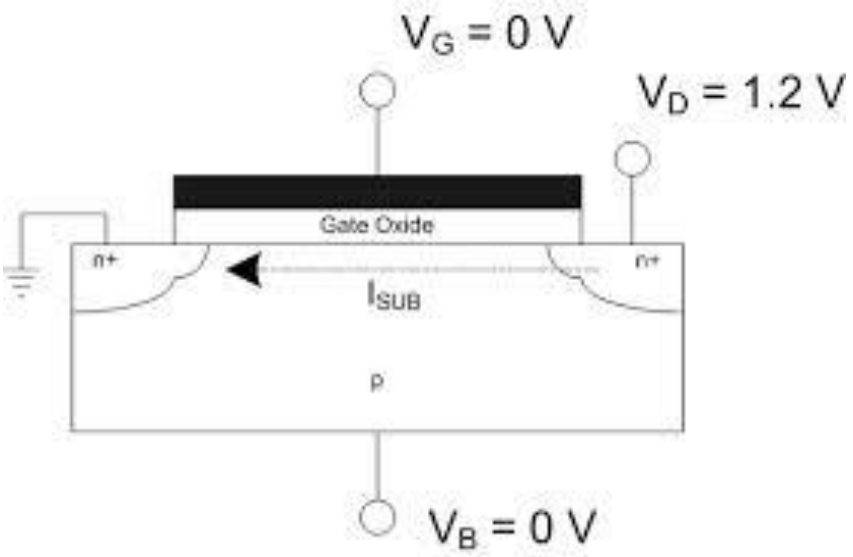


Fig 2.1.2.(A) Subthreshold leakage current

$$I_{SUB} \propto e^{\frac{q(V_G - V_{th})}{mkT}} \quad \text{.....(5)}$$

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3t_{ox}}{W_{dm}} \quad \text{.....(6)}$$

$$S_t \propto m \quad \text{.....(7)}$$

Where

V_G = gate voltage

V_{th} = threshold voltage

C_{ox}=Gate oxide capacitance

C_{dm}=Depletion layer capacitance

t_{ox}=Oxide layer thickness

W_{dm}=Depletion layer width

S_t = subthreshold slope

m = body effect coefficient

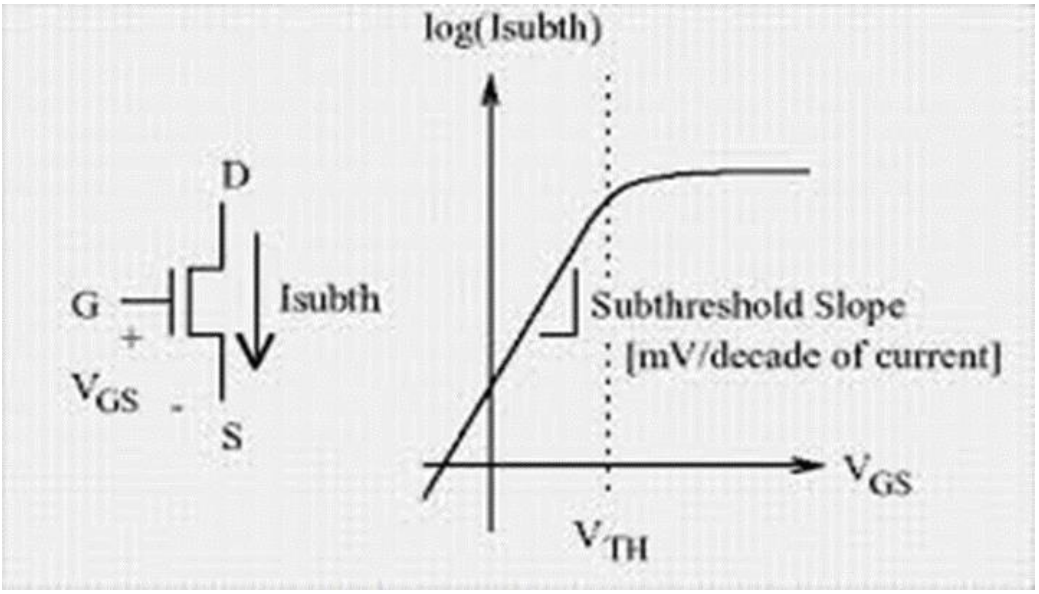


Fig 2.1.2.(B) Subthreshold current vs Gate voltage

Subthreshold slope indicate how effectively drain current can be stopped when gate voltage is less than V_{th}. Lower value of S_t is desirable for that following things can be done.

a) t_{ox} can made smaller

b) Reduce the substrate doping concentration so that W_{dm} can be larger.

Further I_{SUB} can be reduced by increasing the value of threshold voltage (V_{th}). Vth can be increased by modifying following parameter:

- Increasing body bias voltage
- Increasing substrate doping
- Increasing oxide layer thickness
- Decreasing permittivity of oxide layer
- Choosing semiconductor with higher work function

V_{th} also depends upon temperature, it decreases with increase in temperature and S_t increases with temperature. V_{th} also depends on DIBL (drain induced barrier lowering) effect. DIBL occurs in short channel device. Because in short channel device depletion

region of drain interacts with source and lower the source potential barrier, it is illustrated in Fig.2.1.2.(C) Because of DIBL, Vth reduces.

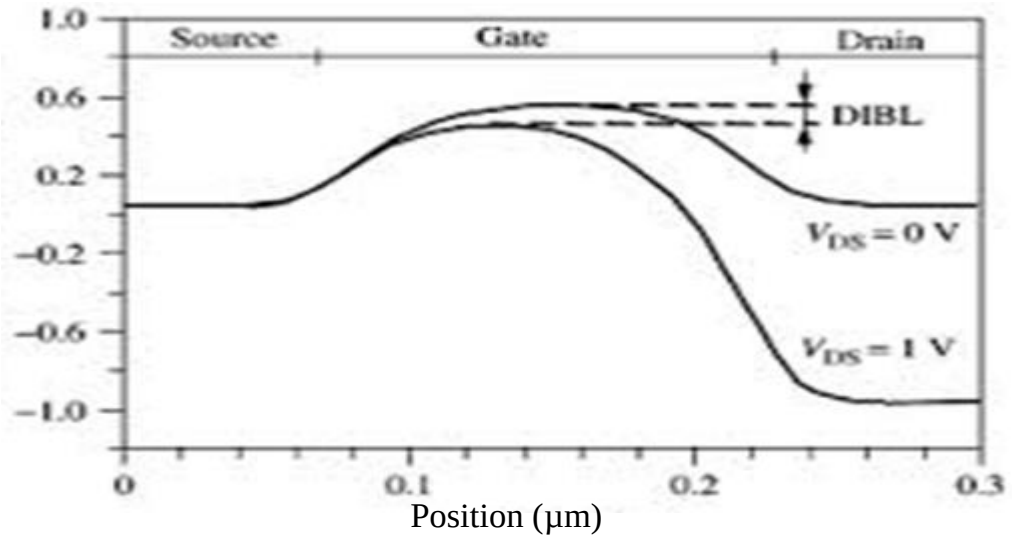


Fig 2.1.2.(C) DIBL effect in NMOS

In nano scaled semiconductor device, quantum mechanical effect cannot be ignored, V_{th} increases because of quantum mechanical effect.

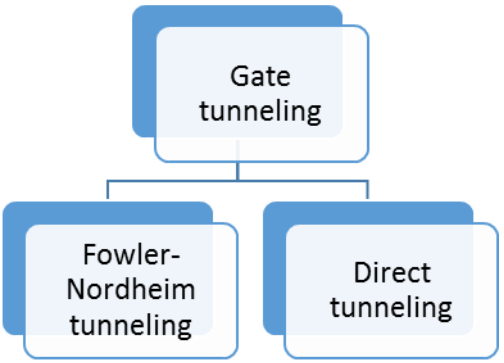
2.1.3 GATE TUNNELLING CURRENT (I_3):-

Tunnelling phenomenon comes from quantum mechanics, it tells because of low oxide thickness (t_{ox}) in submicron devices, high electric field occurs across the oxide that results in electron tunnelling from substrate to gate and gate to substrate. Gate tunnelling is of two types:

- Fowler-Nordheim tunneling (tunneling through triangular potential barrier) occurs when $V_{ox} > \phi_{ox}$.
- Direct tunneling (tunneling through trapezoidal potential barrier) occurs when $V_{ox} < \phi_{ox}$.

Where

V_{ox} is voltage drop across oxide.



ϕ_{ox} is Si-SiO_2 interface barrier height.

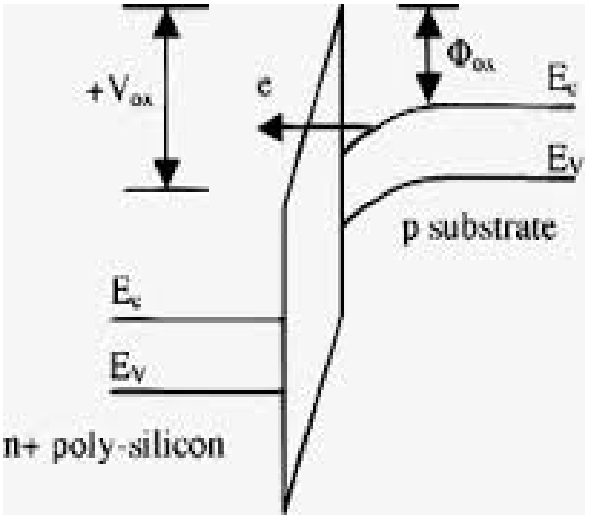


Fig 2.1.3.(A) Fowler-Nordheim tunneling

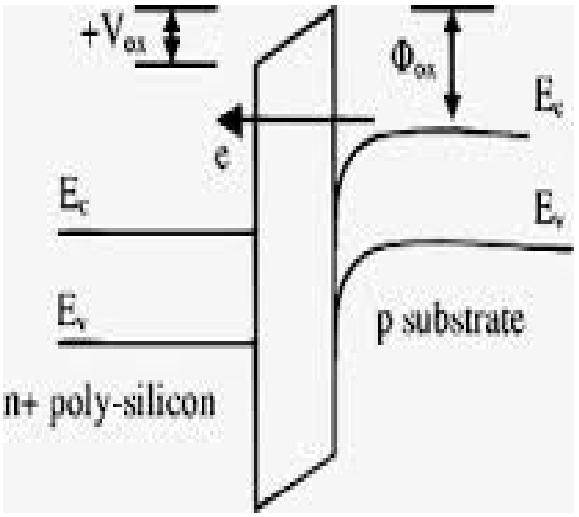


Fig 2.1.3.(B) Direct tunneling

2.1.3.1 MECHANISM OF GATE TUNNELING CURRENT:-

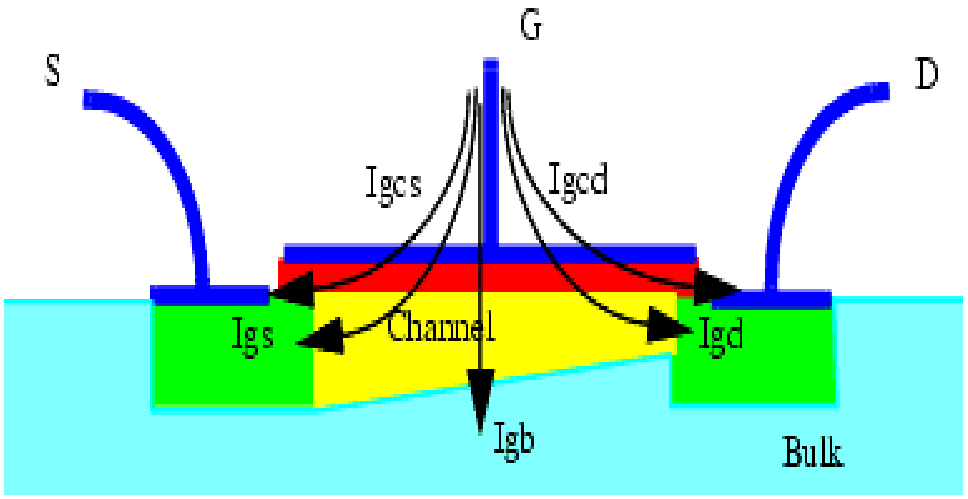


Fig 2.1.3.1 Components of Gate current

Gate current further divide into five parts namely:

I_{gs} : gate to source tunneling current

I_{gd} : gate to drain tunneling current

I_{gb} : gate to body tunneling current

I_{gos} : gate to overlapped source current

I_{god} : gate to overlapped drain current

Mathematically:

$$I_{g,tunnel} = I_{gs} + I_{gd} + I_{gb} + I_{gos} + I_{god}$$

2.1.4 HOT CARRIER INJECTION CURRENT (I_4):-

Carriers have higher temperature than lattice, known as hot carrier. These carriers have higher velocity than thermally generate EHP. If drain voltage is sufficiently large then there is high electric field near the drain end thereby electrons or holes in channel can gain sufficient energy from the electric field to break the covalent bond of molecule and generate EHP (impact ionization). Generated electrons attracted towards drain and can also tunnel to gate, similarly holes are attracted towards body and source as shown in Fig.2.4. Thus total drain current would be:

$$I_D = I_{DS} + I_{g,hot} + I_{DB,hot}$$

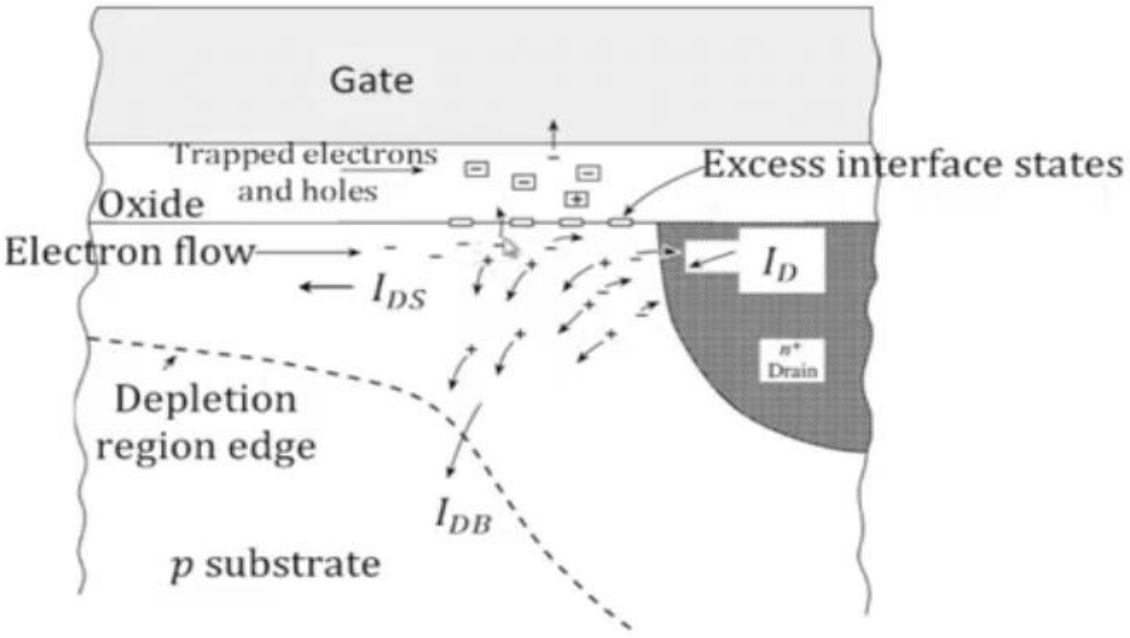
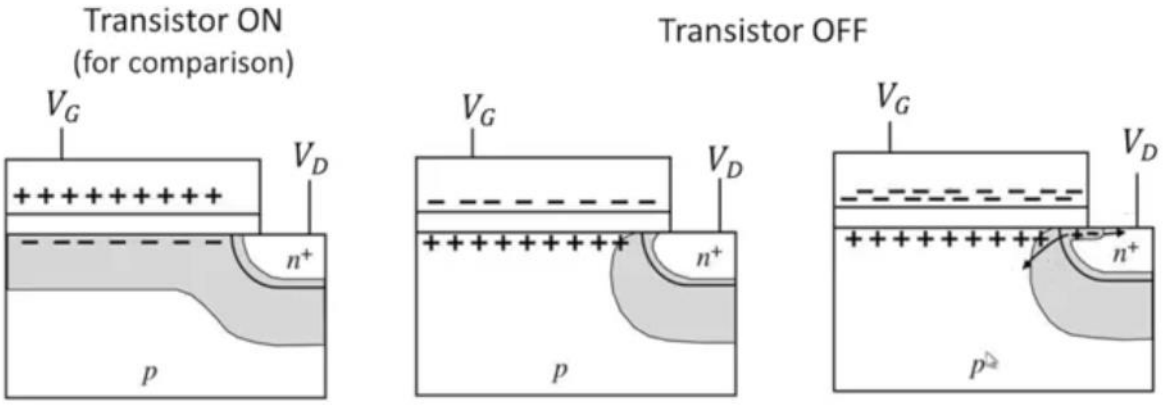


Fig 2.1.4 Hot carrier injection current

2.1.5 GATE INDUCED DRAIN LEAKAGE (I5):-



(A) Normal operation (B) V_G < 0 V (C) V_G is more negative

Fig 2.1.5

GIDL occur in OFF state when MOS is in accumulation region. It is illustrated in Fig.2.5, where Fig (A) represents normal operation of nMOS in ON condition and Fig.2.5.(B) shows how the accumulation region form when gate voltage is slightly less than 0 V. Further if gate voltage is more reduced then p+ region formed near the surface as shown in Fig.2.5.(C). Electrons in drain also repelled by gate voltage in overlapped gate-drain region thus there is high electric field in overlapped region. High electric field results generation of EHP in overlapped region, now generated electron neutralized by drain potential and hole moves towards bulk (or being neutralized by bulk potential). Thus there is a current between bulk and drain because of gate voltage, this is GIDL. GIDL can be enhanced by trap assisted tunneling. GIDL also known as **band to band** tunnelling current. This is shown in Fig.2.1.5.(D).

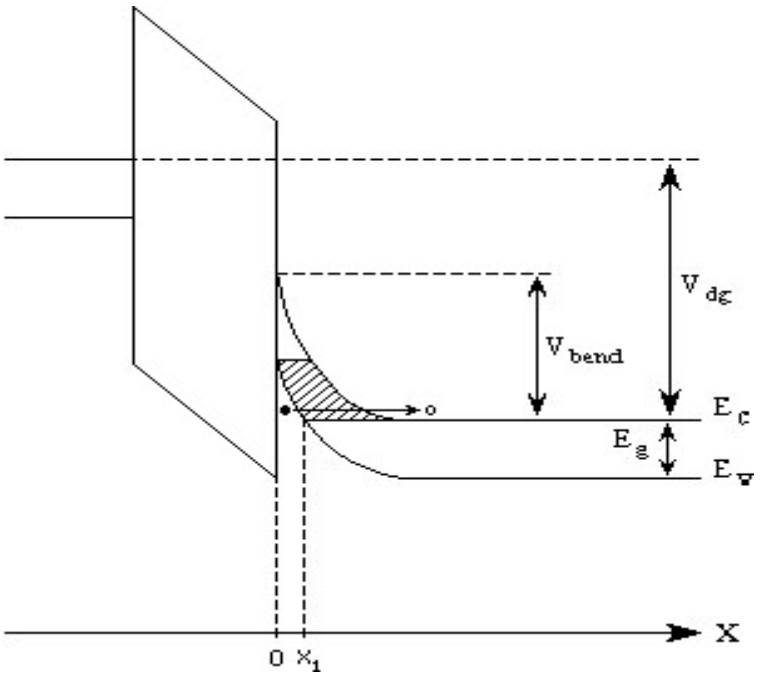


Fig 2.1.5.(D) band to band tunnelling

In order to reduce leakage V_{th} is increased by making body Voltage more negative but we failed because making body more negative results more GIDL and total leakage Current will increased.

2.1.6 PUNCH THROUGH CURRENT (I5):-

In order to compact the nMOS devices reduction in channel length is most effective way. But channel length cannot be reduced too much, Fig.2.1.6.(A) shows variation of current I_{DS} with respect to V_{GS} and V_{DS} in (a) and (b).

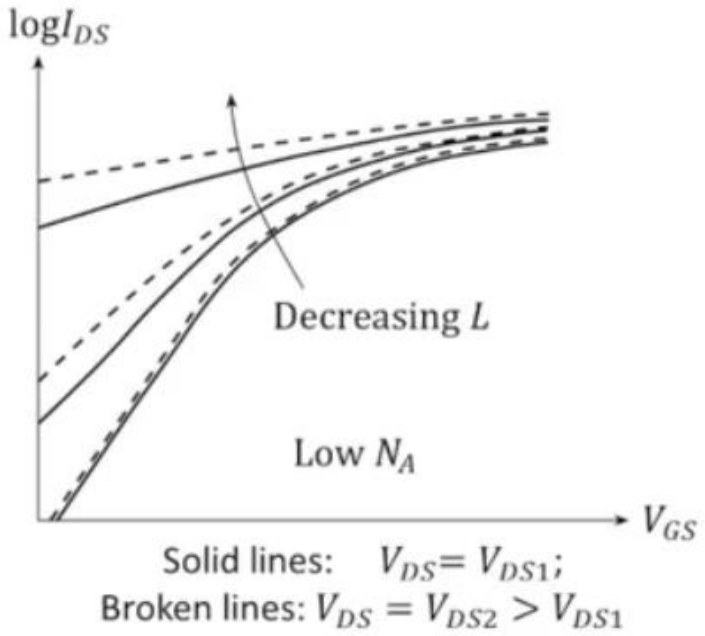


Fig 2.1.6.(A) I_{DS} vs V_{GS} on log scale for different channel length

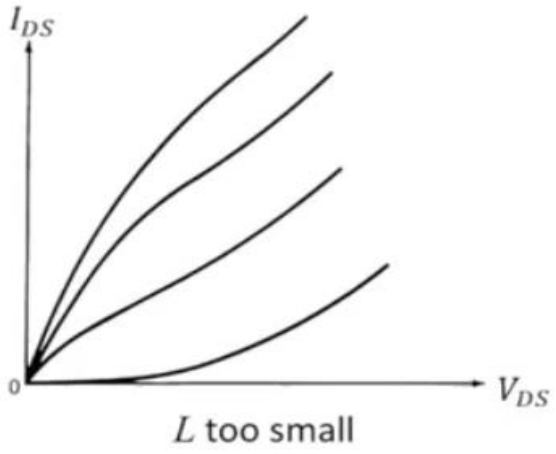


Fig2.1.6.(B) I_{DS} vs V_{DS}

Fig.2.6.(A) shows, for very small channel length, even when V_{GS} is zero volt there is large current between drain and source. This is not drain source expected current but is a very strong leakage current. Fig.2.6.(B) shows, if we use small L device then is practically useless device.

Punch through effect is of two types:

1. Surface punch through
2. Bulk punch through

Very roughly we can understand punch through effect as follows:

2.1.6.1 SURFACE PUNCH THROUGH:-

Assume gate voltage such that no inversion takes place. When the combination of drain and source voltage applied such that depletion region of drain and source touch each-other then we get very large leakage current which cannot be controlled by gate voltage. It is illustrated in Fig2.1.6.1.

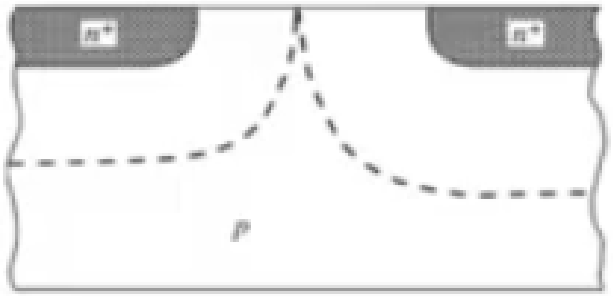


Fig 2.1.6.1 Surface punch-through

2.1.6.2 BULK PUNCH-THROUGH:-

Sometimes ion implantation is used near the channel to control threshold voltage in such case punch-through can be happen through bulk. This is shown in Fig.2.1.6.2.

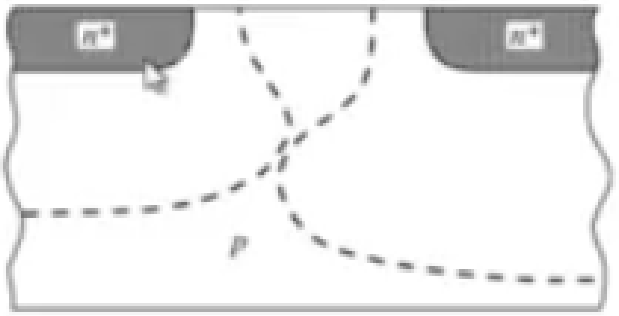


Fig 2.1.6.2 Bulk punch-through

2.2 REVIEW OF DYNAMIC POWER DISSIPATION:-

Changing the logic state of input and output results in short-circuit abs switching power dissipation. These are described as follows:

2.2.1 SHORT-CIRCUIT POWER DISSIPATION:-

To understand the short-circuit power dissipation [17, 18] let's take the example of CMOS inverter as shown in Fig.2.2.1.(A).

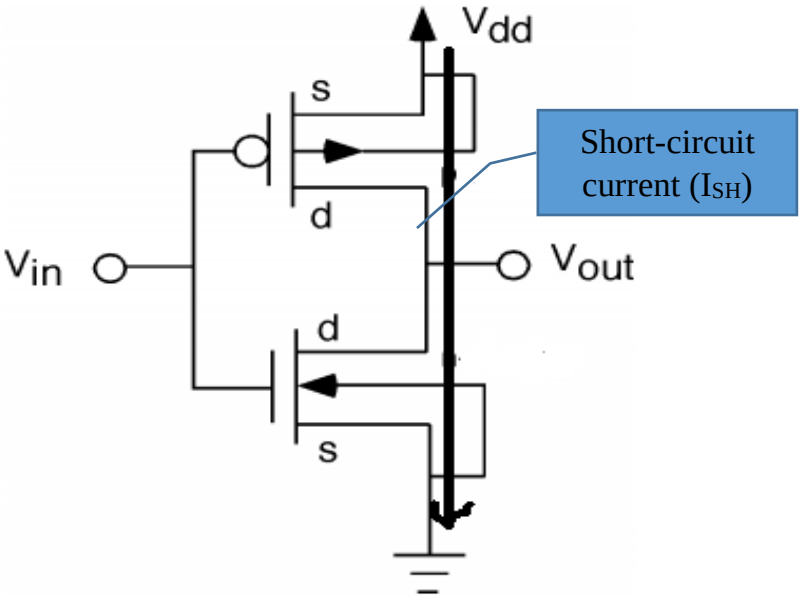


Fig 2.2.1.(A) Short circuit current in an Inverter

Practically instant change in logic state of input is not possible, it is taking some time to change its state, thereby when input is in transition state, region of operation of MOS devices changes accordingly as described in TABLE.2.2.1 and illustrated in Fig.2.2.1.(B).

TABLE: 2.2.1 Region of operation of an Inverter

Region	V_{in}	V_{out}	NMOS	PMOS
A	$< V_{t,n}$	V_{DD}	Cut-off	linear
B	V_{IL}	high	Saturation	linear
C	V_{th}	V_{th}	saturation	Saturation
D	V_{IH}	low	linear	Saturation
E	$V_{DD}+V_{t,p}$	Very low	linear	Cut-off

Where $V_{t,n}$ = threshold voltage of NMOS

$V_{t,p}$ = threshold voltage of PMOS

V_{IL} = low input voltage

V_{IH} = high input voltage

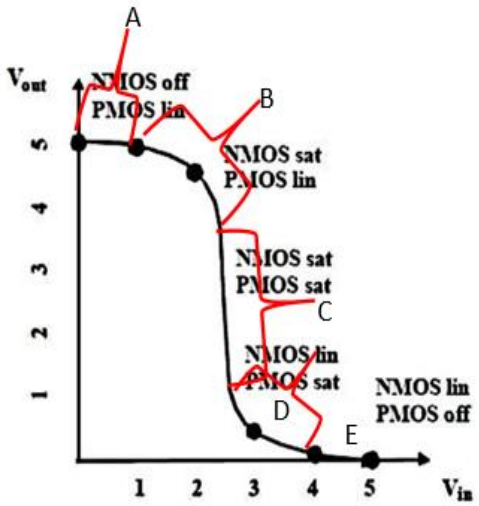


Fig 2.2.1.(B) VTC of an Inverter

In case when both MOS are in saturation region then a direct current flows between supply voltage and ground, that is short circuit current which causes power dissipation. For simplicity in calculation it is assumed that both MOS are symmetrical (i.e., $K_N = K_P = K$ and $V_{t,n} = V_{t,p}$) and symmetrical input signal (i.e., rise time = fall time).

If input signal, rise time = fall time = τ and time period is T. then, equation for short-circuit current and power dissipation are

$$I_{SHORT} = \frac{K}{12.V_{DD}}(V_{DD} - V_{th})^3 \frac{\tau}{T}$$

$$P_{SC} = I_{SHORT}.V_{DD} = \frac{K}{12}(V_{DD} - V_{th})^3 \frac{\tau}{T}$$

Graphically it is shown Fig.2.7.1(C).

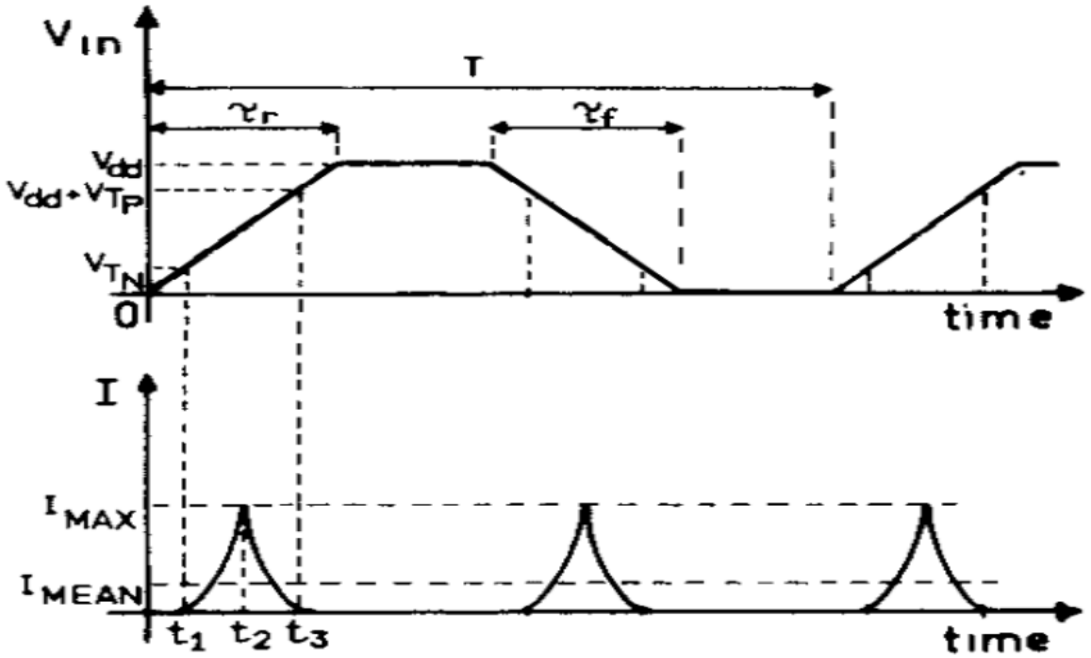


Fig 2.2.1.(C) Graph short circuit current

2.2.2 SWITCHING POWER DISSIPATION:-

Power dissipation at node during switching event comes under switching power dissipation i.e. when output node of a logic gate makes a logic transition. In CMOS logic circuit every node has effective capacitance, if any node making logic transition then this capacitance charge or discharge accordingly. These capacitances are mainly parasitic junction capacitance. Let's take an example of inverter, during charging phase output node charged up to VDD and during discharging phase output node discharged to ground, this is shown in Fig.2.2.2.

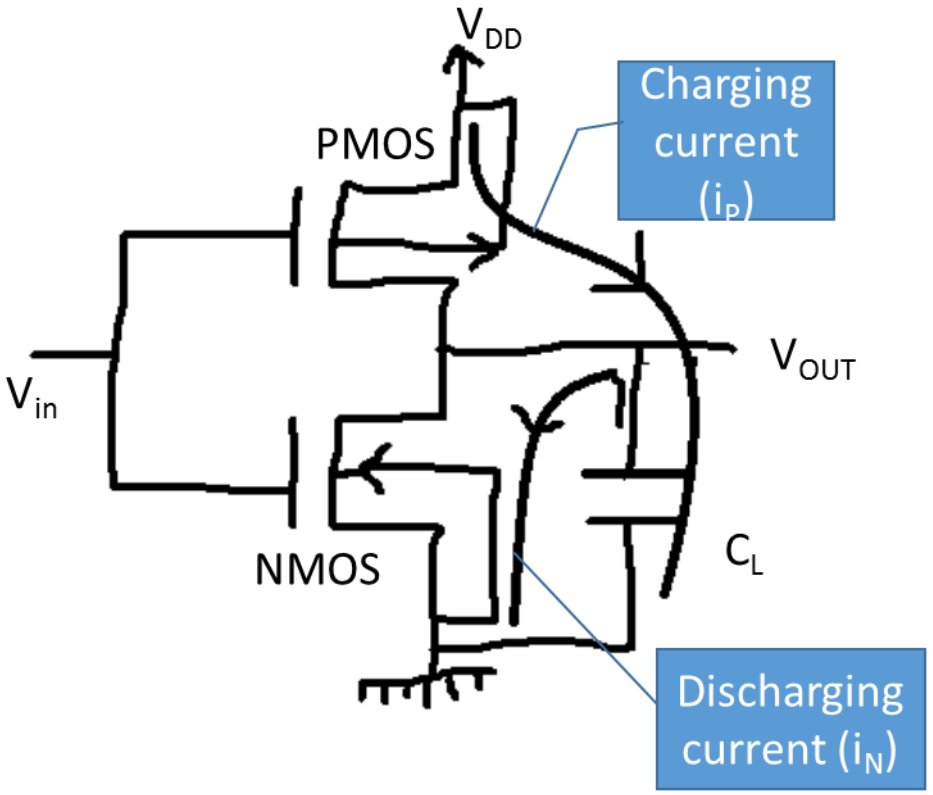


Fig 2.2.2 charging and discharging of output node of an Inverter

Switching power dissipation:

$P_{Switching} = P_{Charging} + P_{Discharging}$

Mathematically:

$$P_{Switching} = f \times C_{eff} \times V_{DD}^2 \quad \text{.....(8)}$$

Where, $$C_{eff} = \sum_{i=1}^{N} \alpha_i \times k_i \times C_i \quad \text{.....(9)}$$

α_i switching activity of node i;

k_i swing range coefficient of node i;

C_i total capacitance of node i;

f clock frequency;

V_{DD} supply voltage;

N number of nodes in circuit.

Thus, $$P_{Total} = I_{Leakage} \times V_{DD} + I_{Short} \times V_{DD} + f \times C_{eff} \times V_{DD}^2$$

Moreover to reduce overall power consumption device should be optimized from fabrication level to application level.

CHAPTER3.

LOW POWER CIRCUIT DESIGN TECHNIQUE AND TIMING DEFINITIONS

3.1 INTRODUCTION:-

Technique to reduce power dissipation will discuss in this chapter. Conventionally dynamic power and static power dissipation are two main component of total power dissipation. Lots of circuit technique have been proposed for low power application in VLSI circuit design. Some of technique is better in static power dissipation while some are better in dynamic power dissipation.

3.2 LOW POWER DESIGN:-

In CMOS (complementary metal oxide semiconductor) circuit, dynamic power dissipation dominate static power dissipation. More precise power dissipation because of logic switching is 50% to 60% of total power dissipation, since it is depends on square of supply voltage, thus reduction in supply voltage is best way to reduce power dissipation. But working with low supply voltage with same threshold voltage also reduce noise margin of circuit. To maintain noise margin with in desired limit threshold voltage must also be made smaller. However, leakage current will be more for low threshold voltage VLSI component, since leakage current is exponentially depends on threshold voltage. Hence the threshold voltage of device need to be that minimize the net power dissipation.

Dynamic power dissipation depends on frequency of transition or probability of transition occurrence. To reduce the transition (dynamic) power dissipation for higher transition probability, corresponding low supply and threshold voltage need to be choose. However, in reality for low transition probability, increase in static power dissipation may larger than reduction in dynamic power dissipation.

Power-delay product is reduces as the supply voltage increases but delay of circuit increases for CMOS logic circuits. Hence the value low supply voltage is choses such that overall power-delay product is optimized for all applications. Delay can be compensated by changing device ratio, doping profile for low supply voltage.

3.3 TECHNIQUES TO REDUCE LEAKAGE POWER:-

In active mode of operation total power dissipation includes dynamic and static power dissipation. When the device in off state, power dissipation in because of standby leakage current. So it is necessary to reduce the static power dissipation component. Static power can be using following technique:

1. Transistor stacking [25]
2. Multi V_{th} technique [24]
3. Dynamic Vth technique [26]
4. Scaling of supply voltage [27]

3.4 TECHNIQUE TO REDUCE DYNAMIC POWER DISSIPATION:-

As described in equation (8) dynamic power directly depends on supply voltage, transition frequency, switching activity, and node capacitance. Variation in these parameters also altered the dynamic power dissipation. In view of reducing dynamic power component following method can be applied:

1. Supply voltage scaling [12]
2. Node capacitance reduction [20]
3. Reduction in frequency [13]
4. Reduction in switching activity [13]

3.5 TIMING CHARACTERIZATION FOR FLIP-FLOPS:-

Clock and data timing is very crucial to flip-flops. Input clock period must be decided as described in paper [11]. Similar condition also applicable on data timing, data provided as input to flip-flop must be hold for setup time and hold time. Further clock period $T_{ckl} \geq t_{pd} + t_s$, where T_{ckl} is clock period; t_{pd} propagation delay of flip-flop; and t_s is setup time of flip-flop.

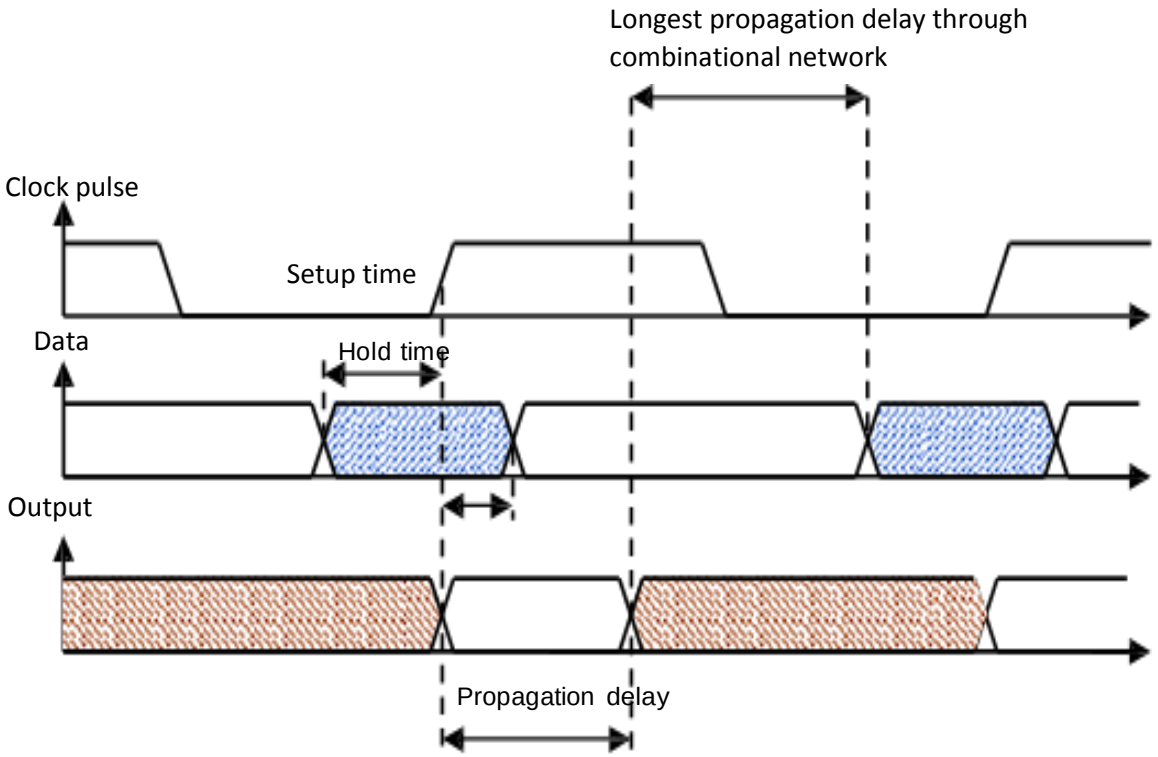


Fig 3.5 Timing definition

3.5.1 SETUP TIME:-

Data must be stable before clock appeared to the flip-flop. Thus setup time is the minimum time difference between data and clock so that data is perfectly transfer to the output without any error.

3.5.2 HOLD TIME:-

Input data must be hold for minimum time after the clock to be recognize by device (flip-flop), this minimum time is define as hold time.

3.6 STABLE, METASTABLE AND FAILURE ZONE:-

Stable, metastable and failure zone is described in paper [xx].

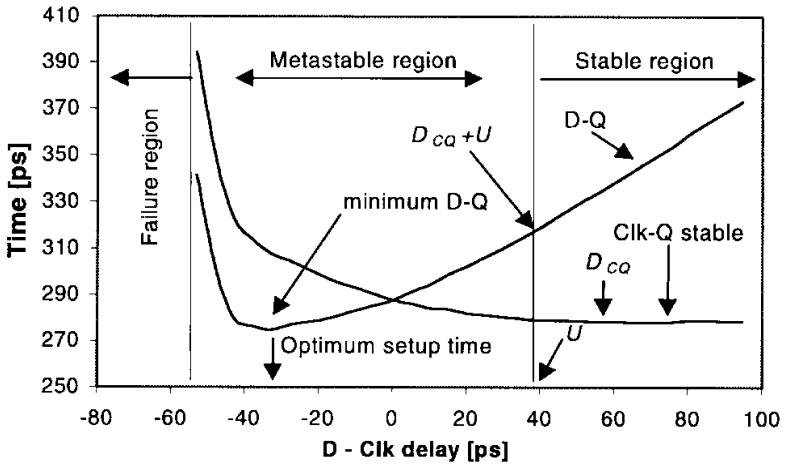


Fig 3.6 Stable, metastable, and failure zone for flip-flop

Stable region is the region of the Data-Clock (the time difference between last change in data and corresponding clock latching edge) axis in which clock-output delay do not depend on data-clock delay.

The region in which clock-output delay rises exponentially with respect to data-clock axis, define as **metastable region** [21].

In **failure zone**, change in data cannot transferred to the output of flip-flop. Setup time is part of stable region, and represented by point from where stable region starts.

However, propagation delay (t_{pd}) of flip-flop is define as maximum time difference clock edge and corresponding output. In order to work correctly, clock period and data timing must be satisfied different timing issues as described above.

Chapter 4:

DESIGN OF DUAL EDGE TRIGGERED FLIP-FLOP

4.1 BRIEF INTRODUCTION:-

As defined in chapter 1, dual edge triggered flip-flop (DETFF) transfer input data to output on both edge (+ve edge and –ve edge) of clock pulse. Many of survey have been done in order to make DETFF. The simplest way to make DETFF is to add –ve edge and +ve edge triggered flip-flop in parallel and operate on opposite phase of clock, as illustrated in Fig.4.1.(A).

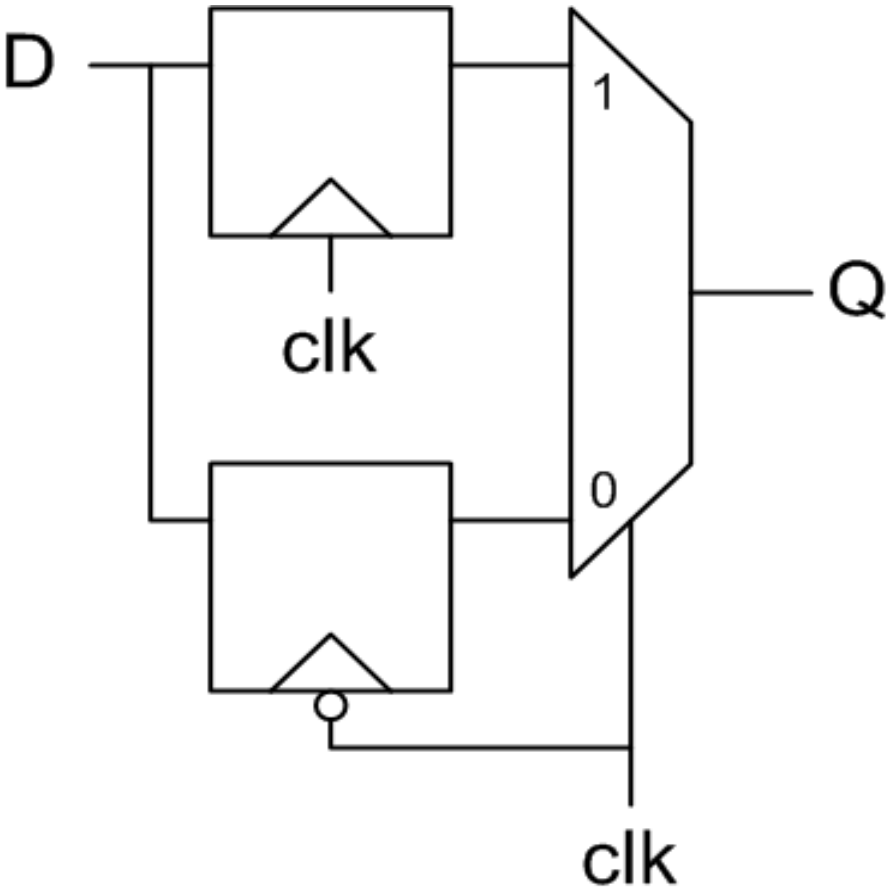


Fig 4.1.(A) Simplest way to make DETFF

In this thesis, we tried to make a DETFF which is improved version of DETFF shown in paper [xx]. The idea is very simple, first generate the short time pulse at each edge of clock pulse then used these short pulse to trigger the pass gate or transmission gate which is connected to input Data, finally a latch circuit is used to store the output data.

In order to make pulse generator, a delay producer circuit (four inverters connected serially) and a XOR/XNOR logic circuit is used. Fig.4.1.(B) shows the block diagram for DETFF discussed in this thesis.

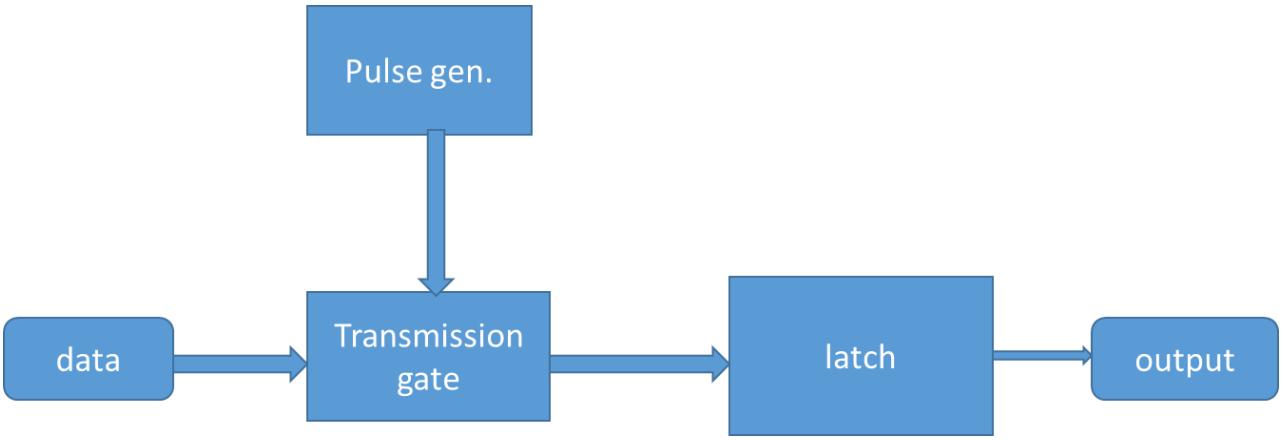


Fig 4.1.(B) Block diagram for DETFF

Working and detailed description of circuit inside the block diagram is discussed in following section.

4.2 CONVENTIONAL DETFF:-

Fig.4.2.(A) shows schematic diagram of conventional DETFF [xx]. Inverters I1, I2, I3, I4 used to produce delayed clock pulse. If each inverter have τ_i sec propagation delay then input clock pulse is skewed by $4\tau_i$ sec that is signal y, and signal x is inverted form of input clock pulse having delay of $3\tau_i$ sec.

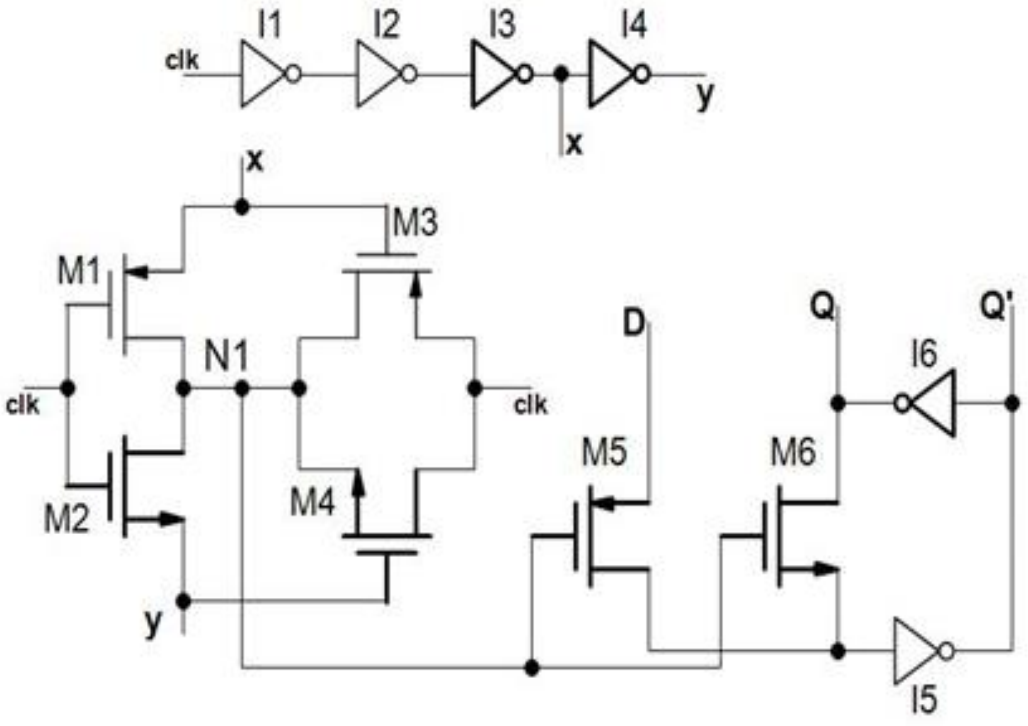


Fig 4.2.(A) Schematic of conventional DETFF

Inverter shown in bold have higher threshold voltage. MOS M1, M2, M3, M4 are connected such that node N1 = clk Θ y, this is shown in Fig.4.2.(B). ***When clk transit from 0 to 1***, M2 goes ON (M1 goes off, M3 will ON after $3\tau_i$ sec and M4 will ON after $4\tau_i$ sec) and N1 discharged through M2 for $4\tau_i$ sec since signal y = clk(t-$4\tau_i$), after 4τi sec N1 charged through M1 and M4. And ***when clk transit from 1 to 0***, M1 goes ON (M2 goes off, M3 will off after $3\tau_i$ sec, M4 will off after $4\tau_i$ sec) and N1 discharged through M1 and M3 and M4 for $4\tau_i$ sec (mostly discharged through M4), after 4τi sec N1 charged through M2 and M3. It is well known that nMOS (pMOS) is bad 1 transmitter and good 0 transmitter (bad 0 transmitter and good 1 transmitter). This is why, combination of M1, M2, M3, M4 used to provide good stability to logic levels. Thus N1 provides XNOR between clk and y.

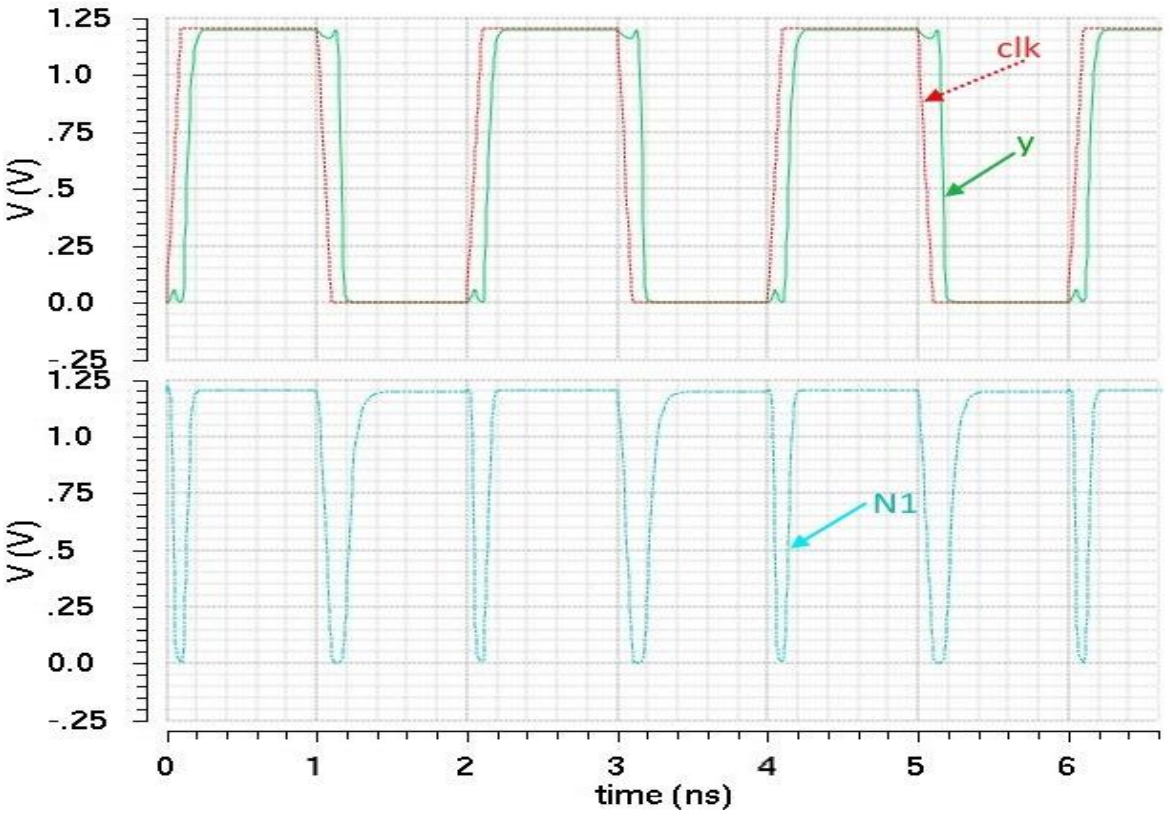


Fig 4.2.(B) N1 = clk Θ y

Input D is connected to M5. When N1 is at logic 0 (for $4\tau_i$ sec), D is getting transferred to output Q through M5, I5 and I6. And when N1 is at high logic, M5 goes off and M6 turns ON thereby output Q get latched.

4.3 PROPOSED_2 DETFF:-

Proposed_2 DETFF is little modification in conventional DETFF. Fig.4.3 shows its schematic. Proposed_2 DETFF utilizes transmission gate to pass the data to latch stage.

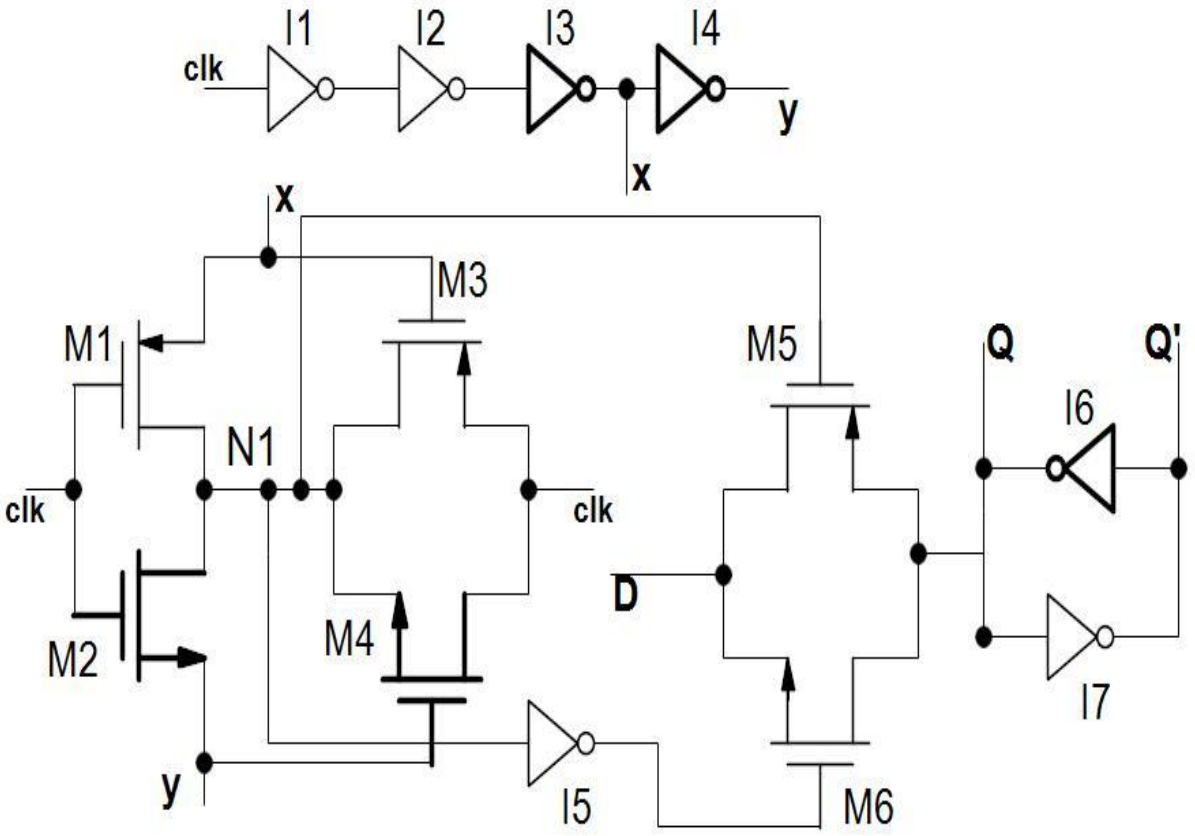


Fig 4.3 Proposed_2 DETFF

To active both MOS (M5 and M6) in transmission gate simultaneously inverter I5 is used. Here latching of data do not depend on level of N1. D is transfer to Q, when N1 is at logic 0 otherwise change in D do not affect output Q.

4.4 PROPOSED_1 DETFF:-

To generate sharp pulse from clock, a XOR logic is utilized in Proposed_1 DETFF. In this, I1, I2, I3, I4 is used to shift the clock by $4\tau_i$ sec where τ_i is delay provided by single inverter. Fig.4.4.(A) shows schematic of Propsed_1 DETFF.

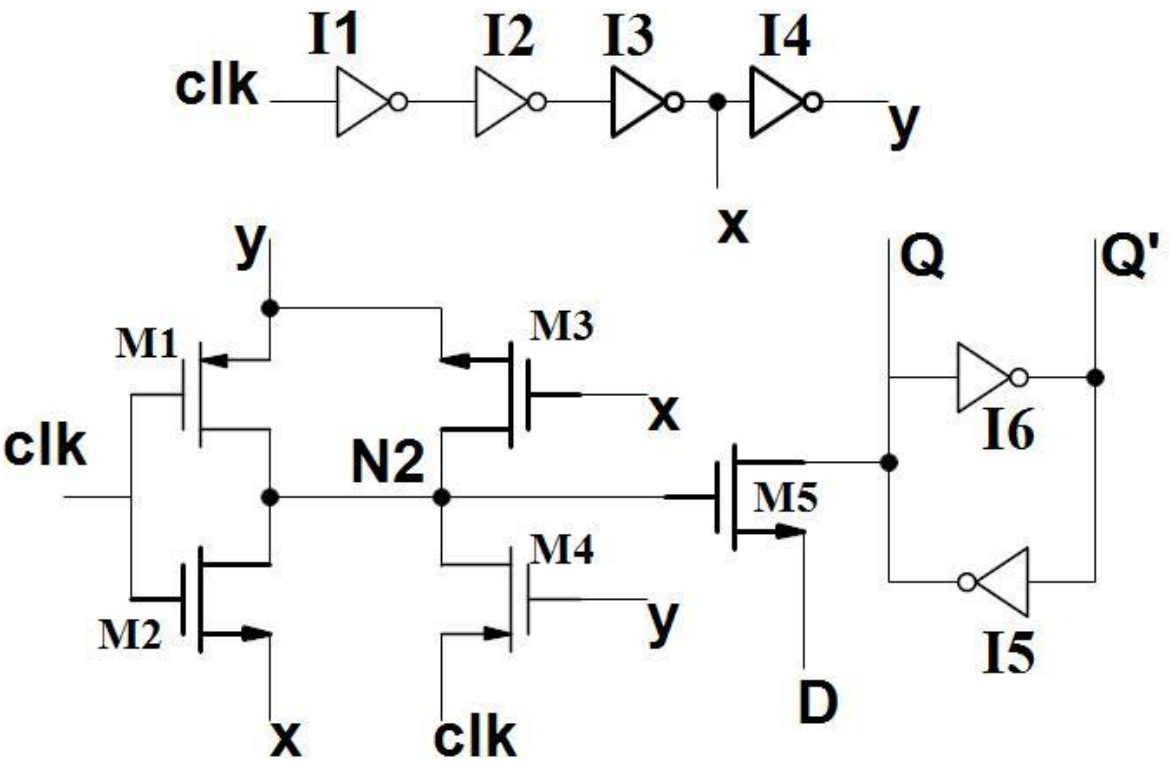


Fig 4.4.(A) Schematic of Proposed_1 DETFF

Here y = clk(t-4τ_i) and x = clk'(t-3τ_i). **When clk transit 0→1**, M2 goes ON, M1 goes off, M3 goes off after 3τ_i sec and M4 goes off after 4τ_i sec. N2 get charged through M4 for 4τ_i sec, however M2 also help to charge N2 for 3τ_i sec. And **when clk remains at 1,** then M2 ON, M1 off, M3 off, M4 off thereby N2 get discharged through M2. **When clk transit 1→0,** M1 goes ON, M2 goes off, M3 goes ON after 3τ_i sec, M4 goes ON after 4τ_i sec therefore N2 get charged through M1 for 4τ_i sec. And when **clk remains at 0** then N2 discharged through M1, M3, and M4 quickly. Thus at N2 a sharp logic high level (for 4τ_i sec) produced whenever there is transition in clk pulse otherwise N2 remains at logic zero. Hence N2 = clk $\oplus$ y. Pictorial view of signal at N2 shown in Fig.4.4.(B).

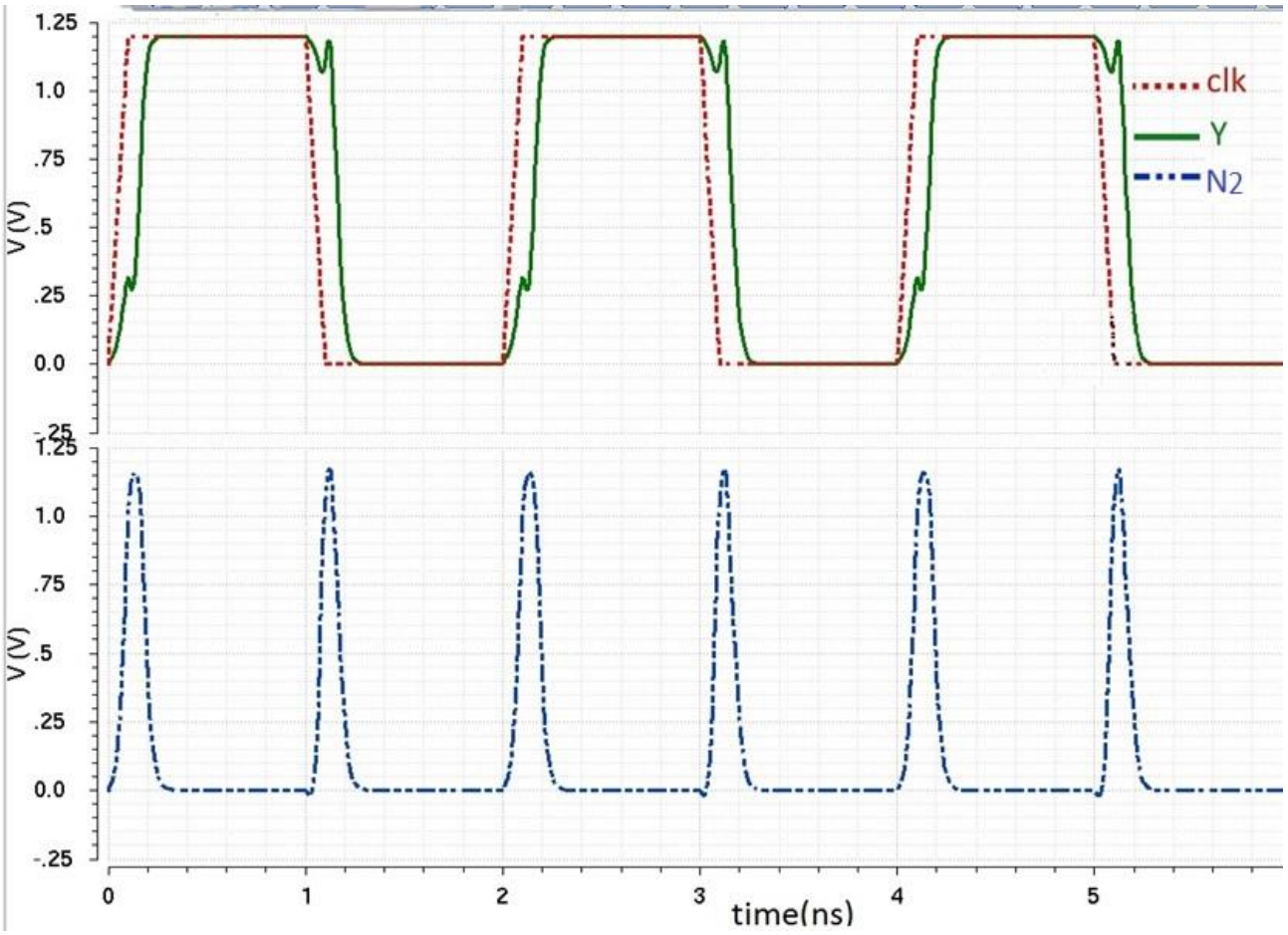


Fig 4.4.(B) Output from node N2

M5 get triggered when N2 is al logic 1 and data D get latched by I5 and I6. Note that when clk do not change its logic state, change in D do not affect output Q.

4.5 SIMULATION RESULTS:-

The proposed DETFFs and DETFF in [xx] were designed using gpdk 90nm CMOS technology and simulated by SPECTERE program. All simulation done at room temperature (300K) after considering RC effect of layout (known as post-layout simulation) for different supply voltages and different clock frequencies at fix data pattern. Comparison of simulated result are summarized in Table 1. Set-up time and hold time of DETFFs were found by method as described in [xx]. Different type of simulation waveform (i.e. power vs. supply voltage, delay vs. supply voltage, power vs. frequency and PDP vs. supply voltage) also shown in Fig.4.5.(A).

TABLE 4.5 COMPARISON OF DETFFs

Circuit used	Clock Freq. (MHz)	Power Supply (V)	tpd delay (ps)	Power (µW)	PDP (fJ)	t_{su} (ps)	t_{hl} (ps)
Conventional DETFF [3]	500	1.2	85.45	15.7	1.34	-2	150
	500	1.5	66.46	26.23	1.74		
	500	2	52.78	54.54	2.87		
Proposed_1 DETFF	500	1.2	76.52	16.84	1.34	20	75
	500	1.5	53.61	28.7	1.53		
	500	2	47.64	61.29	2.91		
Proposed_2 DETFF	500	1.2	61.93	15.46	0.95		
	500	1.5	48.17	26	1.27		
	500	2	34.62	54.32	1.87		

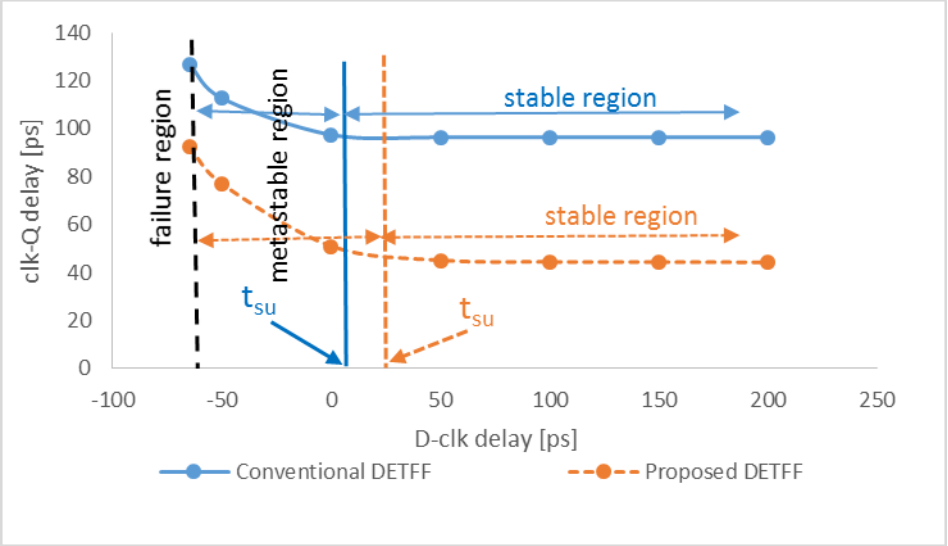


Fig 4.5.(A) Metastable, stable and failure zone

DETFF in Fig.4.2.(A) consumes more power since it have more number of transistor thereby have more area but have less propagation delay as compared to conventional DETFF shown in Fig.4.3.(A) because it don't have extra an MOS to latch the output unlike conventional DETFF. DETFF in Fig.4.4.(A) performs better in both areas (power and delay) also it have less chip area as compared to other two DETFFs described in this paper. This can be seen in Fig.4.5.(B) and Fig.4.5.(C).

Propagation delay is the delay between latching edge of clk to corresponding edge of Q. Here four types of conditions can be generated between clock to output Q, one is Q can be rise at falling edged of clock, second is Q can be fall at falling edge of clock, third is Q can be rise at rising edge of clock and fourth is Q can be fall at rising edge of clock. Finally propagation delay is calculated by taking average of delays for these four conditions. Set-up time and Hold time also described in Table 1.

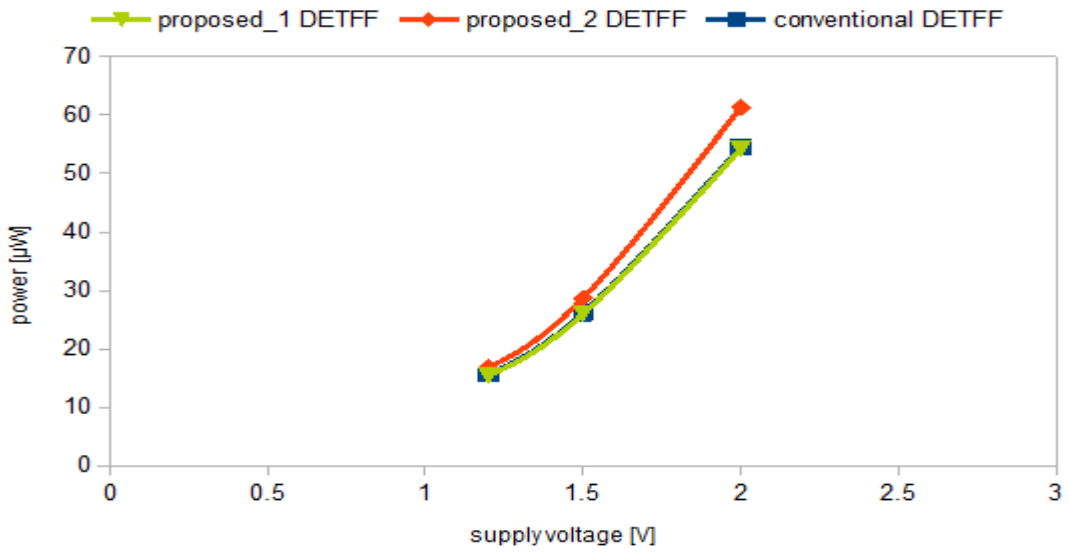


Fig 4.5.(B) Power vs Supply Voltage curve

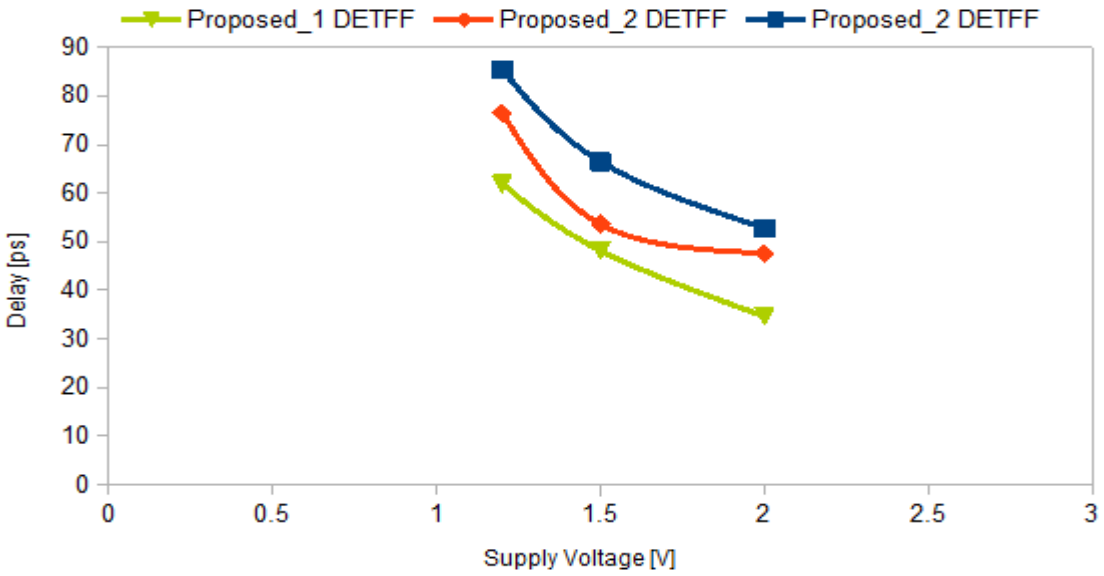


Fig 4.5.(C) Delay vs Supply Voltage

Conclusion

Two design of DETFF for low PDP were proposed in this paper. Proposed_1 DETFF uses pass transistor to transmit data whereas Proposed_2 DETFF uses transmission gate to do the same. In Proposed_2 DETFF, to transfer data through transmission gate one extra inverter has been used this increase area of layout as well as power consumption.

Proposed_1 DETFF consumed nearly equivalent power to conventional DETFF but work fast thereby overall PDP has been reduced. In case of proposed_2 DETFF to which consumed more power than conventional DETFF, but have less propagation delay. It shows considerable improvement in PDP only at 1.5 V supply voltage. In view of PDP Proposed_1 DETFF and Proposed_2 DETFF outperform conventional DETFF by 29% and 12 % at 1.5 V supply voltage respectively.

Future work

In field of low power VLSI device layout play major role in power consumption. Fully optimize layout results minimum power dissipation. Circuit used to generate pulse from clock pulse can also be design in new way (since this part of circuit consumed 70% power of overall DETFF). In future using low power high speed DETFF one can design hearing ads and FIR filter, high speed shift registers.

Appendix

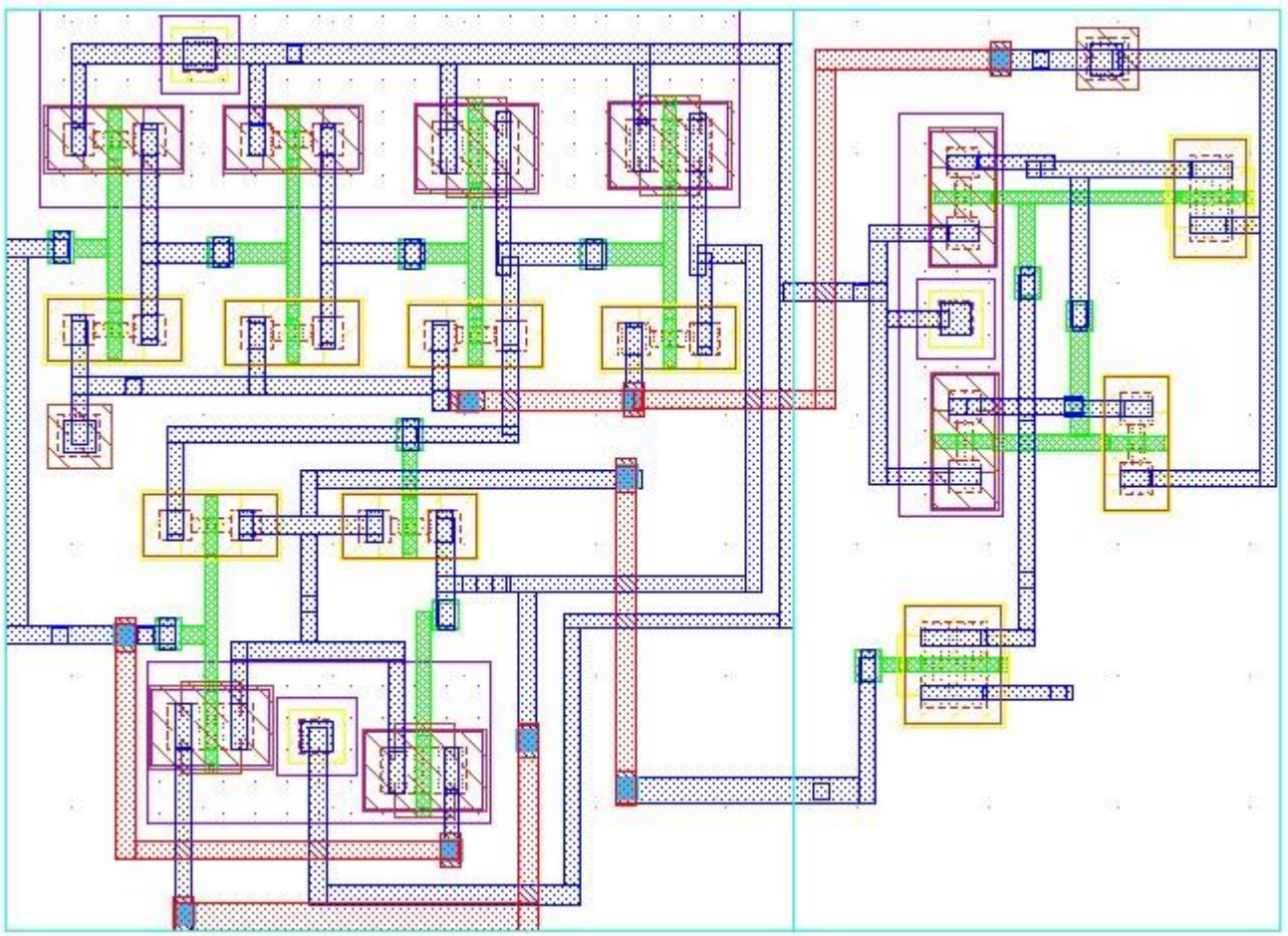


Fig A: Layout of proposed_1 DETFF

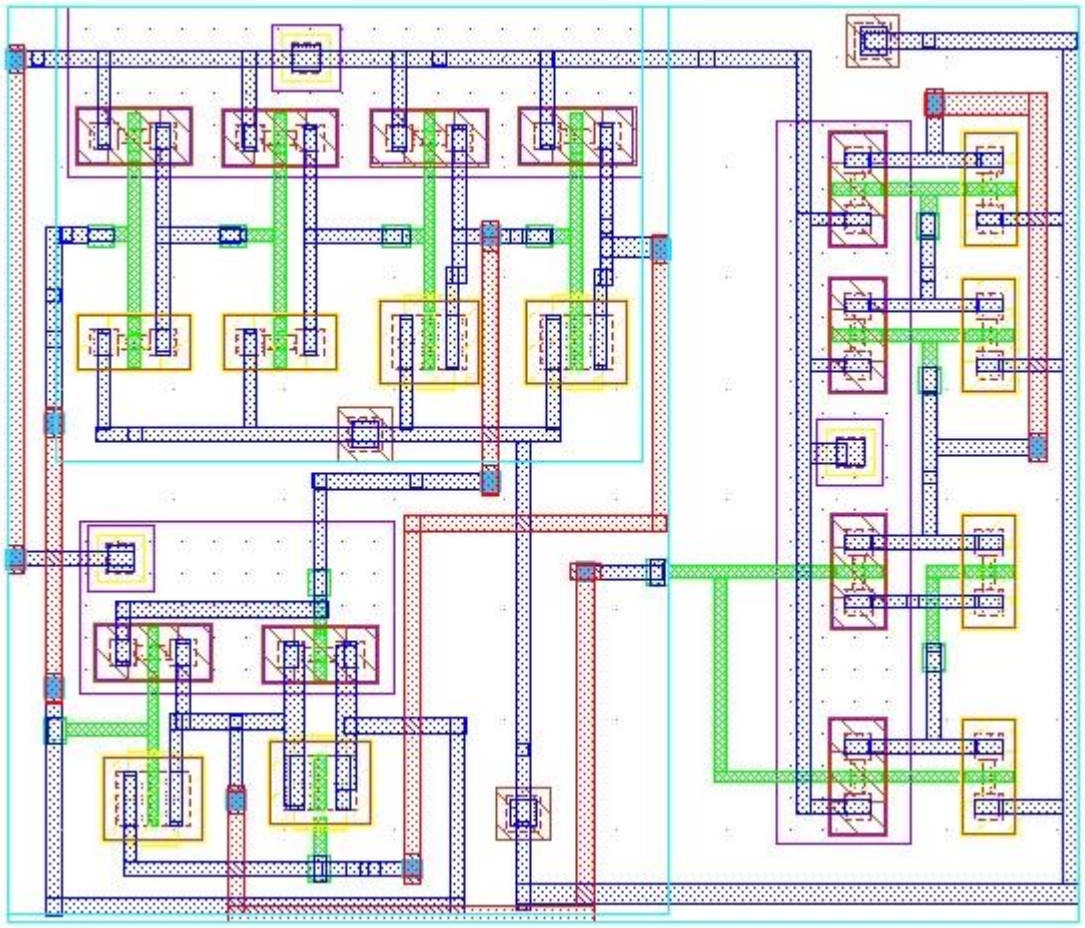


Fig B: Layout of proposed_2 DETFF

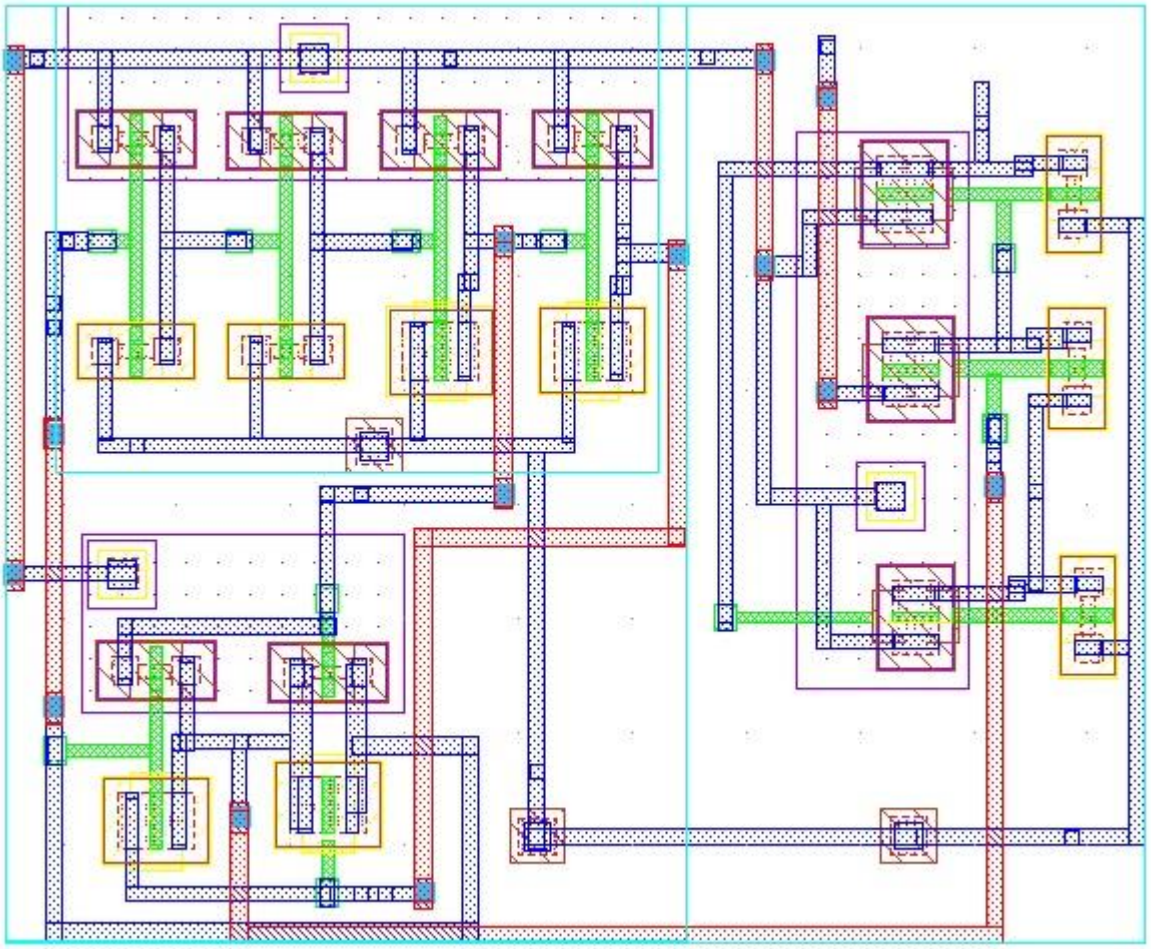


Fig C: Layout of conventional DETFF

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