Design and Development of Advanced Control strategies for Power Quality Enhancement at Distribution Level

Rajesh Kumar Patjoshi

Department of Electronics and Communication Engineering
National Institute of Technology
Rourkela-769008
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Design and Development of Advanced Control strategies for Power Quality Enhancement at Distribution Level

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By

Rajesh Kumar Patjoshi

Roll: 510EC907

Under the Supervision of

Prof. Kamalakanta Mahapatra

National Institute of Technology

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CERTIFICATE

This is to certify that the thesis entitled "**Design and Development of Advanced Control Strategies for Power Quality Enhancement at Distribution Level**", submitted to the National Institute of Technology, Rourkela by **Mr Rajesh Kumar Patjoshi,** bearing Roll No. **510EC907** for the award of the degree of **Doctor of Philosophy** in Department of Electronics and Communication Engineering, is a bonafide record of research work carried out by him under my supervision.

The candidate has fulfilled all the prescribed requirements.

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In my opinion, the thesis is in standard fulfilling all the requirements for the award of the degree of **Doctor of Philosophy** in Electronics and Communication Engineering.

Prof. Kamalakanta Mahapatra

Supervisor

Department of Electronics and Communication Engineering
National Institute of Technology, Rourkela, 769008
Odisha (INDIA)

Dedicated to

My Nation

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ABSTRACT

In recent times, power quality (PQ) issues such as current and voltage harmonics, voltage sag/swell, voltage unbalances have become the important causes for malfunctioning and degradation of the quality of power. Poor power quality severely affects on electrical equipment and finally results in significant economic losses. Hence, installation of the custom power devices to improve the power quality issues becomes an important consideration. Therefore, this thesis considers the enhancement of power quality for power distribution systems by utilizing unified power quality conditioner (UPQC). An UPQC can adequately handle several power quality problems such as load current harmonics, supply voltage distortions, voltage sags/swells and voltage unbalance. Therefore, the main focus behind this thesis is to develop advanced control strategies that improve the compensation capability of the UPQC so that power quality issues of distribution network are efficiently improved.

Firstly, the current harmonics are considered and are compensated by using the shunt active power filter (SAPF). Therefore, two control strategies such as Hysteresis current control (HCC) and Sliding Mode Control (SMC) based control algorithms are implemented to compensate current harmonics in the power distribution network. Furthermore, both the current control techniques utilize the Coulon oscillator based PLL (CO-PLL) for extraction of positive sequence signal from the supply voltage and generate the three-phase reference currents by employing PI-controller based DC-link voltage regulation. The performances of both current control techniques for SAPF are evaluated under different source voltage conditions such as balanced, unbalanced and non-sinusoidal.

The SAPF effectively compensates currents harmonic, however, it is unable to compensate voltage related problems. To overcome this drawback, this thesis considers the UPQC, which comprises with shunt APF and series APF, can be utilized to compensate both current and voltage related problems. The research on UPQC is carried out progressively by considering different advanced control strategies. Each progress in the research enhances the compensation capabilities of the previous UPQC control system. The simulation and real-time Opal-RT studies are carried out to verify the operating performance of each design concept of UPQC.

At first, operating principle and design of UPQC is presented and then a novel control algorithm is introduced with the aid of nonlinear DC-link voltage controller such as nonlinear variable gain fuzzy (NVGF) controller and nonlinear sliding mode controller (NLSMC) with modified synchronous reference frame (SRF) control strategy for improvement of both current and voltage compensation performance of the UPQC. However, existence of large settling time in dc voltage leads to poor dynamic performance of NVGF control technique and hence current harmonics, voltage distortions and voltage disturbance such as voltage sag/swell as well as voltage unbalance compensation capability of this technique is not quite effective in comparison to the NLSMC technique. Moreover, NLSMC is very sensitive to model mismatch and noise. It is quite sluggish in rejecting long drifting grid disturbances. Hence, a suitable control strategy has to be developed in UPQC, which has improved DC-link voltage regulation as well as tracking performance through load and grid perturbations.

To overcome this drawback a resistive optimization technique (ROT) incorporated with enhanced phase-locked loop (EPLL) based NVGF hysteresis control strategy and an optimum active power (OAP) technique combined with enhanced phase-locked loop (EPLL) based fuzzy sliding mode (FSM) pulse-width modulation (PWM) control strategy for UPQC have been discussed. ROT-NVGF and OAP-FSMC based UPQC control strategies are adaptive as well as robust and able to mitigate the PQ problems satisfactorily during all dynamic conditions of power system perturbation. However, performances of these controllers are not effective when there is a variation occurring either in the nonlinear load parameter or supply voltage parameter. Thus, UPQC may not be able to compensate PQ problems satisfactorily.

Considering aforesaid problems, this thesis proposes a command generator tracker (CGT) based direct adaptive control (DAC) applied to a three-phase three-wire UPQC to improve the current and voltage harmonics, sag/swell and voltage unbalance in the power system distribution network. CGT is a model reference control law for a linear time-invariant system with known coefficients and is formulated for the generation of reference signal for both shunt and series inverter. The main advantage of the proposed control algorithm is that no online extraction is needed to perceive the UPQC parameters. Moreover,

the adaptive control law is designed to track a linear reference model to reduce the tracking error between model reference output and measured signal to be controlled. Additionally, this proposed algorithm adaptively regulates the DC-link capacitor voltage without utilizing additional controller circuit. As a result, the proposed algorithm provides more robustness, flexibility and adaptability in all operating conditions of the power system network.

At last, model reference robust adaptive control (MRRAC) technique is proposed for single phase UPQC system. This control strategy is designed with the purpose of achieving high stability, high disturbance rejection and high level of harmonics cancellation. From simulation results, it is not only found to be robust against PI-controller, but also satisfactory THD results have been achieved in UPQC system. This has motivated to develop a prototype experimental set up in the Laboratory using FPGA (Field Programmable Gate Array) based NI (National Instruments) cRIO-9014. From both the simulation and experimentation, it is observed that the proposed MRRAC approach to design a UPQC system is found to be more effective as compared to the conventional PI-controller.

Contents

List of Abbreviations

ASD	Adjustable Speed Drives
AC	Alternative Current
ACVC	STATCOM AC Voltage Controller
ARTEMIS	Advanced Real-Time Electro-Mechanical Transient Simulator
ASVC	Advanced Static Var Compensator
ATC	Available Transfer Capability
AVR	Automatic Voltage Regulator
BFO	Bacterial Foraging Optimization
CGT	Command Generator Tracker
COTS	Commercial Off The Shelf
CPSO	Conventional Particle Swarm Optimization
CPD	Custom Power Devices
CSI	Current Source Inverter
DAC	Direct Adaptive Control
DC	Direct Current
DCVC	STATCOM DC voltage controller
DVR	Dynamic Voltage Restorers
DSP	Digital Signal Processor
EMT	Electromagnetic Transientcs
EPLL	Enhanced Phase-Locked Loop
FACTS	Flexible AC Transmission Systems
FLC	Fuzzy Logic Controller
FPGA	Field-Programmable Gate Array
GA	Genetic Algorithms
GTO	Gate-Turn-Off Thyristor
HDL	Hardware description language
HIL	Hardware-In-the-Loop
HVDC	High-Voltage Direct Current

IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
I/O	Input/output
ITAE	Integral of Time-Multiplied Absolute Value of Error
IWO	Invasive Weed Optimization
JTAG	Joint Test Action Group
MATLAB	Matrix Laboratory
MRRAC	Model Reference Robust Adaptive Control
MPC	Model Predictive Control
MSO	Mixed Signal Oscilloscope
MPLL	Modified Phase-Locked Loop
NLSMC	Non-Linear Sliding Mode Control
NVGFC	Nonlinear Variable Gain Fuzzy Controller
OAP	Optimum Active Power
ORC	Output Regulation-Based Controlle
PQ	Power Quality
PC	Personnel Computer
PCI-Express	Peripheral Component Interconnect - Express
PF	Power Factor
PID	Proportional Integral Derivative
POD	Power Oscillations Damping
PSB	Power System Block set
PSCAD	Power Systems Computer Aided Design
PSO	Particle Swarm Optimization
PCC	Point of Common Coupling
PSS/E	Power System Simulator for Engineering
RTOS	Real-Time Operating Systems
RTW	Real-Time Workshop
ROT	Resistive Optimization Technique
SLG	Single-line-to-ground

SAPF	Shunt Active Power Filters
SMPS	Switch-Mode Power Supply
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
SVM	Space Vector-Modulation
THD	Total harmonic distortion
TCP/IP	Transmission Control Protocol / Internet Protocol
TCPST	Thyristor controlled phase shifting transformer
TCR	Thyristor Controlled Reactor
TCSC	Thyristor Controlled Series Capacitor
TNAs	Transient Network Analysers
TSC	Thyristor Switched Capacitor
TVAC	Time-Varying Acceleration Coefficients
UPFC	Unified Power Flow Controller
UPQC	Unified Power quality Conditioner
VAR	Volt Ampere Reactive
VSI	Voltage Source Inverter
VUF	Voltage Unbalance Factor

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List of Symbols

i_1, i_h	Fundamental and harmonic current
i_S, i_L	Source and load current
C_{dc}	DC-link capacitor
$i_{S(abc)}, i_{S(abc)\_ref}$	Source and source reference Current
$i_{sh(abc)}, i_{sh(abc)\_ref}$	Compensating and reference Compensating Current
V_{ca}, V_{cb}, V_{cc}	Compensating Voltages
$V_{ca\_ref}, V_{cb\_ref}, V_{cc\_ref}$	Reference Compensating Voltages
A_1, f_1, ϕ_1	Fundamental amplitude, frequency and phase angle
u_a, u_b, u_c	Switching states
U_a, U_b, U_c	Unit vector template
L_{sef}, C_{ef}	Inductance and Capacitance of *LC* low pass filter
e_{pd}	Phase error signal of PLL
$\mathbb{S}_x$	Sliding surface
s_k	Switching function
V_S	Source voltage
V_{dc_ref}	Reference DC capacitor voltage
u_{eq}	Equivalent switching function
$\psi(y)$	Nonlinear function
f_c , f_{sw}	Switching frequency
F , P	Linear gain matrix and positive-definite matrix
$I_{\max}$, I_{Sp}	Peak value of source current

i_{Labc}	Load Current
ω	Angular Frequency
$\bar{\alpha}, k_2, y$	Positive constant value, gain matrix and DC-link voltage
HB, h	Hysteresis band
x, α	Design parameters of feed-forward compensator in EPLL
V_{at}, V_{bt}, V_{ct}	Optimal voltage signal
R_e	Optimum resistance value
I_{a1}, I_{b1}, I_{c1}	Optimal current signal
$\bar{P}_s$	Optimized active power
T	Sampling period
V_{Cf}, V_C	Voltage across filter capacitor
C_{sh}	Filter capacitance of shunt inverter
R_{sh}, L_{sh}	Filter impedance
R_s, L_s	Source impedance
K_p, K_i	Proportional and Integral constants of PI controller
V_L	Load voltage
V_{lp}	Peak amplitude of load voltage
r_{sa}, r_{sb}, r_{sc}	Step-input signals
$u_{msh(abc)}, u_{mse(abc)}$	Command input signals for shunt and series inverter
β	Tuning parameter of NLSMC method
m_a	Modulation index
y_p	Plant output
$y_{r(sh-se)}$	Model reference output

$e_{r(sh-se)}$	Tracking error
$U_{p(sh-se)}$	Control law for DAC method
$k_{xue(sh-se)}$	Adaptive gains of both shunt and series inverter
$k_{r(sh-se)}$	Adaptive gains concatenated matrix
$k_{p(sh-se)}, k_{I(sh-se)}$	Proportional gain and integral gain of DAC method
T_1, T_2	Time-invariant weight matrices
t_d	Dead beat time
$\delta(t)$	Dirac pulse input signal
u_{msh}, u_{mse}	Input signals for shunt and series inverter reference model
$u_{(sh-se)}$	Control law for MRRAC method
$k(t)_{sh-se}, l(t)_{sh-se}$	Estimated values for MRRAC method
γ_1, γ_2	Adaptive gains
g, h	Control gains for MRRAC method

Chapter 1

INTRODUCTION

1.1 Background

Widespread growth of power electronics based equipment at power distribution level, results in deterioration of the quality of electric power supply. High power loads such as arc furnace, variable speed driver, fluorescent lamps, microwave ovens, etc. present at industries and domestic are producing harmonics [1] in the power system networks. In contrast, the equipment initiating the disturbances is itself sensitive to the deviation of the supply voltage from its original value. On the other hand, reliability of the power supply also depends on a number of external factors such as lightning, large switching loads, nonlinear load stress and ground fault. Thus, power quality (PQ) problems [2] may be generated from the power distribution system or end user utility devices.

It has been reported in [3] that more than 30 % of power itself has been consumed by sensitive devices such as personal computer (PC), microprocessor, etc. and this percentage is still increasing in day to day. Thus, sensitive devices utilized in the end user environment (industrial and domestic) require high level of power quality and reliability systems. In fact, these devices require low-voltage direct current and are highly sensitive to short power interruptions, voltage surges and sags, harmonics, and other waveform distortions. Therefore, durability of these devices depends on the tolerant of the voltage fluctuations in the power supply. However, the electric power network is not able to provide the level of quality power needed by our computerized assembling sequential construction systems, information systems and our home appliances. Most of these equipments are susceptible to service interruption during poor power quality events.

Different health associations have demonstrated an increased interest in electric fields and stray magnetic, conveying rules on the levels of these fields [4]. Subsequently current generates magnetic fields; it is conceivable to reduce AC magnetic field by lessening harmonic currents existing in the power distribution line. Harmonic contamination on a power network line can be computed by a quantity known as total harmonic distortion

(THD). High harmonic distortion provides adverse effects on the power distribution system, and produces excessive heat in motors, creating early failure. Expanded operating temperatures can influence other equipment also, bringing about malfunctions and early failure. Furthermore, harmonics on the power network can provoke PC to restart and adversely influences other sensitive equipment.

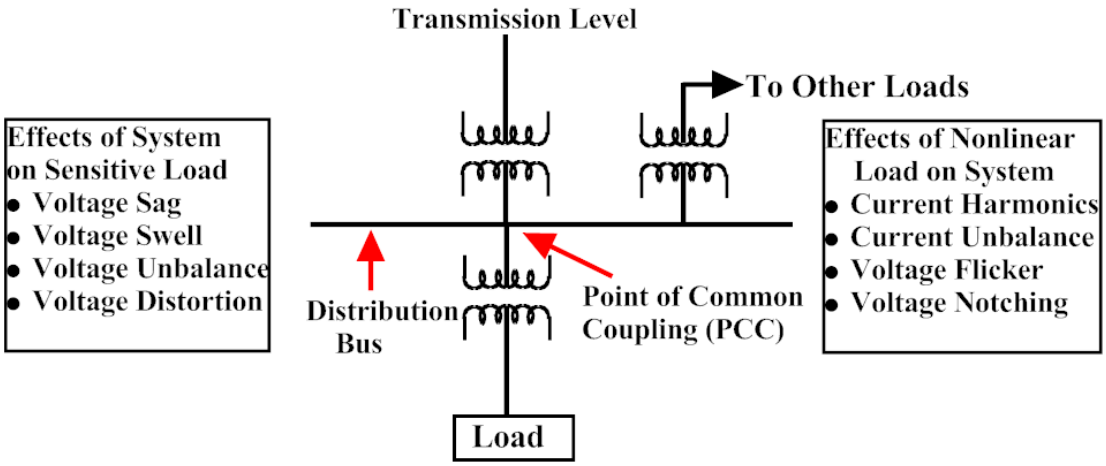
1.2 Power Quality issues

Power quality is a term that retains sinusoidal shape of power distribution line voltages and currents at rated magnitude and frequency. Subsequently, PQ issues are commonly used to express voltage quality and current quality. Additionally, these PQ problems are again classified into two main categories: first factor is the steady-state problems such as current and voltage harmonics; second factor is the transient problems such as load dynamic condition, voltage sag/swell, voltage unbalance and interrupts. Generally, voltage and current harmonics are considered as the most severe problems due to the advancement of nonlinear load, for example, rectifiers, switching power supplies and adjustable speed motor drives in distribution networks. Nonlinear loads cause injection of current harmonics into the distribution systems and subsequently degrade the quality of the network's voltage. On the other hand, voltage quality problem relates to voltage disturbances such as voltage sag/swell, voltage unbalance and voltage distortion caused by grid faults, due to which line voltage is deviated from its nominal value [5].

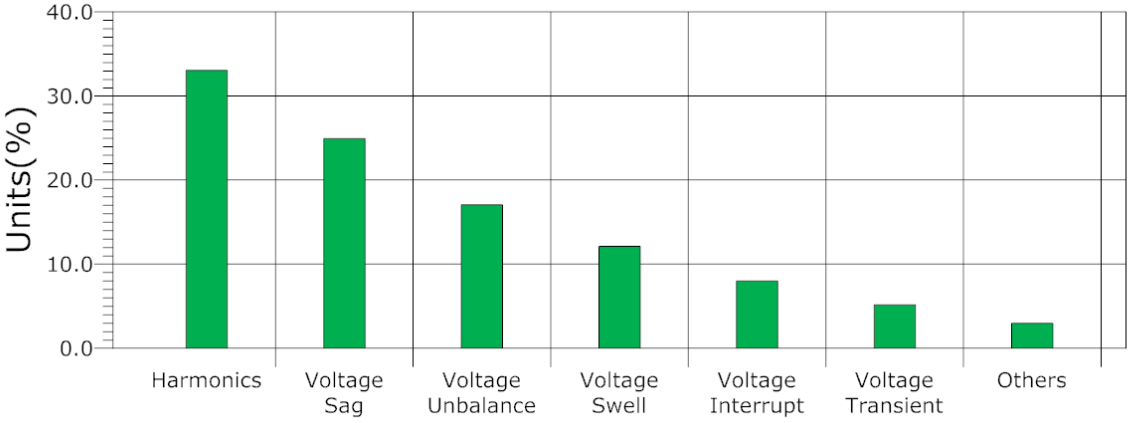
Fig.1.1 (a) shows the general power quality problems that may originate from the end-user power system such as harmonics and voltage disturbances. In addition, a survey [6] demonstrated in Fig.1.1 (b) reveals that current and voltage harmonics, voltage sag, voltage unbalance and voltage swells are the most general power quality issues intensely influenced by equipment operation. The more detailed explanation of these power quality issues will be specified in following sub-sections.

1.2.1 Current and voltage harmonics distortion

Harmonics are periodic steady-state signals that produce continuous distortion in the current and voltage waveforms and whose frequency differs from the fundamental frequency of the sinusoidal signal. Based on the multiplication factor, harmonics are divided into two main groups such as characteristics and non-characteristics.



(a)



(b)

Fig. 1.1. General power quality issues in an electrical system, (a) Schematic diagram, (b) Graphical representation.

Characteristic harmonics usually occur in the electrical system and its frequencies are an integral multiple of the fundamental frequency. When a harmonic order is equivalent to a non-integral multiple of the fundamental frequency, it is called non-characteristic harmonics. These are further sub-divided into sub-harmonics and inter-harmonics.

Harmonics whose frequencies are lower than the fundamental frequency are termed as sub-harmonics. On the other hand, harmonics whose frequencies are greater than the fundamental frequency but not its multiples are called inter-harmonics. The harmonic contents of the signals may be examined element by element. However, if the examined frequency band is varied, this requires a significant amount of work. The harmonic content of a signal may be represented by a single parameter. One method to do this is the calculation of the THD index, which is defined as follows:

$$THD = \frac{\sqrt{\sum_{n=2}^{k} I_n^2}}{I_1} \tag{1.1}$$

where I_1 is the rms value of the fundamental current component, $I_2 \ldots\ldots I_k$ are the rms values of the harmonic frequency current components and *k* is the ordinal number of the highest harmonic component. Eq. (1.1) presents the calculation of the current signal THD index; subsequently the THD index of the voltage signal can be calculated.

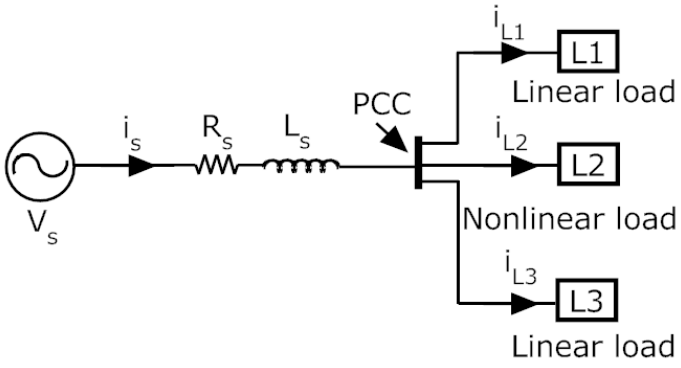


Fig.1.2 Schematic diagram of power system with linear and nonlinear load

Schematic diagram of power system with nonlinear load is shown in Fig. 1.2. The supply voltage V_S is connected to the load through the power line. Multiple loads are connected to the power line at point of common coupling (PCC). As shown, *L1* and *L3* are linear loads, and *L2* is nonlinear load. Consequently, *L2* draws distorted current from the supply, which contains harmonics current i_h as well as fundamental current i_1. Therefore, the supply current i_s will be,

$$i_s = i_{L1} + i_1 + i_{L3} + i_h \tag{1.2}$$

where i_{L1} and i_{L3} are current of load *L1* and *L3* respectively.

The cause of harmonics is the non-linearity of devices and loads that produce current harmonics. These devices are adjustable speed drives (ASD), AC/DC power supplies in domestic, industrial and commercial sector; switch-mode power supply (SMPS),

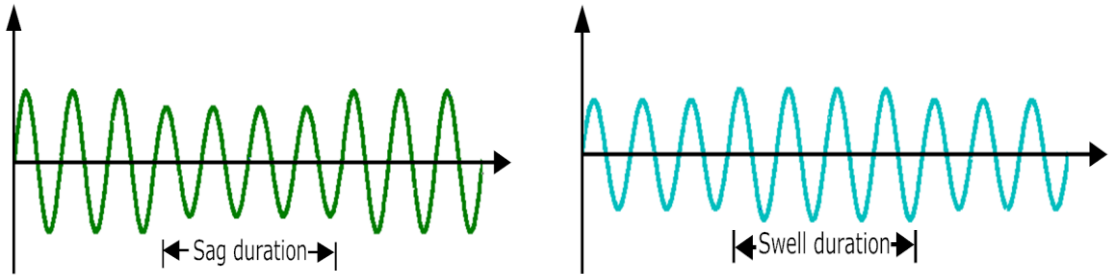
electronic ballast for discharge lamps. Harmonics produced by nonlinear loads have several destructive effects on network modules such as

- Producing voltage distortions at PCC that adversely affect other sensitive loads.
- Increasing power loss, resonances, saturation, winding vibration and decreasing life period of transformers.
- Operational difficulties on circuit breakers, protection relays, and fuses.
- Considerable increase of reactive power and heat on the capacitor.
- Production of pulsating and oscillating torques in turbines and generators.
- Errors in the energy meters and other measurement devices.
- Interferences in communication circuit and others electromagnetic interference EMI-related problems.

1.2.2 Voltage Sags

One of the power quality issues in the power systems is the supply voltage sags [7]. Voltage sag is characterized as a reduction in the rms voltage value between 0.1 and 0.9 per unit (p.u.) at the power frequency, for a span of half cycle to few second as shown in Fig.1.3 (a). Lightning, tree branch or animal contact, and insulation failures or human activity can create single-line-to-ground (SLG) or line-to-line fault. The relatively few customers near the fault will see a deep voltage sag. The magnitude of voltage sag is determined by the customer's distance to the fault location. This presence of voltage sags in the electrical system is a major issue since they may produce high financial losses. Subsequently, the resistance of every device against voltage sag depends on the span of the voltage sag and magnitude of the voltage during sag. Generally, the adverse effects produced by the voltage sags are,

- Tripping and resetting the domestic appliances and consumer electronic products.
- Restarting and shutting down of computerised controlled process industry.
- Speed and torque variation in the motor.
- Tripping of adjustable speed drives during function of voltage protection circuit.
- Flickering of light.



(a) (b)

Fig.1.3 Supply voltage sag and swell, (a) Voltage sag, (b) Voltage swell.

1.2.3 Supply voltage swell

A voltage swell is an increase of the supply voltage usually between 1.1 and 1.8 p.u. in rms voltage for duration from 0.5 cycles to 1 min as shown in Fig. 1.3(b). Voltage swells are almost always caused by an abrupt reduction in load on a circuit with a poor or damaged voltage regulator, although they can also be caused by a damaged or loose neutral connection. Voltage swells can adversely affect the performance of sensitive electronics equipment such as

- Equipment damage and reduction of equipment life
- Data errors in computer
- Shut down of equipment
- Degradation of power protection equipment

1.2.4 Voltage unbalance

A standard three phase supply consists of three phase signals of equal magnitude with a phase shift by 120^0. Any variation of magnitude and phase of one of the three signals will produce a zero phase sequence component and a negative phase sequence component. The expression of voltage unbalance factor (VUF) is defined as the ratio of the negative or zero sequence components to the positive-sequence component as follows.

$$\%\text{VUF} = \frac{\text{Maximum deviation from average voltage}}{\text{average voltage}} \times 100\%$$

Main reason behind the voltage unbalance is the irregular distribution of single-phase loads that can be consistently shifted over a three-phase power system. Some other reasons behind the power system voltage unbalance is the unequal transformer winding impedance,

open delta, and open wye transformer banks and voltage sags produced by grid faults in the power system. Unfavourable impacts of unbalanced voltages can be enumerated as follows:

- Motor efficiency can be decreased.
- Excessive heat on motor can cause early failure of motor.
- Small unbalance in the phase voltage can produce large unbalanced current.
- Rising current on one of the three-phases can provide a wrong operation to the protection circuit.

1.3 Solution to the Power Quality issue

Various power quality issues have been discussed in previous section. It can be assured that if no action is taken to compensate the above power quality issues, they will have great impact and effects in power distribution systems. However, PQ issues can be improved by utilizing active power filters and custom power devices (CPDs). Most common CPDs utilize shunt compensator or shunt active power filters (SAPF) [8-9], series compensator or dynamic voltage restorers (DVR) [10] and combination of these two (i.e., unified power quality conditioners (UPQC)) [11]. These CPDs are the viable choice for power quality improvement, as these equipments eliminate all the drawbacks of passive power filter and also provide adequate power quality solutions. Table 1.1 illustrates the typical power quality issues and their solution using CPDs.

1.3.1 Shunt compensator

Shunt compensator or SAPF are commonly connected across the load to compensate all current related problems such as current harmonics, reactive power compensation, load balancing and flicker reduction. It acts like a current source and injects compensating current at PCC to eliminate all current harmonics and make the source current sinusoidal and in-phase with the source voltage.

While developing shunt compensator [12] two types of converters can be used, these are voltage source inverter (VSI) and current source inverter (CSI). Fig.1.4 (a) depicts VSI based shunt compensator. It has a self-supporting dc bus capacitor. It has become more dominant since it is cheaper, lighter, and expandable to multilevel and multistep versions, to enhance the performance with lower switching frequencies. It is more popular in UPS based applications, because, in the presence of mains, the same inverter bridge can be used as a shunt compensator to eliminate harmonics of critical non-linear loads. The other converter

Table 1.1 Solution of power quality issues with CPD

Custom power device Topologies	Power Quality Issues	
	Caused by Load	Caused by Power supply
Shunt Compensator	Harmonic filtering Reactive power compensation Load balancing Flicker reduction	
Series Compensator		Voltage sag/swell compensation Voltage distortion compensation Supply voltage unbalance compensation
UPQC	Harmonic filtering Reactive power compensation Load balancing Flicker reduction	Voltage sag/swell compensation Voltage distortion compensation Supply voltage unbalance compensation

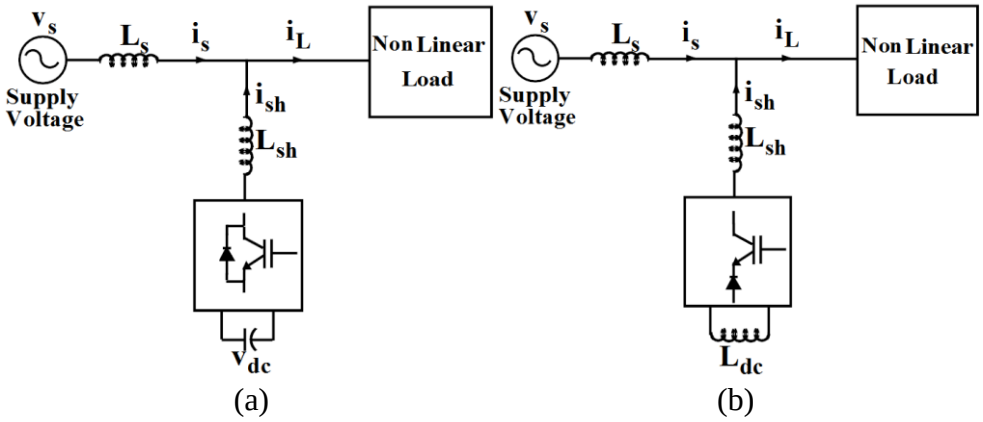


Fig.1.4 Shunt-connected power quality compensator, (a) Voltage Source Inverter, (b) Current Source Inverter.

used as a shunt compensator is a current-fed pulse width modulation (PWM) [13] inverter structure, as shown in Fig. 1.4 (b). It behaves as a non-sinusoidal current source to meet the harmonic current requirement of the non-linear load. A diode is used in series with the IGBT [14] for reverse voltage blocking. However, GTO-based configurations do not need the series diode, but they have restricted frequency of switching. They are considered sufficiently reliable, but have higher losses and require higher values of parallel ac power

capacitors. Moreover, they cannot be used in multilevel or multistep modes to improve performance in higher ratings.

1.3.2 Series compensator

Fig.1.5 shows the PWM converter connected in series with power line through series injection transformers. The series compensator or so-called DVR acts like a part of a controllable voltage source. This structure is most suitable for protecting load sensitive to supply voltage sag, swell, voltage distortion, and voltage unbalance [15].

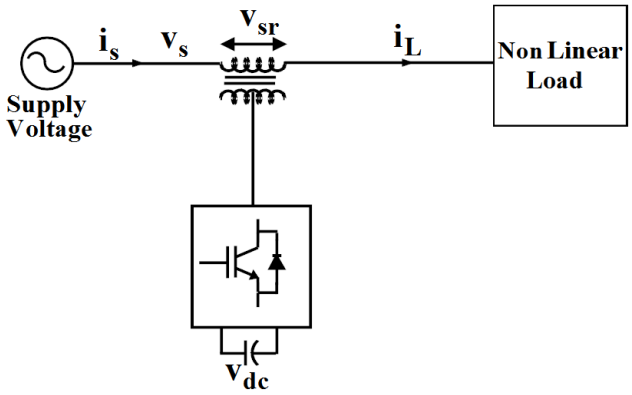


Fig.1.5 Series-connected power quality compensator

The power rating of series compensator is only a fraction of that of the load and the control response is in the order of millisecond, therefore guaranteeing a safe voltage supply under transient power network condition [16]. It has been utilized to reduce the negative-sequence voltage and voltage distortion present on the three-phase power line. In case of supply voltage fault, the series compensator is capable of feeding a certain amount of active power to the power line by extracting active power from dc-link capacitor and simultaneously, the shunt compensator takes the active power from the power line to regulate the dc-link voltage.

1.3.3 Unified power quality conditioner (UPQC)

Fig. 1.6 (a) shows the block diagram of UPQC, consisting of two voltage source compensators (series and shunt compensator) that are connected back to back through one common DC-link capacitor (C_{DC}). Series compensator is connected through transformers between the input supply voltage and the PCC. Shunt compensator is connected in parallel with common connection point through an interfacing inductor. The series compensator operates as a voltage source, while the shunt compensator operates as a current source.

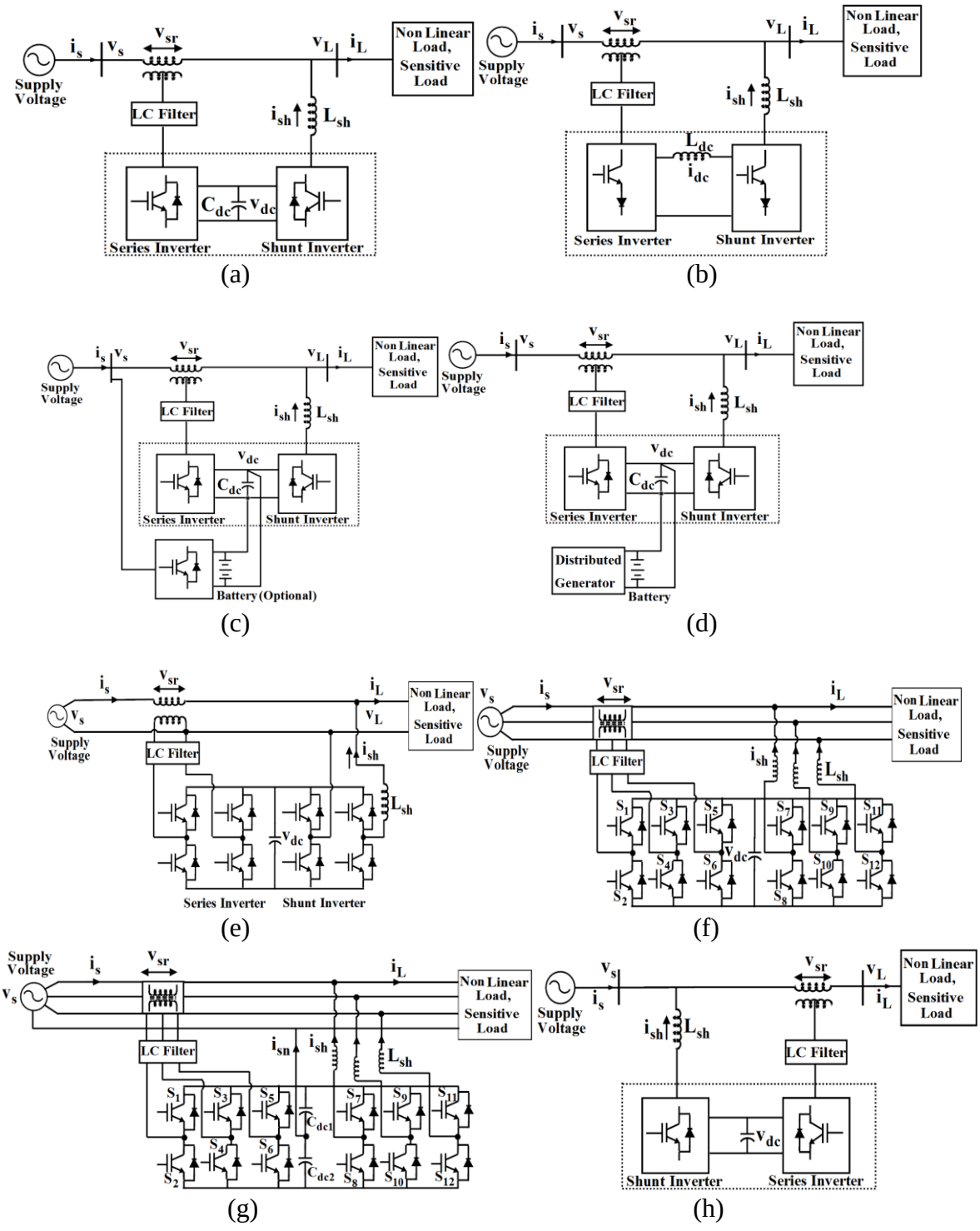


Fig.1.6 UPQC system topologies, (a) General block diagram representation of UPQC, (b) CSI-based UPQC topology, (c) UPQC-MC system topology, (d) UPQC-DG system topology, (e) 1P2W UPQC system topology, (f) 3P3W UPQC system topology, (g) 3P4W UPQC system topology, (h) UPQC-L system topology.

The main objective of the series converter is to mitigate voltage sag and swell and voltage distortion originating from the supply. The ac-filter (LC filter) are connected in each phase to prevent the flow of harmonic current generated due to switching [17]. The transformers connected at the output of each H-bridge inverter provide isolation between the series converter and power line and also prevents the DC capacitor from being shorted due to the operation of various switches [18]. The power circuit of shunt compensator consists of a three phase voltage source PWM converter that is supplied from C_{dc}. Shunt compensator is directly connected through a coupling inductor L_{sh}, which provides isolation between the shunt converter and power line. The objectives of the shunt compensator are to regulate the DC link voltage of both compensators and to suppress the load current harmonics.

The dc-link capacitor (C_{dc}) provides the common DC-link voltage of the series and shunt compensator. Ideally once charged, the DC-link voltage V_{dc} should not fall off its charge, but due to finite switching losses of the inverter-inductor and capacitor, some power is consumed and the charge of the DC-link voltage needs to be maintained in a closed-loop control, through the shunt compensator [19]. The switching devices used in both series and shunt compensator are IGBTs with anti-parallel diodes. As UPQC is used to tackle both current and voltage related problems, based upon physical structure and voltage compensation approach it is classified into different categories as follows.

- Type of energy storage device used.
- Number of phases used.
- Physical location of shunt and series inverter.

According to the energy storage device, the UPQC is classified as

- Current Source Inverter (CSI) based UPQC.
- Multiconverter based MC-UPQC.
- Distributed generator based DG-UPQC.

The UPQC is also constructed using a PWM-CSI [20] that shares the common DC-link energy storage in inductor L_{dc}. A voltage blocking diode is coupled in series with IGBT to realize this topology. Fig.1.6 (b) illustrates single-line demonstration of a CSI-based UPQC system structure. The dc current in the inductor is controlled in such a way that the average

input power is equivalent to the average output power in addition to the power losses in the UPQC. The CSI-based UPQC topology is not so popular because of its cost and higher losses.

The performance of UPQC can be improved by considering supplementary third converter unit to support the dc-link capacitor voltage [21] as shown in Fig.1.6 (c). To further enhance the system performance, the use of storage battery or super capacitor can be used. The third converter can be connected in different ways, for example, in parallel with the same feeder or in series/parallel with the adjacent feeder. Based on the literature [22] this topology is called multiconverter UPQC (MC-UPQC).

The UPQC can be combined with one or numerous distributed generation (DG) such as solar and wind energy systems [23].Thus, the system structure can be referred as UPQC-DG [24] and is demonstrated in Fig.1.6 (d). As presented in figure, the output of DG arrangement is connected to dc-link capacitor of the UPQC. The DG power can be regulated and managed through UPQC to supply to the loads associated with the PCC in addition to the voltage and current power quality problem compensation. Moreover, a battery can be attached to the dc-link, such that the additional DG power can be stored and utilized as a backup.

Fig.1.6 (e) illustrates the UPQC system topology of single-phase two-wire (1P2W) supply structure comprising of two H-bridge inverter [25]. This topology is one of the most popular UPQC system configurations to compensate the power quality problems in the single phase system. A three-phase three-wire (3P3W) VSI-based UPQC system topology is shown in Fig.1.6 (f). It is the most widely studied UPQC [26] because several nonlinear loads are fed from the 3P3W system. Apart from the three-phase loads, numerous industrial plants frequently comprise of combined loads, for example, selection of single-phase loads and three phase loads, supplied by the source. The existence of fourth wire, the neutral conductor, causes an unnecessary neutral current flow and thus, it demands a supplementary compensation requirement. Fig.1.6 (g) depicts the three-phase four-wire (3P4W) system configuration [27]. This topology comprises of two split capacitors on the dc side. The midpoint of the capacitor is utilized as a connection point for the neutral line.

All of the above UPQC represent so far is called UPQC-R system topology however Fig.1.6 (h) illustrates UPQC-L topology. Among two topologies, the UPQC-R [28] is the most usually used, whereas UPQC-L topology is sometimes utilized for exceptional cases such as, to avoid the interface between the shunt and passive filter.

1.4 Literature Review

1.4.1 Related Work on Shunt Active Power Filter

To acquire effective SAPF performance, it is significant to select both an appropriate current reference method and a suitable current control approach. As far as control is concerned, two loops can be identified. The first is utilized to compute the current reference injected by the filter and the second one should guarantee that the filter follow that reference adequately. Several control strategies have been reported in the literature for improving performance of SAPF and these are described below.

The instantaneous p-q method has been proposed in [29] for performance improvement of SAPF under unbalanced supply voltage condition, however, performance under balanced and sinusoidal conditions is satisfactory. A hysteresis-band PWM current controller is employed for generation of switching pulses and proportional integrator (PI) controller supervises the dc capacitor voltages. The resulting source currents are found to be sinusoidal, but voltage regulation performance is not satisfactory. A simple modification is proposed in [30] to develop a generalized p-q theory in active power filtering under the condition of distorted supply condition. The addition of phase-locked loop (PLL) with p-q approach helps in eliminating the adverse effect of the distorted supply voltage. The reference current signal is generated with help of direct and indirect current control technique and hysteresis current controller is used as a PWM generator. The SAPF system maintains a self-supporting DC bus voltage and it functions as a reactive power and harmonic compensator.

Yuan and Merk [31] reported a PI current controller using stationary-frame generalized integrators for current control of APFs. The instantaneous p-q theory is used for reference current generation and the sequence filter based on the positive sequence ideal integrator resolves the problems of the p-q theory under distorted or unbalanced PCC voltage

conditions. Extensive test results from a 10-kW prototype are demonstrated and the utility current is observed to be sinusoidal under both balanced and unbalanced loading conditions.

Synchronous-reference frame (SRF) method is proposed in [32] along with three independent two-level hysteresis comparators operating on a 3-phase VSC. Reference currents are derived directly from the load currents without considering the source voltages. Experimental results from a 2-kVA IGBT prototype showing the transient and steady-state system performance are presented, where the proposed method allows the operation of the SAPF in a large frequency range covering both 50 Hz and 60 Hz three-phase distribution systems and presents better harmonic compensation performance as compared to p-q based SAPF.

A fuzzy logic controller for a three level SAPF based on the p–q theory to identify reference currents have been implemented in [33]. The fuzzy logic control algorithm is proposed for harmonic current and inverter dc voltage regulation to improve the performance of the SAPF. The proposed SAPF has generated a sinusoidal supply current of low harmonic distortion of 0.9% and is in phase with the line voltage as obtained from simulation results. Tey and Chu [34] proposed artificial neural network (ANN) technique to design SAPF system. ANN algorithm computes harmonic contents and reactive power for the nonlinear load and these two signals are used for calculating the reference signal for the hysteresis control of a three phase IGBT based VSI.

Shyu proposed model reference adaptive control (MRAC) design for SAPF, in [35], to improve line power factor and to reduce the line current harmonics. The MRAC approach improves many failures of the fixed gain PI controller, such as undesirable undershoots and overshoots at the transient and non-robustness when changing loads. The proposed MRAC adaptive law is designed using Lyapunov's stability theory and Barbalat's lemma. It guarantees asymptotic output tracking. Furthermore, a prototype system was built to show effectiveness and to verify the performance of the system. An integration of predictive and adaptive ANN-based controller for SAPF has been presented in [36] to improve the convergence and reduce the computational requirement. An adaptive control strategy for SAPF for compensation of harmonic distortion, reactive power, and unbalanced load is proposed in [37]. In the proposed study, the amplitude of SAPF reference current is

generated by the dc-link voltage controller, based on the active power balance of the system. The current controller is implemented by an adaptive pole-placement control strategy integrated into a variable structure control scheme (VS-APPC) in which it introduced the internal model principle (IMP) of reference currents for achieving the zero steady-state tracking error.

A robust control strategy is implemented in [38] to regulate the dc-link voltage by combining a standard PI controller and sliding mode controller (SMC), which helps in generation of the reference current in SAPF. The SMC scheme continuously determines the gains of the PI controller based on the control loop error and its derivative. The chattering due to the SMC scheme is reduced by a transition rule that fixes the controller gains when steady state condition is reached.

1.4.2 Literature Review of Unified Power Quality Conditioner (UPQC)

In [39], the first UPQC structure was presented in 1998 by Fujita. The research on UPQC was mainly focused with two key groups: power circuits and control methods. The power circuit of the UPQC is based on physical structure, supply system, and applications [40]. In this thesis, we only emphasis on the operation and control of the UPQC in three-phase three-wire and single-phase system. Thus, the usual three-phase and single-phase VSIs are implemented for the shunt and series converter in the UPQC system. In contrast, control method takes a more imperative part in the performance of a UPQC. This section demonstrates a review on the control system developed in earlier UPQC system.

The control approach plays an important role in accomplishing good compensation performance of UPQC. Subsequently, UPQC consists of two separate converters, i.e., the shunt converter and the series converter, where each converter plays a different control objective. Hence, two separate control schemes should be established for these two converters.

- Shunt converter control: DC-link voltage regulation, current reference generation, and PWM signals generation for current harmonics compensation.
- Series converter control: Voltage sag/swell detection, voltage reference generation, and PWM signals generation for voltage compensation.

Numerous control methods have been employed to keep the DC-link voltage at a constant level. During the system dynamic conditions, such as, voltage sag/swell, sudden load change etc., the DC-link feedback controller must be executed instantly to stabilize the DC-link voltage to its reference value with a minimum time delay as well as lower overshoot .The complete power balance of UPQC operation is preserved by using DC-link capacitor voltage [41]. DC-link voltage regulation can be achieved by the conventional DC-link voltage feedback or PI control [42], fuzzy-logic controller [43], composite control [44], DC-link coupled to the battery energy storage system [45]. Super capacitor topology [46] and photovoltaic based dc-capacitor voltage regulation [47] are presented in UPQC. An adaptive DC-link voltage controller for UPQC is proposed in [48], which limits the DC-link voltage deviations during transients and assures negligible steady-state error. A reduced dc-link voltage without compromising its compensation capability is proposed in [49]. This topology also helps to match the dc-link voltage requirement of shunt and series inverter of UPQC. In [50], a linear quadratic regulator (LQR)-based self-charging circuit is proposed to regulate the dc-link voltage of the UPQC. In this technique, UPQC operates without relying on an external dc source.

A fast detection of grid perturbation with high accuracy and perfect generation of the reference signal are the key issues for good compensation of the PQ problems. Thus, the detection of grid perturbation such as sag/swell by monitoring $\sqrt{V_d^{\,2}+V_q^{\,2}}$ or V_d is the easiest method for voltage sag detection [51]. The other voltage sag detection methods are root mean square method [52], synchronous frame (d−q) detection method [53], and peak sequence analysis [54].

In addition to the voltage sag/swell and dc-link voltage detections, voltage, and current reference extraction control method also plays a significant role in the UPQC control technique. There are several reference extraction methods available in the literature, two most popular methods for UPQC are, three-phase $p-q$ theory [55] or instantaneous active/reactive power theory and three-phase $d-q$ theory [56] or synchronous reference frame technique. These approaches transfer the current and voltage signals from three-phase ($a-b-c$) frame to stationary reference frame ($p-q$ theory) or synchronously rotating frame ($d-q$ theory) for separating the harmonic and fundamental quantities present in the

signal. Instantaneous active and reactive powers are computed in $p - q$ theory, whereas, the $d - q$ theory contracts current independent to the supply voltage. The important mechanisms of these theories are that the real and reactive powers are converted to fundamental components, whereas distorted current or voltage is converted into dc-quantities. These quantities are extracted easily by utilizing a low-pass filter (LPF). Because of the dc signal extraction, signals filtering in the ($\alpha - \beta$) reference frame is insensitive to several phase shift errors presented by LPF. Due to the cut-off frequency of these HPF or LPF, dynamic performance of UPQC can be affected.

Unit vector template generation (UVTG) technique for reference extraction is given in [57]. In this technique phase-locked loop (PLL) is utilized for generation of unit vector templates for single-phase and three-phase systems. On the other hand, a finite impulse response filter method for extraction of reference signal during current and voltage perturbation is given in [58]. Ghosh and Jindal [59] have described a pole shift control technique for UPQC. In this technique, the closed-loop poles are selected by radially shifting the open-loop poles towards the origin.

Kesler *et al*.[60] proposed SRF based control strategy for the UPQC system. It is optimized without using transformer voltage, load, and filter current measurement, so that numbers of the current measurements are reduced and system performance is enhanced. Artificial Neural- network (ANN) based control technique is proposed in [61], in this technique the ANN is trained offline using data from the conventional PI controller. The online wavelet transformation-based reference signal extraction technique for UPQC is proposed in [62]. The basic approach used in this algorithm is to extract the fundamental component of load current and supply voltage by using wavelet-transform decomposition. Rong *et al*. [63] proposed an adaptive harmonic detection to exactly detect the voltage with multiple zero crossings.

There are numerous control methods existing in the literature, which are effectively applied to UPQC systems for current and voltage regulation. The $H\infty$-based model is employed to control the tracking behaviour of the inverter output waveforms for an effective and robust performance of UPQC [64]. Kamran and Habetler [65] have introduced a control technique based on deadbeat control in which the UPQC inverter combination is treated as a

single unit. The use of Particle swarm optimization-based feedback technique has also been utilized to develop the controller for UPQC in [66]. This feedback controller has optimal performance in various operating condition and is robust to parametric uncertainties. Additionally, an ANN method can also be used for the multi-input multi-output control system effectively. Therefore, this technique can be utilized to develop the controller for the UPQC to compensate different voltage and/or current related problem [67]. Kwan and Lam [68] have presented an output regulation-based controller (ORC) with Kalman filter for optimum operation of the UPQC. The ORC is used to generate a control signal for the converters of UPQC in a coordinate manner and also provides periodic reference tracking. A new optimal control strategy for UPQC is presented in [69]. This strategy is based on feedback linearization control applied to both the converters of UPQC and control law includes a feedback compensator of the load current and network voltage variation.

Various PWM control techniques for inner current control loops within the inverter are proposed for UPQC systems, where the most popular and widely used PWM technique is the hysteresis control [70]. Hysteresis control is relatively simple and easy to implement. However, the inherent variation of switching frequency of the hysteresis control causes poor control performance of the UPQC. A novel adaptive hysteresis band current and voltage controller for UPQC are studied in [71] with the aim to have robust control of the output voltage of the series inverter and output current of the shunt inverter. The adaptive hysteresis current and voltage controller changes the hysteresis bandwidth according to modulation frequency, supply voltage, dc-link capacitor voltage and slope of the reference compensating current and voltage. However, this adaptive-hysteresis current-voltage controller produces some switching power losses due to high frequency, which is solved by adaptive-fuzzy-hysteresis current controller. F. Mekri [72] used fuzzy hysteresis band current and voltage control methods for UPQC, where the band is modulated by the system parameters to maintain the modulation frequency nearly constant. Different current and voltage modulation techniques for VSI are evaluated in [73]. Periodical-sampling controller, triangular-carrier controller, and hysteresis controller are utilized for PWM signal generation. The triangular-carrier controller provides best compensation technique and eliminates all PQ problems effectively. A model predictive control (MPC) has taken into account to generate the PWM signal for UPQC, which is proposed by Zhang *et al.* [74]. This

MPC technique can handle multivariable control problem and has comparatively simple online computations. A sliding mode PWM controller with constant frequency technique is utilized to control the series converter of UPQC in [75]. Authors in [76] suggest a novel space-vector-modulation (SVM)-based hysteresis controller. This method employs all benefits of the hysteresis controller and SVM method. The controller defines a set of space vectors from a region detector and a space vector chosen by main hysteresis controller is applied.

A review on UPQC summarizes that the control performance of UPQC strongly depends on the dc-link voltage control method, PWM technique as well as the voltage and current control methods. Regardless of rigorous study and development of control techniques for UPQC, the complex nature of the control methodology is the real challenge to accomplish a good performance of the UPQC. Furthermore, numerous control methods, which require a large number of current and voltage sensors and on-line parameter extraction techniques that give rise to difficulty in the implementation of UPQC. Hence, to overcome these problems, this thesis emphasizes on improving the control performance of the UPQC to adequately handle various power quality problems with advanced control strategies and simpler implementation methods.

1.5 Motivation for this research

Present civilization depends intensely on power. For example, people want the power to run office equipment, household appliances, manufacturing process, and electronic devices for day-to-day works and activities. Consequently, power has turned into an essential service and the nature of power directly affects the operation of electrical equipment. Hence, power quality issues of distribution systems have become an extra consideration by end users in last decades. Power quality issues can be characterized into two fundamental classes: the first is steady-state issues, for example, current and voltage harmonics, the second is transient issues, for example, voltage sag/swell, voltage disturbances, and interrupts. Generally, current and voltage harmonics are considered as the most serious issues because of the intensive growth of nonlinear loads, for example, adjustable speed motor drives, switching power supplies, and rectifiers in the power system. Nonlinear loads can produce current harmonics in the distribution network and consequently reduce the quality of voltage

in the power system. Furthermore, voltage disturbances, for example, voltage unbalance, and voltage sags/swells produced due to grid faults are additionally considered as costly power quality issues. These disturbances frequently malfunction in the electronic-based equipment that creates huge economic losses because of production loss and materials damage. Because of severe effects of poor power quality, enhancement of power quality in the power distribution network has turned into a mandatory requirement.

PQ can be enhanced by utilizing the CPD and power filters. Normal CPD can be considered as SAPF, dynamic voltage restorers (DVR), and UPQC. The SAPF are essentially used to alleviate current harmonics and reactive power created by nonlinear load, whereas the DVR is a series coupled voltage compensating device that protects sensitive loads from voltage sag/swell, voltage distortion, and voltage unbalance existing in the supply voltage. These compensating devices are viable solutions for PQ issues, however, they are separately used to manage either current related or voltage related power quality issues.

In the current scenario, UPQC has been familiarized as an innovative and powerful compensating device to simultaneously manage current and voltage related issues. The UPQC is an arrangement of a shunt compensator and a series compensator connected in back-to-back through a common DC-link capacitor. A UPQC can successfully compensate the numerous power quality problems, for example, voltage and current harmonics, voltage unbalance, and voltage sag/swell to protect sensitive loads and enhance the power quality in the power distribution network. The usage of the UPQC to enhance power quality in the power distribution network has been considerably increased over a last two decades and various studies on control of UPQC have been accomplished. This thesis emphasizes on developing advanced control strategies to increase the compensation capability of the UPQC so that the UPQC can successfully eliminate numerous power quality issues.

1.6 Objectives of the Thesis

From aforementioned research motivations, this thesis develops advanced control techniques for the UPQC to effectively manage different power quality issues, for example, voltage and current harmonics, voltage unbalance, and voltage sag/swell. The ultimate control objective is to preserve the supply current and load voltage as sinusoidal and

balanced in spite of the utilization of nonlinear load at the load side and disturbances in the supply voltage. The THD values of supply current and load voltage after compensation must be decreased to below 5 % to follow the IEEE 519-1992 standard. In order to achieve these targets, advanced control strategies are developed for both the shunt compensator and series compensator of the UPQC. Keeping above facts into consideration, the objectives of the thesis can be defined as follows.

- To implement a PWM-current control technique for voltage source inverter based shunt active power, which offers satisfactory current regulation, high efficiency, and fast transient response.
- To propose a nonlinear dc-link voltage control technique in terms of accuracy and fast convergence time for dc-link voltage regulation during grid perturbations such as voltage distortion, voltage sag/swell, harmonics, and voltage unbalance.
- To propose new SRF based control approaches for improving the dynamic performance of UPQC system.
- To develop reference signal generation scheme that can self-regulate the dc-link voltage of UPQC.
- To develop an advanced PWM-current and voltage controller strategy for generating the switching pulse to drive the shunt and series converter of UPQC.
- To propose high performance control technique in UPQC, which is not only robust against parametric variations of supply voltage and load, but also reduces the current and voltage tracking error to zero.
- To effectively compensate voltage sag/swell, supply voltage distortion, voltage unbalance and also the current harmonics in the power system distribution network.
- To simulate the proposed control techniques in MATLAB/Simulink and real-time simulation model in Opal-RT simulator.
- To develop a single-phase prototype experimental set up to verify the robustness of the proposed model reference adaptive control techniques in UPQC system.

1.7 Organization of the Thesis

There are seven chapters in this thesis that are organized as follows.

CHAPTER 1 introduces power quality issues with typical solutions to deal with these problems. In addition, different reference current generation approaches as well as current controller techniques employed in SAPF are reviewed. Further an extensive review on several control strategies of UPQC has been provided. Finally, the research motivation and objectives are outlined.

CHAPTER 2 describes the system configuration of shunt active Power filter (SAPF), characteristics of harmonics as well as compensation principle and the filter design with two current control techniques called Hysteresis current control (HCC) and sliding mode control (SMC). Both current control techniques utilized Coulon oscillator based PLL (CO-PLL) for extraction of positive sequence signal from the supply voltage and generates the three-phase reference currents considering PI-controller based DC-link voltage regulation. Performance of both current control methods of SAPF are evaluated under ideal, unbalanced and distorted supply voltage conditions. Both CO-PLL based HCC and SMC approaches are analysed and validated through MATLAB/SIMULINK followed by an experimental setup accomplished with real-time-hardware-in the loop (HIL) system, which comprises of OPAL-RT simulator.

CHAPTER 3 presents a novel nonlinear dc-link voltage controller with modified SRF based control philosophy for UPQC. At first, design of a nonlinear variable gain fuzzy-controller (NVGFC) with modified phase-locked loop (MPLL) based SRF control strategy is proposed for three-phase, three-wire UPQC system. Then, a non-linear sliding mode control (NLSMC) and a novel SRF control technique have been proposed for rapid extraction of reference signal with a new switching dynamics control strategy for UPQC to improve the PQ problem in power system distribution network. These proposed control strategies of UPQC are validated through MATLAB/SIMULINK as well as real-time HIL based OPAL-RT system and adequate results are reported after a comparative assessment with the conventional techniques.

CHAPTER 4 proposes optimization based reference extraction methods with novel PWM current and voltage control techniques for UPQC. Firstly, a resistive optimization technique (ROT) incorporated with enhanced phase-locked loop (EPLL) based nonlinear variable gain fuzzy (NVGF) hysteresis PWM control strategy for UPQC is implemented. Secondly, an optimum active power (OAP) technique combined with EPLL based fuzzy sliding mode (FSM) PWM control strategy for three-phase, three-wire UPQC system is

proposed. These proposed control strategies of UPQC are validated through simulation as well as real-time HIL based OPAL-RT system and adequate results are reported after a comparative assessment with the control structure described in chapter 3.

CHAPTER 5 proposes a high performance UPQC using command generator tracker (CGT) based direct adaptive control (DAC) strategy for improving the power quality in the three-phase three-wire power system distribution network. A CGT is a model reference control law for a linear time-invariant system with known coefficients and it is formulated for the generation of the reference signal for both shunt and series compensator. Additionally, the adaptive control law is designed to track a linear reference model to reduce the tracking error between model reference output and measured signal to be controlled. The proposed control strategy of UPQC is validated through simulation followed by an experimental setup accomplished with real-time-hardware-in the loop (HIL) based OPAL-RT system and satisfactory results are reported after a comparative assessment with the control structures discussed in chapter 4.

CHAPTER 6 focuses on the development of a single-phase experimental prototype set-up for UPQC system and verification with the novel model reference robust adaptive control algorithm. This proposed algorithm is developed in LABVIEW and configured in FPGA-based NI-cRIO-9014 device for generating the required switching signal. This FPGA is interfaced with the prototype set-up and host computer. This chapter provides the design of various modules of this prototype set-up such as a dc-link capacitor, shunt interfacing inductor, series low-pass LC filter, and voltage as well as current sensor circuit. Additionally, the development of sag/swell generation circuit, signal conditioning circuit, blanking circuit and photo-coupler driver circuit are provided in this chapter.

CHAPTER 7 describes the concluding explanations and suggestions for some future research problems as extensions of the work.

Chapter 2

Shunt Active Power Filter (SAPF) Design and Control

2.1 Introduction

In this chapter, current harmonic compensation due to the nonlinear load employing shunt active power filter (SAPF) has been focused. Generally, SAPF is utilized for current harmonics compensation by injecting equal-but-opposite harmonic compensating currents at the point of common coupling (PCC). For this situation, the SAPF works as a current source injection, and it injects the harmonic components produced by the load but phase shifted by 180° [77]. This principle is appropriate for any kind of load considered as a harmonic source. Additionally, with a suitable control technique, the SAPF would be able to compensate load power factor. Therefore, the source current remains sinusoidal and in phase with the supply voltage. The current compensation capability of the SAPF is shown in Figure 2.1 [78]. Fig. 2.1(a) displays the block diagram of SAPF and Fig. 2.1(b) represents the waveforms characteristics of source current with and without SAPF. The general structure of the SAPF usually comprises a voltage source inverter with a DC-link capacitor, interfacing inductor, in addition to the associated control circuit.

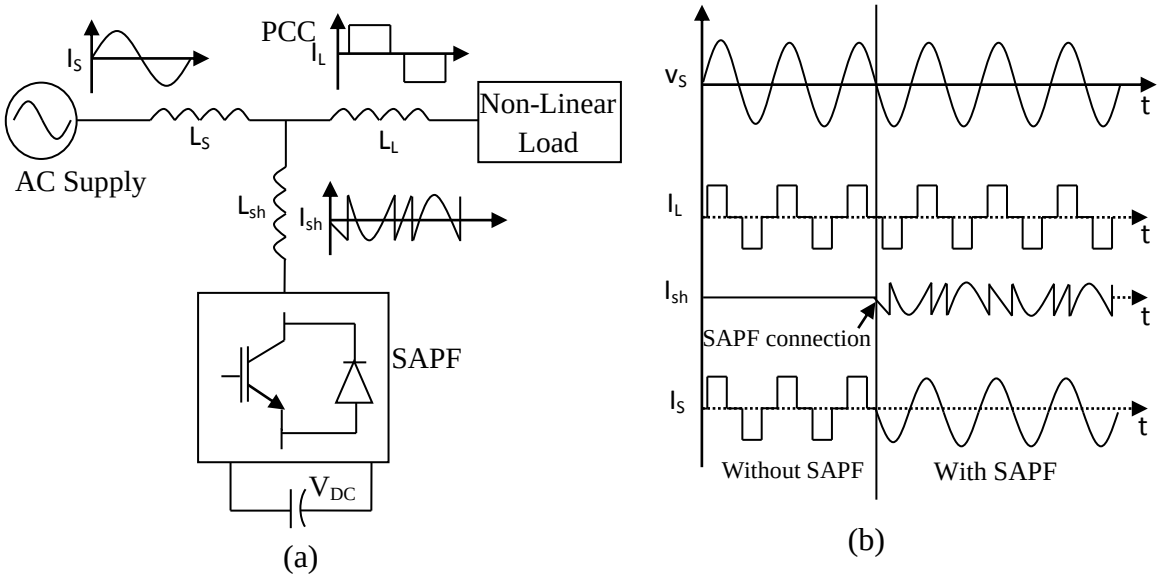


Fig.2.1 (a) Block diagram of shunt APF system, (b) Waveforms characteristic of SAPF

The compensation capability of SAPF is an important criterion. For perfect compensation, the controller must be capable of achieving the following requirements: i) extract and inject load harmonic currents, ii) maintain a constant dc link voltage, iii) avoid absorbing or generating the reactive power with fundamental frequency components. In order to keep satisfactory operation of the active filter [79], the peak value of the reference source current must be adjusted according to the real power drawn by the load from the supply side. This real power absorbed/released by the capacitor compensates the real power difference between the power consumed by the load and the power supplied from the source [80]. If the DC capacitor voltage is recovered and attains the reference voltage, the real power provided by the source is supposed to be equal to that consumed by the load again.

In this Chapter, the two control strategies such as Hysteresis current control (HCC) and Sliding Mode Control (SMC) based control algorithms are implemented to compensate current harmonics and reactive power in the power distribution network. Furthermore, both the current control techniques utilize the Coulon oscillator based PLL (CO-PLL) for extraction of positive sequence signal from the supply voltage and generate the three-phase reference currents by employing PI controller based DC-link voltage regulation. The performances of both current control techniques for SAPF are evaluated under different source voltage conditions such as balanced, unbalanced and non-sinusoidal. The performance comparison has been evaluated in terms of harmonic mitigation and DC-link voltage regulation. The complete simulation results utilizing MATLAB/SIMULINK software are presented to support the feasibility of proposed control techniques. To validate the control methodology, the system is employed with real-time hardware-in-the-loop (HIL) based OPAL-RT system, and adequate results are reported.

2.2 Design of the shunt APF system

Fig. 2.2 shows the three-phase three-wire SAPF and its interconnection to the power line through the interfacing inductor. However, numerous techniques are described for designing the SAPF system parameters. This section describes an idea of general procedures for obtaining the values of system parameter [81]. To design the SAPF, the following steps are considered.

a) Selection of SAPF rating;

b) Reference voltage required for DC-link voltage regulation;

c) Selection of interfacing inductor;

d) Selection of DC-link capacitor;

e) Control method employed;

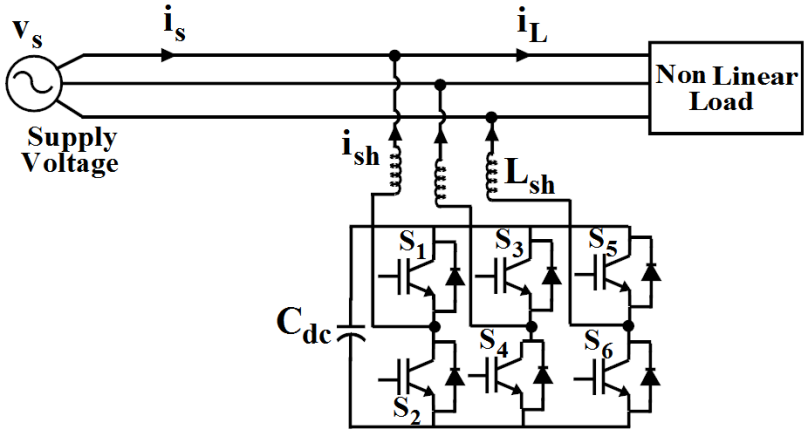


Fig.2.2 Three-phase three-wire shunt active power filter

a) Selection of Device rating:

The current and voltage rating of the device is dependent on the following consideration:

- Switching frequency requirement
- Maximum voltage sustaining limit of the SAPF during the OFF period
- Maximum current rating of the SAPF

Requirement of switching frequency: The high switching frequency should be required for compensation of both reactive power and harmonic currents. Generally PWM switching frequency is utilized ten times superior than that of the harmonic frequency to be compensated [82]. For reactive power compensation, 500 Hz would be sufficient. On the other hand, for harmonic compensation, when we need to compensate a 13^{th} harmonic we ought to utilize 6.5 kHz to compensate this high harmonic.

Maximum voltage sustainable limit: Considering the situation when S_1 being closed and S_2 being open, the maximum voltage blocked by the switch S_2 is equivalent to DC-link

voltage (V_{dc}). Therefore, the SAPF maximum blocking voltage rating is chosen slightly higher than V_{dc} so as to safely operate the SAPF.

Maximum current flow: Maximum current flows through the SAPF when both the switches S_1 and S_2 of one leg are closed together, and this current is equal to the maximum line current [83]. The maximum line current is same as the per phase current in a three-phase system. The maximum current flow is same for all the three legs of SAPF.

b) Reference voltage selection for DC-link capacitor:

The PWM-VSI is supposed to operate in the linear modulation mode $(0 \le m_a \le 1)$, and the amplitude modulation factor m_a is considered as [84].

$$m_a = \frac{V_m}{V_{dc}/2} \tag{2.1}$$

where $V_m = \sqrt{2V_{sh1}}$

Hence, $V_{dc} = 2\sqrt{2V_{sh1}}$ for $m_a = 1$. (2.2)

where V_{sh1} is the fundamental component in the ac-side of PWM-inverter and V_m is the peak value of fundamental component.

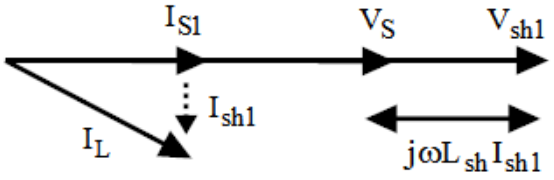


Fig.2.3 Vector diagram

According to the compensation principle, the SAPF regulates current I_{sh1} to compensate the reactive power of the load. If the SAPF completely compensates the fundamental reactive power of the load, then the supply current I_{S1} should be in phase with the supply voltage V_S and the compensation current I_{sh1} should be orthogonal to V_S as shown in Fig. 2.3. Based on the vector diagram,

$$V_{sh1} = V_S + j\omega L_{sh} I_{sh1} \tag{2.3}$$

The value of V_{sh1} should be considered according to the capacity requirement of the system. Based on the aforesaid analysis, the suitable range of V_{sh1} should be as follows.

$$V_S < V_{sh1} \leq 2V_S \tag{2.4}$$

If the value of interfacing inductor is small due to high switching frequency and the voltage V_{sh1} is approximately equal to the source voltage, then the equation (2.2) will be

$$V_{dc} = 2\sqrt{2V_S} \tag{2.5}$$

Suppose the approximation value of V_{dc} is 1.1 times more than the normal value of V_{dc}, then the dc- link voltage is regulated up to 10 % above the peak value of supply voltage. On the other hand, the required value of V_{dc} is reduced because of the sine reference for PWM is modulated through the third and ninth harmonics. The minimum essential voltage of V_{dc} is expressed in terms of the source voltage as:

$$V_{dc} = \frac{2\sqrt{2V_S}}{1.155} \tag{2. 6}$$

c) Selection of interfacing inductor:

The following requirements can be enforced on the estimation of interface inductor value.

- Passes compensating currents for reactive power and harmonics.
- Ensure filtering to a definite quality level of VSI output current and voltage source ripples.

First method: The design of interface inductor L_{sh} is dependent on the ability of harmonics current reduction and reactive power compensation. The inductor is additionally utilized to filter the ripples of the compensation current. For the sinusoidal PWM-VSI that expected to work in the linear modulation mode $0 \leq m_a \leq 1$, the maximum harmonic voltage arises at the frequency $m_f \omega$ [85]. Considering this harmonic content, the ripple current of the SAPF compensation current is given as

$$I_{shh} = I_{shh}(m_f \omega) = \frac{V_{shh}(m_f \omega)}{L_{sh}(m_f \omega)} \tag{2.7}$$

where, the subscript h represents the harmonic components and mf as the frequency modulation ratio of the PWM-VSI. For the measurable consideration, Ripple Attenuation Factor (RAF) is defined as

$$RAF = \frac{I_{shh}}{I_{sh1,rated}} \tag{2.8}$$

The three-phase reactive power Q_{sh1} can be calculated from the vector diagram shown in Fig. 2.3.

$$Q_{sh1} = 3V_S I_{sh1} = 3V_s \frac{V_{sh1}}{\omega L_{sh}}\left(1 - \frac{V_S}{V_{sh1}}\right) \tag{2.9}$$

By solving equations (2.7) and (2.9) simultaneously, the value of L_{sh} and V_{sh1} are calculated.

Second method: In this method peak ripple current is utilized for designing the interface inductor. For computing the ripple current, no-load condition is considered, and the effect of inductor resistance is supposed to be negligible. In this condition, the reference voltage of the VSI is equal to the supply voltage [86]. Thus, the required inductor is specified by the following equation.

$$L_{sh} = \frac{V_S}{2\sqrt{6}\, f_s\, \Delta I_{sh(p-p)\max}} \tag{2.10}$$

where $\Delta I_{sh(p-p)\max}$ is 15% of the peak compensation current.

d) Selection of dc-link capacitor:

The selection of DC-link capacitor is based on the principle of instantaneous power flow [87]. It is utilized for two significant purposes such as (i) preserves the DC-link voltage approximately constant with small ripples in steady state (ii) performs as an energy storage element to supply real power difference between load and source during the transient period. To maintain efficient operation of the SAPF, the peak value of reference current must be regulated to change the real power drawn from the supply. This real power charged/discharged by the capacitor compensates the real power consumed by the load. The selection of the value of dc-link capacitor is based on the stored capacitor energy released instantaneously to support the step increase or decrease in the power consumed by the linear or non-linear load.

First approach: The selection of the dc-link capacitor is dependent on the magnitude of instantaneous power flow on the dc and ac side of the VSI [88]. The design of C_{dc} can be governed by decreasing the voltage ripple. The dc-link capacitor C_{dc} is originated from rated active power line conditioner current $I_{sh1,rated}$ and peak to peak voltage ripple $V_{dr,(p-p)\max}$. It is defined as

$$C_{dc} = \frac{\pi * I_{sh1,rated}}{\sqrt{3}\,\omega V_{dr,(p-p)\max}} \tag{2.11}$$

Second approach: The real power demand of the load has to be supplied by the DC-link capacitor for one cycle of the supply voltage during the transient condition. Therefore, the capacitor value is expressed by the following equation [89].

$$C_{dc} = \frac{2E_{\max}}{V_{dc}{}^2 - V_{dc\min}{}^2} \tag{2.12}$$

where $E_{\max}$ is the maximum energy that the capacitor has to supply during the transient condition.

2.3 Active Power filter control strategies

Control approach [90] is the heart of the SAPF and is realized in three stages.

- In the first stage, the required voltage and current signals are sensed using current and voltage sensors.
- In the second stage, the reference signal in terms of current or voltage levels are derived based on control methods [91] and SAPF configurations.
- In the third stage of control, the switching signals for the SAPF are generated using hysteresis, sliding-mode based controllers.

The control of the SAPF is realized with analog and discrete components or innovative microelectronic devices such as Field programmable gate array (FPGA), Digital signal processing (DSP) etc. There are various published approaches that define the different topologies and different algorithms utilized for SAPF. In many of those, it generally overcomes the explanation of a single method but there are publications that explain and

compare couple of such techniques defining their advantages and disadvantages by providing final monitors as the dynamics, THD reduction, inverter efficiency or the cost of the entire SAPF.

Extraction of positive sequence signal from the supply voltage is one of the important considerations of SAPF control algorithms [90]. Conventional unit vector technique provides adequate performance in sinusoidal and balanced conditions. However, it produces improper reference currents when the supply voltage contains unbalance and distortions, resulting in inadequate harmonics compensation. The reference current is calculated by two steps: first is related to the calculation of the positive-sequence component of unbalanced supply voltage and second is deriving a simple fundamental extraction filter to extract the fundamental frequency component from the distorted positive-sequence voltage, hence increases computation time.

Therefore, a PLL based control strategy for SAPF is considered in this chapter, which is based upon the following facts.

1. A fast and accurate estimation of the fundamental component of the distorted supply voltage under consideration of grid perturbations, which helps in the generation of reference current signal for SAPF system.
2. A proper tracking of reference current signal employing suitable PWM current control techniques to enhance harmonic compensation performance of SAPF.

Keeping these facts into consideration, two control strategies namely Hysteresis current control (HCC) and Sliding Mode Control (SMC) are considered in this chapter, which are independent of all grid perturbations and make harmonic compensation effective in SAPF system. These control strategies are described in the subsequent sections.

2.4 Development of HCC/SMC based SAPF

Fig. 2.4 illustrates the control structure implemented for the three phase three wire SAPF using HCC and SMC. The SAPF is consisted of a DC-link capacitor C_{dc} and three-phase insulated-gate bipolar transistor (IGBT) inverter followed by an inductive output filter (L_{sh}, R_{sh}).

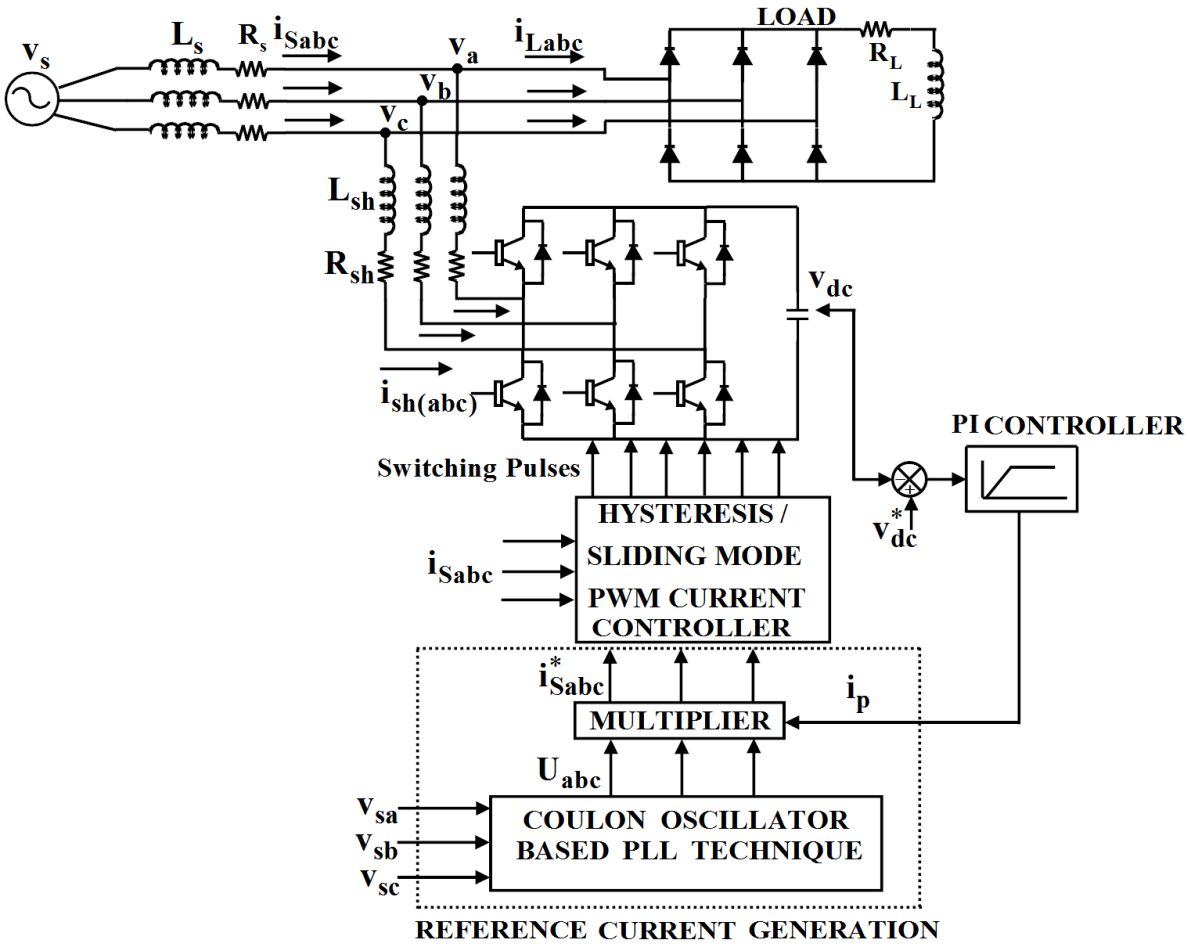


Fig 2.4 HCC/SMC based SAPF

The SAPF is designed to inject a current $i_{sh(abc)}$ (where suffixes *a, b* and *c* represent different phases) at the PCC to cancel the harmonic content of the source current i_{Sabc}, which results in a pure and sinusoidal source current i_{Sabc}. To achieve the aforesaid objective, PLL is utilized for generation of the positive sequence component (U_{abc}) in per unit magnitude of supply voltages. These are modulated with the output of proportional-integral (PI) controller i_P to generate references $\left(i^*_{Sabc}\right)$ for both the current controller.

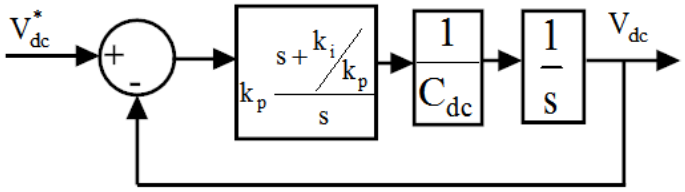


Fig. 2.5 Outer control loop for dc-link voltage control

An outer PI voltage control loop is used to set the proper magnitude of the source current, and the choice of PI parameters (k_p, k_i) are based on the closed loop control as shown in Fig.2.5. In order to regulate the DC-link voltage V_{dc}, the error $V'_{dc} = V^*_{dc} - V_{dc}$ is passed through the PI controller, which is expressed by the following equation.

$$V_{dc} = k_p V'_{dc} + k_i \int V'_{dc} dt \tag{2.13}$$

From the Fig.2.5, the closed loop transfer function of DC-link voltage regulation can be obtained as

$$\frac{V_{dc}(s)}{V^*_{dc}(s)} = \frac{s + \frac{k_i}{k_p}}{s^2 + \frac{k_p}{C_{dc}} s + \frac{k_i}{C_{dc}}} \tag{2.14}$$

where the proportional gain and integral gains are derived from $k_p = 2\delta\omega_n C_{dc}$ and $k_i = C_{dc}\omega_n^2$. The outer loop natural frequency ω_n is considered as the fundamental frequency of the supply voltage.

2.4.1 Reference Current Generation Technique

Usually, the performance of the SAPF depends upon the accuracy of the reference signal generator and for source reference generation, extraction of the positive sequence component is the most important consideration for determining the reference signal of SAPF. The expression for source reference signal is given by

$$i^*_{Sabc} = i_p \times U_{abc} \tag{2.15}$$

The extraction of the positive sequence component of supply voltages using CO-PLL algorithm is presented below.

2.4.2 Positive Sequence Signal extraction method using CO-PLL

The CO-PLL uses an algorithm that is based on the principle of Coulon oscillator [92]. Block diagram of the Coulon oscillator is shown in Fig. 2.6 and the input signal $x(t)$, which is harmonically rich, is given by the following expression.

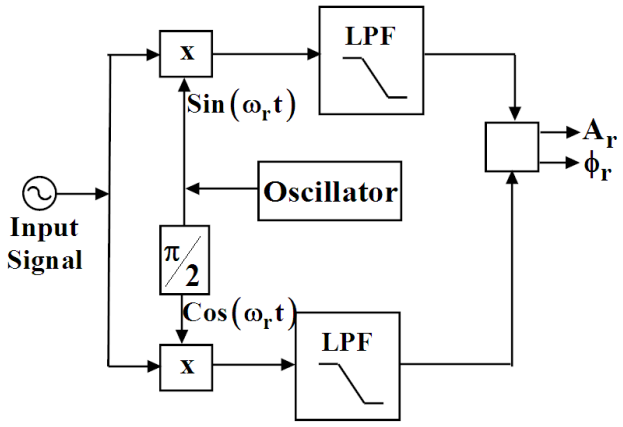


Fig.2.6 Block Diagram of Coulon Oscillator

$$x(t) = \sum_{i=1}^{N} A_i \sin(\omega_i t + \varphi_i) \tag{2.16}$$

where N is the harmonic order, A_i is the harmonic amplitude and φ_i is the phase angle. The Coulon oscillator frequency is defined as $f_r = \omega_r / 2\pi$, which generates the $\sin(\omega_r t)$ and $\cos(\omega_r t)$ signals. Also $x_1(t)$ and $x_2(t)$ can be given by the following expressions.

$$x_1(t) = \sum_{i=1}^{N} A_i \sin(\omega_i t + \varphi_i).\sin(\omega_r t) \tag{2.17}$$

$$x_2(t) = \sum_{i=1}^{N} A_i \sin(\omega_i t + \varphi_i).\cos(\omega_r t) \tag{2.18}$$

Eq. (2.17) and (2.18) can be rewritten as

$$x_1(t) = \sum_{i=1}^{N} \frac{A_i}{2}\{\cos[(\omega_i - \omega_r)t + \varphi_i] - \cos[(\omega_i + \omega_r)t + \varphi_i]\} \tag{2.19}$$

$$x_2(t) = \sum_{i=1}^{N} \frac{A_i}{2}\{\sin[(\omega_i - \omega_r)t + \varphi_i] + \sin[(\omega_i + \omega_r)t + \varphi_i]\} \tag{2.20}$$

Considering $f_1 = \omega_1 / 2\pi$, $\omega_i = i \cdot \omega_1$, $\omega_r = r \cdot \omega_1$ (i and r as the fundamental and harmonic orders), Eq. (2.19) and (2.20) can be defined as follows.

$$x_1(t) = \sum_{i=1}^{N} \frac{A_i}{2} \{\cos[(i-r)\omega_1 t + \varphi_i] - \cos[(i+r)\omega_1 t + \varphi_i]\} \tag{2.21}$$

$$x_2(t) = \sum_{i=1}^{N} \frac{A_i}{2} \{\sin[(i-r)\omega_1 t + \varphi_i] + \sin[(i+r)\omega_1 t + \varphi_i]\} \tag{2.22}$$

In order to extract the fundamental frequency of signal $x(t)$, frequency of the oscillator ω_i should be same as ω_1, i.e. $r = i = 1$. Therefore signal $x(t)$ can be presented as follows.

$$x_1(t) = \frac{A_1}{2}\cos(\varphi_1) - \frac{A_1}{2}\cos(2\omega_1 t + \varphi_1) + \sum_{i=2}^{N} \frac{A_i}{2} \{\cos[(i-1)\omega_1 t + \varphi_i] + \cos[(i+1)\omega_1 t + \varphi_i]\} \tag{2.23}$$

$$x_2(t) = \frac{A_1}{2}\sin(\varphi_1) - \frac{A_1}{2}\sin(2\omega_1 t + \varphi_1) + \sum_{i=2}^{N} \frac{A_i}{2} \{\sin[(i-1)\omega_1 t + \varphi_i] + \sin[(i+1)\omega_1 t + \varphi_i]\} \tag{2.24}$$

The first terms of the Eq. (2.23) and (2.24) are the DC components related to the fundamental magnitude A_1 and phase angle φ_1, and the second terms relate to the second harmonic components and the remaining terms in the equations are higher frequency components. A low-pass filter filters out the DC components of each signal, which are given as follows.

$$V_d' = \frac{A1}{2}\cos\varphi 1 \tag{2.25}$$

$$V_q' = \frac{A1}{2}\sin\varphi 1 \tag{2.26}$$

Therefore, the output of the Coulon oscillator can be expressed as

$$A_1 = \sqrt{(2V_d')^2 + (2V_q')^2} \tag{2.27}$$

$$\varphi_1 = \tan^{-1}\left(\frac{V_q'}{V_d'}\right) \tag{2.28}$$

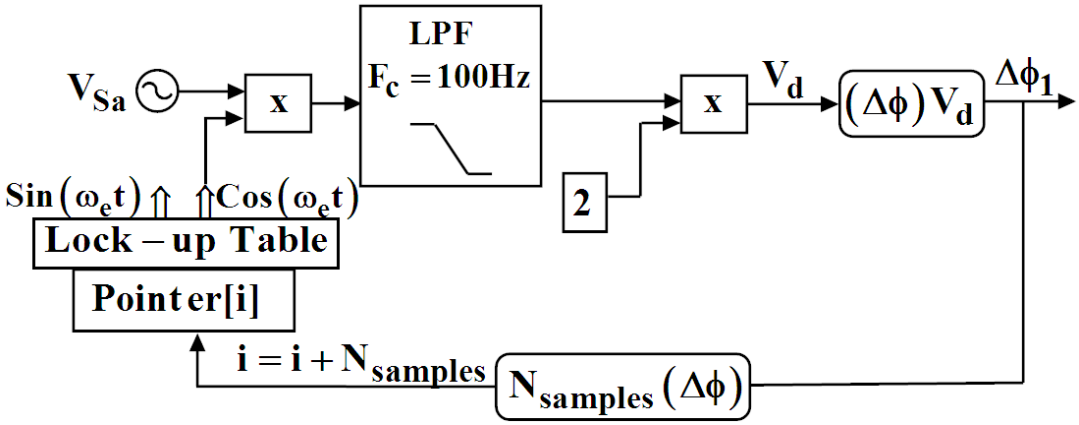


Fig.2.7 Block diagram of the CO-PLL structure

When the phase of the oscillator coincides with the phase of the fundamental component of input signal i.e. φ_1, then $V_d' = 0.5A_1$ and $V_q = 0$. It can be shown that the Coulon oscillator permits only fundamental component of the input signal while rejecting other harmonic components by appropriately tuning of the oscillator. Fig.2.7 shows the block diagram of the CO-PLL structure, where V_{sa} is the phase utility voltage and can be expressed as

$$V_d = 2V_d' = A_1 \cos\varphi_1 \tag{2.29}$$

$$V_q = 2V_q' = A_1 \sin\varphi_1 \tag{2.30}$$

where $\varphi_1 = \arcsin\left(V_q\right), A_1 = 1.0$.

The phase angle φ_1 of the output can be fed back to the oscillator to lock its frequency and phase, so that φ_1 approaches to zero. In this condition, $\sin(\omega_e t)$ and $cos(\omega_e t)$ can be defined as unit phase voltage V_{sa}. The advantage of the CO-PLL in comparison with the other PLL is that it is derived from only one phase voltage, and the unit vector output is not affected by harmonic distortion, unbalance or sag/swell of the utility voltage.

From the Eq. (2.29) and Eq. (2.30), the three-phase unit sine vector signals are defined as follows.

$$\begin{aligned} U_a &= A_1 \sin\varphi_1 = A_1 \sin(\omega t) \\ U_b &= A_1 \sin\left(\omega t - \frac{2\pi}{3}\right) \\ U_c &= A_1 \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{2.31}$$

2.4.3 Hysteresis Current controller

The schematic diagram of the hysteresis current controller is shown in Fig.2.8. The current error signal $\delta_{abc}(t)$ is the difference between the reference current (i^*_{Sabc}) and the measured current (i_{Sabc}). These error signals are fed to the HCC for generation of required switching signal. When the error signal crosses the upper boundary of the hysteresis band (HB), the lower switch of the inverter arm is turned ON, and the upper switch is turned OFF. Therefore, the current starts falling [93]. Fig. 2.9 demonstrates the ON and OFF switching signal to drive the SAPF system. When the error signal exceeds the lower boundary of the band, the upper switch is turned ON, and the lower switch is turned OFF. Consequently, the current is retained within the hysteresis band. Therefore, the actual current is forced to track the reference current in the hysteresis band.

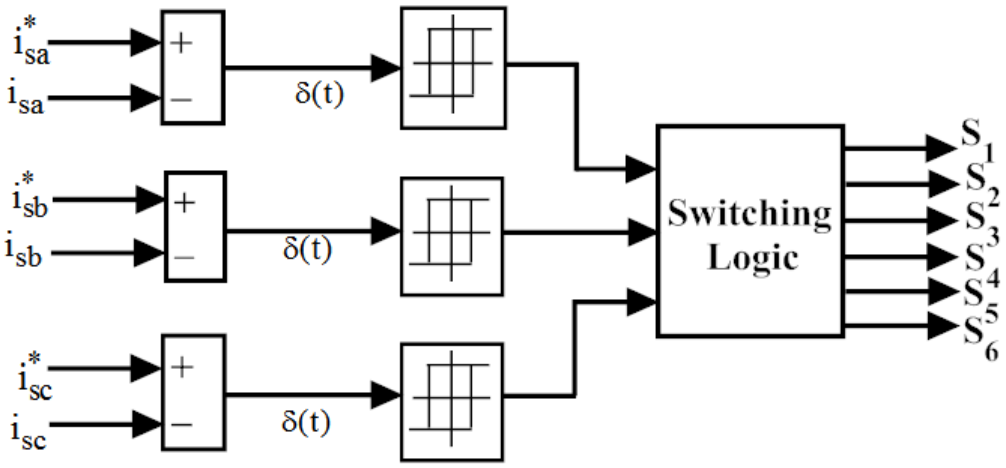


Fig.2.8. Schematic block diagram of hysteresis current controller.

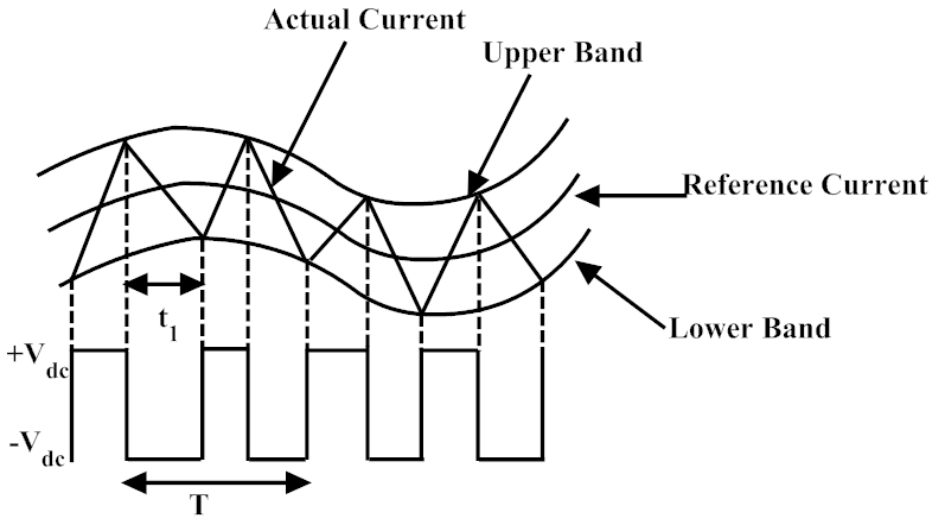


Fig.2.9. Switching pattern of hysteresis current controller.

The phase-A switching state value is defined as

$$S=\begin{Bmatrix} ON \quad if \;\; i_{sa}(t) < i_{sa}^{*}(t) - hb \\ OFF \quad if \;\; i_{sa}(t) > i_{sa}^{*}(t) + hb \end{Bmatrix} \tag{2.32}$$

Correspondingly, the switching state of phase-B and phase-C can be derived by considering the HB. As the circuit of the hysteresis controller is very simple, it is widely used for SAPF applications [94]. However, HCC method exhibits certain unwanted effects such as variable switching frequency and generates significant sideband harmonics around the switching frequency. Thus, it increases switching losses and electromagnetic interference

(EMI) noise issues. To overcome these problems, the SMC based PWM technique is implemented in SAPF. The sliding mode current control method provides superior performance on harmonic compensation perspective, as switching frequency is restricted within a practical range.

2.4.4 Sliding Mode current control

The single-phase equivalent circuit for the shunt converter is illustrated in Fig.2.10. Sliding mode control law based upon switching function 'u' is considered here. When

either S_1 or D_1 conducts, then $u = 1$ and when either S_2 or D_2 conducts, then $u = -1$. The inductor current is given by the following expression,

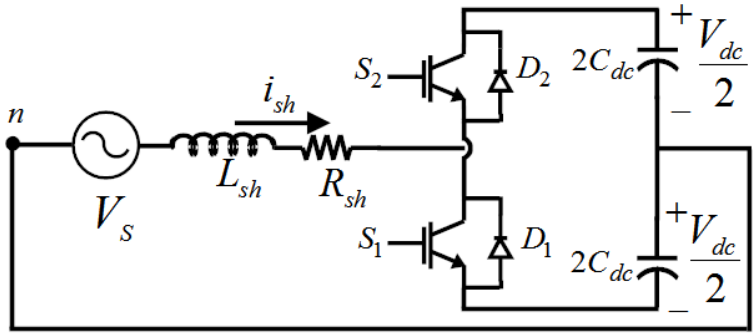


Fig.2.10 Equivalent Circuit for one leg of the shunt converter.

$$\frac{di_{sh}}{dt} = \frac{V_S}{L_{sh}} - u\frac{V_{dc}}{2L_{sh}} - \frac{R_{sh}}{L_{sh}} i_{sh} \tag{2.33}$$

The capacitor voltage equation considering the ripple due to compensating currents can be expressed as

$$\frac{dV_{dc}}{dt} = -\frac{1}{2}[u_a \frac{i_{sha}}{C_{dc}} + u_b \frac{i_{shb}}{C_{dc}} + u_c \frac{i_{shc}}{C_{dc}}] \tag{2.34}$$

where u_a, u_b and u_c are the independent controls for phases *a*, *b*, and *c*, respectively. The SAPF circuit can be decomposed into three first order independent systems that can be expressed as

$$i_{sx} = i_{Lx} + i_{shx} \tag{2.35}$$

$$= i_{Lx} + \int \left[\frac{V_{Sx}}{L_{sh}} - u_x \frac{V_{dc}}{2L_{sh}} - \frac{R_{sh}}{L_{sh}} i_{shx} \right] dt \tag{2.36}$$

where *x* denotes the phase. To apply SMC technique for designing SAPF, the sliding surfaces must be defined such that the source current i_{Sx} should follow the source reference current i_{Sx}^*. The sliding surfaces for source currents can be defined as below.

$$\mathbb{S}_x = [i_{Sx}^* - i_{Sx}] = 0 \tag{2.37}$$

To assure that the system can be maintained on the sliding surface, it must be shown that there is a natural control that satisfies $\mathbb{S}\dot{\mathbb{S}} \le 0$ at all times, i.e., for all values that the state may experience. It u is within the natural control bounds of the physical system for $\dot{\mathbb{S}} = 0$, and then it is possible to remain on the sliding surface at all times and maintain perfect tracking. Setting $\mathbb{S}_x = 0$, the equivalent control can be obtained as follows.

$$u_{eqx} = \left(\frac{di_{Lx}}{dt} + \frac{V_{xn}}{L_{sh}} - \frac{di_{Sx}^*}{dt} - \frac{R_{sh}}{L_{sh}} i_{shx} \right) \left(\frac{2L_{sh}}{V_{dc}} \right) \tag{2.38}$$

The natural control limits of the circuit are $-1 \le u_{eqx} \le 1$. To satisfy $\mathbb{S}\dot{\mathbb{S}} \le 0$, the discontinuous control law is provided below.

$$\text{If } \mathbb{S} < 0 \text{ then } u = 1 \tag{2.39}$$

$$\text{If } \mathbb{S} > 0 \text{ then } u = -1$$

For generating switching pulses, this control law can be applied to the SAPF.

2.5 Simulation Results and Analysis

The control techniques have been verified using MATLAB-SIMULINK according to the structure shown in Fig.2.4. A three phase diode bridge rectifier with RL load is considered as a nonlinear load. The parameters used in the simulation are shown in Table 2.1, where R_{sh} and L_{sh} correspond to the link inductor model, C_{dc} is the DC-link capacitor, V_{dc}^* is the reference DC-link voltage, K_P, K_i are the PI-controller coefficients and V_{rms} is the rms value of the source voltage.

Table 2.1. Simulation Parameters

V_{rms}	360 V	V_{dc}^*	620 V
R_L	6.6 Ω	R_{sh}	1 Ω
L_L	22 mH	L_{sh}	2.7 mH
C_{dc}	1800 μF	K_p	0.1273
R_s and L_s	0.1 Ω and 0.1 mH	K_i	4.5000

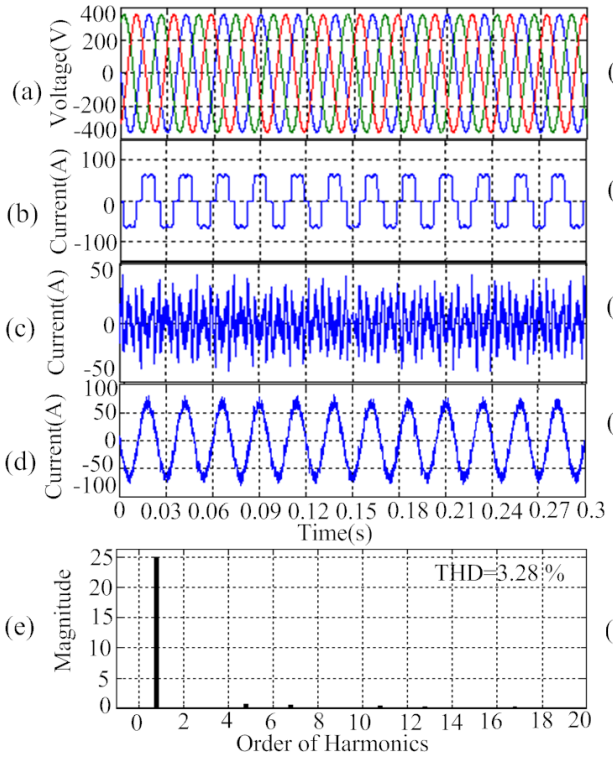


Fig.2.11 Simulation Waveform of the HCC with balanced supply condition (a) Source voltage, (b) Load current, (c) Compensation current (d) Source current, (e) FFT of source current after compensation.

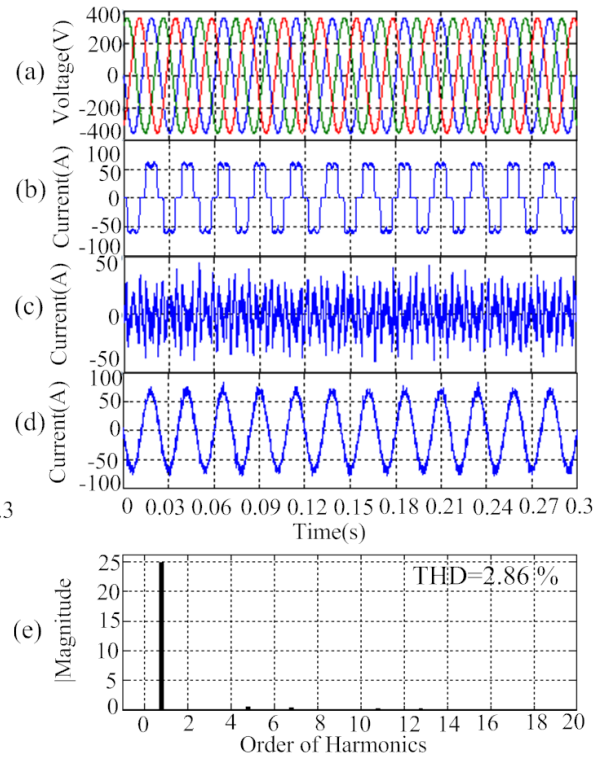


Fig.2.12 Simulation Waveform of the SMC with balanced supply condition, (a) Source voltage, (b) Load current, (c) Compensation current, (d) Source current, (e) FFT of source current after compensation.

Investigations are carried out with three different operating conditions of source voltage such as balanced, unbalanced and distorted. A source voltage of 360 V (rms) is considered for balanced supply condition, and 4^{th} order harmonic component is incorporated into the source voltage for the distorted supply condition. An unbalanced source voltage is created by phase variation to each other. A comparison is made between the both HCC and SMC under balanced, unbalanced and distorted supply voltage conditions. Fig. (2.11) and (2.12) show the performance of shunt active power filter under a balanced source voltage condition with HCC and SMC schemes respectively. The source voltage V_S, load current i_{la}, compensation current i_{sha}, source current i_{sa} and FFT of source current after compensation for phase *a* are shown from top to bottom order. From the Fig.2.11 (d) and Fig.2.12 (d), it is observed that the source current is close to sinusoidal and remains in phase with source voltage therefore unity power factor is maintained. It is also observed that the HCC

technique suffers from the switching ripples and results in a slightly higher value of THD (≈ 3.28 %) in source current as compared to SMC technique (≈2.86 %), which is shown in Table 2. Fig.2.13 and 2.14 shows the performance of SAPF under HCC and SMC with unbalanced supply voltage conditions. It is observed from Fig.2.13 (d) and Fig.2.14 (d) that source current is sinusoidal and in phase with the supply voltage. However, on the basis of calculation of THD, Table 2 shows the superiority of the SMC method (3.12 %) over the HCC method (3.88 %).

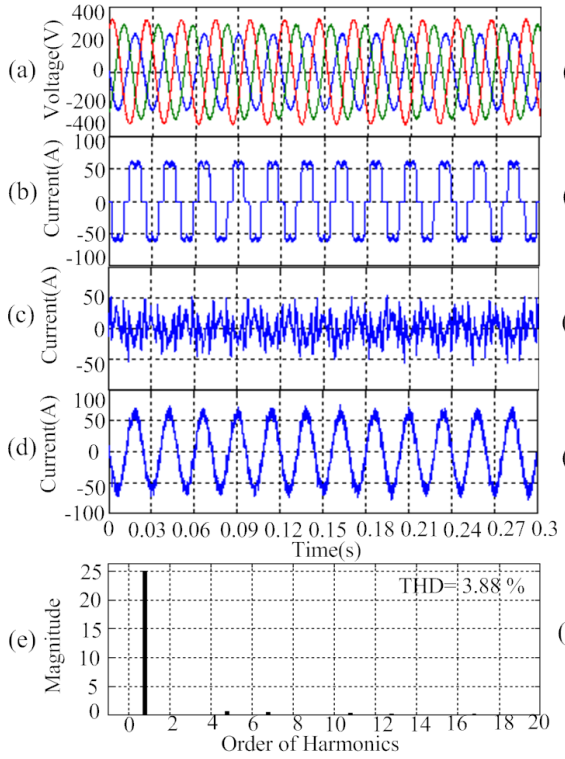


Fig.2.13 Simulation Waveform of the HCC with unbalanced supply condition, (a) Source voltage, (b) Load current, (c) Compensation current, (d) Source current, (e) FFT of source current after compensation.

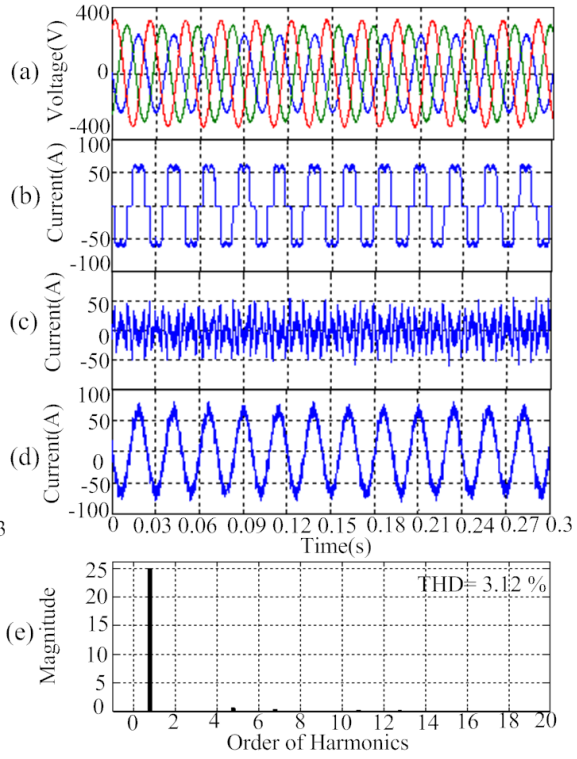


Fig.2.14 Simulation Waveform of the SMC with unbalanced supply condition, (a) Source voltage, (b) Load current, (c) Compensation current, (d) Source current, (e) FFT of source current after compensation.

Fig.2.15 and 2.16 show the performance of SAPF under HCC and SMC with the distorted source voltage condition with a similar order as in the above case. Here source voltage THD is taken as 8.14 %. Source current results (Fig.2.15 (d) and Fig.2.16 (d)) show the successful reduction of harmonics from the supply current by having on the approximation of 4 % THD. Table 2.2 shows that THD of HCC is found to be 4.47 %,

whereas in case of SMC it is 4.06 %. Amplitudes of different harmonic orders (5^{th} to 19th) for balanced source voltage condition are analysed using the above two methods, which are shown in Table 2.3, It is found that the amplitude of harmonics is minimum in SMC as compared to HCC showing the higher priority of former one.

The DC-link voltage performance of both HCC and SMC control scheme are analyzed in Fig.2.17. The DC-link voltage of both controller methods during balanced, unbalanced and distorted supply voltage condition is shown in the figure from top to bottom order. It is observed from the figure that the variations of DC-link voltage are quite satisfactory and able to settle down with a minimum amount of time during balanced, unbalanced and distorted supply voltage condition.

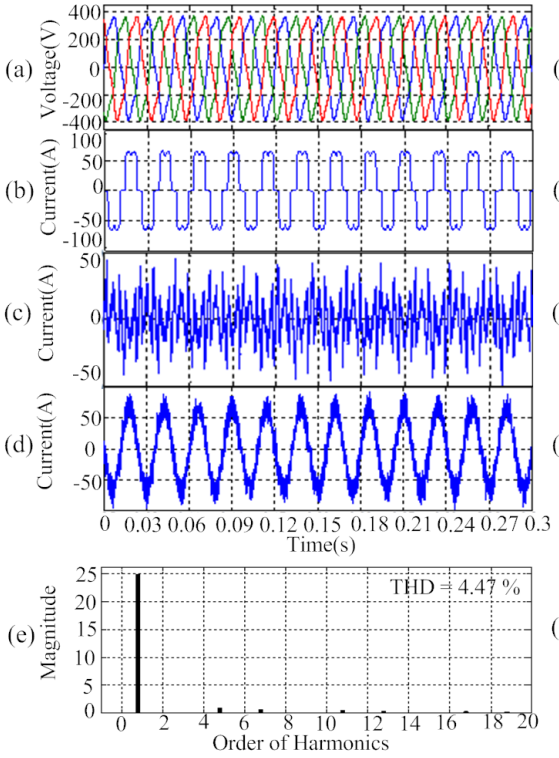


Fig.2.15 Simulation Waveform of the HCC with distorted supply condition, (a) Source voltage, (b) Load current , (c) Compensation current , (d) Source current, (e) FFT of source current after compensation.

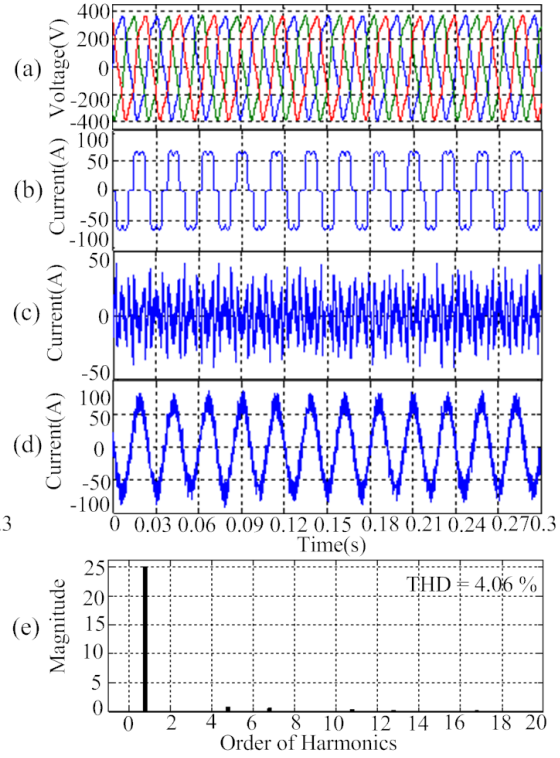


Fig.2.16 Simulation Waveform of the SMC with distorted supply condition, (a) Source voltage, (b) Load current , (c) Compensation current , (d) Source current , (e) FFT of source current after compensation.

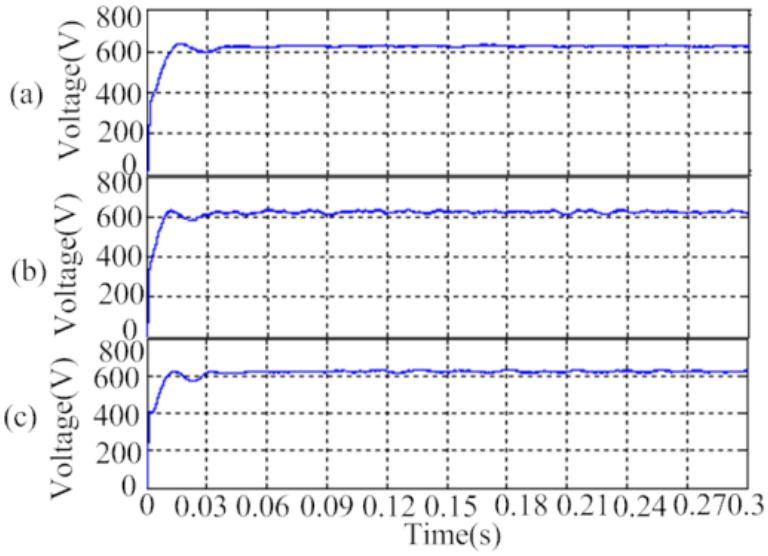


Fig.2.17 DC-link voltage waveforms, (a) During balanced supply voltage condition, (b) During unbalanced supply voltage condition, (c) During distorted supply voltage condition.

Table 2.2 Calculation of THD %

Source Voltage condition	Control Techniques	Source Current Before Compensation	Source Current After Compensation
Balanced Supply Voltage	HCC	29.71 %	3.28 %
	SMC	29.71 %	2.86 %
Unbalanced supply voltage	HCC	29.26 %	3.88 %
	SMC	29.26 %	3.12 %
Distorted supply voltage	HCC	30.11 %	4.47 %
	SMC	30.11 %	4.06 %

Table 2.3 Source current harmonics during balanced supply voltage condition

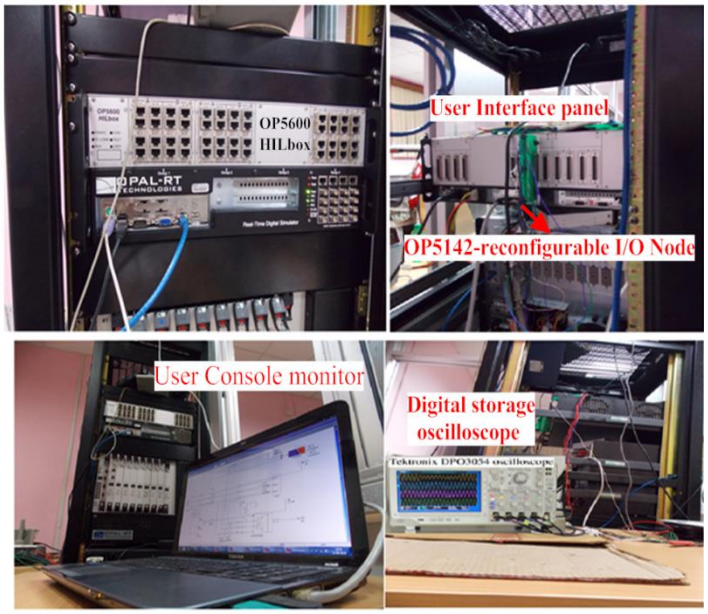
Harmonic order	HCC	SMC
5th	0.41	0.29
7th	0.44	0.27
11th	0.47	0.27
13th	0.36	0.29
17th	0.43	0.25
19th	0.41	0.26

2.6 Real-Time experimental Results using HIL based OPAL-RT simulator

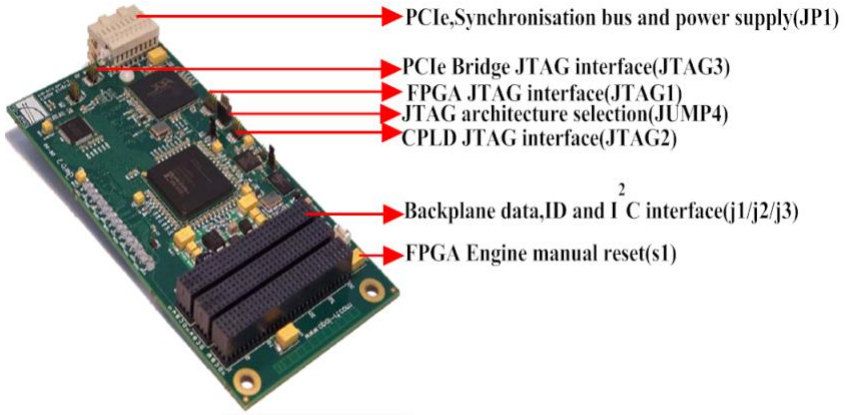
Hardware-in-the-loop (HIL) real-time system is assembled for validating the viability of the proposed technique for practical implementation. Developed laboratory experimental setup using HIL system is depicted in Fig.2.18 and Table 2.1 illustrates the system parameters used for experimental investigation. The HIL real-time system is confined in an OPAL-RT digital simulator (OP5600) with OP5142 Xilinx SPARTAN-3(3xc3s5000) Field programmable gate array (FPGA) processor. The OPAL-RT is a real-time simulation platform, which is equipped in Intel Quad core 2.40 GHz processor with the real-time operating system of type QNX and Red Hat Linux.

The OP5142 reconfigurable FPGA-based input/output (I/O) controller is equipped with 3.3-GHz SPARTAN-3 (3xc3s5000) processor and enables the distributed execution of Hardware Description Language (HDL) capacities and high-speed, high-density digital I/O in real-time models. It is equipped with expansion slots accommodating up to 8 signal conditioning and analog/digital converter modules with 16 or 32 channels each for a total of 128 analog or 256 discrete or mix of analog and digital signals and 16 analog I/O channels and 32 digital I/O channels. The OP5142 is optimized for HIL simulation applications and particularly intended for utilization with Opal-RT's full-line of Real-Time simulators. The OPAL-RT signifies the total power circuit system by implementing the circuit component such as three phase three wire (3P3W) distorted or unbalanced power source, the unbalanced load and both shunt and series converter. The SPARTAN-3 FPGA processor can represent the digital control for the UPQC through its I/O ports. The essential signals utilized for controlling purpose are taken out from the DAC ports.

The experimentation has been carried out at switching frequency of 10 kHz. Fig.2.18 illustrates the performance of SAPF under balanced supply condition, Fig.2.18 (a) provides information about the source voltage and Fig.2.18 (b) shows the waveforms of load current, compensation current, and source current using HCC control scheme. Fig.2.19 follows the same pattern for SMC scheme. Figs.2.20-2.21 (a & b) and Figs.2.22-2.23 (a & b) provide the results using unbalanced and distorted supply voltage conditions respectively. Under all operating conditions of the supply voltage, source current is observed to be more sinusoidal in case of SMC in comparison to the HCC method.



(a)



(b)

Fig.2.18 Real-time OPAL-RT experimental setup, (a) Real time HIL system, (b) OP5142 connectors and layout.

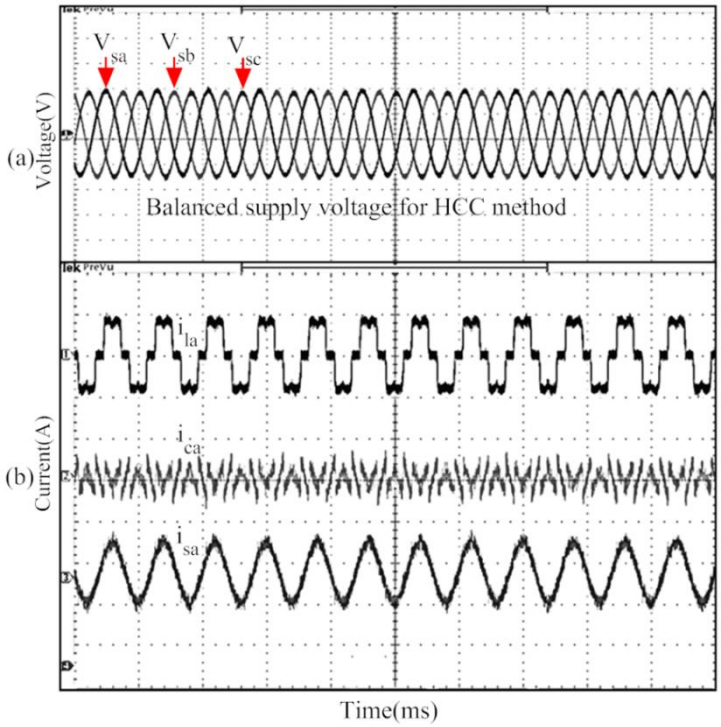


Fig.2.19 Real-time experimental waveform under Balanced supply voltage with HCC method, (a) Source voltage (scale: 200 V/div), (b) Load current (scale: 75 A/div), Compensation current (scale: 125 A/div), Source current (scale: 84 A/div).

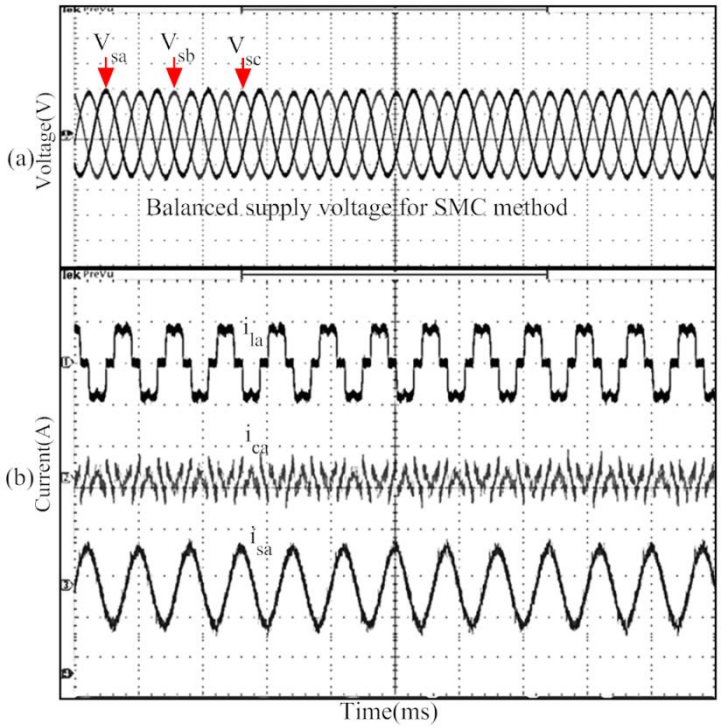


Fig.2.20 Real-time experimental waveform under balanced supply voltage with SMC method, (a) Source voltage (scale: 200 V/div), (b) Load current (scale: 75 A/div), Compensation current (scale: 125 A/div), Source current (scale: 84 A/div).

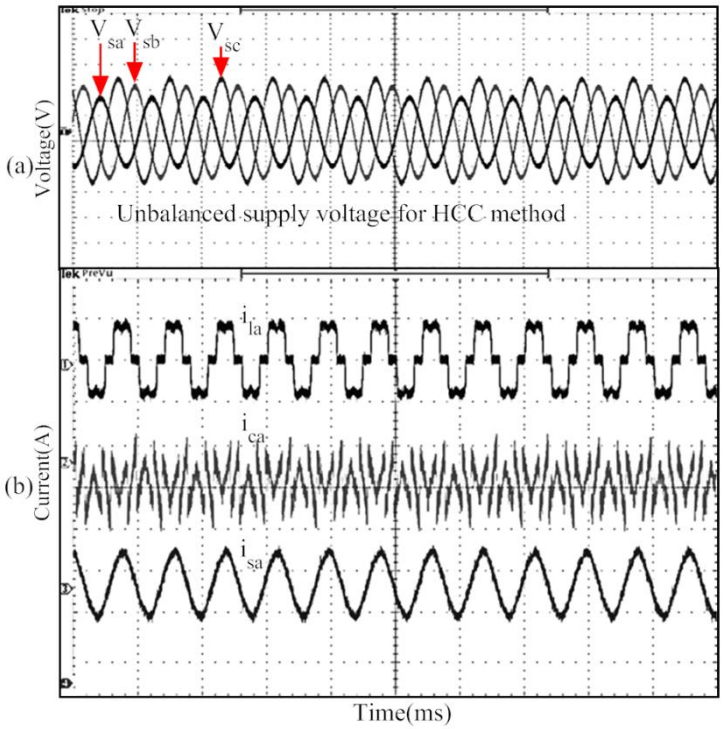


Fig.2.21. Real-time experimental waveform under unbalanced supply voltage with HCC method, (a) Source voltage (scale: 200 V/div), (b) Load current (scale: 75 A/div), Compensation current (scale: 70 A/div), Source current (scale: 84 A/div).

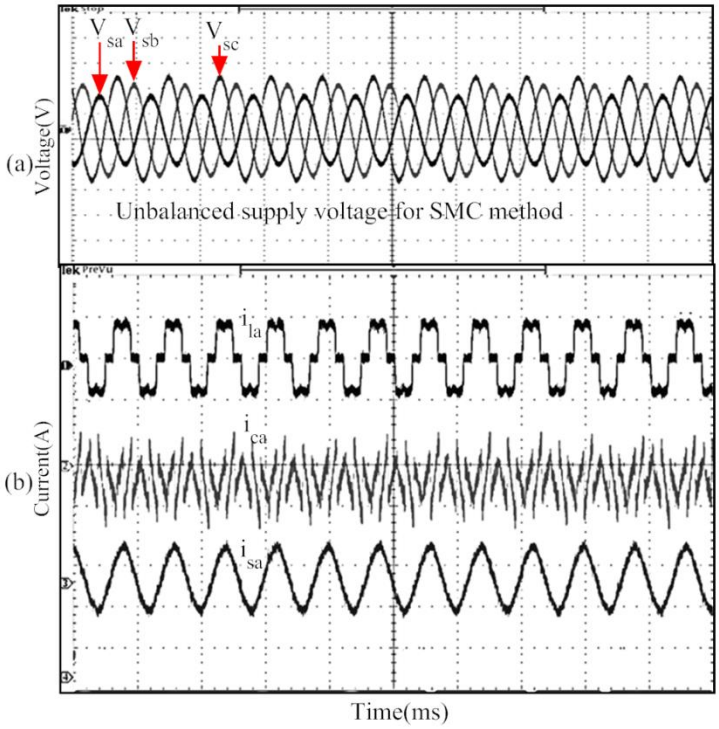


Fig.2.22 Real-time experimental waveform under unbalanced supply voltage with SMC method, (a) Source voltage (scale: 200 V/div), (b) Load current (scale: 75 A/div), Compensation current (scale: 70 A/div), Source current (scale: 84 A/div).

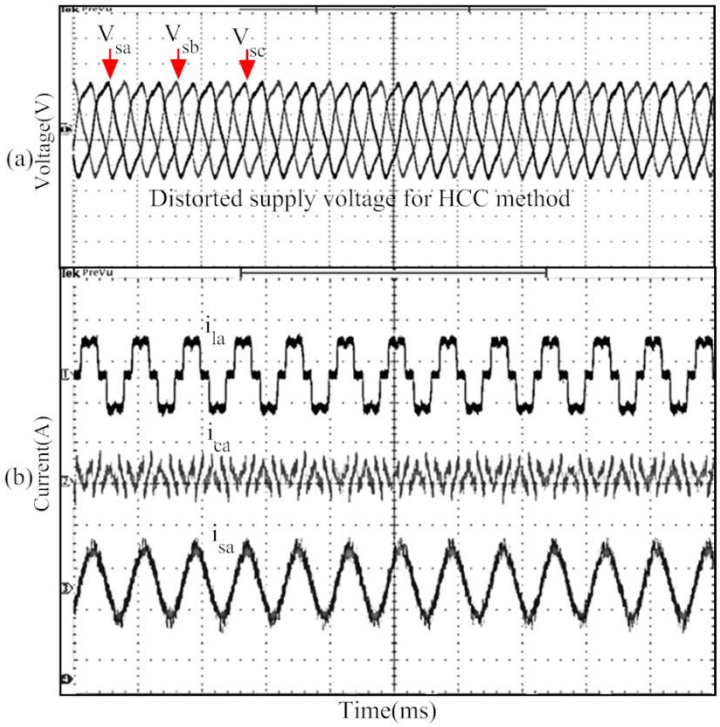


Fig.2.23. Real-time experimental waveform under distorted supply voltage with HCC method, (a) Source voltage (scale: 200 V/div), (b) Load current (scale: 75 A/div), Compensation current (scale: 125 A/div), Source current (scale: 84 A/div).

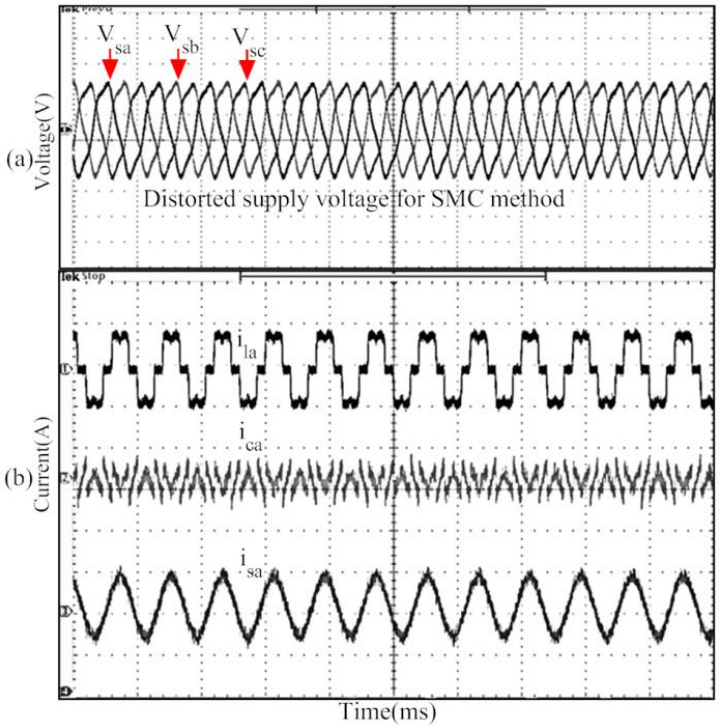


Fig.2.24. Real-time experimental waveform under distorted supply voltage with SMC method, (a) Source voltage (scale: 200 V/div), (b) Load current (scale: 75 A/div), Compensation current (scale: 125 A/div), Source current (scale: 84 A/div).

2.7 Chapter Summary

In this chapter, two control strategies HCC and SMC have been utilized for the three-phase three-wire distribution SAPF system to improve the performance under balanced, unbalanced and distorted supply voltage conditions. Both the control strategies consider CO-PLL technique for positive sequence signal extraction utilized in reference current generation and PI controller utilized in the outer control loop for DC-link voltage regulation. It is observed from both simulation and experimental results that, both control strategies are able to compensate the source current to be almost perfect sinusoidal even with highly distorted load current. However, it is verified through THD factors of the source current that the SMC strategy provides better steady state performance in comparison to the HCC method during balanced, unbalanced and distorted supply voltage condition.

Although these two SAPF have similar fundamental operating principles, the way they are constructed and designed are different. Nevertheless, SAPF is not able to compensate for voltage related problems such as voltage harmonics, voltage sag/swell and supply voltage unbalanced conditions. Therefore, in the next chapter, we will investigate how shunt active power filter can be integrated with series active power filter to provide voltage harmonics, voltage sag/swell and supply voltage unbalanced compensation capability.

Chapter 3

Novel Nonlinear DC-link voltage controller with Modified SRF based Control philosophy for Unified Power Quality Conditioner (UPQC)

3.1 Introduction

In chapter 2, HCC and SMC current control strategies have been developed for the SAPF to effectively eliminate current harmonics produced by nonlinear loads. Even though the superiority of SMC over HCC is justified in Chapter 2, SMC also has a few limitations like huge amount of calculations in designing sliding surfaces. On the other hand, a simpler theoretical analysis is evolved in case of HCC, which provides fast response as well as easier implementation. Moreover, the SAPF cannot compensate PQ issues related to voltage phenomena, such as voltage harmonics, voltage sag/swell and voltage unbalance.

With above considerations, in this chapter, UPQC, which is integrated with shunt APF and series APF, can be utilized to compensate both current and voltage related problems and also HCC is chosen as a suitable PWM control strategy in UPQC system at the beginning stage. Major research works have been carried out on controller and extraction circuit design to increase the operating performance of UPQC. At first, operating principle and design of UPQC is presented and then a novel control algorithm is introduced with the aid of nonlinear DC-link voltage controller with modified synchronous reference frame (SRF) control strategy for improvement of both current and voltage compensation performance of the UPQC. The feasibility of the proposed control algorithm is verified through simulations and experimental results.

3.2 Structural design and operating principle of UPQC

The structural design of UPQC is shown in Fig.3.1. It comprises of series APF and shunt APF. The series APF is a three phase pulse-width modulated (PWM) voltage source inverter. The main objective of series APF is to mitigate voltage sag, swell, voltage distortion and voltage unbalance originating from the source voltage. The LC filter consists of inductor L_{sef} and capacitor C_{ef} connected in each phase to prevent the flow of switching ripples. The transformers are connected at the output of the LC filter to provide isolation

between series APF and the power line and also prevent the DC capacitor from being short circuited due to the operation of various switches. The power circuit of shunt APF consists of a three-phase PWM voltage source inverter, DC side is connected to the DC bus capacitor (C_{dc}). Shunt APF is connected through a filter inductor L_{shf} which provides isolation between the shunt APF and power line. The purpose of shunt APF is to restrain the load current harmonics and to control the DC bus voltage. Ideally, once it is charged, the DC bus voltage V_{dc} should not fall off its charge, but some power is consumed due to finite switching losses of the inverter and losses in the inductor as well as capacitor. Hence, the charge of the DC bus voltage needs to be maintained by using closed-loop control of the shunt APF. Insulated gate bipolar transistors (IGBTs) with anti-parallel diodes are used as switching devices in both series and shunt APF. A 3-phase diode-bridge rectifier employed with resistive (R_L) and inductive (L_L) load produces harmonic current.

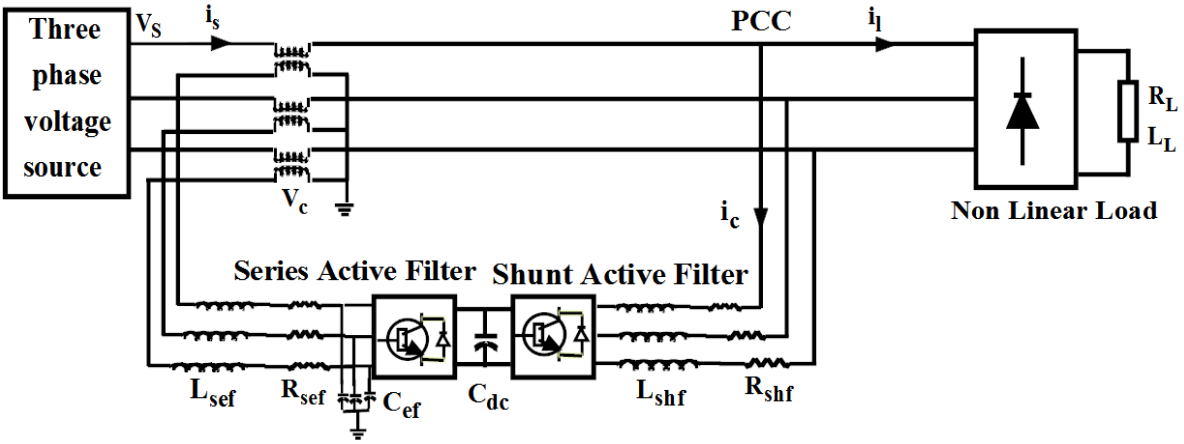


Fig.3.1. Structural design of UPQC

Fig. 3.2 demonstrates the single-phase equivalent circuit of UPQC. The nonlinear load is modeled by two current sources i_{lh} (harmonics current) and i_{lf} (fundamental current). The voltage source V_s is represented as a supply voltage and current source i_c as well as voltage source V_c represent as injection current of the shunt APF and the injection voltage of the series APF, respectively. From the figure, it can be analysed that

$$i_s + i_c = i_l = i_{lh} + i_{lf} \tag{3.1}$$

To achieve the supply current i_s to be perfectly sinusoidal (i_{lf}), Eq.3.1 can be written as

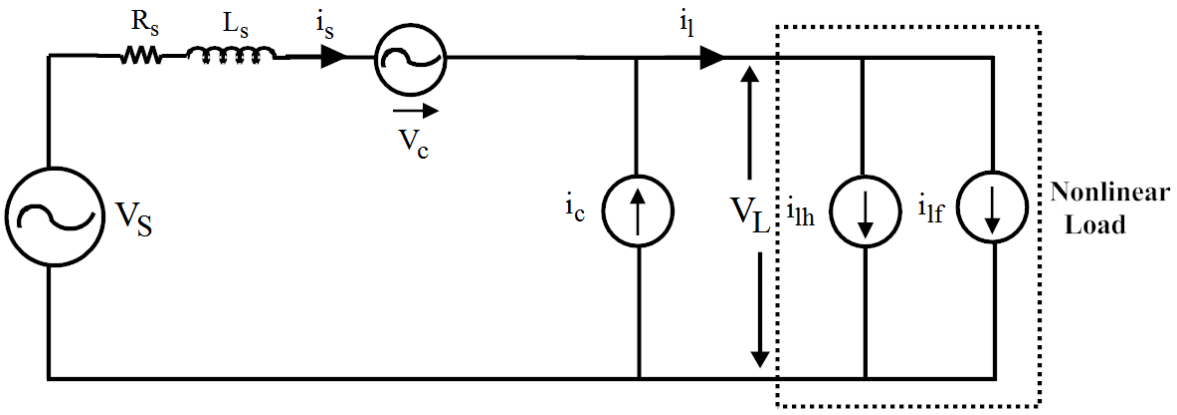


Fig. 3.2 Equivalent single-phase circuit of UPQC

$$i_c = i_{lh} \tag{3.2}$$

Eq.3.2 illustrates that in order to obtain a clean sinusoidal supply current i_S, the shunt APF of the UPQC has to keep on injecting harmonic compensating current that is equal in amplitude and opposite in phase with load current to cancel the current harmonics present in the source current [96].

Similarly, the series active filter compensation objectives are accomplished by injecting voltages in series with the source voltages such that the load voltages are undistorted and balanced, and their magnitudes are kept at the desired level. This voltage injection is delivered by the DC-link capacitor and the series APF. Based on measured supply and load voltages the control technique produces the appropriate PWM signals for the series APF. The series APF is controlled in voltage-control method utilizing the most useful PWM switching scheme described detail in [97]. In order to produce the injected voltage of desired magnitude, the actual voltage signal is compared with the reference voltage signal and the corresponding error signal is applied to the PWM controller for generation of appropriate switching signals. The DC-link capacitor is consecutively connected to the inverter outputs with positive and negative polarity. The output voltages of the series APF do not have the actual shape of the desired signals. However, it contains switching harmonics, which are filtered out by the series low pass filter. Therefore, the amplitude, phase shift, frequency and harmonic content of injected voltages are controllable.

3.3 Nonlinear variable gain fuzzy and modified PLL based SRF control strategy

In this section, the nonlinear variable gain fuzzy (NVGF) controller for DC-link voltage regulation and a simple SRF based reference generation scheme with modified phase-locked-loop (MPLL) control technique are proposed for UPQC to improve the power quality problems such as current harmonics, reactive power, sag/swell, voltage unbalance, and voltage distortion present in the power distribution network. The proposed NVGF controller uses TS-fuzzy type numerical consequent rule, which limits the dc-link voltage deviations in UPQC during the load and supply voltage disturbances and assures an insignificant error causing UPQC robust against all dynamic conditions. The SRF with MPLL technique is able to detect the phase of the utility signal as fast as possible and provides adequate reference signal. Thus the proposed control strategy can be an effective solution for UPQC that requires integrated functionalities such as generation of fast and accurate reference signal, reduction of load and supply voltage disturbances and minimization of the effects of measurement noise produced from sensor. The real time hardware in the loop (HIL) system is developed using an OPAL-RT simulator with OP5142 Xilinx SPARTAN-3 Field programmable gate array (FPGA) processor for validating the performance of the proposed algorithm for practical applications.

3.3.1 Design of NVGF for DC-link voltage regulation

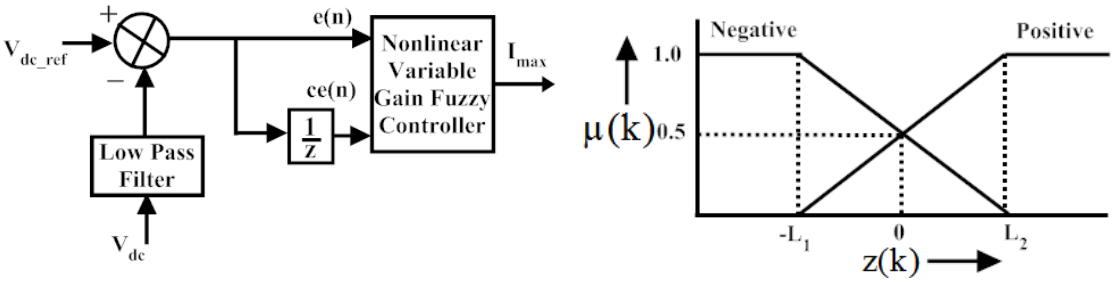
In this section, design of the NVGF control scheme using TS-fuzzy rule is considered for DC-link voltage regulation. Schematic diagram of the TS-fuzzy control scheme for UPQC is shown in Fig.3.3 (a). In order to implement the control algorithm for dc link voltage control of UPQC, the DC-link capacitor voltage V_{dc} is sensed and then compared with the reference value V_{dc_ref}. The error signal $e(n)$ and its change in error $ce(n)$ are applied to the input of fuzzy controllers. The output of the fuzzy controller is the magnitude of peak reference current I_{max}. The deviations $e(n)$ and $ce(n)$ are fuzzified by two input fuzzy sets entitled as positive and negative and the mathematical definition of the membership functions are

$$\mu_p(z_i)=\begin{cases}0, & z_i<-L\\ \dfrac{z_i+L}{2L}, & -L\le z_i\le L\\ 1, & z_i<L\end{cases} \tag{3.3}$$

where $z_i(n)$ denotes error to the fuzzy controller at the n_{th} sampling instant specified by

$$z_1(n)=e(n)=V_{dc\_ref}-V_{dc} \tag{3.4}$$

$$z_2(n)=ce(n)=\dot{e}(n) \tag{3.5}$$



(a) (b)

Fig.3.3. Schematic diagram of the fuzzy control, (a) Control Structure, (b) Membership function.

Similarly the negative set membership function is

$$\mu_N(z_i)=\begin{cases}1 & z_i<-L\\ \dfrac{-z_i+L}{2L} & -L\le z_i\le L\\ 0 & z_i>L\end{cases} \tag{3.6}$$

The membership functions for the $e(n)$ and $\dot{e}(n)$ are shown in Fig.3.3 (b).The values of L_1 and L_2 are chosen on the basis of the maximum values of $e(n)$ and $\dot{e}(n)$. The TS-fuzzy controller uses four simplified rules as

R1: If $e(n)$ is positive and $\dot{e}(n)$ is positive, then $v_1(n)=$

$k_1(a_1e(n)+a_2\dot{e}(n)+a_3.(|e(k)|).\dot{e}(k))$

R2: If $e(n)$ is positive and $\dot{e}(n)$ is negative, then $v_2(n)=$

$k_2v_1(n)$

R3: If $e(n)$ is negative and $\dot{e}(n)$ is positive, then $v_3(n)=$

$k_3v_1(n)$

R4: If $e(n)$ is negative and $\dot{e}(n)$ is negative, then $v_4(n) =$

$k_4 v_1(n)$

The above rule base $v_1(n), v_2(n), v_3(n)$ and $v_4(n)$ denote the output of TS-fuzzy controller. Using Zadeh's fuzzy rules for AND operation and general defuzzifier, we get

$$u(n) = \frac{\sum_{j=1}^{4} (\mu_j)^{\alpha} v_j(n)}{\sum_{j=1}^{4} (\mu_j)^{\alpha}} \tag{3.7}$$

Substituting $v_j(n)$ $(j = 1,2,3,4)$ in Eq. (3.7), we obtain

$$u(n) = \frac{\sum_{j=1}^{4} (\mu_j)^{\alpha} v_j(n)}{\sum_{j=1}^{4} (\mu_j)^{\alpha}} = v_1(n) \frac{\sum_{j=1}^{4} (\mu_j)^{\alpha} k_j}{\sum_{j=1}^{4} (\mu_j)^{\alpha}} \tag{3.8}$$

For $\alpha = 1$, the centroid defuzzifier value $u(n)$ can be specified by

$$u(n) = a\,e(k) + b\,\dot{e}(k) + c.\left(|e(k)|\right).\dot{e}(k) \tag{3.9}$$

where

$$a = a_1 F(z_1, z_2),\ b = a_2 F(z_1, z_2) \text{ and } c = a_3 F(z_1, z_2) \tag{3.10}$$

Based on the Eq. (3.8), we specify $F(z_1, z_2)$ as

$$F(z_1, z_2) = \frac{k_1 \left(\mu_1 + k_2\mu_2 + k_3\mu_3 + k_4\mu_4\right)}{\left(\mu_1 + \mu_2 + \mu_3 + \mu_4\right)} \tag{3.11}$$

Therefore, the proportional and integral gains at any instant depend on an error and its change in error. If the maximum value of error and its change in error are L_1 and L_2 respectively, then $F(L_1, L_2) = k_1, F(L_1, -L_2) = k_1 k_2$, $F(-L_1, L_2) = k_1 k_3$, $F(-L_1, -L_2) = k_1 k_4$.

The above equation described for the TS-fuzzy controller is highly non-linear and the coefficients k_1, k_2, k_3 and k_4 yield extensive variation of the controller gains. In order to design the nonlinear variable gain TS-fuzzy controller, the optimized gain parameters for conventional PI controllers are determined. The PI controller [98] equations are defined as

$$H(s) = K_p + \frac{K_i}{s} \tag{3.12}$$

The proportional and integral gains are derived using $K_p = 2\delta\omega_n C_{dc}$ and $K_i = C_{dc}\omega_n^2$ [31], where $\delta = \sqrt{2}/2$ is the damping ratio, ω_n is the natural frequency and C_{dc} is the dc-link capacitor. The gain variation of the TS-fuzzy controller depends upon z_1 and z_2. Comparing Eq. (3.8) and Eq. (3.10), it is observed that the fuzzy controllers are same as nonlinear PI-controller and hence

$$K_p(z_1, z_2) = a_1 F(z_1, z_2) \tag{3.13}$$

$$K_i(z_1, z_2) = a_2 F(z_1, z_2) \tag{3.14}$$

$$K_e(z_1, z_2) = a_3 F(z_1, z_2) \tag{3.15}$$

where $K_e = \frac{K_p}{K_i}$

Eq. (3.13), Eq. (3.14) and (3.15) represent the variable proportional gain, variable integral gain and equivalent gain respectively. The parameters of variable gains are determined by using the characteristics of $F(z_1, z_2)$, which is determined by the value of k_1, k_2, k_3, k_4 and L as described in [99]. It is desirable to select the parameters k_1, k_2, k_3 and k_4 such that $K_p(0,0), K_i(0,0)$ and $K_e(0,0)$ are equal to K_p, K_i and K_e respectively, where $K_p(0,0), K_i(0,0)$ are the equivalent gains at the steady state of PI controller and $K_e(0,0)$ is the equivalent gain of K_e determined by using Eq.(3.15). Thus $K_p(0,0)$, $K_i(0,0)$ and $K_e(0,0)$ are given by

$$K_p(0,0) = a_1 \frac{k_1(1 + k_2 + k_3 + k_4)}{4} \tag{3.16}$$

$$K_i(0,0) = a_2 \frac{k_1(1 + k_2 + k_3 + k_4)}{4} \tag{3.17}$$

$$K_e(0,0) = a_3 \frac{k_1(1 + k_2 + k_3 + k_4)}{4} \tag{3.18}$$

If we choose the value of $k_1 = 1, k_2 = 0, k_3 = 1, k_4 = 0, K_p(0,0) = K_p, K_i(0,0) = K_i$ and $K_e(0,0) = K_e$ then we can get $a_1 = 2K_p$ from Eq.(3.13) and (3.16). The similar case holds for $a_2 = 2K_i$ and $a_3 = 2K_e$.

3.3.2. Modified PLL technique

The proposed modified PLL technique shown in Fig.3.4 can effectively enhance the performance of the UPQC under unbalanced and distorted source and load conditions. The MPLL is basically utilized for capturing the positive sequence signal of the supply voltage.

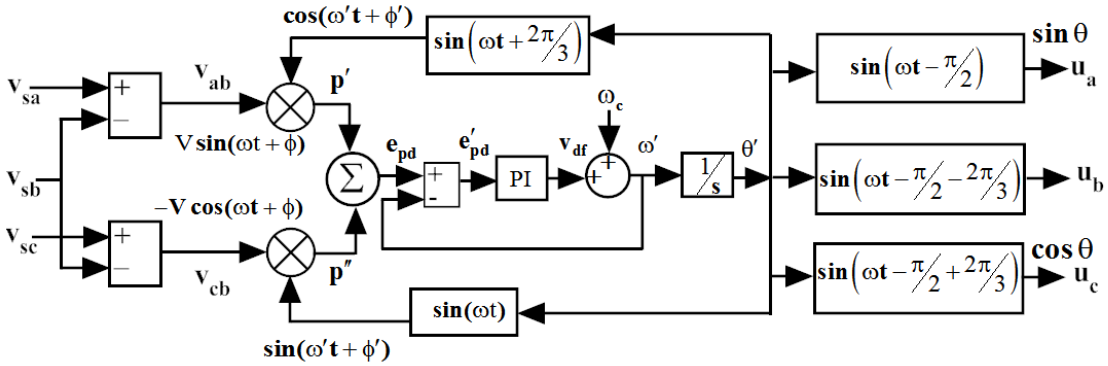


Fig.3.4.Modified PLL structure

The principal objective of modification of conventional PLL is to enhance the filtering performance in extremely distorted voltage and unbalanced voltage condition. The modification of the PLL is based on introducing the negative feedback in the inner control loop of conventional PLL. This negative feedback improves noise suppression capability of PLL and hence reduces the amount of distortions present in the signal before filtering and makes the filtering process smooth.

The proposed modified PLL consists of a phase detector (PD), LPF and voltage controlled oscillator (VCO). The PD is implemented by means of a simple subtractor, multiplier and adder. LPF is based on the PI-controller and the VCO consists of a sinusoidal function supplied by a linear integrator. The three phase signals are applied to the input of PLL. The signal of phase-b is subtracted from both phase-a and phase-c signals to generate in-phase signal $V\sin(\omega t+\phi)$ and quadrature phase signal $-V\cos(\omega t+\phi)$ respectively. These signals are multiplied with the signals $V\cos(\omega' t+\phi')$ and $V\sin(\omega' t+\phi')$ generated from VCO. Finally, the signal generated by the multiplier can be written as

$$p' = \frac{V}{2}\left[\sin(\omega t+\phi+\omega' t+\phi')+\sin(\omega t+\phi-\omega' t-\phi')\right] \tag{3.19}$$

$$p'' = -\frac{V}{2}\left[\sin\left(\omega t + \phi + \omega' t + \phi'\right) - \sin\left(\omega t + \phi - \omega' t - \phi'\right)\right] \tag{3.20}$$

The phase error signal from the PD can be written as

$$\begin{aligned} e_{pd}(s) &= p'(s) + p''(s) \\ &= V\sin\left(\theta(s) - \theta'(s)\right) \end{aligned} \tag{3.21}$$

The disturbance and high-frequency component present in the PD error signal can be cancelled out by the LPF (PI-controller), thus the output of the PI-controller can be written as

$$v_{df} = k_p\left(1 + \frac{1}{k_i s}\right)e_{pd}(s) \tag{3.22}$$

However, multiplier block in PD produces nonlinear phase detection (ω) and feed-forward gain can be added at the output of LPF (PI-controller) for linearization of PLL, which can be written as

$$\omega' = \left(\omega_c + \omega\right) \tag{3.23}$$

where ω_c is the centre frequency of the VCO and is supplied to the PLL as a feed-forward parameter dependent on the supply frequency range. The phase angle $\left(\theta'\right)$ can be obtained by integrating the frequency command $\left(\omega'\right)$ as

$$\theta'(t) = \int \omega' dt \tag{3.24}$$

Here the integrator of PLL is considered as plant transfer function

$$P(s) = \frac{1}{s} \tag{3.25}$$

Then, the transfer function of the LPF is defined as

$$LF(S) = \frac{k_p\left(s + \frac{k_i}{k_p}\right)}{s} \tag{3.26}$$

Thus, the open loop transfer function becomes

$$GOL(s) = p(s) * LF(s) = \frac{k_p s + \frac{k_p}{k_i}}{s^2} \tag{3.27}$$

The closed-loop transfer function can be written as

$$G_\theta(s) = \frac{\theta'(s)}{\theta(s)} = \frac{GOL(s)}{1+GOL(s)} = \frac{k_p s + \frac{k_p}{k_i}}{s^2 + k_p s + \frac{k_p}{k_i}} \tag{3.28}$$

Then the closed-loop negative feedback transfer function becomes

$$e'_{pd} = 1 - G_\theta(s) = \frac{s^2}{s^2 + k_p s + \frac{k_p}{k_i}} \tag{3.29}$$

From Eq. (3.29), the relation of e'_{pd} with the second order transfer function becomes

$$H_\theta(s) = \frac{\omega_n}{s^2 + 2\delta\omega_n s + \omega_n^2} \tag{3.30}$$

Equating the Eq. (3.29) and Eq. (3.30), k_p and k_i are determined as

$$k_p = 2\delta\omega_n \text{ and } k_i = \frac{2\delta}{\omega_n} \tag{3.31}$$

where δ is the damping coefficient equal to 0.707 and ω_n is the natural frequency with consideration of settling time equal to 1sec, based on the settling time $t_s = 1$s.

It is observed from the open loop transfer-function of MPLL defined in Eq. (3.27) that it is of type-2 structure with two poles lying in origin, which indicates that it can perfectly track the constant and variable slope of input phase angle without any delay. Moreover, Eq. (3.28) reveals that MPLL presents a low-pass filtering characteristics in the detection of the input phase angle, which is a very interesting feature for reducing the detection error caused by possible distortion, noise and high order harmonics in the input signal.

3.3.3 Proposed SRF based Reference signal generation technique

The control structure of UPQC depicted in Fig.3.5 presents a novel control strategy based on the SRF for generation of reference current as well as reference voltage signal. The proposed control technique is simple and easy to implement with lessened current measurement technique. The reference source current signal generation algorithm utilizes only source voltage and dc-link voltage. The source voltages are first applied to MPLL, and then three phase unit vector signals are generated from it.

The unit vector signals are transformed to $d-q-0$ coordinate to obtain the real component (u_d) and reactive components(u_q). Some active power should be absorbed from the power system by the shunt inverter for regulating the dc-link voltage. For this purpose, the dc-link voltage V_{dc} is compared with its reference value V_{dc_ref} and the required peak value of the source current I_{max} is obtained from NVGF controller. The source current fundamental reference components$(i'_{sd}$ and $i'_{sq})$ are calculated by multiplying I_{max} with real component u_d and reactive component u_q respectively.

$$i'_{sd} = I_{max} \times u_d \tag{3.32}$$

$$i'_{sq} = i_{max} \times u_q \tag{3.33}$$

The three phase source reference currents are calculated by taking the inverse $d-q-0$ transformation of i'_{sd} and i'_{sq}. The source reference currents$(i_{sa}, i_{sb}$ and $i_{sc})$ are subtracted from the load current $(i_{la}, i_{lb}$ and $i_{lc})$ to produce compensating reference currents $\left(i_{ca\_ref}, i_{cb\_ref}\right.$ and $\left.i_{cc\_ref}\right)$. The compensating reference currents and measured compensating currents (i_{ca}, i_{cb}, i_{cc}) are compared by a hysteresis current controller for producing switching signals for shunt APF.

The generation of reference compensating voltage $(V_{c(abc)\_ref})$ deals with compensation of power quality (PQ) problems such as source voltage sag, swell, voltage distortion and supply voltage unbalance. The proposed algorithm utilizes only supply voltage V_{sabc} and $d-q-0$ transformation to obtain real and reactive component (Vs_{d-q}).The peak detector utilized in the control algorithm detects the peak value of supply voltage V_{sp}. This constant magnitude value V_{sp} is further multiplied with unit vector template $(u_a, u_b$ and $u_c)$ generated from MPLL block to produce the reference source voltage component$(V_{s_ref(dq)})$ .The reference compensating component Vc^*_{d-q} is obtained by subtracting $V_{s\_ref(d-q)}$ from the required value of Vs_{d-q} as shown in Eq. (3.34).

$$Vc^*_{(d-q)} = Vs_{(d-q)} - V_{s\_ref(d-q)} \tag{3.34}$$

The three phase compensating reference voltages $(V_{c(abc)\_ref})$ are obtained by taking inverse transformation of $Vc^{*}_{(d-q)}$. The generated compensating reference voltages and measured compensating voltages $V_{c(abc)}$ are compared in the hysteresis voltage controller to produce the switching pulses for series APF.

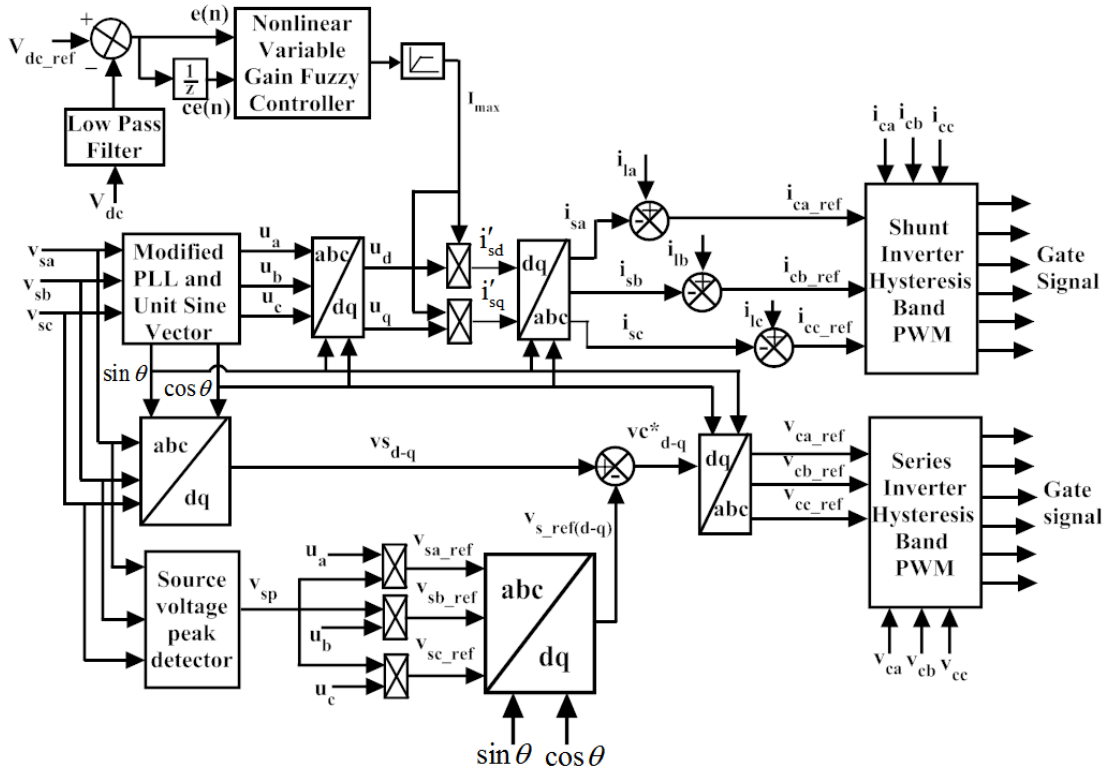


Fig.3.5 Proposed NVGF with MSRF based control structure of UPQC

3.4 Design of nonlinear sliding mode control and novel switching dynamic control strategy

In sub-section (3.3.1), NVGF controllers have been proposed for controlling the DC-link voltage. This controller fails to regulate the DC-link voltage during fast transient conditions of system load and system uncertainty condition due to the failure of system components in the power distribution network. Hence, the DC-link voltage of the UPQC can significantly deviate from its reference value and takes finite time interval to return to its original value, resulting in performance degradation of UPQC compensation process. To ensure high performance UPQC system, the DC-link voltage should settle quickly with a low overshoot. It is a well-comprehended certainty that a low overshoot can be accomplished with high settling time and vice versa, which is not desirable in UPQC as DC-link capacitor

voltage can control the operation of both shunt and series converter. The proposed NLSMC solves this particular problem, which is a combination of composite nonlinear feedback (CNF) technique and SMC technique.

In this section nonlinear sliding mode controller (NLSMC) is proposed for controlling the DC-link voltage and a novel switching dynamics is designed for controlling switching frequency of UPQC for improving the PQ problems such as current harmonics, supply voltage sag/swell, supply voltage unbalance and voltage distortion of power distribution network. NLSMC can vary a system's closed loop damping ratio in its nonlinear surface. At first, the nonlinear surface preserves the damping ratio at a low value and regularly varies it towards an ultimate high value to guarantee a fast response, when DC-link voltage approaches a set point. Furthermore, an improved switching dynamics for hysteresis band (HB) has been designed along with the SRF based reference generation technique in UPQC. The HB is controlled by variation of reference signals, DC-link capacitor voltage, compensating current and compensating voltage in order to maintain switching frequency constant under any operating conditions, whereas SRF algorithm is utilized within its control structure for rapid extraction of reference signal useful for HB calculation. This switching dynamics control technique preserves entire benefits of band controller and avoids disturbances such as a frequent band violation. The proposed control technique is validated through extensive simulation and real-time experimental studies are accomplished by using HIL system in OPAL-RT simulator (OP5600) with OP5142 Xilinx SPARTAN-3(3xc3s5000) field programmable gate array (FPGA) processor for user interconnection. A comparative assessment has been performed between proposed NLVGF modified SRF control strategy and proposed NLMSC modified SRF controller technique.

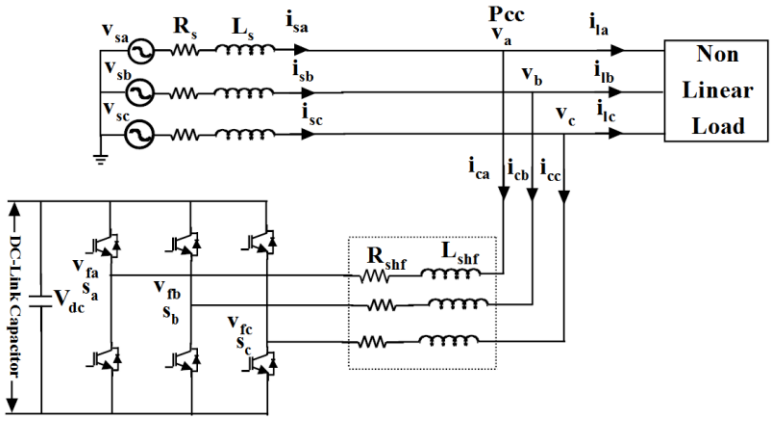
3.4.1 Nonlinear sliding mode control scheme for DC-link voltage control

Generally the shunt APF of UPQC is responsible for DC-link voltage regulation. Thus, the proposed NLSMC scheme is designed for a shunt APF for DC-link voltage regulation. Schematic diagram of the shunt APF is depicted in Fig.3.6 (a). The conventional dynamic equations of plant model in a d-q frame are presented in Eq. (3.35) and (3.36). The plant system representation model is depicted in Fig.3.6 (b) and the step response of proposed NLSMC scheme with initial and final damping ratio and settling time is displayed in Fig.3.6

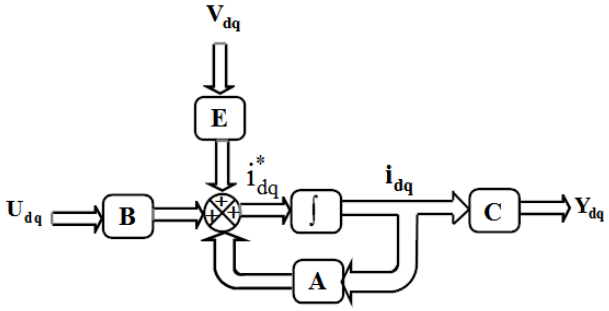
(c). From this step response, it can be seen that both peak overshoot and settling time are essentially low on account of the proposed NLSMC scheme.

$$\frac{dX}{dt} = AX + Bu_{dq} + Ev_{dq} \tag{3.35}$$

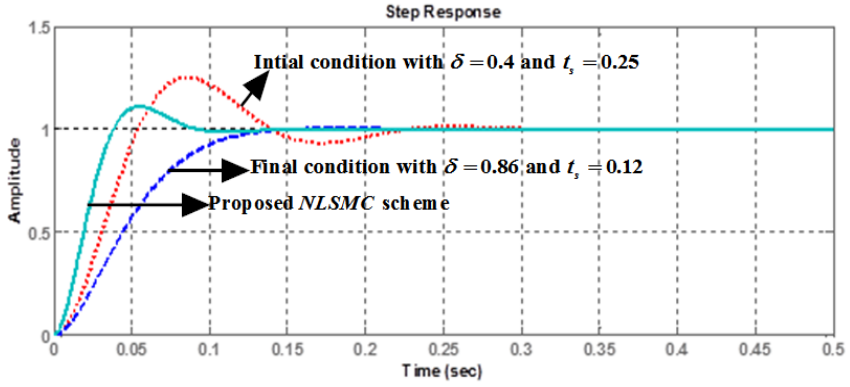
$$y_{dq} = CX \tag{3.36}$$



(a)



(b)



(c)

Fig.3.6 System configuration and response of UPQC, (a) Schematic diagram of shunt voltage source inverter, (b) System representation of part of the plant model of shunt APF, (c) Step response of the proposed method with initial and final condition of damping ratio and settling time.

where,

$$X = \left[i_d, i_q, V_{dc} \right]^T,$$

$$A = \begin{bmatrix} -\frac{R_{shf}}{L_{shf}} & \omega & -\frac{u_d}{L_{shf}} \\ -\omega & -\frac{R_{shf}}{L_{shf}} & -\frac{u_q}{L_{shf}} \\ \frac{3u_d}{2c_{dc}} & \frac{3u_q}{2c_{dc}} & 0 \end{bmatrix}, B = \begin{bmatrix} -\frac{V_{dc}}{L_{shf}} & 0 \\ 0 & -\frac{V_{dc}}{L_{shf}} \\ \frac{3i_{f\_d}}{2c_{dc}} & \frac{3i_{f\_q}}{2c_{dc}} \end{bmatrix}, E = \begin{bmatrix} \frac{1}{L_{shf}} & 0 \\ 0 & \frac{1}{L_{shf}} \\ 0 & 0 \end{bmatrix},$$

$$c = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

where X , u_{dq} , v_{dq} and y_{dq} represent the state-space vector, control input vector, input disturbance vector and control output vector respectively. The switching function s_k of the k^{th} leg of the VSI is defined as

$$s_k = \begin{cases} 1, if\ T_k\ is\ on\ and\ T_k^{'}\ is\ off \\ 0, if\ T_k\ is\ off\ and\ T_k^{'}\ is\ on \end{cases} \tag{3.37}$$

Assume $v_{ck} = s_k V_{dc}$, switching state action u_{nk} is characterized as

$$u_{nk} = \left(s_k - \frac{1}{3} \sum_{j=1}^{3} s_j \right) \tag{3.38}$$

In order to acquire a quick dynamic response, the switching state function u_d and u_q are defined from Eq. (3.35).

$$\begin{aligned} u_d &= \frac{\lambda_d + L_{shf}\, \omega\, i_{c\_q} + v_d}{V_{dc}} \\ u_q &= \frac{\lambda_q - L_{shf}\, \omega\, i_{c\_d}}{V_{dc}} \end{aligned} \tag{3.39}$$

where, $\lambda = \left(\frac{di_c}{dt} \right) + \left(\frac{R_{shf}}{L_{shf}} \right) i_c$

The inputs u_d and u_q are consisting of a linear decoupling compensation term and a nonlinear term. To accomplish a quick dynamic response and zero steady-state errors, the nonlinear sliding surface for the system is defined as,

$$s(z,t) = I_{sp} = c^T z(t) = [c_1\, c_2]\begin{bmatrix} z_1(t) \\ z_2(t) \end{bmatrix} = \begin{bmatrix} F - \psi(y) A_{12}^T p & 1 \end{bmatrix}\begin{bmatrix} z_1(t) \\ z_2(t) \end{bmatrix} \tag{3.40}$$

where, I_{sp} is the peak value of supply current, F is the linear gain matrix, $\psi(y)$ is the nonlinear function, P is the positive-definite matrix and A_{12}^T can be defined from Eq. (3.35) by representing it to be a regular form.

$$A_{reg} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \tag{3.41}$$

where $A_{11} = \begin{bmatrix} -\frac{R_{shf}}{L_{shf}} & \omega \\ -\omega & -\frac{R_{shf}}{L_{shf}} \end{bmatrix}, A_{12} = \begin{bmatrix} -\frac{u_d}{L_{shf}} \\ -\frac{u_q}{L_{shf}} \end{bmatrix}, A_{21} = \begin{bmatrix} \frac{3u_d}{2c_{dc}} & \frac{3u_q}{2c_{dc}} \end{bmatrix}, A_{22} = 0$

The value of $z_1(t)$ and $z_2(t)$ of Eq. (3.40) are defined as

$$z_1(t) = x_1 y_1 \tag{3.42}$$

$$z_2(t) = x_2 y_2 \tag{3.43}$$

where, x_1 is obtained from the average DC bus voltage V_{dc} and its reference value V_{dc_ref}.

$$x_1 = v_{en} = V_{dc\_ref(n)} - V_{dc(n)} \tag{3.44}$$

And derivative of x_1 is defined as

$$x_2 = \dot{x}_1 = \frac{1}{T}\left[v_e(n) - v_e(n-1)\right] \tag{3.45}$$

where T is the sampling time.

In sliding mode approach, the switching function values y_1 and y_2 are defined as follows.

$$\begin{aligned} y_1 &= +1 \quad if\ gx_1 > 0 \\ &= -1 \quad if\ gx_1 < 0 \\ y_2 &= +1\ if\ gx_2 > 0 \\ &= -1\ if\ gx_2 < 0 \end{aligned} \tag{3.46}$$

where g is the switching function and can be represented as $g = c_3 x_1 + c_4 x_2$. c_3, c_4 are constants.

The nonlinear sliding surface defined in Eq. (3.40) is composed of a linear and nonlinear term. Primarily nonlinear terms are zero and subsequently the linear term chooses initial damping ratio δ_1 and settling time t_s. From Eq. (2.40) $c_2 = 1$ and c_1 can be defined as

$$c_1 = F - \Psi(y) A_{12}^T P \tag{3.47}$$

Here F is designed for initial low damping ratio $(\delta_1 = 0.4)$ and initial high settling time $(t_{s1} = 0.25)$ and a matrix of F can be found by using the pole placement technique. Locations of the poles are at $\left(-\delta + \sqrt{\delta^2 - 1}\right)\omega_n$ and $\left(-\delta - \sqrt{\delta^2 - 1}\right)\omega_n$, where the value of natural frequency of oscillation ω_n can be calculated from known values of the damping ratio δ and the settling time t_s. Thus, ω_n can be written as $\omega_n = 4/(\delta t_s)$. Accordingly poles of the close-loop system are found to be placed at $-16 \pm 36.6606i$. Using pole placement technique, the gain matrix is found as $F = [0.1738 \;\; 0.9723]$. Considering final damping ratio as $\delta_2 = 0.86$ and settling time as $t_{s2} = 0.12$, the required gain matrix k_2 can be computed as $k_2 = [0.0804 \;\; 0.9888]$ using pole placement technique.

The nonlinear function $\psi(y)$ changes from 0 to $-\beta$ as output changes from its initial value to final value. It is given in [100,101,102] that the introduction of this function changes the damping ratio of the system from its initial value (δ_1) to the final value (δ_2), where $\delta_2 > \delta_1$. When $\psi(y)$ is zero at $t = 0$, the damping ratio (δ_1) is contributed by F. When its output reaches the final value, the steady state value of $\psi(y)$ becomes $\psi(y) = -\beta$ and the final damping ratio (δ_2) is contributed by k_2. Therefore, $\psi(y)$ can be written as

$$\psi(y) = -\beta e^{-\bar{\alpha} y^2} \tag{3.48}$$

where $\bar{\alpha}$ is a positive constant that should have a large value to ensure a small initial value of ψ, y is the dc-link voltage and β is the tuning parameter, which is determined by the required gain of (k_2) and (F). Thus, the resulting equation is defined as

$$k_2 = F + \beta A_{12}^T P \tag{3.49}$$

In order to realize the desired damping ratio, the above equation can be equivalently expressed as

$$\beta = \frac{k_2 - F}{A_{12}^T P} \tag{3.50}$$

Eq. (3.50) decides the value of β .This parameter helps to choose the damping ratio in conjunction with matrix P , which is determined using LMI technique based on Eq. (3.51) as follows

$$\left(A_{11} - A_{12}F\right)^T P + P\left(A_{11} - A_{12}F\right) = -Q \tag{3.51}$$

where, $p \in R^{2\times 2}$ can be chosen based on the desired final damping ratio δ_2 and Q is the positive-definite matrix.

3.4.2 Proposed SRF based control strategy

The SRF-based control strategy is depicted in Fig. 3.7. The SRF control method is one of the best methods for generation of reference signal during disturbance and uncertainty condition of power system network [43]. For generation of reference signal, the source voltages are applied to a MPLL block, where three phase unit vector signals and sine-cosine signals are generated as described in subsection-3.3.2 . Three phase unit vector signals are transformed to $d-q-0$ coordinate to obtain real component (u_d) and reactive component (u_q). These components are multiplied with the peak amplitude of the source current (I_{sp}), generated using NLSMC scheme and get inverse transformed to $a-b-c$ coordinate for generating the source reference current. Compensating reference current (i_{c_ref}) is obtained by taking the difference between the load current and source reference current. For series APF, the reference voltage generation can be used for solving the voltage power quality (PQ) problems. The control structure is primarily dependent on the integration of source voltage feed-forward $(V_{S(d-q)})$ and load voltage feedback $(V_{L(d-q)})$.The feed-forward controller delivers the essential transient response and calculates the required compensating voltage (V_{c_dq}) by taking difference between the supply voltage (Vs_{d-q}) and load reference voltage $(V_{Load\_ref(d-q)})$. However, it doesn't consider voltage losses due to drop across the injection transformer and LC filters.

Therefore closed loop voltage feedback compensation V_{Lc_dq} is added to minimize losses by passing the difference between load voltage $(V_{L(d-q)})$ and reference load voltage $(V_{Load\_ref\,(d-q)})$ through the PI controller (kp=0.20 and ki=2.40, Refer Appendix-2). These losses are added to the injected compensating voltage V_{c_dq} to produce compensating reference voltage V_{c_dq-ref} and finally inverse transformation is performed to obtain reference compensating voltages V_{c_ref}.

3.4.3 Analysis of switching dynamics in shunt APF

Design of switching dynamics of shunt APF is a significant concern for controlling the switching band of hysteresis controller in transient condition. Instead of considering three-phase VSI, a single phase VSI supported the DC-link capacitor is taken into account for simpler analysis. Fig.3.8 (a) shows schematic circuit for a single-phase shunt APF and tracking of the reference current i_{ca_ref} is presented in Fig.3.8 (b).

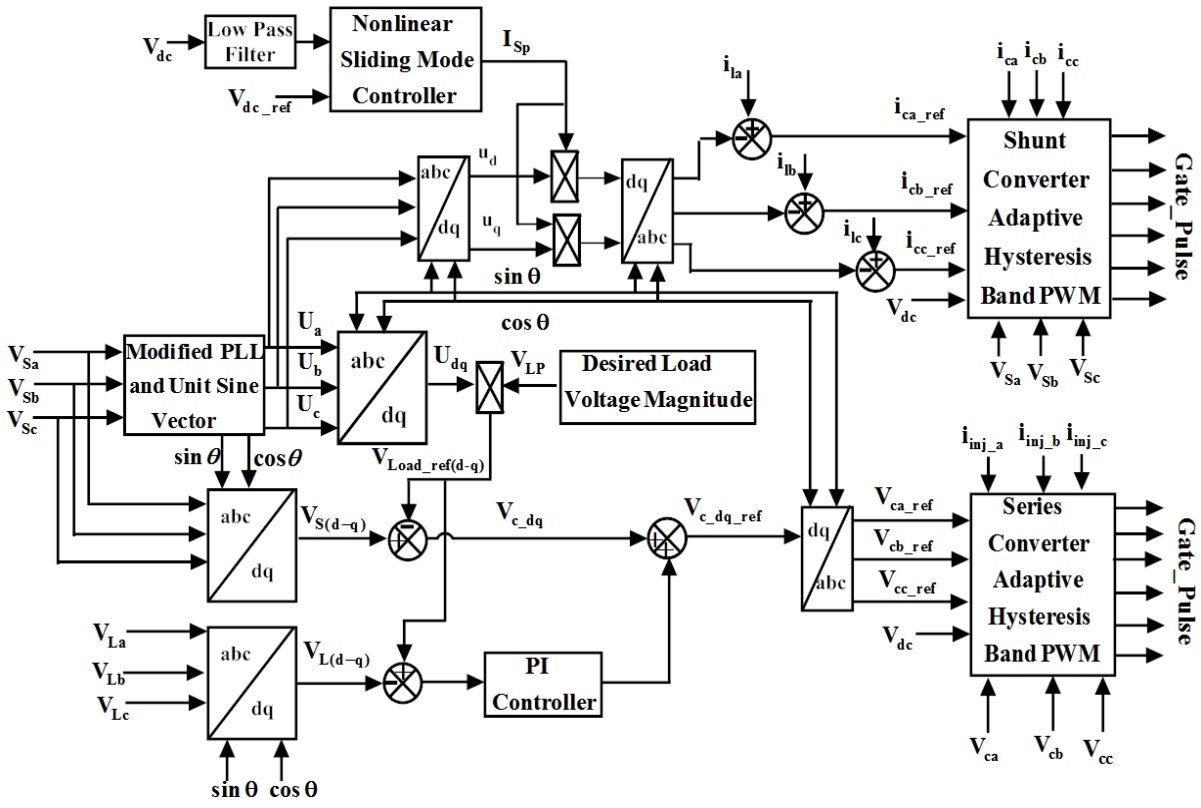


Fig.3.7 Proposed NLSMC with MSRF based control strategy for UPQC.

The higher and lower boundary limits are generated by adding and deducting hysteresis band for the compensating reference current. For tracing a positive reference current at particular time t', switch Q_1 is closed and Q_2 is opened, as a result of which capacitor voltage $\left(\frac{V_{dc}}{2}\right)$ is linked to inverter and also the reference current i_{ca}^{+} increases from $(i_{ca\_ref}-h)$ to $(i_{ca\_ref}+h)$. When it reaches a higher limit $(i_{ca\_ref}+h)$, the reference current i_{ca}^{-} needs to be fetched towards the lower band. To achieve this event, switch Q_1 is opened and Q_2 is closed and consequently capacitor voltage $\left(\frac{-V_{dc}}{2}\right)$ is coupled to the shunt APF for rising of negative reference current slope from instant t'' to t'''.

For designing the switching band, current waveform within a modulation cycle is considered as shown in Fig.3.8 (b). When switch Q_1 conducts, the corresponding voltage equation becomes

$$\frac{V_{dc}}{2}-V_a-i_{ca}R_{shfa}-L_{shfa}\frac{di_{ca}}{dt}=0 \tag{3.52}$$

Thus

$$\frac{di_{ca}}{dt}=\frac{1}{L_{shfa}}\left(\frac{V_{dc}}{2}-V_a-i_{ca}R_{shfa}\right) \tag{3.53}$$

$$\frac{di_{ca}}{dt}=\frac{2HB}{t_{1on}} \tag{3.54}$$

Then on-time (t_{1on}) becomes

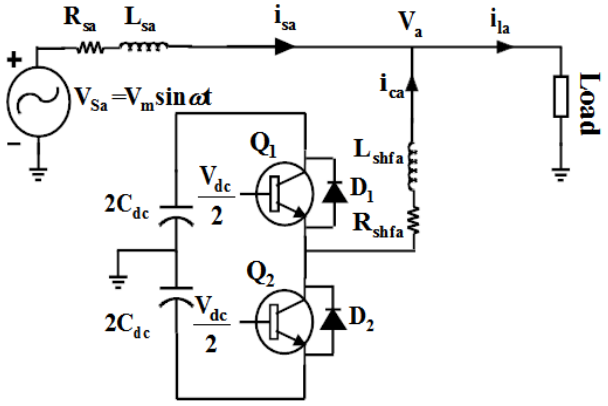
$$t_{1on}=\frac{2HB}{\frac{di_{ca}}{dt}} \tag{3.55}$$

Applying the value of di_{ca}/dt in the Eq. (3.55), t_{1on} becomes

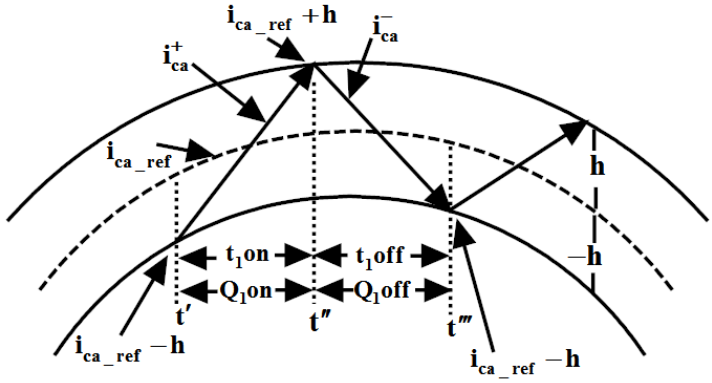
$$t_{1on}=\frac{2HBL_{shfa}}{\frac{V_{dc}}{2}-V_a-i_{ca}.R_{shfa}} \tag{3.56}$$

Similarly, when switch Q_2 conducts, the voltage equation becomes

$$-\frac{V_{dc}}{2}-V_a-i_{ca}R_{shfa}-L_{shfa}\frac{di_{ca}}{dt}=0 \tag{3.57}$$



(a)



(b)

Fig.3.8. Switching dynamics analysis for the shunt APF, (a) Schematic circuit of equivalent single phase shunt APF, (b) Schematic diagram of switching dynamics for shunt APF.

Thus

$$\frac{di_{ca}}{dt}=\frac{1}{L_{shfa}}\left(-\frac{V_{dc}}{2}-V_a-i_{ca}R_{shfa}\right) \tag{3.58}$$

The negative rise of current through the period $t^{"}$ to $t^{'''}$ becomes

$$\frac{di_{ca}}{dt}=\frac{-2HB}{t_{1off}} \tag{3.59}$$

Then off-time (t_{1off}) becomes

$$t_{1off}=\frac{-2HB}{\frac{di_{ca}}{dt}} \tag{3.60}$$

Applying the value of di_{ca}/dt in the Eq. (3.60), t_{1off} becomes

$$t_{1off} = \frac{2HBL_{shfa}}{\frac{V_{dc}}{2} + V_a + i_{ca}R_{shfa}} \tag{3.61}$$

The switching frequency (f_c) is obtained by adding Eq. (3.56) and (3.61).

$$f_c = \frac{1}{t_{1on} + t_{1off}} = \frac{1}{\left(\frac{2HBL_{shfa}}{\frac{V_{dc}}{2} - V_a - i_{ca}R_{shfa}}\right) + \left(\frac{2HBL_{shfa}}{\frac{V_{dc}}{2} + V_a + i_{ca}R_{shfa}}\right)} \tag{3.62}$$

Eq. (3.63) can be obtained after simplifying Eq. (3.62).

$$f_c = \frac{1}{V_{dc}\,2HBL_{shfa}}\left[\frac{V_{dc}^2}{4} - (V_a + i_{ca}R_{shfa})^2\right] \tag{3.63}$$

From Eq. (3.63), the hysteresis band can be obtained as,

$$HB = \frac{1}{V_{dc}\,2f_cL_{shfa}}\left[\frac{V_{dc}^2}{4} - (V_a + i_{ca}R_{shfa})^2\right] \tag{3.64}$$

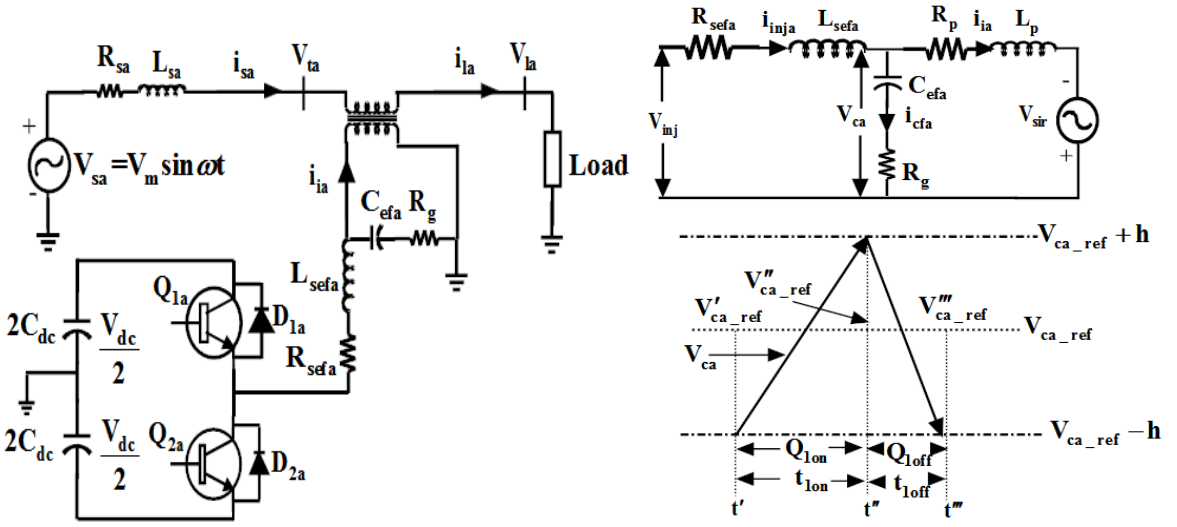
where V_a , V_{dc} , L_{shfa} and i_{ca} are the source voltage, dc-link voltage, coupling inductor and compensating current respectively. For symmetrical operation of all three phases, it can be expected that HB profiles HB_a, HB_b, HB_c will almost be same, but have a phase difference.

3.4.4 Analysis of switching dynamics in series APF

The primary function of a series APF is to suppress the sag/swell, voltage distortion and voltage unbalance from supply voltage. To accomplish this job accurately, the appropriate design of switching band is an important concern. The boundaries of switching band are created using a hysteresis band (h) as well as the reference voltage V_{ca_ref} , the lower and higher boundaries are defined as ($V_{ca\_ref} + h$) and ($V_{ca\_ref} - h$) respectively.

To make the analysis easier, a single phase series APF having a dc-link capacitor is taken into account as illustrated in Fig.3.9 (a). A single phase equivalent of series APF with exterior circuit parts is presented in Fig.3.9 (b), where R_g is the switching band resistor, added in series with filter capacitor to make the switching band more linear in comparison to

the switching band present during only capacitor filter, V_{sir} is the equivalent voltage source and $Z_p = (R_p + jwL_p)$ is the equivalent impedance exterior to the series APF. To originate a relation involving switching frequency along with some additional parameters, one period of switching action is demonstrated in Fig.3.9 (b). Since both positive and negative reference voltages are same for band control operation, we take into account first positive reference voltage.



(a) (b)

Fig.3.9. Switching dynamics analysis for the series APF, (a) Schematic circuit of equivalent single phase series APF, (b) Equivalent circuit of series APF by exterior circuit and switching action of band control.

When switch Q_{1a} is on, a positive dc-link voltage $+\frac{V_{dc}}{2}$ is applied over the filter elements. Applying KVL (Kirchhoff's voltage law) and KCL (Kirchhoff's current law), following equations are obtained.

$$L_{sefa}\frac{di_{inja}}{t_{1on}} = \frac{V_{dc}}{2} - R_{sefa}i_{inja} - V_{ca} \tag{3.65}$$

$$di_{inja} = di_{ia} + di_{cfa} \tag{3.66}$$

Injection current is slowly varied in nature in comparison to the capacitor current. Thus variation of inverter current is nearly equal to the variation in the capacitor current without losing accuracy. Thus Eq. (3.66) becomes

$$di_{inja} = di_{cfa} \tag{3.67}$$

Rearranging the aforementioned equation for calculating the length of positive slope, t_{1on} can be obtained as,

$$t_{1on} = \frac{L_{sefa} di_{cfa}}{\frac{V_{dc}}{2} - R_{sefa} i_{inja} - V_{ca}} \tag{3.68}$$

Further a negative slope is obtained by making the switch Q_{2a} on. This provides a inverter output voltage as $-\frac{V_{dc}}{2}$. The series APF voltage is discharged through capacitor current to reach the lower limit of $(V_{ca\_ref} - h)$. Similar to positive slope, the following equations are obtained for negative slope.

$$L_{sefa} \frac{di_{inja}}{t_{1off}} = \frac{V_{dc}}{2} + R_{sefa} i_{inja} + V_{ca} \tag{3.69}$$

$$di_{inja} = -di_{cfa} \tag{3.70}$$

$$t_{1off} = \frac{L_{sefa} di_{cfa}}{\frac{V_{dc}}{2} + R_{sefa} i_{inja} + V_{ca}} \tag{3.71}$$

Thus the complete time length of one switching period can be calculated as

$$T_{sw} = t_{1on} + t_{1off} = \frac{4V_{dc}}{V_{dc}^2 - (2R_{sefa} i_{inja} + 2V_{ca})^2} L_{sefa} di_{cfa} \tag{3.72}$$

Modification in capacitor current di_{cfa} may be found from the capacitor dynamic equation

$$V_{ca} = \frac{1}{C_{efa}} \int i_{cfa} dt + R_g i_{cfa} \tag{3.73}$$

Differentiating the aforementioned equation, the variation of the capacitor current can be defined as

$$di_{cfa} = \frac{1}{R_g} \left(dV_{ca} - \frac{i_{cfa} t_{1on}}{C_{efa}} \right) \tag{3.74}$$

Since series APF voltage (V_{ca}) is excellently tracking the reference voltage $\left(V_{ca\_ref}\right)$, then $V_{ca} = V_{ca\_ref}$.

Because of a negligible voltage drop across the capacitor at high frequency, the variation of capacitor voltage is minimized. Thus

$$\begin{cases} dV_{ca} = \left(V'_{ca\_ref} + h\right) - \left(V_{ca\_ref} - h\right) = 2HB \\ \dfrac{(i_{cfa} t_{1on})}{C_{efa}} = dV_{cfa} = 0 \end{cases} \tag{3.75}$$

Substituting Eq. (3.75) in Eq. (3.74), the variation of capacitor current is procured as

$$di_{cfa} = \frac{2HB}{R_g} \tag{3.76}$$

Substituting Eq. (3.76) in Eq. (3.72), the time required for one switching period is obtained as

$$T_{sw} = \frac{L_{sefa} 8HBV_{dc}}{R_g \left[V_{dc}^2 - (2R_{sefa} i_{inja} + 2V_{ca})^2\right]} \tag{3.77}$$

A fundamental component can only be assumed in the reference voltage and the switching frequency of the band controller can be expressed as

$$f_{sw} = \frac{R_g \left[V_{dc}^2 - 4(R_{sefa} i_{inja} + V_{ca})^2\right]}{L_{sefa}\, 8HBV_{dc}} \tag{3.78}$$

From Eq. (3.78), it is perceived that the switching frequency relies on R_g / L_{sf} ratio, capacitor voltage, voltage drop in filter resistance, reference voltage and band (h). Simplifying Eq. (3.78), the hysteresis band for series APF is obtained as

$$h = \frac{R_g}{V_{dc}\, 2 f_{sw} L_{sefa}} \left[\frac{V_{dc}^2}{4} - (R_{sefa} i_{inja} + V_{ca})^2\right] \tag{3.79}$$

3.5 Performance analysis

3.5.1 Simulation and real-time HIL based OPAL-RT result of NVGF based modified SRF theory

To verify the effectiveness of UPQC, the proposed control strategy has been tested using MATLAB/SIMULINK and real-time HIL based OPAL-RT system. The system parameters are given in the Appendix-1. For simulation and experimental analysis, a step change of load at 0.15 s is considered for transient performance. Further, 20% of sag/swell creation between 0.12 s to 0.18 s for 4 cycles, source voltage harmonic creation by adding 5^{th} and 7^{th} harmonics to the source voltage and voltage unbalance formation by varying of phase-*a* amplitudes up to $\pm 40\%$ from its nominal value are considered.

Fig.3.10 and 3.11 illustrate the simulation and real-time experimental results respectively for performance of PLL in voltage distortion condition. Fig.3.10 demonstrates the simulation results for the transformation angle (ωt) and unit sine vector along with the conventional PLL [60] and modified PLL from top to bottom order. Similarly, Fig.3.11 (a) and (b) show the real-time experimental result of transformation angle (ωt) for the conventional PLL and modified PLL technique respectively. From this figure it is observed that the transformation angle (ωt) of the modified PLL has a negligible oscillation under highly distorted condition in comparison to the conventional PLL. Thus, unit sine vector signal generation using modified PLL shows perfect result, where as some distortions are present in the unit sine vector generated by using conventional PLL depicted in Fig.3.11 (c) and (d). As a result modified PLL can give better performance and provide an adequate reference signal in all operating conditions of power system network.

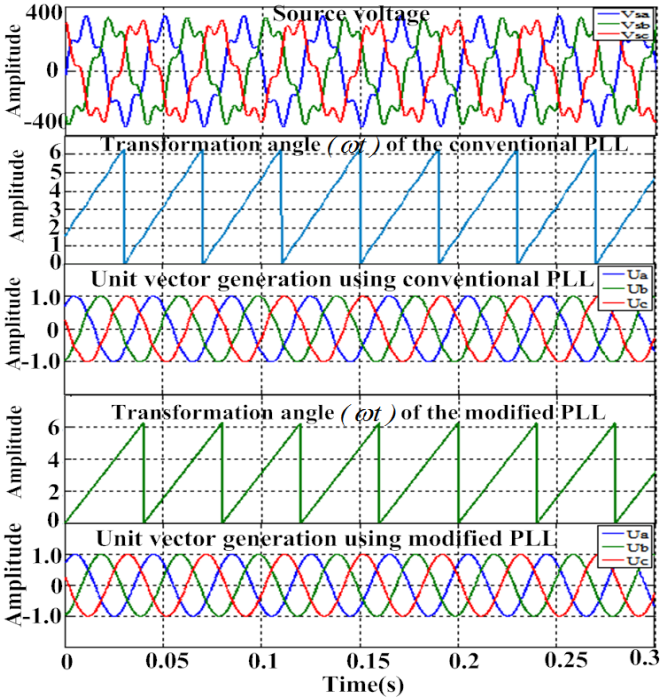


Fig.3.10 Performance of conventional and modified PLL during voltage distortion condition

Fig.3.12 and 3.13 illustrate the details of simulation and experimental results for shunt APF of UPQC during steady-state and load transient condition. Fig.3.12 (a) and (b) provide the information about compensating current and source current under steady-state condition. Fig.3.12 (c) and 3.13 (a) show the performance of NVGF Controller for controlling the dc-link voltage during transient state condition of load. The load parameters are changed to

($R_L = 25\Omega$ and $L_L = 34\,mH$) from $t = 0.15\,s$ to $t = 0.3\,s$. Fig.3.12 (d) and 3.13 (b) provide the information regarding source current before compensation and it is observed from the figure that source current is changed its current amplitude from 47 A to 67 A at t=0.15 s. Fig.3.12 (e) and (f) as well as Fig. 3.13 (c) and (d) provide the information regarding compensating current and source current after compensation respectively. It is observed from the figure that, the shunt APF performance is quite satisfactory during load side transient condition. Thus, the source current is sinusoidal in nature. Additionally, Fig.3.12 (g) and (h) convey the information regarding the THD of source current before and after compensation during steady-state condition and they are observed to be 28.3 % and 3.83 % respectively. Similarly, Fig.3.12 (i) and (j) provide the information about the THD of source current before and after compensation under transient-state condition and they are found to be 31.8 % and 4.17 % respectively.

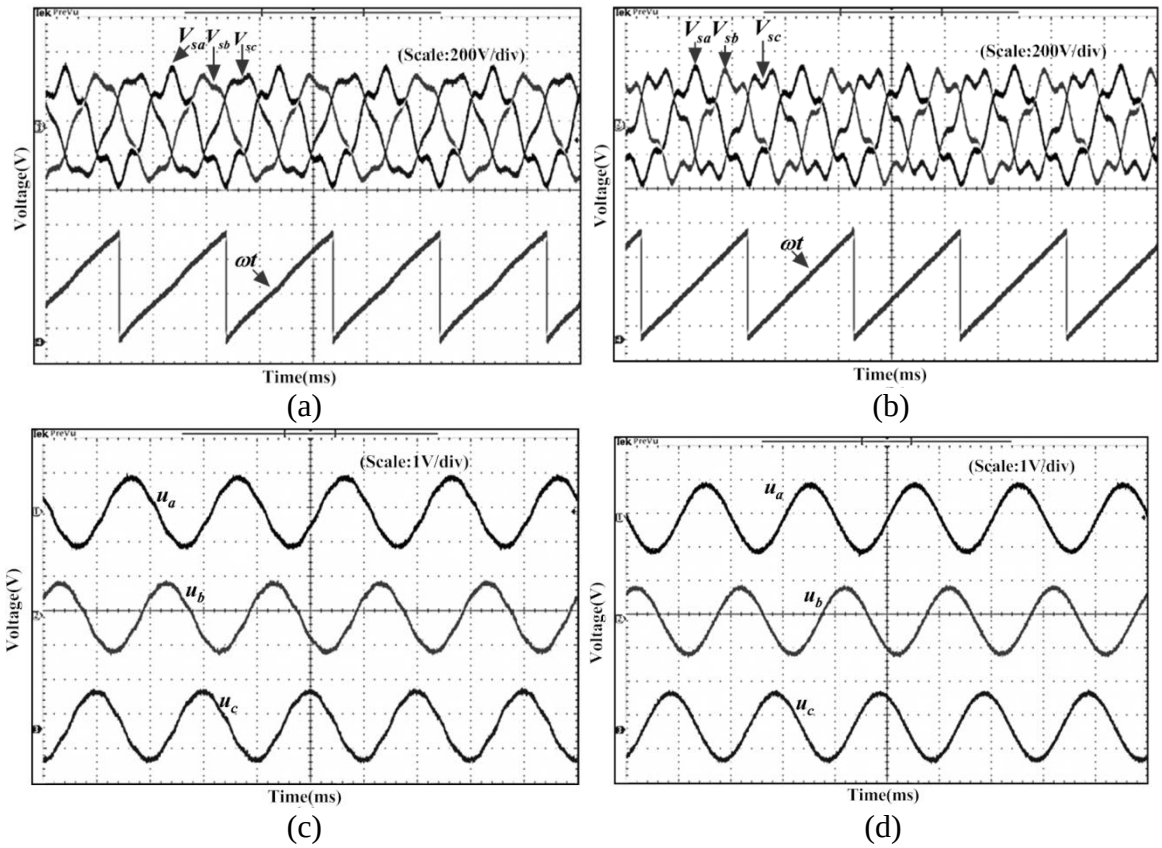


Fig.3.11 Real-time experimental results of PLL algorithm under distorted supply condition, (a) Transformation angle (ωt) of conventional PLL (scale: 2 V/div), (b) Transformation angle (ωt) of modified PLL (scale: 2 V/div), (c) Unit vector signal from conventional PLL (scale: 1 V/div), (d) Unit vector signal from modified PLL (scale: 1 V/div).

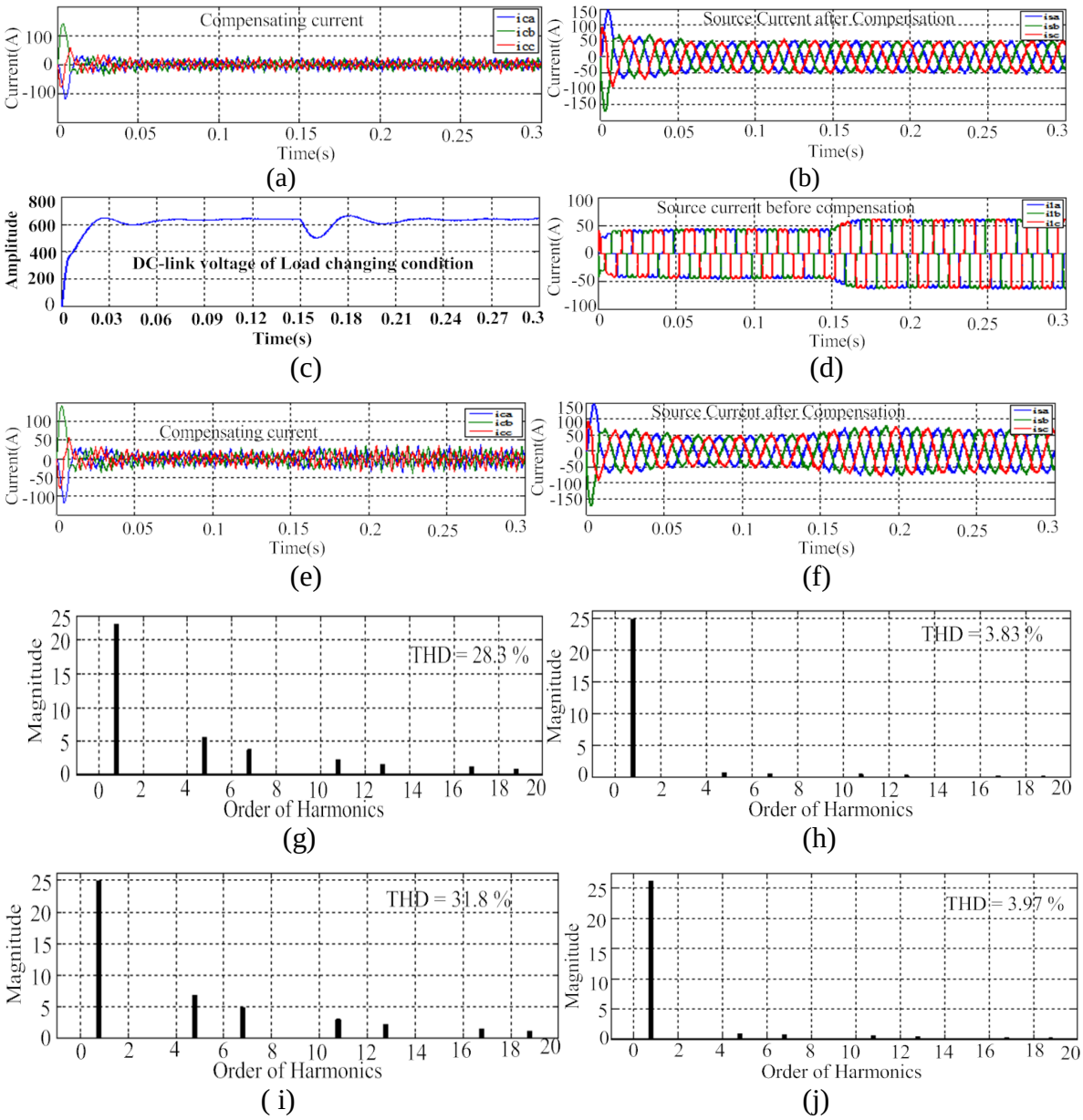


Fig.3.12 Simulation results, (a) Compensation current during steady-state condition, (b) Source current after compensation during steady-state condition, (c) dc-link voltage under transient condition, (d) Source current before compensation during transient-state condition, (e) Compensation current during transient-state condition, (f) Source current after compensation during transient-state condition, (g) Source current spectrum before compensation during steady-state condition, (h) Source current spectrum after compensation during steady-state condition (i) Source current spectrum before compensation during transient-state condition, (j) Source current spectrum after compensation during transient-state condition.

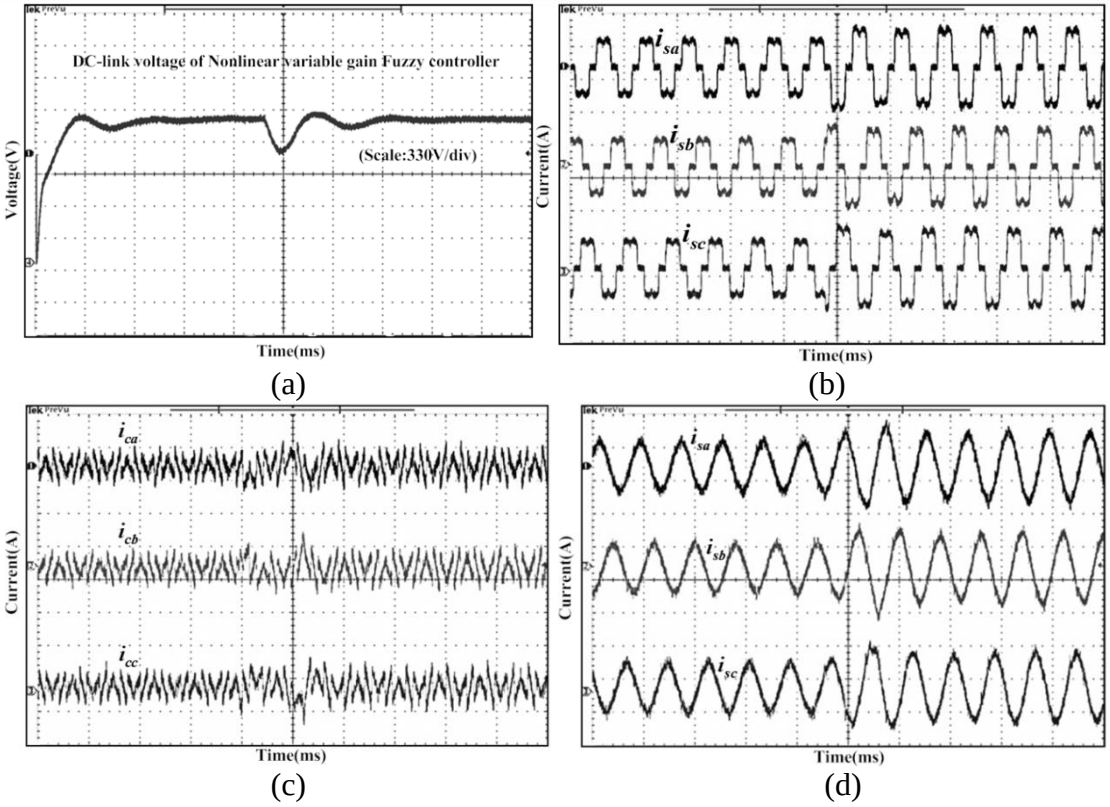


Fig.3.13 Real-time experimental results, (a) dc-link voltage under transient condition, (b) Source current before compensation (scale: 52 A/div), (c) Compensation current (scale: 40 A/div), (d) Source current after compensation (scale: 55 A/div).

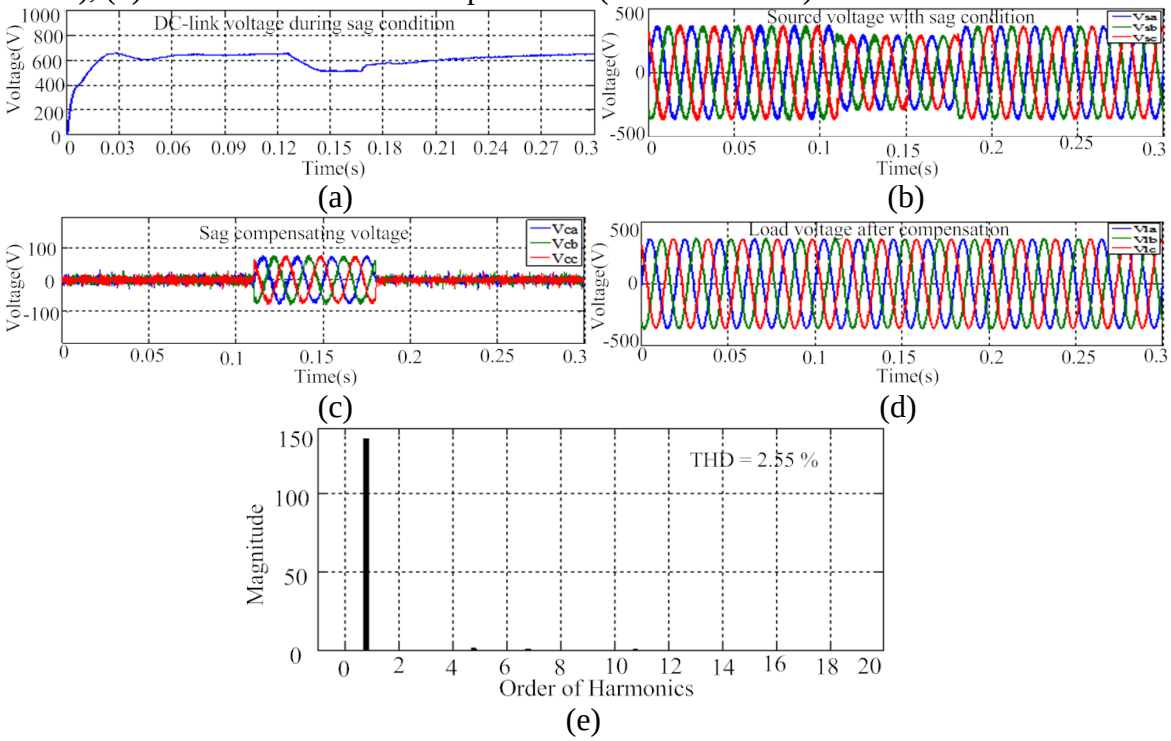


Fig.3.14 Simulation results during sag condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage, (e) Load voltage spectrum after compensation.

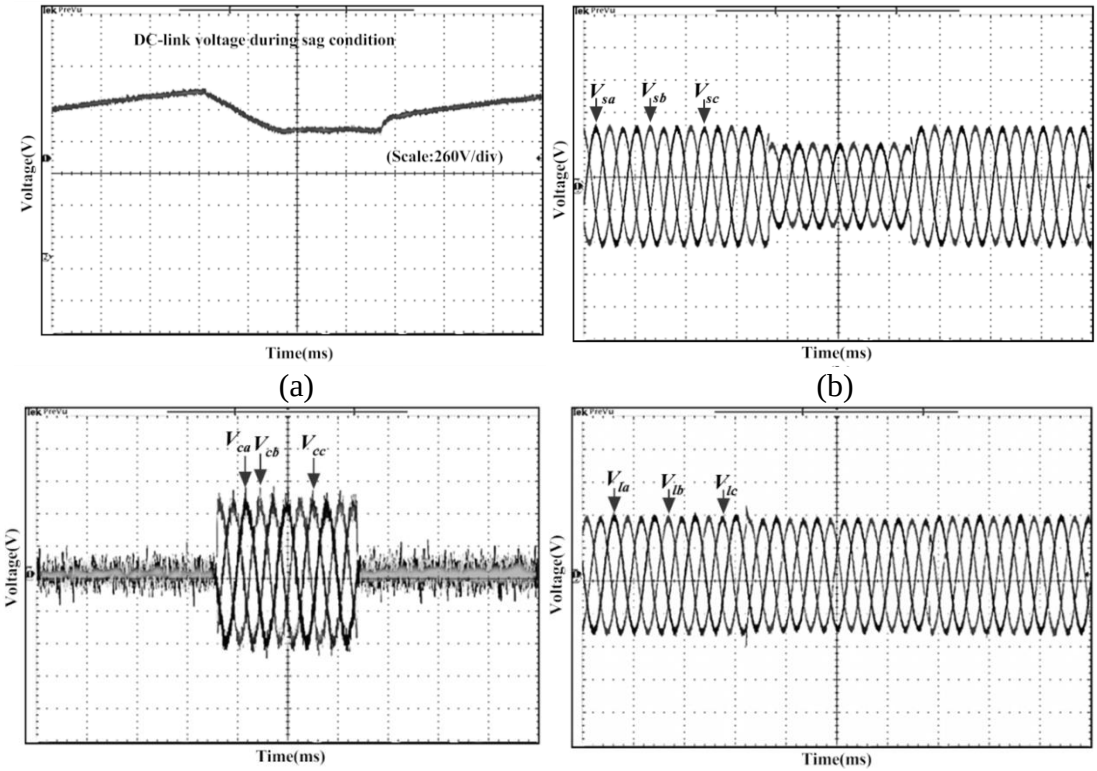


Fig.3.15 Real-time experimental results during sag condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 65 V/div), (d) Load voltage after compensation (scale: 200 V/div).

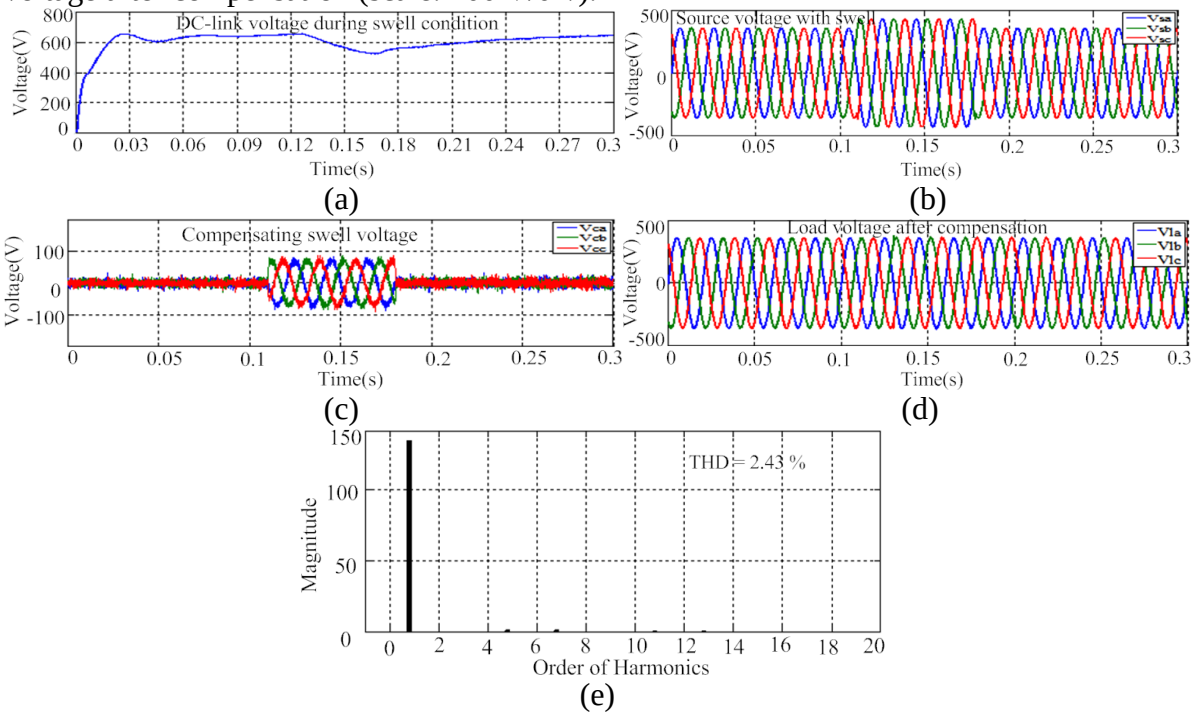


Fig.3.16 Simulation results of swell condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

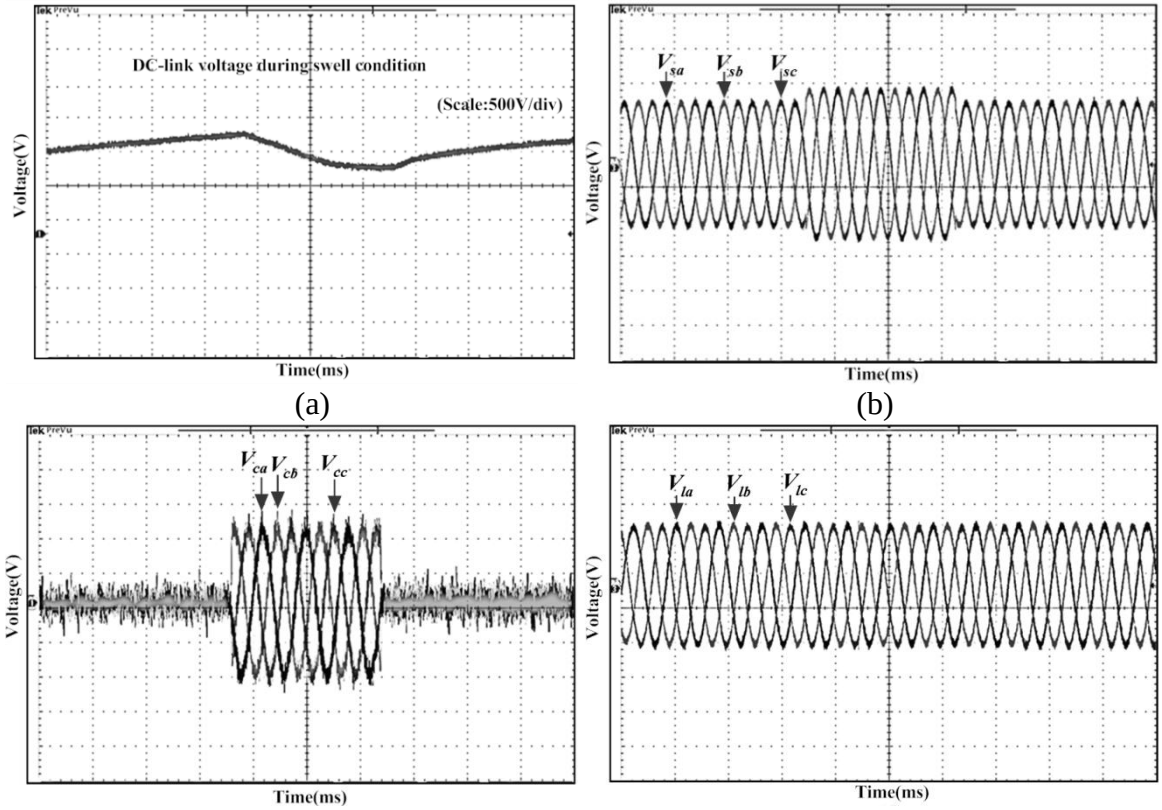


Fig.3.17 Real-time experimental results during swell condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 73 V/div), (d) Load voltage (scale: 200 V/div).

Fig.3.14 and 3.15 depict the simulation as well as real-time experimental results of dc-link voltage, supply voltage, compensating voltage and load voltage after compensation during sag voltage condition. Fig. 3.14 (a) and 3.15 (a) show the DC-link voltage of proposed method during sag condition. Fig.3.14 (b) and 3.15 (b) show the waveform of voltage sag of 4 cycles with a depth of 20 % and its corresponding compensating voltage and load voltage after compensation are shown in Fig.3.14 (c) and (d) as well as Fig.3.15 (c) and (d) respectively.

From the figure it is clear that the proposed control strategy can compensate the voltage sag accurately and regulate the load voltage to its nominal value. Fig.3.14 (e) displays THD information of load voltage after compensation and it is found to be 2.55 %. Similarly, Fig.3.16 and 3.17 illustrate the simulation as well as real-time experimental results of dc-link voltage, supply voltage, compensating voltage and load voltage after compensation

during swell conditions. Fig.3.16 (a) and 3.17 (a) show the dc-link capacitor voltage during the voltage-swell condition of proposed controller. Fig.3.16 (b) and 3.17 (b) show the waveform of voltage swell of 20 % obtained for 4 cycles and its corresponding compensating voltage and load voltage are shown in Fig. 3.16 (c) and (d) as well as Fig.3.17 (c) and (d) respectively.

It is observed from the figure that the proposed control strategy can compensate the voltage swell existing in the supply voltage and regulate the load voltage to its nominal value. Fig. 3.16 (e) shows the information regarding THD spectrum of load voltage after compensation, and its THD is around 2.43 %. Fig.3.18 (a) and 3.19 (a) provide information about simulation as well as experimental results of dc-link capacitor voltage during unbalanced supply voltage condition. Fig.3.18 (b), (c) and (d) as well as Fig.3.19 (b), (c) and (d) show the unbalanced source voltage, compensating voltage and load voltage after compensation of the proposed method respectively. Fig. 3.18 (e) shows the THD spectrum of load voltage after compensation and it is found to be 2.88 %.

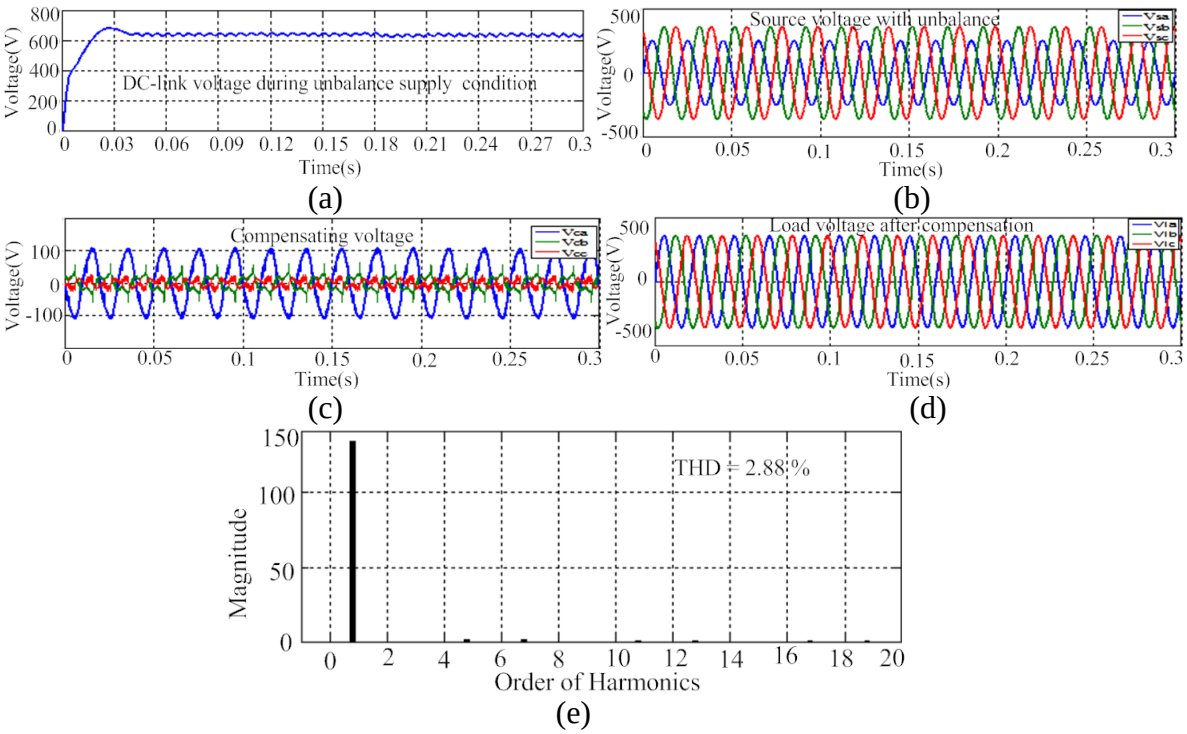


Fig.3.18 Simulation results during unbalanced supply condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

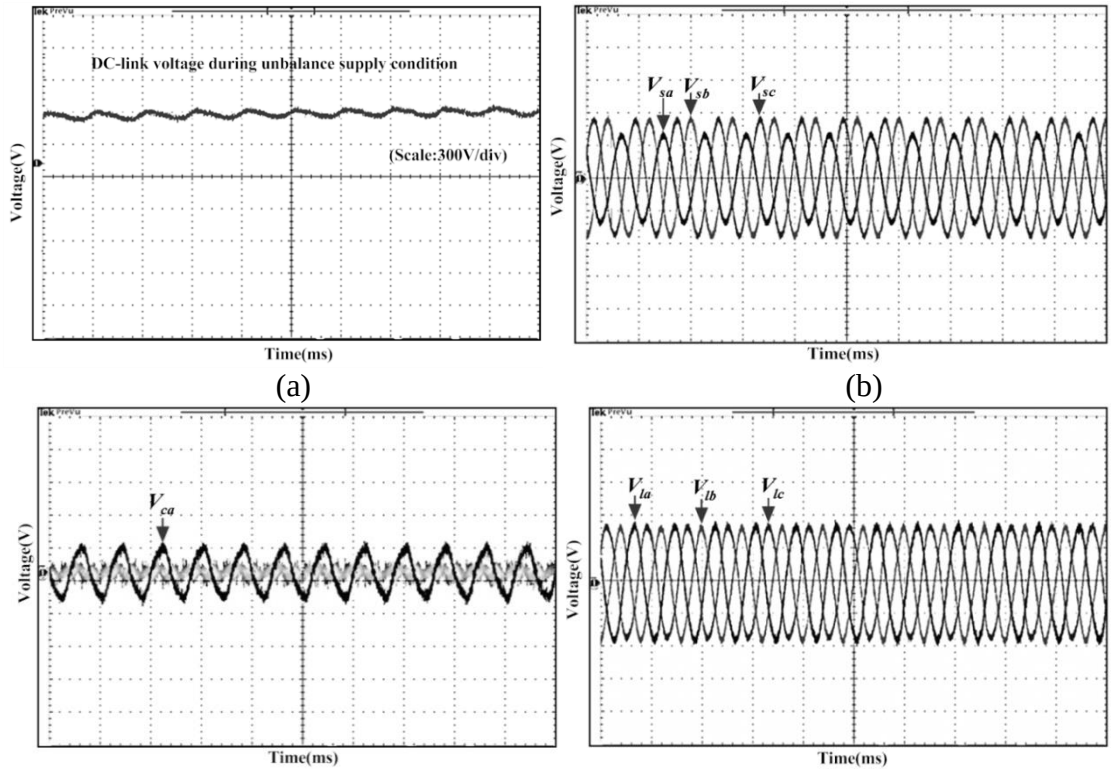


Fig.3.19 Real-time experimental results during unbalanced supply condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 80 V/div), (d) Load voltage after compensation (scale: 200 V/div).

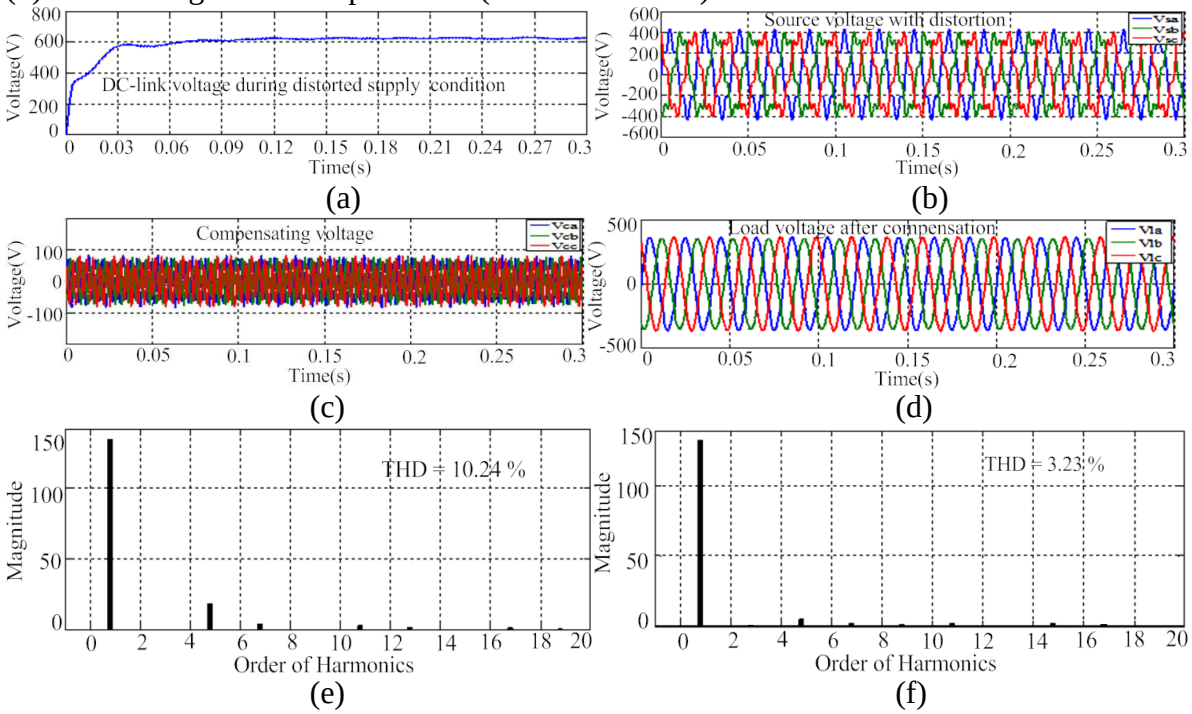


Fig.3.20 Simulation results during distorted supply condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Distorted supply voltage spectrum, (f) Load voltage spectrum after compensation.

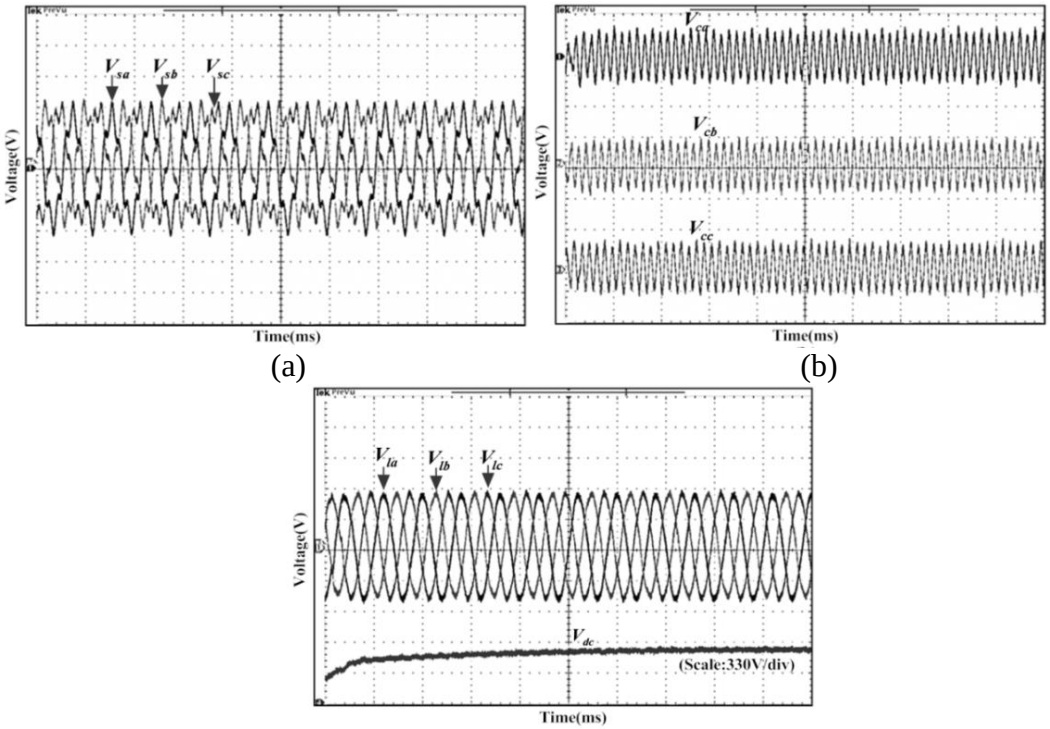


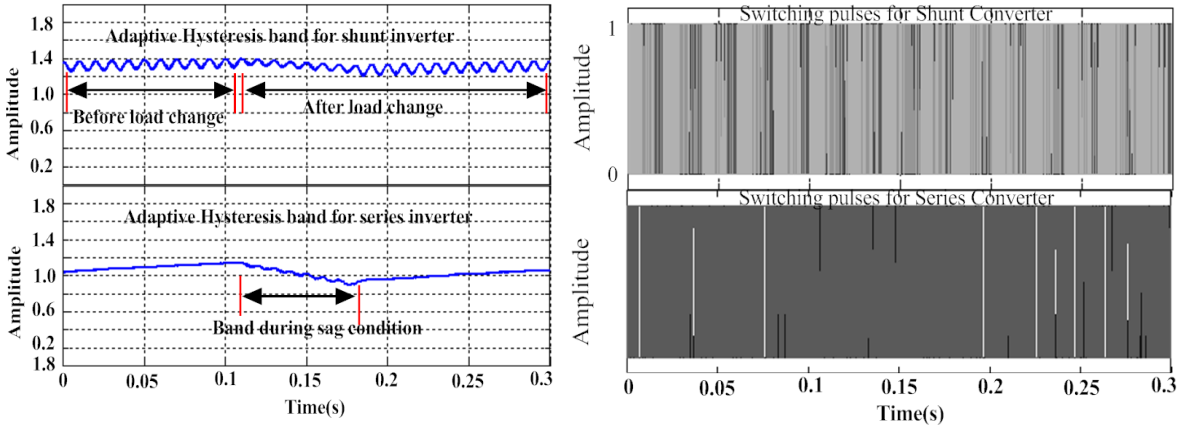
Fig.3.21 Real-time experimental results under distorted supply voltage condition, (a) Source voltage (scale: 200 V/div), (b) Compensation voltage (scale: 25 V/div), (c) Load voltage after compensation (scale: 200 V/div) and DC-link voltage (scale: 330 V/div).

Fig. 3.20 and 3.21 depict the simulation and experimental results during voltage distortion condition. Fig.3.20 (a) shows the simulation result of DC-link capacitor voltage during supply voltage distorted condition. Furthermore, Fig. 3.20 (b), (c) and (d) represent the simulation result of source voltage, compensating voltage and load voltage after compensation respectively. Fig.3.20 (e) and (f) illustrate the THD spectrum of load voltage before and after compensation and they are observed to be 10.24 % and 3.23 % respectively. Fig. 3.21 (b), (c) and (d) represent the experimental results of source voltage, compensating voltage, load voltage after compensation and dc-link voltage respectively.

3.5.2 Simulation and real-time HIL based OPAL-RT result of NLSMC based modified SRF theory

For simulation and experimental analysis, a step change of load at 0.15s is considered for transient performance. Also, 20 % of sag/swell creation between 0.12 s to 0.21 s for 5 cycles, source voltage distortion by adding 5^{th} and 7^{th} harmonics to the source voltage and voltage

unbalance formation by varying of phase *a* and phase *c* amplitudes up to ±30% and ±20% respectively from its nominal value are considered.



(a) (b)

Fig.3.22. Hysteresis band and switching patterns for shunt and series inverter, (a) Hysteresis band for shunt and series inverter, (b) Switching patterns for shunt and series inverter.

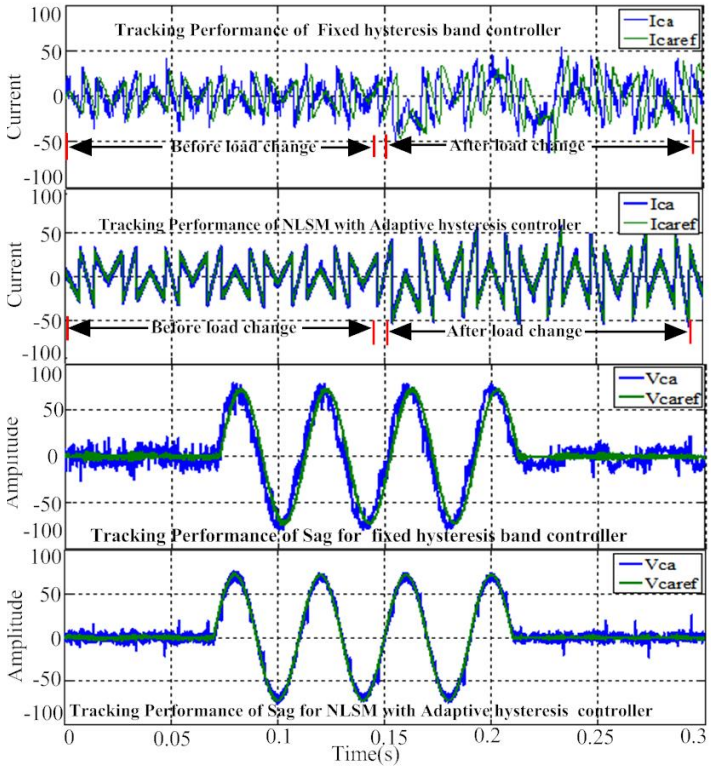


Fig.3.23. Tracking Performance of fixed hysteresis controller and NLSM with adaptive hysteresis controller.

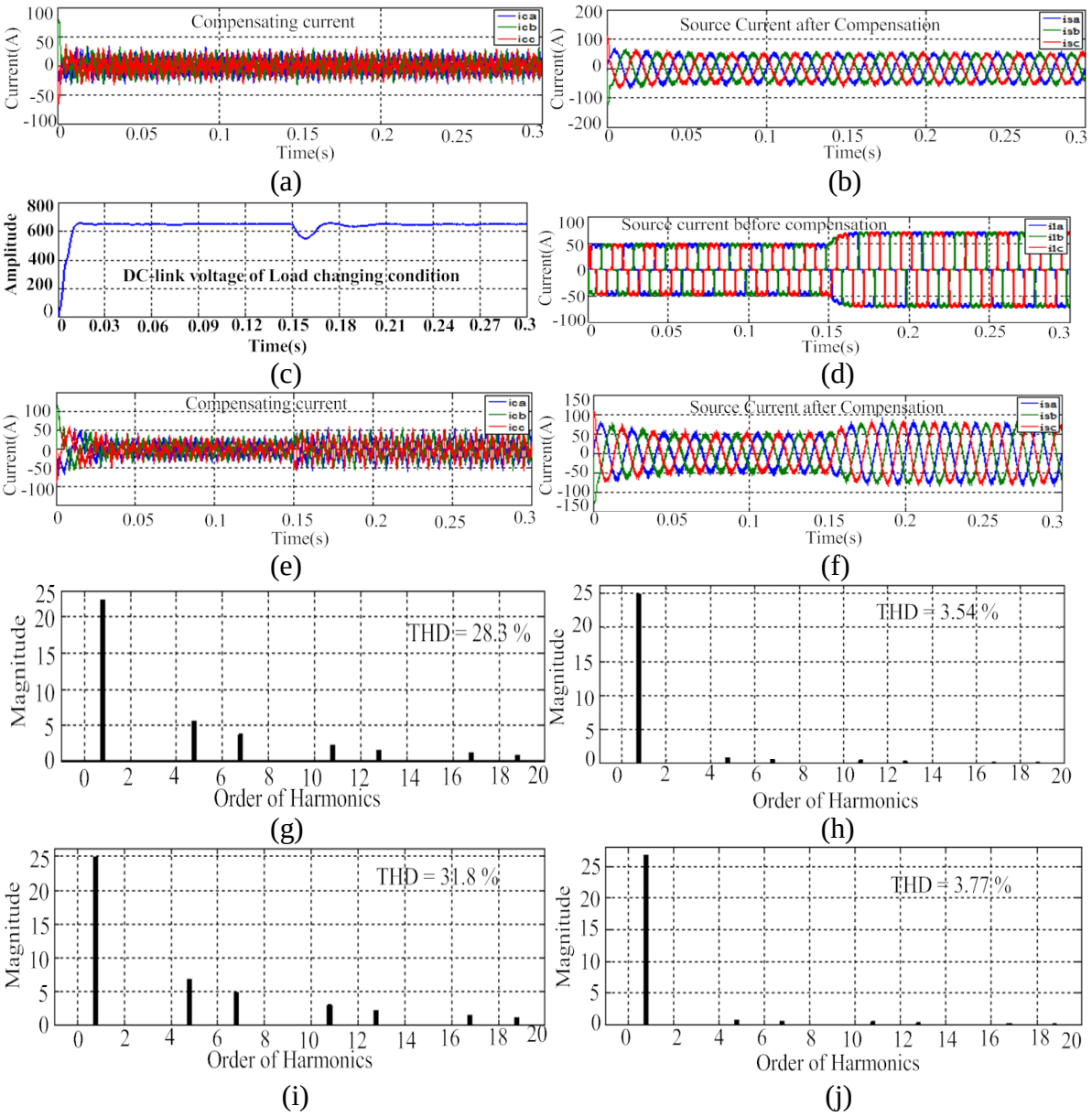


Fig.3.24 Simulation results, (a) Compensation current during steady-state condition, (b) Source current after compensation during steady-state condition, (c) DC-link voltage under transient condition, (d) Source current before compensation during transient-state condition, (e) Compensation current during transient-state condition, (f) Source current after compensation during transient-state condition, (g) Source current spectrum before compensation during steady-state condition, (h) Source current spectrum after compensation during steady-state condition (i) Source current spectrum before compensation during transient-state condition, (j) Source current spectrum after compensation during transient-state condition.

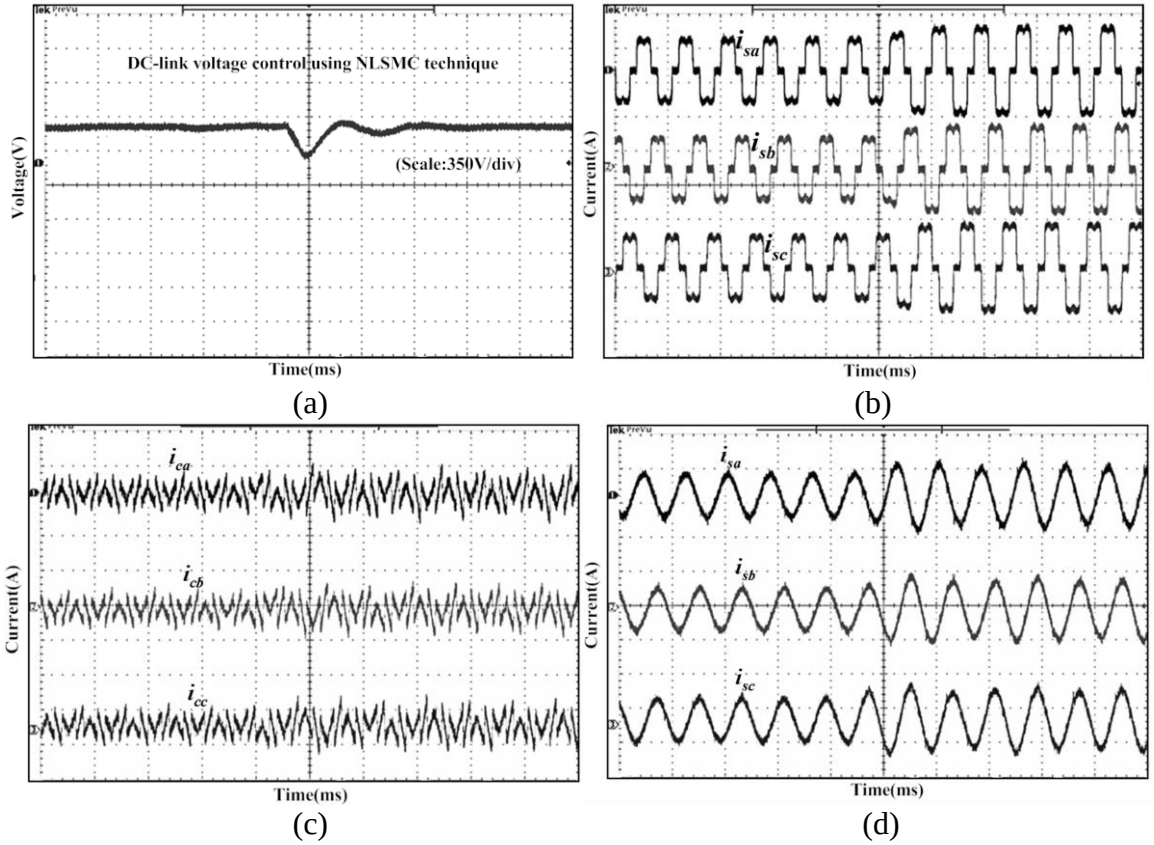


Fig.3.25 Real-time experimental results, (a) DC-link voltage under transient condition, (b) Source current before compensation (scale: 52 A/div), (c) Compensation current (scale: 40 A/div), (d) Source current after compensation (scale: 55 A/div).

Fig.3.22 (a) and (b) show the switching bands and switching patterns of both shunt and series APF of UPQC. For shunt APF the band violation is negligible during load changing conditions, thus tracking performance of compensating current is improved with greater reduction of ripples in the source current. In case of series APF, band violation is less during sag condition and band voltage is almost linear. Thus, it improves the tracking performance of compensating voltage, which in turn leads to better compensation capability to load voltage. The compensating current and voltage tracking performances during sag condition of fixed hysteresis controller and proposed NLSMC with adaptive hysteresis controller are sequentially presented in Fig.3.23. From the figure, it is clear that the proposed control strategy exhibits better tracking performance irrespective of disturbance occurring in load side or source side.

The performance of shunt APF with proposed controller using simulation study and real-time experimental study are shown in Fig.3.24 and 3.25 with load transient conditions. Fig.3.24 (a) and (b) provide the information about compensating current and source current under steady-state condition. Fig.3.24 (c) and 3.25 (a) show the performance of NLSMC method for controlling the dc-link voltage during transient state condition of load. Fig.3.24 (d), (e) and (f) as well as Fig.3.25 (b), (c) and (d) provide the information regarding simulation and experimental results of source current before compensation, compensating current and source current after compensation respectively. It is observed from the figure that, the proposed NLSMC with modified SRF control strategy can provide better compensation as compared to NVGF with modified SRF controller.

Thus, the source current in NLSMC is more sinusoidal in nature in comparison to the NLVGF controller. Fig. 3.24 (e) and (f) show the information regarding the THD of source current before and after compensation during steady-state condition. Fig. 3.24 (g) and (h) show the information about the THD of source current before and after compensation during transient-state condition. Table 3.1 lists the THD of source current before and after compensation employing NVGF control method and NLSMC method. It is indicated from the Table that THD of the source current before compensation during steady-state and transient-state conditions are found to be 28.3 % and 31.8 % respectively. However, THD of source current after compensation during steady-state and transient-state conditions are found to be 3.83 % and 4.17 % respectively in NVGF controller. whereas, in case of NLSMC method the source current after compensation during steady-state and transient-state are found to be 3.54 % and 3.87 % respectively.

Fig.3.26 and 3.27 depict the simulation and experimental results of series APF with NLSMC method during voltage distortion condition. Fig.3.26 (a) and 3.27 (a) show the simulation and experimental results of DC-link capacitor voltage during supply voltage distorted condition. Moreover, Fig 3.26 (b), (c) and (d) represent the simulation results of source voltage during distorted condition, compensating voltage and load voltage after compensation respectively. Similarly, Fig. 3.27 (b), (c) and (d) represent the experimental result of source voltage during distorted condition, compensating voltage and load voltage after compensation respectively. Fig.3.26 (e) and (f) illustrate the THD spectrum of load voltage before and after compensation and they are found to be 10.24 % and 3.04 %

respectively. Table 3.1 gives the THD analysis of both NVGF controller and NLSMC method. From the tabulation it is clear that the proposed NLSMC strategy can satisfactorily eliminate all the distortion in the source voltage by injecting proper compensation voltage and makes the load voltage free from all such disturbances which confirms the superiority of the proposed NLSMC strategy over NVGF control strategy.

Fig. 3.28 and 3.29 show simulation and real-time experimental result of the sag voltage compensation performance. Fig. 3.28 (a) and 3.29 (a) show the DC-link voltage of proposed NLSMC method during supply voltage sag condition. Fig.3.28 (b), (c) and (d) as well as 3.15 (b), (c) and (d) show the waveform of supply voltage sag of 5 cycles with a depth of 20 %, compensating voltage and load voltage after compensation respectively. It is observed from the figure that, the series APF is utilized to compensate the load voltage around its nominal value by proper injection of compensating voltage through series transformer. Fig. 3.28 (e) displays THD spectrum of load voltage after compensation and it is found to be 2.32 %. Table 3.2 gives the THD comparison of load voltage using both the control technique.

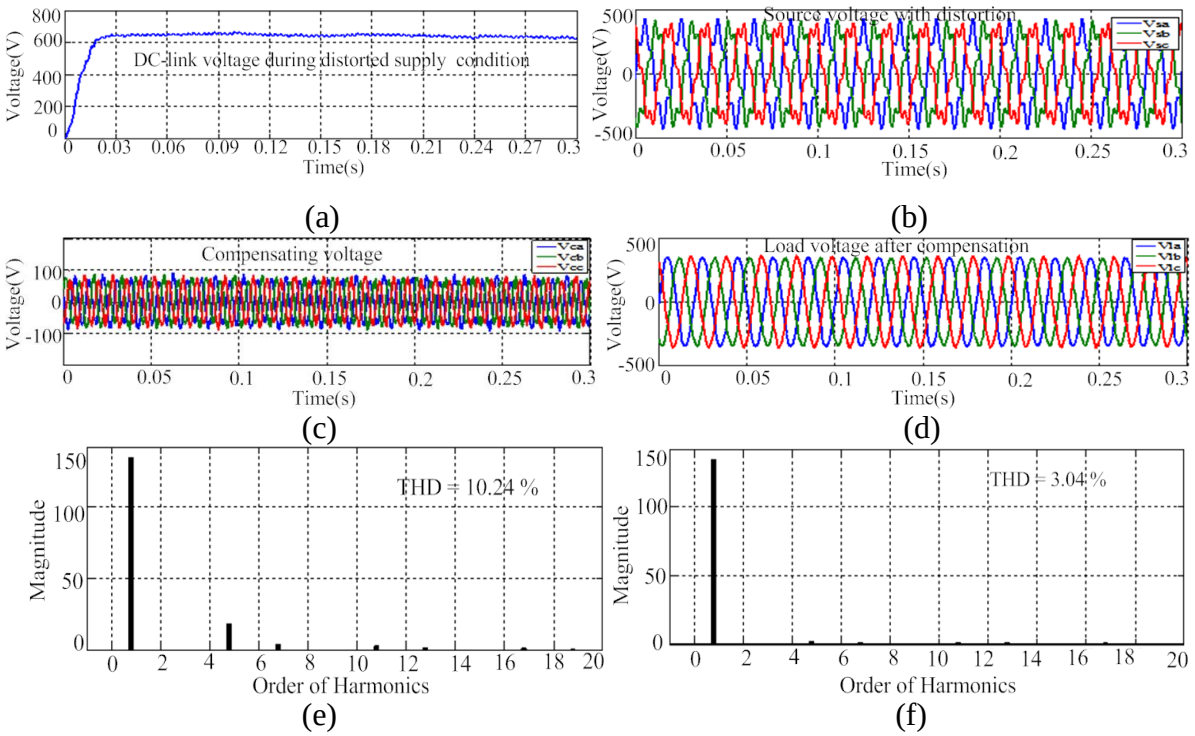


Fig.3.26 Simulation results during distorted supply condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Distorted supply voltage spectrum, (f) Load voltage spectrum after compensation.

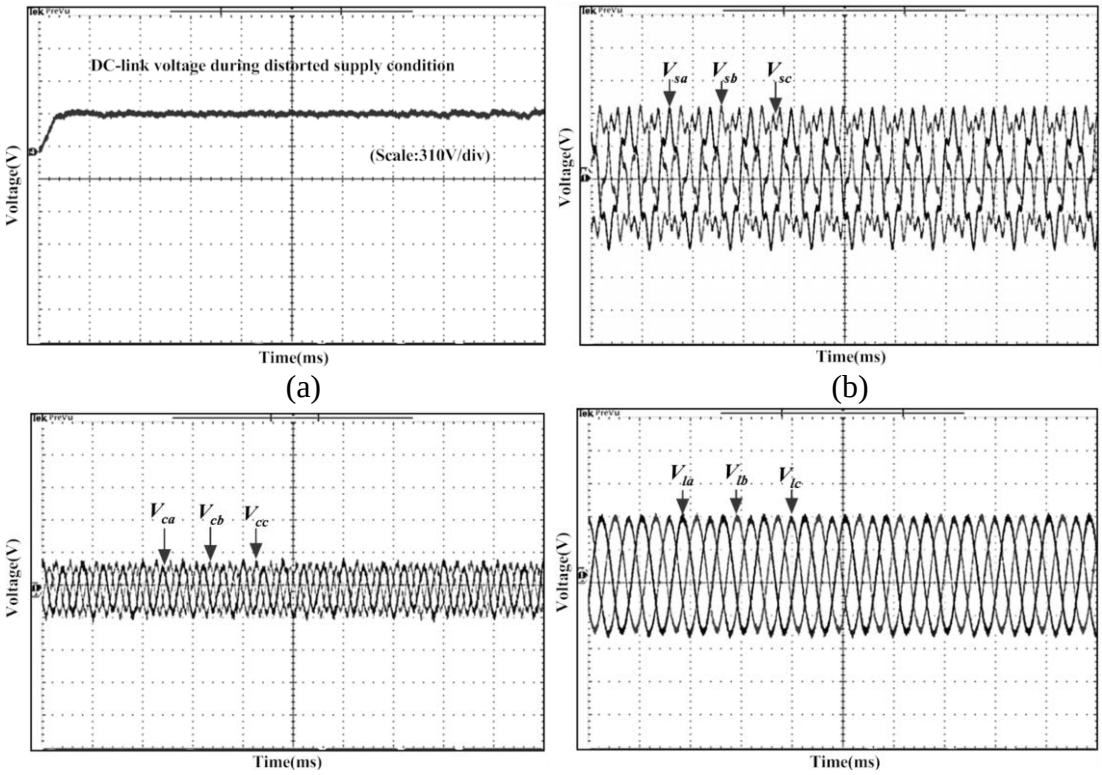


Fig.3.27 Real-time experimental results under distorted supply voltage condition, (a) DC-link voltage, (a) Source voltage (scale: 200 V/div), (b) Compensation voltage (scale: 25 V/div), (c) Load voltage after compensation (scale: 200 V/div).

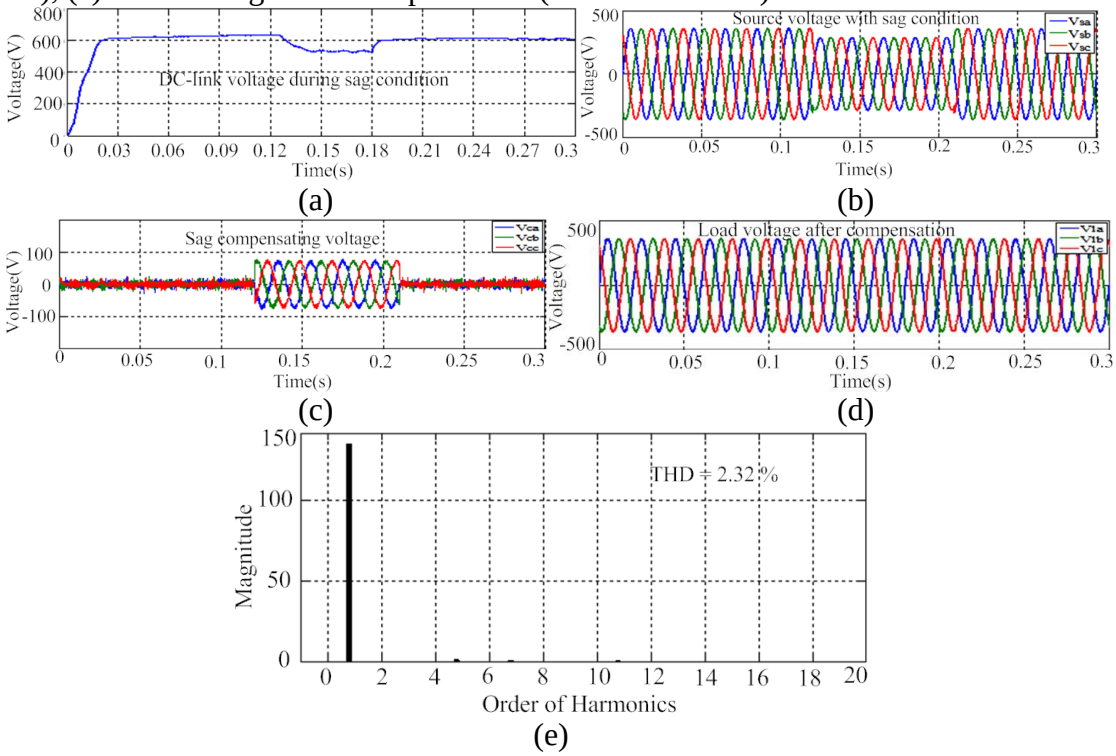


Fig.3.28 Simulation results during sag condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage, (e) Load voltage spectrum after compensation.

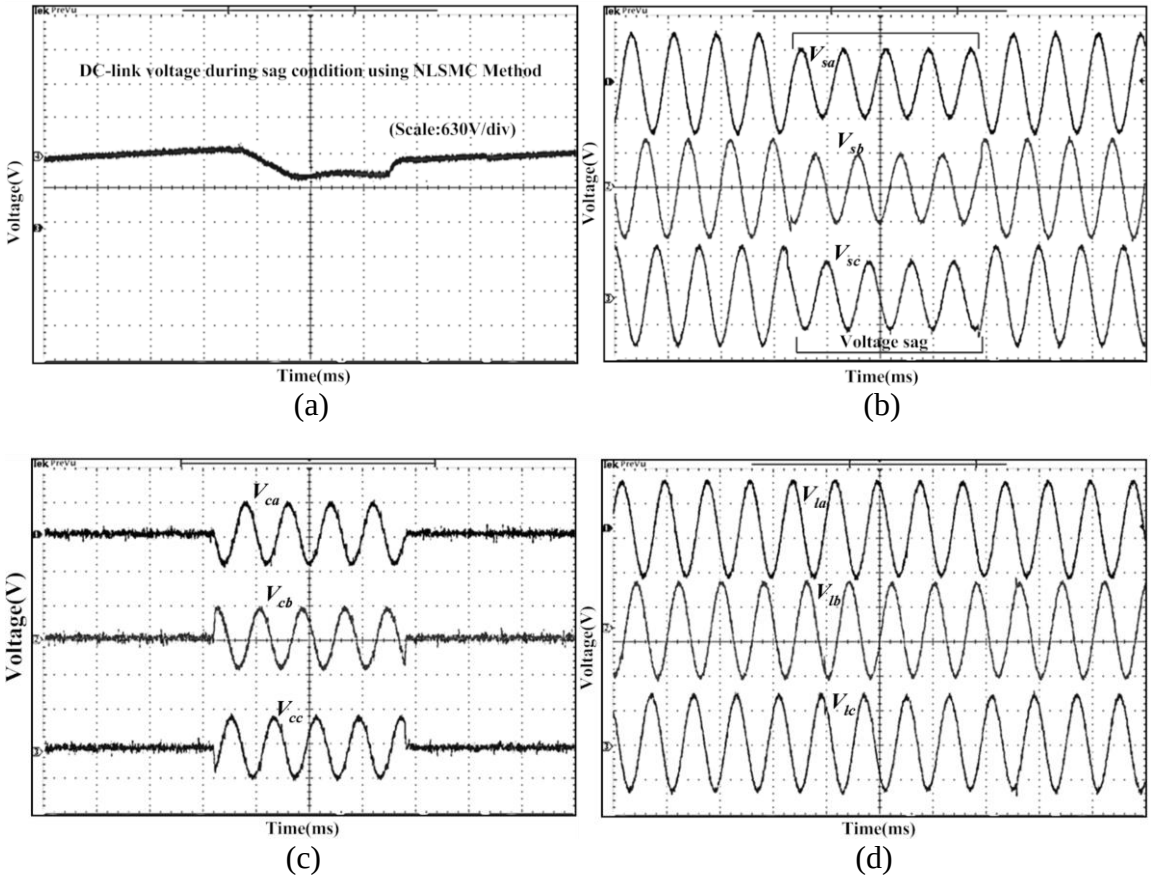


Fig.3.29 Real-time experimental results during sag condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 65 V/div), (d) Load voltage (scale: 200 V/div).

Fig.3.30 and 3.31 demonstrate the simulation as well as real-time experimental results of swell conditions using NLSMC method. Fig. 3.30 (a) and 3.31 (a) show the dc-link capacitor voltage of proposed controller during the voltage-swell condition. Fig.3.30 (b) and 3.31 (b) show the waveform of voltage swell of 20 % obtained for 5 cycles and its corresponding compensating voltage and load voltage are shown in Fig.3.30 (c) and (d) as well as Fig.3.31 (c) and (d) respectively. It is observed from the figure that the proposed control strategy can compensate the voltage swell existing in the supply voltage and regulate the load voltage to its nominal value. Fig. 3.30 (e) shows the information regarding THD spectrum of load voltage after compensation and its THD is found to be 2.27 %.

Table 3.2 provides the THD information of load voltage during supply voltage swell condition using both the control methods. It is observed from the table that proposed NLSMC

technique can enhance the compensation capability by reducing amount of ripple in the load voltage. Fig.3.32 and 3.33 show the simulation and experimental results of compensation performance of series APF of UPQC for compensating unbalance source voltage. Fig. 3.32 (a) and 3.33 (a) provide information about simulation as well as experimental results of dc-link capacitor voltage during unbalanced supply voltage condition. Fig. 3.32 (b), (c) and (d) as well as Fig. 3.33 (b), (c) and (d) show the unbalanced supply voltage, compensating voltage and load voltage after compensation using proposed NLSMC method respectively. Fig. 3.32 (e) shows the THD spectrum of load voltage after compensation and it is about 2.71 %.

Table 3.2 provides the THD information of load voltage during supply voltage unbalance condition using both the control technique. It is clear from the table that, the proposed control strategy can satisfactorily compensate the unbalance present in the source voltage by injecting proper compensation voltage and makes the load voltage free from all such disturbances, which confirms the superiority of the proposed NLSMC strategy over NVGF controller.

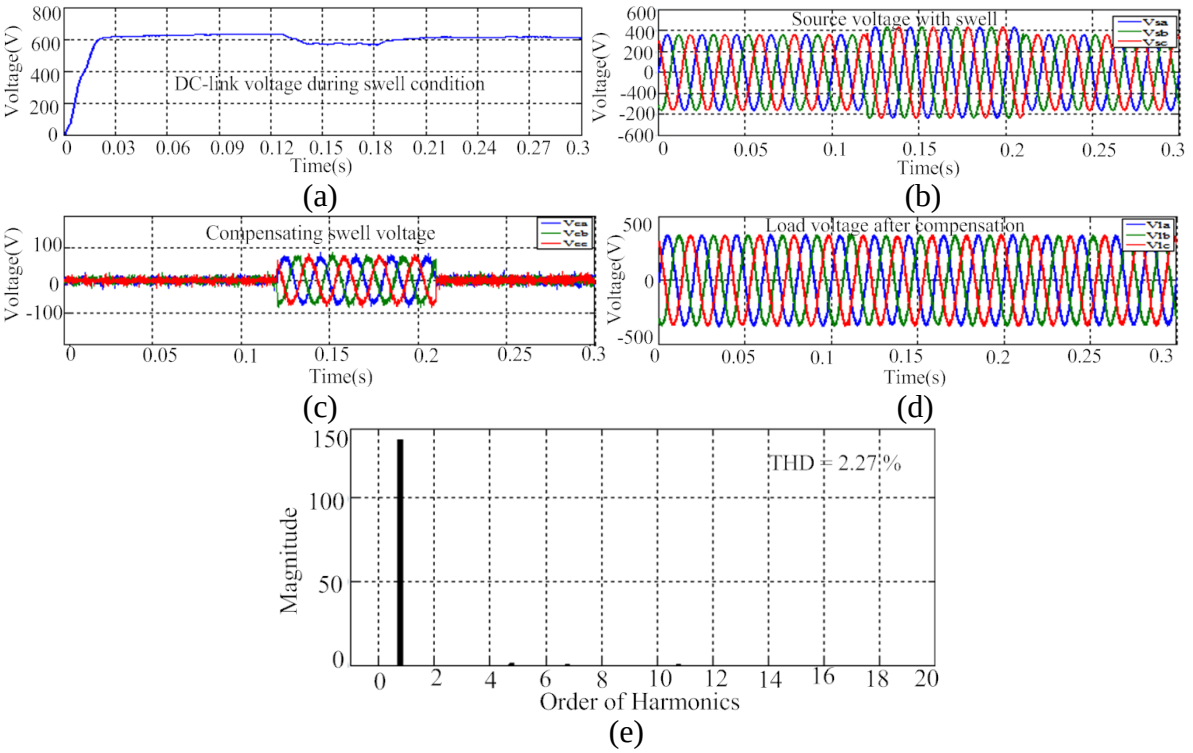


Fig.3.30 Simulation results of swell condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

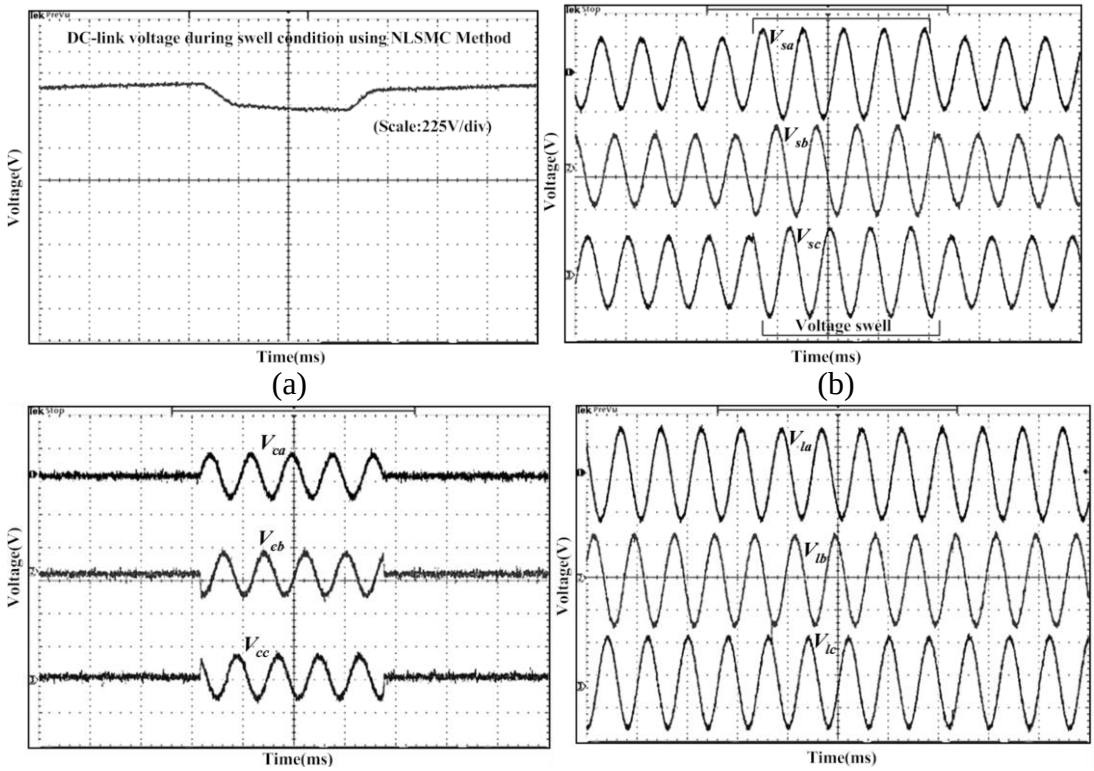


Fig.3.31 Real-time experimental results during swell condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 73 V/div), (d) Load voltage (scale: 200 V/div).

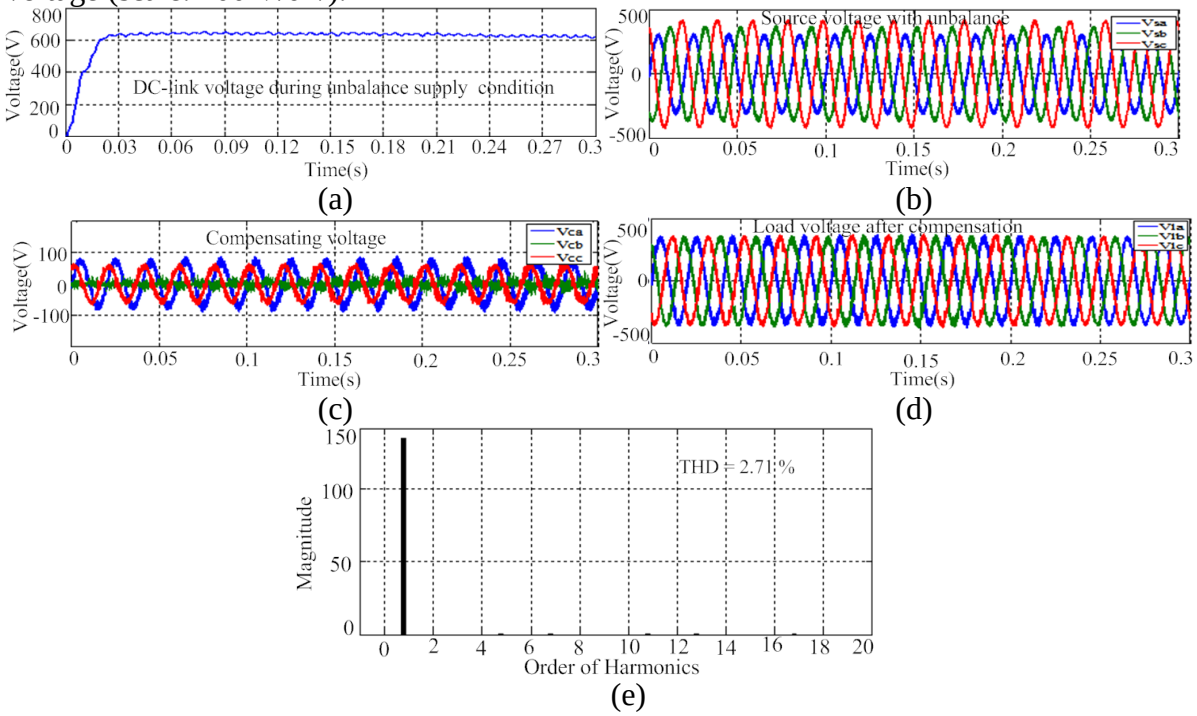


Fig.3.32 Simulation results during unbalanced supply condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

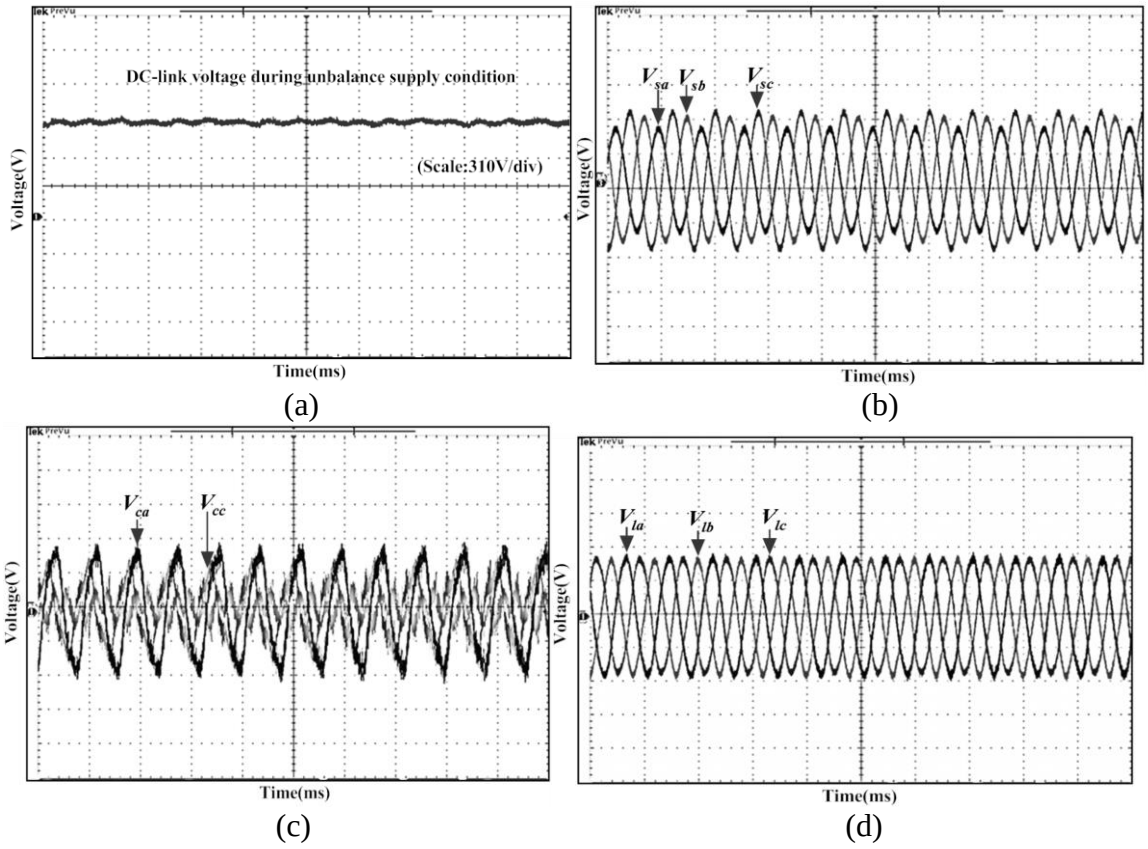


Fig.3.33 Real-time experimental results during unbalanced supply condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 80 V/div), (d) Load voltage after compensation (scale: 200 V/div).

Table 3.1. Comparison of source current THD and load voltage THD

Type of condition	Before Compensation	Compensation with UPQC	
		NVGF with modified SRF controller	NLSMC with modified SRF controller
Source current THD during Steady-state condition	28.3 %	3.83 %	3.54 %
Source current THD during Transient-state condition	31.8 %	3.97 %	3.77 %
Load voltage THD during distorted supply condition	10.24 %	3.23 %	3.04 %

Table 3.2. Comparison of load voltage THD during dynamic condition of supply voltage

Type of condition	Compensation with UPQC	
	NVGF with modified SRF controller	NLSMC with modified SRF controller
Load voltage THD after compensation during supply voltage sag condition	2.55 %	2.32 %
Load voltage THD after compensation during supply voltage swell condition	2.43 %	2.27 %
Load voltage THD after compensation during supply voltage unbalance condition	2.88 %	2.71 %

3.6 Chapter Summary

This chapter starts with a discussion of structural design and operating principle of UPQC as well as two novel control strategies such as NVGF based modified SRF control technique and NLSMC with modified SRF technique. The average DC-link voltage regulation technique is the most interesting nonlinear control philosophy, which realises two control activities simultaneously to control the voltage across the DC-link capacitor and defines the amplitude of the source current.

Moreover, the reference generation strategy based upon proposed SRF is fairly simple and easy to implement. The MPLL design involved in this strategy is having an additional negative feedback applied in the inner loop of the conventional PLL, as a result, it is more immune to noise, distortion and harmonics indicating a perfect extraction of positive sequence signal during supply voltage distortion and unbalance condition. Also, this design can eliminate the transformation angle oscillation during conversion process, resulting in a fast and accurate extraction of the reference signal through all operating conditions of power system. Therefore, the complete control strategy is independent of all disturbances and oscillations present during the fault occurred in source as well as load sides and makes the UPQC robust against all operating conditions.

Among various modulation methods the hysteresis control seems to be the most suitable PWM controller for the shunt and series compensator. The hysteresis control technique has simpler implementation, improved system stability and increased reliability as well as

response speed. However, it is suffered from inherent switching losses and band violation during load as well as source side perturbations.

Therefore, this Chapter considers the switching dynamics control strategy for calculation of hysteresis band. Consequently, this control strategy can overcome drawbacks of band violation and switching losses occurring in the fixed hysteresis band, in presence of load as well as source perturbations. Therefore, the tracking performance of UPQC is improved, which drastically reduces the switching ripples present in the load voltage and source current. With the aforementioned views, it can be concluded that the proposed control strategy can enhance the performance of UPQC in all operating conditions by eliminating PQ problems such as current harmonics, voltage distortion, sag, swell and voltage unbalance. Furthermore, to study the effectiveness of this proposed NLSMC technique over NVGF controller technique, a comparative assessment has been performed using both load as well as supply side dynamic conditions. From the simulation and real-time simulation results, it is observed that the proposed NLSMC technique outperforms NVGF controller.

Chapter 4

Optimization Based Reference Extraction Methods with Novel PWM Techniques for UPQC

4.1 Introduction

Chapter 3 has presented nonlinear control techniques such as NVGF control method and NLSMC method for DC-link voltage regulation and modified SRF technique for reference generation. However, existence of large settling time in dc voltage leads to poor dynamic performance of NVGF control technique and hence current harmonics, voltage distortions and voltage disturbance such as voltage sag/swell as well as voltage unbalance compensation capability of this technique is not quite effective in comparison to the NLSMC technique. Moreover, NLSMC is very sensitive to model mismatch and noise. It is quite sluggish in rejecting long drifting grid disturbances. Hence, a better control strategy has to be developed in UPQC, which has improved DC-link voltage regulation as well as tracking performance during load and grid side disturbances.

To overcome the aforementioned issues, this chapter proposes a resistive optimization technique (ROT) incorporated with enhanced phase-locked loop (EPLL) based NVGF hysteresis control strategy and an optimum active power (OAP) technique combined with enhanced phase-locked loop (EPLL) based fuzzy sliding mode (FSM) pulse-width modulation (PWM) control strategy for unified power quality conditioner (UPQC). These proposed techniques can mitigate several power quality (PQ) problems existing in a three-phase three-wire power distribution network.

The novel resistive optimization control strategy is used for reference signal generation for both shunt and series APF. This proposed algorithm adaptively regulates the DC-link capacitor voltage without utilizing additional controller and makes the control system simple as it does not involve any complex optimization methods. Furthermore, a nonlinear variable gain fuzzy based hysteresis controller is proposed for controlling the hysteresis band, which effectively reduces the band violation and improves the tracking behavior of UPQC during load transient and supply side transient conditions of power system.

Similarly, the OAP control technique is utilized for extraction of the reference signal for both shunt and series APF and also regulates the dc-link capacitor voltage adaptively. Moreover, fuzzy sliding mode (FSM) controller is designed in the inner current and voltage control loops to generate PWM signals for switching both shunt and series APF. FSM provides fixed switching frequency by eliminating high frequency chattering caused by the sliding mode control and improves the character of reaching segment by forcing the tracking error to zero.

4.2 Resistive optimization with nonlinear variable gain fuzzy (RO-NVGF) based hysteresis controller

A low-pass filter (LPF) is used in DC-link control loop for filtering the ripples present in the dc-link voltage, which introduces a finite delay resulting in large settling time of dc-link voltage. Additionally, utilization of fixed dc-link voltage control techniques can generate switching losses and conduction losses with the variation of load as well as supply voltage [103]. Therefore, dc-link voltage has to be changed adaptively with load and supply side perturbations, which can result in better compensation performance and operational flexibility as compared to the NVGF and NLSMC techniques described in chapter-3. With the above-mentioned views, the proposed control technique utilizes enhanced phase-locked-loop (EPLL) technique for perfect extraction of positive sequence signal during power system perturbation and computes optimum value of resistance for generation of the reference signal with self-supporting dc-link voltage. The proposed control technique provides fast detection of transient conditions occurred in the supply or load sides, and accordingly dc-link voltage is regulated by changing the amplitude of the real fundamental component of the reference current. Therefore, a small amount of real power is flowing through the shunt inverter into the dc-link capacitor for compensating conduction and switching losses and keeps the dc-link voltage constant.

On the other hand, to accomplish significant compensation with good accuracy and very fast response, hysteresis controllers [56] are well known for PWM signal generation. However, the conventional hysteresis technique exhibits an undesirable feature such as variable switching frequency. As a result, the switching losses are increased and the source current as well as the load voltage contains some additional ripples. Several papers reported in the literature deal with these issues and try to eliminate such drawbacks by many effective

solutions [104,105], which are based on controlling the hysteresis bandwidth. The adaptive hysteresis band controller discussed in Chapter-3 provides excellent performance by reducing the switching losses, but fails to provide satisfactory performance during dynamic as well as uncertainty condition of load and supply voltage variation. To overcome this drawback, a NVGF [106,107] based hysteresis controller is considered for PWM signal generation in both shunt and series inverter of UPQC. This hysteresis controller provides a better hysteresis band computation approach during power system dynamic and transient condition.

Under these circumstances mamdani fuzzy logic controller is unable to provide a wide variation of control gain for controlling the hysteresis band during a load transient, sag/swell, voltage unbalance and distorted source voltage condition. This results in band violation and tracking performance degradation. This problem can be eliminated by NVGF hysteresis controller based on Takagi-Sugeno (TS) fuzzy rule scheme, where an extensive variation of the controller gain improves the tracking performance to a large extent. The performance of the proposed approach is validated through MATLAB/SIMULINK followed by the real-time experimental studies, which are accomplished by using hardware-in-the-loop (HIL) system OPAL-RT simulator (OP5600) with Xilinx SPARTAN-3(3xc3s5000) OP5142 field programmable gate array (FPGA) processor for user interconnection.

4.3. Proposed Resistive Optimization Technique

Distorted, unbalanced and faulty supply conditions create numerous problems in power system. In such situations, extraction of reference signal is one of the challenging tasks, as compensation capability of UPQC depends on how accurately and how quickly the reference signals are extracted from power system. To overcome such issues, a novel control structure is proposed to calculate the optimal value of resistance for generating the reference signal and regulating the dc-link voltage to eradicate the PQ problems present in power system. Additionally, the quality of grid synchronization is a significant factor which determines the complete control structure compensation capability of PQ problems; therefore an Enhanced phase locked loop (EPLL) is employed for accurate and rapid extraction of positive sequence signal from polluted grid voltage.

4.3.1 Enhanced PLL (EPLL)

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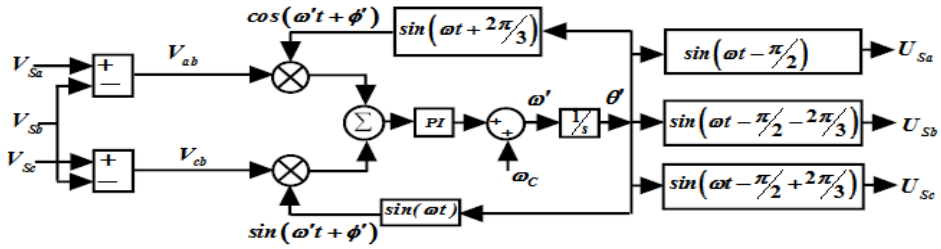

Fig.4.1. Enhanced PLL structure

$$C(s)=\frac{t}{(s+e)} \tag{4.1}$$

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4.3.2 Resistive optimization technique for calculation of reference signal

Chapter 3 has presented nonlinear control techniques such as NVGF control method and NLSMC method for DC-link voltage regulation and modified SRF technique for reference generation. However, existence of large settling time in dc voltage leads to poor dynamic performance of NVGF control technique and hence current harmonics, voltage distortions and voltage disturbance such as voltage sag/swell as well as voltage unbalance compensation capability of this technique is not quite effective in comparison to the NLSMC technique. Moreover, NLSMC is very sensitive to model mismatch and noise. It is quite sluggish in rejecting long drifting grid disturbances. Hence, a better control strategy has to be developed in UPQC, which has improved DC-link voltage regulation as well as tracking performance during load and grid side disturbances.

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4.3.3. Design of Nonlinear Variable Gain Fuzzy controller for hysteresis band calculation

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4.4 Optimum active power with fuzzy sliding mode controller (OAP-FSMC) based PWM control technique

The ROT-techniques proposed in the sub-section (4.3.2) have considered more than half cycle to estimate change in amplitude of load current and supply voltage at the beginning. Hence, the compensation performance of the UPQC decreases significantly, which leads to increased oscillations in DC-link voltage. Therefore, switching losses and conduction losses are increased with the variation of load as well as supply voltage.

To overcome the aforementioned issue, in this section, we propose another control technique that computes optimum active power (OAP) to generate reference signal with a self-supporting dc-link voltage regulation. In this approach, when any transient condition occurs in the supply or load side, dc-link voltage is regulated accordingly by altering the amplitude of the real fundamental component of the reference current. As a result, a small amount of real power is flowing through the shunt inverter into the dc-link capacitor for compensating conduction and switching losses and hence keeps the dc-link voltage constant. Furthermore, enhanced phase-locked-loop (EPLL) method, which is described in the sub-section 4.3.1, extracts the fundamental positive-sequence signal during power system perturbations.

On the other hand, PWM technique such as NVGF-hysteresis controller is not effective in tracking the reference signal during load and supply side perturbations, which results in degradation of PQ compensation capability of UPQC. Hence, sliding mode controller (SMC) is extensively preferred for its compatibility with the inherent switching nature of power converters [110, 111]. Moreover, the SMC is popular for its stability, robustness, good regulation and frequent switching action under all operating conditions of load and supply voltage perturbations.

Regardless of excellent performance, SMC suffers from chattering problem, which leads to generate a variable switching frequency causing switching and power losses, as well as electromagnetic compatibility (EMC) noise in the VSI. To avoid these drawbacks, a fuzzy logic controller is considered in conjunction with SMC to generate a fixed switching methodology. This fuzzy SMC (FSMC) [112, 113] is one of the promising solutions to handle power system uncertainties as well as nonlinearity situations. Power system uncertainty arises due to random variation of system loads, irregular fluctuations of system parameter such as capacity of distribution line and sudden failure of system component of

the power line. To operate UPQC in the above uncertainty conditions, a fuzzy SMC based PWM (FSMPWM) technique is proposed for accurately tracking the reference signal, which provides better compensation capability of PQ problems. The performance of the proposed approach is validated using MATLAB/SIMULINK followed by real-time experimental studies, which are accomplished by using hardware-in-the-loop (HIL) system OPAL-RT simulator (OP5600) with Xilinx SPARTAN-3(3xc3s5000) OP5142 field programmable gate array (FPGA) processor for user interconnection. To study the efficacy of the proposed control strategy, a comparative assessment has been performed with the proposed ROT-NVGF hysteresis controller.

4.5 Reference signal extraction technique

The OAP based reference generation technique is determined with extraction of optimum active power from the power line. Therefore, a novel control structure is formulated to calculate the OAP for generating the reference signal in UPQC under consideration of power system perturbations. In addition to this, the quality of grid synchronization is a significant factor in determining reference signals hence an enhanced phase-locked loop (EPLL) is employed for accurate and rapid extraction of positive sequence signal from grid voltage.

4.5.1 Optimized Active Power (OAP) Technique

The proposed control strategy shown in Fig.4.5 is employed to create a reference compensating signal for UPQC and also to generate PWM signal. At first OAP technique is considered for reference signal generation by assuming the following three-phase desired source voltages and source currents given in Eq. (4.26) and Eq. (4.27) respectively.

$$\begin{aligned} V_{sa} &= V_m \sin(\omega_1 t + \varphi) \\ V_{sb} &= V_m \sin(\omega_1 t - 120^\circ + \varphi) \\ V_{sc} &= V_m \sin(\omega_1 t + 120^\circ + \varphi) \end{aligned} \tag{4.2}$$

$$\begin{aligned} i_{sa} &= I_m \sin(\omega_1 t + \varphi) \\ i_{sb} &= I_m \sin(\omega_1 t - 120^\circ + \varphi) \\ i_{sc} &= I_m \sin(\omega_1 t + 120^\circ + \varphi) \end{aligned} \tag{4.3}$$

where V_m, I_m are the magnitude of supply voltage and current respectively and φ is the phase angle between the supply voltage and current.

The output of low-pass filter (LPF) is the optimized active power that can be represented as

$$\bar{p}_s = \frac{1}{T}\int_0^T \sum_{x\in k} V_{sx} I_{sx} dt = \frac{3V_m I_m}{2} \tag{4.4}$$

Based on the necessity of supply voltage, the source voltage block provides the peak amplitude of supply voltage $\left(V_{sp}\right)$. Similarly, the peak amplitude of source current $\left(I_{sp}\right)$ can be determined as

$$I_{sp} = \left(i_{sa}^2 + i_{sb}^2 + i_{sc}^2\right)^{1/2} \tag{4.5}$$

Depending on these peak amplitudes of source current and supply voltage, the optimum values of current $\left(I_m\right)$ and voltage $\left(V_m\right)$ are calculated from OAP.

$$I_m = \frac{2\bar{p}_s}{3\,V_{sp}} \tag{4.6}$$

and

$$V_m = \frac{2\bar{p}_s}{3I_{sp}} \tag{4.7}$$

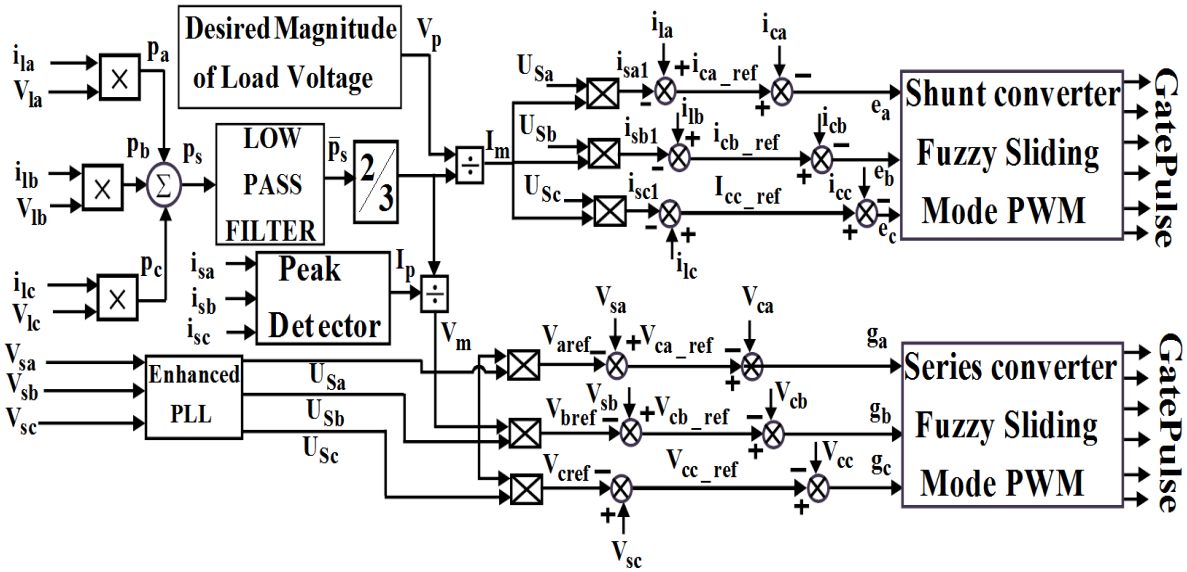


Fig.4.2. Proposed OAP with EPLL based FSM-PWM control structure of UPQC

These optimum values of current and voltage are multiplied with unit sine vector produced from the IPLL block to generate the reference source current and reference load voltage as given below.

$$\begin{aligned} I_{sa1} &= I_{\mathrm{m}} * \sin(\omega_1 t + \varphi) \\ I_{sb1} &= I_{\mathrm{m}} * \sin(\omega_1 t - 120^{\circ} + \varphi) \\ I_{sc1} &= I_{\mathrm{m}} * \sin(\omega_1 t + 120^{\circ} + \varphi) \end{aligned} \tag{4.8}$$

$$\begin{aligned} V_{aref} &= V_{\mathrm{m}} * \sin(\omega_1 t + \varphi) \\ V_{bref} &= V_{\mathrm{m}} * \sin(\omega_1 t - 120^{\circ} + \varphi) \\ V_{cref} &= V_{\mathrm{m}} * \sin(\omega_1 t + 120^{\circ} + \varphi) \end{aligned} \tag{4.9}$$

The reference source currents are subtracted from the load current $(i_{la}, i_{lb}$ and $i_{lc})$ for the generation of compensating reference currents $(i_{caref}, i_{cbref}$ and $i_{ccref})$. Similarly, compensating reference voltages $(V_{faref}, V_{fbref}$ and $V_{fcref})$ are calculated by subtracting the reference voltage $(V_{aref}, V_{bref}$ and $V_{cref})$ from supply voltage $(V_{sa}, V_{sb}$ and $V_{sc})$. These references as well as actual compensating currents and voltages are applied to the FSM controller for producing PWM signal for shunt and series converter, the details of which are described in the next section.

4.5.2 Fuzzy sliding mode for shunt APF

To apply the FSMC theory to the shunt APF, sliding surfaces are designed first and then equivalent control laws are formulated accordingly. After that PWM signals are generated by utilizing mamdani based fuzzy system at the sliding surface. For designing of sliding surface, the equivalent circuit for one leg of shunt converter is considered which is illustrated in Fig.2.9 of chapter-2. The expression for inductor current given in Eq. (2.13) is rewritten as

$$\frac{di_c}{dt} = \frac{V_S}{L_{shf}} - u\frac{V_{dc}}{2L_{shf}} - \frac{R_{shf}}{L_{shf}} i_c \tag{4.10}$$

The fuzzy sliding surface trajectory is achieved by deducting the measured compensating current (i_{cabc}) from the reference compensating current (i_{cabc_ref}). The sliding surface for shunt converter is given by

$$s(t) = e_x(t) \tag{4.11}$$

where *x* denotes a particular phase and the expression of Eq.(4.15) becomes

$$e_x(t) = [i_{cx\_ref} - i_{cx}] = 0 \tag{4.12}$$

For the shunt converter, the expression for $\dot{s}(t)$ can be written as

$$\dot{s}(t) = \dot{e}_x(t) \tag{4.13}$$

Thus, $\dot{e}_x(t) = \left(\dot{i}_{cx\_ref} - \dot{i}_{cx}\right)$

$$\begin{aligned} &= \left(\frac{di_{cx\_ref}}{dt} - \frac{di_{cx}}{dt}\right) \\ &= \left(\frac{di_{cx\_ref}}{dt} + \frac{R_{shf}}{L_{shf}} i_{cx} + u_x \frac{V_{dc}}{2L_{shf}} - \frac{V_{Sx}}{L_{shf}}\right) \end{aligned} \tag{4.14}$$

Setting the sliding surface $\dot{e}_x(t)$=0, the equivalent control law can be defined as

$$u_{eqx} = \left(\frac{V_{Sx}}{L_{shf}} - \frac{di_{cx\_ref}}{dt} - \frac{R_{shf}}{L_{shf}} i_{cx}\right)\left(\frac{2L_{shf}}{V_{dc}}\right) \tag{4.15}$$

The natural control limits of the circuit are $-1 \le u_{eqx} \le 1$; this expression could be utilized for establishing the design procedure and performance of the shunt converter. It can be seen that Eq. (4.17) is linear with respect to u_x such that

$$\text{If } u_x < u_{eqx} \text{ then } \dot{e}_x < 0 \tag{4.16}$$

If $u_x > u_{eqx}$ then $\dot{e}_x > 0$

Further, the equivalent control is driven by the natural bounds of the circuit i.e., $-1 \le u_{eqx} \le 1$, from which the following expressions can be summarized.

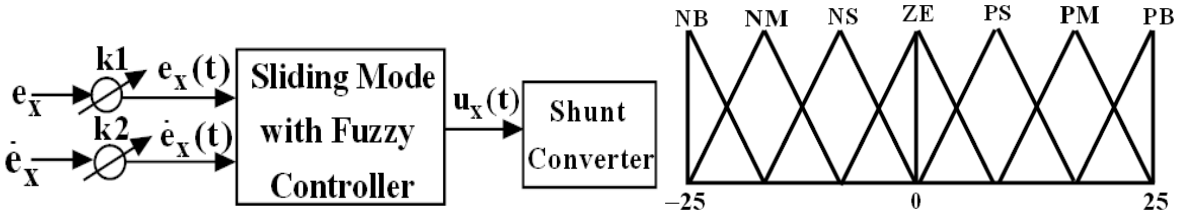
If $u_x = 1$ then $\dot{e}_x > 0$

$$\text{If } u_x = -1 \text{ then } \dot{e}_x < 0 \tag{4.17}$$

To satisfy $e_x \dot{e}_x \le 0$, the discontinuous control law can be seen by applying the variable e_x and $\dot{e}_x$ to the fuzzy controller and fuzzy controller must be satisfying the condition of Eq. (4.12) for generating the PWM signal for shunt converter.

$$u_x(t) = \begin{cases} 1 & for\ s(e_x, t) < 0 \\ 0 & for\ s(e_x, t) = 0 \\ -1 & for\ s(e_x, t) > 0 \end{cases} \tag{4.18}$$

The block diagram of proposed fuzzy sliding mode controller (FSMC) for shunt converter is shown in Fig.4.3 (a). Here e_x and $\dot{e}_x$ are the inputs and $u(t)$ represents the output of the FSMC. Further $e_x(t)$ and $\dot{e}_x(t)$ are the fuzzified variables and $u_x(t)$ is the defuzzified output in the form of gate pulse. Universes of discourse of $e_x(t)$ and $\dot{e}_x(t)$ are arranged from -25 to 25 whereas output universes of discourse are arranged from -1 to 1, thus the range of nonfuzzy variables e_x and $\dot{e}_x$ must be scaled by suitable gains k_1 and k_2 to fit the universe of discourse of fuzzified variables $e_x(t)$ and $\dot{e}_x(t)$. In this case $\dot{e}_x(t)$ is approximated by $(e(t)_k - e(t)_{k-1})/T$, where T is the sampling period. Here a triangular type membership function is chosen for the fuzzification of the input variable and singleton membership function is chosen as a defuzzified output variable, as shown in Fig. 4.6 (b) and Fig.4.7. The FSMC has to use the natural control conditions called Lyapunov stability conditions $e_x(t)\dot{e}_x(t) < 0$ with consideration of $e_x(t)$ and $\dot{e}_x(t)$ be the fuzzy variables of the system.



(a) (b)

Fig. 4.3 FSMC for shunt converter, (a) Block diagram representation, (b) Membership functions for the input variable $e_x(t)$ and $\dot{e}_x(t)$

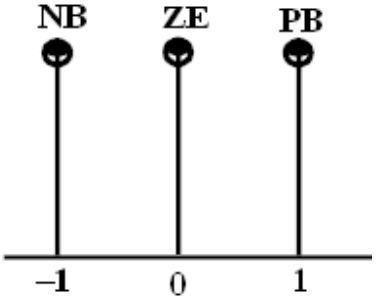


Fig.4.4 Membership functions for the output variable

A rule table shown in Table 4.1 is constructed by using two-dimensional space i.e., $e_x(t)$ and $\dot{e}_x(t)$, each having seven triangular membership functions with 49 fuzzy rules. Now, we choose a Lyapunov function for stability analysis,

$$V(t) = \frac{1}{2} e_x(t)^2 \tag{4.19}$$

Then

$$\dot{V}(t) = e_x(t)\dot{e}_x(t) \tag{4.20}$$

Based on the qualitative analysis described above and the Lyapunov stability condition ($e_x(t) = 0$ and $\dot{V}(t) < 0$), the sliding surface is asymptotically stable and simultaneously matches the reaching conditions $e_x(t)\dot{e}_x(t) < 0$.

Mamdani's min-operation fuzzy inference system is considered here and singleton defuzzification method is adopted for generating switching signal for shunt converter. The control rules of Table 4.1 are defined below:

(1) If $e_x(t)$ is PB and $\dot{e}_x(t)$ is PB, then $u_x(t)$ is NB.

Table 4.1 Rule based table for shunt FSMC

$e_x / \Delta e_x$	NB	NM	NS	ZE	PS	PM	PB
NB	PB	PB	PB	ZE	NB	NB	NB
NM	PB	PB	PB	ZE	NB	NB	NB
NS	PB	PB	PB	ZE	NB	NB	NB
ZE	PB	PB	PB	ZE	NB	NB	NB
PS	PB	PB	ZE	ZE	NB	NB	NB
PM	PB	ZE	ZE	NB	NB	NB	NB
PB	ZE	ZE	ZE	NB	NB	NB	NB

This control rule implies that if $e_x(t)$ and $\dot{e}_x(t)$ are both positive big (i.e., $e_x(t)\dot{e}_x(t)$ is largely positive), then a large negative change in the control input is required to decrease $e_x(t)\dot{e}_x(t)$ quickly.

(2) If $e_x(t)$ is PB and $\dot{e}_x(t)$ is NB, then $u_x(t)$ is ZE.

This control rule implies that if $e_x(t)$ is positive big and $\dot{e}_x(t)$ is negative big (i.e., no changes in $e_x(t)\dot{e}_x(t)$), then there is no change in the control input.

4.5.3 Fuzzy sliding mode for series APF

Fig.4.8 shows the single-phase equivalent circuit of series APF for the analysis of FSMC. The voltage and current at the converter side are represented as $u_c \frac{V_{dc}}{2}$ and i_f respectively. The ac-filter capacitor voltage and current are signified as V_{Cf} and i_{Cf} respectively. The voltage and current on the grid side are represented as V_C and i_{sf} respectively. We assume that injected voltage is equivalent to the voltage across the filter capacitor $\left(V_{Cf} = V_C\right)$ of the series converter and the injection transformer is recognized as ideal with 1: n turns ratio. With these assumptions, voltage and current at the output terminal of the series converter can be written as

$$\frac{di_f}{dt} = \frac{V_{dc}}{2L_{sef}} u_c - \frac{R_{sef}}{L_{sef}} i_f - \frac{1}{L_{sef}} V_{Cf} \tag{4.21}$$

$$\frac{dV_{Cf}}{dt} = \frac{dV_C}{dt} = \frac{1}{C_{ef}} i_f - \frac{1}{C_{ef}} i_{sf} \tag{4.22}$$

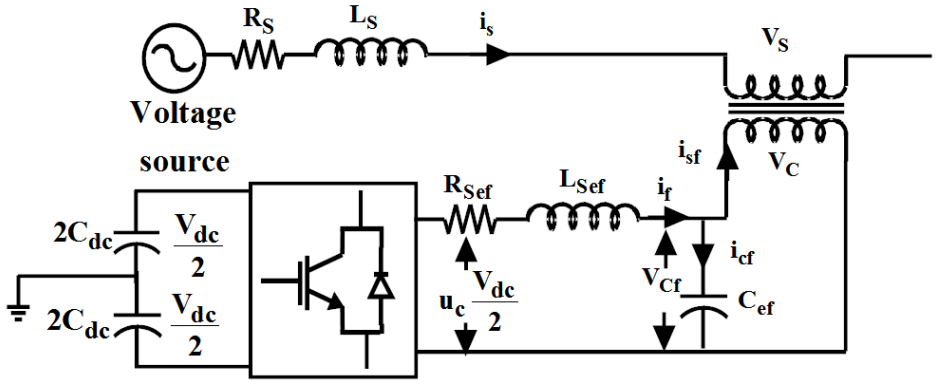


Fig.4.5 Equivalent circuit for a single phase of the series converter

The standard method for selecting the sliding surface for series converter is represented by the following equation.

$$s_x(t) = \dot{g}_x(t) \tag{4.23}$$

where x is phase sequence and the corresponding error function $g_x(t)$ is defined as,

$$g_x(t) = \left(V_{Cx\_ref} - V_{Cx}\right) \tag{4.24}$$

For the series converter, the expression for $\dot{s}(t)$ can be written as,

$$\dot{s}(t) = \ddot{g}(t) \tag{4.25}$$

Thus

$$\dot{s}_x(t) = \left(\ddot{V}_{Cx\_ref} - \ddot{V}_{Cx}\right) \tag{4.26}$$

Applying the value of dV_C/dt in Eq. (4.26), the value of $\dot{s}_x(t)$ becomes

$$\begin{aligned}\dot{s}_x(t) &= \left(\ddot{V}_{cx\_ref} - \frac{1}{C_{ef}}\dot{i}_{fx} + \frac{1}{C_{ef}}\dot{i}_{sfx}\right) \\ &= \ddot{V}_{cx\_ref} + \frac{1}{C_{ef}}\dot{I}_{sfx} - \frac{1}{C_{ef}}\left(\frac{V_{dc}}{2L_{sef}}u_{cx} - \frac{R_{sef}}{L_{sef}}i_{fx} - \frac{1}{L_{sef}}V_{cfx}\right)\end{aligned} \tag{4.27}$$

Setting the sliding surface $\dot{s}(t)$=0, the equivalent control law can be defined as

$$u_{eqsx} = \left(\frac{2R_{sef}}{V_{dc}}i_{fx} + \frac{2V_{Cf}}{V_{dc}} + \frac{2L_{sef}}{V_{dc}}\dot{i}_{sfx} + \frac{\ddot{V}_{cx\_ref}}{V_{dc}}2C_{ef}L_{sef}\right) \tag{4.28}$$

The existence of sliding mode is observed through the condition, $s(\dot{g}_x, t) = 0$. Hence, the switching law can be expressed by the following equation.

$$s(\dot{g}_x, t)\dot{s}(\ddot{g}_x, t) < 0 \tag{4.29}$$

Thus, the natural control limits of the series converter are $-1 \le u_{eqsx} \le 1$ and this expression is used for the equivalent control for both performance and design procedure of the converter. Also, it is observed that Eq. (4.25) is linear with respect to u_c such that

If $u_c < u_{eqsx}$ then $\dot{s}(\ddot{g}_x, t) > 0$

If $u_c > u_{eqsx}$ then $\dot{s}(\ddot{g}_x, t) < 0$ (4.30)

The equivalent control is constrained by the natural bounds of the converter, such that $-1 \le u_{eqsx} \le 1$ and it is observed that

If $u_c = -1$ then $\dot{s}(\ddot{g}_x, t) > 0$ (4.31)

If $u_c = 1$ then $\dot{s}(\ddot{g}_x, t) < 0$

For the fulfillment of this discontinuous control law, the actual error functions $\dot{g}$ and $\ddot{g}$ need to be scaled to their corresponding universes of discourse $\dot{g}(t)$ and $\ddot{g}(t)$ applied to the

fuzzy controller as shown in Fig. 4.9 (a). The scaling factors x_1 and x_2 corresponding to $\dot{g}(t)$ and $\ddot{g}(t)$ are arranged from -6 to 6.The output of the fuzzy controller is $k(t)$ which is defuzzified output and is arranged from -1 to 1. As data manipulation in fuzzy controller is based on the fuzzy set theory, the associated fuzzy subset defined for controlling the series converter are as follows,

$\dot{g}(t)$={NB,NM,NS,ZE,PS,PM,PB}

$\ddot{g}(t)$={NB,NM,NS,ZE,PS,PM,PB}

$k(t)$={NB,ZE,PB}

where NB is negative big, NM is negative medium, NS is negative small, ZE is zero, PS is positive small, PM is positive medium and PB is positive big. The membership functions for input fuzzy subsets $\dot{g}(t)$ and $\ddot{g}(t)$ are depicted in Fig. 4.9 (b) and corresponding output membership function $k(t)$ is shown in Fig.4.7. The resulting linguistic rule based on FSMC for series active power filter is summed in Table 4.2. Construction of the fuzzy rules is based on the following situation.

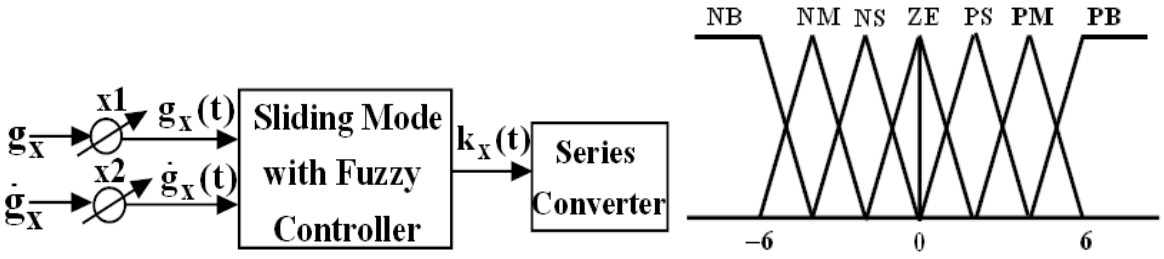
1) If $s(\dot{g}_x,t)<0$ and $\dot{s}(\ddot{g}_x,t)$<0, then declining k_j will increase $s(\dot{g}_x,t)$ $\dot{s}(\ddot{g}_x,t)$ and the system will go towards the stable region.

2) If $s(\dot{g}_x,t)>0$ and $\dot{s}(\ddot{g}_x,t)>0$, then growing k_j will decrease $s(\dot{g}_x,t)$ $\dot{s}(\ddot{g}_x,t)$ and the system will go towards the stable region.

The fuzzy rule is formed by using discontinuous control law of Eq. (4.32),

$$u_{cx}=\begin{cases} 1 & for\ s(\dot{g}_x,t)>0 \\ 0 & for\ s(\dot{g}_x,t)=0 \\ -1 & for\ s(\dot{g}_x,t)<0 \end{cases} \tag{4.32}$$

Based on the fuzzy rule described in Table 4.2, the fuzzy controller can generate PWM signal for series converter and series compensation voltage can be injected for recompensing symmetrical and unsymmetrical sag/swell, voltage harmonics and voltage unbalance.



(a) (b)

Fig. 4.6 FSMC for series converter, (a) Block diagram representation, (b) Membership functions for the input variable $\dot{g}(t)$ and $\ddot{g}(t)$.

Table 4.2 Rule based table for series FSMC

$\dot{g}$ / $\Delta\dot{g}$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	ZE	PB	PB	PB
NM	NB	NB	NB	ZE	PB	PB	PB
NS	NB	NB	NB	ZE	PB	PB	PB
ZE	NB	NB	NB	ZE	PB	PB	PB
PS	NB	NB	ZE	ZE	PB	PB	PB
PM	NB	ZE	ZE	PB	PB	PB	PB
PB	ZE	ZE	ZE	PB	PB	PB	PB

4.6 Performance analysis

4.6.1 Simulation and real-time HIL based OPAL-RT result of ROT with NVGF hysteresis controller

To validate the performance of the proposed ROT based NVGF hysteresis control, a comprehensive simulation and experimental studies are conducted in the MATLAB/SIMULINK and real-time HIL based OPAL-RT system environment respectively. The simulated test system data are given in Appendix-1.

Fig.4.10 and 4.11 illustrate the simulation and experimental result for performance of proposed EPLL technique in distorted voltage condition. Fig.4.10 (a) and (b) show the simulation result of distorted source voltage and transformation angle (ωt) for the EPLL technique. From the above figure it is observed that the transformation angle (ωt) of the EPLL has a negligible oscillation under highly distorted condition. Therefore, unit sine vector signal generation using EPLL is purely sinusoidal and in phase with supply voltage that is shown in Fig. 4.10 (c). Fig.4.11 demonstrates the experimental result of EPLL in voltage distortion condition. Fig.4.11 (a) shows the distorted supply voltage and transformation angle (ωt) for the conventional PLL. Fig.4.11 (b) shows the unit sine vector signal generation and transformation angle (ωt) using EPLL. It is observed from this figure

that EPLL technique exhibits better performance as the transformation angle of the EPLL has a negligible oscillation under highly distorted conditions.

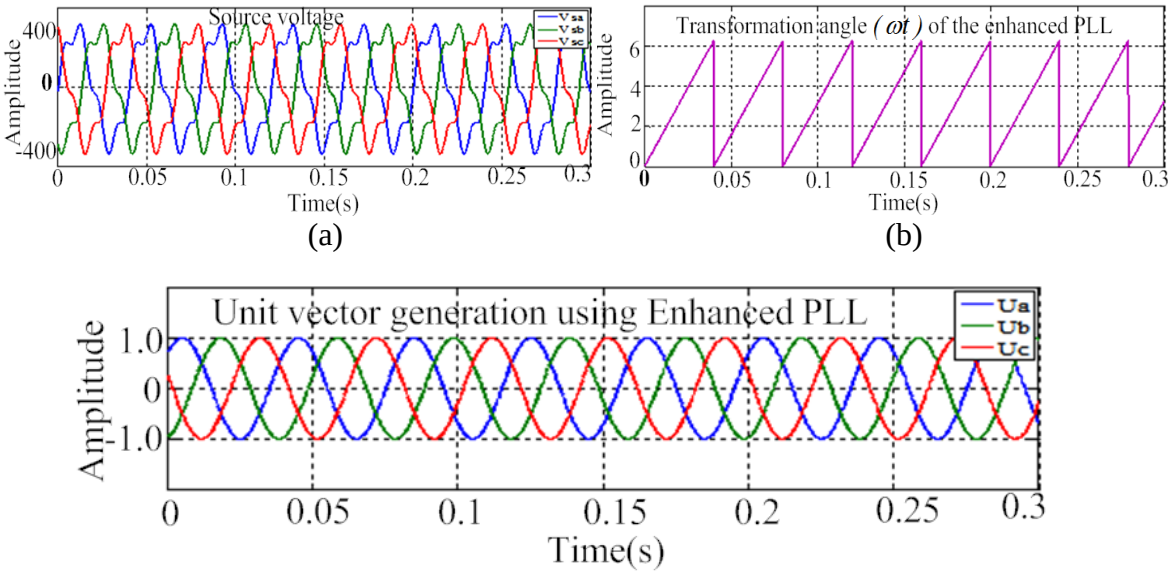


Fig.4.7 Simulation results of EPLL algorithm under distorted supply condition, (a) Distorted supply voltage, (b) Transformation angle (ωt) of EPLL, (c) Unit vector signal from EPLL.

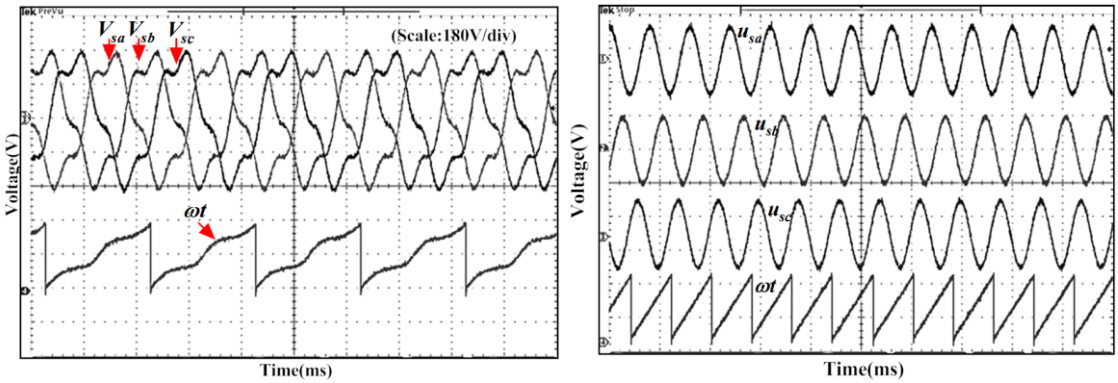
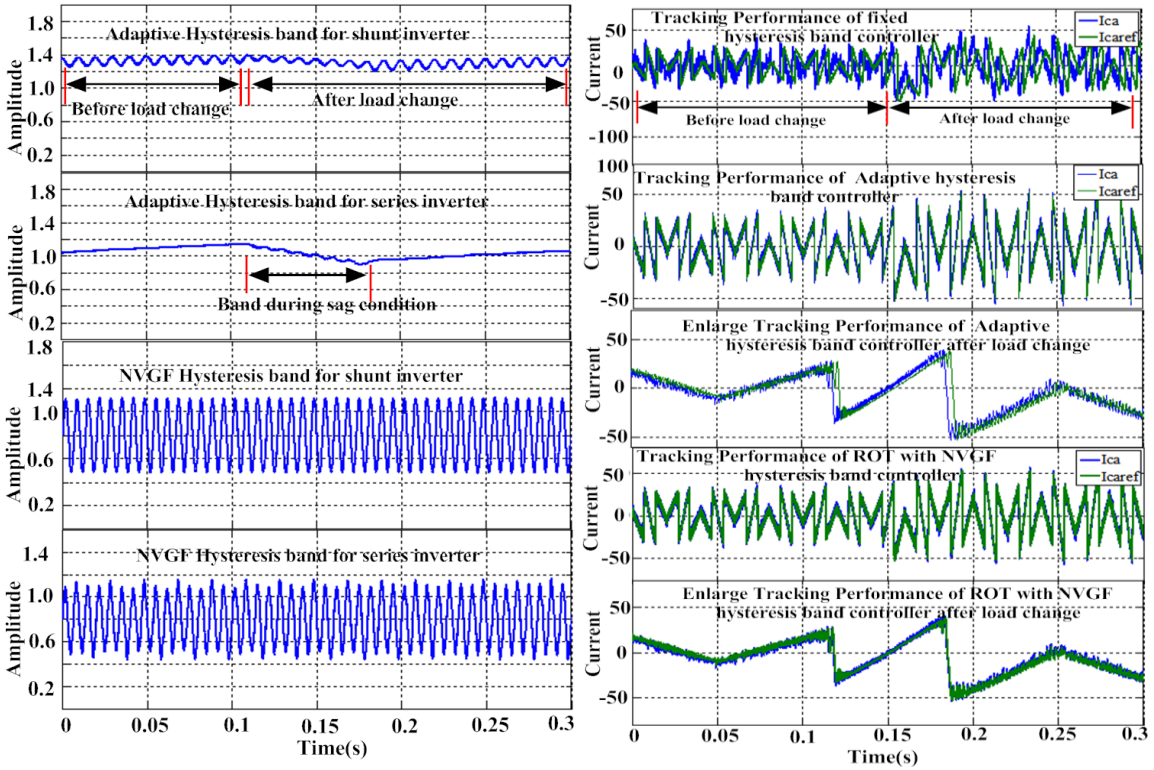


Fig.4.8 Real-time experimental results of EPLL algorithm under distorted supply condition (a) Distorted supply voltage and transformation angle (ωt) of conventional PLL (scale: 2 V/div), (b) Unit vector signal generation using EPLL technique (scale: 1 V/div) and transformation angle (ωt) of EPLL technique (scale: 2 V/div).

Performance of the hysteresis band during a load transient and voltage sag condition by using NLSMC-AHB and ROT-NVGF hysteresis band controller is shown in Fig.4.12 (a) from top to bottom order. From this figure it is observed that AHB of shunt APF produces

hysteresis band with slight variation thus keeps switching frequency partially constant and band violation relatively less during a load transient condition. Whereas, the NVGF hysteresis band for shunt controller generates variable band to keep the switching frequency nearly constant during all operating conditions of load and provides better tracking performance in comparison to the AHB controller. Additionally, AHB controller for series APF provides almost linear hysteresis band and a small band violation is occurred during sag condition, therefore switching frequency is partially constant. On the other hand, NVGF hysteresis band for series APF produces variable hysteresis band to keep the switching frequency nearly constant during all operating conditions of supply voltage.

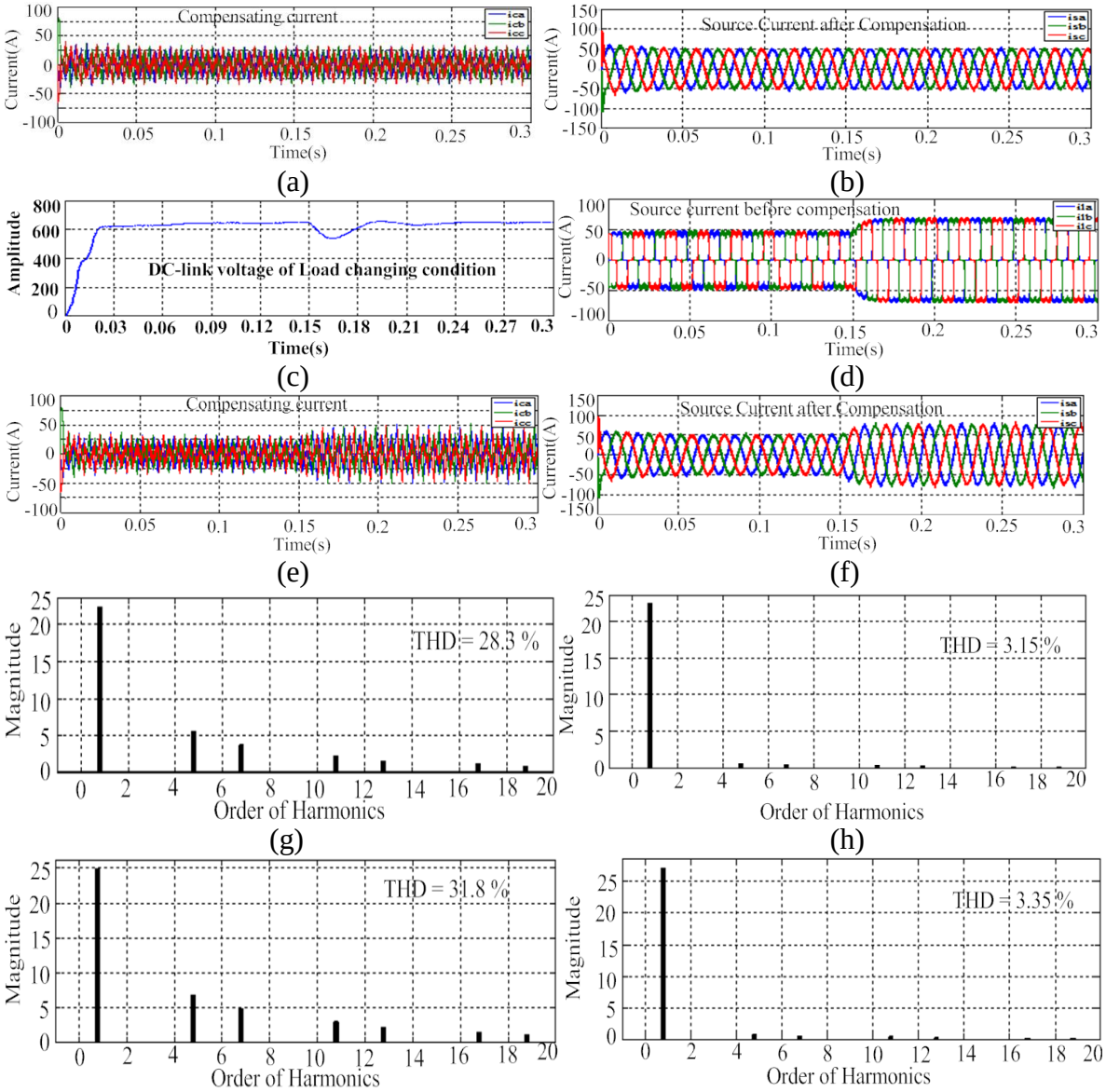
The compensating current tracking performances of fixed hysteresis and adaptive hysteresis band controller as well as ROT with NVGF hysteresis band controller are



(a) (b)

Fig.4.9 Hysteresis band and tracking performance of reference signal, (a) Adaptive hysteresis band and NVGF Hysteresis band controller for shunt and series APF, (b) Performance comparison for tracking of compensating reference signal using NLSMC with AHB and ROT with NVGF hysteresis band controller.

Fig.4.13 (a) and (b) deliver the information about compensating current and source current under steady-state condition. Fig. 4.13 (c) and 4.14 (a) display the simulation and experimental result of ROT-NVGF controller for controlling the dc-link voltage during transient state condition of load. The load parameters are changed to ($R_L = 25\,\Omega$ and $L_L = 34\,mH$) from $t = 0.15\,s$ to $t = 0.3\,s$. Fig. 4.13 (d) and 4.14 (b) provide the information about source current before compensation. Fig. 4.13 (e) and (f) as well as Fig. 4.14 (c) and (d) provide the information regarding compensating current and source current after compensation respectively. It is observed from the figure that, the shunt APF performance is quite satisfactory during load side transient condition. Therefore, the source current is sinusoidal in nature without any ripple.



(i) (j)

Fig.4.10 Simulation results, (a) Compensation current during steady-state condition, (b) Source current after compensation during steady-state condition, (c) DC-link voltage under transient condition, (d) Source current before compensation during transient-state condition, (e) Compensation current during transient-state condition, (f) Source current after compensation during transient-state condition, (g) Source current spectrum before compensation during steady-state condition, (h) Source current spectrum after compensation during steady-state condition (i) Source current spectrum before compensation during transient-state condition, (j) Source current spectrum after compensation during transient-state condition.

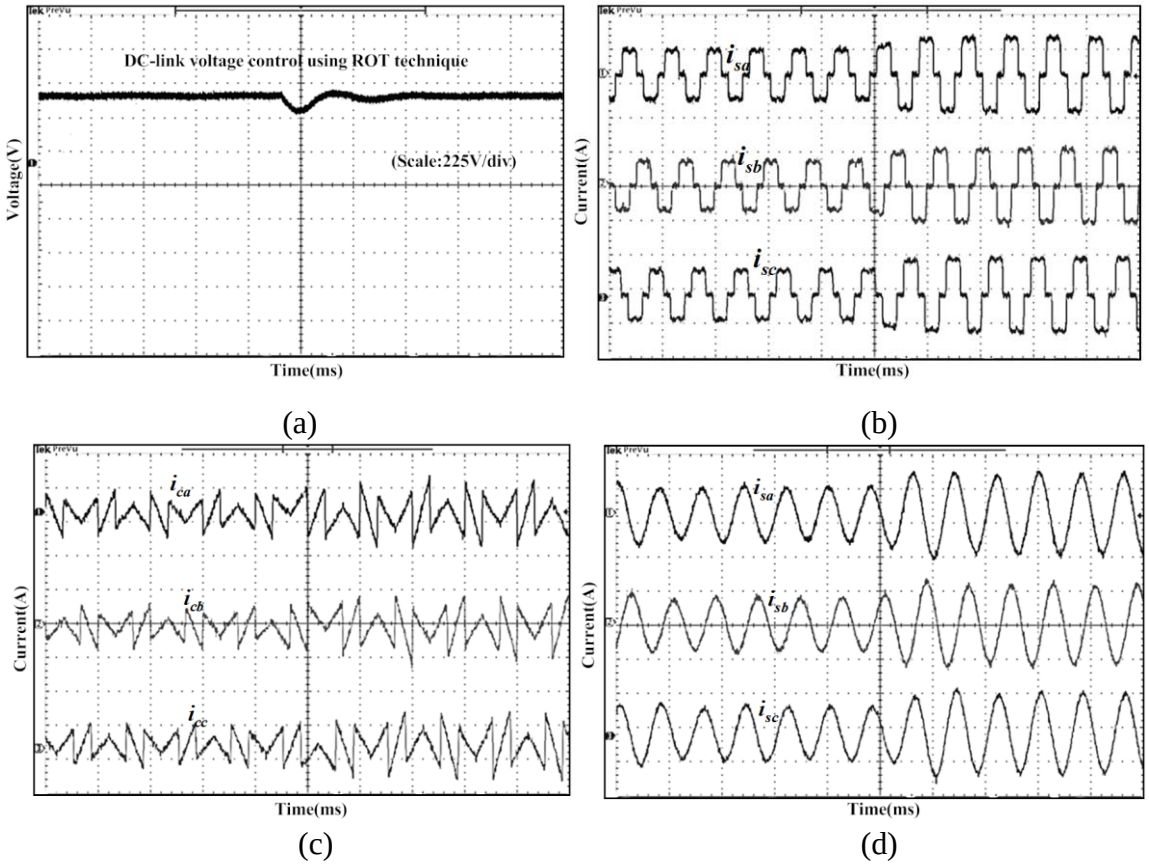


Fig.4.11 Real-time experimental results, (a) DC-link voltage under transient condition, (b) Source current before compensation (scale: 62 A/div), (c) Compensation current (scale: 40 A/div), (d) Source current after compensation (scale: 65 A/div).

Moreover, Fig.4.13 (g) and (h) give the information regarding THD of the source current before and after compensation during steady-state condition and they are observed to be

28.3 % and 3.15 % respectively. Similarly, Fig.4.13 (i) and (j) provide the information about the THD of source current before and after compensation under transient-state condition and they are observed to be 31.8 % and 3.35 % respectively.

Fig.4.15 and 4.16 illustrate the simulation as well as real-time experimental results during sag conditions. Fig. 4.15 (a) and 4.16 (a) show the DC-link voltage of proposed method during sag condition. Fig.4.15 (b) and 3.16 (b) show the waveform of voltage sag of 4 cycles with a depth of 20 % and its corresponding compensating voltage and load voltage after compensation are shown in Fig. 4.15 (c) and (d) as well as Fig.4.16 (c) and (d) respectively. From the figure it is observed that, the series APF of UPQC compensates the voltage sag by injecting a voltage with proper amplitude and polarity.

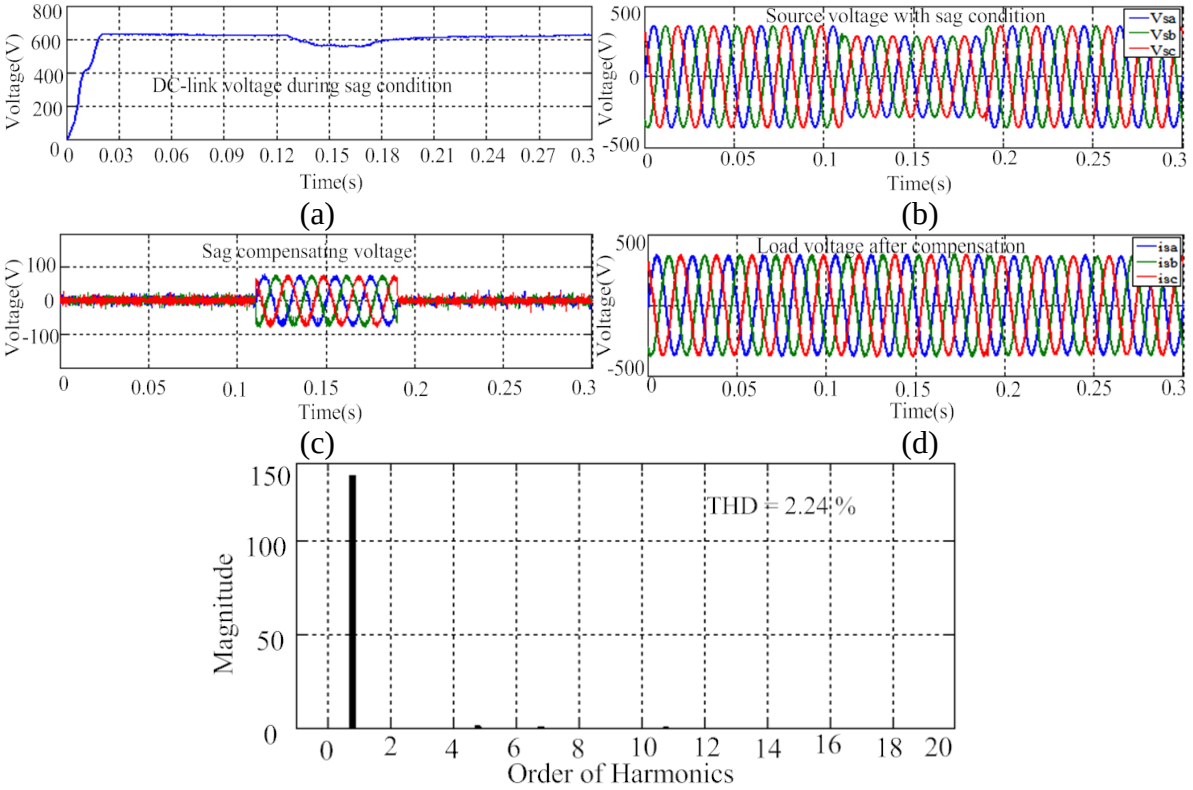


Fig.4.12 Simulation results during sag condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

Fig.4.15 (e) displays THD information of load voltage after compensation and it is found to be 2.24 %. Correspondingly, Fig. 4.17 and 4.18 demonstrate the simulation as well as

real-time experimental results of dc-link voltage, supply voltage, compensating voltage and load voltage after compensation during swell conditions. Fig. 4.17 (a) and 4.18 (a) show the dc-link capacitor voltage of proposed controller during the voltage-swell condition. Fig.4.17 (b) and 4.18 (b) show the waveform of supply voltage swell of 20 % obtained for 4 cycles and its corresponding compensating voltage and load voltage are shown in Fig.4.17 (c) and (d) as well as Fig. 4.18 (c) and (d) respectively. It is observed from the figure that the proposed control strategy can compensate the voltage swell existing in the supply voltage and regulate the load voltage to its nominal value. Fig. 4.17 (e) shows the information about THD spectrum of load voltage after compensation and its THD is around 2.18 %.

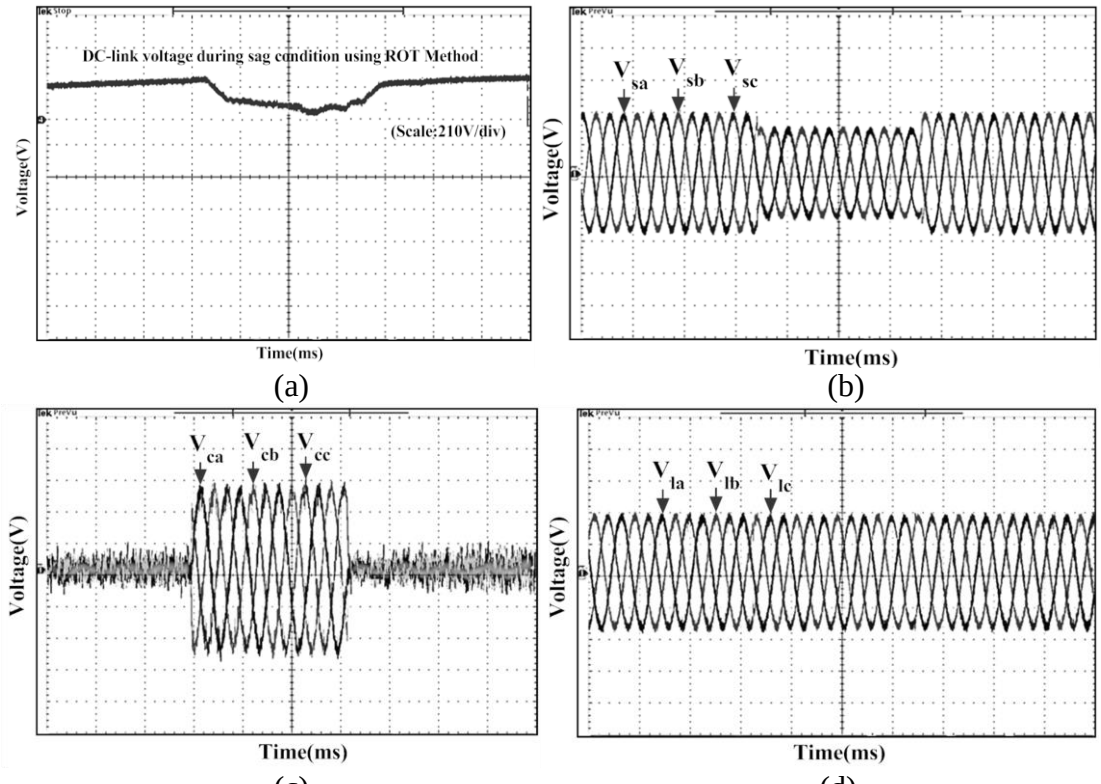
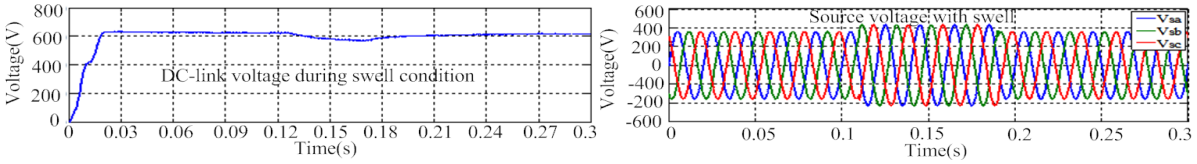


Fig.4.13 Real-time experimental results during sag condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 65 V/div), (d) Load voltage after compensation (scale: 200 V/div).



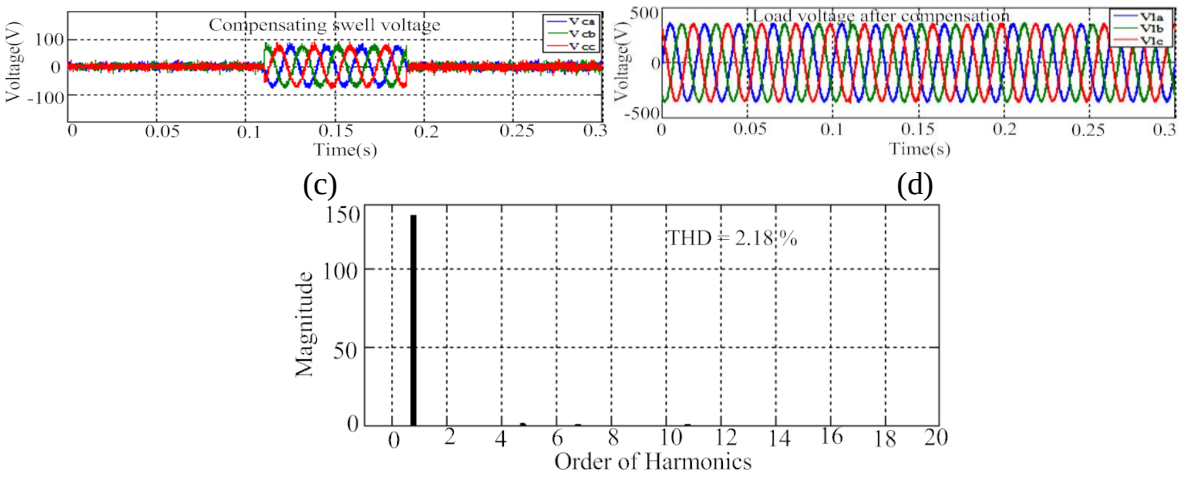


Fig.4.14 Simulation results of swell condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

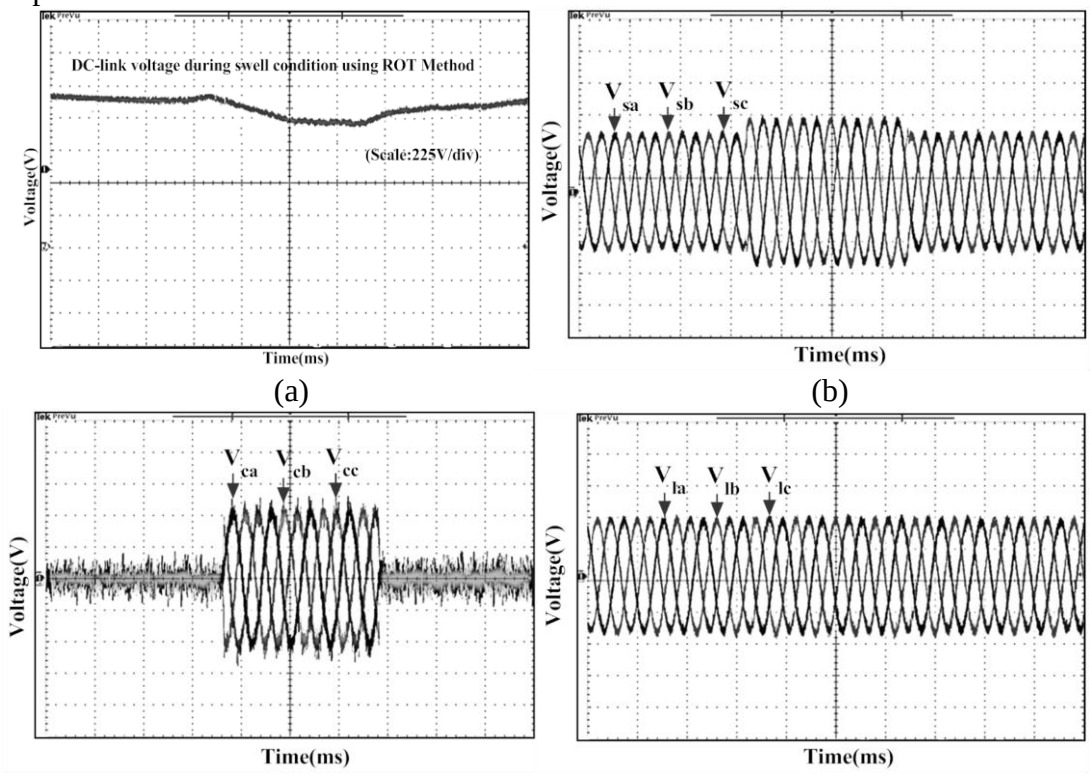
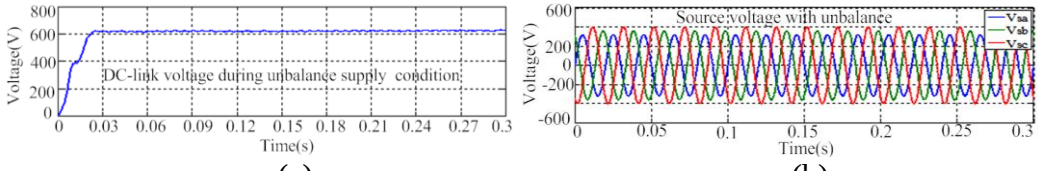


Fig.4.18 Real-time experimental results during swell condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 73 V/div), (d) Load voltage (scale: 200 V/div).



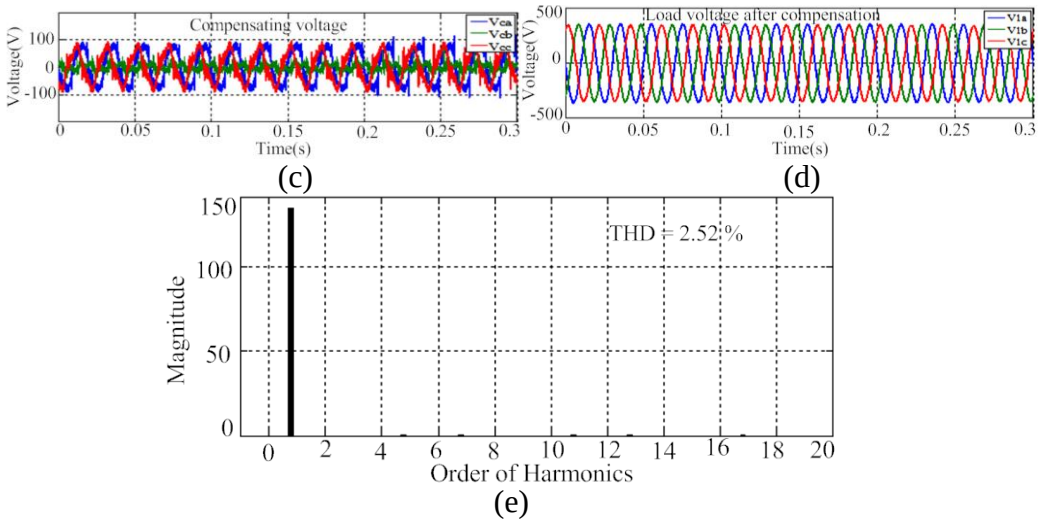


Fig.4.15 Simulation results during unbalanced supply condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Load voltage spectrum after compensation.

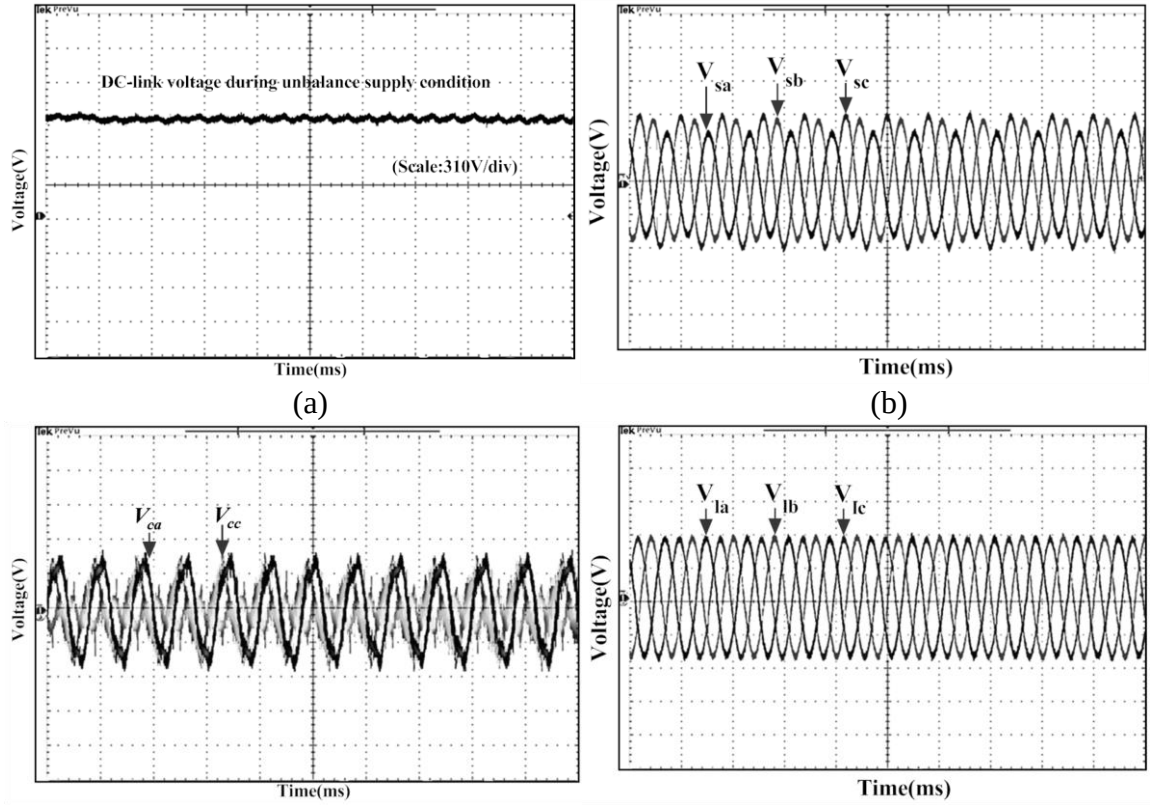


Fig.4.16 Real-time experimental results during unbalanced supply condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 80 V/div), (d) Load voltage after compensation (scale: 200 V/div).

Fig. 4.19 (a) and 4.20 (a) provide information about simulation as well as experimental results of dc-link capacitor voltage during unbalanced supply voltage condition. Fig. 4.19 (b), (c) and (d) as well as Fig. 4.20 (b), (c) and (d) show the unbalanced source voltage ($V_{sa} = 290\ V$, $V_{sb} = 360\ V$ and $V_{sc} = 410\ V$), compensating voltage and load voltage after compensation of the proposed method respectively. Series APF of the UPQC injects a proper voltage for regulating the load voltage to its nominal value. Fig. 4.19 (e) shows the THD spectrum of load voltage after compensation and it is found to be 2.88 %.

Fig.4.21 and 4.22 depict the simulation and experimental study of voltage distortion compensation capability of the proposed algorithm. In this case, a 2 % of the 5th and 1 % 7th harmonic voltage have been mixed with the grid voltage to create voltage distortion. The series APF of UPQC acts as a series-type distortion voltage compensator to filter out distortion components and provides quality voltage to the load. Fig 4.21 (b), (c) and (d) represent the simulation result of source voltage, compensating voltage and load voltage after compensation respectively.

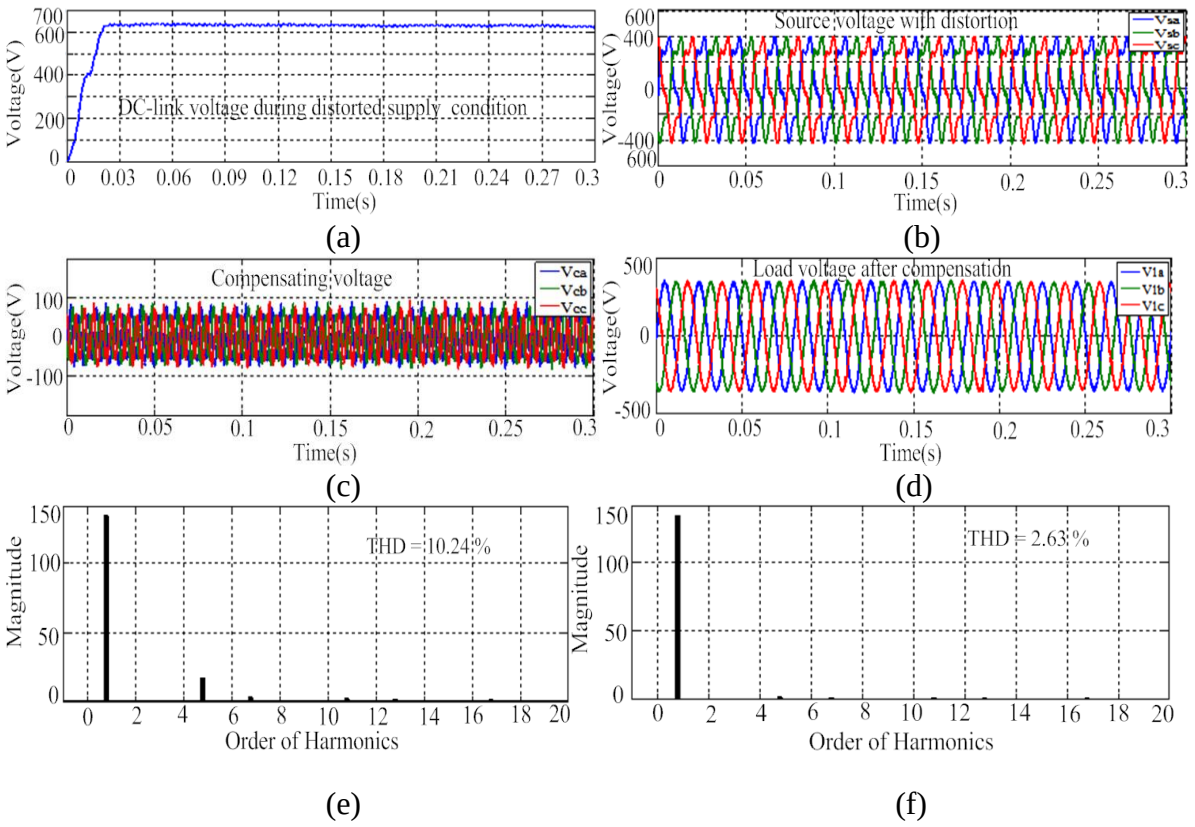
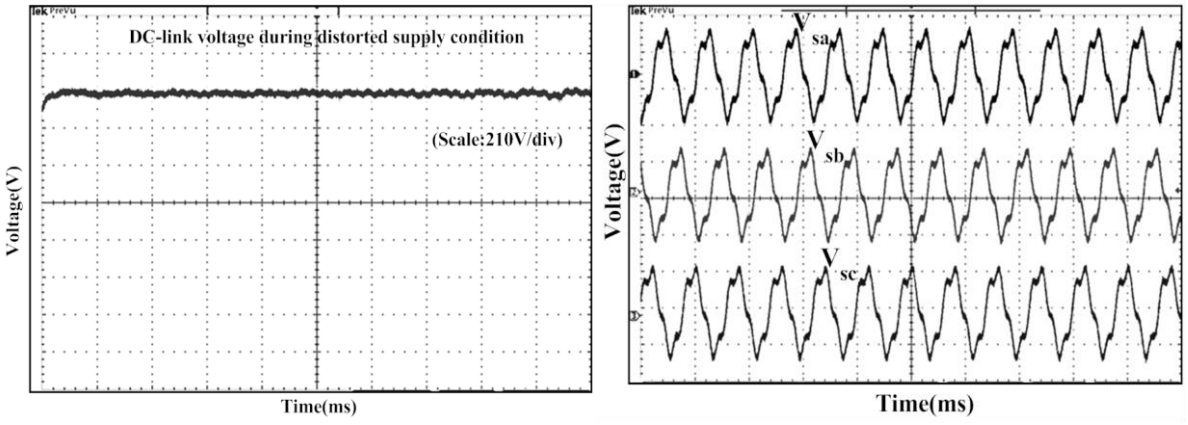
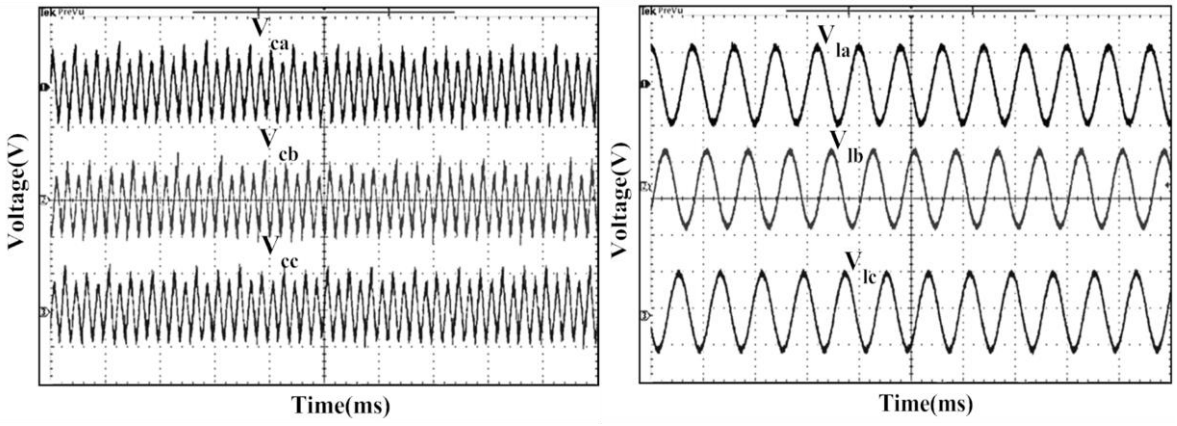


Fig.4.17 Simulation results during distorted supply condition, (a) DC-link voltage, (b) Source voltage, (c) Compensation voltage, (d) Load voltage after compensation, (e) Distorted supply voltage spectrum, (f) Load voltage spectrum after compensation.

Similarly, Fig 4.22 (b), (c) and (d) represent the real-time experimental result of source voltage, compensating voltage, load voltage after compensation and dc-link voltage respectively. From the figure it is observed that the load voltage waveform is quite clean and sinusoidal. Thus, it is confirmed that series APF of UPQC can compensate the source voltage distortion by utilizing the proposed algorithm. Fig. 4.21 (e) and (f) illustrate the THD spectrum of load voltage before and after compensation and they are found to be 9.34 % and 3.23 % respectively.



(a) (b)

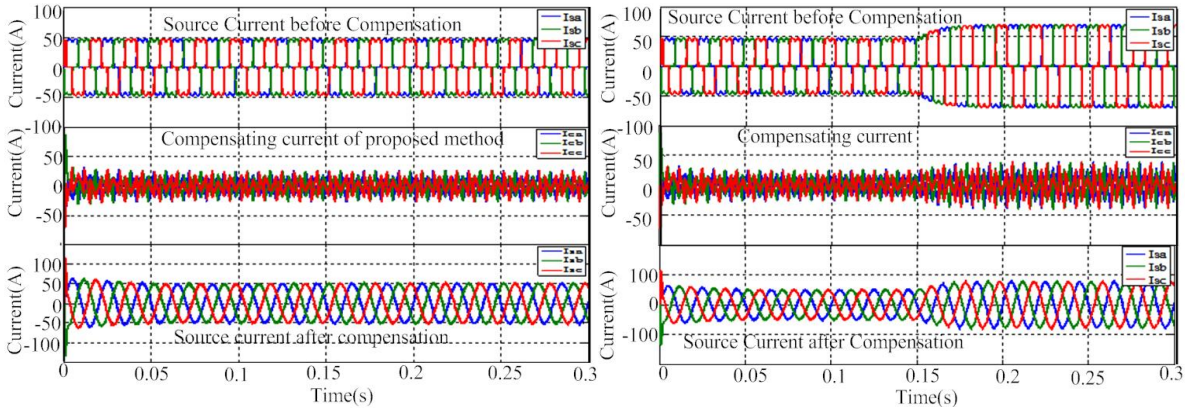


(c) (d)

Fig.4.18 Real-time experimental results under distorted supply voltage condition, (a) DC-link voltage, (b) Source voltage (scale: 200 V/div), (c) Compensation voltage (scale: 25 V/div), (d) Load voltage after compensation (scale: 200 V/div).

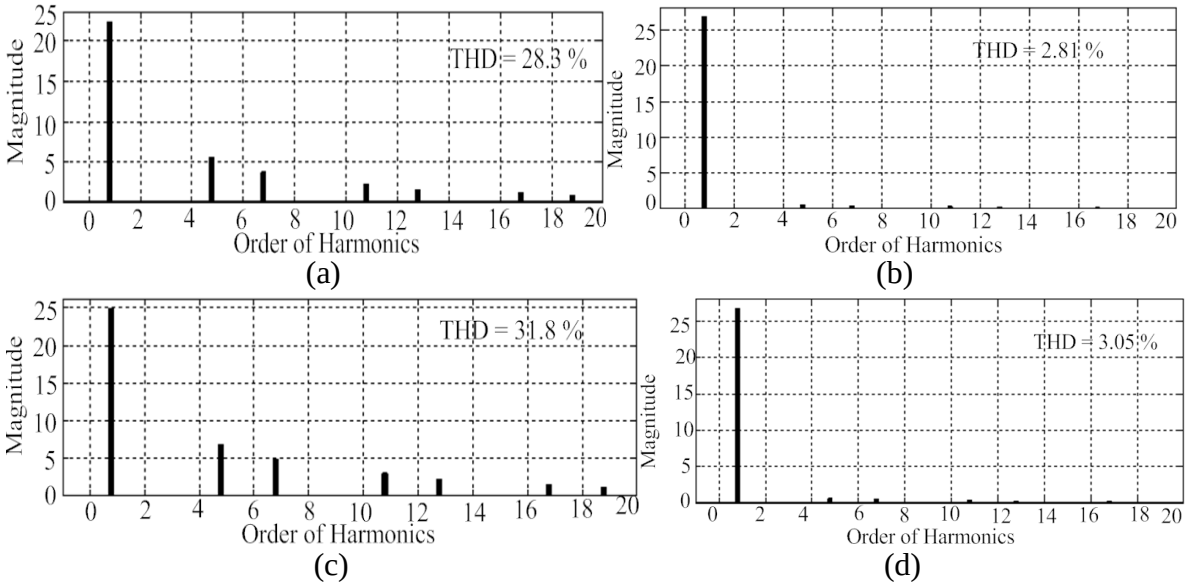
4.6.2 Simulation and real-time HIL based OPAL-RT result of OAP with FSMC-PWM controller

To verify the effectiveness of UPQC, the proposed control strategy has been tested using MATLAB/SIMULINK and real-time HIL based OPAL-RT system. The system parameters are given in the Appendix-1. The performance of UPQC using OAP with FSMC strategy is tested under different power quality events like current harmonics, voltage distortion, voltage sag, voltage swell and unbalanced supply voltage condition.



(a) (b)

Fig.4.23 Simulation result of shunt APF, (a) Shunt APF compensation waveforms during steady state condition, (b) Shunt APF compensation waveforms during transient-state condition.



(a) (b)

(c) (d)

Fig.4.19 Current harmonics spectrum before and after compensation, (a) Source current spectrum before compensation during steady-state condition, (b) Source current spectrum after compensation during steady-state condition (c) Source current spectrum before compensation during transient-state condition, (d) Source current spectrum after compensation during transient-state condition.

Current harmonics suppression capability of shunt APF is analyzed in both steady state and transient state conditions. Fig.4.23 (a) illustrates the simulation result of shunt APF during steady-state condition. From top to bottom, the waveforms are source current before compensation, compensating current and source current after compensation respectively. From the results, it is clear that the proposed OAP-FSMC current control technique for shunt APF of UPQC provides an effective compensation of current harmonics reducing THD from 28.3 % to 2.47 % in the source current. The performance of current harmonics filtering of shunt APF during load transient condition is illustrated in Fig.4.23 (b). During transient state, the source current THD before and after compensation are found to be 31.8 % and 3.05 % respectively.

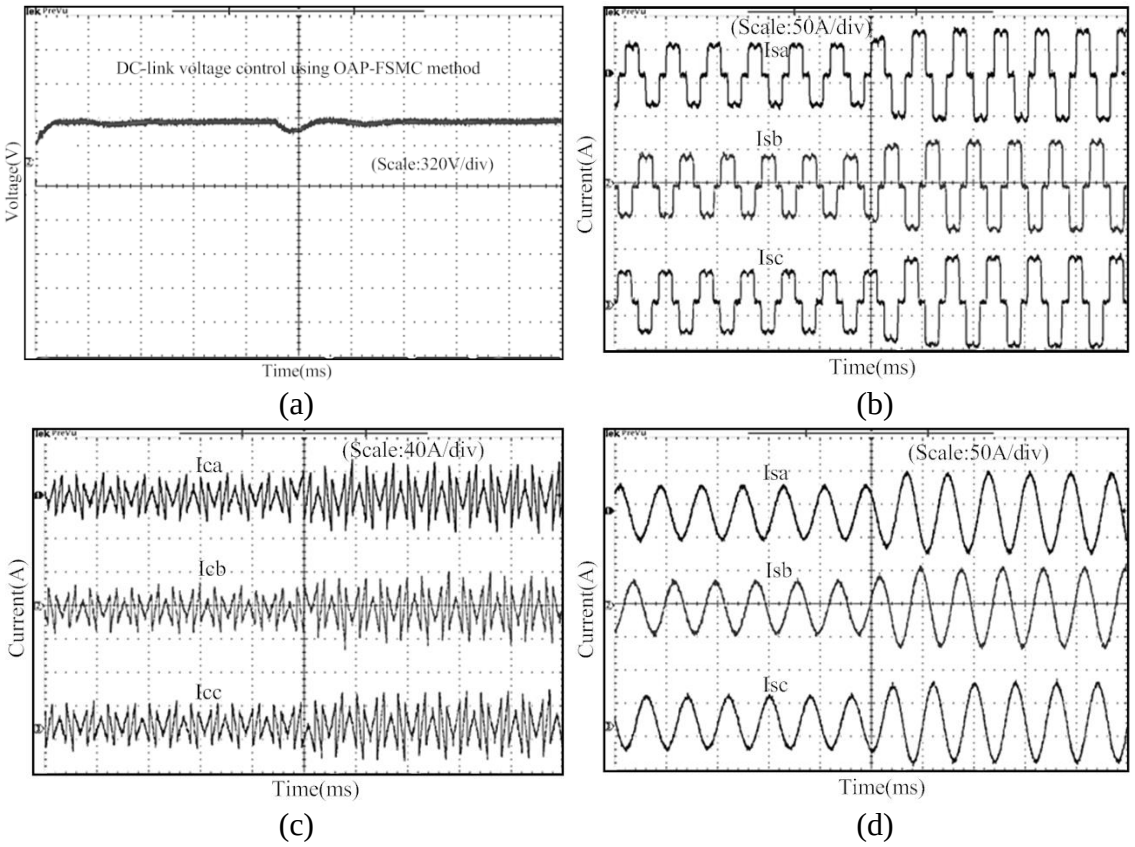
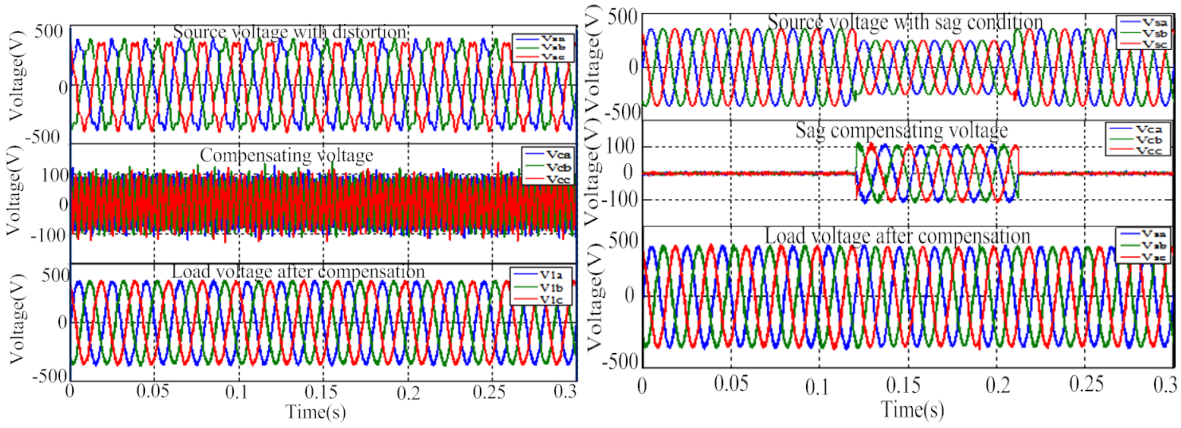


Fig.4.20 Real-time experimental results of shunt APF of UPQC during transient condition, (a) DC-link voltage during transient-state, (b) Source current before compensation under transient-state, (c) Compensation current under transient -state (d) Source current after compensation under transient -state

Fig.4.24 (a) and (b) convey the information regarding the THD of source current before and after compensation during steady-state condition. Similarly, Fig. 4.24 (c) and (d) provide information about THD of source current before and after compensation under transient-state condition. Table 4.3 lists THD of source current before and after compensation using ROT-NVGF control method and OAP-FSMC method. It indicates that proposed OAP-FSMC strategy can satisfactorily eliminate all the harmonics from the source current by injecting proper compensation current and makes the source current clean and sinusoidal, which confirms the superiority of the proposed OAP-FSMC strategy over ROT-NVGF control strategy.

The real time experimental verifications for shunt APF of UPQC during transient-state load condition are depicted in Fig. 4.25. The experimentation has been accomplished at switching frequency of 10 kHz. Fig. 4.25 (a), (b), (c) and (d) depict the transient-state performance of DC-link voltage, source current before compensation, compensating current as well as source current after compensation respectively.



(a) (b)

Fig.4.21 Simulation result of distorted and supply voltage sag condition, (a) Series APF compensation waveform during voltage distortion condition, (b) Supply voltage sag compensation waveform.

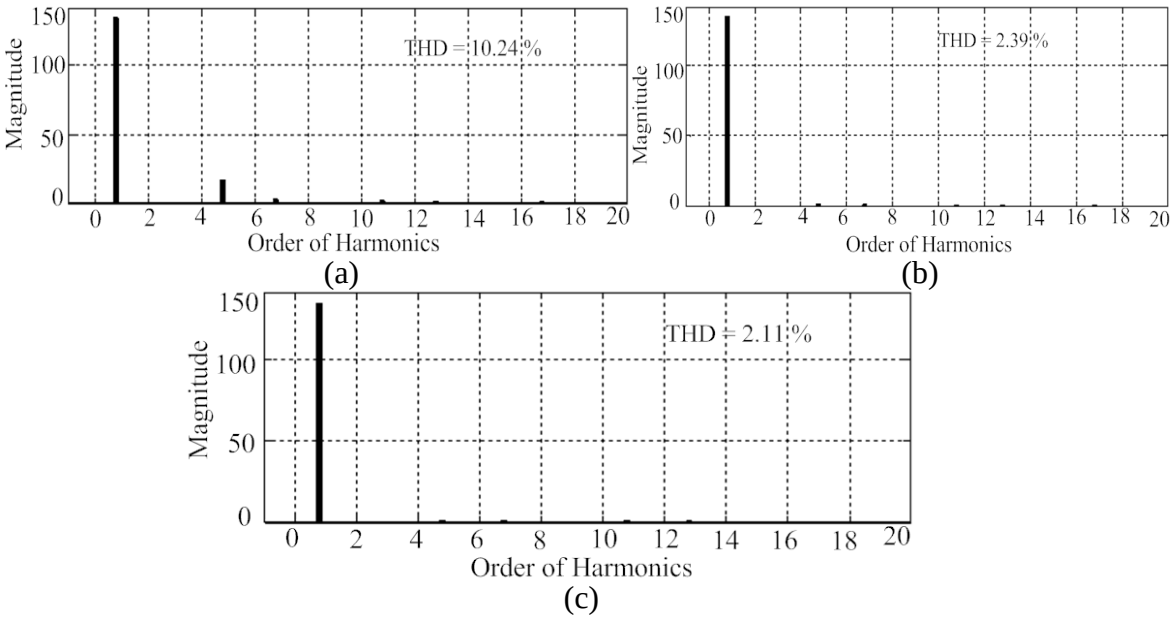
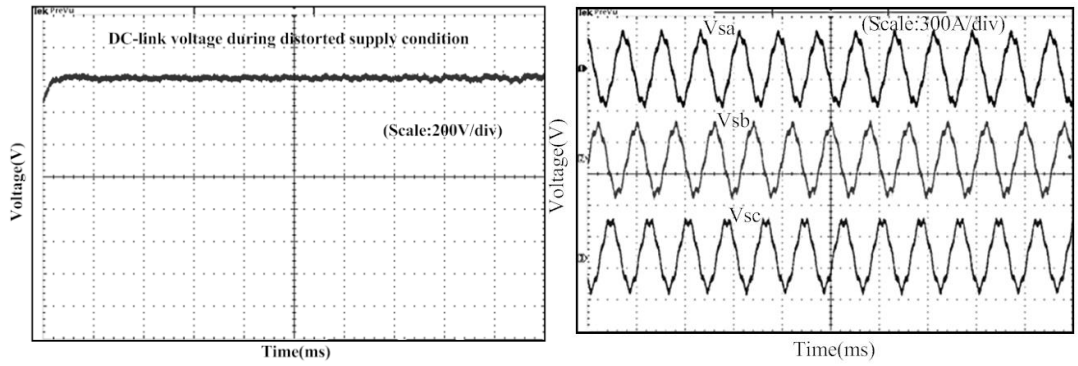


Fig. 4.22 Voltage distortion and sag compensation spectrum, (a) Distorted supply voltage spectrum, (b) Load voltage spectrum after compensation during distorted supply condition, (c) Load voltage spectrum after compensation during sag condition.

Fig.4.26 (a) depicts the performance of UPQC for voltage distortion compensation of proposed OAP-FSMC method. The source voltage, compensating voltage and load voltage after compensation with proposed OAP-FSMC method are shown in figure from top to bottom order respectively. Fig.4.27 (a) and (b) illustrate THD spectrum of load voltage before and after compensation during supply voltage distortion condition and they are found to be 10.24 % and 2.49 % respectively. Table 4.3 gives the THD analysis of both ROT-NVGF controller and OAP-FSMC method. From the tabulation, it is clear that the proposed OAP-FSMC strategy can satisfactorily eliminate all the distortions in the source voltage by injecting proper compensation voltage and makes the load voltage free from all such disturbances, which confirms the superiority of the proposed OAP-FSMC strategy over ROT-NVGF control strategy.



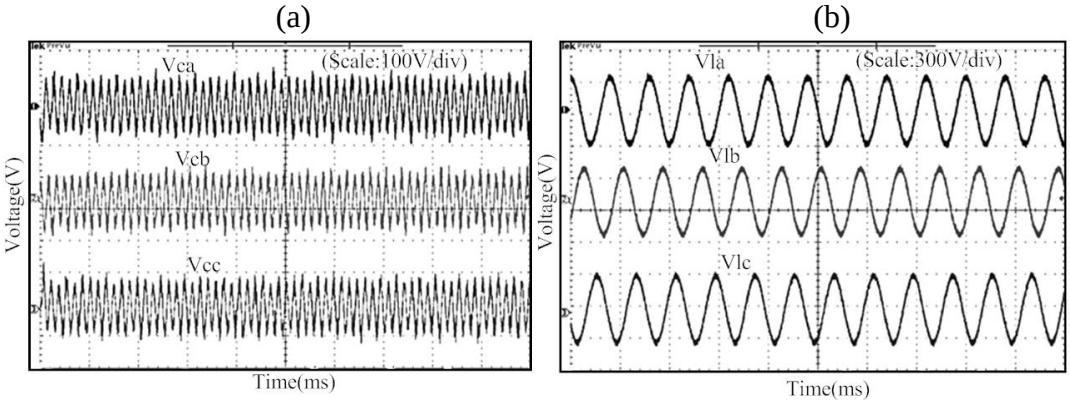
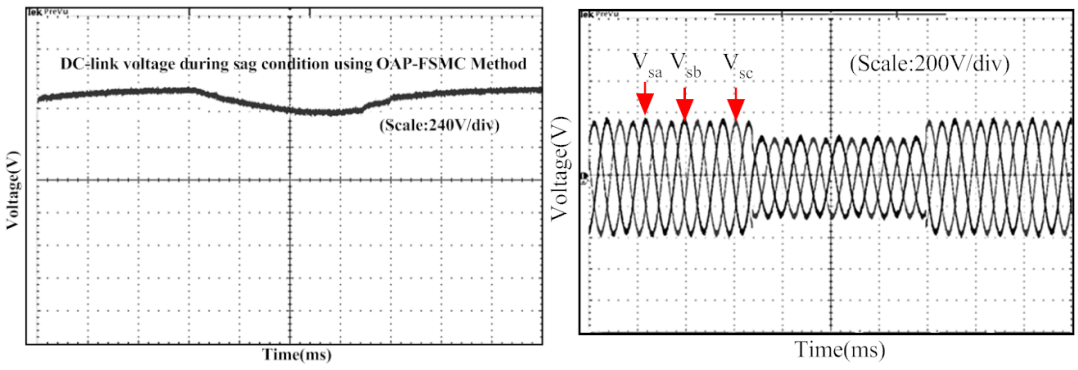
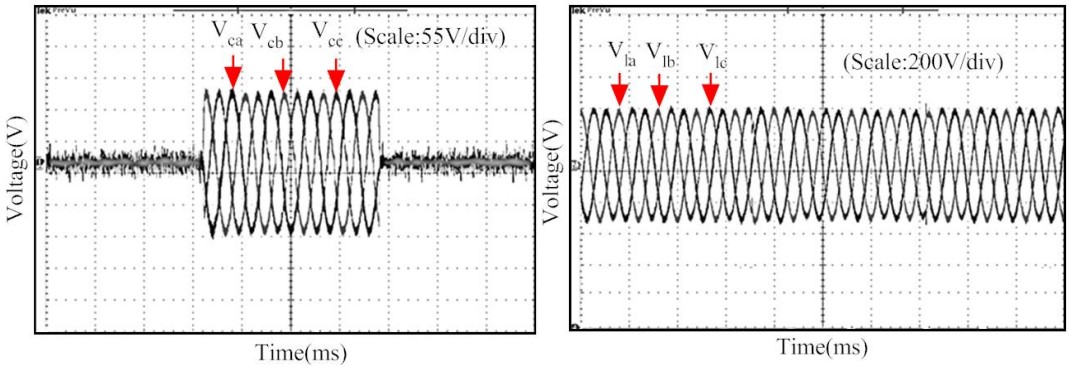


Fig.4.23 Real-time experimental results of series APF of UPQC, (a) DC-link voltage during distorted supply condition, (b) Source voltage under distortion condition, (c) Distortion compensation voltage, (d) Load voltage after distortion compensation.

Further, in case of supply voltage sag condition, 30 % of sag occurring in the interval of $0.12\,s \le t \le 0.21\,s$ is considered for four cycles of ac-mains. Fig.4.26 (b) shows the compensation effectiveness of proposed OAP-FSMC technique during the sag condition. From the top to bottom, the waveforms observed are supply voltage, compensating voltage and load voltage of sag condition. Fig. 4.27(c) displays the THD spectrum of load voltage after compensation during sag condition and it is found to be 2.11 %. Table 4.4 gives the THD comparison of load voltage during sag condition employing ROT-NVGF and OAP-FSMC technique. From the table it is found that the OAP-FSMC strategy can effectively compensate the load voltage with less THD in comparison to the ROT-NVGF control technique.



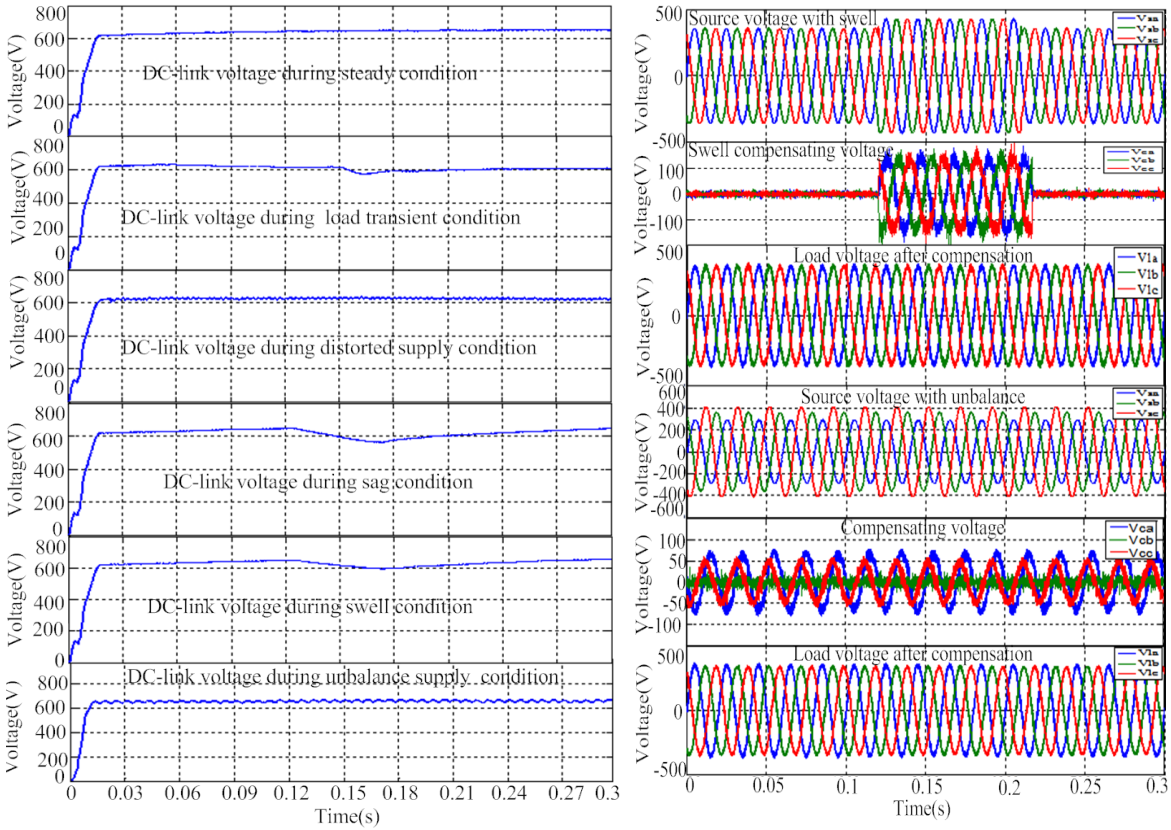


(c) (d)

Fig.4.24 Real-time experimental results of series APF of UPQC during sag condition, (a) DC-link voltage during sag condition, (b) Sag Voltage, (c) Sag compensation voltage, (d) Load voltage after compensation during sag condition.

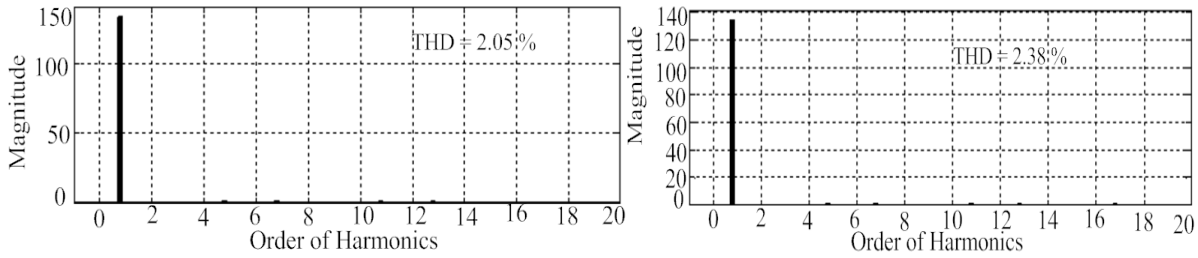
Fig.4.28 shows a real-time experimental result of voltage distortion compensation capability of the OAP-FSMC strategy. Fig.4.28 (a), (b), (c), and (d) show the experimental result of DC-link voltage, distorted voltage, compensating voltage and load voltage after compensation respectively. From the figure it is observed that the load voltage waveforms V_{la}, V_{lb} and V_{lc} are all sinusoidal. This confirms that series APF of UPQC can efficiently compensate the source voltage distortion by utilizing the proposed OAP-FSMC algorithm.

Fig. 4.29 shows the experimental result of voltage sag compensation capability of the OAP-FSMC method. Fig. 4.29 (a), (b), (c) and (d) show the experimental results of DC-link voltage, supply voltage, compensating voltage and load voltage after compensation respectively. The series APF of the UPQC injects a proper voltage during voltage sag leading to a compensating load voltage.



(a) (b)

Fig.4.25 Simulation results of DC-link voltage, swell and unbalanced supply compensation, (a) DC-link voltage waveforms of shunt and series APF, (b) Swell and unbalanced supply compensation waveforms.



(a) (b)

Fig. 4.26 Voltage swell and supply voltage unbalanced compensation spectrum, (a) Load voltage spectrum after compensation during voltage swell condition, (b) Load voltage spectrum after compensation during unbalanced supply condition.

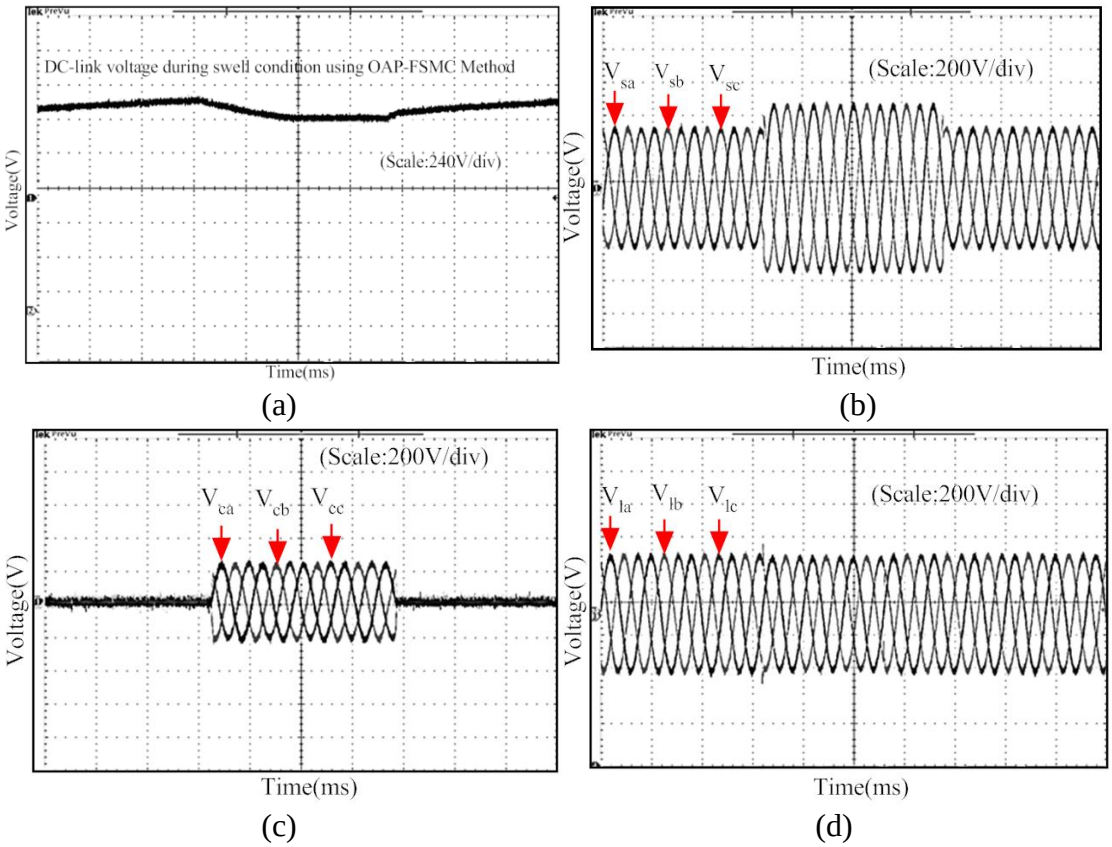


Fig.4.27 Real-time experimental results of series APF of UPQC, (a) DC-link voltage during swell condition, (b) Swell Voltage, (c) Swell compensation voltage, (d) Load voltage after compensation during swell condition.

Fig.4.30 (a) analyzes the DC-link voltage performance of proposed controller during steady and transient state condition of load and supply voltage. The transient condition involves with sudden load change at 0.15 s, supply voltage sag/swell and source voltage unbalance. During these transient conditions voltage across the dc-link capacitor deviates from its reference value. The magnitude of the dc-link voltage deviation depends on the size of a load connected, disconnected to the power distribution line and depth of sag/swell on the supply side. The DC-link voltage of proposed controller method for steady state load condition, transient load condition, voltage distortion condition, voltage sag/swell and supply voltage unbalance is shown in figure from top to bottom order. However, it is observed from the figure that the variations of DC-link voltage are quite satisfactory. The capacitor voltage is able to settle down within a minimum amount of time, both in initial and transient condition of load and supply voltage.

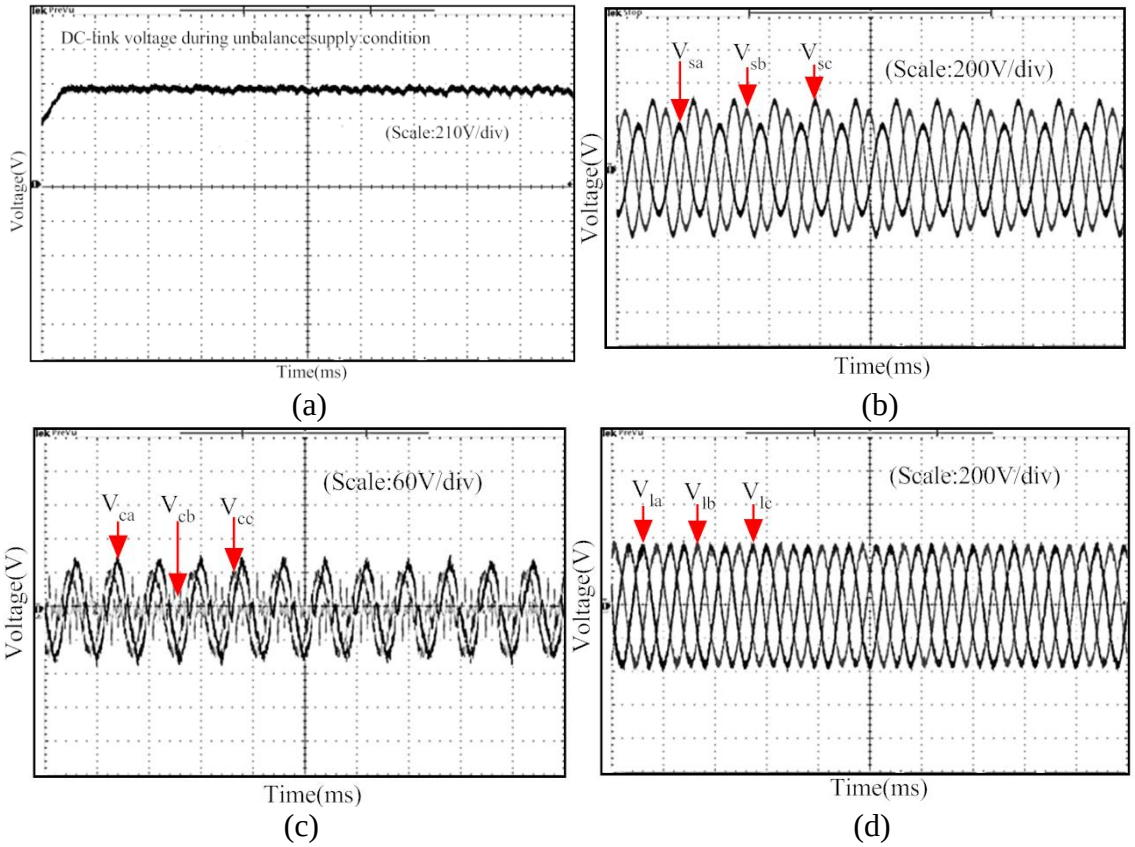


Fig.4.28 Real-time experimental results during unbalanced supply voltage condition, (a) DC-link voltage, (b) Source voltage, (c) Unbalanced compensation voltage, (d) Load voltage after compensation.

Table 4.3 Comparison of source current THD and load voltage THD

Type of condition	Before Compensation	Compensation with UPQC		
		NLSMC with modified SRF controller	ROT with NVGF hysteresis controller	OAP with FSMC-PWM control strategy
Source current THD during Steady-state condition	28.3 %	3.54 %	3.15 %	2.81 %
Source current THD during Transient-state condition	31.8 %	3.77 %	3.35 %	3.05 %
Load voltage THD during distorted supply condition	10.24 %	3.04 %	2.63 %	2.39 %

Moreover, in case of voltage swell and unbalanced supply voltage condition, 20 % of swell is considered here, occurring in the interval of $0.12\,s \le t \le 0.21\,s$ for four cycles of ac-mains. Similarly, voltage unbalance is created by considering $V_{sa} = 290\ V$, $V_{sb} = 360\ V$ and $V_{sc} = 410\ V$. Fig.4.30 (b) shows the simulation result of compensation effectiveness of proposed OAP-FSMC technique during swell and voltage unbalance condition. From the top to bottom, the waveforms observed are supply voltage, compensating voltage, load voltage of both swell and unbalanced supply voltage condition. Fig. 4.31 displays the THD spectrum of load voltage after compensation during swell and unbalanced supply condition and they are found to be 2.05 % and 2.38 % respectively. Table 4.4 gives the THD comparison of load voltage using ROT-NVGF and OAP-FSMC technique. From the table it is found that the OAP-FSMC strategy can effectively compensate the load voltage with less THD in comparison to the ROT-NVGF control technique.

Table 4.4 Comparison of load voltage THD during dynamic condition of supply voltage

Type of condition	Compensation with UPQC		
	NLSMC with modified SRF controller	ROT with NVGF hysteresis controller	OAP with FSMC-PWM control strategy
Load voltage THD after compensation during supply voltage sag condition	2.32 %	2.24 %	2.11 %
Load voltage THD after compensation during supply voltage swell condition	2.27%	2.18 %	2.05 %
Load voltage THD after compensation during supply voltage unbalance condition	2.71 %	2.52 %	2.38 %

Fig. 4.29 represents experimental results of voltage swell compensation capability of the proposed algorithm. Fig. 4.32 (a), (b), (c) and (d) show the DC-link voltage, supply voltage, compensating voltage and load voltage after compensation respectively. The series APF of the UPQC injects a proper voltage during voltage swell leading to a compensating load voltage. Fig.4.33 shows an experimental study of voltage unbalance compensation capability of the proposed algorithm. Fig.4.33 (a) shows the DC-link voltage during unbalanced supply

condition. Fig.4.33 (b) shows the waveforms of the three phase unbalanced voltages. Fig. 4.33 (c) and (d) depict compensation voltage and load voltage after compensation respectively. Series inverter of the UPQC injects the proper amount of compensating voltage for regulating the load voltage to its nominal value.

4.7 Chapter Summary

This chapter presents a novel approach for reference signal generation based on ROT method and OAP technique. The ROT based reference generation method utilizes EPLL for perfect extraction of positive sequence signal during power system perturbation and self-regulates the dc-link voltage by analyzing the peak amplitude of source current. It is observed from the both simulation and experimental results that the proposed approach improves many drawbacks of NVGF and NLSMC technique, such as delay in response time due to presence of LPF in dc-link loop and undesirable overshoot as well as undershoot occurred during transient condition.

It is also observed from the result that proposed NVGF hysteresis band controller provides variable-band with uniform switching frequency and less band violation in comparison to adaptive hysteresis controller. Thus, the proposed technique provides better tracking performance in all operating conditions of power system network and delivers smoother sinusoidal source current and voltage in comparison to the adaptive hysteresis controller. Thus, this technique reduces the band violation and provides excellent tracking performance in a wide range of power system dynamic condition.

The novel OAP based reference generation method utilizes EPLL for perfect extraction of positive sequence signal during power system perturbation and presents a novel fixed frequency based FSMC PWM control strategy for UPQC. These control strategies mainly compensates current and voltage harmonics, reactive power, voltage sag/swell and voltage distortions present in the supply voltage. The OAP and EPLL control structures added to the UPQC system quickly extract the reference signal from the supply voltage as well as self-regulate the dc-link capacitor voltage considering the peak amplitude of reference source current. Thus, the response time for controlling dc-link voltage can be significantly improved in comparison to the ROT based control strategy. Additionally the proposed FSMC based PWM technique provides higher tracking performance with lower switching

losses and eliminates the chattering problem associated with the sliding mode controller. From the experimental validation, it is clear that the proposed control strategy of UPQC is robust with excellent recovery feature to sudden load and supply voltage variation. The simulation and experimental results show that the proposed UPQC not only mitigates current harmonics correctly but also compensates voltage related problems such as voltage distortion, voltage sag/swell and voltage unbalance efficiently as compared to the ROT-NVGF method.

Chapter 5

High Performance UPQC using Command Generator Tracker (CGT) Based Direct Adaptive Control Strategy

5.1 Introduction

In the previous chapter, ROT based NVGF hysteresis controller and OAP based FSMC PWM controller of UPQC are discussed. Simulation and experimental results are also presented. ROT-NVGF and OAP-FSMC based UPQC control strategies are adaptive as well as robust and able to mitigate the PQ problems satisfactorily during all dynamic conditions of power system perturbation. However, performances of these controllers fail when there is a variation occurred either in the nonlinear load parameter or supply voltage parameter. Thus, UPQC may not be able to compensate PQ problems satisfactorily under those conditions.

Keeping above facts into consideration, this chapter proposes a particular control strategy of UPQC by employing command generator tracker (CGT) based direct adaptive control (DAC) [114] to eliminate PQ problems such as current harmonics, voltage sag/swell, voltage distortion and voltage unbalance present in the power distribution network. First, the command input signals (r_{abc}) are formulated with respect to three step-input signals, which are associated with three different step times for producing 120^0 phase shifted signal. Then, the command generator tracker (CGT) also known as model reference tracker (MRT) is designed by considering the reference model as an ideal oscillator. When three step-input signals having different step times are multiplied with the desired amplitude of source current and load voltage and fed into the reference model, then output would result in a desired sinusoidal reference signal. This provides a self-supporting dc-link voltage regulation by active power balancing system. In this system, the peak value of the reference current is responsible for proportionally changing of real power drawn from the supply. Therefore, any small variation of capacitor voltage gets regulated by the real power flowing through the shunt inverter into the dc-link capacitor and makes the dc-link voltage constant by keeping a power balance between AC and DC sides.

Finally, control law for UPQC is designed through appropriate adaptive gains, which are selected from the states of the CGT and tracking error. Therefore, asymptotic tracking is achieved by keeping the difference between true UPQC output and CGT output nearly zero. Thus, the states of the UPQC maintain desired trajectories in all operating conditions of the power system. These control inputs are applied to the triangular carrier pulse width modulator (PWM) controller for generation of required switching pulse for shunt and series APF of UPQC. Therefore, the proposed algorithm provides more robustness, flexibility and adaptability in all operating conditions of the power system over an OAP-FSMC technique. The performance of the proposed approach is validated through MATLAB/SIMULINK followed by the real-time experimental studies utilizing hardware-in-the-loop (HIL) system OPAL-RT simulator (OP5600). For analyzing current and voltage tracking performance of UPQC, a comparative assessment has been performed between proposed CGT-DAC approach and OAP-FSMC approach.

5.2 Structure of UPQC

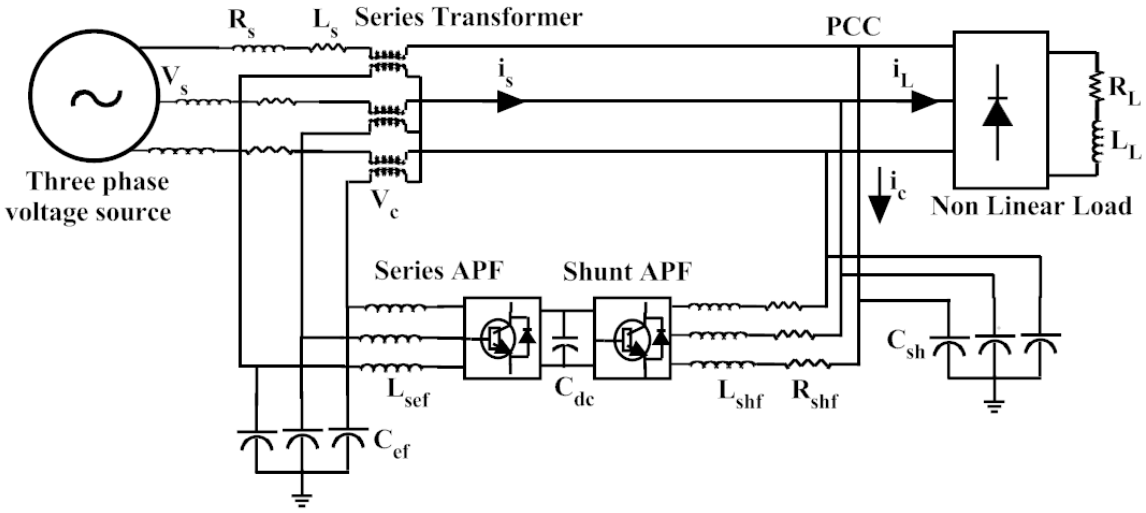


Fig.5.1 Structure of UPQC.

Fig. 5.1 shows the structure of a UPQC, which is an integration of two voltage source inverter (VSI) connected back to back through a common dc-link bus [70]. One VSI is connected in parallel with the load which behaves as a shunt inverter and another one is connected in series with the line demonstrated as a series inverter. The shunt inverter has the best capability for tackling current related problems; however the series inverter is most appropriate for voltage related problems. A three phase uncontrolled diode-bridge rectifier

with resistive R_L and inductive L_L load is used as a nonlinear load for producing current harmonics. Shunt interfacing inductor (L_{shf}) is utilized for coupling the shunt inverter to the system network and shunt capacitance C_{sh} connected across shunt inverter is utilized to remove the switching frequency components still remaining in the terminal voltage. The LC filter serves as a passive low-pass filter (LPF) to remove the high-frequency switching ripples present in the series inverter output voltage. The series transformer connected in series with the power line is utilized to establish a link between the series inverter and the system network.

5.3 Plant model for UPQC

The single phase equivalent representation of the UPQC in a power system distribution network is shown in Fig. 5.2. The LC filter connected to the series inverter is signified by L_{sef} and C_{ef}, whereas the resistance R_{sef} and R_{shf} represent as switching losses in the series and shunt inverter, respectively.

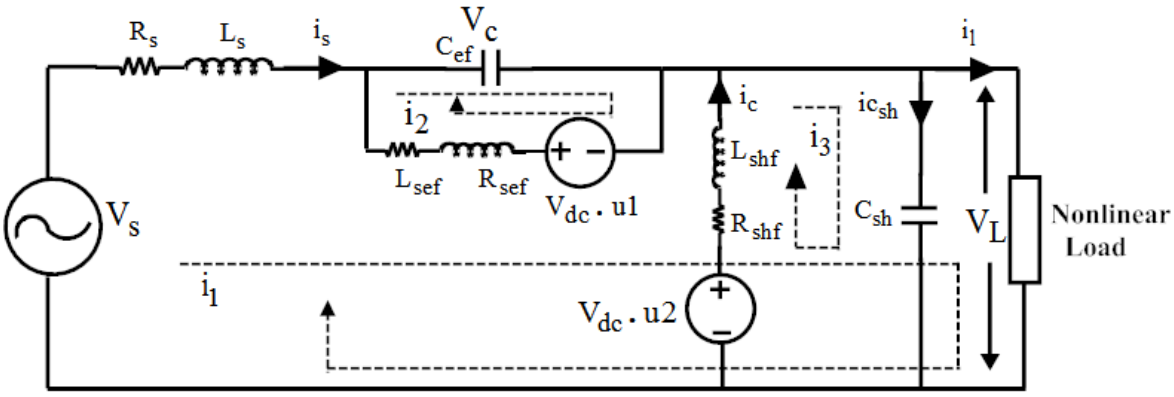


Fig.5.2. Single phase equivalent representation of UPQC.

Similarly, L_{shf} and C_{sh} are represented as coupling inductor and filter capacitor of shunt inverter respectively. The voltage across C_{sh} is denoted as V_L and voltage across C_{ef} is represented as V_C utilizing as a series injection voltage, whereas i_c represents as injection current for the shunt inverter. $V_{dc}.u1$ and $V_{dc}.u2$ denote as switching voltages across the series and shunt inverter output terminals of the UPQC respectively.

The state space model of the above system is analyzed with four state variables as three loop current and two capacitor voltage and can be represented as

$$x = \left[i_1, i_2, i_3, V_C, V_L \right]^T \tag{5.1}$$

The single-phase equivalent circuit model of UPQC consists of three forcing functions namely the source voltage V_S and switching variables u_1 as well as u_2. The control vector can be represented by

$$u = \left[u_1, u_2 \right]^T \tag{5.2}$$

By considering the state vector 'x_p', control vector 'u' and forcing functions 'V_S', the complete state-space equation becomes

$$\dot{x}_p = A_p x_p + B_1 u + B_2 V_S \tag{5.3}$$

In order to derive the state matrices A_p, B_1 and B_2, we apply the Kirchhoff's voltage and current laws to the three current loops specified in Fig.5.2.

From the current loop i_1, the state variable $\dot{i}_1$ becomes,

$$\dot{i}_1 = \frac{1}{L_{shf}} V_S - \frac{R_{shf}}{L_{shf}} i_1 - \frac{1}{L_{shf}} V_C - \frac{1}{L_{shf}} V_L \tag{5.4}$$

Similarly the state variables $\dot{i}_2$ and $\dot{i}_3$ are obtained from current loops i_2 and i_3. Also they are denoted by the following expressions.

$$\dot{i}_2 = \frac{V_{dc}}{L_{sef}} u_1 - \frac{R_{sef}}{L_{sef}} i_2 - \frac{1}{L_{sef}} V_C \tag{5.5}$$

$$\dot{i}_3 = \frac{V_{dc}}{L_{sef}} u_2 - \frac{R_{shf}}{L_{shf}} i_3 - \frac{1}{L_{shf}} V_L \tag{5.6}$$

The state variables for capacitor voltage C_{ef} and C_{sh} are given as

$$\dot{V}_C = \frac{1}{C_{ef}} (i_1 + i_2) \tag{5.7}$$

$$\dot{V}_{sh} = \dot{V}_L = \frac{1}{C_{sh}} \left(ic_{sh} \right) \tag{5.8}$$

By re-arranging the Eq. (5.4)-(5.7), the following matrix coefficients are obtained for the UPQC, which acts as a plant.

$$A_p=\begin{bmatrix} -\frac{R_{shf}}{L_{shf}} & 0 & 0 & -\frac{1}{L_{shf}} & -\frac{1}{L_{shf}} \\ 0 & -\frac{R_{sef}}{L_{sef}} & 0 & -\frac{1}{L_{sef}} & 0 \\ 0 & 0 & -\frac{R_{shf}}{L_{shf}} & 0 & -\frac{1}{L_{shf}} \\ \frac{1}{C_{ef}} & \frac{1}{C_{ef}} & 0 & 0 & 0 \\ \frac{1}{C_{sh}} & 0 & \frac{1}{C_{sh}} & 0 & 0 \end{bmatrix};\ B_1=\begin{bmatrix} 0 & 0 \\ \frac{V_{dc}}{L_{sef}} & 0 \\ 0 & \frac{V_{dc}}{L_{shf}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix};\ B_2=\begin{bmatrix} \frac{1}{L_{shf}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.9}$$

The output equation of the plant is given by the following expression.

$$y_p = C_p x_p + D_1 u + D_2 V_S \tag{5.10}$$

where

$$C_p=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix};D_1=\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix};\ D_2=\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

In the state space model, the supply voltage V_S is considered as exogenous input. The load voltage V_L and the source currents i_s are reflected as outputs of the plant and the variables u_1 and u_2 are the control inputs to the plant. Consequently, state variables can be represented in terms of the network parameters as follows.

$$\begin{cases} i_s = i_1 \\ i_{se} = i_2 \\ i_c = i_3 \\ V_{inj} = V_c \\ ic_{sh} = i_1 + i_3 - i_l \end{cases} \tag{5.11}$$

where i_{se} is the current flowing through R_{sef} and L_{sef}.

5.4. CONTROL DESIGN

In this section, two approaches normally CGT and DAC are considered. CGT is employed for reference signal generation and DAC for controlling the tracking performance between output of the plant $y_p = (i_s, V_l)^T$ and the reference signal $r_{(abc)} = (i_s^*, V_l^*)$. Further, this tracking error is utilized as a part of a set of evaluated equations of adaptive control law by adjusting the control gains. This adaptation rule progressively minimizes the error between plant output and CGT output. Therefore, this adaptive control law provides better tracking performance [115] throughout the load and supply side perturbations.

5.4.1 Construction of the CGT based reference generation

The design of CGT based reference control technique is based on attaining the output response of the plant (UPQC). As source current $\mathrm{i_s}$ and load voltage $\mathrm{V_L}$ are considered as the plant outputs, these signals are to be maintained as pure sinusoidal waves of nominal amplitude and frequency of power system network. Therefore, CGT reference model design specifications are incorporated in such a way that, when reference step-inputs are fed into the model, the CGT model behaves like an ideal oscillator and generates sinusoidal wave of frequency 50Hz with amplitude equivalent to peak value of source current and load voltage.

A linear time-invariant reference model can be defined for both shunt and series inverter of UPQC. The state space model for both shunt and series inverter can be defined as

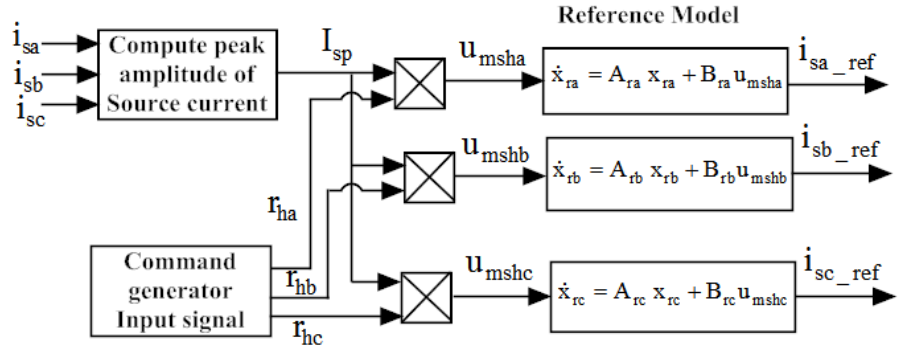
$$\begin{cases} \dot{x}_{r(abc)} = A_{r(abc)} x_{r(abc)} + B_{r(abc)} u_{msh(abc)} \\ y_{r(abc)} = C_{r(abc)} x_{r(abc)} \end{cases} \tag{5.12}$$

where $x_{r(abc)}$ is the $n_{r(abc)} \times 1$ model state vector, $u_{msh(abc)}$ and $u_{mse(abc)}$ are the $r \times 1$ model command inputs for shunt and series inverter reference model respectively, $y_{r(abc)}$ is the $r \times 1$ model output vector, $A_{r(abc)}, B_{r(abc)}$ and $C_{r(abc)}$ are the reference model system matrix and system output matrix. These matrices are defined as

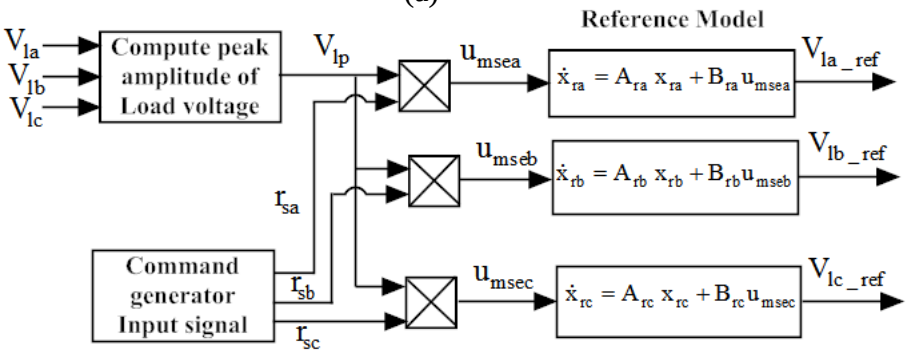
$$A_{r(abc)} = \begin{bmatrix} 0 & 1 \\ -\omega^2 & 0 \end{bmatrix}, B_{r(abc)} = [0;1], C_{r(a,b)} = [-315 \;\; 315] \text{ and } C_{rc} = [315 \;\; -315] \tag{5.13}$$

where $\omega = 2 \cdot \pi \cdot f$, f is the fundamental frequency.

Fig. 5.3 (a) and (b) show the CGT based reference signal generation model for both shunt and series inverter. This model consists of peak amplitude computation blocks, command generation input blocks and reference model blocks respectively. The computational block utilizes Eq. (5.14) and (5.15) for calculating the peak amplitude of source current (I_{sp}) and load voltage (V_{lp}) and these equations are defined as follows.



(a)



(b)

Fig.5.3 CGT based reference generation model (a) Reference signal generation for shunt APF, (b) Reference signal generation for series APF.

$$I_{sp} = \left(2/3(i_{sa}^2 + i_{sb}^2 + i_{sc}^2)\right)^{1/2} \tag{5.14}$$

$$V_{lp} = \left(2/3(V_{la}^2 + V_{lb}^2 + V_{lc}^2)\right)^{1/2} \tag{5.15}$$

Next three step-input signals as command reference input signal (r_{abc}) are applied to the model. Each step signal is associated with a different step time of $r_a = 0.01\,ms$, $r_b = 0.067\,ms$, $r_c = 0.035\,ms$, which result in 120^0 phase shifted reference signals at the reference model outputs. The command input signals for shunt inverter reference model and series inverter reference model are calculated by the following expressions.

$$u_{msh(abc)} = I_{sp} \times r_{h(abc)} \tag{5.16}$$

$$u_{mse(abc)} = V_{lp} \times r_{s(abc)} \tag{5.17}$$

When these command input signals are fed into the reference model, sinusoidal reference signal for shunt inverter ($i_{s(abc)\_ref}$) and series inverter (V_{la_ref}) are produced from output of the model.

5.4.2 Direct adaptive control algorithm

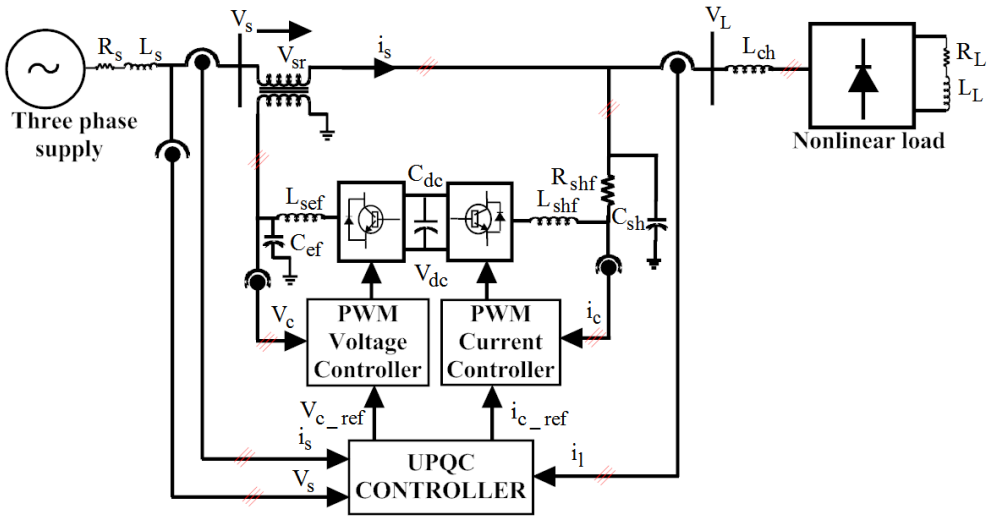


Fig.5.4 Overall control structure of the UPQC.

In this section, a single phase analysis of DAC technique is analyzed and this control methodology automatically finds the corrected gain and adjusts the control law effectively to minimize the tracking error between model $(y_{r(sh-se)})$ and plant (y_p) outputs. Thus, the tracking error is defined as

$$e_{r(sh-se)} = y_{r(sh-se)} - y_p \tag{5.18}$$

The overall control structure of UPQC is shown in Fig.5.4. The DAC control algorithm block is utilized for computing the adaptive control law so that the tracking error $e_{r(sh-se)}$ of both shunt and series inverter are approached to zero. To achieve this control objective, the adaptive control law is chosen according to the CGT control law [116] and this control law is defined as follows.

$$U_{p(sh-se)} = k_{x(sh-se)} x_r + k_{u(sh-se)} u_{m(sh-se)} + k_{e(sh-se)} [y_{r(sh-se)} - y_p] \tag{5.19}$$

where $U_{p(sh-se)}$ is the control law, $u_{m(sh-se)}$ is the step input signal, $k_{x(sh-se)}$, $k_{u(sh-se)}$ as well as $k_{e(sh-se)}$ are the adaptive gains of both shunt and series inverter.

The state vector x_r is computed from Eq. (5.12) and is defined below.

$$x_r = \frac{y_r}{C_r} \tag{5.20}$$

To rearrange the calculations given below, the adaptive gains are concatenated into the $m \times n_r$ matrix $k_{r(sh-se)}$, which is characterized as follows.

$$k_{r(sh-se)} = \left\{ k_{e(sh-se)}\, k_{x(sh-se)}\, k_{u(sh-se)} \right\} \tag{5.21}$$

Similarly, if the states vectors are set into appropriate places in the $n_r \times 1$ vector form, then the corresponding vector $s(t)$ is defined as follows.

$$s(t) = \begin{bmatrix} e_{r(sh-se)} \\ x_r \\ u_{m(sh-se)} \end{bmatrix} = \begin{bmatrix} (y_{r(sh-se)} - y_p) \\ x_r \\ u_{m(sh-se)} \end{bmatrix} \tag{5.22}$$

Then

$$U_{p(sh-se)} = k_{r(sh-se)}\, s(t) \tag{5.23}$$

The concatenated gain $k_{r(sh-se)}$ defined above is equivalent to the sum of a proportional gain $k_{p(sh-se)}$ and integral gain $k_{I(sh-se)}$, which is defined as follows.

$$k_{r(sh-se)} = k_{p(sh-se)} + k_{I(sh-se)} \tag{5.24}$$

However, the proportional gain and integral gain are defined as below.

$$k_{p(sh-se)} = v(t)\, s^T(t)\, T_1 \tag{5.25}$$

$$\dot{k}_{I(sh-se)} = v(t)\, s^T(t)\, T_2 \tag{5.26}$$

where

$$v(t) = C_p\, e_{r(sh-se)} = (y_{r(sh-se)} - y_p) \tag{5.27}$$

and T_1, T_2 are $n_r \times n_r$ time-invariant weight matrices. Selection of these weight matrices is considered according to the sufficient conditions for stability [35] and these matrices are given as

$$T_1 = 0.00025, \qquad T_2 = \begin{bmatrix} 0.0001 & 0 & 0 \\ 0 & 0.0001 & 0 \\ 0 & 0 & 0.0001 \end{bmatrix}$$

5.5 Simulation result

To validate the performance of the proposed control algorithm, a comprehensive simulation study is accomplished in the MATLAB/SIMULINK environment. The simulated test system data are given in Appendix-1. Performance of the proposed CGT-DAC algorithm is simulated and compared with the OAP-FSMC strategy. Simulation studies of steady-state and dynamic conditions for both load as well as source sides are performed and discussed in the following.

A. Case 1: Performance comparison of dc-link voltage during steady and dynamic state condition.

Case-1 analyzes the DC-link voltage performance comparison of both OAP-FSMC and proposed CGT-DAC controller during steady-state and transient-state condition. In this comparison, the time required for stable operation is analyzed. The dynamic condition involves with sudden load change at 0.15s, voltage sag/swell and source voltage unbalance. During these dynamic conditions voltage across the dc-link capacitor deviates from its reference value. The magnitude of the dc-link voltage deviation depends on the size of a load connected, disconnected to the power distribution line and depth of sag/swell on the supply side. The DC-link voltage stability condition for OAP-FSMC method is shown in Fig.4.31 (a) (chapter-4). Similarly, the waveforms for steady-state and transient-state load conditions in CGT-DAC method are shown in Fig.5.5 (a), where voltage distortion, voltage sag/swell and supply voltage unbalance are represented from top to bottom order. It is perceived from the Fig. 4.31 (a) that during steady-state condition of load, the OAP-FSMC method takes 0.018s for stabilizing the dc-link voltage at the initial stage. But when the load changes from $R_L = 42\ \Omega$, $L_L = 35$ mH to $R_L = 34\ \Omega$, $L_L = 28$ mH with a step change of

0.15 s to 0.3 s, it nearly takes 0.05 s to reach its steady state value. Similarly, during voltage distortion condition the OAP-FSMC method takes 0.016 s for stabilizing the dc-link voltage at the initial stage and also contains some ripples in dc-link voltage. During sag/swell conditions, the dc-link voltage falls to 560 V and 580 V respectively at 0.13 s from its reference value and takes 0.09 s and 0.08 s for stabilization. In case of the unbalanced supply voltage condition, OAP-FSMC method takes 0.018 s for stabilizing the dc-link voltage and further some ripples are observed in DC-link voltage. However, in case of proposed CGT-DAC method, DC-link voltage stabilizes within 0.011 s at the initial stage and in the transient condition, it takes about 0.02 s to reach its steady state. Additionally, the steady state ripples in DC-link voltage are negligible. Thus, it helps in reduction of steady state distortion in source current. Similarly, during voltage distortion condition, the proposed CGT-DAC method takes 0.012 s for stabilizing the dc-link voltage at the initial stage and also the steady state ripples in DC-link voltage are small. When sag and swell occur in the supply side, DC-link voltage falls to 590 V and 610 V respectively at 0.13 s and takes about 0.05 s and 0.04 s to become stable. In unbalanced case, the proposed method takes 0.013 s for stabilizing the dc-link voltage at the initial stage and it doesn't deviate from its original position and always follows the reference value. Thus, the proposed CGT-DAC method enhances the performance of UPQC to a large extent. Table 5.1 gives a comparative study of the DC-link performance for OAP-FSMC and CGT-DAC method.

B. Case 2: Tracking Performance during dynamic Load and supply condition

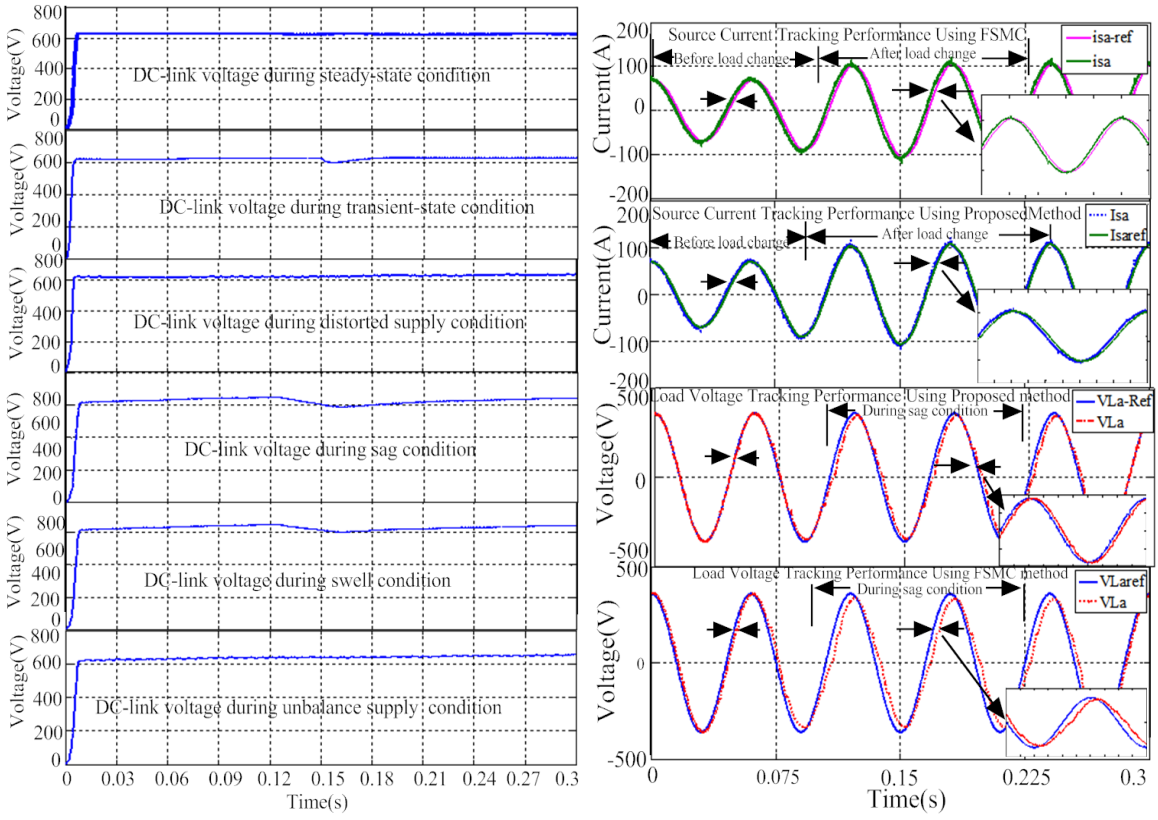
In this case, tracking performance of proposed control strategy is compared with the OAP-FSMC method, which is utilized in inner loop for current tracking performance in shunt APF and voltage tracking performance in series APF. Fig.5.5 (b) shows the current and voltage tracking performance of OAP-FSMC method and the proposed method during dynamic load condition and source voltage sag condition in a top to bottom order.

For current tracking performance in case of OAP-FSMC method, the tracking time delay is 0.003s before load changing condition, whereas it is increased to 0.008s when the load changes with a step change of 0.15 s to 0.3 s. In case of proposed one, tracking time delay is almost 0.001s before load changing condition and 0.003s after load changing condition. For voltage tracking performance in case of OAP-FSMC method, the tracking time delay before sag condition is almost 0.003 s, whereas it is increased to 0.012 s during sag condition. In

case of proposed CGT-DAC method, the tracking time delay before sag condition is 0.003 s, whereas it is increased to 0.006 s during sag condition. Table 5.2 summarizes the comparison of tracking performance of both OAP-FSMC method and the proposed CGT-DAC method.

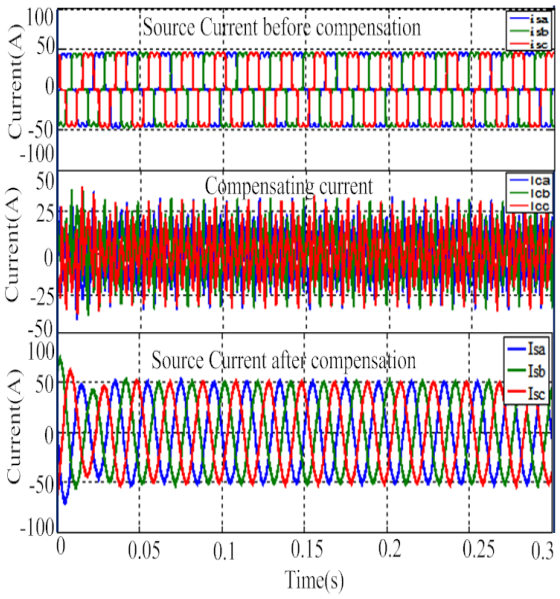
C. Case 3: Overall performance of UPQC

The overall performance of the UPQC in both steady and dynamic condition of load and supply voltage is demonstrated here. The performances of shunt APF during steady-state and dynamic condition are shown in Fig.5.5 (c) and (d).

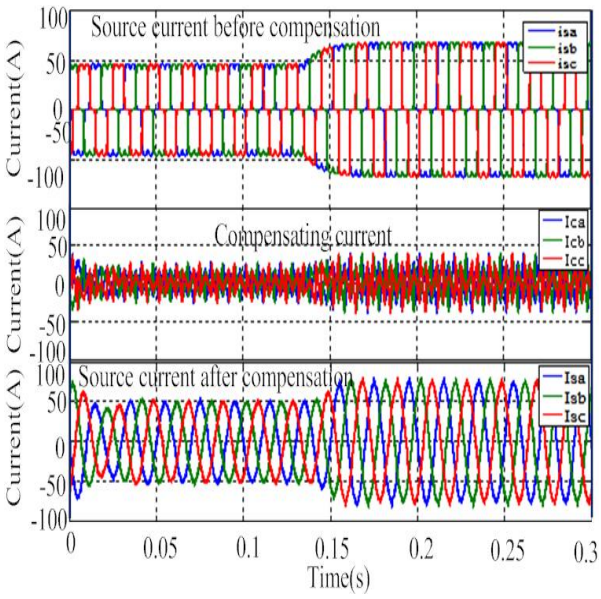


(a) (b)

Fig.5.5 Simulation results for operating performance of the UPQC system, (a) Performance comparison of DC-link voltage using PI-controller and CGT-DAC method, (b) Tracking Performance comparison of PI-controller and CGT-DAC method, (c) Performance of the shunt APF of the UPQC during steady state condition, (d) Performance of the shunt APF of the UPQC during load dynamic condition, (e) Performance of series converter of UPQC during sag/swell condition using CGT-DAC method, (f) Performance of series converter of UPQC during distorted and unbalanced supply condition using CGT-DAC method.



(c)



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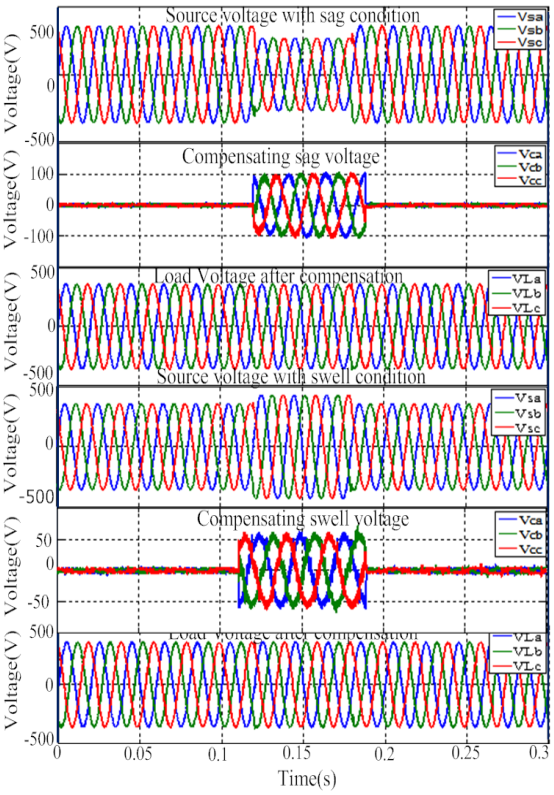
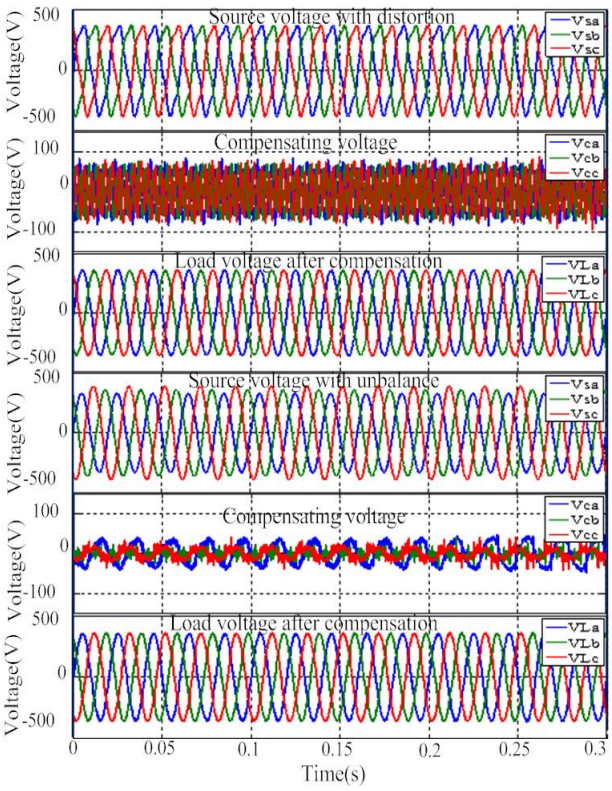


(e)



(f)

Fig.5.5 Simulation results for operating performance of the UPQC system (Continued)

Table 5.1 Comparison of the OAP-FSMC and CGT-DAC for DC-link voltage control performance

Type of conditions	OAP-FSMC method	CGT-DAC method
Time required for stabilization at initial stage during steady-state and transient-state condition	0.018 s	0.011 s
Time required for stabilization at initial stage during voltage distorted and unbalanced supply condition	0.016 s and 0.018 s	0.012s and 0.013 s
Time required for stabilization at load dynamic	0.05 s	0.02 s
Time required for stabilization at sag condition	0.09 s	0.05 s
Time required for stabilization at swell condition	0.08 s	0.04 s

Table 5.2 Tracking performance comparison of both OAP-FSMC and CGT-DAC method.

Conditions	OAP-FSMC method		CGT-DAC method	
	Before load change or before sag condition	After load change or during sag condition	Before load change or before sag condition	After Load change or during sag condition
Tracking time-delay of shunt APF	0.003 s	0.008 s	0.001 s	0.003 s
Tracking time-delay of series APF	0.003 s	0.012 s	0.003 s	0.006 s

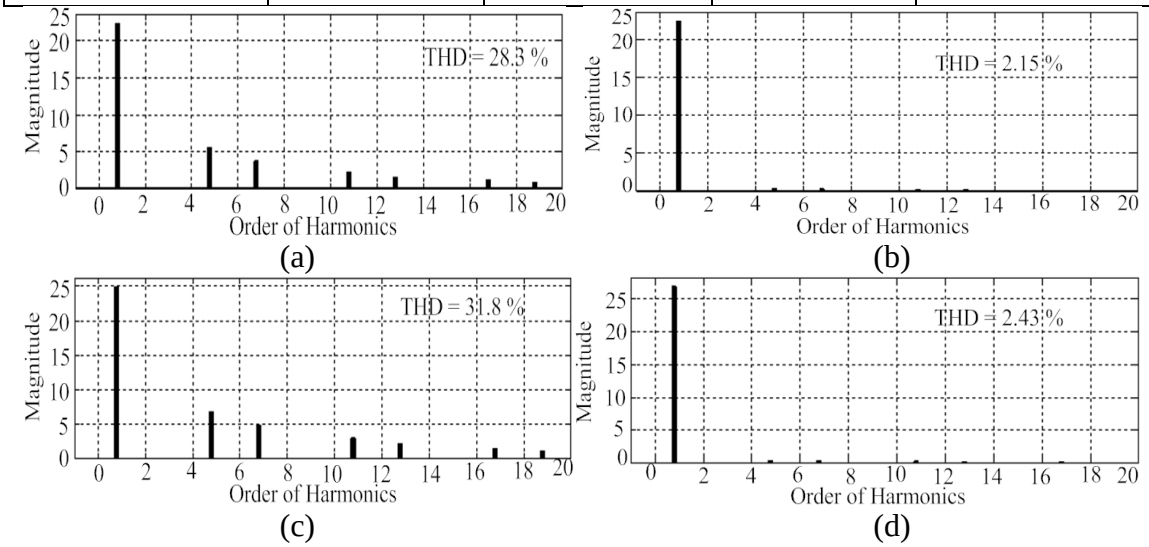


Fig.5.6 Current harmonics spectrum before and after compensation, (a) Source current spectrum before compensation during steady-state condition, (b) Source current spectrum after compensation during steady-state condition (c) Source current spectrum before compensation during transient-state condition, (d) Source current spectrum after compensation during transient-state condition.

From top to bottom, the waveforms observed are source current before compensation, compensating current, and source current after compensation using proposed CGT-DAC method. From the figure, it is observed that during steady-state and dynamic load conditions, proposed CGT-DAC method provides better reduction of harmonics from source current and makes the source current more sinusoidal as compared to the OAP-FSMC method. Fig.5.6 (a) and (b) convey the information regarding the THD for source current before and after compensation during steady-state condition. Similarly, Fig.5.6 (c) and (d) provide the information about the THD for source current before and after compensation under transient-state condition. Table 5.3 lists the THD of source current before and after compensation using OAP-FSMC method and CGT-DAC method. It indicates that THD of the source current of OAP-FSMC method during steady-state and transient-state condition are found to be 2.81 % and 3.05 % respectively, whereas in case of proposed CGT-DAC method, they are reduced to 2.15 % and 2.43 % respectively.

Fig.5.5 (e) shows the sag/swell voltage compensation performance, where the series converter is utilized to compensate the load voltage around its nominal value by proper injection of compensating voltage through series transformer. Fig.5.5 (f) shows the compensation performance of series converter of UPQC for compensating harmonics in distorted supply voltage and unbalanced supply voltage. It is clear that, the proposed control strategy satisfactorily eliminates all distortions and unbalances present in the source voltage by injecting proper compensation voltage and makes the load voltage free from all such disturbances, which confirms the superiority of the proposed control strategy.

Figs. 5.7 (a) and (b) display the THD spectrum of load voltage after compensation during sag and swell condition, and they are found to be 1.98 % and 1.88 %. Table 5.4 gives the THD comparison of load voltage during sag and swell condition using OAP-FSMC technique and CGT-DAC technique. From the Table it is found that the CGT-DAC strategy can effectively compensate the load voltage with less THD in comparison to the OAP-FSMC technique.

Fig.5.7 (c) and (d) illustrate the THD spectrum of load voltage before and after compensation during supply voltage distortion condition and they are observed to be 10.24 % and 2.25 % respectively. Table 5.4 gives the THD analysis of both OAP-FSMC method and CGT-DAC method. From the table, it is clear that, the proposed CGT-DAC strategy can

satisfactorily eliminate all the distortions present in the source voltage by injecting proper compensation voltage and makes the load voltage free from all such disturbances, which confirms the superiority of the proposed CGT-DAC strategy over OAP-FSMC strategy.

Fig. 5.7 (e) displays the THD spectrum of load voltage after compensation during unbalanced supply condition and it is found to be 2.07 %. Table 5.4 gives the THD comparison of load voltage using OAP-FSMC technique and CGT-DAC technique. From the table it is found that the proposed CGT-DAC strategy can effectively compensate the load voltage with less THD in comparison to the OAP-FSMC technique.

5.6. Experimental validation using the real time HIL system

The real time experimental verifications for shunt inverter of UPQC by utilizing the proposed CGT-DAC technique are depicted in Fig. 5.8. The experimentation has been accomplished at switching frequency of 10 kHz. Fig. 5.8 (a), (b), (c) depict the steady-state performance of source current before compensation, compensating current and source current after compensation respectively.

Table. 5.3 Comparison of source current THD.

Type of condition	Before Compensation	Compensation with UPQC	
		OAP-FSMC method	CGT-DAC method
Source current THD in steady-state condition	31.6 %	2.81 %	2.15 %
Source current THD in transient-state condition	31.6 %	3.05 %	2.43 %

Table 5.4. Comparison of load voltage THD during dynamic condition of supply voltage

Type of condition	Compensation with UPQC	
	OAP-FSMC method	CGT-DAC method
Load voltage THD after compensation during supply voltage sag condition	2.11 %	1.98 %
Load voltage THD after compensation during supply voltage swell condition	2.05 %	1.88 %
Load voltage THD during distorted supply condition (THD 10.24%)	2.39 %	2.25 %
Load voltage THD after compensation during supply voltage unbalance condition	2.38 %	2.07 %

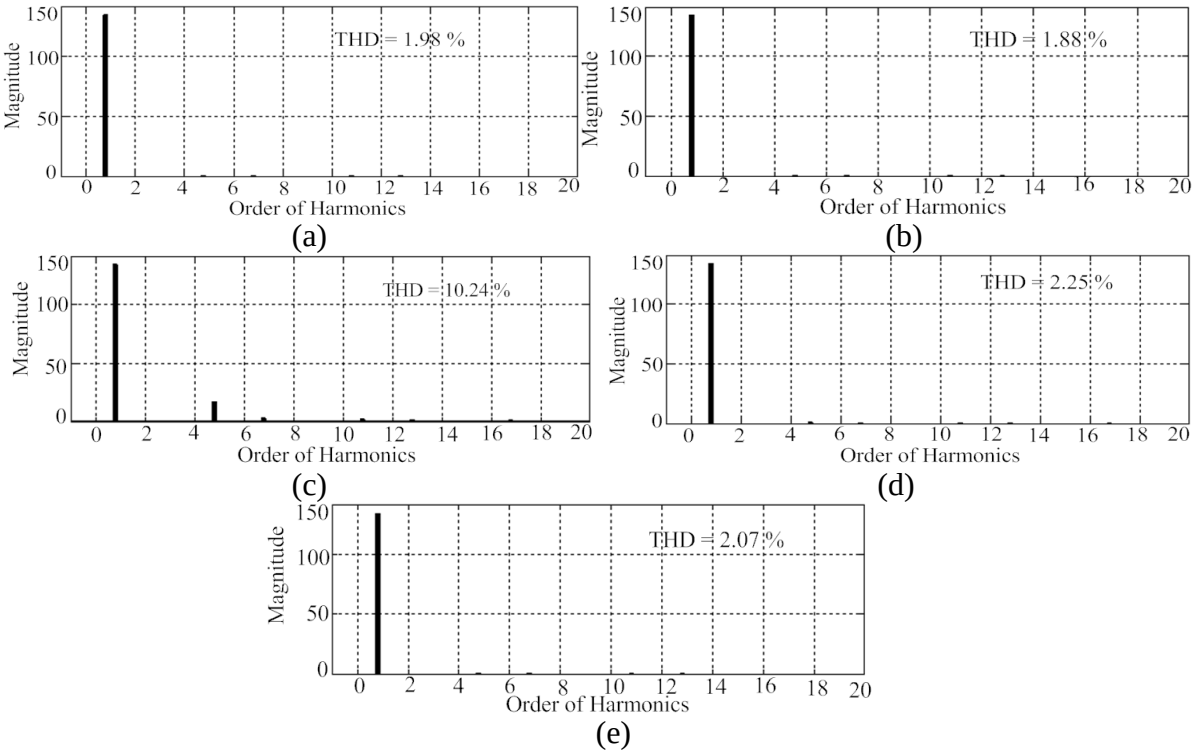


Fig. 5.7 Voltage sag/swell, voltage distortion and supply voltage unbalance compensation spectrum, (a) Load voltage spectrum after compensation during voltage sag condition, (b) Load voltage spectrum after compensation during voltage swell condition, (c) Distorted supply voltage spectrum, (d) Load voltage spectrum after compensation, (e) Load voltage spectrum after compensation during unbalanced supply condition.

Fig. 5.8 (d) shows the source current before compensation under transient state condition with a step change of load at t= 0.15 s. Fig. 5.8 (e) and (f) provide the information about compensating current and source current after compensation respectively and it is observed that proposed controller effectively eliminates all harmonics from source current and makes the source current sinusoidal. Fig. 5.9 shows the voltage sag/swell compensation capability of the proposed CGT-DAC method. For this reason, 30 % of voltage sag has been considered for the grid voltage for a period of three cycles. Fig.5.9 (a), (b) and (c) show the experimental results of supply voltage (V_S), compensating voltage (V_C) and load voltage (V_L) respectively. The series inverter of the UPQC injects a proper voltage during voltage sag leading to a compensating load voltage. Fig. 5.9 (d), (e) and (f) represent experimental results of voltage swell compensation capability of the proposed CGT-DAC algorithm. In this case, 20 % of voltage swell for a time interval of three cycles has been applied to the grid. Fig.5.10 shows the experimental result of distortion voltage compensation capability of the proposed

algorithm. In this case, 2 % of the 5th and 1 % of 7th harmonic voltage have been mixed with the grid voltage to create distortion voltage. The series inverter of UPQC acts as a series-type distortion voltage compensator to filter out all distortions present in the supply voltage and provides quality voltage to the load.

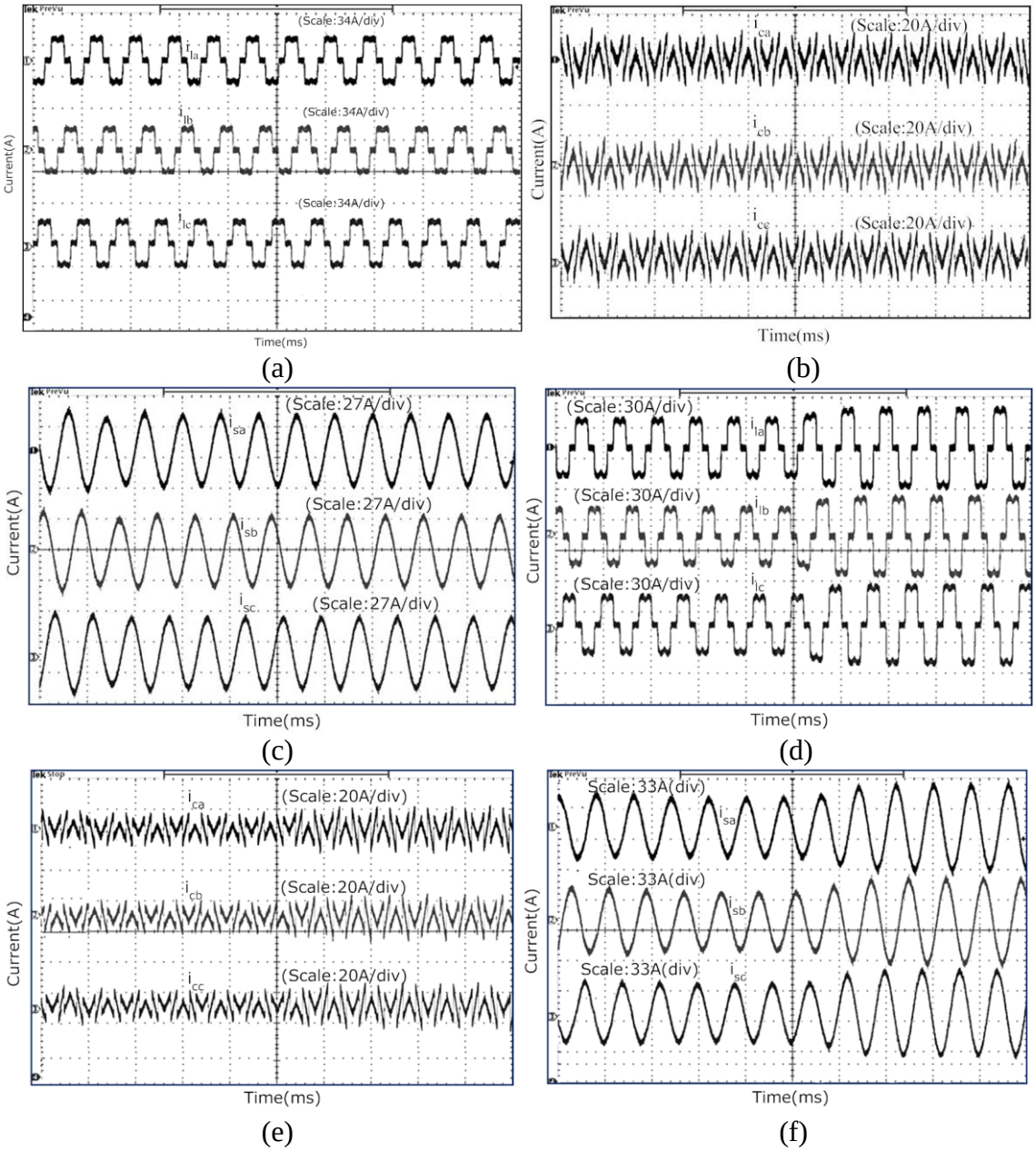


Fig.5.8 Real-time experimental results of proposed CGT-DAC method, (a) Source current before compensation under steady-state, (b) Compensation current under steady-state, (c) Source current after compensation under steady-state, (d) Source current before compensation under load dynamic condition, (e) Compensation current under load dynamic condition, (f) Source current after compensation under load dynamic condition.

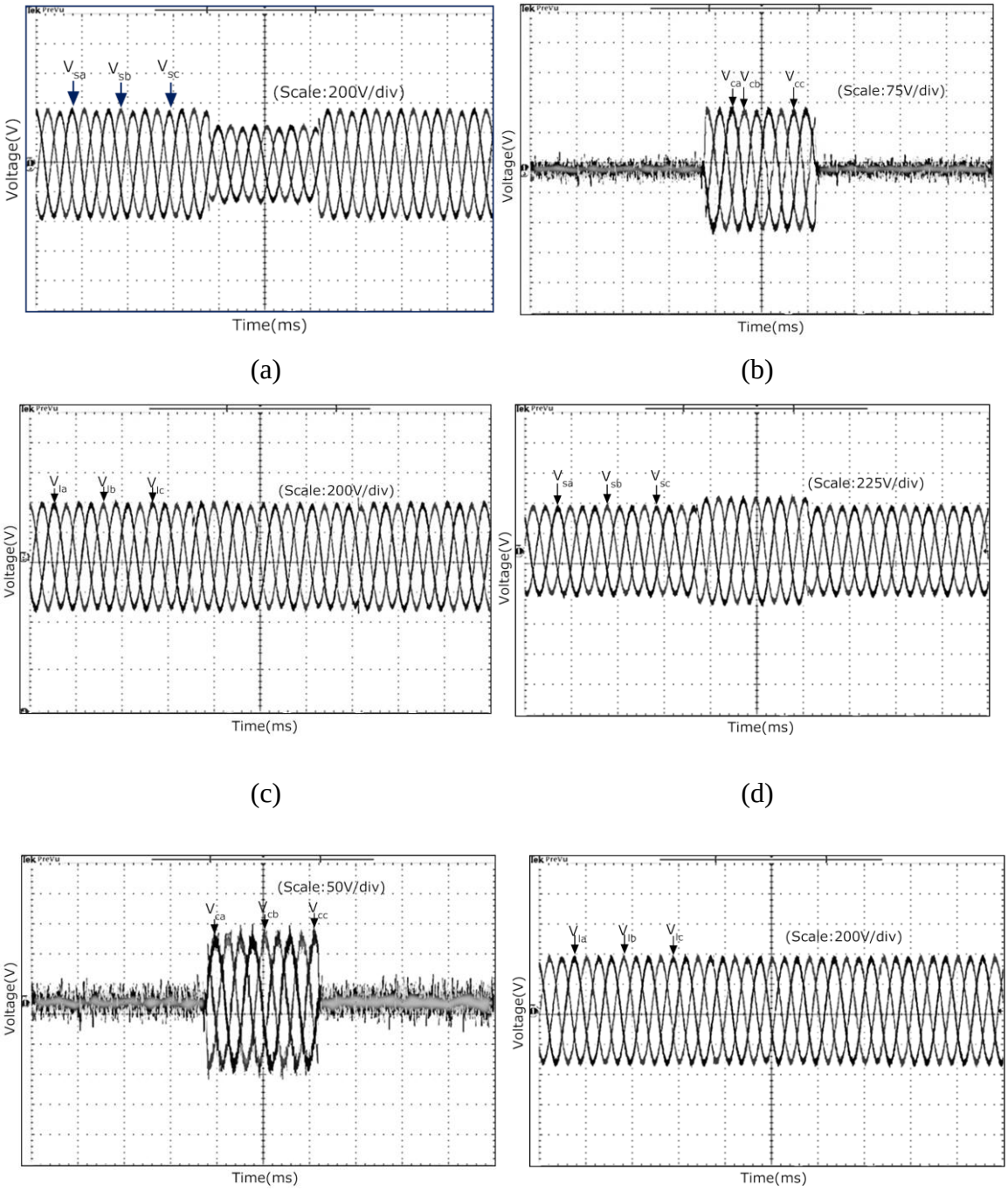


Fig.5.9 Real-time experimental results under sag/swell condition with proposed CGT-DAC method, (a) Source voltage with sag, (b) Sag compensation voltage, (c) Load voltage after sag compensation, (d) Source voltage with swell, (e) Swell compensation voltage, (f) Load voltage after swell compensation.

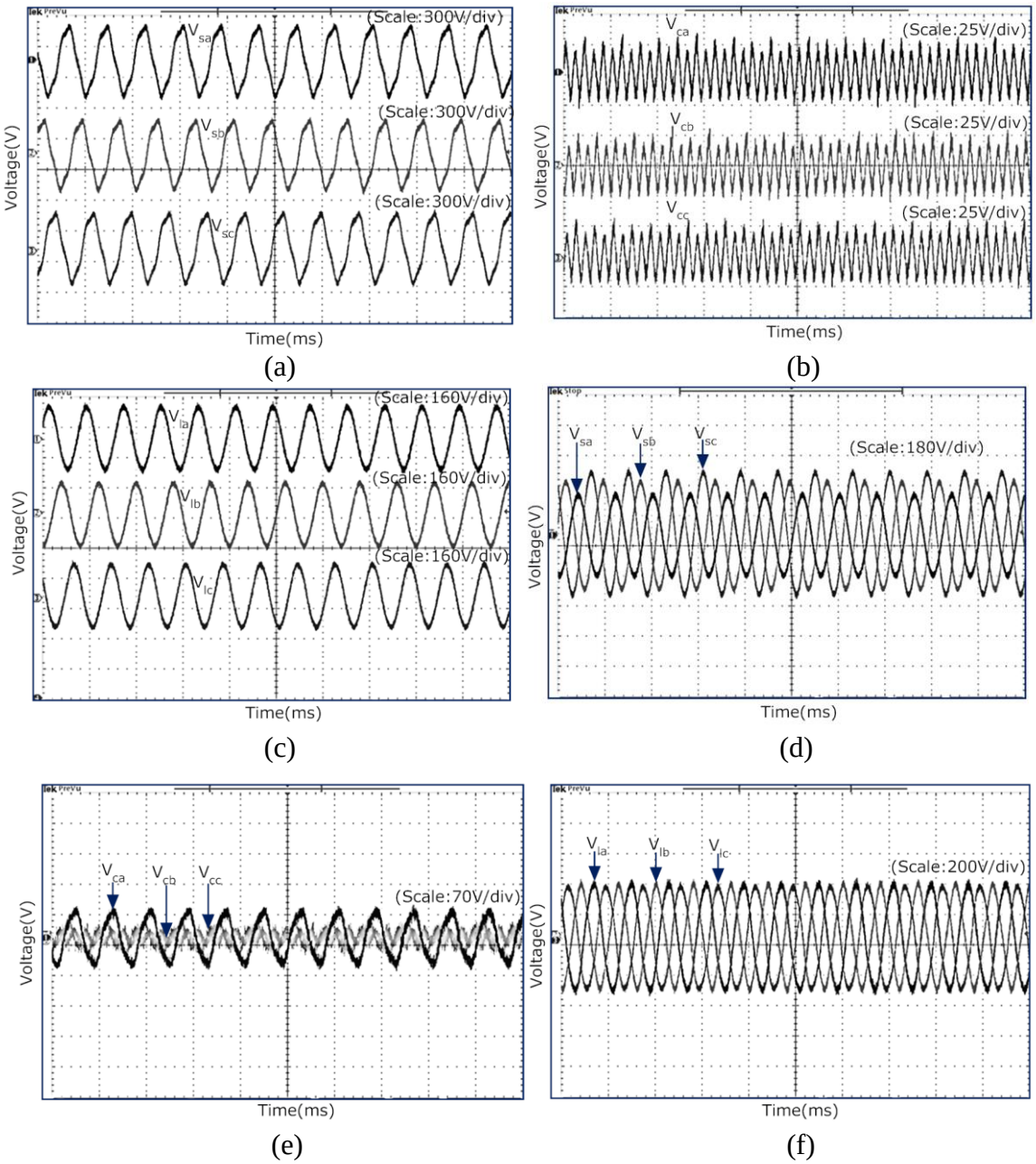


Fig.5.10 Real-time experimental results under voltage distortion and unbalance condition, (a) Source voltage with distortion, (b) Distortion compensation voltage, (c) Load voltage after distortion compensation, (d) Source voltage with unbalance, (e) Unbalance compensation voltage, (f) Load voltage after unbalance compensation.

Fig.5.10 (a), (b) and (c) show the experimental results of supply voltage under distortion condition, compensating voltage and load voltage respectively. From the figure, it is observed that the load voltage waveforms $V_{La,}V_{Lb}$ and V_{Lc} are sinusoidal. This is confirmed

that by utilizing the proposed CGT-DAC algorithm, series inverter of UPQC compensates the source voltage distortion effectively. Fig.5.10 (d), (e), and (f) show an experimental study of voltage unbalance compensation capability of the proposed CGT-DAC algorithm. Fig.5.10 (d) shows the waveforms of the three phase unbalanced voltages. In this study, voltage unbalance is created by considering three different amplitudes such as $V_{Sa} = 280\ V$, $V_{sb} = 360\ V$ and $V_{sc} = 400\ V$. Fig. 5.10 (e) and (f) depict compensation voltage and load voltage respectively. Series inverter of the UPQC injects the proper amount of compensating voltage for regulating the load voltage to its nominal value.

5.7. Chapter Summary

In this chapter, a novel CGT based model reference approach for reference signal generation and DAC method for reduction of tracking error between plant output and model output have been presented for the control of a UPQC. The CGT based reference generation method can self-regulate the dc-link voltage by considering the peak amplitude of source current and minimizes the effects of dc-link voltage deviation during load and source dynamic condition. This approach improves several feature of OAP-FSMC method, such as delay in response time and undesirable overshoot as well as undershoot occurred during the transient condition.

The proposed DAC method adaptively changes the control gain according to the wide range of power system dynamic condition. As a result, it provides better tracking performance in all operating conditions of the power system network and delivers smoother sinusoidal source current and voltage in comparison to the OAP-FSMC method. This adaptive performance of the UPQC is first verified through the simulation studies. Experimental studies on the HIL system with the OPAL-RT platform are then carried out to validate its real-time implementation. The compensation capability of the UPQC for harmonics in the load voltage and supply current, voltage sags/swell and voltage unbalance is accomplished successfully.

Chapter 6

Model Reference Robust Adaptive Control (MRRAC) based Experimental Prototype set-up for UPQC

6.1 Introduction

In the previous chapters, several novel control strategies of three-phase three-wire UPQC system are discussed and simulation and experimental results are also presented. It is concluded that all proposed control techniques efficiently eliminate the PQ problems such as current harmonics, voltage distortion, voltage sag/swell and unbalanced supply voltage presented in the power system distribution network. However, all these control strategies discussed are mainly utilized in three phase three wire industrial and commercial nonlinear loads such as three phase variable speed drives, uninterruptable power supply (UPS), three phase rectifiers, arc furnaces, magnetic cores and resistance arc welders. However, a significant portion of nonlinear loads used in the domestic and service industries are single phase loads. These nonlinear loads such as personal computers, printers, copiers, and fax machines are finding their way into nearly every desk. In these loads, an AC system is usually connected to a low cost single-phase rectifier with a capacitor filter on DC side. The current drawn by this type of load is discontinuous because the capacitor only draws current for short period of time. Therefore source current is distorted normally over 70% [117] that results in failure or missed operation in all of these equipments.

To overcome the aforesaid single phase PQ issues, this chapter discusses about the single phase UPQC system by developing a prototype experimental set-up for testing robustness of the proposed model reference robust adaptive control (MRRAC). The objective of this experimental set-up is to demonstrate the working of a single phase UPQC system by compensating numerous PQ problems such as current harmonics, and voltage sag/swell. The performance capability of UPQC to compensate these PQ problems depends upon the accuracy of control strategy. Recently, significant attention has been paid to the control circuit designs of the UPQC, with objective to obtain reliable control algorithms and fast response techniques so that the UPQC can simultaneously tackle most of the PQ problems in the power distribution system.

In most of the UPQC systems, a fixed conventional controller like proportional plus integral (PI) controller [118] is employed in inner and outer control loop for PQ compensation. When the power system parameter is not estimated precisely, the design of PI gains fails to resist the power system perturbation and hence shows low stability and robustness [119,120]. Further, these controllers provide low robust competence when the UPQC encounters to multiple challenges of the operating environment of a power system network such as load transient, supply side transient and so on.

To overcome the aforementioned problems of PI-controlled UPQC, this chapter utilizes MRRAC [121]. Moreover, the adaptive control law is designed to track a linear reference model to reduce the tracking error between model reference output signal and UPQC output signal to be controlled. Additionally, this proposed MRRAC algorithm adaptively regulates the DC-link capacitor voltage without utilizing additional controller. As a result, the proposed algorithm provides more robustness, flexibility and adaptability in all operating conditions of the power system over a conventional PI controller. The proposed control strategy of UPQC is implemented through MATLAB/SIMULINK followed by the experimental validation by using prototype experimental set-up with LABVIEW cRIO-9014 and adequate results are reported after a comparative assessment with the conventional PI-controller.

6.2 Description of an experimental prototype Set-up for UPQC

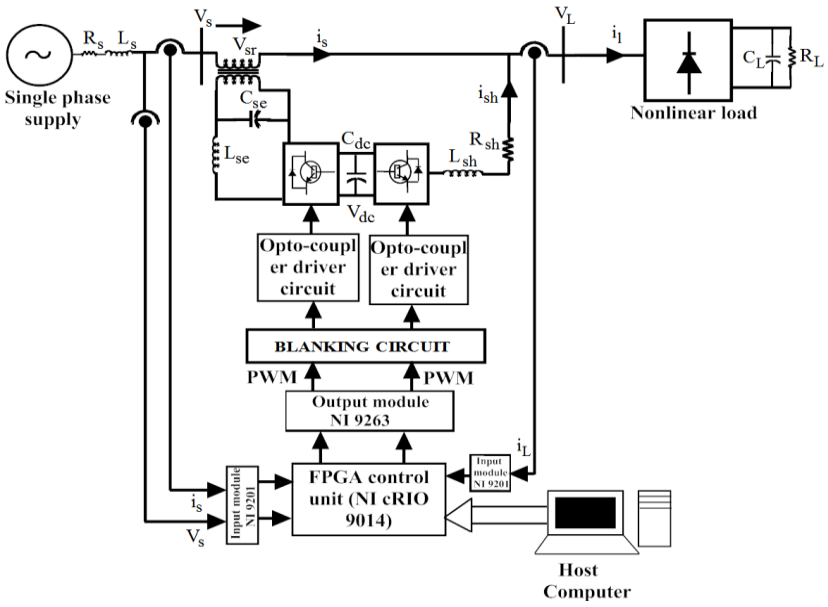


Fig. 6.1 Block Diagram of the Experimental Set-up

The basic topology of a single phase experimental set-up of UPQC developed in the laboratory is shown in Fig. 6.1. This topology is composed of a single-phase supply, a UPQC and a nonlinear load. The shunt APF and series APF of the UPQC are developed with four insulated-gate bipolar transistor (IGBT) modules SKM75GB063D. A nonlinear load comprising a single phase diode bridge rectifier with RC load is considered. The control of UPQC is achieved by MRRAC controller based algorithm implemented in LABVIEW NI cRIO-9014. The interface between LABVIEW and NI cRIO-9014 facilitates running the control algorithm. The NI cRIO-9014 combined with input and output (I/O) panels (NI 9201 and NI 9263) provides an interface between the NI cRIO-9014 and the host computer. All computational tasks are processed by the cRIO-9014 controller module which is connected to the host PC where all possible controls are handled. The switching signals generated from the output port of NI 9263 connector panel are fed to blanking circuit and opto-isolation driver circuit, which finally provide gate pulses for the single-phase insulated IGBT bridge, where the PWM frequency is set to 10 kHZ. The dead time for each leg of IGBT is set to 4 µs. The source current i_s and load current i_l are sensed using Hall effect current sensors and then fed to the input module of NI 9201 panel after passing through signal conditioning circuit. Similarly, source voltage is sensed through voltage sensors and fed to the input module. A photograph of the experimental setup is shown in Fig. 6.2. This experimental setup is composed of the following items.

- Control Platform:
  - FPGA control unit-NI cRIO-9014
  - Input and Output module NI 9201 and NI 9263
- Single-phase IGBT based inverter with following specifications:
  - IGBT module: SKM75GB063D (4 nos)
  - Opto-coupler drivers circuit: TLP-250 (8 nos)
  - DC-link: 4700 µF/400 V (2 nos)
  - Input DC voltage: 220 V

- Output AC voltage: 100 V
- Output Current: 5A max
- Output Frequency: 50 Hz
- Switching Frequency: 10 kHz max

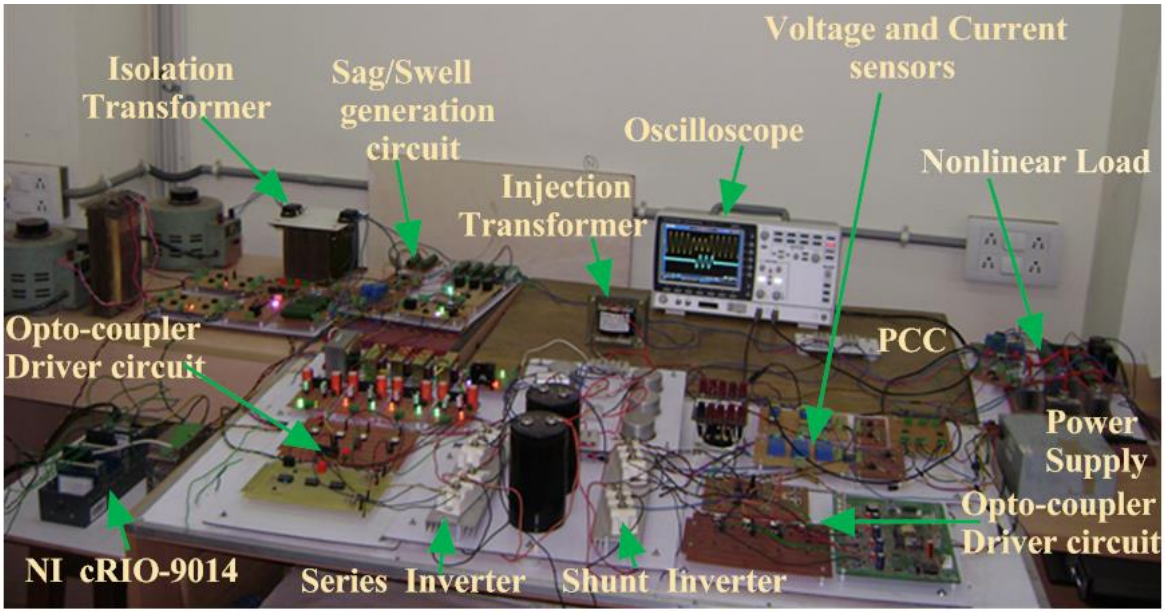


Fig. 6.2 Experimental set-up for UPQC system

- Single-phase Auto-transformer:
  - Max. Current capacity: 28 A per phase
  - Voltage Range: 0-100 V
  - Over-voltage Range: 0-170 V
- The measuring system includes:
  - Voltage Transducer-LEM LV 25-P [122]

    Current Transducer-LEM LA 55-P [123]

- Nonlinear Load:
  - Single-phase Diode Bridge Rectifier with a series RC load (R=0-100Ω, C=0-20 μF)

- DC Power supply:
  - ± 15 V DC supply
  - 5-0-5 V DC supply

The detail overviews of above components are presented in the next section.

6.2.1 Non-Linear Load

An assembly of nonlinear load is provided in Fig. 6.3, which is consisting of a single phase diode bridge rectifier, a resistive load and capacitive load. The resistive and capacitive loads are connected in parallel with the rectifier bridge. The load current can be changed with a variation of resistance (0-100 Ω) of resistive load since there are ten different tapings available in this load.

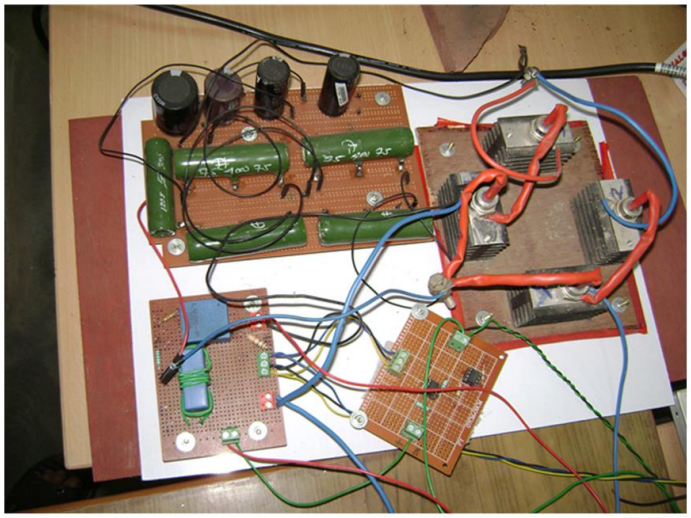


Fig.6.3 Nonlinear load

6.2.2 Voltage Source Inverter with DC-link capacitor

The single-phase UPQC is made up by using two VSI connected back to back through common DC-link capacitor. Each VSI consists of four units of IGBTs as shown in Fig. 6.4. Every unit of IGBT device has a rating of 1200 V and 35 A at 120 ˚C case temperature. The IGBT associates with some characteristics of bipolar junction transistor (BJT) and power metal oxide-semiconductor field-effect transistor (MOSFET). The new cluster of IGBT can be switched without the utilization of snubber components. The prospect of snubberless operation results in simpler design. Thus, it delivers a lower cost substitute to a MOSFET. Moreover, the continuity of current during blanking time period is maintained by the built-in

anti-parallel diodes. Furthermore, the DC-link capacitors connected to the IGBTs are consisting of two series capacitors of rating 450 V, 2200 μF. Thus, the DC-link capacitor has achieved the desired goal by restricting the DC voltage ripples with in the reasonable limit. The DC voltage ripple is determined according to the amount of active power supplied by the DC-link capacitor during both load and supply side perturbations.

6.2.3 Interfacing Inductors

Fig.6.5 shows the interfacing inductor L_{sh} connected between the ac-side of the VSI and PCC. It is utilized to transfer the energy between DC-link capacitor and the power line. Hence, it is required to balance between the switching losses and system response. The interfacing inductor is designed according to [124]. From the design requirement, minimum inductance ($L_{\min}$) value is calculated as follows.

$$L_{\min} = \frac{V_{S(peak)} + V_{dc}}{4hf} \tag{6.1}$$

The source current can be controlled by $L_{\min}$ in such a way that the rising slope of the source current is smaller than the slope of the triangle of the PWM. The UPQC system considers the supply voltage swelling up to 140 V. Thus, the values of $V_{s(peak)}, V_{dc}, h$ (peak value of triangular wave) and f_{sw} (switching frequency) are considered as 100 V, 220 V, 12 V, 10 kHz respectively. Therefore, $L_{\min}$ is calculated as 1.6 mH. However, an inductor value of 2 mH is adopted for safety reason.

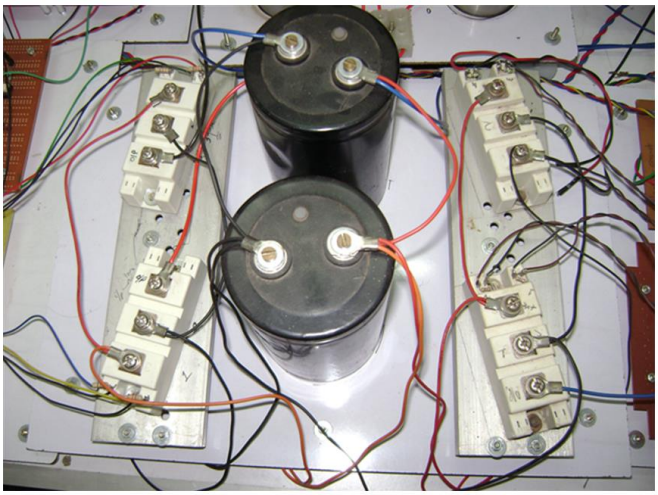


Fig. 6.4 IGBT based VSI

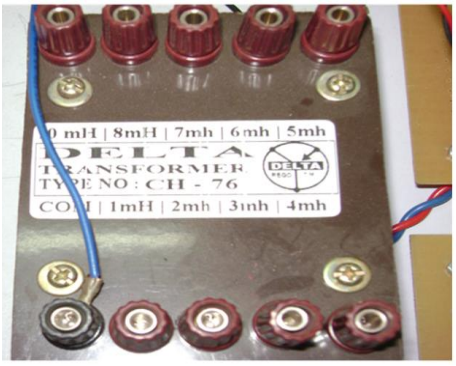


Fig. 6.5 Interfacing inductor

6.2.4 LC filter for series APF

LC filter is designed to eliminate the high frequency ripples of the inverter output voltage. Since the LC-filter is a low-pass filter, the resonant frequency of the LC-filter is designed to be as low as possible in order to achieve good filter result. The lowest possible resonant frequency is limited by the filtering band of the series APF, which is about 2 kHz.

The value of inductor and capacitor are determined by considering switching frequency f_{sw}. The value of capacitance (C_{se}) and inductance (L_{se}) are chosen in such a way that they offer a low impedance and high impedance path to the switching ripple. The reactance given by the capacitor C_{se} and inductor L_{se} calculated at half of the switching frequency are defined as,

$$X_{Rc} = \frac{1}{(2.\pi.f_{sw}.C_{se})} = \frac{1}{2.(3.14).C_{se}.5000} \tag{6.2}$$

$$X_{Rl} = 2.\pi.f_{sw}.L_{se} = 2.(3.14).L_{se}.5000 \tag{6.3}$$

Considering the values of X_{Rc} and X_{Rl} as 3 Ω and 100 Ω respectively, the values of C_{se} and L_{se} are calculated as 10.61 μF and 3.18 mH respectively. For the worst case condition, this dissertation adopts the values of C_{se} and L_{se} equal to 10 μF and 3.5 mH respectively.

6.2.5 Series coupling transformer

The injection transformers, which are used to inject the compensation voltage produced by the series APF, consist of single-phase transformers. The current rating of the coupling transformers is designed somewhat higher than those required by the applications to minimize the copper losses. In addition to this, the transformer core is designed to have

smaller iron losses compared to the ordinary power transformers. Based on the injection requirement, this dissertation considers the transformation ratio of the injection transformer as 4:1.

6.2.6 Design of sag/swell generation circuit

The sag/swell generation circuit described in this dissertation is simple and easy to implement in laboratory. Fig. 6.6 (a) shows single-phase 40 % sag generation circuit, which occurred during 3 cycle intervals of ac mains. The figure consists of 3 switches (S_1, S_2, S_3) and two resistor R_1 and R_2. Voltage sag can be generated using the voltage drop across these resistors. During normal operation, switch S_1 is closed and switches S_2 and S_3 are opened. However, switch S_1 is opened and switches S_2 and S_3 are closed during the voltage sag by adjusting the time relay for 60 ms. The magnitude of voltage sag generated during this time is dependent on voltage drops across the resistance R_1 and R_2. Switch S_1 is closed again and switches S_2 and S_3 are opened when the voltage sag ends. Similarly, Fig. 6.6 (b) shows a circuit diagram of single-phase 40 % voltage swell during 3 cycle intervals. Switch S_1 is closed and switch S_2 is opened during normal operation. However, switch S_1 is opened and switch S_2 is closed during voltage swell by adjusting the time relay for 60 ms. During this time, autotransformer T_2 is connected to the line through switch S_2 for adding extra 40 % of voltage with line voltage to generate voltage swell. Fig. 6.7 shows the experimental set-up for sag/swell generation circuit. The set-up consists of three relay switches (S_1, S_2 and S_3), timer circuit, Resistor banks R_1 and R_2 and auto-transformer as well as injection transformer required for voltage swell.

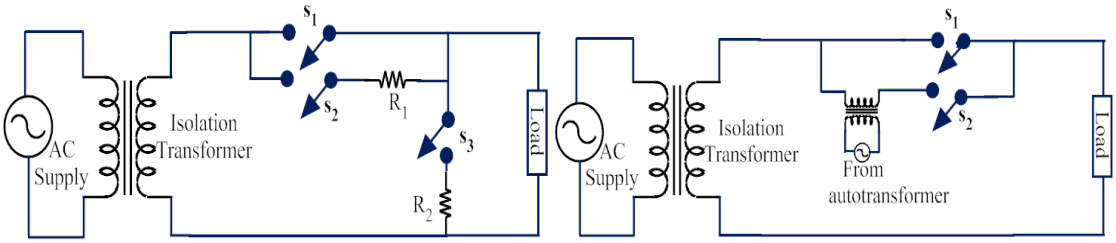


Fig.6.6 Schematic Diagram of (a) Sag generation circuit, (b) Swell generation circuit.

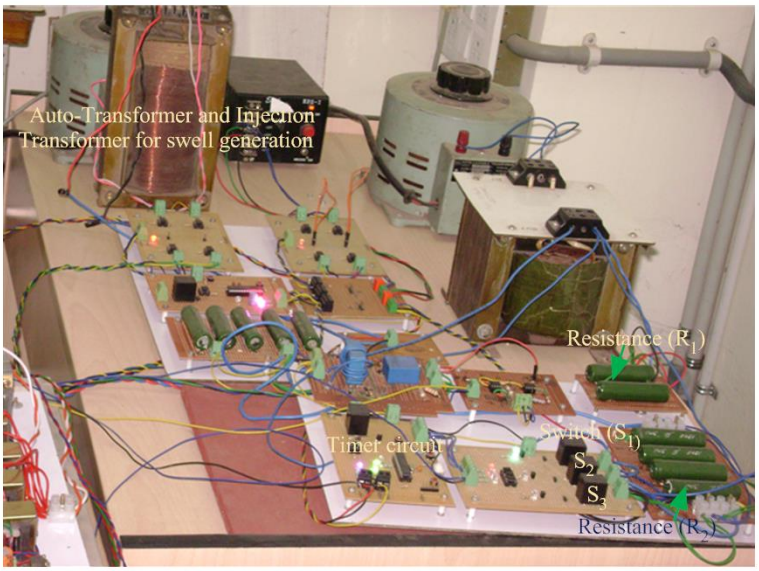


Fig. 6.7 Sag/Swell generation circuit

6.2.7 Voltage & Current Sensors:

Hall effect current and voltage transducer circuits measure high currents and voltages and transform them to a low voltage signal. These transducers offer many advantages. Some of these are:

- Very good linearity
- Low temperature drift
- Excellent accuracy

With knowledge of the magnitude of the currents and voltages to be measured, tranducer circuits are selected. Thus, the LEM LV 25-P and the LEM LA 55-P are used as voltage and current transducers respectively and the schematic diagrams of which are represented in Fig. 6.8 (a) and Fig. 6.8 (b) respectively. Both transducers require a ± 15 V supply voltage as well as external resistors to determine the ratio between the input signal and the output signal. This ratio is determined by the magnitude of the maximum current or voltage that must be measured on the primary side of the transducer circuits as well as by the magnitude of the desired output voltages on the secondary side. The transducer circuits provide isolation between the power network and the signal level circuits. The output signals must be restricted to ± 10 V, which is the maximum allowable voltage of the input module.

(i.) Design of the Voltage Sensor Circuit

In the experimental set up, the supply voltage is scaled down from ± 100V to ± 10V range. Referring the data sheet of the transducer [122], the input resistance R_{in} is chosen so as to fall the output resistance R_{op} in the range of 100-350Ω. The input current i_{in} can be obtained from $V_{in} = 100V$ and $R_{in} = 15k\Omega$.

$$i_{in} = \frac{V_{in}}{R_{in}} = \frac{100}{15 \times 10^3} = 6.67\,mA \tag{6.4}$$

With conversion ratio of 2500:1000 for transducer, the output current is calculated as

$$i_{op} = i_{in} \times \frac{2500}{1000} = 6.67 \times 2.5 = 16.67\,mA \tag{6.5}$$

The output resistance is chosen to be 300 Ω so that transducer output voltage lies in the range of ± 10V and hence the transducer output voltage becomes,

Output voltage= $R_{op} \times i_{op} = 300 \times 16.67 \times 10^{-3} = 5V$

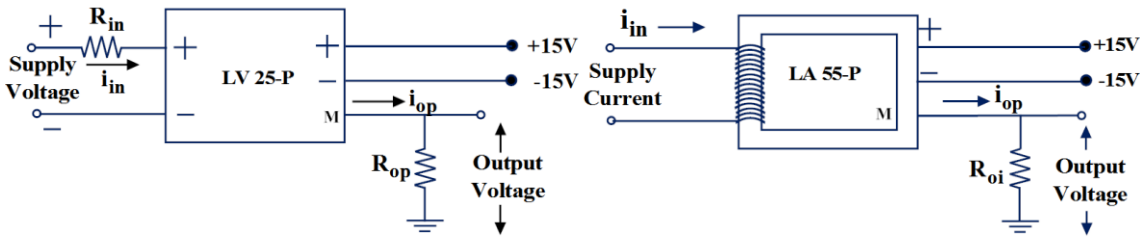
(ii.) Design of the Current Sensor Circuit

A current of ± 10A in the power network is converted to ± 10 V. The number of primary turns (N_p) is chosen such that the output resistance falls in the range of 50-160 Ω as specified in the datasheet of transducer [123]. With conversion ratio of 1:1000, $N_p = 5$ and $i_i = 10A$, the output current can be computed as

$$i_{op} = N_p \times i_{in} \times \frac{1}{1000} = \frac{5 \times 10}{1000} = 0.05A \tag{6.6}$$

The output resistance is chosen to be 100 Ω so that transducer output voltage lies in the range of ± 10V and hence the transducer output voltage becomes,

Output voltage = $R_{oi} \times i_{op} = 100 \times 0.05 = 5\,V$ (6.7)



(a) (b)

Fig. 6.8 Schematic Diagram of (a) Voltage Sensor, (b) Current Sensor

6.2.8 Signal Conditioning Circuit

The low level voltage signals (± 5 V) obtained from the voltage and current sensors are passed through the signal conditioning circuit (Fig. 6.9) to make them compatible with the NI-9201input panel (± 10 V). OPAMP TL064 has been used in this signal conditioning circuit and a DC supply of ± 15 V is applied.

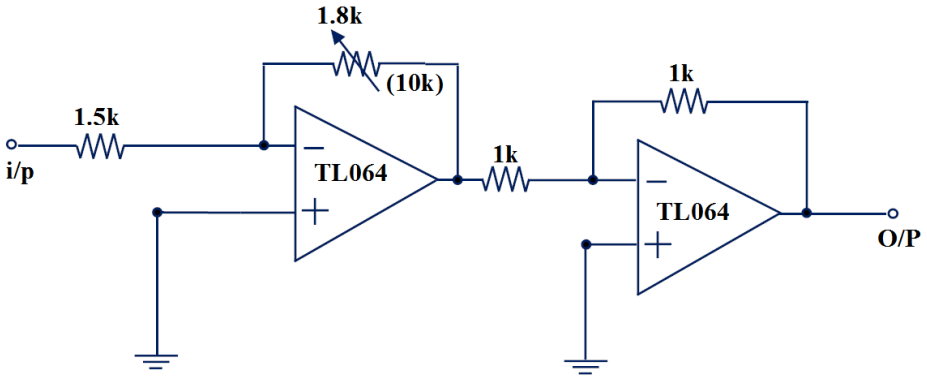


Fig. 6.9 Schematic Diagram of Signal conditioning Circuit

6.2.9 Blanking Circuit

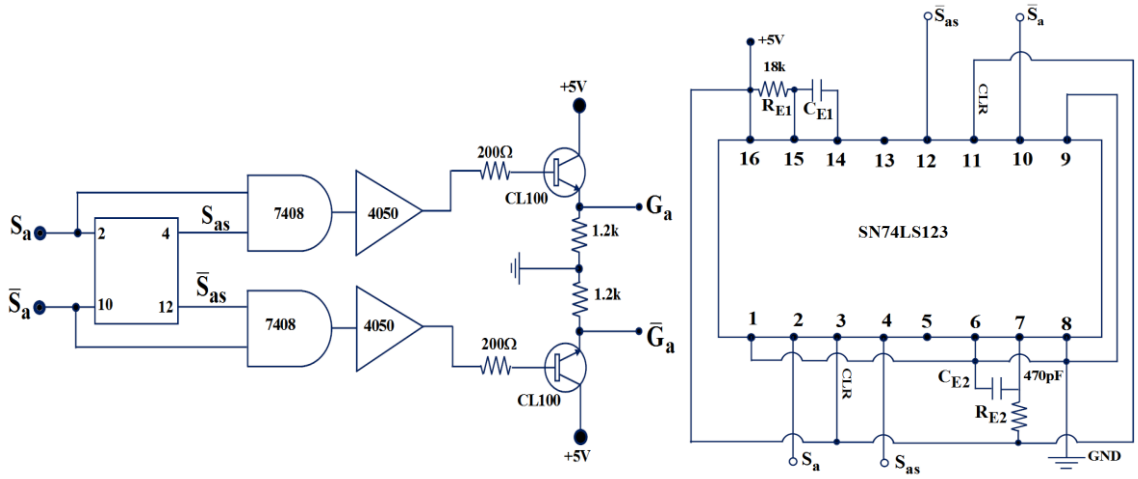
The switching pulses generated from the output port of NI-9263 panel are not directly fed to the IGBT switches of inverter. They are passed through the blanking circuit to avoid short circuit of the dc-link capacitor during the turning ON and OFF of both switches in the same leg of inverter. Hence, a dead band time is provided between turning ON and turning OFF of the switches in the same leg. Fig. 6.10(a) shows the blanking circuit. Its inputs are the switching pulses S_a and $\overline{S}_a$ generated from the output module of NI 9263. The detailed circuit diagram for two channels of the blanking circuit using mono-stable multi-vibrator (SN74LS123) is shown in Fig. 6.10(b). This unit generates two shot pulses S_{as} and $\overline{S}_{as}$ with

a duration of t_d . The gate signal G_a is generated by ANDing S_a and S_{as} using IC 7408 and passing this signal through a buffer (CD4050) and a transistor (CL100). Similarly, the complementary gate signal $\bar{G}_a$ can be achieved. The timing diagram of the blanking circuit including signals S_a, $\bar{S}_a$, S_{as}, $\bar{S}_{as}$, G_a and $\bar{G}_a$ is depicted in Fig. 5.20(c).

The expression for obtaining dead beat time 't_d' of mono-stable multi-vibrator [125] is given as follows.

$$t_d = 6 + 0.05C_{E1} + 0.45R_{E1}C_{E1} + 11.6R_{E1} \tag{6.8}$$

where, R_{E1} and C_{E1} are the external resistance and capacitance in kΩ and pF respectively. In this experiment, a dead beat time of 4μs is chosen by considering the values of R_{E1} and C_{E1} as 18 kΩ and 470 pF respectively in the above Eq. (6.8).



(a) (b)

Fig. 6.10 Schematic Diagram of (a) Banking Circuit, (b) Mono-stable Multi-vibrator circuit connection diagram.

6.2.10 Opto-Isolation Circuit

The gate signals obtainable from the blanking circuit can't be directly applied to the gates of the IGBT switches which consist of the high power network. Hence, high speed opto-couplers (TLP-250) with isolated dc power supplies are used for providing isolation between the logic control units and the power network. The schematic diagram of opto-coupler circuit is presented in Fig. 6.11.

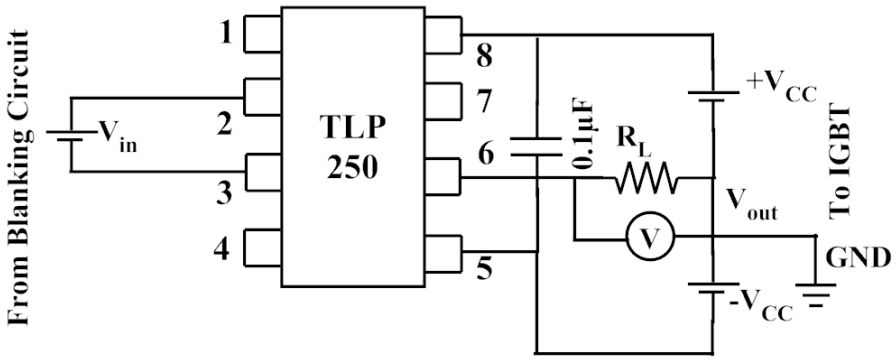


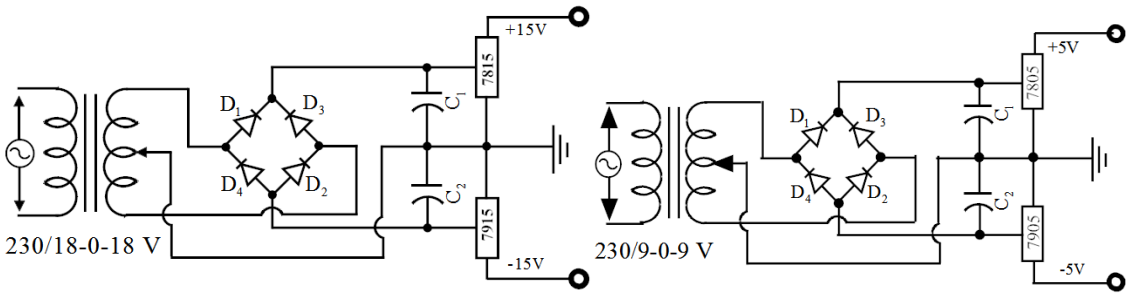
Fig. 6.11 Schematic Diagram of Opto-coupler circuit

6.2.11 Power supply

To build the experimental set-up, different voltage levels of DC power supplies are required, the details of which are given in Table 6.1. Fig. 6.12 (a) shows the circuit diagram of ±15 V DC supply. To produce a ±15 V DC voltage supply, a 230/18-0-18 V Centre-tapped step-down transformer of 1A rating is used. A full-bridge rectifier is used, which consists of 4 diodes (IN4007). Electrolytic capacitors C_1 and C_2, with 25 V and 2200 μF are used as filter capacitors at the output of rectifier. The centre-tap of the transformer and the second leg of the capacitors are connected to the ground. The unregulated dc voltages +15 V and -15V are given as input to the positive voltage regulator IC7815 and negative voltage regulator IC7915 respectively to generate DC output voltages of $\pm$ 15 V. Similarly, Fig.6.12 (b) shows the circuit diagram of ± 5 V DC power supply. A 230/9-0-9 V centre-tapped step-down of 1A and the positive and negative voltage regulator of IC7805 and IC7905 are used to generate a ± 5 V DC supply.

Table 6. 1 DC supply required for various Circuits

SL No.	Circuits	Dc Voltage
1.	Hall Effect Current Sensor Circuit	±15 V
2.	Hall Effect VoltageSensor Circuit	±15 V
3.	Signal Conditioning Circuit for Current Sensor	±15 V
4.	Signal Conditioning Circuit for VoltageSensor	±15 V
5.	Blanking Circuit	±5 V
6.	Opto-driver Circuit	±15 V and ±5 V



(a) (b)

Fig. 6.12 Schematic Diagram of DC power supply (a) $\pm 15\,V$ power supply, (b) $\pm 5\,V$ power supply.

6.3 Field-Programmable Gate Array (FPGA)

Field Programmable Gate Array (FPGA) is a reconfigurable circuit, which is commonly specified using a Hardware Description Language (HDL). The benefits of FPGA over Application Specific Integrated Circuit (ASIC) are enumerated below.

- ASICs are designed for a specific purpose utilizing CAD tools. Building up an ASIC is time consuming and expensive.
- It is not possible to rectify the errors of ASIC after fabrications.
- FPGA can be re-configured according to design requirement.
- The design and prototype measure of FPGA is small as compared to ASIC.

FPGA comprises programmable logic components named as logic blocks and a hierarchy of reconfigurable interrelates that permit the blocks to be weird together. Logic blocks are designed to execute complex combinational and sequential functions.

6.4 CompactRIO-9014

National Instruments (NI) compactRIO is a small rugged industrial data acquisition and control system powered by Reconfigurable Input-Output (RIO). NI compactRIO includes a real-time processor and reconfigurable FPGA for reliable stand-alone embedded or distributed applications. CompactRIO systems are recognized employing LABVIEW, the LABVIEW Real-Time (RT) Module and the LABVIEW FPGA Module [126,127,128]. CompactRIO includes following modules:

- 4 or 8-slots reconfigurable chassis
- Power supply
- Real time embedded processor
- Swappable industrial I/O modules

A block diagram of programmable controller is presented in Fig.6.13.

6.4.1 Reconfigurable Chassis

The reconfigurable chassis, as displayed in Fig. 6.14, is the foundation of NI compactRIO embedded systems. The reconfigurable chassis attributes the same rugged metal construction that characterizes the entire compactRIO platform.

6.4.2 Power Supply

CompactRIO-9014 comprises a power supply module which delivers a DC output of 24 V and 5 A to the real time embedded processor and input output modules.

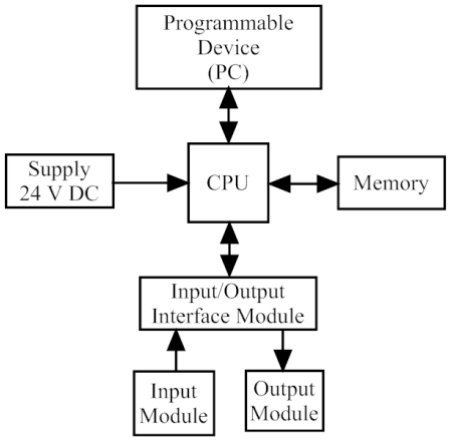


Fig.6.13 1 Block diagram of programmable controller

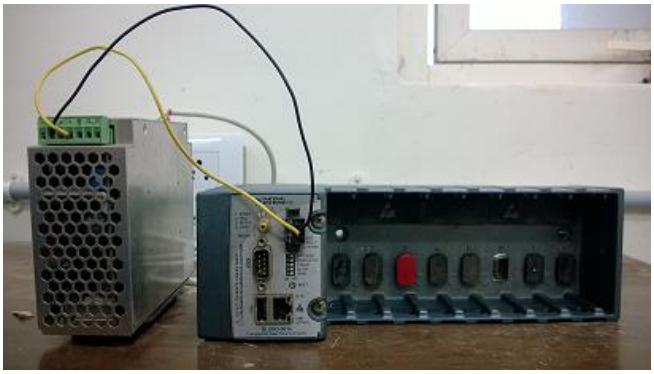


Fig. 6.14 The reconfigurable chassis

6.4.3 Real Time Embedded Processor

CompactRIO combines a low-power consumption real-time embedded processor with a high-performance RIO FPGA chip [129]. A local peripheral control interface (PCI) bus connection offers a high-performance interface between the RIO FPGA and the real-time processor. The cRIO core has built-in data transfer mechanisms to allow data to pass through the embedded processor for real-time analysis, post-processing, data logging, or communication to a networked host computer. For direct accessing of each module, the RIO FPGA chip is connected to the I/O modules in a star topology. Fig.6.15 (a) represents a cRIO real-time processor.

6.4.4 Input/output Modules

Each compactRIO I/O module includes built-in signal conditioning and screw terminal, BNC or D-Sub connectors. By assimilating the connector junction box into the modules, the compactRIO system significantly diminishes the space requirements and cost of field wiring. A variety of I/O types are available including ±10 V simultaneously sampling analog inputs/outputs, 24 V industrial digital I/O with up to 1 A current drive. Such an I/O module is depicted in Fig. 6.15 (b).

(a) (b)

Fig. 6.15 Real time processor with I/O module (a) FPGA controller, (b) An I/O module

6.5 Model Reference Robust Adaptive controller

In this section of dissertation, the feasibility of MRRAC system is considered, which is used in the UPQC system However, all these control strategies discussed are mainly utilized in three phase three wire industrial and commercial.

It is concluded that all proposed control techniques efficiently eliminate the PQ problems such as current harmonics, voltage distortion, voltage sag/swell and unbalanced supply voltage presented in the power system distribution network. However, all these control strategies discussed are mainly utilized in three phase three wire industrial and commercial nonlinear loads such as three phase variable speed drives, uninterruptable power supply (UPS), three phase rectifiers, arc furnaces, magnetic cores and resistance arc welders. However, a significant portion of nonlinear loads used in the domestic and service industries are single phase loads. These nonlinear loads such as personal computers, printers, copiers, and fax machines are finding their way into nearly every desk. In these loads, an AC system is usually connected to a low cost single-phase rectifier with a capacitor filter on DC side. The current drawn by this type of load is discontinuous because the capacitor only draws current for short period of time. Therefore source current is distorted normally over 70% [117] that results in failure or missed operation in all of these equipments.

To overcome the aforesaid single phase PQ issues, this chapter discusses about the single phase UPQC system by developing a prototype experimental set-up for testing robustness of the proposed model reference robust adaptive control (MRRAC). The objective of this experimental set-up is to demonstrate the working of a single phase UPQC system by compensating numerous PQ problems such as current harmonics, and voltage sag/swell. The performance capability of UPQC to compensate these PQ problems depends upon the accuracy of control strategy. Recently, significant attention has been paid to the control circuit designs of the UPQC, with objective to obtain reliable control algorithms and fast response techniques so that the UPQC can simultaneously tackle most of the PQ problems in the power distribution system.

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6.5.1 Simulation result

The proposed MRRAC method of UPQC is simulated using MATLAB/SIMULINK. The model consists of a simple 50 Hz power distribution system with single phase diode bridge rectifier feeding R_L, C_L load, which is considered as a nonlinear load. The performance of UPQC with MRRAC strategy is tested under different power quality issues like harmonics in supply current, voltage sag and voltage swell. The proposed control algorithm successfully mitigates all power quality problems and provides distorted less power to the load. In this simulation study, 50 % variation of three phase voltage for sag/swell is considered. The parameters used in the simulation are given in Appendix-4, where R_{sh} and L_{sh} are the interfacing inductor parameters for shunt APF, C_{dc} is the DC-link capacitor, V_{dc_ref} is the reference DC-link voltage, L_{se}, C_{se} are the inductance and capacitance of filter circuit respectively and V_{rms} is the RMS value of the supply voltage.

The current harmonics suppression capability of shunt APF is analyzed using proposed MRRAC method. The nonlinear load contains harmonics with total harmonics distortion (THD) of 23.6% shown in Fig. 6.19 (e). Fig. 6.19 (a), (b),(c) and (d) show the waveforms of

source current before compensation, compensation current (i_c), source current after compensation(i_s) and DC-link voltage (V_{dc}) respectively for the proposed method. From the results, it is clear that the shunt APF of UPQC provides an effective compensation of harmonics with THD of 2.13% in source current, which is shown in the source current spectrum of Fig.6.19 (f).

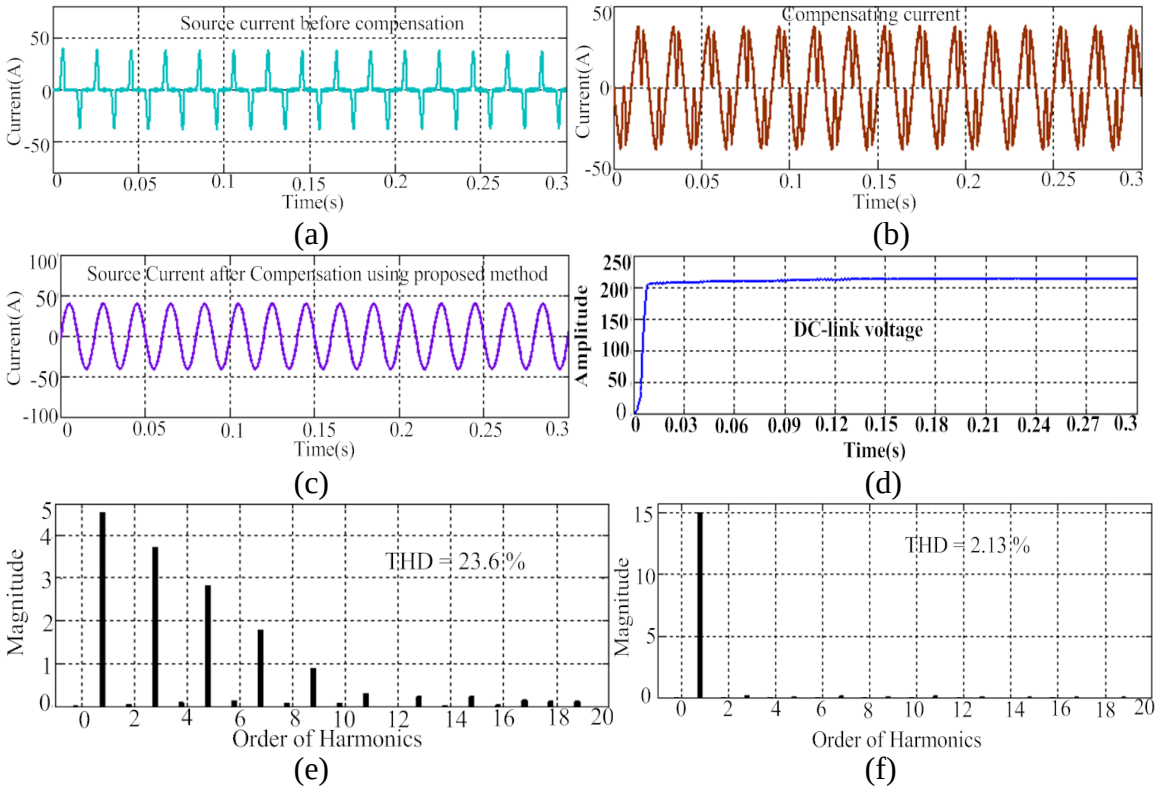


Fig.6.16 Simulation result of shunt APF for proposed MRRAC method, (a) Source current before compensation, (b) Compensating current, (c) Source current after compensation, (d) DC- link Capacitor voltage, (e) Source current spectrum before compensation, (f) source current spectrum after compensation.

The compensation capability of the conventional PI-control method is presented in Fig.6.20. Although the shunt APF of UPQC can compensate the harmonics in source currents, some amount of distortions are detected in source current, which is clearly observed from the Fig.6.20 (a).The primary cause behind this distortion is the performance inefficiency of conventional PI-control method in tracking the reference current. Fig.6.20 (b) and (c) deliver the information about compensating current and source current spectrum after compensation. Table 6.2 shows the THD comparison of both the control methods.

Table 6.2 THD comparison of Proposed MRRAC method and conventional PI-control method

Control method	THD before compensation	THD after Compensation
	Source current	Source current
Proposed method	23.6 %	2.13 %
Conventional PI-control method	23.6 %	3.91 %

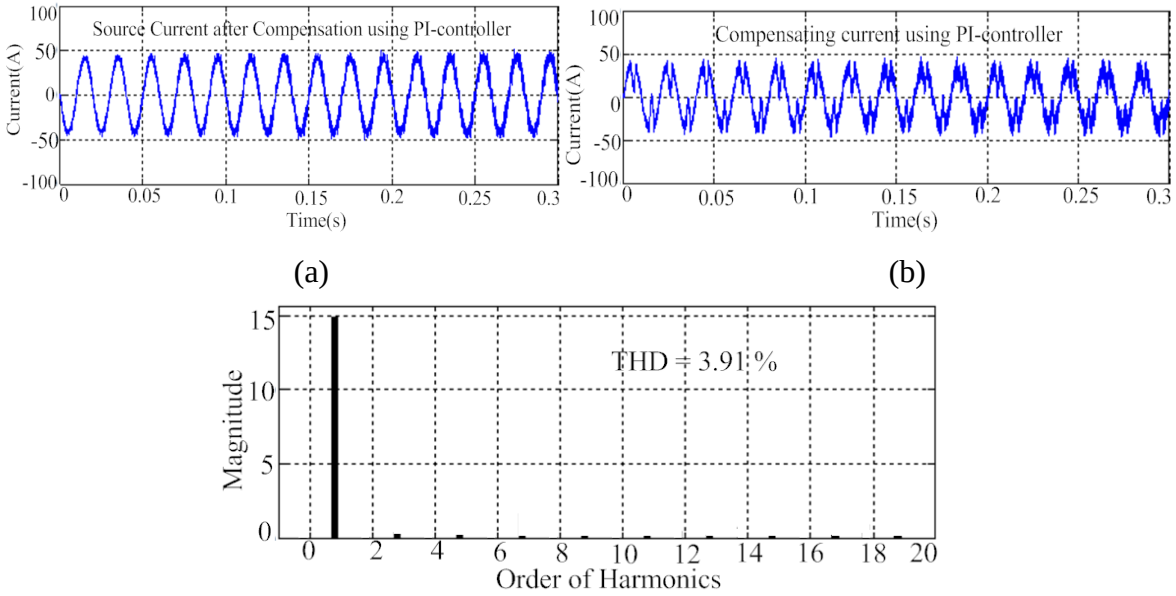
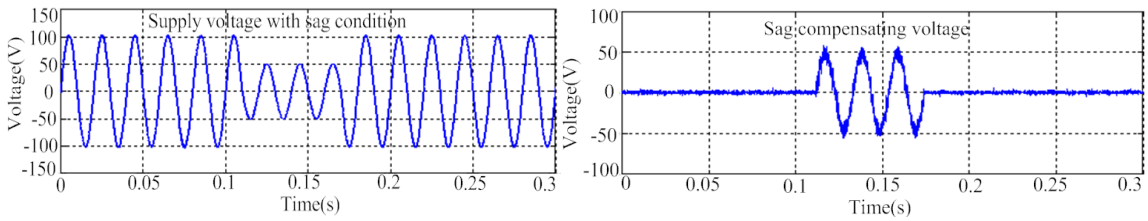


Fig.6.17 Simulation result of shunt APF for conventional PI-control method, (a) Source current after compensation, (b) Compensating current, (c) Source current spectrum after compensation.

Further, in case of sag/swell condition, 50 % of sag and 30 % of swell are considered, occurring in the interval of $0.12\,s \le t \le 0.18\,s$ for 3 cycles of ac-mains. Fig. 6.21 shows the compensation effectiveness of proposed technique during sag condition. Fig. 6.21 (a), (b), (c) and (d) signify the supply voltage (V_S) during the voltage sag condition, compensating voltage (V_C), load voltage (V_L) after compensation and DC-link voltage (V_{dc}) respectively.



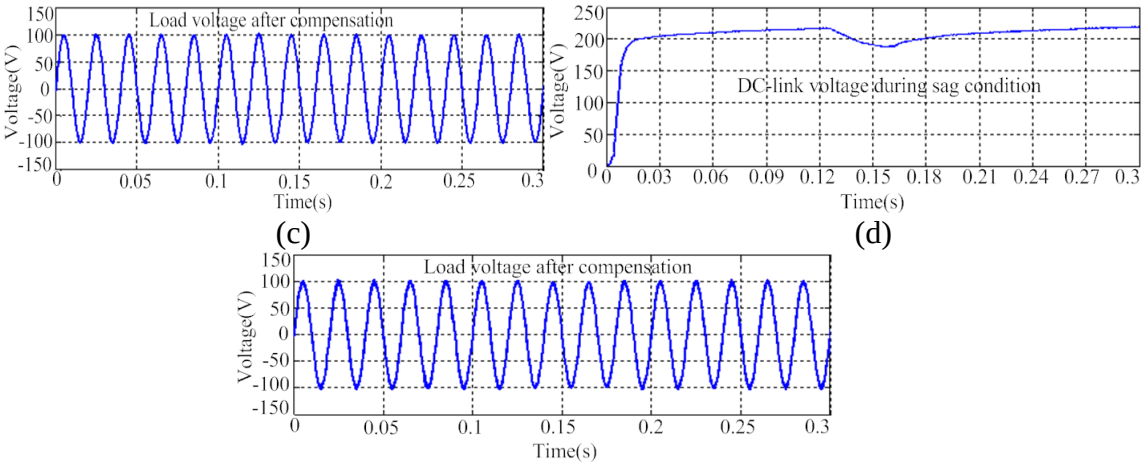


Fig.6.18 Simulation results during sag condition, (a) Supply voltage, (b) Compensation voltage, (c) Load voltage after compensation, (d) DC-link voltage, (e) Load voltage after compensation with PI-control method.

Also, Fig. 6.21 (e) shows the load voltage after compensation using PI-control method. Fig.6.22 (a) and (b) demonstrate the THD spectrum of load voltage after compensation using both the control methods and it is found that THDs of the load voltage using proposed MRRAC method and PI-control method are 2.06 % and 2.92 % respectively. Table 6.3 gives the THD analysis of both proposed MRRAC method and PI-control method during sag condition. From the tabulation it is clear that the proposed MRRAC method can satisfactorily compensate the sag in the load voltage with less THD in comparison to conventional PI-control method.

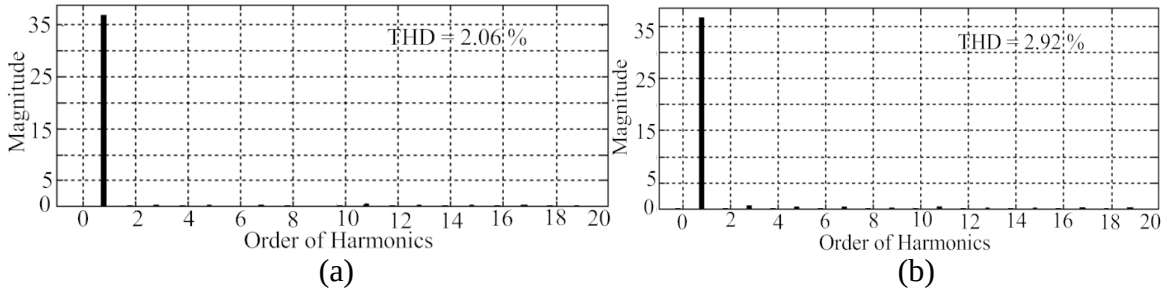


Fig.6.19 Load voltage spectrum after compensation during sag condition, (a) Using proposed MRRAC method, (b) Using conventional PI-control method.

Correspondingly, Fig.6.23 presents simulation result during swell condition. Fig. 6.23 (a), (b), (c), (d) and (e) represent the supply voltage (V_{sa}) during swell condition, compensating voltage (V_C), load voltage (V_L) after compensation using proposed MRRAC method, DC-link voltage (V_{dc}) and load voltage (V_L) after compensation using conventional

PI-control method respectively. Fig.6.24 (a) and (b) display the THD spectrum of load voltage after compensation. It is observed that THD of the load voltage using proposed MRRAC method is 2.02 %, whereas, the THD of Load voltage using PI-control method is 2.87 %. Table 6.4 gives the THD analysis of both proposed MRRAC method and PI-control method during supply voltage swell condition. From the tabulation it is clear that the proposed MRRAC method can satisfactorily compensate the swell in the load voltage with less THD in comparison to conventional PI-control method.

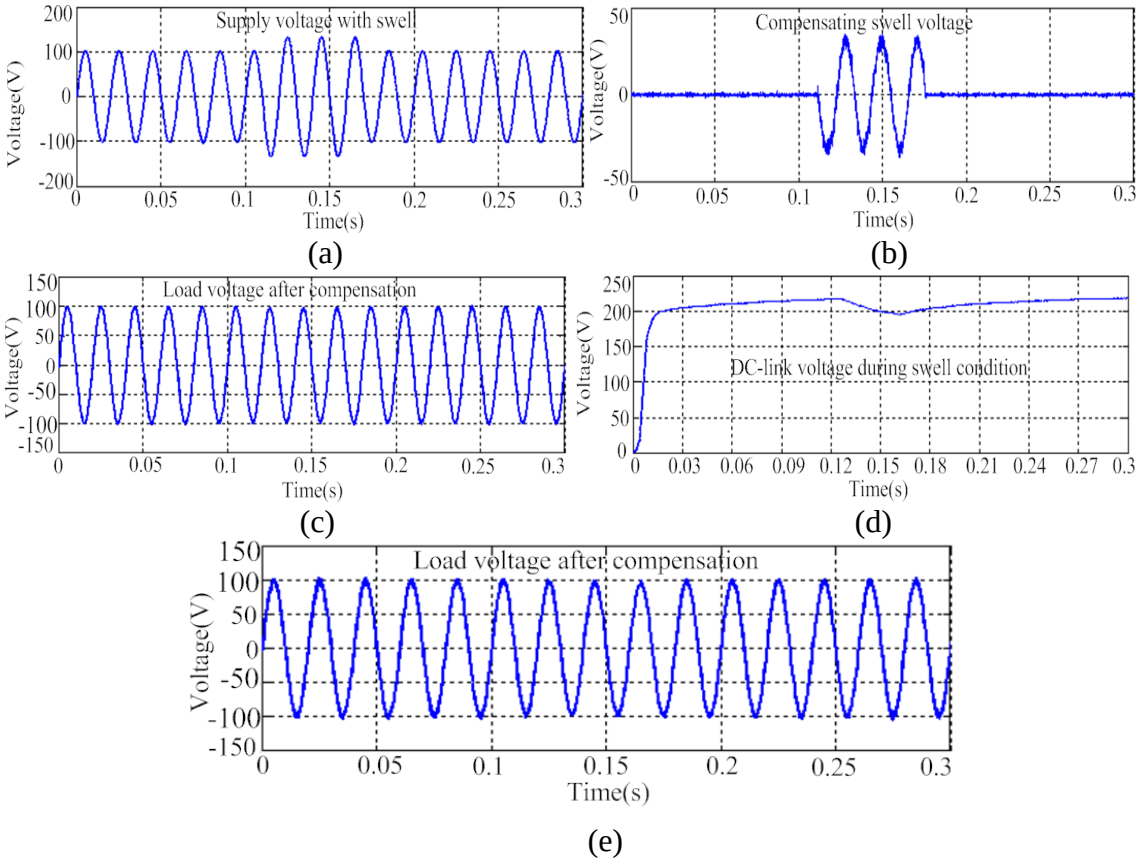
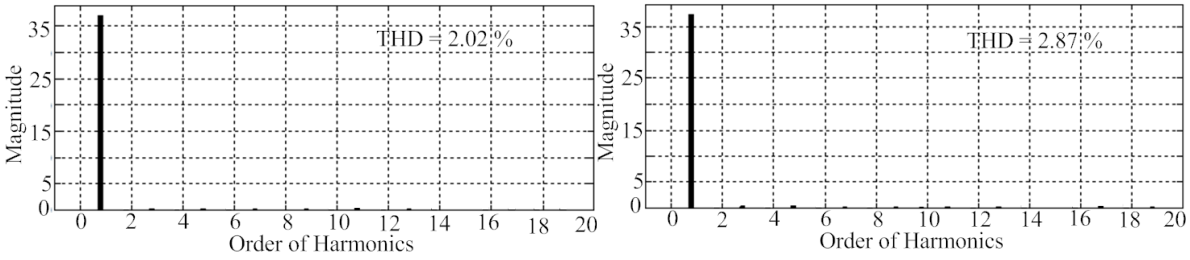


Fig.6.20 Simulation results during swell condition, (a) Supply voltage, (b) Compensation voltage, (c) Load voltage after compensation, (d) DC-link voltage, (e) Load voltage after compensation with PI-control method.



(a) (b)

Fig.6.24 Load voltage spectrum after compensation during swell condition, (a) Using proposed MRRAC method, (b) Using conventional PI-control method.

Table 6.3 Comparison of load voltage THD during sag/swell condition

Type of condition	Compensation with UPQC	
	Using proposed MRRAC method	Using PI-control method
Load voltage THD after compensation during supply voltage sag condition	2.06 %	2.92 %
Load voltage THD after compensation during supply voltage swell condition	2.02 %	2.87 %

6.5.2 Experimental result

The proposed MRRAC algorithm has been implemented in LABVIEW based FPGA CompactRIO-9014 system, which can control the experimental set up developed in the Lab to mitigate the PQ issues like current harmonics, voltage sag and voltage swell. The efficacy of the proposed MRRAC scheme is compared with conventional PI-control scheme based on the obtained experimental results. The design specifications and circuit parameters in laboratory prototype are mentioned in Appendix-4.

Fig.6.25 shows the experimental results for current harmonics compensation capability of shunt APF by using proposed MRRAC method. Fig. 6.25 (a) shows the experimental result of source current before compensation and compensating current in trace-1 and 2 respectively. Fig. 6.25 (b) and (c) show the source current after compensation and dc-link voltage respectively. Similarly, Fig. 6.25 (d) shows the experimental waveform of source current after compensation and compensating current using PI-control method in trace-1 and 2 respectively. From the result it is observed that the proposed MRRAC method can provide better harmonics compensation and make the soure current more sinusoidal in comparison to the PI-control method.

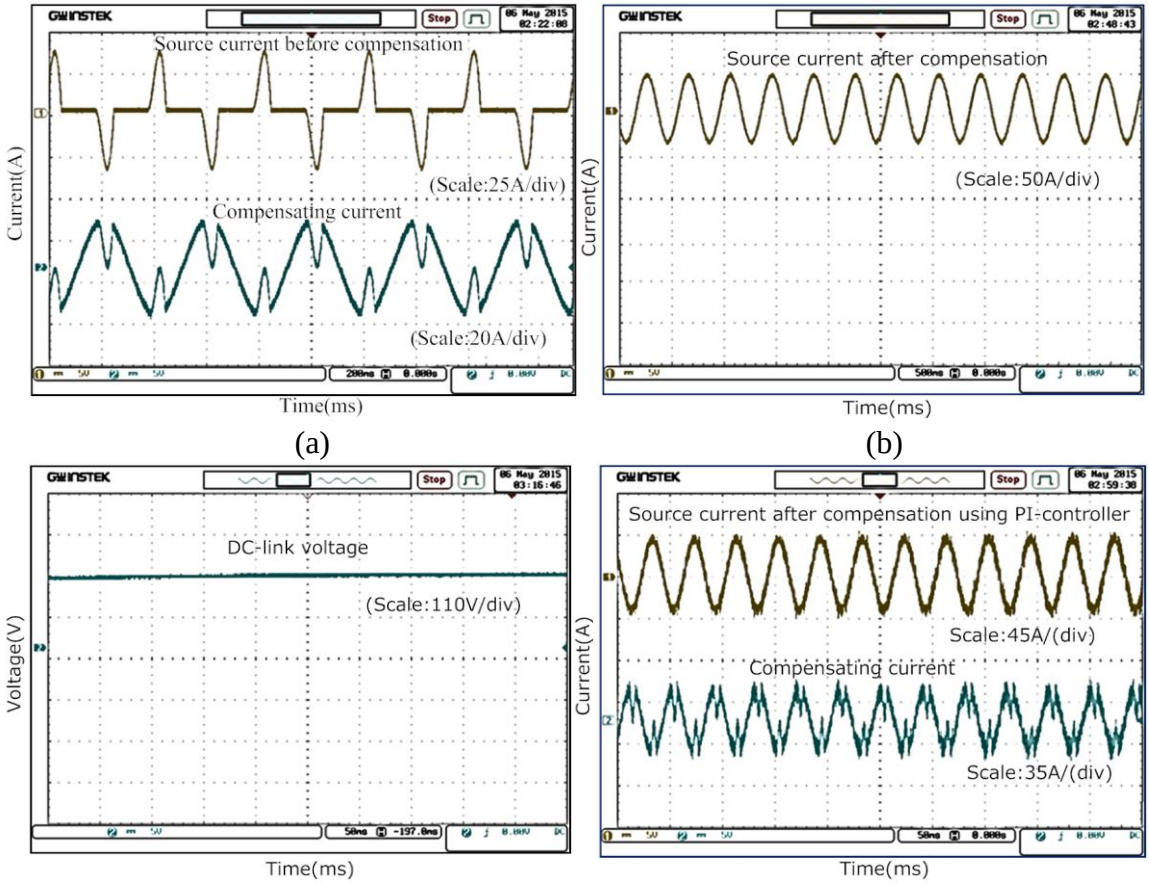


Fig.6.21 Experimental results of shunt APF using proposed MRRAC and PI-control method, (a) Source current before compensation and compensating current, (b) Source current after compensation, (c) DC-link voltage, (d) Source current after compensation and compensating current using PI-control method.

Fig. 6.26 illustrates the performance of UPQC during voltage sag condition. Fig.6.26 (a) shows the experimental result of supply voltage sag with a depth of 50 % and its corresponding compensating voltage in trace-1 and 2 respectively. Fig.6.26 (b) and (c) show the experimental waveforms of load voltage after compensation using proposed MRRAC method and dc-link voltage using sag condition respectively. Fig. 6.26 (d) shows the experimental waveform of load voltage after compensation using PI-control method. From the experimental results it is observed that the proposed MRRAC method compensates the voltage sag efficiently by utilizing the series APF, which injects the proper amount of voltage in the power network to make the load voltage stable in comparison to the PI-control method.

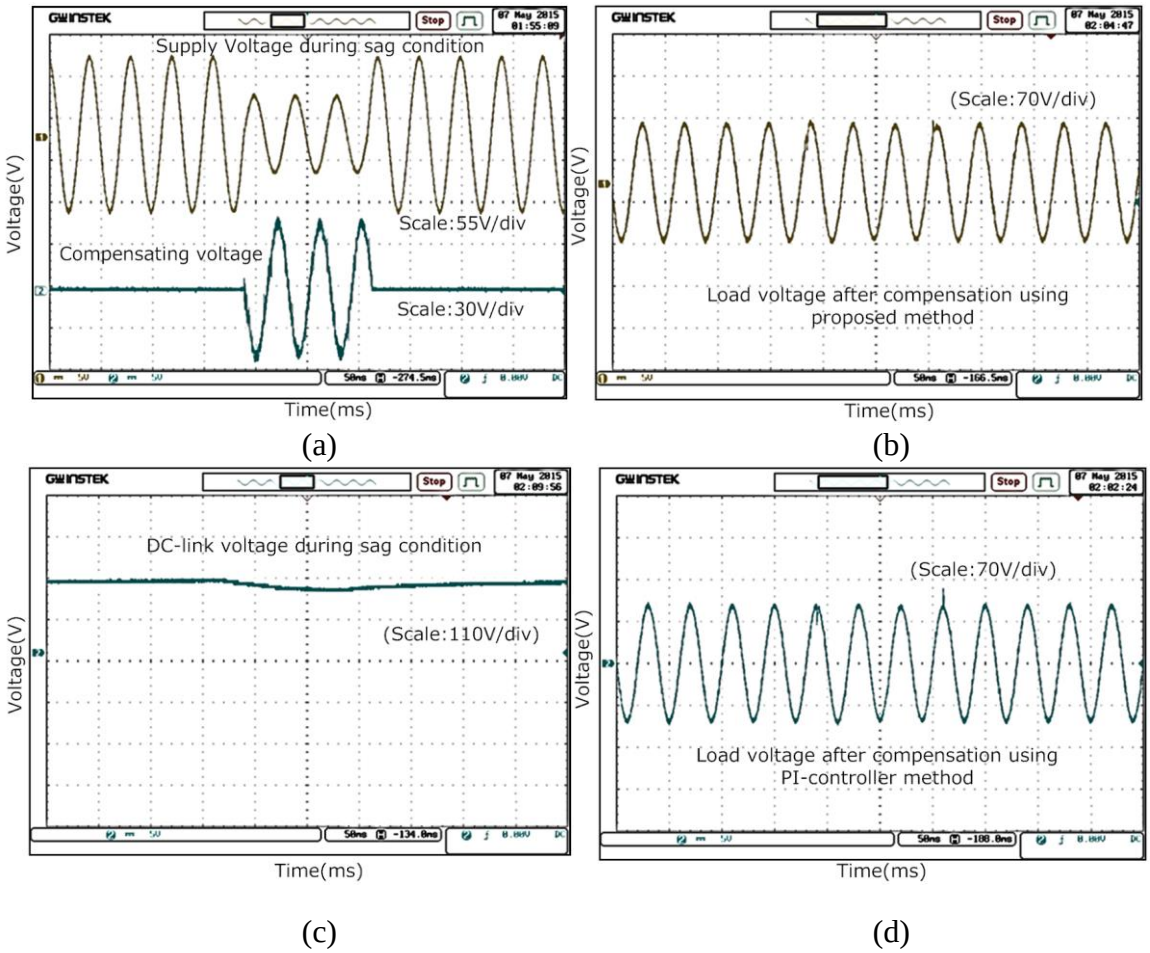


Fig 6.22 Experimental results during sag condition, (a) Supply voltage during sag condition and compensation voltage, (b) Load voltage after compensation using proposed MRRAC method, (c) DC-link voltage during sag condition, (d) Load voltage after compensation using PI-control method.

Fig. 6.27 demonstrates the performance of UPQC during voltage swell condition. Fig.6.27 (a) shows the experimental waveform of supply voltage swell of 30 % and its compensating voltage in trace-1 and 2 respectively. Fig.6.27 (b) and (c) show the experimental result of load voltage after compensation using proposed MRRAC method and dc-link voltage during swell condition respectively. Fig. 6.27 (d) shows the experimental result of load voltage after compensation using PI-control method. From the experimental results it is observed that the proposed MRRAC method compensates the voltage swell properly by utilizing the series APF, which injects the proper amount of voltage in the power network to make the load voltage stable in comparison to the PI-control method.

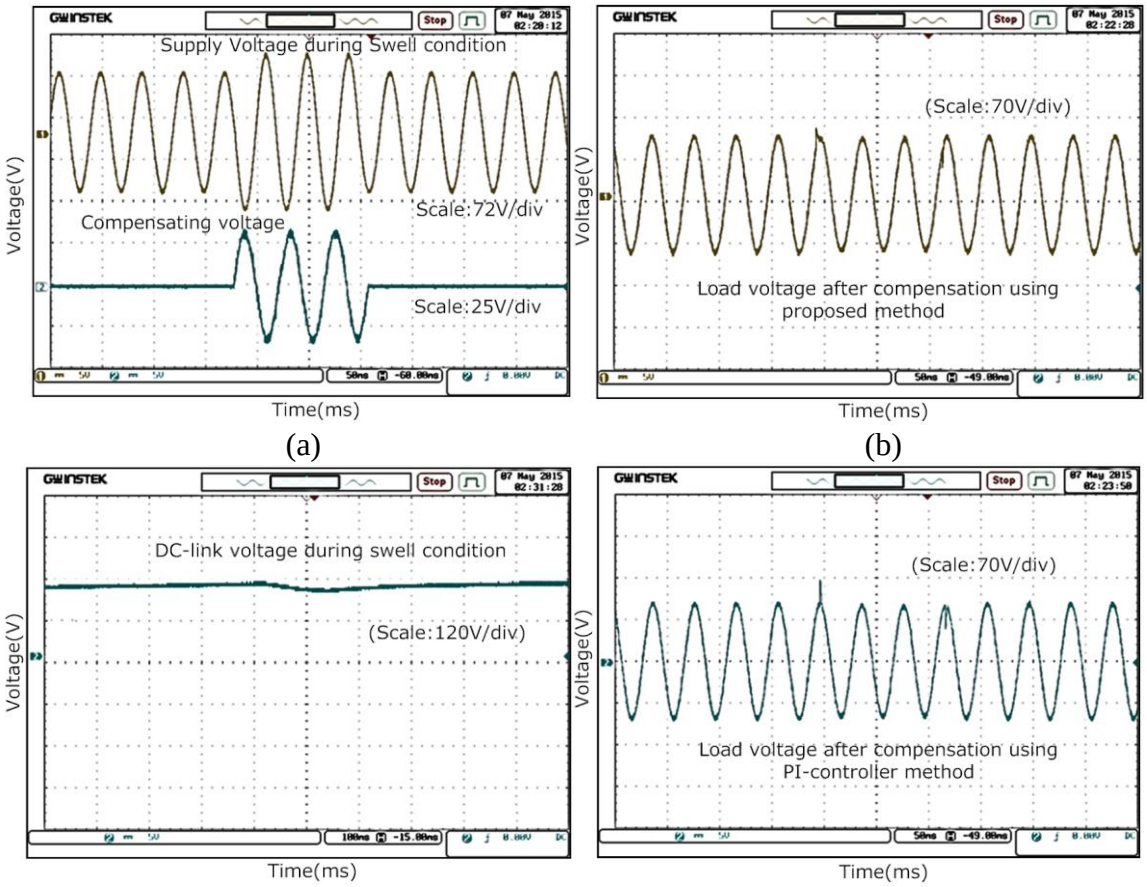


Fig 6.23 Experimental results during swell condition, (a) Supply voltage during swell condition and compensation voltage, (b) Load voltage after compensation using proposed MRRAC method, (c) DC-link voltage during swell condition, (d) Load voltage after compensation using PI-control method.

6.6 Chapter Summary

In this chapter, a MRRAC method has been developed for a single phase UPQC system. The proposed MRRAC algorithm can perform two control aspects, generates the reference signal for both APF and provides accurate tracking performance between plants output and reference signal. The model approach reference generation scheme is simple, reliable and self-regulator of dc-link voltage, which does not necessitate PI controller loop. A robust adaptive control approach is adopted in the inner control loop for achieving high stability and high disturbance rejection in UPQC. A proper selection of adaptive gain functions has been performed to specify the robustness, control effort performance and error tracking

performance of UPQC. Finally, the designed control scheme is tested on an experimental prototype UPQC model.

The power line uncertainties such as fluctuation of load, variation of system parameter, sudden failure of power system components and sensor nonlinearities degrade the reliability and efficiency of the UPQC system. Moreover, grid perturbations such as harmonics, measurement noise and supply voltage variation are responsible for power quality deterioration. Hence, the objective of designing a robust control strategy in UPQC system is achieved by accommodating all the possible perturbations occurring in the power system. From the experimental results, it is also observed that the proposed control approach to design a UPQC system is found to be robust in comparison to the PI-controller by yielding improvement in power quality more effectively in terms of tracking error reduction, efficient current harmonics mitigation as well as sag/swell compensation.

Chapter 7

Conclusion and Suggestions for future work

This chapter presents the overall conclusion and also suggests some future scope of research work as an extension of the work pursued in this thesis.

7.1 Overall Conclusion

This thesis has presented new reference voltage and reference current generation schemes along with new current and voltage control approaches for performance enhancement of Unified Power Quality Conditioner (UPQC). An extensive review on different control aspects of UPQC has been described in chapter 1 along with the discussion of their merits and demerits. Further, necessity of designing new control strategies in UPQC to achieve higher performance is explored.

The innovation of the thesis work lies in the introduction of nonlinear variable gain fuzzy-controller (NVGFC), non-linear sliding mode control (NLSMC), modified phase-locked loop (MPLL) based SRF, optimum active power (OAP) technique, fuzzy sliding mode (FSM) PWM control, resistive optimization technique (ROT), nonlinear variable gain fuzzy (NVGF) hysteresis PWM control, command generator tracker (CGT) based direct adaptive control (DAC) and model reference robust adaptive control algorithm (MRRAC) for minimization of both voltage and current concerned PQ problems in power system. A summary of developed control strategies of UPQC is presented below.

Two control strategies such as HCC and SMC have been proposed for the three-phase three-wire SAPF system in chapter-2 to enhance the PQ problem under balanced, unbalanced and distorted supply voltage conditions. Both the control strategies employ CO-PLL technique for positive sequence signal extraction utilized in reference current generation and PI controller for DC-link voltage regulation. It is observed from both simulation and experimental results obtained from Opal-RT that both control strategies of SAPF are able to compensate the source current to be almost sinusoidal under highly distorted load conditions. However, THD calculation confirms that SMC provides better

compensation capability as compared to HCC under balanced, unbalanced and distorted supply voltage condition.

To compensate both current and voltage related PQ problems, UPQC has been developed in chapter-3. Two novel control strategies such as nonlinear variable gain fuzzy-controller (NVGFC) and non-linear sliding mode control (NLSMC) with modified SRF technique have been proposed for DC-link voltage regulation in UPQC. The MPLL design involved in these control strategies is having an additional negative feedback applied in the inner loop of the conventional PLL and hence it is more immune to noise, distortion and harmonics indicating a perfect extraction of positive sequence signal during supply voltage distortion and unbalance condition. Further, this design eliminates the transformation angle oscillation during conversion process resulting in a fast and accurate extraction of the reference signal during power system perturbations. Consequently, the complete control strategy is independent of all disturbances and oscillations present during the fault occurred in source as well as load sides and makes the UPQC robust against all operating conditions of power system network. From simulation and experimental results it is demonstrated that the both NLSMC and NVGFC strategies successfully eliminate the several PQ problems such as current harmonics, voltage sag/swell, voltage unbalance and voltage distortion existing in the power distribution network. However, THD calculation confirms that NLSMC strategy provides better compensation by making source current and load voltage more sinusoidal in comparison to the NVGFC method during power system perturbations.

This thesis has further developed a resistive optimization technique (ROT) for reference signal extraction for both shunt and series APF as NLSMC technique is very sensitive to model mismatch and noise. This proposed ROT control algorithm adaptively regulates the DC-link capacitor voltage and makes the control system simple as it does not involve any complex optimization methods. A nonlinear variable gain fuzzy (NVGF) based hysteresis controller is proposed for regulating the hysteresis band, which effectively reduces the band violation and improves the tracking behaviour of UPQC during load transient and supply side transient conditions of power system. Additionally, an optimum active power (OAP) technique combined with enhanced phase-locked loop (EPLL) based fuzzy sliding mode (FSM) PWM control strategy have been implemented in UPQC. This structure quickly extracts the reference signal from the supply voltage and self-regulates the DC-link

capacitor voltage considering the peak amplitude of reference source current. Hence, the response time for regulating DC-link voltage is significantly improved as compared to the ROT based control strategy. Furthermore, the proposed FSM based PWM technique provides higher tracking performance with lower switching losses and eliminates the chattering problem associated with the sliding mode controller. The simulation and experimental results show that the proposed OAP-FSMC method of UPQC not only mitigates current harmonics correctly but also compensates voltage related problems such as voltage distortion, voltage sag/swell and voltage unbalance efficiently as compared to the ROT-NVGF method.

When there is a variation in either nonlinear load parameter or supply voltage parameter, the aforesaid control strategies described in chapter-4 fail to perform satisfactorily. Therefore, a command generator tracker (CGT) based direct adaptive control (DAC) is designed for UPQC in chapter-5. Initially, the command input signals are generated with respect to three step-input signals, which are accompanied with three different step times for making 120^0 phase shifted signal. Additionally, the command generator tracker (CGT) is designed by considering the reference model as an ideal oscillator. When three step-input signals having different step times are multiplied with the desired amplitude of source current as well as load voltage and are applied to the reference model, the output results in a desired sinusoidal reference signal. This provides a self-supporting DC-link voltage regulation by active power balancing system. Moreover, the proposed CGT-DAC approach provides more robustness, flexibility and adaptability in all operating conditions of the power system over OAP-FSM technique as observed from both the simulation and real-time experimental studies.

Control Strategies employed in the chapter 3, 4, and 5 consider a three-phase three-wire UPQC system. However, a significant portion of nonlinear loads used in the domestic and service industry areas are single phase loads and these nonlinear loads such as personal computers, printers, copiers and fax machines are finding their way into nearly every desk. Keeping above facts into consideration, chapter-6 discusses about the single phase UPQC system by developing a prototype experimental set-up based on LABVIEW NI cRIO-9014. A model reference robust adaptive control (MRRAC) technique is proposed in this chapter. Here, the adaptive control law is designed to track a linear reference model to reduce the

tracking error between model reference output signal and UPQC output signal to be controlled. Additionally, this proposed algorithm adaptively regulates the DC-link capacitor voltage without employing additional controller and hence provides more robustness, flexibility and adaptability in all operating conditions of the power system over a conventional PI-controller. Additionally, the proposed MRRAC technique adaptively changes the control gain according to the wide range of power system dynamic condition. As a result, it provides better tracking performance in all operating conditions of the power system network and delivers smoother sinusoidal source current and voltage in comparison to the conventional PI-controller. This adaptive performance of the UPQC is first verified through the simulation studies. Then experimental studies are carried out by using prototype hardware set-up. From both simulation and experimental results it is observed that proposed MRRAC technique can provide better PQ compensation such as current harmonics and voltage sag/swell in comparison to the conventional PI-controller.

7.2 Contributions of the Thesis

- A Coulon oscillator based PLL (CO-PLL) technique is proposed for extraction of positive sequence signal from the supply voltage and generates reference currents for SAPF under ideal, unbalanced and distorted supply voltage condition.
- A novel nonlinear dc-link voltage controller with modified SRF based control philosophy is proposed for UPQC in chapter-3. At first, design of a nonlinear variable gain fuzzy-controller (NVGFC) with modified phase-locked loop (MPLL) based SRF control strategy is proposed for three-phase, three-wire UPQC system. Then, a non-linear sliding mode control (NLSMC) and a novel SRF control technique have been proposed for rapid extraction of reference signal with a new switching dynamics control strategy for UPQC to improve the PQ problem in distributed power system network.
- Optimization based reference extraction methods with novel PWM current and voltage control techniques have been proposed for UPQC in chapter-4. Firstly, a resistive optimization technique (ROT) incorporated with enhanced phase-locked loop (EPLL) based nonlinear variable gain fuzzy (NVGF) hysteresis PWM control strategy for UPQC is implemented. Secondly, an optimum active power (OAP)

technique combined with EPLL based fuzzy sliding mode (FSM) PWM control strategy for three-phase three-wire UPQC system is proposed.

- A command generator tracker (CGT) based direct adaptive control (DAC) strategy has been proposed in UPQC for improving the power quality in three-phase three-wire distributed power system in chapter-5. A CGT is a model reference control law for a linear time-invariant system with known coefficients and it is formulated for the generation of the reference signal for both shunt and series compensator. Moreover, the adaptive control law is designed to track a linear reference model to reduce the tracking error between model reference output and measured signal to be controlled.
- A model reference robust adaptive control (MRRAC) is proposed in chapter-6. This proposed algorithm adaptively regulates the DC-link capacitor voltage without utilizing additional controller circuit. As a result, it provides more robustness, flexibility and adaptability in all operating conditions of the power system over a conventional PI controller.

7.3 Suggestions for future work

Although various power quality problems have been successfully tackled by the proposed control methods for the UPQC in this thesis, there are some possible problems that need to be considered and solved in the future research. They can be suggested as:

- This research can be extended to investigate the 3-phase 4-wire UPQC system.
- The experimental set-up developed for single phase UPQC system in Chapter-6 can be extended to three-phase three-wire UPQC system.
- Intelligent and new robust adaptive control techniques have to be designed for UPQC to optimize control objectives during different power system perturbations.
- A complete FPGA based controller for UPQC system can be developed that would add flexibility for controller design.

References

[1] H. Akagi and H. Fujita, "A new power line conditioner for harmonic compensation in power systems," *IEEE Transactions on Power Delivery*, vol. 10, no. 3, pp. 1570-1575, Jul. 1995.

[2] R. C. Dugan, M. F. McGranaghan, and H. W. Beaty, *Electrical Power Systems Quality*. New York: McGraw-Hill, 1996.

[3] IEEE, "IEEE recommended practice for powering and grounding electronic equipment," *IEEE Std 1100-1999*, pp. 1–408, 1999.

[4] ICNIRP, "Guidelines for Limiting Exposure to Time-Varying Electric, Magnetic and Electromagnetic Fields (Up to 300 MHz)," International Commission on Non-Ionizing Radiation Protection.

[5] C. Sankaran, *Power Quality*. Electric Power Engineering Series, Taylor & Francis, 2001.

[6] Y. Lim, G. Strbac, E. Engineering, and Electronics, *Probabilistic Assessments of Voltage sag Occurrence and the Evaluation of the Dynamic Voltage Restorer Capability*. UMIST.

[7] W. E. Brumsickle, R. S. Schneider, G. A. Luckjiff, D. M. Divan, and M.F. Mcgranaghan, "Dynamic sag correctors: cost-effective industrial power line conditioning," *IEEE Transactions on Industry Application*, vol.37, no.1, pp. 212-217, Feb.2001.

[8] A. F. Zobaa, "Optimal multiobjective design of hybrid active power filters considering a distorted environment," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 107-114, Jan. 2014.

[9] N. Gupta, S. P. Singh and S. P. Dubey, "Neural network based shunt active filter for harmonic and reactive power compensation under non-ideal mains voltage," *The 5th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pp.370-375, 15-17 June 2010.

[10] M. Newman, D. Holmes, J. Nielsen, and F. Blaabjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," *IEEE Transactions on Industry Application*,,vol.41, no. 6, pp. 1744–1753, Dec. 2005.

[11] B. B. Ambati, and V. Khadkikar, "Optimal Sizing of UPQC Considering VA Loading and Maximum Utilization of Power-Electronic Converters," *IEEE Transactions on Power Delivery*, vol.29, no.3, pp.1490-1498, Jun. 2014.

[12] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *IEEE Transactions on Industrial Electronic.*, vol. 46, no. 5, pp. 960 - 971, Oct. 1999.

[13] M. K. Mishra, A. Joshi, and A. Ghosh, "A new algorithm for active shunt filters using instantaneous reactive power theory," *IEEE, Power Engineering Review*, vol.20, no.12, pp.56-58, 2000.

[14] V. G. Kinhal, P. Agarwal, and H. O. Gupta, "Performance Investigation of Neural-Network-Based Unified Power-Quality Conditioner," *IEEE Transactions on Power Delivery*, vol.26, no.1, pp.431-437, Jan. 2011.

[15] S. Zhikang, Y. Peng, Z. J. Shen, T. Chunming, J. Fei, and C. Ying, "Design Considerations of a Fault Current Limiting Dynamic Voltage Restorer (FCL-DVR)," *IEEE Transactions on Smart Grid*, vol.6, no.1, pp.14-25, Jan. 2015.

[16] A. Ghosh, A. K. Jindal, and A. Joshi, "Design of a capacitor-supported dynamic voltage restorer (DVR) for unbalanced and distorted loads," *IEEE Transactions on Power Delivery*, vol.19, no.1, pp.405-413, Jan. 2004.

[17] M. El-Habrouk, M. K. Darwish, and P. Mehta, "Active power filters: A review," *IEE Electr. Power Appl.*, vol. 147, no. 5, pp. 403–413, 2000.

[18] S. Moran, "A line voltage regulator/conditioner for harmonic-sensitive load isolation," *in Proc. Ind. Appl. Soc. Annu. Meet. Conf.*, pp. 947–951, Oct. 1–5, 1989.

[19] S. Ganguly, "Multi-Objective Planning for Reactive Power Compensation of Radial Distribution Networks With Unified Power Quality Conditioner Allocation Using Particle Swarm Optimization," *IEEE Transactions on Power Systems*, vol.29, no.4, pp.1801-1810, Jul. 2014.

[20] P. E. Meli´ın, J. R. Espinoza, J. A. Mu˜noz, C. R. Baier, and E. E. Espinosa,"Decoupled control of a unified power quality conditioner based on a current source topology for fast AC mains disturbance compensation," *in Proc. IEEE Int. Conf. Ind. Technol*., pp. 730–736, Mar. 2010.

[21] D. Graovac, V. Katic, and A. Rufer, "Power quality compensation using universal power quality conditioning system," *IEEE Power Eng. Rev*., vol. 20, no. 12, pp. 58–60, 2000.

[22] H. R. Mohammadi, R. Y. Varjani, and H. Mokhtari, "Multiconverter unified power-quality conditioning system: MC-UPQC," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1679–1686, Jul. 2009.

[23] B. Han, B. Bae, H. Kim, and S. Baek, "Combined operation of unified power-quality conditioner with distributed generation," *IEEE Transactions on Power Delivery*, vol. 21, no. 1, pp. 330–338, Jan. 2006.

[24] M. Davari, S. M. Ale-Emran, H. Yazdanpanahi, and G. B. Gharehpetian, "Modeling the combination of UPQC and photovoltaic arrays with multi-input single-output DC–DC converter," *in Proc. Power Syst. Conf. Expo*., pp. 1–7, Mar. 15–18, 2009.

[25] S. Chakraborty, M.Weiss, and M. Simoes, "Distributed intelligent energy management system for a single-phase high-frequency AC microgrid,"*IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 97–109, Feb. 2007.

[26] M. Aredes, K. Heumann, and E. H. Watanabe, "An universal active power line conditioner," *IEEE Transactions on Power Delivery*, vol. 13, no. 2, pp. 545–551, Apr. 1998.

[27] T. Zhili and D. Zhu, "A new control strategy for three-phase four-wire UPQC when voltage fluctuating on its DC side," *in Proc. 2nd IEEE Int. Symp. Power Electron. Distrib. Generation Syst.*, pp. 190–195, Jun. 16–18, 2010.

[28] S. W. Park, I. Y. Chung, J. H. Choi, S. I. Moon, and J. E. Kim, "Control schemes of the inverter-interfaced multi-functional dispersed generation," in Proc. Power Eng. Soc. Gen. Meet., Jul. 13–17, pp. 1924–1929, 2003.

[29] M. Aredes, J. Hafner, and K. Heuma, "Three-Phase Four-Wire Shunt Active Filter Control Strategies," *IEEE Transactions on Power Electronics,* vol. 12, no. 2, pp. 311-318, Mar. 1997.

[30] V. Khadkikar, A. Chandra, and B. N. Singh, "Generalised single phase p-q theory for active power filtering: simulation and DSP-based experimental investigation," *IET Power Electronics,* vol. 2, no. 1, pp. 67-78, 2008.

[31] X. Yuan, W. Merk, and H. Stemmler, "Stationary-frame generalized integrators for current control of active power filters with zero steady state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 523-532, Apr. 2002.

[32] V. Soares, and P. Verdelho , G. D. Marques, "An Instantaneous Active and Reactive Current Component Method for Active Filters," *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 660-669, Jul 2000.

[33] N. Gupta, S. P. Singh and S. P. Dubey, "Fuzzy logic controlled shunt active power filter for reactive power compensation and harmonic elimination," *2nd International Conference on Computer and Communication Technology (ICCCT),* pp.82-87, 15-17 Sept. 2011.

[34] L. H. Tey, P. L. So, and Y. C. Chu, "Improvement of power quality using adaptive shunt active filter," *IEEE Transactions on Power Delivery*, vol.20, no.2, pp. 1558-1568, 2005.

[35] K. K. Shyu, M. J. Yang, Y. M. Chen, and Y. F. Lin, "Model reference adaptive control design for a shunt active power filter system", *IEEE Transactions on Industrial Electronics,* vol.55, no.1, pp. 97-106, Jan. 2008.

[36] A. Bhattacharya, and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN based predictive and adaptive controllers", *IEEE Transactions on Industrial Electronics,* vol.58, no.2, pp. 421-428, Feb. 2011.

[37] R. L. A. Ribeiro, C. C. Azevedo, and R. M. Sousa, "A Robust Adaptive Control Strategy of Active Power Filters for Power-Factor Correction, Harmonic Compensation, and Balancing of Nonlinear Loads", *IEEE Transactions on Power Electronics,* vol.27, no.2, pp. 718-730, Feb. 2012.

[38] R. L. A. Ribeiro, T. O. A. Rocha, and R. M. Sousa, "A Robust DC-Link Voltage Control Strategy to Enhance the Performance of Shunt Active Power Filters Without Harmonic Detection Schemes", *IEEE Transactions on Industrial Electronics*, vol.62, no.2, pp. 803-813, Feb. 2015.

[39] H. Fujita and H. Akagi, "The unified power quality conditioner: The integration of series and shunt-active filters," *IEEE Transactions on Power Electronics*, vol. 13, no. 2, pp. 315–322, 1998.

[40] V. Khadkikar, "Enhancing electric power quality using upqc: A comprehensive overview," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2284–2297, May. 2012.

[41] N. G. Jayanti, M. Basu, M. F. Conlon, and K. Gaughan, "Rating requirements of the unified power quality conditioner to integrate the fixed speed induction generator-type wind generation to the grid," *Renewable Power Generation, IET* , vol.3, no.2, pp.133-143, 2009.

[42] M. Basu, S. P. Das, and G. K. Dubey, "Investigation on the performance of UPQC-Q for voltage sag," IET Gener. Transm. Distrib., vol. 2, no.3, pp. 414-423, 2008.

[43] A. Teke, L. Saribulut, and M. Tumay, "A Novel reference signal generation method for power-quality improvement of unified power-quality conditioner," *IEEE Transactions on Power Delivery*, vol.26, no.4, pp.2205-2214, Apr. 2011.

[44] H. Xinming, L. Jinjun, and Z. Hui,. "A unified compensator design based on instantaneous energy equilibrium model for the DC link voltage control of UPQC," *Applied Power Electr. Conf. and Exposition, 24 Annual IEEE*, pp. 1577-1582. 2009.

[45] M. Davari, S. M. Aleemran, H. NafIsi, I. Salabeigi, and G. B. Gharehpetian, "Modeling the combination of UPQC and photovoltaic arrays with multi-input single-output DC-DC converter," *Industrial Technology, IEEE International Conference*, pp.1-6, 2009.

[46] H. Zhou, J. Wan, C. Yuan, and S. Li, "Analytical research on unified power quality conditioner based on super capacitors energy storage system," *Power Electronics Systems and Applications (PESA), 2011 4th International Conference*, pp.1-5, 8-10 June 2011.

[47] M. C. Cavalcanti, G. M. S. Azevedo, B. A. Amaral and F. A. S. Neves, "Unified power quality conditioner in a grid-connected photovoltaic system," *EPQU Journal*, vol. 12, pp. 59-69, 2006.

[48] A. Iurie, M. Basu, and M. F. Conlon, "DC link voltage control of UPQC for better dynamic performance," *Electric Power Systems Research*, vol. 81, no.9, pp. 1815-1824, 2011.

[49] T. Zhili, and Z. Dongjiao, "Design of dc voltage controller for UPQC by using its small signal model," *in Proc. Electr. Control Eng*., pp. 3572–3575, Jun. 25–27, 2010.

[50] Z. Dongjiao and T. Zhili, "A new method to design the dc voltage controller for UPQC," *2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp.196-199, 16-18 June 2010.

[51] C. Fitzer, M. Barnes, and P. Green, "Voltage sag detection technique for a dynamic voltage restorer*," IEEE Transactions on Industry Applications*, vol. 40, no. 1, pp. 203–212, 2004.

[52] D. Kisck, V. Navrapescu, and M. Kisck, "Single-phase unified power quality conditioner with optimum voltage angle injection for minimum va requirement," *Electronics Specialists Conference* in *Power, PESC 2007. IEEE*, pp. 574–579, 2007.

[53] R. Sudeep Kumar and P. Ganesan, "250 kVA unified power quality controller," in TENCON 2006. 2006 IEEE Region 10 Conference, pp. 1–4, 2006.

[54] K. Kwan, P. So, and Y. Chu, "Unified power quality conditioner for improving power quality using mVR with Kalman filters," *The 7th International* in *Conference Power Engineering, IPEC 2005.*, pp. 980–985 Vol. 2, 2005.

[55] V. Khadkikar, A. Chandra, "A Novel Control Approach for Unified Power Quality Conditioner Q without Active Power Injection for Voltage Sag Compensation," *Industrial Technology (ICIT), IEEE International Conference*, pp.779-784, 15-17 Dec. 2006.

[56] I. Axente, J. Ganesh, M. Basu, M. Conlon, and K. Gaughan, "A 12-kVA dsp-controlled laboratory prototype UPQC capable of mitigating unbalance in source voltage and load current," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1471–1479, Jun. 2010.

[57] V. Khadkikar, A. Chandar, A. O. Barry and T. D. Nguyen, "Application of UPQC to protect a sensitive load on a polluted distribution network," *Power Engineering Society General Meeting*, IEEE, pp. 1-6, 2006.

[58] Y. Chen, X. Zha, J. Wang, H. Liu, J. Sun and H. Tang, "Unified power quality conditioner (UPQC): The theory, modeling and application,*" Power System Technology, International Conference*, vol. 3, pp. 1329-1333, 2000.

[59] A. K. Jindal, A. Ghosh and A. Joshi, "The protection of sensitive loads from inter-harmonic currents using shunt series active filters," *Electric Power Systems Research*, vol.73, no.2, pp. 187-196, 2005.

[60] M. Kesler, E. Ozdemir, "Synchronous-Reference-Frame-based control method for UPQC under unbalanced and distorted load conditions," *IEEE Transactions on Industrial Electronics*, vol.58, no.9, pp.3967-3975, Sep.2011.

[61] L. H. Tey, P. L. So and Y. C. Chu, "Neural network-controlled unified power quality conditioner for system harmonics compensation," *Asia Pacific IEEE/PES Transactions and Distr. Conf. and Exhibition*, vol. 2, pp. 1038-1043, 2002.

[62] M. Forghani and S. Afsharnia, "Online Wavelet Transform-Based Control Strategy for UPQC Control System," *IEEE Transactions on Power Delivery*, vol.22, no.1, pp.48-491, Jan. 2007.

[63] R. Yuanjie, C. Li, and Q. Ding. "An adaptive harmonic detection and a novel current control strategy for unified power quality conditioner." *Simulation Modelling Practice and Theory*, vol.17, no.5, pp.955-966, 2009.

[64] K. H. Kwan, Y. C. Chu, and P. L. So, "Model-based H-∞ control of a unified power quality conditioner," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2493– 2504, Jul. 2009.

[65] F. Kamran and T. Habetler, "Combined deadbeat control of a series-parallel converter combination used as a universal power filter," *IEEE Transactions on Power Electronics*, vol. 13, no. 1, pp. 160–168, Jan.1998.

[66] S. Karanki, M. Mishra, and B. Kumar, "Particle swarm optimization-based feedback controller for unified power-quality conditioner," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2814–2824, Oct. 2010.

[67] Z. Ming, W. Jian-Ru, W. Zhi-Qiang, and C. Jian, "Control method for power quality compensation based on levenberg-marquardt optimized bp neural networks," *Conference in Power Electronics and Motion Control, IPEMC 2006. CES/IEEE 5th International*, vol. 3, pp. 1–4, 2006.

[68] K. H. Kwan, P. S. Lam and Y. C. Chu, "An Output Regulation-Based Unified Power Quality Conditioner With Kalman Filters," *IEEE Transactions on Industrial Electronics* , vol.59, no.11, pp.4248-4262, Nov. 2012.

[69] A. E. Leon, S. J. Amodeo, J. A. Solsona, and M. I. Valla, "Non-linear optimal controller for unified power quality conditioners." *IET Power Electronics*, vol. 4, no.4, pp. 435-446, 2011.

[70] Y. Rong, C. Li, H. Tang, and X. Zheng, "Output feedback control of single-phase UPQC based on a novel model," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1586–1597, Jul. 2009.

[71] M. Fatiha, M. Mohamed, and A. A. Nadia. "New hysteresis control band of an unified power quality conditioner." *Electric Power Systems Research*, vol.81, no.9, pp.1743-1753, 2011.

[72] F. Mekri, M. Machmoum, N. A. Ahmed, and B. Mazari, "A fuzzy hysteresis voltage and current control of an unified power quality conditioner." *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008.

[73] R. Faranda, "UPQC compensation strategy and design aimed at reducing losses," *Industrial Electronics, 2002. ISIE 2002. Proceedings of the 2002 IEEE International Symposium on* , pp.1264-1270, 2002.

[74] X. Zhang, W. Zhang, Y. Lv, W. Liu, and Q. Wang, "Unified power quality conditioner with model predictive control," *in Proc. 5th Int. Conf. Comput. Sci. Educ.*, pp. 1239–1244, Aug. 24–27, 2010.

[75] Y. Kolhatkar, R. Errabelli, and S. Das, "A sliding mode controller based optimum UPQC with minimum VA loading," *in Proc. Power Eng. Soc. Gen. Meet.*, pp. 871–875, Jun. 12–16, 2005.

[76] B. H. Kwon, T. W. Kim, and J. H. Youm, "A novel SVM-based hysteresis current controller," *IEEE Transactions on Power Electronics*, vol.13, no.2, pp.297-307, Mar. 1998.

[77] H. Akagi, "New trends in active filters for power conditioning," *IEEE Transactions Industrial Applications*, vol. 32, no. 6, pp. 1312-1322, Dec.1996.

[78] H. Akagi "Trends in Active Power Line Conditioners" *IEEE Transactions on Power Electronics*, vol.9, no.3, pp. 263-268, May. 1994.

[79] S. Bhattacharya and D. M. Divan, "Hybrid series active/parallel passive power line conditioner with controlled harmonic injection," U.S. Patent 5 465 203, Nov. 1995.

[80] J. H. Choi, G. W. Park, and S. B. Dewan, "Standby power supply with active power filter ability using digital controller," *in Proc. IEEE APEC'95*, pp. 783–789, 1995.

[81] A. Chaoui, J. P. Gaubert, F. Krim and L. Rambault, "On the Design of Shunt Active Filter for Improving Power Quality" *IEEE International symposium on Industrial Electronics*, pp.31-37, July. 2008.

[82] K. K. Mahapatra, "Active Harmonic current compensation using Hard and soft-switched Inverters" *Thesis for the degree of Doctor of Philosophy, Indian Institute of Technology-Kanpur*, June. 1999.

[83] Arun karuppaswamy. B, "Synchronous Reference Frame Strategy based STATCOM for Reactive and Harmonic Current Compensation" *Thesis for the degree of Master of Technology, National Institute of Technology-calicut*, June. 2007.

[84] S. K. Jain and P. Agarwal, "Design Simulation and Experimental investigation on a shunt active power filter for harmonics, and reactive power compensation," *Electric Power Components and Systems*, vol.31, no.7, pp. 671-692, July. 2003.

[85] S. J. Chiang and J.M. Chang, "Design and Implementation of the parallelable active power filtre," *Proc. 30th Annual IEEE Power Electr. Specialists Conference (PESC-99)*, vol.1, pp. 406-411, Jul. 1999.

[86] S. Ponnaluri and A. Brickwedde, "Generalized System Design of Active filters," *IEEE Conference on PESC*, Jun. 2001.

[87] R. K. Patjoshi and K. K. Mahapatra,"New control strategy of unified power quality conditioner with sliding mode approach," *India Conference (INDICON), 2013 Annual IEEE*, pp.1-6, 13-15 Dec. 2013.

[88] A. Ferrero and G. S. Furga, "A new approach to the definition of power components in three-phase systems under non-sinusoidal conditions*"IEEE Transactions on Instrumentation and Measurement*, vol. 40, pp. 568–577, Jun. 1991.

[89] H. Akagi and A. Nabae, "The p-q theory in three-phase systems under non-sinusoidal conditions," Eur. Trans. Elect. Power Eng., vol. 3, no. 1, pp. 27–31, Feb. 1993.

[90] Z. Zhou, Y. Liu, "Pre-sampled data based prediction control for active power filters," *International Journal of Electrical Power and Energy Systems*, vol.37, pp.13–22, 2012.

[91] R. K. Patjoshi, K. K. Mahapatra and V. R. Kolluru, "Real time Implementation of Sliding mode Based Direct and Indirect Current Control Techniques for Shunt Active Power Filter," *WSEAS Transactions on Systems and Control*, vol.10, no.1, pp. 186-197, 2015.

[92] V. Soares, P. Verdelho, and G. Marques, "Active Power Filter Control Circuit Based on the Instantaneous Active and Reactive Current id–iq Method," *IEEE Power Electronics Specialists Conference* pp. 1096-1101, 1997.

[93] C. H. da Silva, R. R. Pereira and L. E. B. da Silva, "A digital PLL scheme for three-phase system using modified synchronous reference frame," *IEEE Transactions on Industrial Electronics*, vol. 57, no.11, pp. 3814-3821, Nov. 2010.

[94] A. Nabae, S. Ogasawara, and H. Akagi, "A Novel Control Scheme for Current-Controlled PWM Inverters" *IEEE Transactions Industrial Applications*, vol 1A-22, no.4, pp.562-570, Jul. 1986.

[95] J. Zeng, C. Yu, Q. Qi, Z. Yan, Y. Ni, B.L. Zhang, S. Chen and Felix F. Wu "A novel hysteresis current control for active power filter with constant frequency" *Electric Power Systems Research*, vol.68, no.1, pp. 75-82, 2004.

[96] P. Verdelho and G. D. Marques, "An active power filter and unbalanced current compensator," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, pp. 321-328, Jan. 1997.

[97] Mohd Izhar Bin A Bakar, "Active power filter with automatic control circuit for neutral current harmonic minimization technique," *Ph.D thesis*, University of Science, Malaysia, Jun. 2007.

[98] E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmun, J. Bergas-Jané, "A multi objective control strategy for grid connection of DG (distributed generation) resources," *Journal of Energy*, vol.35, no.12, pp.5022-5030, 2010.

[99] P. K. Dash and S. Mishra, "Damping of multimodal power system oscillations by FACTS devices using non-linear Takagi-Sugeno fuzzy controller," *International journal of electrical power & energy systems,* vol. 25, no.6, pp. 481-490, 2003.

[100] D. Fulwani, B. Bandyopadhyay, and L. Fridman, "Non-linear sliding surface: towards high performance robust control," *IET Control Theory Applications*, vol.6, no.2, pp. 235-244, 2012.

[101] B. Bandyopadhyay and D. Fulwani, "High-Performance Tracking Controller for Discrete Plant Using Nonlinear Sliding Surface," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 9, pp. 3628–3637, Sep. 2009.

[102] R. K. Patjoshi and K. K. Mahapatra, "Non-linear sliding mode control with SRF based method of UPQC for power quality enhancement," *Industrial and Information Systems (ICIIS), 2014 9th International Conference*, pp.1-6, 15-17 Dec. 2014.

[103] Y. Pal, A. Swarup and B. Singh, "A comparative analysis of different magnetics supported three-phase four-wire unified power quality conditioners–A simulation study," *International Journal of Electrical Power and Energy Systems*, vol.47, pp.436–47, 2013.

[104] A. Ketabi, M. Farshadnia, M. Malekpour and R. Feuillet, "A new control strategy for active power line conditioner (APLC) using adaptive notch filter," *International Journal of Electrical Power and Energy Systems*, vol.47, pp.31–40, 2013.

[105] H. Vahedi, A. Sheikholeslami, M. T. Bina and M. Vahedi, "Review and Simulation of Fixed and Adaptive Hysteresis Current Control Considering Switching Losses and High-Frequency Harmonics," *Advances in Power Electronics Hindawi*, 2011.

[106] H. Ying, "Constructing Nonlinear Variable Gain Controllers via the Takagi–Sugeno Fuzzy Control," *IEEE Transactions on Fuzzy System*, vol.6, no.2, pp.226–34, 1998.

[107] P. K. Dash, S. Morris and S. Mishra, "Design of a Nonlinear Variable-Gain Fuzzy Controller for FACTS Devices," *IEEE Transactions on Control System Technology*, vol.12, no.3, pp.428–38, May. 2004.

[108] S. Ozcelik and H. Kaufman, "Robust Direct Model Reference Adaptive Controllers," *34th Conference on Decision & Control*, pp.3955–60, 1995.

[109] P. K. Dash and S. Mishra, "Damping of multimodal power system oscillations by FACTS devices using non-linear Takagi-Sugeno fuzzy controller," *International Journal of Electrical Power and Energy Systems*, vol.25, no.6, pp.481–90, 2003.

[110] S. C. Tan, Y. M. Lai and C. K. Tse, "Implementation of pulse-width-modulation based sliding mode controller for boost converters," *IEEE Power Electronics Letters*, vol.3, no. 4, pp.130-135, Dec. 2005.

[111] W. Yan, J. Hu, V. Utkin and L. Xu, "Sliding Mode Pulse width Modulation," *IEEE Transactions on Power Electronics*, vol.23, no.2, pp.619-626, Mar. 2008.

[112] R. J. Wai, "Fuzzy Sliding-Mode Control Using Adaptive Tuning Technique," *IEEE Transactions on Industrial Electronics*, vol.54, no.1, pp.586-594, Feb. 2007.

[113] F. Barrero, A. Gonzalez, A. Torralba, E. Galvan and L. G. Franquelo, "Speed control of induction motors using a novel fuzzy sliding-mode structure," *IEEE Transactions on Fuzzy Systems*, vol.10, no.3, pp.375-383, Jun. 2002.

[114] S. Sastry and M. Bodson, "Adaptive control: stability, convergence and robustness," *Courier Corporation*,2011.

[115] W. S. Levine, "The control handbook," *CRC press*, 1996.

[116] P. S. Maybeck, "Stochastic models, estimation, and control," *Academic press*, 3rd ed. 1982.

[117] B. R. Lin, and Y. L. Hou, "Single-phase integrated power quality compensator based on capacitor-clamped configuration," *IEEE Transactions on Industrial Electronics,* vol.49, pp. 173–185, Feb. 2002.

[118] H. Hossein, and A. H. Moghadasi, "Optimization scheme in combinatorial UPQC and SFCL using normalized simulated annealing," *IEEE Transactions on Power Delivery,* vol.26, no.3, pp.1489-1498, Jul. 2011.

[119] T. E. Nunez-Zuniga, and J. A. Pomilio, "Shunt active power filter synthesizing resistive loads," *IEEE Transactions on power Electronics,*, vol. 17, no. 2, pp. 273–278, Mar. 2002.

[120] M. Basu, S. P. Das, and G. K. Dubey, "Parallel converter scheme for high-power active power filters," *IEE Proceedings Electric Power Applications*, vol. 151, no. 4, pp. 460–466, Jul. 2004.

[121] P. A. Ioannou and J. Sun, "Robust adaptive control," *Courier Corporation*, 2012.

[122] LEM, \Voltage Transducer LV 25-P," Datasheet.

[123] LEM, \Current Transducer LA 55-P," Datasheet.

[124] K. K. Shyu, "Design and implementation of high performance shunt active power filter systems" *Thesis for the degree of Doctor of Philosophy, National central university - Taiwan*, 2006.

[125] M. K. Mishra, K. Karthikeyan, G. Vincent and S. Sasitharan, "A DSP based integrated hardware set up for a DSTATCOM; Design, development and implementation issues," *IETE Journal of Research*, vol. 56, no. 1, pp. 11-21, 2010.

[126] *NI CompactRIO concepts manual.*

[127] *NI 9201 Operating Instructions manual.*

[128] *NI 9263 Operating Instructions manual.*

[129] Michael Barr., "Embedded Systems Glossary," *Netrino Technical Library*.

[130] P. A. Ioannou and B. Fidan, "Adaptive control tutorial," *Society for Industrial and Applied Mathematics Philadelphia*, 2006.

THESIS DISSEMINATIONS

Journal Papers

(1) R. K. Patjoshi, K. K. Mahapatra, and V. R. Kolluru, "Real-time Implementation of Sliding mode Based Direct and Indirect Current Control Techniques for Shunt Active Power Filter," WSEAS Trans. on Systems and Control, vol. 10, no. 1, pp. 186–197, 2015.

(2) R. K. Patjoshi, K. K. Mahapatra, "Performance Enhancement of Unified Power Quality Conditioner Using Command Generator Tracker based Direct Adaptive Control Strategy," IET Power Electronics (Accepted).

(3) R. K. Patjoshi, K. K. Mahapatra, "High Performance Unified Power Quality Conditioner using Nonlinear Sliding Mode and New Switching Dynamics Control Strategy," IET Power Electronics (Revised copy submitted).

(4) R. K. Patjoshi, K. K. Mahapatra, "A New Reference Signal Extraction Approach in a Fuzzy Sliding mode Based Unified Power Quality Conditioner," Electric Power Components and Systems (Taylor & Francis) (Revised copy submitted).

Conference Papers

(1) R. K. Patjoshi, K. K. Mahapatra, "Non-linear sliding mode control with SRF based method of UPQC for power quality enhancement," 9th IEEE International Conference on Industrial and Information Systems (ICIIS),Gwalior, 15-17 Dec. 2014.

(2) R. K. Patjoshi, K. K. Mahapatra, "New control strategy of unified power quality conditioner with sliding mode approach," India Annual IEEE Conference (INDICON'13), Mumbai, 13-15 Dec. 2013.

(3) R. K. Patjoshi, K. K. Mahapatra, “Performance comparison of direct and indirect current control techniques applied to a sliding mode based shunt active power filter," India Annual IEEE Conference (INDICON’13), Mumbai,13-15 Dec. 2013.

(4) R. K. Patjoshi, K. K. Mahapatra ,"Performance analysis of shunt active power filter using PLL based control algorithms under distorted supply condition," IEEE Students Conference on Engineering and Systems (SCES’13), Allahabad, 12-14 Apr. 2013.

Appendix-1

Table.A.1. Simulated test system data

System	Parameters	Notation	Value
Source	Voltage, Frequency, Resistor, Inductor	V_{sabc}, f, R_s, L_s	$360V$ (P-P),50 Hz, 1Ω,$0.1mH$
Load	Diode rectifier, Resistor, Inductor	R_L, L_L	6-diode, 42Ω,35 mH
DC Link	Reference voltage, Capacitor	V_{dc_ref}, C_{dc}	$630V$,$4000\mu F$
Shunt converter	(Interface inductor ,resistor) and Switching frequency	(L_{shf}, R_{shf}), f_{sw}	($2.1mH$, 0.1Ω) $10kHz$
Series converter	AC filter inductor and capacitor	(L_{sef}, C_{ef}, R_{sef})	$2.1mH$,$6\mu F$ and 2Ω
	Transformer specification and inductance	L_j	$4mH$
Enhanced PLL	Proportional-integral gain Feed-forward compensator parameter	kp, ki x, α	0.04, 0.02 0.01, 100
Modified PLL	$k_p = 8.0$ and $k_i = 0.044$		
NVGF controller for DC-link voltage regulation	$K_p = 0.3535$ $K_i = 12.50$, $K_e = 0.028$, $a_1 = 0.7070$, $a_2 = 25$ and $a_3 = 0.056$		
NVGF Hysteresis band for shunt inverter	$\delta = 0.707, \omega_n = 56.5771, K_p = 0.068, K_i = 6.722, Z_c = 0.0101,$ $a = 0.1360, b = 13.44\, and\, c = 0.0202$		
NVGF Hysteresis band for series inverter	$\delta = 0.707, \omega_n = 10kHz, \alpha = 20e-5, K_p = 0.20, K_i = 2.40, Z_c = 0.083,$ $a = 0.40, b = 4.80\, and\, c = 0.16$		

Appendix-2

The design of PI-controller for compensation the losses present in RLC filter and series transformer is based on plant transfer function $G_p(s)$ and PI-compensator transfer function $G_i(s)$.

$$G_p(s) = \frac{1}{s^2 L_{sf} C_f + (R_{sf} s C_f + R_g C_f)s + 1}$$

$$G_i(s) = k_p + \frac{K_i}{s}$$

The closed-loop transfer function $G_c(s)$ of the above equation is

$$G_c(s) = \frac{s + \frac{k_i}{k_p}}{s^3 + \frac{(R_{sf} + R_g)s^2}{L_{sf}} + \frac{(k_p + 1)}{L_{sf} C_f} s + \frac{k_i}{L_{sf} C_f}}$$

Based on desired characteristics polynomial $\left(s^2 + 2\delta\omega_n s + \omega_n^2\right)\left(s + \alpha\omega_n\right)$, k_p and k_i are found to be

$$k_p = L_{sf} C_f (1 + 2\alpha\delta)\omega_n - 1 \text{ and } k_i = \alpha L_{sf} C_f \omega_n^3$$

where ω_n is the natural frequency, α is constant and σ is the damping coefficient.

Appendix-3

The design of PI-controller gain, meant for hysteresis band calculation of series inverter is based on plant transfer function $G_p(s)$ and PI-compensator transfer function $G_i(s)$.

$$G_p(s) = \frac{1}{s^2 L_f C_f + R_f C_f s + 1}$$

where R_f is the internal resistance of filter inductance.

$$G_i(s) = k_p + \frac{K_i}{s}$$

The closed-loop transfer function $G_c(s)$ can be represented by the following equation.

$$G_c(s) = \frac{s + \frac{k_i}{k_p}}{s^3 + \frac{R_f}{L_f} s^2 + \frac{(k_p + 1)}{L_f C_f} s + \frac{k_i}{L_f C_f}}$$

Based on desired characteristic polynomial $\left(s^2 + 2\delta\omega_n s + \omega_n^2\right)\left(s + \alpha\omega_n\right)$, k_p and k_i are found to be

$k_p = L_f C_f (1 + 2\alpha\delta)\omega_n^2 - 1$ and $k_i = \alpha L_f C_f \omega_n^3$

where ω_n is the natural frequency, α is constant and σ is the damping coefficient.

Appendix-4

System Parameters for simulation and experimental set-up

Table A.2 List of parameters used in simulation and experimentation for single phase UPQC system

Parameters	Experimental Values
Supply voltage/ frequency	100 V/50 Hz
Resistor (R_L) and Capacitor (C_L)	$120\,\Omega$,$220\ \mu F$
LC low pass filter (L_{se} ,C_{ef})	5 mH, $6\ \mu F$
Interface inductor L_{sh}	3 mH
DC-link capacitance (C_{dc})	4700 μF
Reference voltage (V_{dcref})	220 V
Voltage source inverter	SKM75GB063D IGBT module, TLP-250 for Gate driver circuit, Amplifier circuit, Separate Power supply for driver circuit.
Sensors	LEM make LV25-P for phase voltage, LA55-P for current transducer.

Appendix-5

NI cRIO-9014

Table A.3 Processor Datasheet

Network	
Network Interface	10 Base T and 100 Base TX Ethernet
Compatibility	IEEE 802.3
Communication Rates	10 Mbps, 100 Mbps, auto-negotiated
Maximum Cabling Distance	100 m/segment
SMB Connector	
Output Characteristics	
Logic High	3.3 V
Logic Low	0 V
Driver Type	CMOS
Sink/Source Current	± 50 mA
3-state output leakage current	± 5 µA
Input Characteristics	
Maximum Input level	-500 mV
Maximum input low level	990 mV
Minimum input high level	2.31 V
Maximum input level	5.5 V
Input capacitance	2.5 pF
Resistive strapping	1 kΩ to 3.3 V
USB Port	
Maximum data rate	12 Mb/s
Maximum current	500 mA
Memory	
cRIO-9014	2 GB
DRAM	
cRIO-9014	128 MB
Internal Real-Time Clock	
Recommended power supply	48 W secondary, 18 V DC to 24 V DC
Power Consumption	
Controller only	6 W
Controller supplying power to eight CompactRIO modules	20 W
Power Supply	
On Power	9 to 35 W
After power up	6 to 35 V
Safety Voltages	
V-to-C	35 V max

Table A.4 Input Modules NI 9201

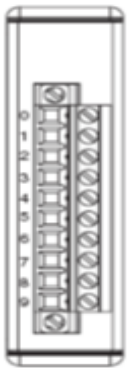
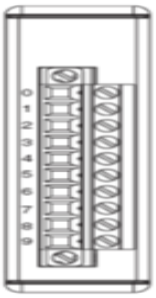
Module	Terminal	Signal
	0	AI0
	1	AI1
	2	AI2
	3	AI3
	4	AI4
	5	AI5
	6	AI6
	7	AI7
	8	NO CONNECTION
	9	COM

Table A.5 Output Module NI 9263

Module	Terminal	Signal
	0	AO0
	1	COM
	2	AO1
	3	COM
	4	AO2
	5	COM
	6	AO3
	7	COM
	8	NO CONNECTION
	9	COM