Doping Dependent Subthreshold Swing Modelling of Quadruple Gate MOSFETs

A dissertation submitted in partial fulfillment of requirement for the Degree of

Bachelor of Technology in Electronics and Instrumentation Engineering

and

Master of Technology in V.L.S.I. Design and Embedded Systems

submitted by

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710EC2090

to

Department of Electronics and Communication Engineering
NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA (INDIA)

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June 1, 2015

Certificate

This is to affirm that the work presented in the thesis entitled *Analytical Subthreshold Swing Modelling of Quadruple Gate MOSFETs* by **Tuhinansu Gourav** is a record of genuine research work carried out by him, under my supervision and guidance in partial fulfilment of the requirements for the award of the degree of Master of Technology with the specialization of V.L.S.I. Design and Embedded System in the department of Electronics and Communication Engineering, National Institute of Technology, Rourkela. Neither this thesis nor any part of it has been submitted for any degree or academic award elsewhere.

Place: NIT Rourkela
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Abstract

MOSFET scaling has undergone a drastic change in the size and packing density in the recent years and new methods of improvising the performance of the device being introduced every year. Many ingenious techniques have been used to model the device and its properties. There are many to model the same device parameter. So it is upto the designer's requirement to choose the method that is suitable for him. Some methods give more accuracy but take very large computational time where as some may provide results with less accuracy but provide results faster. Here in this thesis we have brought a balance between the two, i.e. the methodology used here is simple but very efficient in providing results to very satisfactory levels.

A potential function has been developed for a quadruple gate MOSFET by introducing the concept of effective number of gates (ENGs). In this ENGs concept the quadruple gate MOSFET is broken into 2 double gate MOSFETs and so the need to solve large 3-D equations nullifies. The 2-D potential function in the channel is assumed to be parabolic in nature and the 2-D Poission's equation has been solved to obtain the channel potential function. After introducing the concept of ENGs the 3-D structure has been successfully modelled into a 2-D structure. This is the main advantage of this technique. Then the subthreshold swing parameter is obtained by the concept of effective conduction path. Finally after the device has been modelled the effect of variation of device parameters on subthreshold swing is analysed. The device parameters that have been considered for variation are device channel length, oxide thickness, channel thickness, drain to source voltage, channel doping.

ATLAS^{TM} has been used for obtaining the simulation results and validated against the modelling results obtained with the help of MATLAB^{TM}. Both the results have been plotted together and their level of matching in observed and analysed.

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List of Symbols

Symbol	Description
n_i	Intrinsic carrier concentration
T	Temperature in kelvin
L	Device channel length
d_{eff}	Effective conduction path
ε_{ox}	Permittivity of gate oxide
V_{bi}	Built-in voltage
t_{ox}	Gate oxide thickness
t_{si}	Device channel thickness
W	Quadruple Gate MOSFET channel width
H	Quadruple Gate MOSFET channel depth
V_{fb}	Flat-band voltage
V_{DS}	Drain to source voltage
V_G	Gate voltage
$\psi(x, y)$	Device channel potential function
λ	Characteristic length of the device
ψ_{VC}	Virtual Cathode potential
d_{eff}	Effective conduction path
S	Subthreshold swing

CHAPTER 1

Introduction

This chapter is introductory chapter to this thesis. In this chapter we describe various types of semiconductors and explain various terms briefly associated to our device. We also present the scaling theory and its various types. Then a section has been provided for the short channel effects and explained them. Finally towards the end of the chapter we present the evolution of the architecture of MOSFETs.

1.1 Semiconductors and its various associated concepts

1.1.1 Types of Semiconductors

- Semiconductors can be differentiated based on impurity concentration as 2 major types namely intrinsic type semiconductor or extrinsic type semiconductor.
  - Intrinsic semiconductors are very pure form of the element or compound with the number of electrons or holes in conduction band and valence band being very small and exactly equal. Their electrical conductivity is very poor and is a function of temperature alone. As shown in figure1.1 is a pure silicon crystal and an intrinsic semiconductor.
  - Extrinsic semiconductors are formed by adding small amount of impurities to the original crystal structure of pure semiconductors. An excess of conducting particles, either electrons or holes, are always present and increase the conductivity of the device drastically. As shown in figure 1.2, n type semiconductor, silicon crystal doped with phosphorous atoms, and p type semiconductor, silicon crystal doped with boron atoms, are examples of extrinsic type of semiconductors. The electrical conductivity is a function of both temperature and impurity concentration.
    The method of introducing impurities to the semiconductor material is termed as doping.

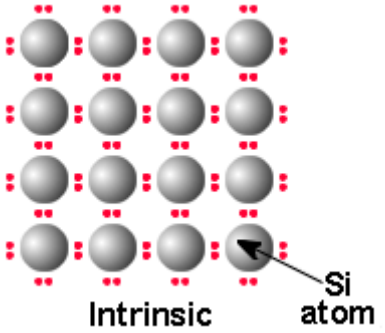

Figure 1.1: Intrinsic type semiconducors

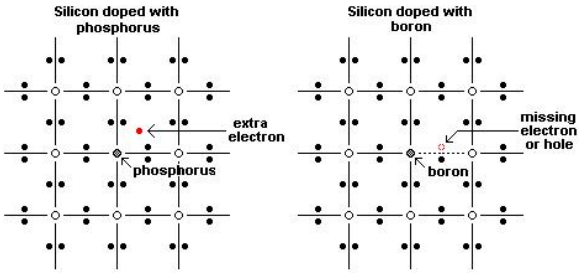

Figure 1.2: Extrinsic type semiconducors

- Semiconductors can be differentiated based on type of impurity present or majority carrier as n-type or p-type semiconductor.

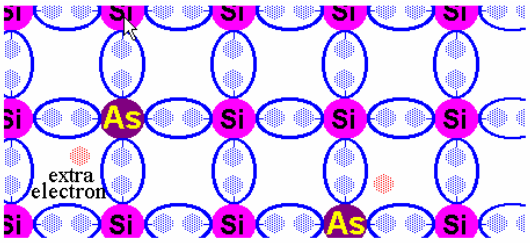

Figure 1.3: n-type semiconductor made by doping Arsenic in silicon

  - n-type semiconductors are formed when a semiconductor is doped with an element or a compound with 5 valence electrons. Four bonds shall be made with the silicon atom but there will be an extra electron that can move through the crystal freely. This gives rise to extra mobility of electrons in n-type semiconductors. As shown in figure 1.3 a n-type semiconductor is formed by doping Arsenic in Silicon giving rise to an extra free electron.
  - p-type semiconductors are formed when a semiconductor is doped with an element or a compound with 3 valence electrons. Three bonds shall be made

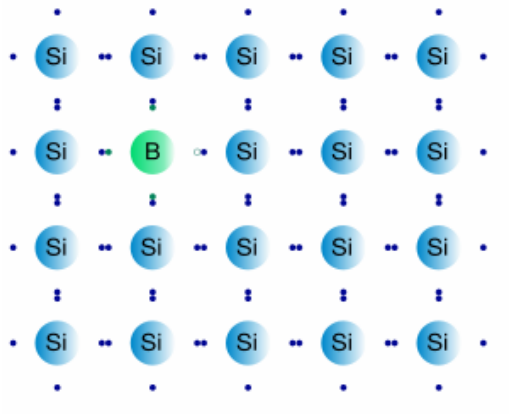

Figure 1.4: p-type semiconductor made by doping Boron in silicon

with the silicon crystal but there will be a extra hole that can move through the crystal freely. This gives rise to extra mobility of holes in p-type semiconductors. As shown in figure 1.4 a n-type semiconductor is formed by doping Boron in Silicon crystal lattice. But boron can form bonds with 3 of the four electrons that a silicon atom is in need of, each silicon atom is left with an associated hole.

1.1.2 Electron affinity

Electron affinity is referred to as the amount of energy released or energy change (in $kJ/mole$) of a neutral atom when an extra electron is added to it forming a negetive ion.

1.1.3 Fermi Level

The Fermi level represents the energy level of an electron such that the statistical probability of finding an electron in this energy level at equilibrium shall be 50%. The Fermi level may not always imply to an actual existing energy level (as for the case of an insulator, the Fermi energy level will be present in the energy band gap).

The Fermi–Dirac distribution function $f(\epsilon)$ is a function that is used to find out the probability of occupancy of an electron (at thermodynamic equilibrium) having an energy ϵ. In other words, it represents the total number of electrons that may occupy the given energy state under the constrain that has been imposed by the very Pauli exclusion principle :

$$f(\epsilon) = \frac{1}{\exp\left(\frac{(\epsilon-\epsilon_F)}{kT}\right) + 1}$$

Here, T represents the temperature in absolute scale and k represents the Boltzmann's constant. From the above equation we observe that there is a energy level at the Fermi energy level ($\epsilon = \epsilon_F$) that this energy state will have a 50% probability of being occupied by electron at any period of time.

1.1.4 Work fuction

The work function can be defined as the amount of voltage required to remove an electron from the fermi energy level to vacuum energy level. It is a surface property and depends on crystal face and impurities.
Flat band voltage is the amount of voltage required to be applied at the gate terminal produce a flat energy band throughout the semiconductor.

$$V_{FB} = \phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x dx$$

where ρ_{ox} is charge density inside the oxide region.

1.1.5 Drift Current

- The displacement of mobile charged carriers in the presence of the available electric field is known as drift.
- Travel direction of charge carriers
  - Holes will always tend to travel in the direction of the available electric field (from $+ve$ to $-ve$)
  - Electrons will always tend to travel in the direction opposite to the available electric field (from $-ve$ to $+ve$)
- Here movement of mobile charge carriers will be highly non-directional in the macro scale, but will have a net direction of motion in the macroscopic scale.
- The overall net movement is dictated by the drift velocity, v_d with units $cm/second$
- The overall movement of mobile charged carriers will give rise to the total current.
- The total current density J ($I = J * Area$) that flow in the semiconductor device with the area A under the force of the electric field E, one of the component of J due to drift of carriers will be:
  Hole drift current density

  $$J_p|_{Drift} = qpv_d$$

  and
  Electron drift current density

  $$J_n|_{Drift} = qnv_d$$

- At low values of electric field, $J_p = qp\mu_p E$ and $J_n = qn\mu_n E$
  where μ represents the "mobility" in the semiconductor device and is a measure of the ease with which the carriers will be able to travel through the crystal. $[\mu] = \frac{cm^2}{V.Second}$
- The total drift current obeys Ohm's Law.

1.1.6 Diffusion Current

- The movement of charged particles due to difference in concentration of charged carriers is termed as diffusion. Charged carriers flow from higher concentration region to lower concentration regions. Ficks law expresses the diffusion current as the flux, F, (of particles in our case) is directly proportional to the concentration gradient in the device.

  $$F = -D\nabla\eta$$

  where, η represents the concentration and D represents the diffusion coefficient.

- For the charge carriers, electrons and holes, the total diffusion current density (flux of particles times $\mp q$) can be represented as,

  $$J_p|_{Diffusion} = -qD_p\nabla p$$

  or

  $$J_n|_{Diffusion} = qD_n\nabla n$$

  The point here to be noted is the opposite sign for electrons and holes.

- The diffusion current does not obey Ohm's Law

1.1.7 Debye length

Debye length represents the radius of sphere, known as debye sphere, outside whose volume the electrical charges are screened from the influence.

1.1.8 Effect of Gate-Body Voltage on Surface condition

1. Flatband Condition
   A semiconductor may not be neutral everywhere due to presence of contact potential and net effective interface charges. These net effective interface charges consists of 4 parts :

   - Charges due to presence of non zero potential value between the gate oxide material and the substrate, an effective concentration of charges will appear on both of the sides oxide.
   - Oxide fixed charges exists very close to the oxide-semiconductor interface due to the mechanism of oxide formation at the time of such formation. These charges are independent of oxide thickness, body doping, and doping concentration.
   - Oxide trapped charges can exists throughout the oxide which can be acquired by radiation, photo-emission, or the injection of high-energy carriers from body.
   - A mobile ionic charge can exists within the oxide due to contamination by alkali ions introduced by the environment during fabrication.
   - An interface trap charge (also called surface-state charge) exists at the oxide-semiconductor interface. It is caused by defects at that interface, which give rise to charge "traps".

An external voltage can be applied between gate and substrate terminals to keep the semiconductor neutral everywhere by cancelling the effects of contact potential and net concentration of charges. This voltage is the flat-band voltage for the MOSFET and is denoted by V_{FB}. Here

$$V_{GB} = V_{FB}, \psi_S = 0$$

2. Accumulation
   If V_{GB} decreases below V_{FB} then holes will start accumulating at the surface to provide a net positive charge. This condition is called accumulation. In accumulation we have
   $$V_{GB} < V_{FB}, \psi_S < 0$$

3. Depletion
   Now if V_{GB} increases above V_{FB} but not much larger then the total positive potential at the surface of the device with respect to device body will simply drives the holes away from the device surface, making it depleted. This condition of the device is called depletion. The charge under the oxide is due to the uncovered acceptor atoms, each of which contributes a charge of -q.
   $$V_{GB} > V_{FB}, \psi_S > 0$$

4. Inversion
   As V_{GB} is further increased, more acceptor atoms are uncovered and ψ_S will become sufficiently positively charged to attract a large number of free mobile electrons to the device surface. Finally, with sufficiently large V_{GB} the density of free electrons will overcome that of holes at the device surface. This situation is opposite from that normally expected in a p-type material, we now have surface inversion.
   $$V_{GB} > V_{FB}, \psi_S > 0$$

1.1.9 Threshold voltage

Qualitatively threshold voltage of a device can be defined as the smallest differential gate voltage that is required to start conduction in the channel. Quantitatively the threshold voltage can be explained as the minimum differential gate potential voltage to create depletion region and any further change in gate voltage will result in change of inversion layer charge. The formation of depletion region and inversion charge layer creation is shown in figure 1.5. Now, if $V_{GS} > V_T$ and V_{DS} is large, then the state after which the amount of inversion layer charge density becomes sufficiently small (ideally zero) at the drain side end of the device is known as pinch-off. The potential value of V_{DS} at pinch-off is represented as $V_{DS,sat}$. After pinch-off, any further increase in the lateral electric field component will be absorbed by the creation of a thin high field region with low charge carrier density.

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_S q N_a \phi_F}}{C_{ox}}$$

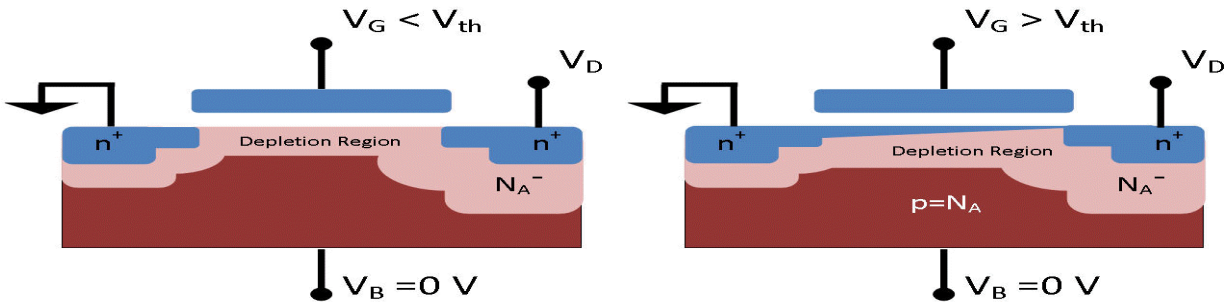

Figure 1.5: Depletion region and inversion charge layer creation

1.1.10 MOSFET modes of operation

MOSFETs can be operated in 3 different modes qualitatively based on the values of potential present at its different terminals : cutoff,subthreshold or weak inversion region, triode region, saturation region.

- If $V_{GS} < V_T$, then no conductive channel will be available and $I_D = 0$, this is known as the cutoff region.
- When $V_{GS} < V_T$ and $V_{DS} < V_{DS,sat}$, the semiconductor device will be in the triode region of device operation. Increasing the value of V_{DS} increases the lateral component of electric field in the device channel, and therefore the current. Increasing V_{GS} will increase the transverse component of the electric field and therefore the amount of inversion layer density, which will also increase the total current.
- When $V_{GS} < V_T$ and $V_{DS} > V_{DS,sat}$, the device will be in the saturation region of device operation. Since channel density at the drain end of the device has become low, the current will be much less depend on the value of V_{DS} , but will be still dependent on the value of V_{GS}, as increased V_{GS} will still increases the inversion layer density.

1.2 Scaling

The process of reducing a particular key dimension of a device, from one technology generation to the next, is termed as scaling. This has led to an ever increase in speed and circuit complexity per unit of chip area, and decrease in cost per transistor and cost per circuit function. Today scaling down of certain dimensions has almost reached its limits, for example, scaling down oxide thickness greatly increases dc gate leakage. Thus new technologies needs to be applied with the classical scaling scenarios.

1.2.1 Classical Scaling

1.2.1.1 Constant-field scaling

The process of scaling in which internal electric field shape and maximum magnitude of the scaled device is same as the in the original device is known as constant-field scaling.

Quantity	Scaling factor
Device dimensions	$\frac{1}{\kappa}$
Area	$\frac{1}{\kappa^2}$
Packing density (devices per unit of chip area)	κ^2
Doping concentration, N_a	κ
Bias voltage and V_T	$\frac{1}{\kappa}$
Bias currents	$\frac{1}{\kappa}$
Power dissipation for a given circuit	$\frac{1}{\kappa^2}$
Power dissipation per unit of chip area	1
Capacitances, C	$\frac{1}{\kappa}$
Capaciatances per unit area,	κ
Charges, Q	$\frac{1}{\kappa^2}$
Charges per unit area,	1
Electric field intensity	1
Body effect coefficient, γ	$\frac{1}{\sqrt{\kappa}}$
Transistor transit time, τ	$\frac{1}{\kappa}$
Transistor power-delay product	$\frac{1}{\kappa^3}$

Table 1.1: Constant-field scaling

Let a large device is scaled in all three dimensions by a factor of $\frac{1}{\kappa}$, where $\kappa > 1$, the from table 1.1 we find the different quantities and the amount by which they they are scaled.

1.2.1.2 Constant voltage scaling

The scaling technique discussed above has certain problems, in the weak inversion region of the device the device width will not scale. Hence, any voltage swing required for turning the device from off to on may be unacceptably large fraction of the total voltage available. In addition, established device on chip interface specifications should be obeyed for which voltage levels have been fixed, and, therefore the voltage in device doesn't get scaled. The rules that are followed in these cases, for decreasing the device dimensions while still keeping the voltage levels unaffected, is termed as constant voltage scaling.
It is to be expected that high electric fields can become severe under constant-voltage scaling.

1.2.1.3 Quasi-constant-voltage scaling

To avoid extreme cases of constant-field and that of constant-voltage scaling a combination of is made. For example, geometric dimensions and substrate doping are scaled as in constant-field scaling but voltages here are scaled less drastically. This technique is known as quasi-constant-voltage scaling.

Scaling factor				
Quantity	Constant-field scaling $1 < \kappa' < \kappa$	Constant voltage scaling	Quasi-constant-voltage scaling	Generalized scaling
W, L	$\frac{1}{\kappa}$	$\frac{1}{\kappa}$	$\frac{1}{\kappa}$	$\frac{1}{\kappa}$
t_{ox}	$\frac{1}{\kappa}$	$\frac{1}{\kappa'}$	$\frac{1}{\kappa}$	$\frac{1}{\kappa}$
N_a	κ	κ	κ	$\frac{\kappa^2}{\kappa'}$
V, V_T	$\frac{1}{\kappa}$	1	$\frac{1}{\kappa'}$	$\frac{1}{\kappa'}$

Table 1.2: Different Scaling Techniques

1.2.1.4 Generalized scaling

In the above scaling the depletion region width do not get scaled by the same factor as W, L, and t_{ox}. This is avoided if the scaling factor for N_a is modified appropriately resulting in the generalized scaling technique.
Different scaling techniques with their corresponding scaling factors for the device width (W), length(L), oxide thickness (t_{ox}), channel doping (N_a), Voltage(V) and threshold voltage (V_T) are listed in table 1.2.

1.2.2 Modern Scaling

The balance between the needs for low I_{off}, determined by the threshold voltage, and high I_{on} (on-state drive current in digital operation, determined by the supply voltage for a given device size) have kept threshold voltage and supply voltage roughly constant. Fine adjustment of the threshold is the key to balancing the speed-power trade-offs between the different types of technology families. Other areas that are being pursued in modern scaling are

- doping profile engineering (e.g., the introduction of halo implants)
- the use of new materials (e.g., the use of hafnium-based gate dielectrics rather than silicon-dioxide, and metals rather than polysilicon gates)
- the use of strain engineering to increase mobility and thus current drive capability
- and the investigation of novel device structures.

1.3 Short Channel Effects

Short-channel effects [1] arise in devices where device channel length becomes comparable or of the same magnitude as that of the depletion widths (xdD, xdS) junctions near the source and drain regions. Under these effects the MOSFETs behave differently from the conventional MOSFETs. As the device channel length L is scaled to improve both the

operational speed and the packing density chip then the effects of short-channel arise. The short-channel effects can arise due to two main reasons:

1. the limitations forced on the electron drift velocity in the device channel,
2. the alteration of the threshold voltage of the device due to the short device channel lengths.

Some of the short channel effects are :

1. Carrier Velocity Saturation
2. Drain-Induced Barrier Lowering
3. Hot-carrier injection
4. Impact Ionization

All the above mentioned effects will be discussed in the next sections.

1.3.1 Carrier Velocity Saturation

When large electric fields are applied in the semiconductor the charge carrier velocity saturates at a maximum value termed as velocity saturation. Generally carrier velocity is directly proportional to the applied electric field, but as electric increases further the carrier velocity does not increase at the same rate as they tend to lose energy through scattering in the deice lattice and phonos or photons are emitted.
So as the device length decreases, the potential per unit length or electric field increases. There is a extend to which this process can be done and at some large electric field value. When the length is small enough, then the velocity of the charge carriers is no longer proportional to electric field and the charged mobile carrier eventually will not be able to move any faster, having already reached its saturation velocity.

1.3.2 Drain-Induced Barrier Lowering

Drain-induced barrier lowering or DIBL [2] is a short-channel effect in MOSFETs referwhichring originally referred to the reduction of the device threshold voltage of the transistor at large drain voltages. The start of the threshold decrease can be explained as a consequence of charge neutrality. The total charge in the depletion region of the device channel will be balanced by mainly the three electrode charges namely gate terminal, source terminal and the drain terminal. As drain voltage will be increased further, the depletion region in the p-n junction between the drain region and body region will increase in range and will extend under the regions of the gate, so the drain takes the responsibility of mostly balancing depletion region charge, leaving only a smaller burden on the gate. This results in the charges available on the gate terminal to maintain the charge balance by bringing more mobile charged carriers into the device channel. This is an effect which is same as to lowering the threshold voltage of the device. As a result, the device channel will become more alluring for the electrons. So the total potential energy barrier for charged carriers or electrons in the device channel will be lowered. So the word "barrier lowering" has been used to term this effect.

1.3.3 Hot-carrier injection

Hot carrier injection (HCI) is an effect in which mobile charged carriers gain enough kinetic energy to cross the potential barrier of the oxide and sometimes get trapped in the interface, thereby permanently damaging the transistor.

1.3.4 Impact Ionization

Impact ionization [3] is the method in which the energetic mobile charge carriers create additional charge carriers. Charge carriers with large enough kinetic energy can strike an electron hole pair and create and electron hole pair. Large kinetic energy can be obtained by large elcric field. If the electron and hole generated have sufficient kinetic energy then it can result in avalanche breakdown.

1.4 Subthreshold Swing

Subthreshold swing (S) [4], [5] of a device is defined by the amount of gate voltage that needs to be applied to change the drain current by 1 decade. It is also defined by the inverse of the subthreshold slope. It has a unit of $[mV/decade]$. Generally we need to minimise the subthreshold swing to have a better channel control. i.e. for example $\frac{I_{on}}{I_{off}}$, that gives us the leakage performance parameter and less energy wastage.
Subthreshold swing is given by

$$S = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right)$$

where C_d =depletion layer capacitance C_{ox} =gate-oxide capacitance
The minimum value of the subthreshold swing is obtained by putting $C_{ox} \to \infty$ at room temperature of $T = 300K$. A device which corresponds to a high value of subthreshold slope exhibits a faster transition between off state and on state currents and is suitable of switching applications.

1.5 Evolution of architecture of MOSFETs

MOSFETs have a rich history. Starting from planar device structures, MOSFETs have gone a long way. Now a days heavy research is going on all around the world to make even better performance for the device. Various variations to the device structure, material etc. are done, experimentation and observations are reported and conclusions are made. In this section we will briefly go through each of the device.

1.5.1 Planar SOI MOSFETs

Silicon on insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance. Their are basically two types of SOI MOSFETs

1. Partially Depleted SOI MOSFETs

2. Fully Depleted SOI MOSFETs

Figure 1.6 shows the structures of the PD-SOI and FD-SOI MOSFETs. Table 1.3 shows the difference between the two.

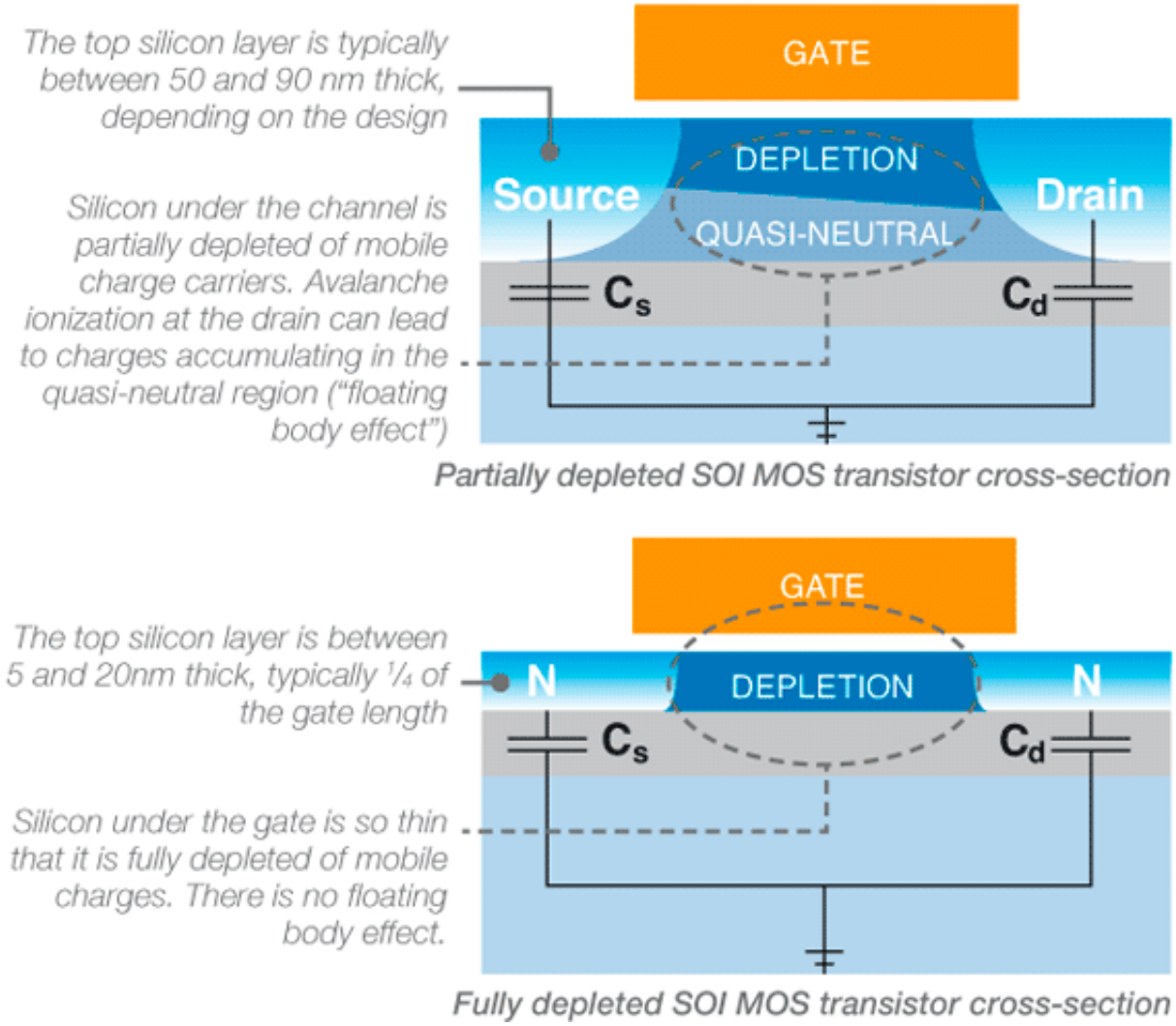

Figure 1.6: The 2 types of Depleted SOI MOSFETs

1.5.2 Finfet MOSFET

The term FinFET [6], [7], [8] is used to describe a nonplanar, double-gate transistor built on an SOI substrate to mitigate the effects of short channels and reduce drain-induced barrier lowering. The "fin" refers to the narrow channel between source and drain. A thin insulating oxide layer on either side of the fin separates it from the gate. Figure 1.7 shows the device structure of a Doublegate FinFET.

Type	Structural Differences	Target Applications	Advantages	Challenges	Nodes
PD-SOI	• Doped channel • Top silicon 50 to 90nm thick (or more for "thick SOI" applications) • Insulating BOX layer is typically 100 to 200nm thick	• High performance microprocessor • Most others (embedded, analog, RF, automotive, power, military, aerospace, etc)	• Well understood • Industrially proven • Easy to manufacture • Can leverage floating for performance gain or memory applications	• Pysical limits to scalability are approaching for high-performance	• 180nm to 22nm
FD-SOI	• Often uses undoped or lightly doped channel • Top silicon 5 to 20nm thick • Insulating BOX layer may be ultra thin: 5 to 50nm	• High performance microprocessors • Low-power electronics • Ultra-low power	• Leakage and power consumption are drastically reduced • For undoped channels, random fluctuations in V_t are minimized • No floating body effect; easier to control short-channel effects	• New methodology needed to detect defects in very thin layers • V_t defined by gate work function and intrinsic body • Very thin body can be challenging to manufacture and implement performance boosters	• 22nm and beyond for high performance micro processors and low-power electronics • Ultra-low power now at 150nm

Table 1.3: Types of Depleted MOSFETs

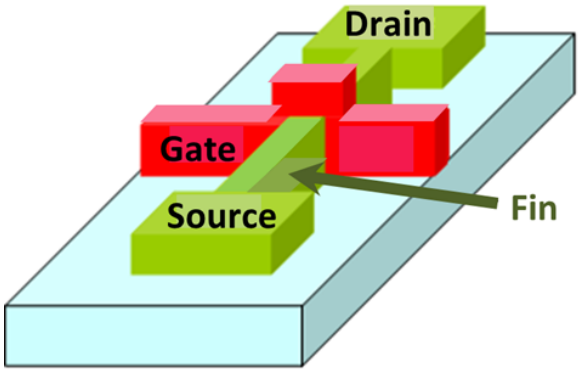

Figure 1.7: Doublegate FinFET structure

1.5.3 Trigate MOSFET

Trigate MOSFETs [9], [10], [11] employ a single gate stacked on top of two vertical gates allowing for essentially three times the surface area for electrons to travel. Tri-gate transistors reduce leakage and consume far less power than current transistors. This allows up to 37% higher speed, or a power consumption at under 50% of the previous type of transistors used.

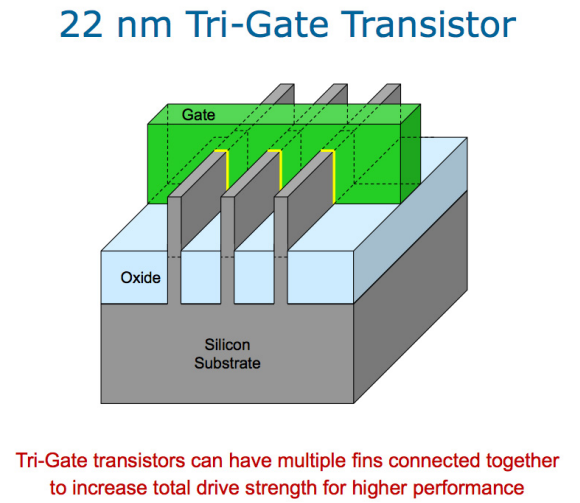

Figure 1.8: Tri-gate MOSFET device structure

1.5.4 Gate all around (GAA) MOSFET

Gate-all-around FETs [12], [13] are similar in concept to FinFETs except that the gate material surrounds the channel region on all sides. Depending on design, gate-all-around FETs can have two or four effective gates. Figure 1.9 shows the device structure of a quadruple gate mosfet and figure 1.10 shows the device structure of a cylindrical gate mosfet.

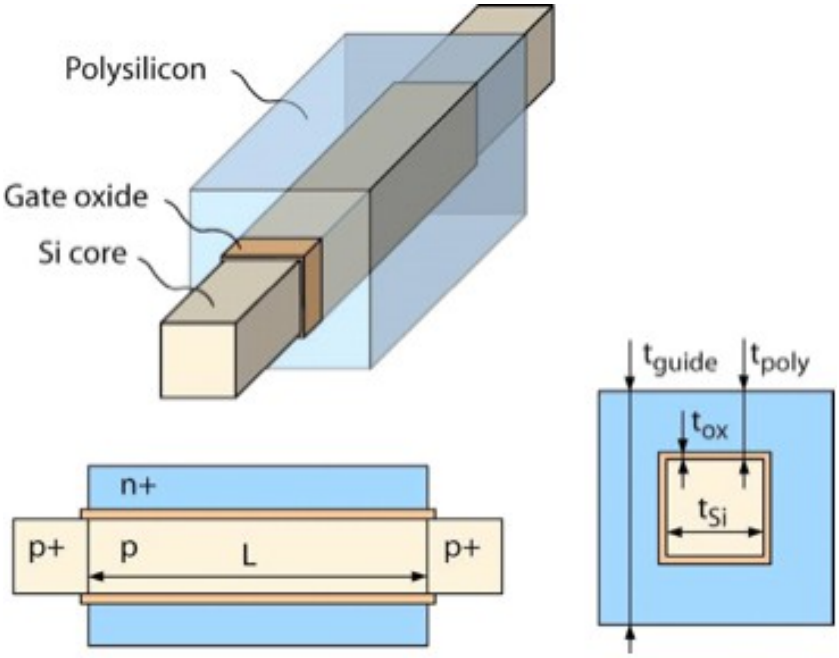

Figure 1.9: Quad-gate MOSFET device structure

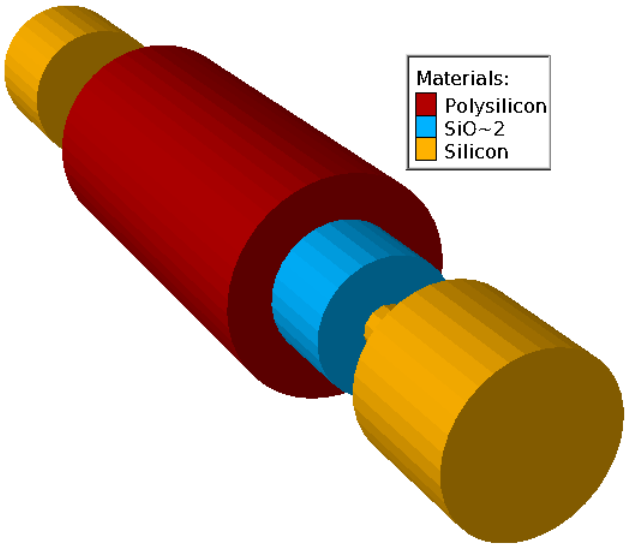

Figure 1.10: Cylindrical gate MOSFET device structure

1.6 Organization

This thesis is organized as follows.

Chapter 1 : This chapter presents a brief description of various terms and concepts used in this thesis, and a short description on evolution of architecture of MOSFETs.

Chapter 2 : This chapter presents the literature review that has been done on dou-

ble gate and quadruple gate MOSFETs. Further the device structure has been discussed followed by the problem statement of the dissertation.

Chapter 3 : This chapter presents the analytical modelling of subthreshold swing using the concept of ENGs and effective conduction path.

Chapter 4 : This chapter presents the results of modelling that are verified against ATLAS^{TM} device simulator.

Chapter 5 : This chapter presents the outcome of the thesis and the future scope.

CHAPTER 2

Literature Review

2.1 Introduction

Here we present the various works done by researchers around the world on multi gate MOSFETs and the new concepts derived by them to model their device. We shall be using some of their concepts for deriving the analytical model equations for our own device. Here we start from the analytical modelling of double gate MOSFETs [14] then move on to higher number of gates, then we put some light on the new concepts developed for solving quadruple gate MOSFETs. Figure 2.1 shows the hierarchy of MOSFETs that have been developed.

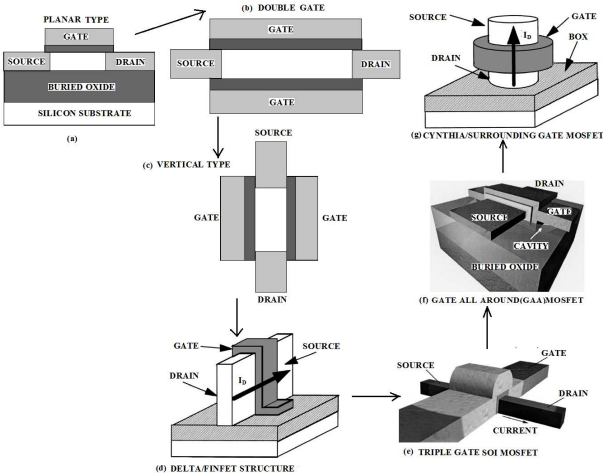

Figure 2.1:Schematic diagram of Multi-Gate MOSFETs

2.2 Multi-Gate MOSFETs

2.2.1 Analytical Modelling of different MOSFETs

2.2.1.1 Double Gate MOSFETs

Pramod Kumar Tiwari, C.R.Panda and other [15] have presented a simple yet efficient 2-D model of subthreshold swing for a symmetric double gate MOSFET by solving 2-D Poisson's equation and parabollic approximation. They have shown the dependency of subthreshold swing (S) on channel doping (N_a), oxide thickness, device channel length, drain to source voltage, channel thickness. They validated the results by comparing their model values with the commercially available ATLAS^{TM} simulation software.
Biswajit Ray and Santanu Mahapatra [16] proposed a new physical and mathematically based on the classical continuous potential distribution function model, specifically considering the device channel at its middle, and for a short-channel with undoped substrate body and symmetrical double-gate (DG) MOSFET. It involved a very classical method for solving the 2-D non-linear Poisson's equation in the rectangular coordinate system. Their model was valid from the weak to the strong inversion regions and ranging from the device channel center till the device surface. They validated, using their present model, that the device channel potential vs gate voltage characteristics for different devices having same channel lengths but varying thickness coincide at a single common point (termed as "crossover point"). Based on their potential function model,they formulated a new compact model for the subthreshold swing (S). They also showed that for the MOSFETs having large short-channel effects (SCE), the effective subthreshold slope was mainly controlled by the potential value close to the device channel middle rather than the space near the device surface. Short Channel Effects and drain-induced barrier lowering (DIBL) were also considered using this newly proposed model and checked with a professional available physical device simulator. Their model showed improvement over the previous models in the regions of low drain voltage subthreshold slope and Short Channel Effect calculation.
Qiang Chen, Bhavna Agrawal, and James D. Meindl [17] analysed a universal mathematical subthreshold swing (S) modelling for symmetric double gate (DG) MOSFETs using the method of evanescent-mode. They explained the doping concentration (N_a) vs subthreshold swing (S) providing all new enhanced S model for undoped Double Gate (DG) MOSFETs. Expressions for device scale length was formulated which project the various specifications of DG MOSFET.

2.2.1.2 FinFET

Abd El Hamid, H and Guitart and others [18] have proposed an mathematical model for undoped FinFET structure in the subthreshold and near-threshold regime. They have solved the 3-D Poisson's equation which also comprise the mobile-charge term. Their analysis show a new subthreshold swing model which has been proposed. The model has been developed on a new physically based analysis for the conduction path in the device. The model results have been verified by 3-D device simulation data and showed a reasonable agreement between the simulation and experimental data.

2.2.1.3 Quadruple Gate MOSFETs

Dheeraj Sharma and Santosh Kumar Vishvakarma [19] have derived a new analytical 3-D potential model in the subthreshold and strong inversion region for the Quadruple gate-all-around (QGAA) MOSFET. They obtained the potential distribution in the subthreshold and strong inversion region of the channel region of a QGAA MOSFET by simultaneously solving the 3-D Laplace equation and the 3-D Poisson's equations. They had assumed potential distribution function to be parabolic along the z-axis in the device channel direction and appropriately matched it with the results of the 3-D device simulator after consideration of z-depended characteristic device length in subthreshold regime. For proper valuation of short channel effects(SCE),they additionally modified electrostatics near source region and drain region. They found out accurate gate-to-gate potential distribution function after considering higher order terms in the approximated parabolic potential profile. They compared the numerical data that they found out from Atlas device simulator with the modelling results. The deviations found in the parabolic potential distribution was due to potential flattening.
Dheeraj Sharma and Santosh Kumar Vishvakarma [20] of quad gate all around (Q-GAA) MOSFETs. They solved 3-D Poission's equation to finf out potential distribution function. They experimented using isomorphic polynomial for potential function. They reported that the subthreshold swing can be enhanced by adding z-dependent characteristics length, and the location of lowest center potential in the device channel by virtual cathode potential.

2.2.1.4 Cylindrical Gate MOSFET

Hamdy Abd El Hamid, Benjamin Iniguez [21] have proposed a mathematical model for threshold voltage, subthreshold swing and DIBL of undoped cylindrical GAA MOSFETs. The model is based on the analytical solution of the 2-D poisson's equation solved in the cylindrical coordinates which comprise the mobile charge term. Using this analytical model, the have analysed the variation of the above mentioned electrical characteristics for the variation in the physical parameters including channel lengths and channel thickness. The model values for their results have been verified with the simulation data obtained from the 3-D numerical simulations for the device.

2.3 Previous Works on Multi Gate MOSFETs

Doyle, Datta [22] have worked on fully-depleted (FD) tri-gate CMOS transistors with 60 nm physical gate lengths on SOI substrates. These devices consisted of a top and two side gates on an insulating layer. These transistors showed almost-ideal subthreshold gradient and excellent Drain Induced Barrier Lowering behaviour, and had drive current characteristics greater than any non-planar devices that were reported so far, for correctly-targeted threshold voltages. They also showed tri-gate devices also demonstrated full depletion at silicon body dimensions approximately 1.5 - 2 times greater than either single gate SOI or non-planar double-gate SOI for similar gate lengths, indicating that these devices are easier to fabricate using the conventional fabrication tools. They also compared tri-gate transistors to conventional bulk CMOS device at the same technology node, and found that these non-planar devices are competitive with similarly-sized bulk CMOS transistors. Furthermore, three-dimensional (3-D) simulations of tri-gate transistors with transistor

gate lengths down to 30 nm showed that the 30 nm tri-gate device remains fully depleted, with near-ideal subthreshold swing and excellent short channel characteristics, suggesting that the tri-gate transistor could pose a viable alternative to bulk transistors in the near future.

Te-Kuang Chiang[23], presented a novel scaling theory for fully depleted, multiple-gate (MG) MOSFET. The scaling theory was derived from the equation for effective number of gates [24] ($ENGs$), $ENG_{QG} = ENG_{DG,1} + ENG_{DG,2}$, where the MG device was broken into two equivalent double gate (DG) transistors working in parallel based on the perimeter weighted-sum method. Numerical device simulation data for drain-induced-barrier-lowering were compared with the model to validate the formula. Using the scaling theory, the minimum effective channel length improvement factor of $\rho_{MG} = 1 - \left(\frac{ENG_{DG}}{ENG_{MG}}\right)^{\frac{1}{2}}$ showed an improvement of up to 30% in the minimum effective channel length for the MG MOSFET in comparison with DG MOSFET. This theory opens up a vast area of simplifying complex 3D equations by converting them into simpler 2D equations.

2.4 Device Structure

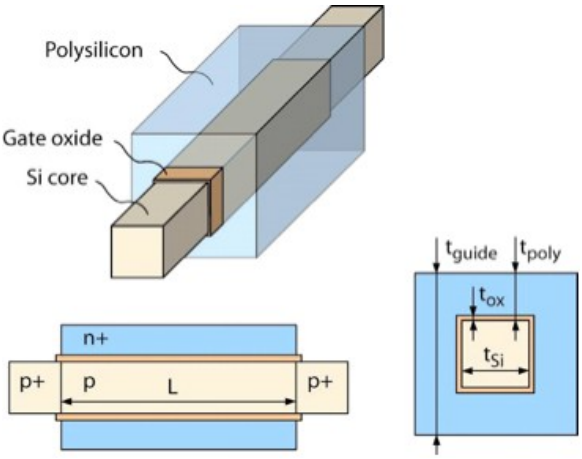

Figure 2.2: Device Structure

Figure 2.2 shows the schematic diagram of our proposed device. The top figure shows the 3-D view of the device and the two bottom figures shows the cross sectional view of the device. In the figure t_{ox} shows the oxide thickness, t_{Si} shows the channel thickness, L shows the device channel length. As shown in the figure the source, channel and the drain are of same thickness and width. Together they form a narrow cuboidal region. The source and the drain are heavy doped where as the channel is lightly doped. The channel is surrounded by gate oxide SiO_2 from the four sides in a rectangular geometry. The gate is further surrounded by polysilicon or metal in a similar rectangular geometry.

2.5 Problem Statement

The study of the effect on subthreshold swing by varying channel doping,device channel length for different channel thickness, oxide thickness, drain to source voltage and effect of effective conduction path with channel doping for various channel length.

CHAPTER 3

Analytical Modelling of Subthreshold Swing

3.1 Introduction

Here in this chapter we will be presenting the detailed methodology used to derive the potential, characteristics length,subthreshold swing parameter of our device. The sections following this one, will each describe one of the parameters derived. Each section will be in continuation to the previous one. All the symbols used have been defined earlier or will be defined thereonly. The concepts that we learnt in the literature survey will be used to model some of the parameters and overall modelling.

3.2 Characteristic Length and Potential Modelling

The device structure of Quadruple Gate MOSFET (QG MOSFET) considered for modelling has been shown in figure 3.1, where t_{ox}, W, H and L are the gate-oxide thickness, the channel width, the channel height and the device channel length respectively. Here we have considered a uniform p-type channel with impurity concentration doping of N_a. Now our objective here is to obtain potential function $\psi(x, y, z)$, we may proceed here first by solving 3D Poisson equation. But it is quite difficult, so instead here, in our method, we will first start by solving 2D Poisson equation and then use Effective number of gates concept to obtain the characteristics length.

$$\frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}} \tag{3.1}$$

The boundary conditions for the DG MOSFET can be obtained from electrical properties of the device, voltage at the source end of the channel, electric field, continuity equation, built-in voltage, and voltage at the drain end of the channel which are as follows :

$$\psi(x,y)_{y=0} = \psi_0(x) \tag{3.2}$$

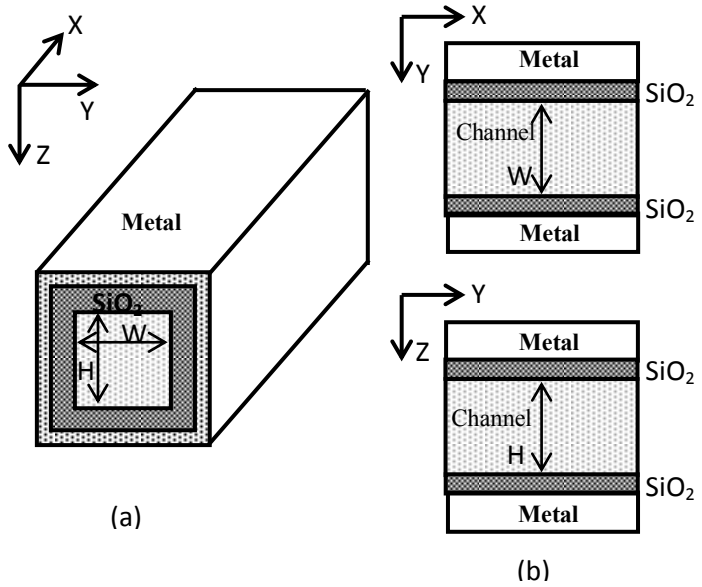

Figure 3.1:
(a)Schematic diagram of a Quadruple Gate MOSFET
(b) $X-Y$ and $Y-Z$ cross-sectional view of the QG MOSFET

$$\left.\frac{\partial\psi(x,y)}{\partial x}\right|_{y=0} = 0 \tag{3.3}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_G - V_f b - \psi\left(x, \pm\frac{t_{si}}{2}\right)\right] = \pm\varepsilon_{si}\left.\frac{\partial\psi}{\partial x}\right|_{y=\pm\frac{t_{si}}{2}} \tag{3.4}$$

$$\psi(0,0) = V_{bi} \tag{3.5}$$

$$\psi(L,0) = V_{bi} + V_{DS} \tag{3.6}$$

Here we shall assume that the 2-D channel potential function to be parabolic approximation and so the resulting function can be expressed as a quadratic equation with 3 unknown constants.

$$\psi(x,y) = C_0(x) + C_1(x)y + C_2(x)y^2 \tag{3.7}$$

Now to find out the constants of 3.7 we will be using the boundary conditions (3.2) and (3.3) in (3.7) and we may obtain

$$C_0(x) = \psi_0(x) \tag{3.8}$$

$$C_1(x) = 0 \tag{3.9}$$

Further, to find out the third constant of 3.7 we will be using (3.4) in (3.7) so that we may obtain

$$C_2(x) = [V_G - V_{fb} - \psi_0(x)]\left[\frac{t_{si}^2}{4}\left(1 + \frac{4\varepsilon_{si}t_{ox}}{\varepsilon_{si}t_{si}}\right)\right]^{-1} \tag{3.10}$$

At this point we have found out all the constants of 3.7 so after substituting the values of C_0, C_1, C_2 obtained above in the original equation of (3.7) we get the 2D channel potential function to be

$$\psi(x,y) = \psi_0(x) + \left(\frac{V_G - V_{fb} - \psi_0(x)}{\lambda_{DG}}\right) y^2 \tag{3.11}$$

where

$$\lambda_{DGj} = \frac{{t_j}^2}{4}\left[1 + \frac{4\varepsilon_{si} t_{ox}}{\varepsilon_{si} t_j}\right]_{(j=1,2)} \tag{3.12}$$

Now from the concepts discussed in literature review MG MOSFET device can be broken into two separate but equivalent DG MOSFET devices working in parallel based on the perimeter-weighted-sum (PWS) method. So now we can replace λ_{DGi} by λ_{QG} that is the characteristics length for Quadruple Gate MOSFETs and it could be written as

$$\frac{1}{\lambda_{QG}} = \frac{1}{\lambda_{DG1}} + \frac{1}{\lambda_{DG2}} \tag{3.13}$$

$$\frac{1}{\lambda_{DG1}} = \frac{8C_{ox}}{4W\varepsilon_{si} + C_{ox}W^2} \tag{3.14}$$

$$\frac{1}{\lambda_{DG2}} = \frac{8C_{ox}}{4W\varepsilon_{si} + C_{ox}H^2} \tag{3.15}$$

Where λ_{DG1}, λ_{DG2} are the natural lengths for both of the DG MOSFETs working in the x-z and y-z planes respectively. W and H are the channel width and height of the QG MOSFET respectively, and C_{ox} is the gate oxide capacitance per unit area of the QG MOSFET.

Now at this point we have converted our QG MOSFET into an equivalent DG MOSFET. So now we can apply all the equation in 2D rather than solving in 3D.
Now applying 2D Poisson's equation at the centre of the resulting device

$$\left.\frac{\partial^2\psi(x,y)}{\partial x^2}\right|_{y=0} + \left.\frac{\partial^2\psi(x,y)}{\partial y^2}\right|_{y=0} = \frac{qN_a}{\varepsilon_{si}} \tag{3.16}$$

Substituting the value of $\psi(x,y)$ from (3.11) in (3.16), we may obtain

$$\frac{\partial^2\psi_0(x,y)}{\partial x^2} - \frac{2}{\lambda_{QG}}\psi_0(x) = \frac{qN_a}{\varepsilon_{si}} - \frac{2}{\lambda_{QG}}(V_G - V_{fb}) \tag{3.17}$$

Using the boundary conditions of (3.5) and (3.6) in (3.17), we obtain the central channel potential function $\psi_0(x)$ as

$$\psi_0(x) = k_1 \exp\left(\sqrt{\frac{2}{\lambda_{QG}}}x\right) + k_2 \exp\left(\sqrt{-\frac{2}{\lambda_{QG}}}x\right) + \left[V_G - V_{fb} - \frac{\lambda_{QG} q N_a}{2\varepsilon_{si}}\right] \tag{3.18}$$

where

$$k_1 = \frac{V_{DS} + \beta_1\left[1 - \exp\left(-\sqrt{\frac{2}{\lambda_{QG}}}L\right)\right]}{\exp\left(\sqrt{\frac{2}{\lambda_{QG}}}L\right) - \exp\left(-\sqrt{\frac{2}{\lambda_{QG}}}L\right)} \tag{3.19}$$

$$\beta_1 = V_{bi} + V_{fb} + \frac{\lambda_{QG} q N_a}{2\varepsilon_{si}} - V_G \tag{3.20}$$

$$k_2 = \beta_1 - k_1 \tag{3.21}$$

3.3 Virtual Cathode Modelling

Now let ψ_{0min} represent the minimum channel potential value of $\psi_0(x)$ at $x = x_{0min}$ i.e. $\psi_{0min} = \psi_0(x_0 min)$ The value of x_{0min} can be obtained by equating the first derivative of $\psi_0(x)$ to 0 i.e. $\left.\frac{d\psi_0(x)}{dx}\right|_{x=x_{0min}} = 0$, which is given by

$$x_{0min} = \sqrt{\frac{\lambda_{QG}}{8}} \ln\left(\frac{k_2}{k_1}\right) \tag{3.22}$$

Now we can obtain the value of ψ_{0min} by substituting the value of x_{0min} from (3.22) in (3.18) which results in

$$\psi_{0min} = 2\sqrt{k_1 k_2} + V_G - V_{fb} - \frac{\lambda_{QG} q N a}{2\varepsilon_{si}} \tag{3.23}$$

Now the total drain current (I_D) in the Double Gate (DG) MOSFET will be the result of summation of all the available conducting electrons that are present along $x = x_{0min}$ $\forall y$. This state can be analogically considered equivalent to a virtual cathode that is located parallel to the y-axis at $x = x_{0min}$ which provides all the free conducting electrons resulting in the total drain current. From the above situation it can be concluded that the total drain current (I_D) is directly related to the total available conducting electrons (majority charge carriers) that are present at the position of virtual cathode.

Let $n_m(y)$ represent the total conducting electrons density at (x_{0min}, y) of the above mentioned virtual cathode. We assume that for the subthreshold region the electron quasi-Fermi potential level will be almost non-varying throughout the device channel except at the places that are very close to the drain region. Now from the very classical Boltzmann's equation, we obtain

$$n_m(y) = \frac{n_i^2}{N_a} \exp\left[\frac{\psi_{VC}(y)}{V_T}\right] \tag{3.24}$$

Now let $\psi_{VC}(y)$ represent the potential function of the virtual cathode i.e. $\psi_{VC}(y) = \psi(x_{0min}, y)$ which is given by

$$\psi_{VC}(y) = \psi_{0min} + \left[\frac{V_G - V_{fb} - \psi_{0min}}{\lambda_{QG}}\right] y^2 \tag{3.25}$$

3.4 Subthreshold Swing Modelling

The model derived by Xiaoping and Taur showed I_D is proportional to $n_m(y)$. We use this result in (3.24) so that we obtain the subthreshold swing (S) as

$$S = \left(\frac{\partial \log I_D}{\partial V_G}\right)^{-1} = \ln 10 \left(\frac{\partial \ln I_D}{\partial V_G}\right)^{-1} \tag{3.26}$$

$$S = \frac{kT}{q} \ln 10 \left[\frac{\partial \psi_{VC}}{\partial V_G} \right]^{-1} \tag{3.27}$$

Now after substituting the value of $\psi_{VC}(y)$ from (3.25) in (3.27) we can show that

$$\frac{\partial \psi_{VC}(y)}{\partial V_G} = \left(1 - \frac{y^2}{\lambda_{QG}}\right) \frac{\partial \psi_{0min}}{\partial V_G} + \frac{y^2}{\lambda_{QG}} \tag{3.28}$$

After substituting (3.19) to (3.21) in (3.23), we obtain

$$\frac{\partial \psi_{0min}}{\partial V_G} = 1 + K \tag{3.29}$$

where

$$K = \frac{1}{\sqrt{k_1 k_2}} \left[(k_1 - k_2) \left(\frac{1 - \exp\left(-\sqrt{\frac{2}{\lambda_{QG}}} L\right)}{\exp\left(\sqrt{\frac{2}{\lambda_{QG}}} L\right) - \exp\left(-\sqrt{\frac{2}{\lambda_{QG}}} L\right)} \right) - k_1 \right] \tag{3.30}$$

Until now we have found the subthreshold swing parameter of our device as a function of y. To obtain S independent of y we use the effective conduction path concept developed by Chen et al. at $y = d_{eff}$
where

$$d_{eff} = \frac{\int_0^{\frac{t_{si}}{2}} y.n_m(y)dy}{\int_0^{\frac{t_{si}}{2}} n_m(y)dy} \tag{3.31}$$

Now, substituting (3.28) to (3.30) in (3.27) and again substituting y by d_{eff} in the final resulting expression for Subthreshold Swing S, the subthreshold swing (S) parameter of the QG MOSFET shall be derived in the terms of the effective conducting path d_{eff} as follows -

$$S = (\ln 10) \frac{kT}{q} \left[1 + K \left(1 - \frac{d_{eff}^2}{\lambda_{QG}} \right) \right]^{-1} \tag{3.32}$$

CHAPTER 4

Results and Discussion

In this section we present some theoretical and simulated results of electrical characteristics, subthreshold characteristics for the symmetric QG MOSFET structure. Different dedicated section have been dedicated for studying of effective conduction path and subthreshold swing by varying various device parameters. The simulation values are obtained from the commercially available ATLAS^{TM} device simulator. A detail explanation of the result is provided in each section. All the device parameters that are not varying have been specified in the figures itself. Some comparisons are also made from different figures and merged into a single figure. For simplicity of understanding all the simulation data have been visualized as a single symbol, i.e. "$\triangle$". All the modelling values have been obtained with the help of MATLAB^{TM}. Both the values have been merged to obtain a single figure in MATlAB^{TM} itself.

4.1 Variation of effective conduction path (d_{eff}) vs channel doping (N_a)

The dependence of the effective conduction path parameter (d_{eff}) on the channel doping N_a has been presented in figure 4.1 for various gate lengths. In conventional MOSFETs the electrons flow mostly on the surface of the device channel and therefore historically known as surface conducting devices. It is observed from figure 4.1 that for smaller values of N_a ($< 1020m^{-3}$), the value of d_{eff} becomes much closer to the centre of the channel which implies that the centre potential is higher than the surface potential and charge carrier responsible for subthreshold conduction mainly flows through the centre of the device. However, as N_a increases further, the surface potential value becomes much higher near the surface than that of other positions along the transverse direction of the channel and thus the overall electron conduction becomes largely confined to the Si/SiO_2 interfaces. This validates the assumption of surface conduction of charge carriers in conventional long channel MOSFETs.

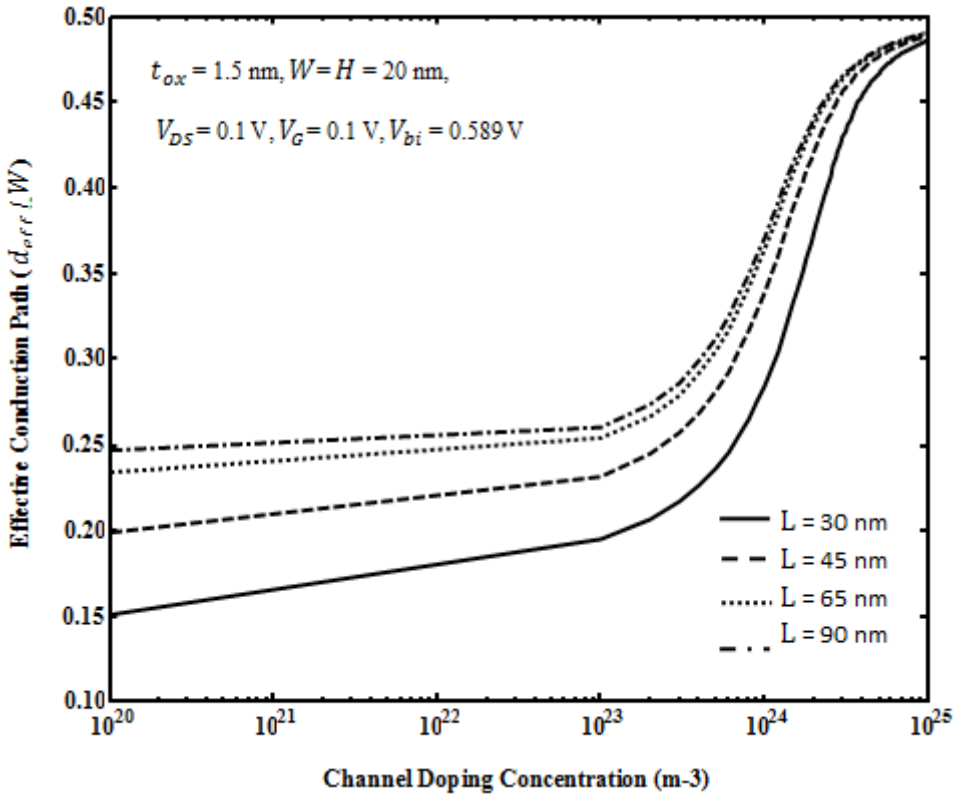

Figure 4.1: Variation of effective conduction path (d_{eff}) with channel doping (N_a)

4.2 Variation of the Subthreshold Swing (S) vs the Device Channel Length (L) for various Oxide Thickness (t_{ox})

The variation of subthreshold swing (S) with the channel length (L) is shown in figure 4.2 for different oxide thicknesses. The solid line shown in the figure is for $t_{ox} = 3nm$ and the broken line represents $t_{ox} = 1.5nm$. As we can see from the figure, $t_{ox} = 3nm$ gives higher subthreshold swing compared to $t_{ox} = 1.5nm$. This can be explained by the fact that thinner gate oxide means higher gate capacitance, that implies V_{FB} increases and gate voltage has to overcome this extra potential in case of thinner oxide compared to thick gate oxide to make channel inversion.The results of figure 4.2 suggest that thinner gate oxides are required to get better subthreshold characteristics.

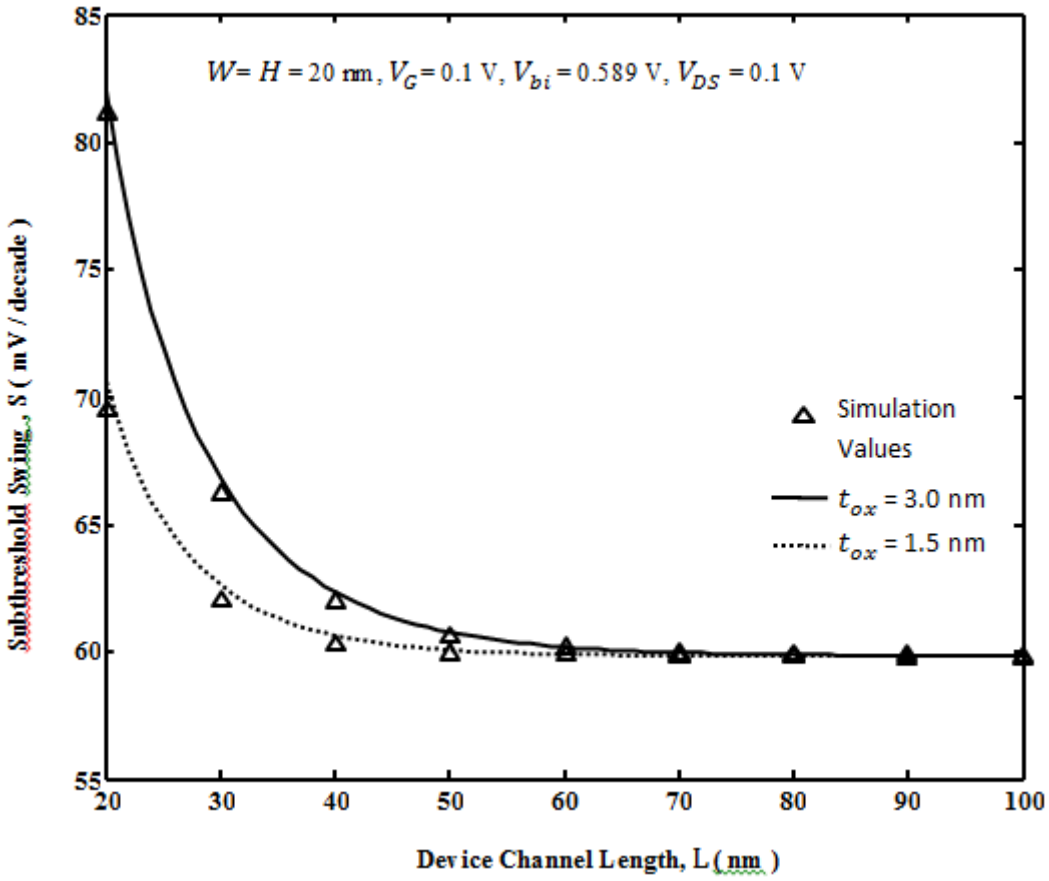

Figure 4.2: Variation of the Subthreshold Swing (S) with the Channel Length (L) for different Oxide Thickness (t_{ox})

4.3 Variation of Subthreshold Swing (S) vs the Device channel Length (L) for various channel thickness (t_{si}) at various V_{DS}

The variation of subthreshold swing parameter S as a function of the device channel length (L) for various channel thicknesses (W and H) at $V_{DS} = 0.1\ V$ and $0.5\ V$ is shown in figure 4.3 and figure 4.4 respectively. The parameter S is found to be increased with the shrinkage of channel length resulting in the poor switching characteristics of the device. But for a fixed channel length, the switching characteristics are observed to be improved as we decrease the values of channel thickness. Since, the gate will be in better position to control it for smaller channel thickness, the above results seem to be well justified.

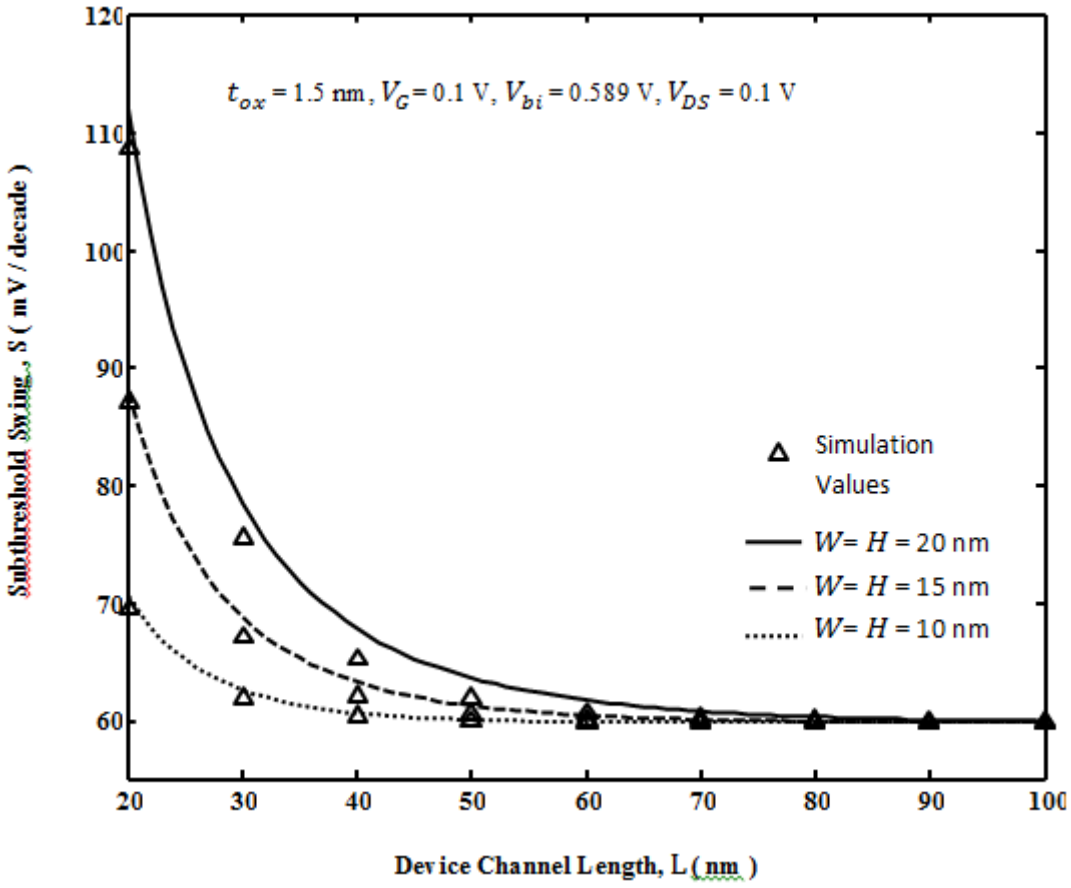

Figure 4.3: Variation of Subthreshold Swing (S) with the channel Length (L) for different channel thickness (t_{si}) at $V_{DS} = 0.1V$

Figure 4.5 is used to compare the values of figure 4.3 and figure 4.4 for $t_{ox} = 1.5nm$, $W = H = 20\ nm$. Lower value of V_{DS} improves the subthreshold characteristics of the device. However, the effect of V_{DS} on the subthreshold swing decreases as the device channel length increases.

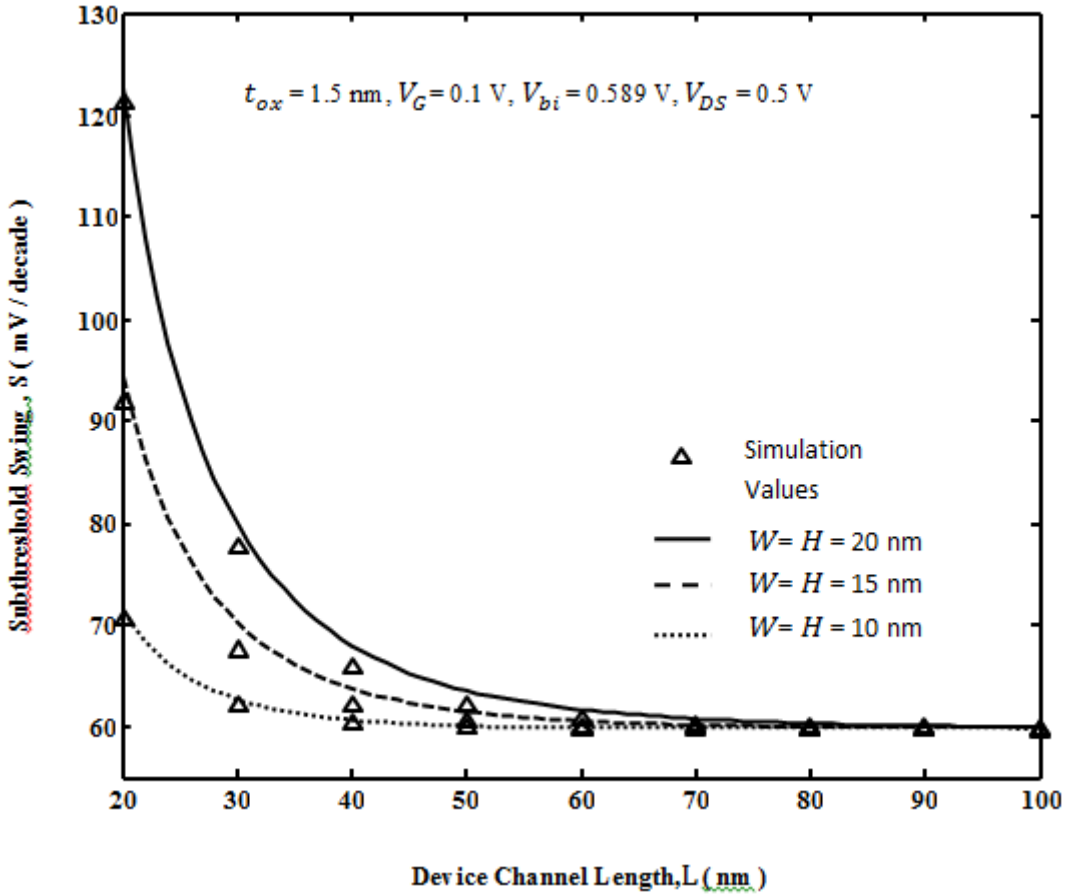

Figure 4.4: Variation of Subthreshold Swing (S) with the channel Length (L) for different channel thickness (t_{si}) at $V_{DS} = 0.5V$

4.4 Variation of Subthreshold Swing (S) vs the channel doping for different channel thickness (t_{si})

Figure 4.6 shows the dependence of the subthreshold swing parameter, on the channel doping concentration N_a for different values of channel thickness. It may also be observed from the figure that the subthreshold swing, is almost constant for $N_a < 1020m^{-3}$ and S is increased with N_a for higher values implying an improved subthreshold characteristics of the device. The figure further shows that the channel thickness and width of the device can also play an important role in controlling the subthreshold swing parameter. As the channel thickness goes down from 20 nm to 10 nm with all other parameters remaining unchanged, the value of the subthreshold swing goes down significantly.

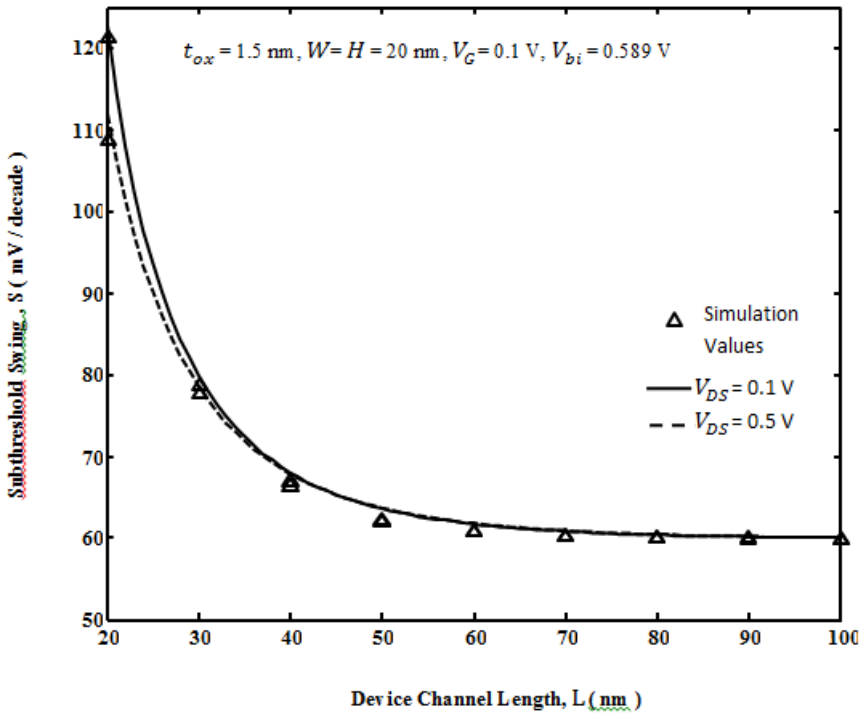

Figure 4.5: Variation of Subthreshold Swing (S) with the channel Length (L) for different V_{DS}

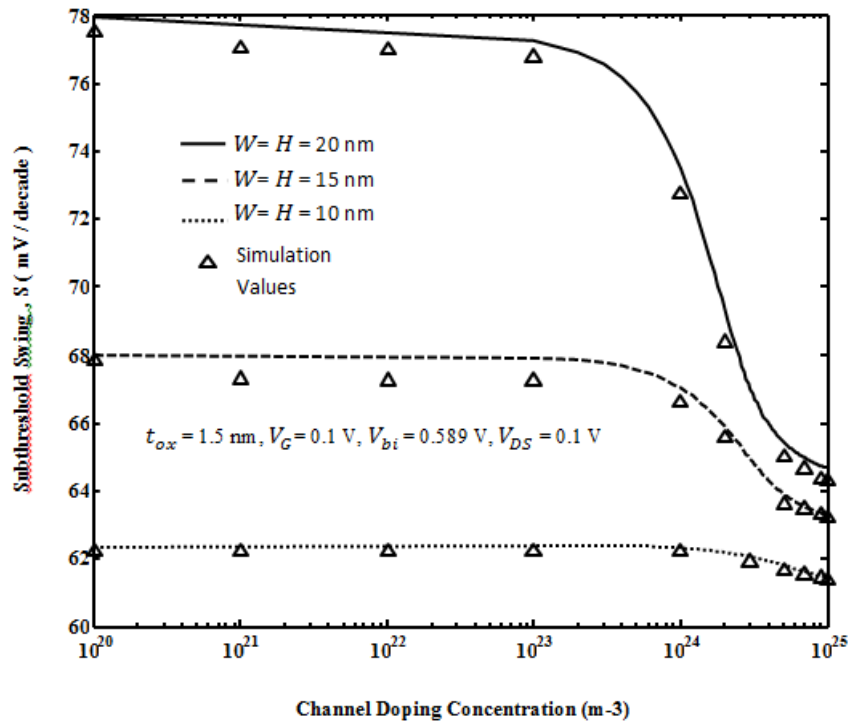

Figure 4.6: Variation of Subthreshold Swing (S) with the channel doping (N_a) for different channel thickness (t_{si})

CHAPTER 5

Summary and Future Scope

5.1 Summary

In this thesis a potential function was obtained for the quadruple gate MOSFET was obtained using the concept of ENGs. Thereafter analysis of subthreshold swing was performed by varying various device parameters that are channel doping, device channel length, channel thickness and channel width, oxide thickness, drain to source voltage. It has been observed that the effective conduction path of electron conduction is in the bulk if channel doping is low and moves towards oxide interface as doping increases, effective conduction path moves towards the channel center as device channel length is decreased. The subthreshold swing of the device can be improved by decreasing oxide thickness, increasing channel length, decreasing device thickness and width, increasing drain to source voltage and increasing channel doping concentration.

5.2 Future Scope

In future introducing different types of material for gate oxide, effect of temperature on the device can be analysed.

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