DESIGN AND IMPLEMENTATION OF A NOVEL FLASH ADC FOR ULTRA WIDE BAND APPLICATIONS

A Thesis report submitted in partial fulfillment of the requirement for the degree of

Doctor of Philosophy

In

ELECTRONICS AND COMMUNICATION ENGINEERING

By

GEORGE TOM VARGHESE

(Roll no: 511EC102)

Under the guidance of

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CERTIFICATE

This is to certify that the thesis entitled "**Design and Implementation of a Novel Flash ADC for Ultra Wide Band Applications"** submitted by **Mr. George Tom Varghese** in partial fulfillment of the requirements for the award of **Doctor of Philosophy** Degree in Electronics and Communication Engineering with specialization in "VLSI Design and Embedded Systems" during the session 2011-2014 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/Institute for the award of any Degree or Diploma.

Date:

Place:

Prof. Kamalakanta Mahapatra
Department of Electronics & Communication Engineering
National Institute of Technology, Rourkela

Dedicated

To

Chachen, Amma &Achu

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ABSTRACT

This dissertation presents a design and implementation of a novel flash ADC architecture for ultra wide band applications. The advancement in wireless technology takes us in to a world without wires. Most of the wireless communication systems use digital signal processing to transmit as well as receive the information. The real world signals are analog. Due to the processing complexity of the analog signal, it is converted to digital form so that processing becomes easier. The development in the digital signal processor field is rapid due to the advancement in the integrated circuit technology over the last decade. Therefore, analog-to - digital converter acts as an interface in between analog signal and digital signal processing systems. The continuous speed enhancement of the wireless communication systems brings out huge demands in speed and power specifications of high-speed low-resolution analog-to - digital converters.

Even though wired technology is a primary mode of communication, the quality and efficiency of the wireless technology allows us to apply to biomedical applications, in home services and even to radar applications. These applications are highly relying on wireless technology to send and receive information at high speed with great accuracy. Ultra Wideband (UWB) technology is the best method to these applications. A UWB signal has a bandwidth of minimum 500MHz or a fractional bandwidth of 25 percentage of its centre frequency. The two different technology standards that are used in UWB are multiband orthogonal frequency division multiplexing ultra wideband technology (MB-OFDM) and carrier free direct sequence ultra wideband technology (DS-UWB). ADC is the core of any UWB receiver. Generally a high speed flash ADC is used in DS-UWB receiver.

Two different flash ADC architectures are proposed in this thesis for DS-UWB applications. The first design is a high speed five bit flash ADC architecture with a sampling rate of 5 GS/s. The design is verified using CADENCE tool with CMOS 90 nm technology. The total power dissipation of the ADC is 8.381 mW from power supply of 1.2 V. The die area of the proposed flash ADC is 186 µm × 210 µm (0.039 mm^2). The proposed flash ADC is analysed and compared with other papers in the literature having same resolution and it is concluded that it has the highest speed of operation with medium power dissipation.

The second design is a reconfigurable five bit flash ADC architecture with a sampling rate of 1.25 GS/s. The design is verified using CADENCE tool with UMC 180 nm technology. The total power dissipation of the ADC is 11.71 mW from power supply of 1.8 V. The die area of the implementation is 432 µm × 720 µm (0.31104 mm^2). The chip tape out of the proposed reconfigurable flash ADC is made for fabrication.

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ABBREVIATION

UWB	-	Ultra Wide Band
SAR	-	Successive Approximation Register
ADC	-	Analog to Digital Converter
LNA	-	Low Noise Amplifier
BPF	-	Band Pass Filter
CMOS	-	Complementary Metal Oxide Semiconductor
ROM	-	Read Only Memory
SS	-	Spread Spectrum
RF	-	Radio Frequency
WPAN	-	Wireless Personal Area network
FCC	-	Federal Communication Commission
DS-UWB	-	Direct Sequence UWB
OFDM	-	Orthogonal Frequency Division Multiplexing
MB-OFDM	-	Multiband OFDM
QPSK	-	Quadrature Phase Shift Keying
BPSK	-	Binary Phase Shift Keying
PPM	-	Pulse Position Modulation
CDMA	-	Code Division Multiple Access
DSP	-	Digital Signal Processing/Processor
DAC	-	Digital to Analog Converter
CCD	-	Charge Coupled Device
HDTV	-	High Definition Television
SNR	-	Signal to Noise Ratio
MSB	-	Most Significant Bit
SQNR	-	Signal to Quantization Ratio

SNDR	-	Signal to Noise Distortion Ratio
ENOB	-	Effective Number of Bits
SFDR	-	Spurious Free Dynamic Range
Op-Amp	-	Operational Amplifier
LSB	-	Least Significant Bit
LVS	-	Layout Vs Schematic
DRC	-	Design Rule Check
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N-Type Metal Oxide Semiconductor
PMOS	-	P-Type Metal Oxide Semiconductor
RCX	-	Resistance Capacitance Extraction
INL	-	Integral Non Linearity
DNL	-	Differential Non Linearity
FoM	-	Figure of Merit
GND	-	Ground
LAN	-	Local Area Network
FFT	-	Fast Fourier Transform
DSSS	-	Direct Sequence Spread Spectrum
FHSS	-	Frequency Hopping Spread Spectrum
CCK	-	Complementary Code Keying

CHAPTER 1

OVERVIEW

1.1 Introduction to research

The advancement in wireless technology takes us in to a world without wires. Most of the wireless communication systems use digital signal processing to transmit as well as receive the information. The real world signals are analog. Due to the processing complexity of the analog signal, it is converted to digital form so that processing is easier. The development in the digital signal processor field is rapid due to the advancement in the integrated circuit technology over the last decade. Moreover, advantage of digital processing is that it is more immune to noise. So analog-to-digital converter plays an interface role in between analog signal and digital signal processing system. The continuous speed enhancement of the wireless communication systems have bring out huge demands in speed and power specifications of high speed low resolution analog-to-digital converters.

Even though wired technology is primary mode of communication, the quality and efficiency of the wireless technology allows us to apply to biomedical applications, in home services and even to radar applications. These applications rely heavily on wireless technology to send and receive information at high speed with great accuracy. The restricted availability of commercially available communication frequency spectrum limits the application range. Commercial radio frequency bands use bandwidths of the order of 100 MHz to few GHz [1]. This leads wireless technology may be applied to only narrow band applications.

Up to 2002, the frequency spectrum from 3.1 GHz to 10.6 GHz is used for military applications in United States. However in 2002, the federal communication commission (FCC) deregulated the use of this frequency spectrum and made it available for commercial applications. Subsequently other countries also deregulate this frequency spectrum for commercial purposes. This range of frequencies is widely known as ultra wideband spectrum (UWB). Due to this, large frequency band distributes over 3.1 GHz to 10.6 GHz can be used for commercial applications.

1.2 Motivation

Conventional radio transmissions transmit data by changing power level, phase or frequency of a sinusoidal signal. But UWB communication transmits each slice of information over a

wide frequency band [2, 3]. The pulses which are using for the UWB communications are very short. Due to high data transmission rate and resistance to multipath fading, UWB technology becomes more and more popular.

Fig. 1.1 shows the typical block diagram of UWB receiver [14]. It consists of mainly three parts.

- Radio frequency front end
- ADC
- Digital backend

ADC is the core of any UWB receiver. Since UWB signals are widely distributes over a large frequency range [4], the selection of an ADC is crucial in the design of UWB receiver. The types of ADCs used may be varied in accordance with different applications. It is determined mainly based on the sampling frequency, power consumption and resolution. For example, flash ADCs can be utilized in low resolution high speed applications. Due to its parallel operation, all the conversions are done in a single clock cycle. But a successive approximation register (SAR) ADC uses in high resolution low speed application. So the selection of an ADC is determined by the application where it is used. High sampling frequency ADCs are widely used for UWB applications.

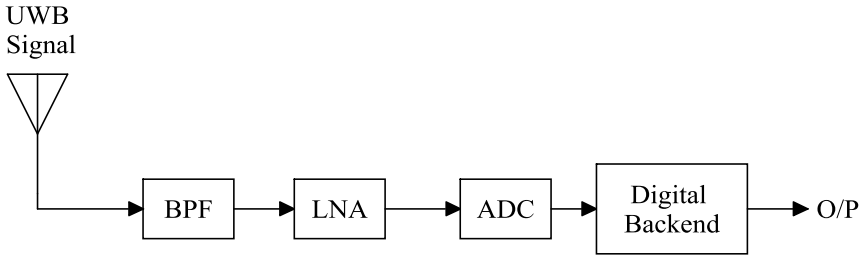


Fig. 1.1 Block diagram of UWB receiver

The prime focus of the research is to design a high speed medium power ADC used in UWB receiver architecture [5]. This UWB receiver mainly targets applications such as in home wireless connectivity and biomedical devices.

1.3 Research aims and objectives

The prime focus of this research is to develop a high speed flash ADC used in UWB applications of in-home wireless systems and biomedical devices. The main aims of this research are

- To inspect UWB receiver architecture and identify its requirement and specification of an ADC for the application.
- Design and implement a high speed pseudo dynamic logic based CMOS comparator for the specific application.
- Develop and implement a high speed pseudo dynamic logic based encoder which converts thermometer code to binary code in flash ADC.
- Implement a high speed ADC for the application by combining resistor ladder, comparators and encoder.
- Analyse and compare the results with other types of similar ADCs.
- Design and implement a reconfigurable flash ADC used for similar applications with lower frequency of operation. Characteristics of the proposed ADC is figured out and explained. Comparisons have been made with other similar architectures.

  The proposed flash ADC block diagram is shown in Fig. 1.2.

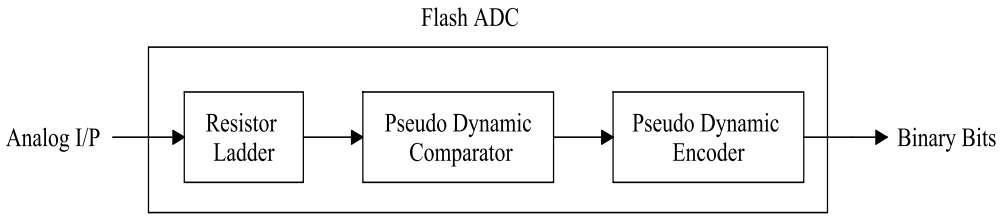


Fig. 1.2 Block diagram of proposed flash ADC

1.4 Design methodology

The design methodology followed in the research is shown below

- To inspect UWB receiver architecture and identify its requirement and specification of an ADC for the application.

  A wide range study of two different UWB receiver architectures is carried out. Specification of flash ADC used in the receiver architecture is also suggested.
- Design and implement a high speed pseudo dynamic logic based CMOS comparator.

  Since comparators play a crucial role in the design of a flash ADC, this research includes detailed study of different architectures. To enhance the speed of comparator, pseudo dynamic logic based comparator is proposed and analysed.
- Develop and implement a high speed encoder which converts thermometer code to binary code in flash ADC.

  There are different methods with which the implementation of thermometer code to binary code can be done. Wallace tree encoder, multiplexer based encoder, logic

based encoder, fat tree encoder and ROM based encoder are some of the different methods. A detailed study of different encoders are carried out and proposed the most apt pseudo dynamic logic based encoder for the conversion of thermometer to binary code.

- Implementation of a high speed ADC used for the application.

  Integrating resistor ladder, comparators and thermometer to binary code encoder, flash ADC is designed. All the parameters of ADCs are tested and trade off between speed and power is made.

- Analyze and compare the results with other types of ADCs

  A detailed analysis of the implementation is done and compared the proposed ADC with other types of ADCs used for the specific application. The complete ADC is designed and implemented using CMOS 90 nm technology using CADENCE environment.

- Implementation of a reconfigurable five bit flash ADC

  The output bits of a reconfigurable flash ADC is not constant. It can be varied according to the operating conditions. In this design, MSB of the flash ADC is found out first and with the help of MSB bit, flash ADC's remaining bits are calculated. Finally it is compared with other similar flash ADCs and performance is evaluated. The chip tape out of the proposed reconfigurable flash ADC has made in the last stage.

1.5 Thesis Organization

The thesis is structured into seven chapters. Following to the overview, chapter two demonstrates a literature survey of UWB communication standards. The different standards are described in detail with their advantages and disadvantages and finally conclude with the selection of the standard used for this application. It also describes about different architectures of ADC such as flash, pipeline, successive approximation register, sigma delta and dual slope. Different ADCs are used for different applications. Sampling frequency, power dissipation and resolution of ADCs are determined on the basis of specific application. Five bit flash ADC is taken as the appropriate one for the specific application. Chapter three illustrates different comparator architectures and proposes a high speed pseudo dynamic logic based comparator used for the application and analyses its properties. Chapter four portrays different methods of converting thermometer to binary code. The methods are presented in detail with advantages and disadvantages and finally propose a pseudo dynamic logic based

encoder used for the application. Chapter five represents the implementation of the complete flash ADC by integrating the blocks such as resistor ladder, comparators and thermometer to binary code encoder. It also discusses about the parameters of the specific ADC, layout and post layout simulation of the total module. The chapter also compares the implemented ADC with other ADCs with the same resolution and describes about the advantages and disadvantages of the implementation. Chapter six describes about implementation of a reconfigurable flash ADC. The chapter compares the results of the proposed ADC with other ADCs and finally chip tape out has been made for the reconfigurable ADC. Chapter seven concludes the total work and briefly discusses about the future work.

1.6 Thesis Contributions

- A five bit flash ADC with a sampling rate of 5GS/s is designed and tested the functionality.
- It consists of a high speed preamplifier based pseudo dynamic latch comparator. In order to reduce the overdrive recovery time, a pas transistor is added to the preamplifier circuit.
- An improved multiplexer based implementation is done in order to convert thermometer code to binary code. To meet the sampling rate of 5GS/s, the implementation is done using pseudo dynamic logic.
- A bubble tolerant thermometer code to binary code converter is implemented by using an intermediate step of adding a gray code encoding before producing the desired binary code.
- An improved reconfigurable five bit flash ADC is also realized with the help of high speed comparators, multiplexers and 3:2 encoders.

1.7 Conclusion

In reality, digital signal has the benefits of effortless processing, testing and storage. So we convert the analog signal to the digital signal for processing. The way to implement this is with the help of analog-to-digital converter as the interface. Researchers are exploring new design techniques for an ADC with the aim of drop off power consumption and to enhance the speed of operation. In all the other types of ADCs, flash ADC design turns out to be more significant as a result of the reality that it frequently plays a crucial role in other types of ADCs such as multi bit sigma delta ADC and pipelined ADC. Based on sampling frequency, power dissipation and resolution, the research proposes a high speed pseudo dynamic based five bit flash ADC for UWB receiver that uses in biomedical as well as in home wireless

applications. In the similar manner, a reconfigurable five bit flash ADC is also designed and implemented for similar application with lower sampling frequency of operation. The proposed ADC is having better performance characteristics in comparison with previously designed flash ADC, when it is operating in a lower frequency of operation. Chip tape out is made for the reconfigurable flash ADC in the final stage of implementation.

CHAPTER 2

Introduction to UWB and Selection of ADC architecture for UWB applications

2.1 Introduction to UWB

Ultra Wideband (UWB) is a means of communication that's historically as old as Morse code but is new in its potential for far reaching applications. It is a communication scheme that primarily uses the frequency spectrum from 3.1 GHz to 10.6 GHz for short range, low power and high speed-high bandwidth communications. Communication is based on the use of sharp pulses with coded data represented by each of these pulses hovering about a centre axis frequency at very low emission levels minus the use of a high frequency carrier. Each pulse is miniscule in its time frame such that its energy is spread over the entire frequency range.

In the 1960s, UWB was primarily harnessed for its potential use in military applications. In 2002, when the FCC in USA deregulated its use, it brought with it a host of issues and challenges. A UWB signal has a bandwidth of at least 500 MHz or a fractional bandwidth of 25 percent of its centre frequency. Ultra Wideband brings with it unique properties of non-interference with other systems, immunity to multi-path fading, frequency and bandwidth adaptive, simple system architecture, low cost digital solutions and being extremely difficult to detect. UWB signal spectrum occupies a wide frequency range and sits at a very low power level (-41.3 dBm/MHz) [6] as compared to other communication systems. This is because the FCC has placed a limit on the amount of power that can be used by UWB device to minimise interference to other frequency devices. The limit means that only very low power can be used for transmission and reception of UWB signals thereby effectively restricting the use of UWB to indoor, short-range communications for high data rates or very low data rates at substantial distances.

The advantages of UWB [7] make it more useful for consumer communications applications. Especially, UWB systems have the following advantages.

- Improved channel capacity
- Ability to share the frequency spectrum with narrowband signals
- Less sensitive to multipath effects

- High immunity to detection and interception
- Extremely high data rates possible
- Simple transceiver structure
- Fine time resolution

2.2 Applications of UWB

Applications of UWB systems include military applications, biomedical health monitoring systems, In-home wireless connectivity and collision avoidance systems. This research mainly focuses on UWB applications of in-home wireless connectivity and biomedical systems.

2.2.1 Military Applications

Potential military applications include

- Inter vehicle short range – limited mobility wireless network
- Intra-vehicle wireless network
- Obstacle detection
- Range finding and self location
- Terrain mapping

In manned and unmanned military vehicles, intra vehicle wireless network is highly used because it abolishes the problems related with cable weight and cost. In order to operate different vehicle subsystems away from the vehicle, inter vehicle short range wireless network is used. Range determination is crucial for tracking and recognizing of both potential targets and friendly elements. Self location is highly used in autonomous applications. Object sensing and identification is used in unmanned systems which needs the capability to sense and recognize the objects in a variety of surroundings. Terrain mapping is used in specified military applications which involve sensing accuracy and plotting of different features of terrain from moderately small ranges.). It is used to sense, evade or deactivate hidden items (explosives, mines) and unpredicted objects (debris, rubbles). UWB is a superior option for terrain mapping due to its resistance to hostile jamming, hostile detection, and effective penetration ability through different materials, radio frequency interference, and good delay resolution capability.

2.2.2 Biomedical health monitoring system

Low power, non-invasiveness, biocompatibility, non-contact remote operation biological easiness, environmental friendliness and the accurate detection of UWB makes it appropriate for medical monitoring application [8]. Highly strong pulses are used in UWB technology.

UWB radar helps in supervising and evaluating patient's movements in the medical field. The usage of UWB in observing the patient in emergency unit could stay away from the using of too many wires near the patient. The application can be used to observe the patients whether he is moving in the specified time.

2.2.3 In-home wireless connectivity

Home network application is a critical feature to create pervasive home network environment. Within the home environment, UWB technology can possibly be suitable nomine to enable different applications. The wireless connectivity of different home electronic systems gets rid of the wiring mess in living room. In-home wireless connectivity permits a user sitting in a room at home to examine and be aware of the situation of the TV, desktop and security system there inside the house.

2.2.4 Collision avoidance system

UWB technology is highly used in detecting the vehicle speed and informs the driver about the accident that can occur [9]. The idea of the intelligent car consists of providing the vehicle with best possible number of sensors with the intention of monitor the environment which encloses it to make sure an automatic guidance control of the vehicle and to be in touch with the external medium. The originality of this radar is its capability to sense easily various barriers and to provide their signatures. High power efficiency, fine range resolution, low probability of detection and low probability of interference make UWB outstanding candidate technology in collision avoidance applications.

2.3 Characterization of UWB

Ultra-Wideband (UWB) offers an attractive new technology for small range high speed communications in the range from 3.1 GHz to 10.6 GHz. It maintains a bit rate larger than 100 Mbps inside a 10-meter radius for wireless personal area communications [2].

Since the communications channel capacity in a non fading surroundings is expressed as

$C = B * \log_2 (1+S/N)$

Where

C = channel capacity (bit/s)

S = signal power (watts)

N = noise power (watts)

B = channel bandwidth 'BW' (Hz)

In relation to above equation, the capacity can be enlarged by either raising channel bandwidth or signal to noise ratio. It is understandable that the capacity can be enlarged more

by raising the bandwidth rather than signal to noise ratio. UWB systems could also experience interference from different wireless technologies that are present in the neighbourhood of operation, but the problem can be diminished by using adaptive frequency bands selection in multi band UWB systems.

Ultra wideband technology has been approved for short range communication, except with constraints on the frequencies over which the transmission can spread and the power limits. This permits the ultra wideband transmissions to communicate effectively, but without influencing active narrowband transmissions. To attain these prerequisites, ultra wideband transmissions can officially work in the range 3.1 GHz up to 10.6 GHz at a transmit power of -41 dBm/MHz. In addition to the transmissions have to reside in a bandwidth of at least 500 MHz [10] and having a fractional bandwidth of not less than 25 % of the centre frequency. A typical representation of the statement can be written as

$$f_B = \frac{2(f_H - f_L)}{f_H + f_L} \geq 25\ \%$$

Where f_B is the fractional bandwidth of the UWB signal,

f_L and f_H are the lower and upper bounds of the frequency spread.

Subsequently, UWB offers remarkable channel capacity at small range which limits interference.

2.4 Comparison with other communication schemes

The main challenge to UWB in terms of competing wireless technologies for in-home wireless connectivity and Bio-Medical applications are Wi-Fi LAN, Bluetooth and Zig-Bee. Taking a closer look at these specific communications standards;

2.4.1 WiFi (802.11 x)

Wireless LAN as a means of network connectivity technology has been around for a number of years. It has progressed effectively enough to replace cable based Ethernet in providing internet and data connectivity. However it has struggled to provide the same amount of data rate as compared to cable Ethernet until the emergence of the 802.11n standard. Cable based Ethernet provides 100 Mega bits per second (Mbps) connection while Gigabit Ethernet provides more, whereas Wi-Fi is restricted to 11 Mbps for 802.11b, 22 Mbps for 802.11a, 54 Mbps for 802.11g and 300 Mbps maximum for 802.11n. These rates are still relatively low compared to the potential of minimum 500 Mbps data rate acquirable through UWB communication [29, 30].

2.4.2 Zig-Bee and Bluetooth

Zig-Bee and Bluetooth are recent communication standards with communication ranges of 20 feet for Zig-Bee and 30 feet for Bluetooth. They are serious contenders for short range wireless communications. The comparison in terms of cost leads Zig-Bee to march ahead of Bluetooth, however Bluetooth has a far superior and established data standard. These two standards are typically applicable to non-bandwidth intensive uses as the comparable data rates do not match even close to Wi-Fi LAN. Zig-Bee has a maximum efficient data rate of around 500 Kilo bits per second (Kbps) and Bluetooth of about 1 Mbps [29, 30]. Table 2.1 provides the comparison between Bluetooth, Zig-Bee, UWB and Wi-Fi.

Table 2.1 Comparison of the Bluetooth, UWB, Zig-Bee and Wi-Fi Protocols

Standard	Bluetooth	Zig-Bee	Wi-Fi	UWB
IEEE Spec	802.15.1	802.15.4	802.11a/b/g	802.15.3a
Frequency Band	2.4 GHz	869/915 MHz; 2.4 GHz	2.4 GHz; 5 GHz	3.1-10.6 GHz
Max Signal Rate	1Mb/s	250Kb/s	54Mb/s	500Mb/s
Nominal Range	10 m	10-100m	100m	10 m
Normal Transmission Power	0-10 dBm	-25 to 0 dBm	15-20 dBm	-41.3 dBm/MH
Channel Bandwidth	1 MHz	0.3/0.6 MHz; 2MHz	22 MHz	500 MHz- 7.5 GHz
Number of RF channels	79	1/10,16	14 (2.4 GHz)	1-15
Spreading	FHSS	DSSS	DSSS, CCK,OFDM	DS-UWB, MB-OFDM

In brief, Zig-Bee and Bluetooth are appropriate for low data rate applications with restricted battery power (such as battery operated sensor networks and mobile devices) caused by their low power consumption steering to an extensive lifetime. Alternatively, for high data rate operations (such as wireless in home connectivity, audio/video inspection systems, military application and bio medical application) Wi-Fi and UWB would be superior solutions because of their low standardized energy consumption. The data rate of Wi-Fi is still low compared to minimum 500 Mbps which is attainable by UWB communication.

2.5 Ultra Wideband Standards

The two different technology standards used in UWB are carrier free direct sequence ultra wideband technology (DS-UWB) and multiband orthogonal frequency division multiplexing ultra wideband technology (MB-OFDM) [15]. The two different standards are having different signalling scheme. This leads to different transceiver configuration that determines the type of ADC (architecture, resolution) which uses in the transceiver [11]. Since the main scope of the work is dealing with ADC, the transmitter section in neglected and more importance is given to receiver section [12].

2.5.1 Multi Band Orthogonal Frequency Division Multiplexing Ultra Wide Band Technology (MB-OFDM)

The MB-OFDM group was initially started by Intel and later on grew to include a number of other industry partners including Samsung, Panasonic, Texas Instruments and others. The industry groups were commonly referred to as the Multi-Band OFDM UWB Alliance (MBOA). The MBOA approach utilised the 7.5 GHz of frequency spectrum from 3.1 GHz to 10.6 GHz, by splitting them into 15 individual non-overlapping frequency bands, each occupying a little over 500 MHz of frequency spectrum.

MB-OFDM UWB receiver (Fig. 2.1) consists of low noise amplifier, low pass filter, ADC, matched filter bank, PN co-relator bank and data recovery circuits. The system is based on OFDM or Quadrature Phase Shift Keying technique (QPSK). The ADC requires high resolution with low sampling rates and low bandwidth. So generally time interleaved ADCs are used in this receiver. Each converter feeds into matched filter circuit and the output is given to PN co-relator bank for correcting the timing. The output of the PN co-relator bank is given to data recovery circuit to get the final data. As the date rate increases, the number of ADC used in the operation also increases. This increases the complexity of the receiver. Summary of MB-OFDM UWB receiver requirements are given in Table 2.2.

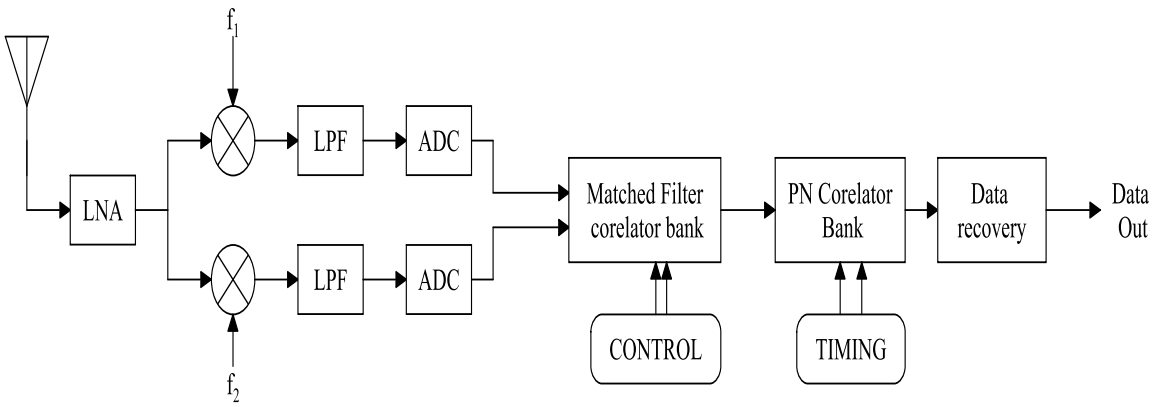


Fig. 2. 1 MB-OFDM UWB receiver topology

Table 2.2 Summary of MB-OFDM UWB receiver requirements

Bandwidth	500-528 MHz
Bands	13-15 Bands
Signalling Scheme	OFDM(N-Point), QPSK
Pulse Interval	More than 100 ns
ADC Used	N time interleaved sigma delta High resolution (5-8 bits) Low sampling rates

2.5.2 Direct Sequence UWB standard

The DS-UWB group was consisted of Xtreme Spectrum/Motorola and Freescale Semiconductor who were the leading proponents for this standard. The group grew to include other alliances such as Philips and Samsung.

UWB is an innovative wireless technology which permits data to be transmitted at a speed greater than 100 Mbps. Gaussian pulses with low power are generally used in this standard. The transmissions widen out over a large bandwidth normally in the range of 100 MHz to even some GHz. Each of the DS-UWB pulses is particularly small duration which is normally in the range of 10 to 1000 picoseconds. Because of the short duration pulse, multipath effects can be disregarded which provides a large amount of flexibility in the transmission when the signal path is surrounded by the building.

DS-UWB utilizes the frequency spectrum of 7.5 GHz from 3.1 GHz to 10.6 GHz for operation. It is done by splitting the band into two non overlapping bands (Lower band and Upper band). The lower band ranges from 3.1 to 4.7 GHz and the upper band ranges from 5.8 to 10.6 GHz. The band from 4.8 to 5.7 is kept free for wireless LAN to eliminate any chances of narrow band interference.

The well accepted modulation methods for DS-UWB are Pulse Position Modulation (PPM) and Binary Phase Shift Keying (BPSK). Modulation efficiency and spectral performance are the two important parameters for the modulation schemes which are remarkable for these two modulation schemes. PPM encodes the data by altering the time interval and hence the pulse

position. BPSK reverses the pulse phase (180 degree) to indicate the transmitted data. As the pulses contain an initial upward or downward voltage, it is effortless to change the phase of the pulse by 180 degree. In addition to this, the transmission can be done with the help of direct sequence codes. The received signal should be compared with the exact direct sequence code which is to be demodulated. The advantage of this technique is only the specified receiver can demodulate it. Normally all the transmission methods uses carrier based approach. But UWB technology presents the opportunity of very large data rate transmissions with very low power.

Fig. 2.2 shows the block diagram description of a DS-UWB receiver [13, 15]. In comparison with MB-OFDM UWB technology, DS-UWB uses a single analog-to-digital converter with high sampling rate and low to medium resolution. So generally a high speed flash ADCs are used in these types of receivers. This topology is having the advantage of having lesser number of ADCs in comparison with MB-OFDM UWB. This effectively reduces the device count in the receiver thereby saving area and power consumption.

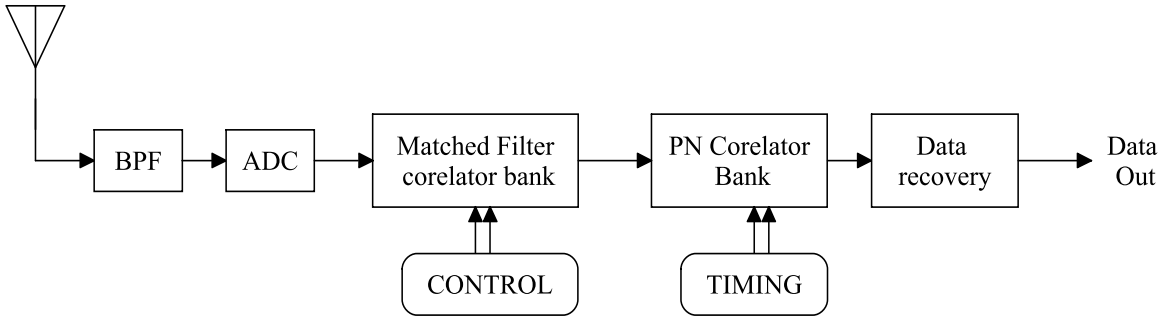


Fig. 2.2 Block diagram of DS-UWB receiver

Summary of DS-UWB receiver requirements are given in Table 2.3.

Table 2.3 Summary of DS-UWB receiver requirements

Bandwidth	2 GHz to 5 GHz
Bands	2 (Lower and Upper)
Signalling Scheme	BPSK, PPM
Access Methodology	Spread spectrum CDMA
Pulse Interval	1 ns (max)
ADC used	High speed Flash Low to medium resolution (3-5 bits) High sampling rate

Because of the reduced area and less complexity involved in the design, DS-UWB technology based applications are considered in this thesis. So in-home wireless connectivity and biomedical applications are taken as the examples. The next section describes about different ADCs architectures used in different applications.

2.6 Introduction to Analog to Digital Converter

Digital signal has the benefits of easier processing, analysis and storage. Nowadays, a lot of applications make use of digital signal processing (DSP) to demodulate the transmitted information. Over the years, improvement of digital integrated circuit has strongly followed Moore's Law. As a result, transistor size has significantly reduced in size and the speed of digital circuit has been exponentially boosted. This trend broadens the gap between the digital circuit and its analog counterpart, for which the technology progress is not as beneficial. On one hand, there exists high speed digital circuit with its ever growing processing power and efficiency. On the other hand, analog circuit struggles and largely falls short to maintain pace. Most of systems require communication with the real analog world at some point or other. For that purpose analog interface circuit, is a crucial factor in the whole system. It is attractive to push the analog digital border nearer to the real world, where the system can acquire enhanced advantage of the high speed digital circuit. This development places high pressure on analog circuit designers to build up very high speed interface circuits, analog-to-digital and digital to analog converters (ADCs and DACs) that can sustain with the digital world by maintaining other desirable attributes like small chip area and low power consumption.

The continuous speed enhancement of serial links and emergence of new communication technologies such as ultra wideband (UWB) have begins greater demands on the speed and power requirements of high speed (3 to 5 GHz) low to medium resolution (4 to 6 bits) analog to digital converters (ADCs). ADCs are the fundamental building blocks that provide a border between the digital domain and analog world. As it is the major block in mixed signal applications, it plays a crucial role in data processing applications and that limits the performance of the overall system. The basic block diagram of analog-to-digital converter is depicted in Fig. 2.3. An analog signal is applied to the input of the converter which converts it into digital data which is used for further processing. ADCs can be categorized into different types mainly based on sampling rate, resolution and power dissipation and target

application. Based on the applications, ADC architecture can be mainly classified into three types.

- Low speed high resolution
- Medium speed medium resolution
- High speed low resolution

The different types of ADCs are flash, pipeline, successive approximation, dual slope and sigma delta [16]. The chapter deals with different analog-to-digital converter architectures and concludes with the selection of the ADC architecture which can be appropriately used for UWB applications. The next section gives detail description about each ADC used in different applications.

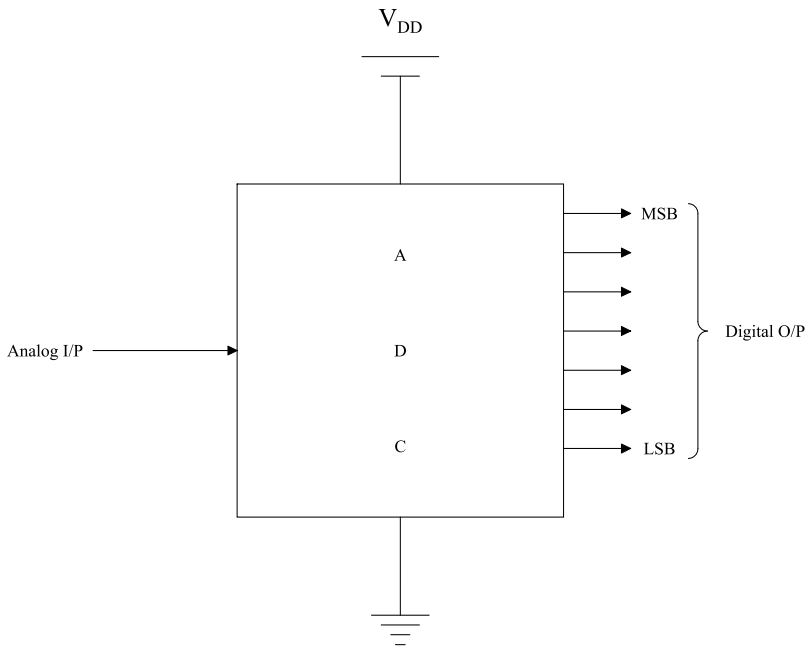


Fig. 2.3 Block diagram of analog to digital converter

2.6.1 Flash ADC

Flash ADCs utilize massive parallelism in its architectures and hence the name parallel ADC. The results of the conversion are available at the end of one clock cycle. Due to the parallel structural design it is the fastest ADC among all the other types and is appropriate for large bandwidth applications such as radar processing data acquisition, high density disk drives, satellite communication, data communications and real time oscilloscopes. It is also highly used in other types of ADCs such as pipeline ADCs and multi bit sigma delta ADCs. Flash ADC is limited to a resolution of six to eight bits because the numbers of comparators utilized in these ADCs are doubled if the resolution is enhanced by one bit. Due to this, it consumes a lot of power and becomes costly, as the resolution increases [17].

Fig. 2.4 shows the generic flash ADC block diagram. From the figure, it is clear that 2^N -1 comparators are needed for N bit flash ADC. Each comparator is connected with one input to an analog input and another to a reference voltage. The reference voltage for the comparator is generated with the help of a resistor ladder. The resistor ladder consists of 2^N resistors. The reference voltages are uniformly spaced by least significant voltage between the smallest reference voltage and the largest reference voltage. When the input voltage is less than the reference voltage of comparator it produces logic low otherwise, the comparator output is logic high. The outputs of the comparators are coming in a specific fashion which is known as thermometer code. It's named because it is like a mercury thermometer, where the mercury column always rises to the suitable temperature and no mercury is available beyond that temperature. This thermometer code is further translated into a binary data with the assist of a thermometer to binary code converter. Flash ADC requires a huge number of comparators when the resolution increases. For example, a 6-bit flash ADC requires 63 comparators, but 1023 comparators are required for a 10-bit flash ADC. This exponential increase of comparators needs a large die size which leads to huge amount of power consumption.

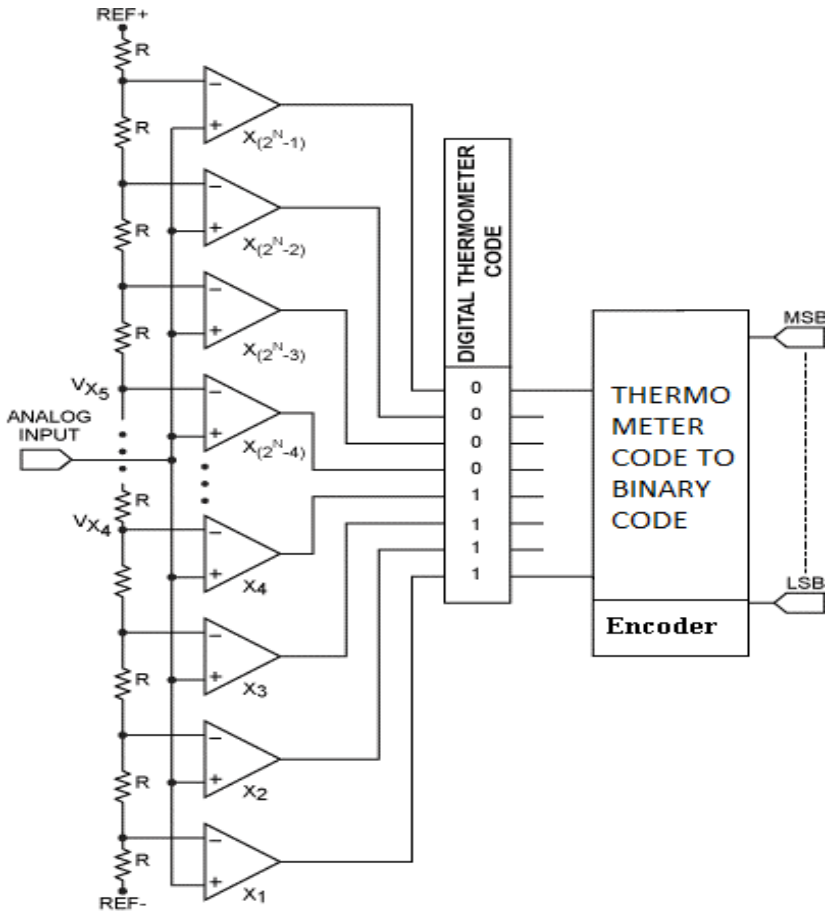


Fig. 2.4 Generic block diagram of flash ADC

2.6.2 Pipeline ADC

Pipeline ADC is the one of the popular ADC architecture [18]. It can work from few mega samples to above hundred of mega samples with resolution ranging from 8 bit to 16 bits. Due to its high resolution and medium sampling rate, it is commonly used in medical and communication applications such as, CCD imaging, digital receiver, digital video (HDTV), ultrasonic medical imaging, cable modem, base station and fast Ethernet. Pipeline ADCs are also used in data acquisition systems, where frequency and time domain features are both important. Pipeline ADCs are useful in configurations where latency is not critical and for applications where latency is critical, flash ADC is preferred. Design complexity grows linearly (not exponentially) with the resolution, thus providing converters with medium speed, low power and high resolution at the same time.

The basic pipelined architecture is shown in Fig. 2.5. The pipeline ADC consists of serially connected N stages. Each stage includes one bit ADC, sample and hold circuit and an amplifier with a gain of two. Once the input signal is sampled, it is compared with ($V_{REF}/2$). The output of the each one bit ADC (comparator) generates the binary bit. If analog input voltage is larger than ($V_{REF}/2$), comparator output is logic high and $V_{REF}/2$ is deducted from the held signal and transfer it to the amplifier. If the input voltage is less than $V_{REF}/2$, then transfer the original signal to the amplifier. The last step of operation is to multiply the summation result by two and transfer it to the next stage sample and hold circuit. The total time taken for the conversion of the analog input to digital data is time of N clock cycles. The one of the main disadvantage of this converter is a small error in the first stage transmits through the converter and results in a large amount of error at the end of conversion.

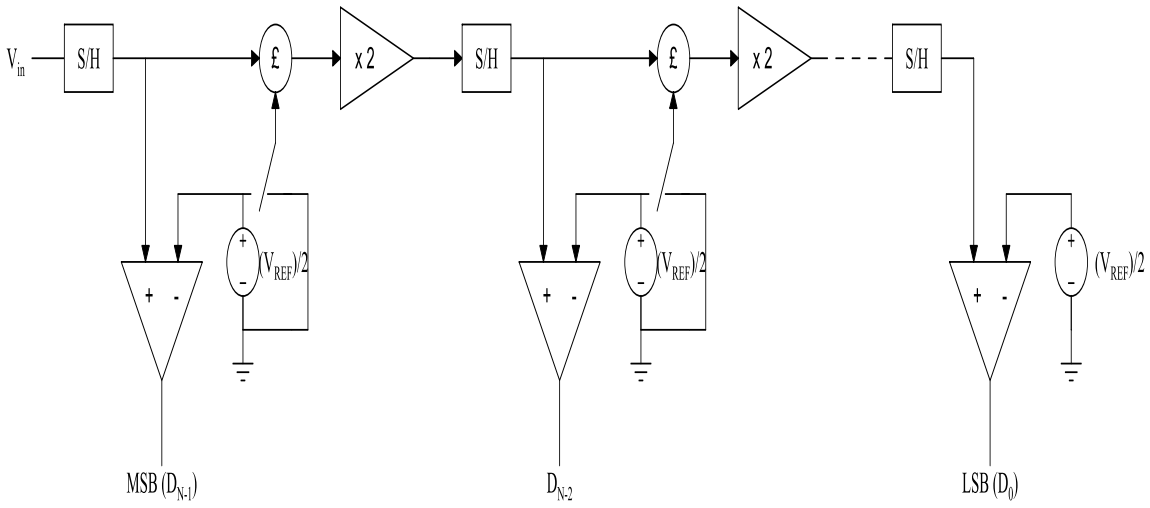


Fig. 2.5 Basic architecture of pipeline ADC

2.6.3 Successive Approximation Register (SAR) ADC

Successive approximation register (SAR) analog-to-digital converters (ADCs) are commonly used in low sampling rate and medium to high resolution applications [18]. The resolution is in the range between 8 to 16 bits. It also offers low power consumption and small form factor. Since its power consumption is low therefore it is a better alternative for low power applications such as industrial controls, data acquisition systems, portable/battery powered devices and pen digitizers. For a three bit SAR ADC, three comparisons are needed for the complete operation but at the same time flash ADC requires seven comparisons are required with seven different comparators. The power consumption is reduced by a large amount in SAR ADC in comparison with flash ADC because of the reduced number of comparators.

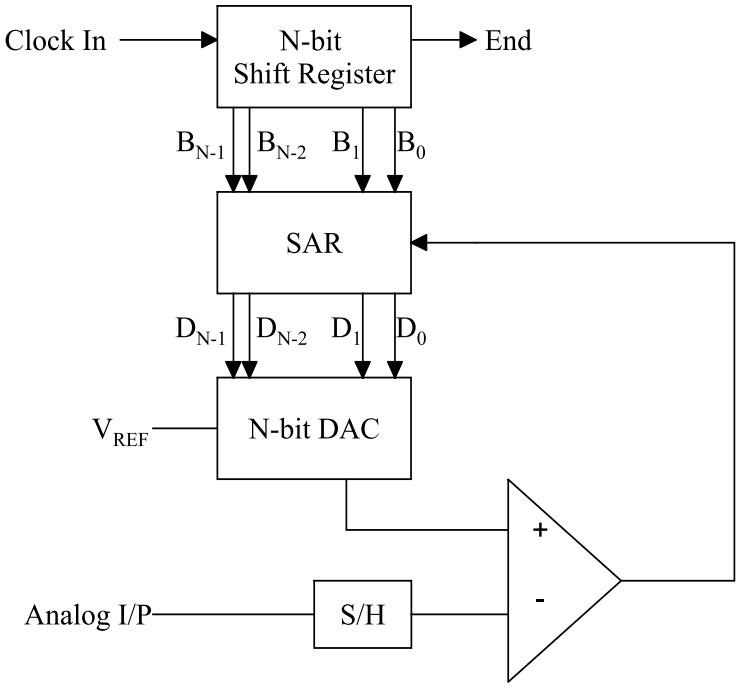


Fig. 6

Fig. 2.6 Block Diagram of SAR ADC

Fig. 2.6 shows the SAR ADC block diagram. Logic high is applied to the input of the shift register. For each bit conversion, the logic high ("1") is moved to the right by one bit position. Initially B_{N-1} is logic high and B_{N-2} to B_0 is zero. In the similar fashion, MSB of SAR, D_{N-1} is firstly set to logic high whereas residual bits are set to zeroes. Since digital to analog converter (DAC) output is controlled by SAR output, DAC output is set to $V_{REF}/2$. If analog input voltage is greater than $V_{REF}/2$, comparator output remains in zero and D_{N-1} remains in logic high. If it is the reverse case, comparator resets D_{N-1} to logic low ("0"). The logic high which is enforced to the shift register is shifted by one position in the next step. D_{N-2} is set to logic high with keeping all others in logic low. The output of DAC is either

$V_{REF}/4$ (D_{N-1}=0) or $3V_{REF}/4$ (D_{N-1}=1). The output of the DAC is compared with analog input. If DAC output is larger than analog input, D_{N-2} is set to logic zero; otherwise D_{N-2} remains in logic high. The process is continued until the output of the DAC converges to a value within the resolution of the converter.

2.6.4 Sigma-delta ADC

Sigma-Delta analog-to-digital converters are used in high precision and high accuracy applications [18]. The converter consists of a 1-bit digital-to-analog converter that functions as a switch. It also comprises of a comparator, Integrating circuit and Digital Filter. Typically functionality of a sigma-delta converter makes use of a tolerable over sampling ratio to perform highly accurate conversions. The architecture is shown in Fig. 2.7

The working of the converter can be explained by applying a low frequency signal at the input. The single bit digital-to-analog converter then samples and quantizes the input at a high sampling rate. The output is then compared through a comparator and passed onto the decimation filter where noise components and the sampling rate are reduced, thereby increasing the overall resolution and its accuracy. The accuracy of the converter is heightened by using the over-sampled clocking mechanism and the reference circuitry. Unlike Flash topology, where the reference resistors are susceptible to noise, this is not the case in sigma-delta. On the other hand these converters are suitable for very low speed applications, and are the slowest of all the converter topologies. Due to the oversampling mechanism, the actual conversion of the input signal takes quite a few clock cycles to perform. The design of the decimation filter is also a challenge due to its inherent complexity while converting the analog value into a digital equivalent.

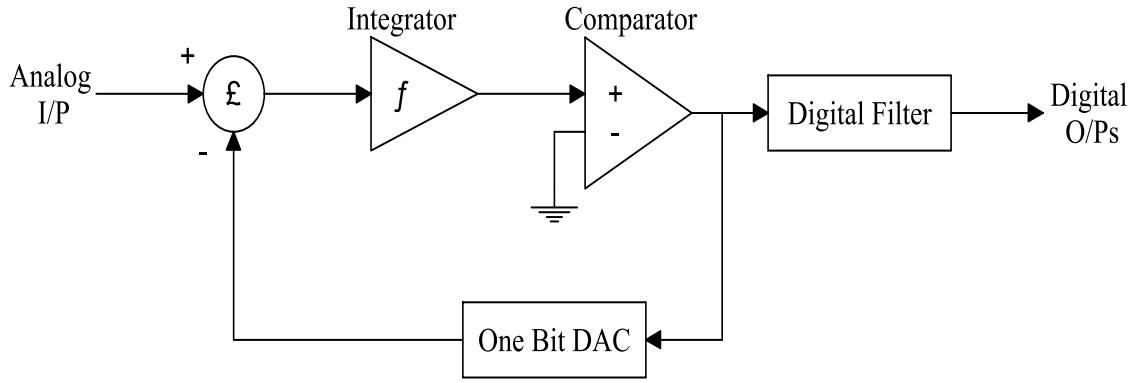


Fig. 2.7 Block Diagram of Sigma delta ADC

The sigma delta ADC is highly accepted for high resolution with low bandwidth applications because of the capability of noise shaping. Sigma delta ADC has been used widely in industry where better accuracy is required. The sigma delta ADC put forwards three main advantages:

- High performance conversion with low cost,
- Integrated digital filter
- Digital Signal Processor (DSP) compatibility for system integration

The speed of operation is the main drawback of sigma delta converter. It is the slowest architecture in all types of ADC converters. This conversion takes places in many clock cycles. The second disadvantage of sigma delta converter is its difficulty in designing the digital filter that is used to translate duty cycle information into digital word.

2.6.5 Dual slope ADC

Integrating ADCs are also called dual slope ADCs. These types of ADCs are having three parts; integrator, comparator and a counter [18]. The basic architecture is shown in Fig. 2.8.

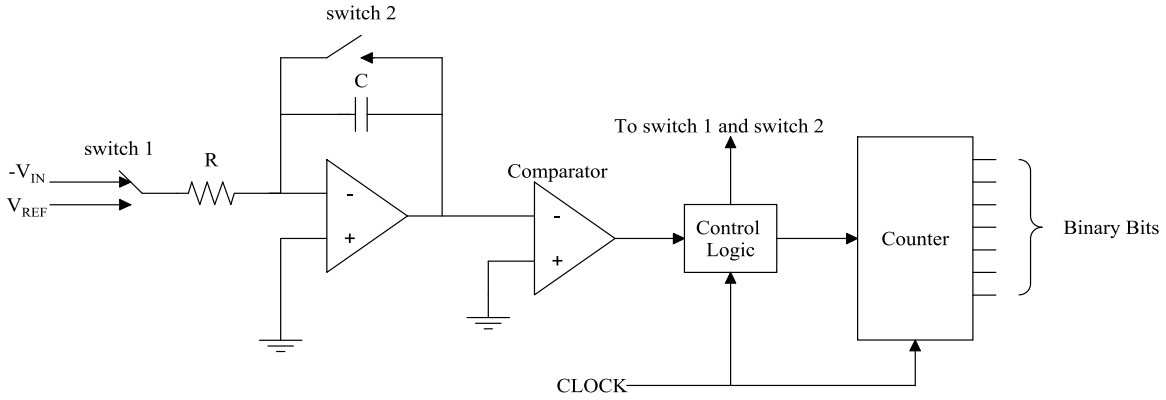


Fig. 2.8 Architecture of Dual slope ADC

The op-amp which is functioning as an integrator is used to generate a reference ramp signal that compares with input signal by a comparator. The input voltage (V_{IN}) is integrated for a predetermined time interval that matches to the highest count of the internal counter. At the ending of this time period, the system resets its counter and an opposite polarity is applied to the integrator input (V_{REF}). When polarity signal which is opposite starts functioning, the integrator de-integrates till its output achieves zero. At this stage, the counter is discontinued and the integrator is reset. Charge which has been attained by the capacitor within the integrator during integrating interval must be equal to that lost during de-integrating interval. During this condition, the binary output is directly proportional to the ratio of these time durations ($T_{INT}/_{TDE-INT}$). The dual slope ADC timing diagram is shown in Fig. 2.9.

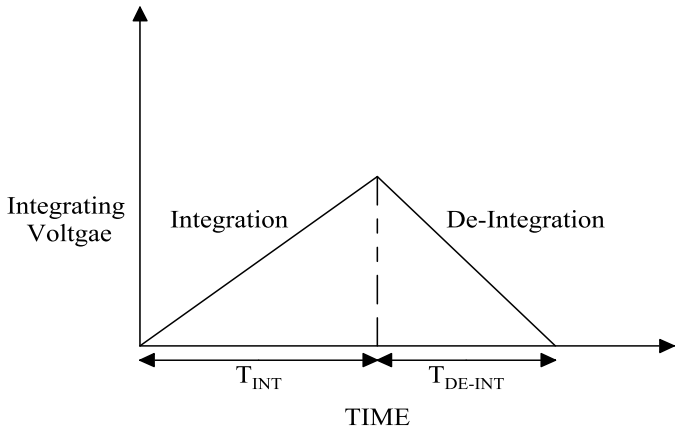


Fig. 2.9 Timing diagram of dual slope ADC

$$(V_{IN}/V_{REF})= (T_{INT}/T_{DE-INT})$$

This ADC produces output with superior noise immunity. Due to this reason it is highly useful for high accuracy applications. The other advantage of this structure is that it keeps away the use of DAC in the structure which reduces the design complexity. The main disadvantage of this ADC is that it is only suitable for low bandwidth input signals.

2.7 Comparison of different ADC architectures

Depending upon the conversion method, encoding method, conversion time, size, resolution and sampling frequency ADCs can be chosen for the specific application [16]. All families of converters are speed up with the CMOS process developments. This also increases the power consumption of data converters. The following table (Table 2.4) gives a brief summary about the different types of ADCs.

Table 2.4 Comparison of different ADC architectures

Architecture of ADC	Pipeline ADC	Flash ADC	SAR ADC	Sigma-Delta ADC	Dual slope ADC
Selection of ADC	Applications with medium speed and medium to high resolution are required	Highly used in high speed applications with low resolution (3 to 5 GHz)	Used in medium resolution applications with low speed	Applications where low to medium speed with high resolution required	Used in applications where high resolution and low bandwidth are required

Conversion method	Serial conversion (For N bit ADC requires N clock cycles)	Parallel conversion with the help of 2^N-1 comparators	Binary search algorithm is used	Integrator, comparator and single bit DAC constitutes the conversion	Integrator and comparator makes up the conversion
Encoding method	Digital correction logic	Thermometer to binary code encoder	Successive approximation	Digital filter	Analog integration
Disadvantage	Cannot be used in high speed applications	Large die size and high power consumption	requirement of an anti aliasing filter	For higher order ADCs, high order DAC required	Slow conversion rate
Conversion time	With increased resolution, it increases linearly	Independent of resolution	With increased resolution, it increases linearly	Trade off between noise free resolution and data output rate	Conversion time doubles with each bit of increase in resolution
Optimum Resolution	12 to 16 bits	4 to 8 bits	10 to 16 bits	14 to 20 bits	16 bits (typical)
Sampling Frequency	10 MHz to 100 MHz	100 MHz to 5 GHz	50 KHz to 500 KHz	100KHz to 500 MHz	40 KHz to 100KHz

Die size	With increase in resolution, size increases linearly	Increases exponentially as resolution increases	With increase in resolution, size increases linearly	Size is not having any change with increase in resolution	With increase in resolution, size will not change

2.8 ADC characterization parameters

Analog signals have a continuous range of values on the real number line. ADC produces a digital output based on analog input. The ADC should estimate every analog input level with one of the digital output code. The output of ADC is a digital data which depends upon the resolution of the converter. The number of bits that ADC utilizes to represent the analog input is the resolution of the ADC. The resolution is not a sign of accuracy of the converter, but just indicates to the number of output bits in it.

In order to determine the performance of the converter, different performance specifications are to be utilized. ADC specifications [18] are generally classified into two categories.

- Static (DC) characteristics
- Dynamic (AC) characteristics

DC characteristics are related to the static transfer function of the ADCs and AC characteristics deals with the dynamic performance of the converter.

2.8.1 Static characteristics

It mainly includes resolution, gain error, offset error, quantization error, conversion speed, integral non linearity and differential non linearity.

2.8.1.1 Resolution

The resolution of an ADC is defined as the number of output bits of an ADC. Generally flash ADC is used for low resolution applications and other types of ADCs are used for medium to high resolution applications.

2.8.1.2 Quantization error

The conversion of the sampled signal from continuous level to discrete level is called quantization and is achieved with the help of a quantizer. In quantization, the sampled signal is estimated to definite levels. These signals are then allotted integer numbers depending on their levels. But due to finite number of amplitude levels are utilized for quantization, this

process sets up an error called the quantization error. In other words, the variation between the real analog value and the digital value that is quantized is called quantization error. This error is either due to rounding or truncation. Quantization is included to some degree in digital signal processing, since the procedure of characterizing a signal in digital format normally includes rounding.

If N bits (2^N quantization levels) are used to represent a full scale voltage of $\pm V_{REF}$, then the step size of the quantizer (Δ) is determined by

$$\Delta = \frac{2V_{REF}}{2^N} \tag{2.1}$$

This is the smallest value with which the input can be quantized. This is called the resolution or least significant bit (LSB) of the quantizer. Each analog input is restricted to within $\pm\Delta/2$ of a quantization level. Thus the quantization error (ε) stretches out in the range $(-\Delta/2, \Delta/2)$.

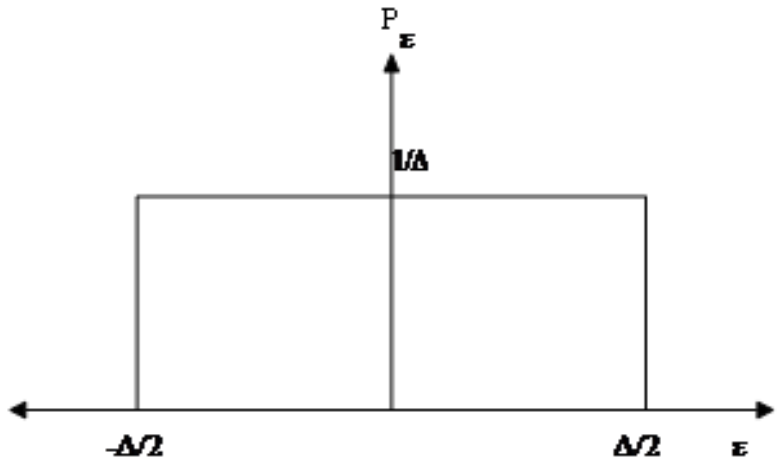


Fig. 2.10 Probability density function of the quantization noise

The quantization error is always deterministic as the actual value of the input signal at the sampling instant can be known. So it is only a function of the input signal. But if the signal distribution is uniform, all the levels are assigned equal probability. The quantization error can be supposed to be a white noise process with a uniform probability density function as shown in Fig. 2.10. With this assumption of uniform distribution of the quantization noise, the noise power is given by the variance of the quantization error as follows

$$\sigma^2 = \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 . \frac{1}{\Delta} d\varepsilon = \frac{\Delta^2}{12} \tag{2.2}$$

2.8.1.3 Conversion speed

Conversion speed of that ADC is defined as the amount of analog input that can be converted by an ADC in one second. Speed of conversion is a crucial parameter in selecting the type of an ADC because high speed applications require a high speed ADC.

2.8.1.4 Offset error

The variation in the performance of an ADC at zero is called an offset error. For example in an ideal ADC the first transition from '000' to '001' happened at voltage equals to half LSB, as shown in Fig. 2.11(a). But in the actual ADC the transition from '000' to '001' occurred exactly at voltage equals to 1 LSB as shown in Fig. 2.11(b). The deviation from the actual transition voltage from the ideal one is an offset error. Offset error is a constant value. In this case, the offset error is half LSB. This error can easily be abolished from the conversion system by just calibration.

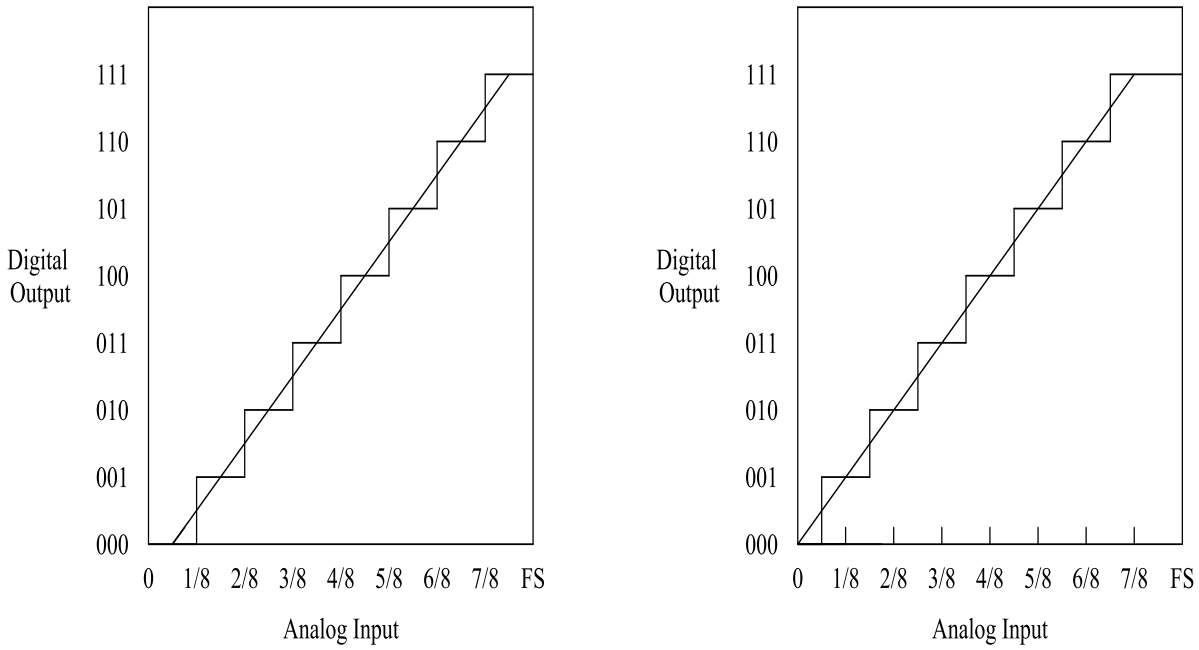


Fig. 2.11 (a) ADC characteristics with offset (b) Ideal ADC characteristics

2.8.1.5 Gain error

The difference in slope of the straight lines (from zero to full scale value) of an actual ADC to an ideal one is called gain error. The gain error can also be removed from the ADC by calibration. Fig. 2.12 shows the gain error in the ADC

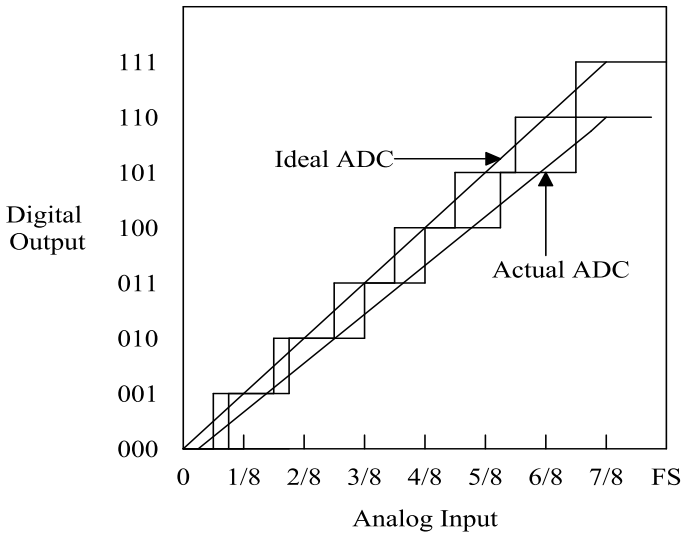


Fig. 2. 12 Gain error in ADC

2.8.1.6 Differential Nonlinearity (DNL)

It is the variation between two successive transition codes point in the input axis from the value of ideal voltage of 1 LSB with all other errors are set to zero. In other words it is the variation between actual code width of a non ideal ADC and the ideal ADC. Fig. 2.13 shows an ADC with DNL. It is not possible to eliminate its effects with calibration.

DNL = Actual step width – Ideal step width

$$DNL(i) = \frac{code(i+1) - code(i)}{1LSB} - 1 \tag{2.3}$$

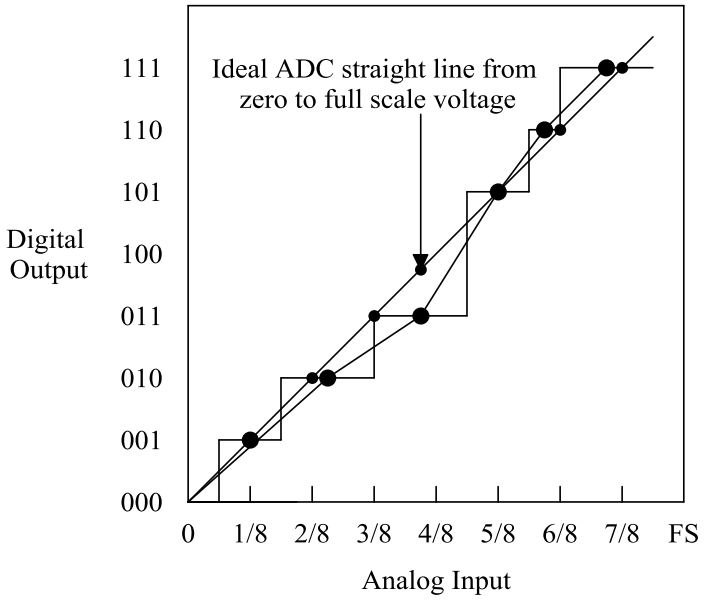


Fig. 2. 13 Non ideal ADC with DNL and INL

2.8.1.7 Integral Nonlinearity (INL)

The maximum deviation in between straight lines passing through the end points of input/output characteristics of an ideal converter to the actual one with all other errors are set to zero is called integral nonlinearity. DNL errors add together to produce a total Integral Non-Linearity (INL). Fig. 2.13 shows an ADC with INL. It is also not possible to remove its outcome with calibration.

$$INL(i) = \frac{code(i) - (1LSB \times i + code(i))}{1LSB} \tag{2.4}$$

2.8.2 Dynamic characteristics

All real ADCs experience from performance degradation from an ideal ADC because in all real ADCs the noise sources and distortion processes are present. These imperfections can be calculated by dynamic performance of the ADC. Distortion measurement is obtained by inputting a sine wave to the system. The analog response is first calculated and then evaluated in the frequency domain. The processed waveform is converted into its spectrum using the Fast Fourier Transform (FFT) algorithm. The computations are done based on the frequency components.

2.8.2.1 Signal to quantization ratio (SQNR) or SNR

The ratio between the input signal power and the total noise power due to quantization is defined as the signal to noise ratio (SNR).

Mean square value of quantization error $=\Delta^2/12$

If the input signal is A sinωt, then signal power $=A^2/2$

For an N bit ADC, full scale range is $2^N \Delta$

$A_{max} = 2^{N-1} \Delta$

Maximum signal power = $((2^{N-1} \Delta)^2)/2$

Noise power = $\Delta^2/12$

Peak SQNR = $(((2^{N-1} \Delta)^2)/ (2* \Delta^2/12))$

$=3. 2^{2N-1}$

SQNR in decibel $=10 \log_{10} (3.2^{2N-1})$

$= (6.02 N+1.76)$ dB (2.5)

2.8.2.2 Signal to noise distortion ratio (SNDR)

Signal to noise and distortion ratio is similar to SNR but non linear distortion components are also taken into consideration in addition to noise. The distortion components are determined as the root of the sum of the squares of the individual harmonics.

2.8.2.3 Effective number of bits (ENOB)

ENOB is a typical measure of lowest limit of a tolerable ADC resolution for a specific SNDR.

SNR = (6.02 N+1.76) dB, where N is the resolution of ADC.

N = (SNR-1.76)/6.02

ENOB is a very fine way to check the performance of an ADC for any specific input signal and sampling frequency. The first step is to calculate the SNDR for the output of an ADC for a particular input and sampling frequency and calculate ENOB by following equation

ENOB = (SNDR-1.76)/6.02 (2.6)

2.8.2.4 Spurious free dynamic range (SFDR)

Spurious Free Dynamic Range (SFDR) is ratio of signal power to the highest spurious spectral component power or in other words SFDR is the variation in amplitude between the signal and highest spur. As the input power is increased, the SNDR first increases and reaches a maximum and then decreases because of distortion components or spurs. The range of input for which the SNDR is greater than zero is termed as SFDR. SFDR is an important specification in communications systems because it characterizes the smallest value of signal that can be differentiated from a large interfering signal. SFDR can be specified with respect to full scale (dBFS) or with respect to the actual signal amplitude (dBc).

2.9 Selection of ADC architecture

Among the different ADC architectures, flash architecture is the most popular candidates for a high speed design [16]. The high speed is due to the parallel comparisons between the input signal and the reference voltages in the comparator unit. These parallel comparisons make the design critical with respect to power management. Since DS-UWB technology is preferred for the application, a high speed low resolution flash ADC is used in receiver architecture. The SFDR of the proposed ADC is not less than 35 dB. To achieve this ratio, the minimum number of output binary bits required is five. The range of input frequencies that can be applied to the input of ADC is between 500 MHz and 2.5 GHz. So the sampling rate of ADC is between 1 GHz and 5 GHz. In conclusion a five bit flash ADC with a maximum sampling frequency of 5 GHz should be designed. The proposed ADC's specification is summarized in Table 2.5.

Table 2.5 Summary of the proposed ADC specification

Communication standard used	DS-UWB
Input frequency range	500 MHz- 2.5 GHz
Sampling frequency	1 GHz- 5 GHz
SFDR of ADC	>=35 dB
Minimum resolution	5 bits
ENOB	> 4 bits
Architecture of ADC	Full flash ADC
Technology used	CMOS Technology 90/180 nm

2.10 Conclusion

Ultra Wideband is a new and exciting technology standard that has the potential to revolutionise the wireless industry. Applications of UWB include military applications, biomedical health monitoring system, in-home wireless connectivity and collision avoidance system. UWB technology is compared with other communication standards such as Wi-Fi, ZigBee and Bluetooth. The two standards which are widely used for the UWB wireless communications are Direct Sequence UWB (DS-UWB) and Multi-band OFDM (MB-OFDM). The type of ADCs used in the both communication technologies is also discussed. The next section of the chapter discusses about the different types of ADCs and its usages.

The most popular ADC architectures have been considered thoroughly in this chapter. The flash ADC architecture is the fastest, the SAR ADC architecture is used for medium resolution applications with low speed, the sigma delta ADC is very useful for applications where low to medium speed with high resolution required, the pipelined ADC can be useful for various applications depending on how the sub flash ADCs are arranged and the dual slope ADCs can be applied to low bandwidth applications. All ADC architectures have tradeoffs among sampling frequency, resolution and power consumption. The next section of

this chapter deals with ADC characterization parameters which is very useful in deciding the performance of ADC. Finally flash ADC (sampling frequency of 5 GHz and resolution of 5 bits) is chosen as the appropriate architecture for the specified application. The next chapter describes about the comparator design in the proposed ADC.

CHAPTER 3

COMPARATOR DESIGN

3.1 Introduction to comparator

The comparator is a crucial part of almost all kind of analog-to-digital (ADC) converters [18]. In today's analog world, everything is digitized. As a result, we have to convert the analog data into digital data with the help of ADCs. A lot of research work is currently going on in the field of high speed low power ADCs. As the technology expands, with the help of small feature size processes, reduction in power consumption can be achieved.

Comparators play a vital role in the design of an ADC [19]. Speed, gain, power dissipation, offset and resolution are the important parameters of any type of comparators. The type and architecture of the comparator is having a considerable impact on the performance of the target application. Comparator block diagram is shown in Fig. 3.1. The fundamental aim of the comparator is to compare an input signal (V_{IN}) with a reference signal (V_{REF}) and to produce an output logic low or logic high depending on whether the input signal is greater or smaller than reference. Comparator can be considered as a decision making circuit because it makes a decision based on the value of input signal and reference signal.

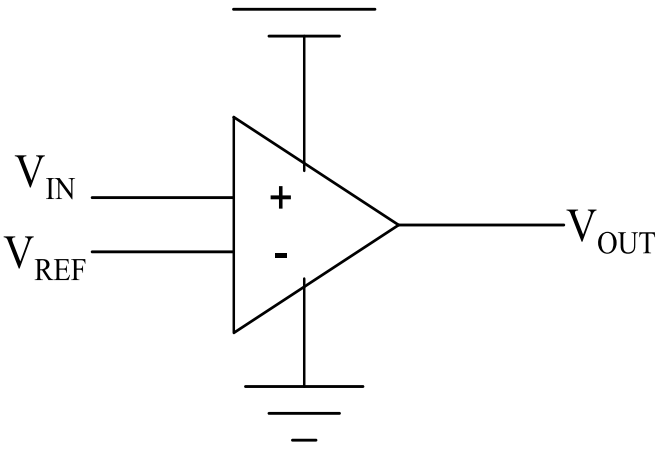


Fig. 3. 1 Block diagram of basic comparator

Fig. 3.2 shows the ideal transfer characteristics of the ideal comparator. If the reference signal is above the input signal, the comparator output (V_{OUT}) shifts to logic low and if the reference voltage is below the input signal, the output is logic high.

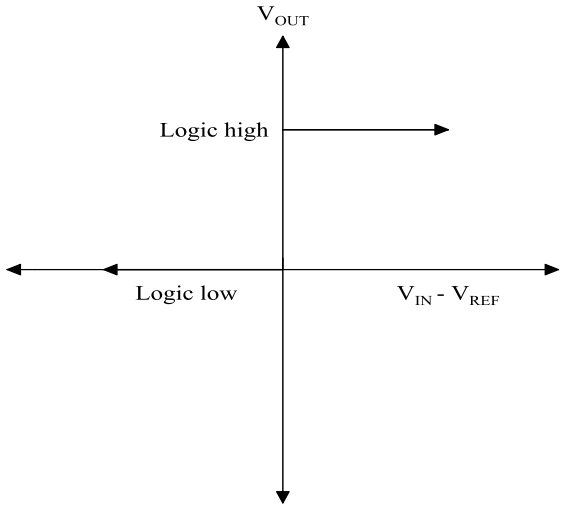


Fig. 3.2 Transfer characteristics of ideal comparator

If $V_{IN} > V_{REF}$, V_{OUT} = logic high

If $V_{IN} < V_{REF}$, V_{OUT} = logic low

In high frequency circuits, an optimum value should be made between power dissipation and speed. Slew rate requirement is one of the important factors that influences the speed of the comparator. The comparator gain also affects the power dissipation and speed. With the increase of power supply, the gain can be increased. But increasing the power supply beyond a specific limit is not possible for a specific technology. Generally comparators can be categorized into open loop and regenerative comparators. Open loop comparators are op-amps without compensation. Regenerative comparators make use of the positive feedback mechanism to carry out the comparator operation.

3.2 Comparator characteristics

Comparator performance can be specified in terms of static and dynamic characteristics [18].

3.2.1 Static Characteristics

3.2.1.1 Gain

Gain of a comparator is defined as the smallest amount of input change that makes the output transition between the two binary states. Consider a comparator with a finite gain. The comparator output makes a transition between V_{OH} and V_{OL} based on the difference between input voltage and the reference voltage (V_{IN} - V_{REF}). The transfer curve of a comparator is shown in Fig. 3.3.

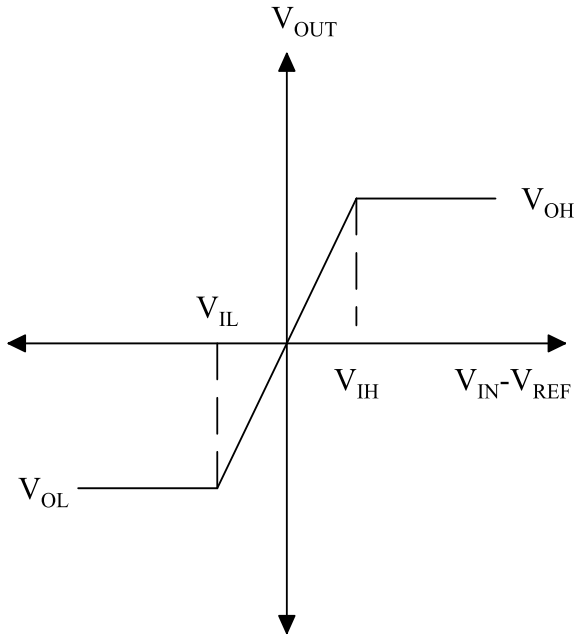


Fig. 3.3 Transfer curve of a comparator with a finite gain

$$A_V = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{3.1}$$

V_{IH} = When the output voltage is $V_{OH,}$ corresponding smallest input voltage

V_{IL} = When the output voltage is $V_{OL,}$ corresponding largest input voltage

3.2.1.2 Offset voltage

Input offset voltages can be classified into two types; systematic offset and random offset. Systematic offset in the comparator arises due to the mismatches in the threshold voltage (V_{TH}) and mismatches in the trans-conductance parameter ($\beta = \frac{\mu C_{ox} W}{L}$). Random offset is as a result of the random errors that are evolving during the fabrication. These errors results in the mismatch of ideally symmetrical devices [20, 33 and 55]. The effect of offset can be minimized but it cannot be totally avoided. In the ideal case, the output voltage makes a transition when input voltage difference crosses zero. But in practical cases, output is not going to change until input voltage differences cross a specific value. The specific voltage is called as the output offset voltage (V_{OS}). Based on the circuit topology adopted, the offset voltage varies accordingly. Fig. 3.4 shows the comparator transfer characteristics with offset voltage.

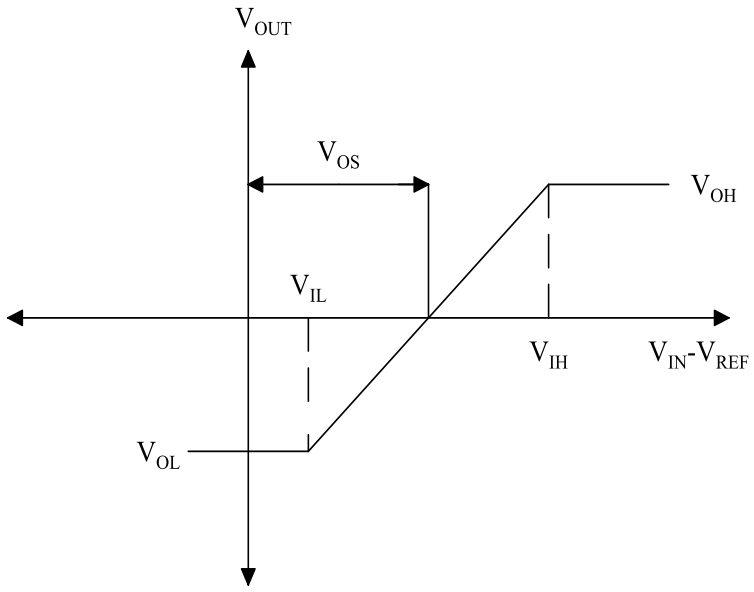


Fig. 3.4 Comparator transfer characteristics with offset voltage

3.2.1.3 Input common mode range

It is defined as input voltage ranges with which the comparator functions normally. Typically it is the range where all the transistors of the comparator remain in saturation.

3.2.1.4 Noise

Noise causes the output voltage to change from one logic level to another logic level, even when the difference between input voltage and reference voltage remains constant. The presence of noise ultimately leads to ambiguity in the switching region. The noise performance of the comparator is influenced by thermal and flicker noise. At low frequency flicker noise is significant, whereas at higher frequencies the thermal noise is more important.

3.2.2 Dynamic characteristics

3.2.2.1 Propagation delay

Propagation delay is one of the significant parameters for many applications because it limits the maximum input frequency which can be processed. Propagation delay gives an idea about the speed of the amplifier with which it responds to the applied inputs. Propagation delay is defined as the time needed for the output to attain the 50 % point of a transition after the differential input signal crosses the offset voltage, when driven by a square wave [18, 19]. Fig. 3.5 shows the propagation delay time of the comparator.

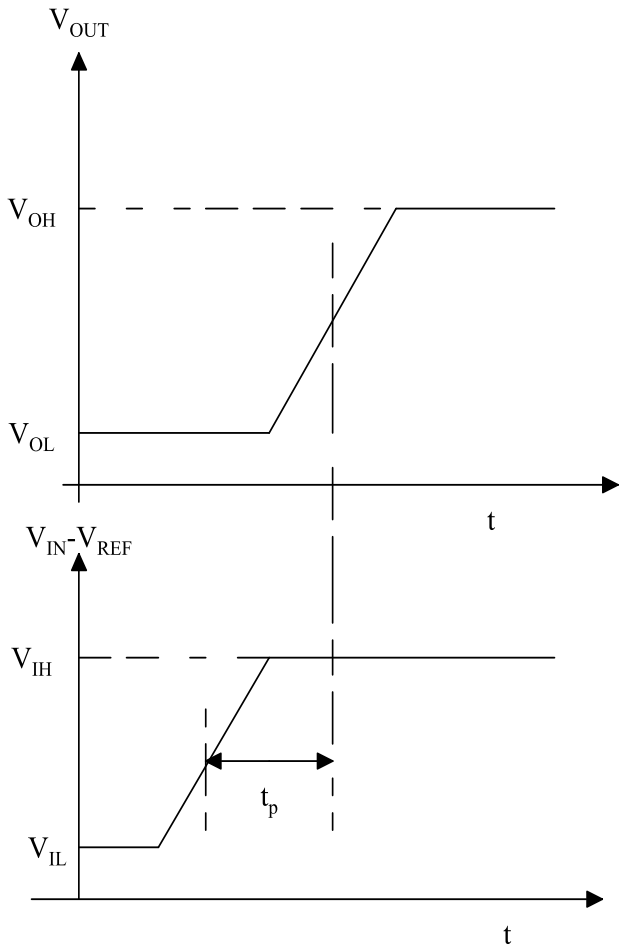


Fig. 3.5 Propagation delay time of comparator

Propagation delay time = (rising propagation delay time + falling propagation delay time)/2

$$t_p = (t_{plh} + t_{phl})/2 \tag{3.2}$$

3.2.2.2 Slew rate

Propagation delay varies in accordance with the amplitude of the input. A larger input results in a smaller delay and vice versa. There is an upper limit for an input voltage above which the voltage is not be having any effect on delay. This effect is called slewing and this introduces the term slew rate. The rate of change of output voltage is called slew rate [42].

$$\text{Slew rate} = \frac{dV_O}{dt} \tag{3.3}$$

Slew rate comes from the relationship

$I = C\frac{dV}{dt}$, where I is the current through the capacitor and V is the voltage across it. (3.4)

If the current is limited, then the voltage rate also limited. The relation between slew rate and the propagation delay can be written as

$t_p = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2.SR}$, where SR is the comparator slew rate and t_p is the comparator propagation delay time. (3.5)

3.2.2.3 Comparator sensitivity

It is defined as the minimum amount of input voltage which can be detected by the comparator and it should switch this voltage into logic high or logic low [43]. Considering a five bit flash ADC, it requires a sensitivity of 0.5 LSB (Least Significant Bit). If the supply voltage is 1.2 V, the sensitivity voltage is 18.75 mV. There are 32 different levels for five bit flash ADC. So LSB represents (1.2 V/32). Since the sensitivity is 0.5 LSB, the sensitivity voltage 1.2 V/64 = 18.75 mV.

3.3 Different types of comparators

The various types of comparators are generally classified into open loop comparators and regenerative comparators.

3.3.1 Open loop comparators

Operational amplifier without frequency compensation is called open loop comparators. Since frequency compensation mainly affecting gain and linearity, a large gain can be achieved with the help of open loop comparators. The main disadvantage of this comparator is the limited gain bandwidth product. This problem is solved by cascading a number of open-loop amplifiers which results in a larger gain bandwidth product. But this increases the area and power consumption of the implementation. Because of these disadvantages, open loop comparators are generally not used in ADC design.

3.3.2 Regenerative comparators

Regenerative comparators are mainly classified into non-clocked comparators and clocked comparators.

3.3.2.1 Non-clocked comparators

Clock is not present in these types of comparators. Non-clocked comparator contains three stages namely preamplifier, decision making and output buffer. The preamplifier amplifies the input signal difference voltage into a higher voltage level, in order to get better sensitivity of the comparator. It also separates the comparator input from the decision making stage. The decision making stage generally uses positive feedback mechanism for the operation. Positive feedback mechanism is used to determine the larger input signal from the two inputs. The output buffer amplifies the signal coming out from the decision making stage and generate

the final digital output. Fig. 3.6 shows the block diagram representation of the non-clocked comparator.

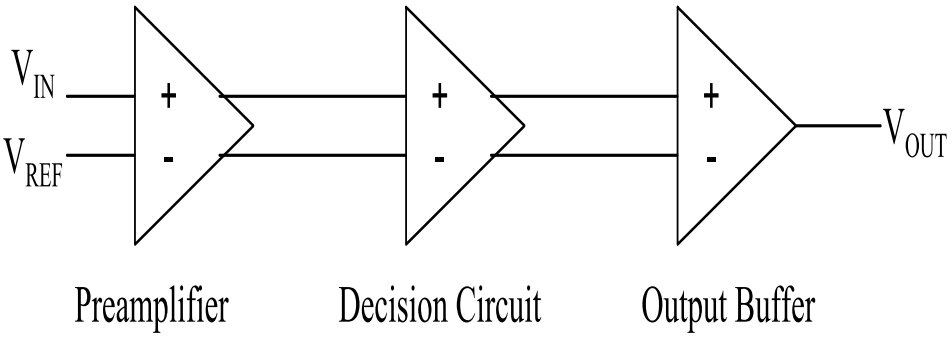


Fig. 3.6 Block diagram of non-clocked comparator

3.3.2.2 Clocked Comparators

The basic block diagram of clocked comparator is shown in Fig. 3.7. Clocked comparators are often called dynamic Comparators [23]. The speed of clocked comparators is very high because regenerative feedback mechanism is frequently used in these types of comparators.

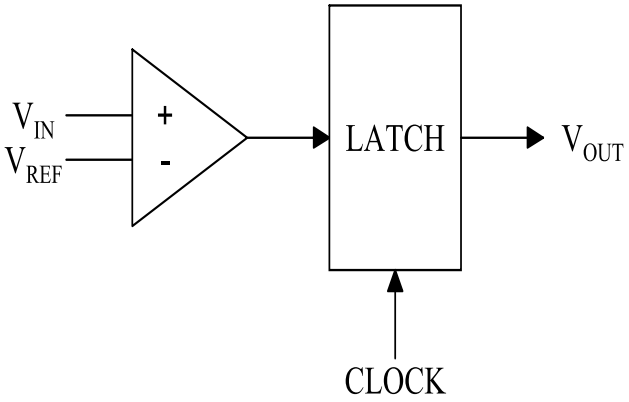


Fig. 3.7 Block diagram of clocked comparator.

A clocked comparator normally consists of two stages. The first stage interfaces input signal with reference signal. This stage determines whether the input signal is below or above the reference signal. The second (regenerative) stage contains two cross coupled inverters, where each input is attached to the other output. Any symmetric structure with this cross coupling creates regenerative feedback. The clock is used to reset the circuit and also used to get a balanced state earlier to regeneration. Clocked comparators are widely used in the design of high speed ADCs.

3.4 Design of a high speed preamplifier based pseudo dynamic latched comparator for high speed ADCs

Dynamic comparators are highly used in ADCs because of its high speed and zero static power dissipation [21, 57 and 58]. Such ADCs are extensively used in applications such as fast serial links, high speed measurement instruments and data storage systems. Dynamic comparators utilizes back to back inverters which uses positive feedback mechanism that converts small input voltage difference into full scale digital output voltage (either logic zero or logic one). The device mismatches such as threshold voltage, current factor, parasitic node capacitance, output load capacitance mismatches causes an input referred latch offset [22] which limits the accuracy of dynamic comparators. Due to this, one of the important design parameter in the latched comparator is the input referred latch offset voltage [27, 34]. Mismatch can be reduced with the help of large device used in the latching stage which effectively increases the total comparator power dissipation. Another main disadvantage of dynamic latch is the kickback noise [35]. A spike is generated at the differential input voltage signal due to high transmission current which is called kick back noise. However, kickback noise is produced, if the output nodes of preamplifier are directly attached to the regeneration nodes [38]. Both of these problems can be reduced by using a preamplifier before the regenerative latch [36].

The preamplifier amplifies the difference between the input voltages to a large voltage. Increasing the gain of the preamplifier helps to decrease the input referred noise due to the latch [29]. The preamplifier reduces the input referred offset voltage [55] and isolates the inputs from the regenerative latch stage which cuts out a direct path from inputs of the preamplifier to the latch thereby reducing the effect of kickback noise [30-32]. The preamplifier should have wide bandwidth and small gain to achieve high speed. The preamplifier latch comparator has low propagation delay as compared to the latched comparator. For further enhancing the speed, pseudo dynamic [53] comparator is also introduced. In order to separate the comparator output from large capacitive loads, inverter buffers are attached to the output of the dynamic latch comparator. The proposed design is mainly divided into different parts. The first section gives the design steps in the comparator. The later sections include design equations of the comparator, transient analysis and the properties of the proposed comparator. Layout, post layout simulation and comparison are carried out in the last sections.

The flow chart (Fig. 3.8) presents the different steps in the design of the proposed comparator.

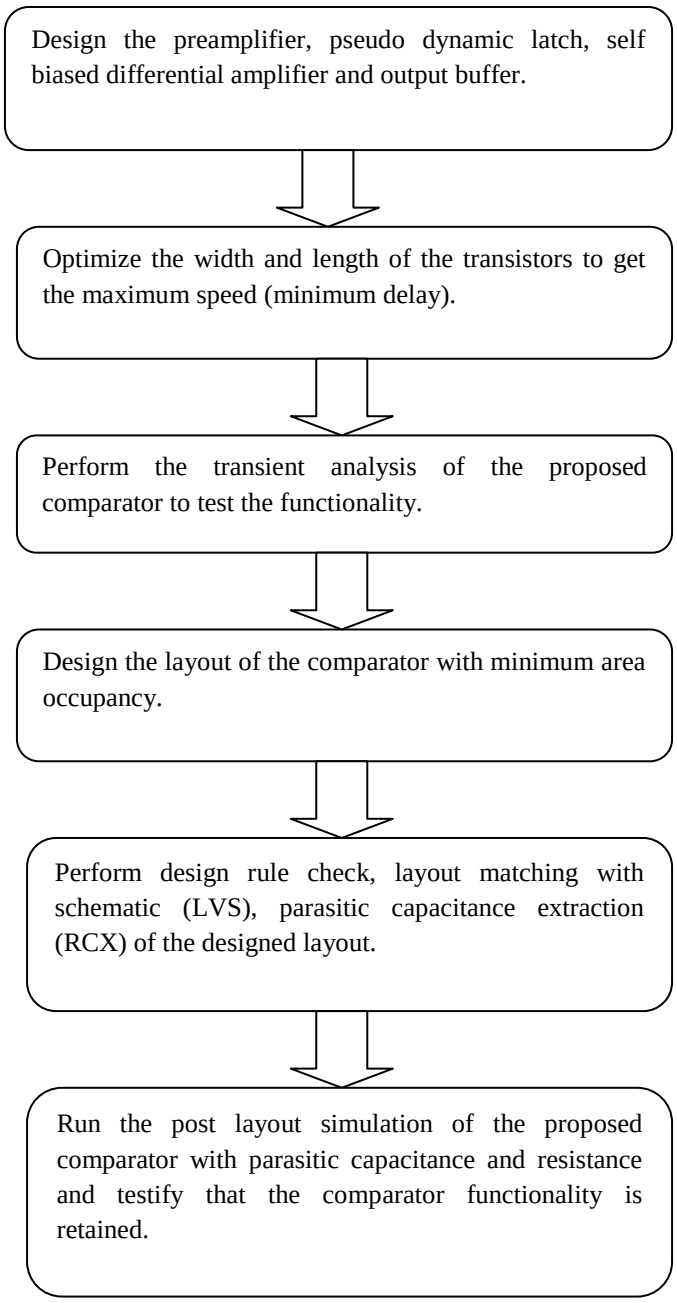


Fig. 3.8 Flowchart of the design of the proposed comparator

The typical comparator architecture which contains preamplifier, latch stage and output buffer [44, 49, 51]. The comparator is having tracking and latching modes of operation. In the tracking mode, the preamplifier is enabled and output is tracking the input. During this time, the latch is disabled. In the latching mode, the preamplifier section is disabled and latching stage is enabled. In this mode, regeneration process is happened and logic levels are produced [45]. The output of the preamplifier should not be decreased, when it is making a transition

from tracking stage to latching stage due to the presence of parasitic capacitance at the output of the preamplifier.

3.4.1 Preamplifier design

The basic function of the preamplifier is to amplify the small difference between the inputs to a large value before it is connected to the latch stage [28, 56]. The circuit response of the preamplifier and the latch are shown in Fig. 3.9. From the figure, it is clear that the preamplifier is having a negative exponential response while that of latch stage is having a positive exponential response.

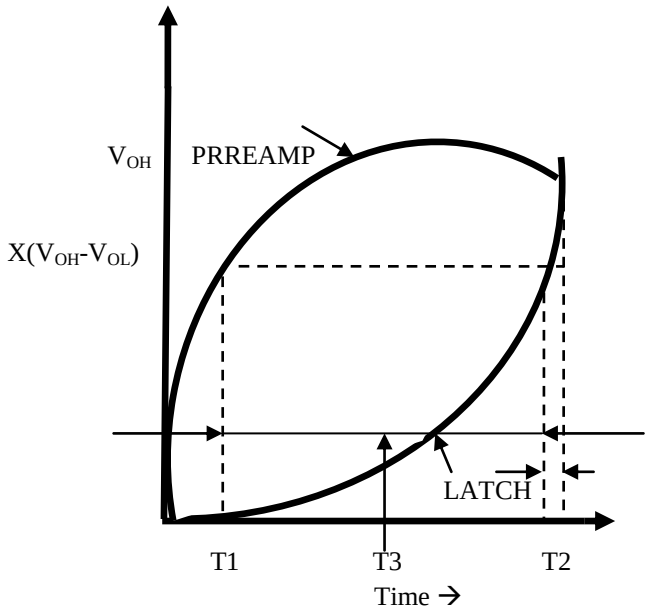


Fig. 3.9 Response of preamplifier and latch

If only latch is used, it takes a long time to reach to a logic high value (V_{OH}). The preamplifier amplifies the voltage into an intermediate voltage (x (V_{OH}-V_{OL})) within time T1 so that reaching to logic high takes less time. If preamplifier alone is used, then the time taken to reach logic high value is T1+T2+T3. So if the combination of both preamplifier and the comparator is used, it takes a time of T1+ T2 to reach V_{OH} which is comparatively a less value. Moreover preamplifier reduces the input referred offset voltage of the comparator. With the introduction of the preamplifier, offset is reduced by a factor A which is the gain of the amplifier. The offset of the comparator is given by

$V_{os,comp} = V_{os,preamp} + (\frac{1}{A})V_{os,latch}$, where $V_{os,preamp}$ is the offset of the preamplifier, $V_{os,latch}$ is the offset of the latch and A is the dc gain of the amplifier. [52] (3.6)

3.4.1.1 Existing preamplifier

Fig. 3.10 shows the one of the preamplifier circuit used in a high speed comparator. It amplifies the difference between the V_{IN} and V_{REF} and produces V_P and V_M outputs. The disadvantage of this preamplifier is that it is having a high value of comparator overdrive recovery time. For reducing the overdrive recovery time, the modified architecture is introduced. The modified architecture is shown in Fig. 11.

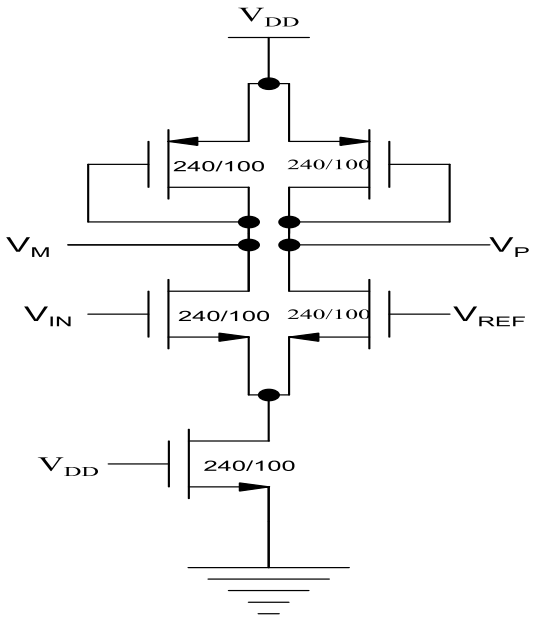


Fig. 3.10 Existing preamplifier

3.4.1.2 Modified preamplifier

Overdrive recovery time of the comparator is a speed limiting factor in high speed analog-to-digital converters [50]. When a large input is followed by opposite polarity input, a high value of overdrive recovery time is occurring. Adding an extra input CLK to this preamplifier structure reduces the comparator overdrive recovery time with excess power dissipation. In order to reduce the on resistance of the extra transistor, the W/L ratio is chosen as (360/100). Effectively it increases the speed of the comparator. During CLK=1, the preamplifier amplifies the difference between the inputs and the outputs are available at the output nodes

(V_P and V_M). When CLK=0, PMOS transistor is switched on and equalize the output nodes so that overdrive recovery time is reduced. The W/L ratio is chosen in such a way that the gain of the preamplifier gives a value of 2.5. The propagation delay with and without the extra transistor are 180 ps and 200 ps respectively.

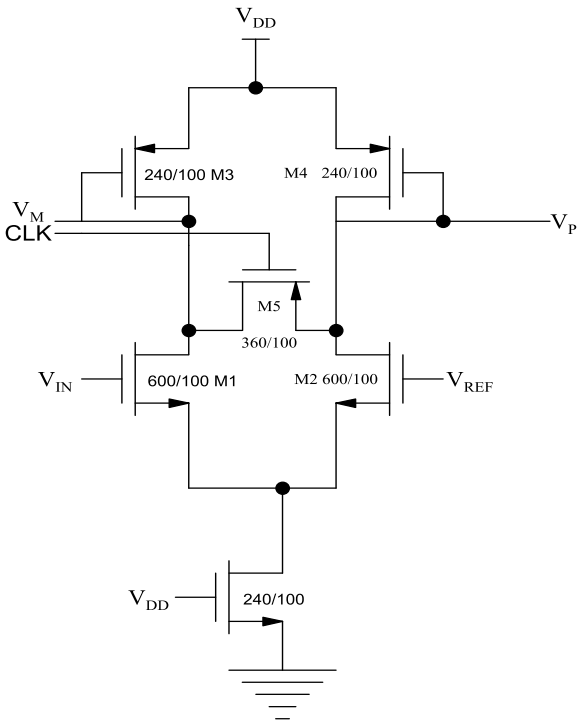


Fig. 3.11 Modified preamplifier

3.4.1.3 Modified current source architecture

MOSFET which is operating in saturation works as a constant current source. NMOS transistor connected to V_{DD} acts as a constant current source in the preamplifier [18]. The disadvantage of this current source is that through gate source capacitance, a short circuit can happen between V_{DD} and ground. In order to avoid this, modified current source architecture is introduced with the use of current mirror scheme is shown in Fig. 3.12. By adjusting the (W/L) value of M5 and keeping the (W/L) of M7 and M8 same, the identical value of drain current can be obtained what it is getting in the first case. This method is having the advantage of eliminating the direct path from V_{DD} to ground through gate source capacitance thereby introducing more safe operation of the circuit. The complete preamplifier circuit is shown in the Fig. 3.13.

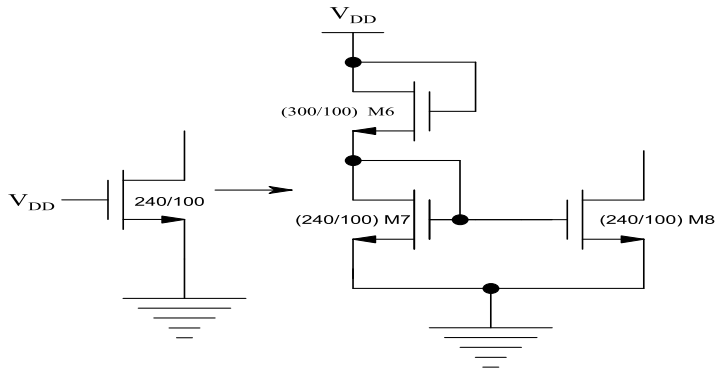


Fig. 3.12 Modified current source

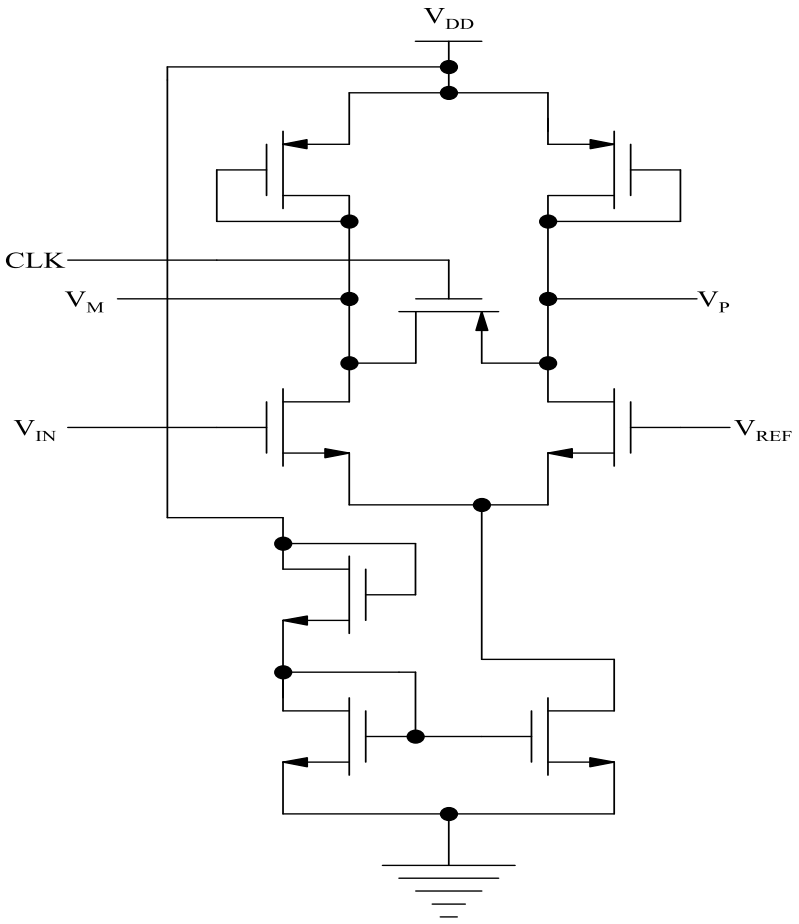


Fig. 3.13 Complete preamplifier circuit

3.4.2 Latch stage design

If the preamplifier outputs are directly connected to latch stage, a high value of kick back noise is generated [39]. In order to reduce the kickback noise effect, an inverter is added in between the preamplifier and latch stage. Even though the additional inverter delays the entire operation, the proposed comparator can drive large current to the load than a comparator without inverter. As the size of the load becomes larger, the proposed

comparator shows better speed. The power dissipation of the comparator with and without the inverter is 85.81 µW and 65.74 µW.

3.4.2.1 Existing dynamic latch

There are different ways to decrease the propagation delay of the latch. Firstly, if a large input is applied to the latch, the time required for the output to reach logic high value is less [24-26]. So it is better to apply a large input voltage to latch in order to take the merit of increasing slope of the positive exponential characteristics of the latch. Since gain-bandwidth product is a constant for a specific preamplifier, a trade-off between gain and bandwidth should be taken. Secondly, the response is fast, if the latch time constant is a small value. The propagation delay of the latch can be reduced by decreasing the pull up or pull down path delay, thereby achieving the regeneration quickly [46]. One of the dynamic latches used in high speed comparator is shown in the Fig. 3.14.

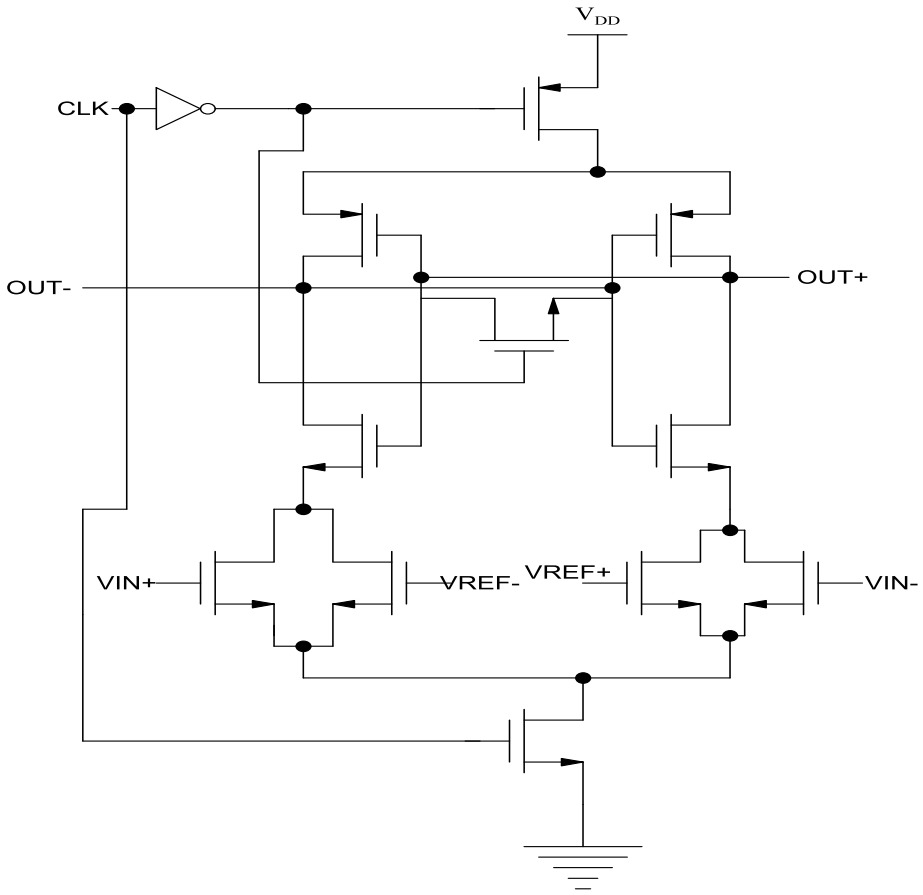


Fig. 3.14 Existing dynamic latch

When clock is high, latch is in regeneration mode and outputs are latched. When the clock is low, latch is disconnected from V_{DD} and ground. This mode is called reset mode. In the reset mode, pre-charging path is disconnected and the pass transistor which connects the

two regenerating nodes is switched onto equalize the two output voltages to approximately $V_{DD}/2$.

3.4.2.2 Proposed pseudo dynamic latch

Proposed pseudo dynamic latch schematic is shown in Fig. 3.15. Transistors M9 – M12 constitute the cross coupled inverter pair structure which forms the main regenerative loop for the latch. The sizes of these transistors are kept nominal for least capacitive effects. The equivalent (W/L) ratio of the pull up transistor is taken as (240/100) (effective value of two (480/100) transistor in parallel gives (240/100)) which is double the size of the pull down network (120/100).

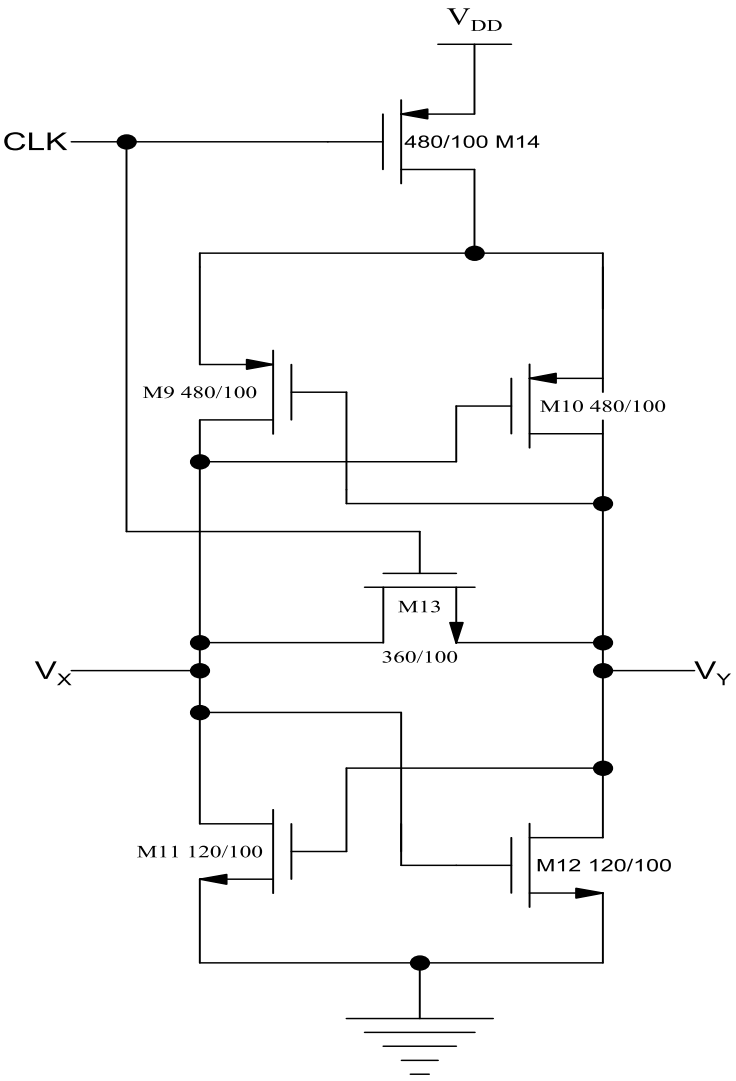


Fig. 3.15 Proposed pseudo dynamic latch

When clock is low, the latch is working in regenerate mode. Compared with dynamic latch, one NMOS pull down transistor which is connected to clock is removed in the pseudo dynamic latch. The switching transistor is used to short circuit the latch's differential nodes to a common DC level. Increasing the width of the transistor brings the DC level on both sides near to each other. To make the reset operation fast, the (W/L) of M13 should be taken as (360/100). Effectively it increases the speed of the latch by decreasing the pull down path delay in comparison with the dynamic comparator. In order to maintain the proper working of the circuit, the size of PMOS and NMOS transistors must be chosen carefully.

The disadvantage of pseudo dynamic latched comparator is the presence of static power dissipation. When clock is low, current flows from V_{DD} to ground (pull up as well as pull down path is on), that gives rise to an extra power dissipation called static power dissipation which is not present in dynamic comparators. So with the help of pseudo dynamic logic, speed of the latch is increased with an added amount of static power dissipation. When clock is high, latch is operating in reset mode and the regenerating output nodes are at a voltage $V_{DD}/2$. The propagation delay with pseudo dynamic latch is 148 ps, which is a very less value as compared with dynamic logic.

3.4.3 Output buffer

The function of the output buffer is to convert the latch output into a logic high or logic low value [32]. The circuit consists of two parts. Self biased differential amplifier and two inverters. Conventional CMOS differential amplifiers which are operating in saturation region cannot provide the switching current that is larger than quiescent current which is set by the current source device. The ability of providing momentarily high current pulses helps the self biased differential amplifier suitable for high speed comparator applications. The differential amplifiers are complimentary to each other. The n-type devices works in a push-pull style with a matching p-type device.

With the help of negative feedback, the differential amplifiers are self biased. The advantage of this is that active region biasing is having less sensitivity towards variations in temperature, processing and supply. When $V_X = 1$ and $V_Y = 0$, node potential at X goes down which makes the output node to be charged to V_{DD} through a path shown in Fig. 9. In the similar way when $V_X = 0$, $V_Y = 1$, node potential at X goes up which makes the output node to be discharged to ground through a path shown in Fig. 3.16.

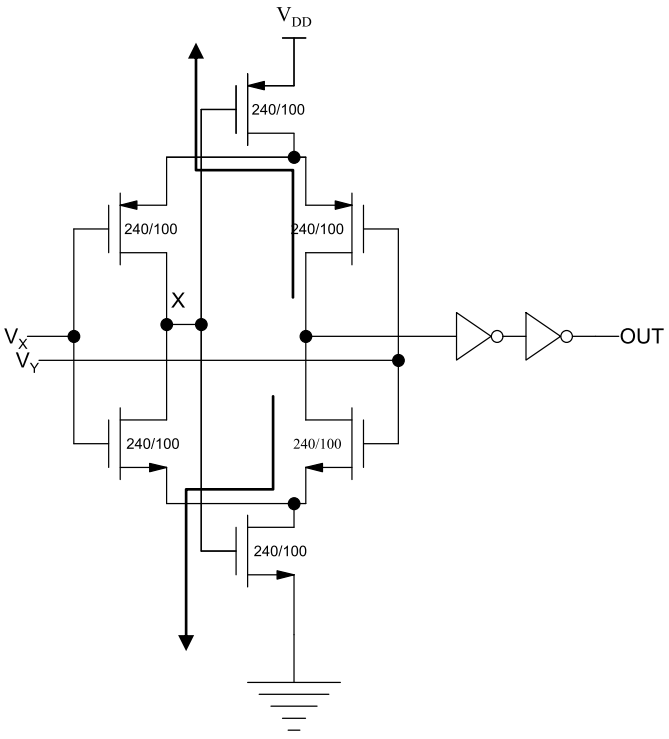


Fig. 3.16 Output buffer

The inverters are added to separate any capacitance load from the self biased differential amplifier. The schematic of the circuit is shown in Fig. 3.16. The equivalent values of (W/L) ratio of the pull up transistors are chosen as double that of the pull down transistors to match the delay.

3.5 Block diagram of comparator

Proposed comparator consists of mainly three parts; Preamplifier, pseudo dynamic latch and output buffer. Complete block diagram of the comparator is shown in Fig. 3.17.

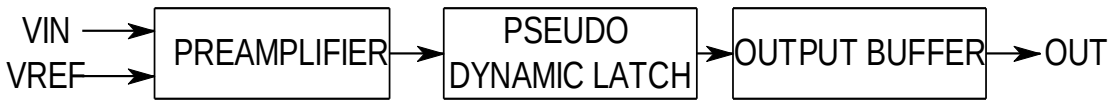


Fig. 3.17 Block diagram of Comparator

3.6 Transient analysis of the proposed comparator

Run the simulation for a time period of 10 ns and check the functionality of the comparator. Simulation results (Fig. 3.18) show that the comparator is working fine at 8 GHz frequency with a V_{DD} of 1.2 V. Power dissipation the comparator is 92.48 µW at 8 GHz.

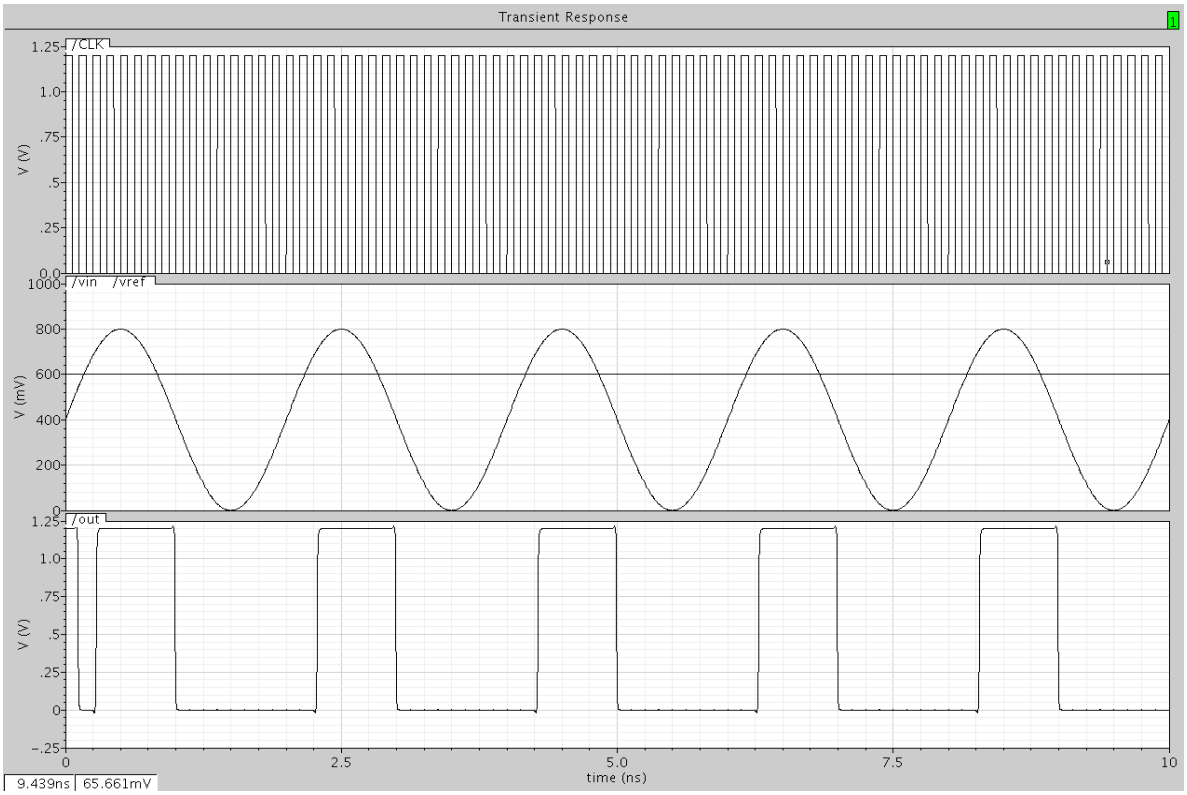


Fig. 3.18 Transient analysis of the proposed comparator

3.7 Properties of the proposed comparator

3.7.1 Offset voltage

Offset voltage is calculated by plotting the transfer curve. Transfer curve is a plot between input and output with one input is varying between 0 to V_{DD} and another one is keeping at a constant dc voltage. The transfer curve is shown in Fig. 3.19.

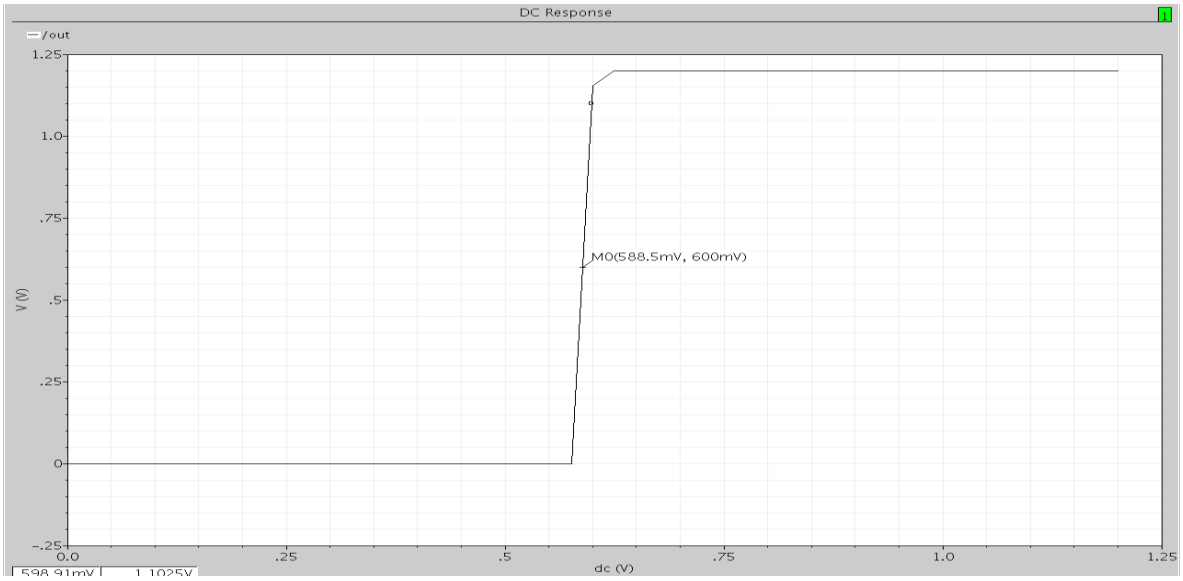


Fig. 3.19 Transfer curve of the comparator

Transfer curve shows that the proposed comparator is having an offset voltage of 11.5 mV. In this we are taking the assumption that the input referred offset voltage is just due to input differential pair threshold mismatches. So monte carlo simulation is not performed.

3.7.2 Maximum gain

The derivative of the transfer curve gives the maximum gain of the comparator. Fig. 3.20 shows that the proposed comparator gives a maximum gain of 48.11.

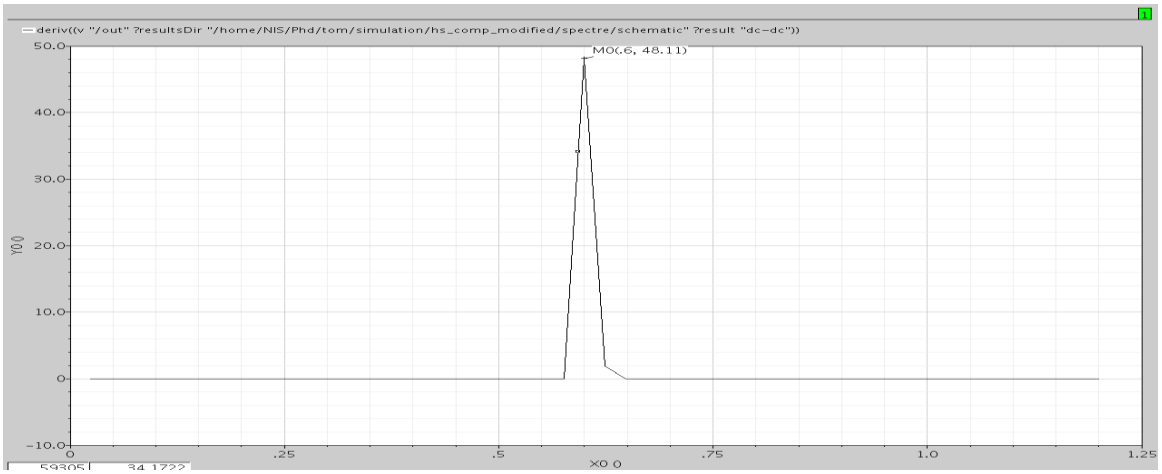


Fig. 3.20 Maximum gain of the comparator

$A_v = \frac{V_{OH} - V_{OL}}{\Delta V_{IN}}$, where V_{OH} and V_{OL} are the high and low logic states and A_V is gain (3.7)

V_{OH} =1.2 V, V_{OL} =0 V and A_V = 48.11

ΔV_{IN} =24.94 mV

Total gain = gain of the preamplifier x gain of the latch

Gain of the preamplifier

$$A_{v1} = \frac{g_{m1}}{g_{m3}} = 2.5 \quad (3.8)$$

$$g_m = \sqrt{2K_p \frac{W}{L} I_D} \quad (3.9)$$

Gain of the latch $A_{v2} = \frac{g_{m9} R_{13}}{2 - g_{m11} R_{13}} = 20$ (3.10)

$$R_{13} = \frac{L_{13}}{uC_{ox}W_{13}(V_{GS} - V_T)} \tag{3.11}$$

$$A_V = A_{v1}A_{v2} = 50 \tag{3.12}$$

It is matching with the simulation results of Fig. 3.20.

3.7.3 Kick back noise

The large difference on the regeneration nodes are connected to the comparator input through parasitic capacitances and disturb the input voltages. So the inputs of the comparator should be isolated from the regenerative part of the comparator in order to reduce the kick back noise [54]. If otherwise, it degrades the performance of the comparator. A sampling switch can be used to reduce the kick back noise. The sampling switch is positioned before the comparator inputs. In regeneration phase, the sampling switches are kept open and detach the inputs from the remaining portion of the circuit. To reduce the effect of charge injection, the size of the switches should be made small. Isolation transistors are used to separate the differential pair from the regenerative nodes. Isolation transistors are generally a group of NMOS transistors managed by the clock or set of inverters which is positioned between the differential pair drain and regeneration outputs. In the regeneration phase, the isolation transistors are switched off avoiding the charge injection to the differential inputs. This reduces the kickback noise effect [37-40, 48]. With the help of preamplifier also, kick back effect can be reduced. The pre-amplifier can be placed before the comparator in order to decrease the kickback effect. In the design of this comparator, kick back noise is largely reduced by the use of preamplifier and the introduction of an inverter between preamplifier and the regenerating nodes. The simulation result of the kick back noise is shown in Fig. 3.21. Average value of the kick back noise is 1.2 µV.

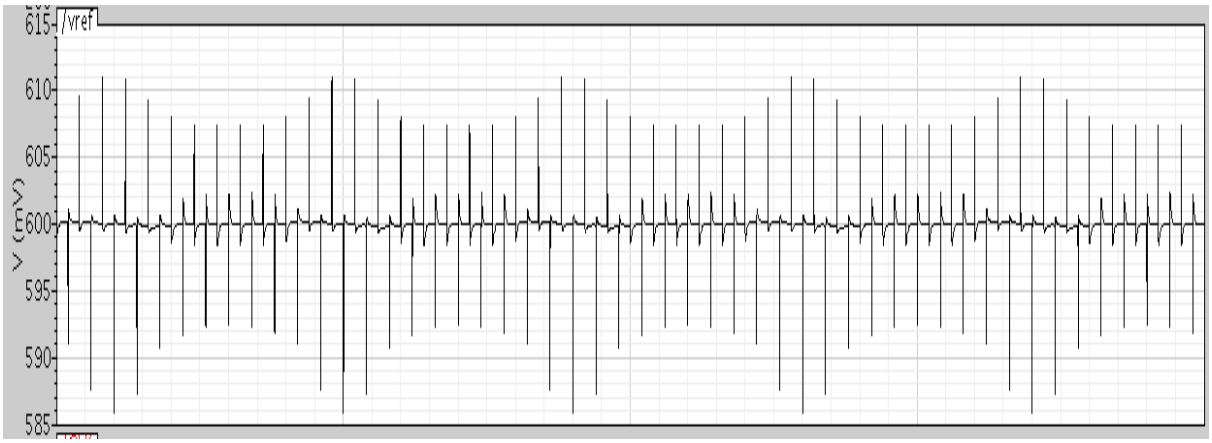


Fig. 3.21 Kick back noise simulation

3.7.4 Hysteresis

The hysteresis is defined as the difference between the two values of input voltages when there are transitions [41]. Noisy signal can occur in any applications and it is unacceptable. It can be reduced with the help of adding a small amount of hysteresis to the comparator. A noisy input signal can cause the output to switch rapidly back and forth, if the comparator is having only a single threshold value. Hysteresis introduces another threshold value into the comparator. So the switching occurs only when the comparator crossing the second threshold value which is effectively increasing the noise immunity of the circuit. With the help of a positive feedback a small amount of hysteresis is added into the comparator (7.2 mV approximately) which is calculated from the transient simulation of the comparator.

3.7.5 Meta-stability error

A comparator is said to be in a meta-stable state if the output of the comparator cannot be understood by succeeding digital logic [28, 105]. Meta-stability is a dilemma that occurs in all latching comparators when the input is close to the comparator transition point. The problem takes place when the comparator takes extra time to switch to a valid output state than is available in the sample interval. This meta-stability delay is random and can switch the output to the wrong logical levels that cause system malfunction or failure. The figure demonstrates the voltage transfer characteristics of two back to back connected inverters. Two stable points are there for inverter; V_{DD} or ground. The midpoint at which the two curves intercept each other is meta-stable point as shown in the Fig. 3.22. Ideally the meta-stable point of an inverter is at midway of the input range i.e. $V_{DD}/2$. If the first inverter input slightly departs from $V_{DD}/2$, the second inverter output moves to one of the stable states. During this range, the output is random and can change to wrong logic level.

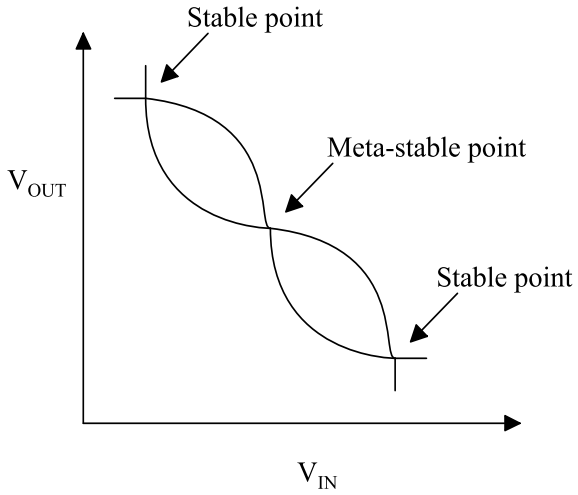


Fig. 3.22 VTC of back to back connected two inverters

This probability of meta- stability error can be made very low through proper circuit design techniques but never made to be zero. One of the solutions is to use of two cascaded comparator stages which is working on opposite phases of the clock, making the total evaluation time period is one whole clock cycle or use PMOS and NMOS as the switching device to enable the different stages of operation. This improves the effective gain approximately by a factor exp (T/τ) which decreases the probability of bit errors by several orders of magnitude. The second method is implemented in the design of the comparator. Choosing the optimal device size, aspect ratio and circuit configuration looks the most feasible approach to improve robustness against meta-stability at the circuit design stage.

Probability of meta-stability error can be expressed as

$$P_{error}(T) = \frac{2V_l}{A_v V_R} * e^{-T/\tau} \tag{3.13}$$

A_v = Gain of the comparator

V_R = maximum amount of change in the voltage at the input of the comparator that can be made without causing a transition in the output of the comparator.

V_l = Final output voltage of the comparator

T = time constant of the latch

The proposed comparator is having a voltage gain of 40 which reduces the probability of error by a factor of 40.

3.7.6 Propagation delay

The propagation delays (t_{plh} and t_{phl}) determine the input to output signal delay during the low to high transitions and high to low transitions of the output [19]. The propagation delay in the non inverting circuit is defined in the following way. t_{plh} is the time delay between transition of the rising input voltage (zero to 50% of the voltage) and the transition of the rising output voltage (zero to 50% of the voltage). t_{phl} is the time delay between transition of the falling input voltage (100 to 50% of the voltage) and the transition of the falling output voltage (100 to 50% of the voltage). The propagation delay waveform is shown in Fig. 3.23. Figure shows that the proposed comparator is having t_{plh} value of 142 ps and t_{phl} value of 154 ps.

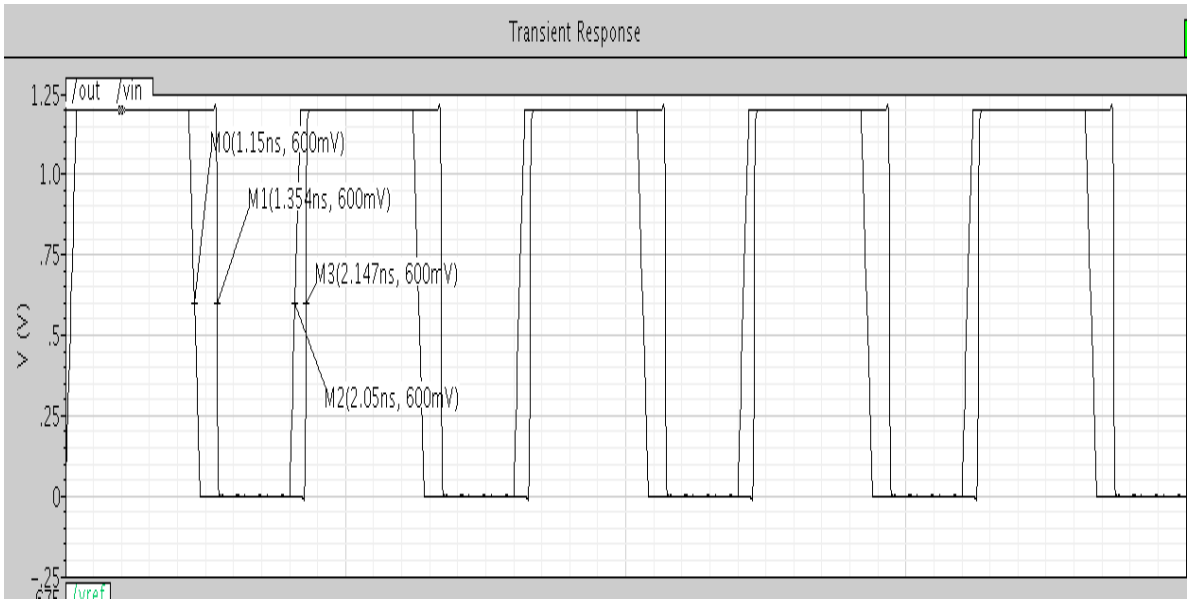


Fig. 3.23 Propagation delay

$t_p = (t_{plh} + t_{phl})/2$

= 148 ps

The propagation delay of the latch is given by

$t_p = t_l \ln \frac{V_{OH} - V_{OL}}{2\Delta V_o}$, where t_l = latch constant, V_{OH} and V_{OL} are the output logic states high and low and ΔV_O = input to the latch (3.14)

$t_l = 0.67 C_{ox} \sqrt{\frac{WL^3}{2K'I}}$, where C_{ox} is gate capacitance per unit area, W, L are the width and length of the transistors and I is the initial current through latch. (3.15)

= 120 ps.

The latch stage in the comparator contributes major portion of delay in the comparator stage. The remaining delays are added by the preamplifier and the buffer stages. So it is approximately equals with propagation delay which calculated from the simulation results.

3.8 Pre-layout process corner simulation results

The Table 3.1 contains the different corner definitions used in the simulation of the comparator.

Table 3.1 Corner specifications

Corners	V_{DD} (in Volts)	Temperature (in degree Celsius)
TT	1.20 V	27
SS	1.08 V	80
FF	1.32 V	-20
SF	1.20 V	27
FS	1.20 V	27

The Table 3.2 gives the pre-layout corner simulation results of the comparator.

Table 3.2 Pre-layout simulation with process corner simulations

Corners	TT	SS	FF	SF	FS
Propagation delay (ps)	148	252	76	160	94
Offset voltage (mV)	11.5	12	10.6	11.8	14
Gain (dB)	48.11	47.2	47.9	48.02	42.36
Power dissipation (µW)	92.48	80.32	120.47	86.68	113.73

3.9 Layout of the proposed comparator

Layout of the proposed comparator is shown in Fig. 3.24. Die area of the layout of the proposed comparator is 17.605 µm × 8.57 µm.

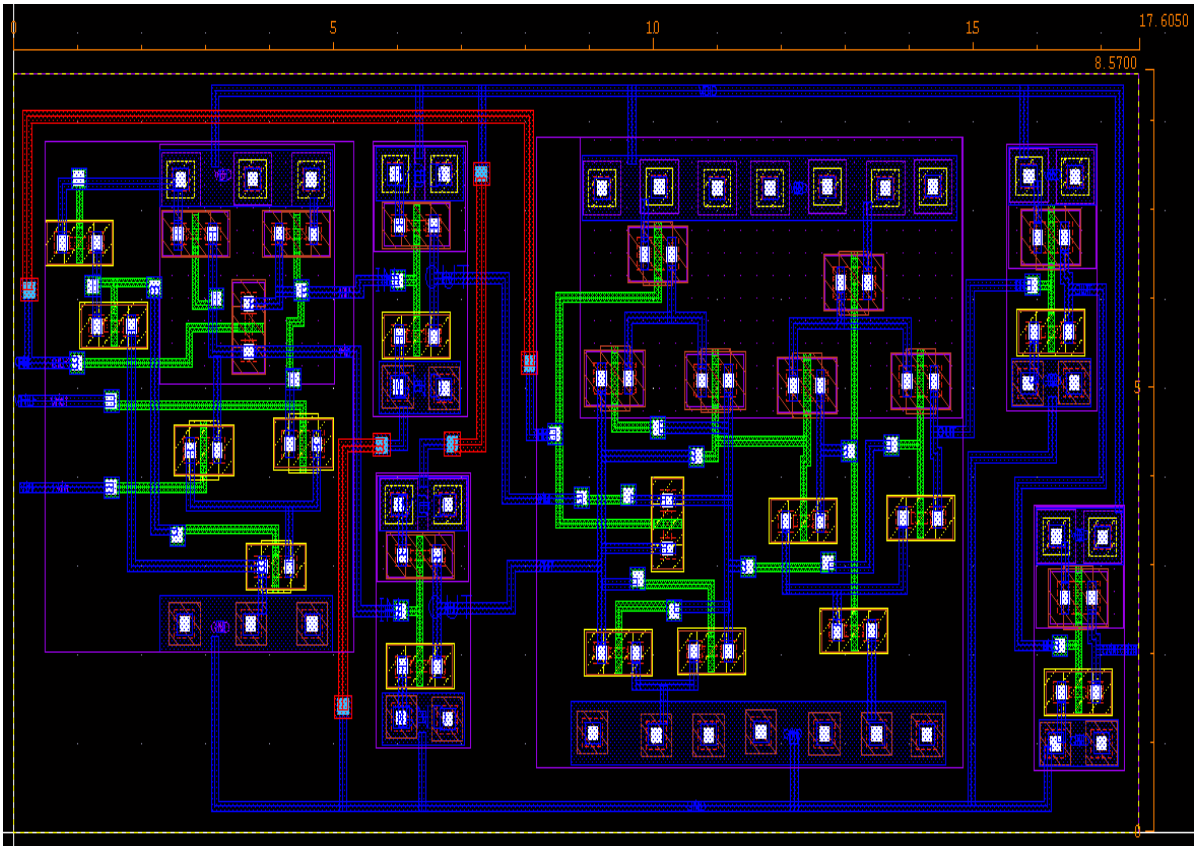


Fig. 3. 24 Layout of the proposed Comparator

3.10 Post layout simulation

Post layout design is used to verify the completed design. After designing the layout, design rule check (DRC) operation is performed. Post layout simulation provides a clear assessment of circuit speed, influence of the circuit parasitic (parasitic resistances and capacitances) and any glitch that occurs due to signal delay mismatches. After successfully passing DRC, layout versus schematic checking (LVS) is done. After successful completion of the LVS, parasitic capacitance extraction (RCX) is done. Then a layout view of av_extracted is obtained with parasitic capacitances and resistors. With the use of av_extracted view, post layout simulation is performed. The simulation results include the effects of parasitic capacitances and resistances which are extracted using RCX. Transient analysis of post layout simulation is show in Fig. 3.25. The power dissipation of post layout simulation is 128.8 µW which is larger value in comparison with 92.48 µW (pre layout power dissipation). This is because of the presence of parasitic capacitances and resistors in the circuit which is not present in the pre-layout design. The simulation result shows that comparator is working well in the post layout simulation with increased power dissipation.

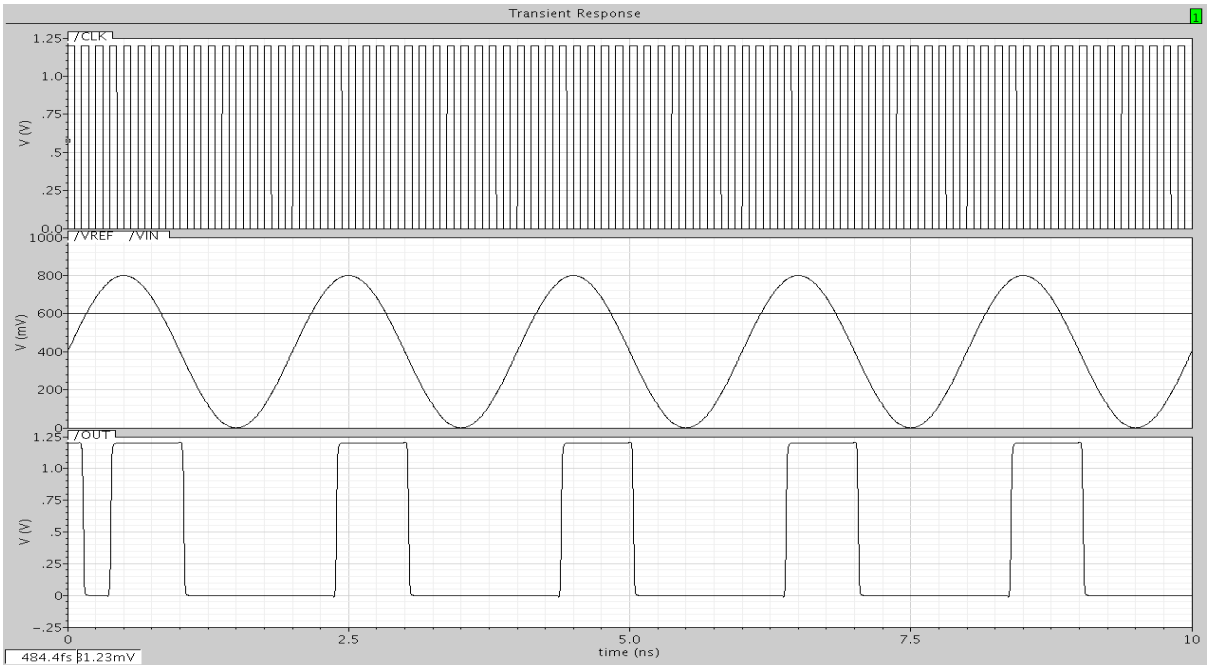


Fig. 3. 25 Post Layout Simulation of the proposed comparator

The propagation delay of the comparator is increased to 156 ps due to the effects of parasitic capacitances and resistances. The average value of the kick back noise is increased to 1.5 µV since parasitic capacitance increases the coupling of regeneration node voltage to the input. The offset voltage after post layout simulation is 11.5 mV.

3.11 Post layout corner simulation results

Table 3.3 gives the post layout corner simulation results of the comparator.

Table 3.3 Post layout corner simulation results of the comparator

Corners	TT	SS	FF	SF	FS
Propagation delay (ps)	156	283	94	174	118
Offset voltage (mV)	11.5	12	10.6	11.8	14
Gain (dB)	48.11	47.2	47.9	48.02	42.36
Power dissipation (µW)	128.8	94.14	142.87	102.13	136.24

The corner "SS" has a high value of propagation delay with an ultra low power dissipation. Since large value of propagation delay limits the speed of operation, "SS" is not used in comparator design. The corner "FF" is having a high value of power dissipation with low propagation delay. Since power dissipation is very high, corner "FF" is also not employed for the design. The corner "SF" is having large value of propagation delay as compared to "TT" with a less power dissipation as compared with "TT". The comparator propagation delay is a crucial factor in deciding the speed of operation, corner "SF" also is not utilized for the design. Corner "FS" is having a low propagation delay with medium value of power dissipation. Since the offset voltage of "FS" corner is very high as compared to other corners, it is also not selected for the design. The corner "TT" is the best suited for the application, since it is having a medium value of propagation delay with a low value of power dissipation.

3.12 Comparison with other works

Thus a high speed preamplifier based pseudo dynamic latch comparator used in high speed analog-to-digital converters is designed. The comparator is simulated by CADENCE spectre in 90 nm technology. Simulation results show that the comparator can work at a frequency of 8 GHz with an offset voltage of 11.5 mV and a propagation delay of 156 ps. The comparator dissipates a 128.8 µW from a 1.2 V supply. A comparison has been made with previous architectures and listed in Table 3.4.

Table 3.4 Comparison with previous architectures

Performance	[51]	[28]	[46]	[19]	This Work
Technology (nm)	90	90	90	180	90
Supply Voltage (V)	1.0	1.1	1.2	1.8	1.2
Offset Voltage (mV)	33.1	---	<11	-----	11.5
Input Sensitivity (mV)	63	2	<15	------	24.94
Power Dissipation (µW)	4300	---	240	460	128.8
Propagation Delay (ns)	---	---	----	1.699	.156
Maximum Clock Frequency (GHz)	4	0.2	6	0.1	8

3.13 Conclusion

This chapter describes the design and implementation of a high speed comparator for DS-UWB based flash analog-to-digital converter. The introduction about the comparator is discussed in the first section of the chapter. The comparator characteristics (both static and dynamic) are explained. The different types of comparators such as open loop comparators and regenerative comparators are also presented. We propose a high speed preamplifier based pseudo dynamic latch comparator used in flash analog-to-digital converters. An improved current source based on current mirror operation is used in the preamplifier circuit to reduce the noise coupling effect. In order to reduce the comparator overdrive recovery time, an extra pass transistor is added into the preamplifier circuit. An extra inverter is also added between preamplifier and the pseudo dynamic latch not only to reduce the kick back noise effect but also to improve the output load drivability. The proposed circuit is designed using 90 nm technology with a supply of 1.2 V. The comparator is having an offset voltage of 11.5 mV with a propagation delay of 156 ps. Layout of the proposed comparator is drawn and occupies an active area of 17.605 µm × 8.57 µm. Post layout simulation result shows that the comparator can work well with a clock frequency of 8 GHz having a power dissipation of 128.8 µW. The proposed comparator architecture is compared with other architectures. The maximum operating frequency of other architecture is 6 GHz. As a result, we conclude that the proposed comparator design is well suited for flash ADC which is used for DS-UWB applications. The outputs of the comparators in a flash ADC comes in a regular form which is called thermometer code, since there are 2^N-1 comparators are present in flash ADC. The thermometer code is converted to binary code for further processing. The next chapter deals with different types of thermometer to binary code conversion techniques used in flash ADCs.

CHAPTER 4

ENCODER DESIGN FOR FLASH ADC

4.1 Introduction

Flash ADC is one of the fastest methods to convert analog information into digital information. Flash ADCS are highly used in applications where large bandwidth is required such as radar processing, sampling oscilloscopes, data acquisition and satellite communication applications. Flash ADC comprises of three parts; resistor ladder, comparator and thermometer code to binary code converter. N bit flash ADC architecture requires 2^N-1 comparators for its operation [59]. The reference voltage is generated with the help of 2^N equally sized resistor which constitutes resistor ladder. Since the comparators are working in parallel, flash ADC completes its conversion in one cycle. The output of the comparators is coming in a specific manner which is called thermometer code [61]. The thermometer code is converted into binary code with the help of thermometer code to binary code conversion. The speed of the converter plays a crucial role in the design of flash ADC.

4.2 Different types of thermometer to binary code encoders

There are different ways with which the implementation of thermometer code to binary code conversion can be done. It includes ROM encoder, fat tree encoder, wallace tree encoder, multiplexer based encoder and logic style encoder [67]. Each of these encoders are explained with its advantages and disadvantages and finally proposes the most suitable encoder which is used for the application.

4.2.1 ROM encoder

A standard and uncomplicated method to encode the thermometer code to binary code is to utilize ROM encoder [63, 64]. The ROM based method is having two stages. In the initial stage, the thermometer code is translated in to 1 out of 2^N-1 code. This can be made by using array of NAND gates. The second stage is the ROM configuration which receives the 1 out of 2^N-1 code as input and chooses suitable row in the ROM and generates the binary outputs which is shown in Fig. 4.1 for a five bit flash ADC assuming that 1 out of 2^N-1 code is the input. Even though ROM encoder approach is simple and straight forward to design, it is slow and consumes large power due to a constant static current which is present in the ROM encoder. As the conversion speed increases, the probability of occurring bubble error is also

increases. In order to reduce the bubble error, extra circuitry is added to the encoder [83]. As the circuit complexity increases, propagation delay also increases. This reduces the maximum frequency of operation of the encoder [70]. The extra circuitry consumes more area in the chip which increases the power dissipation also. Since speed is a critical factor in our application, ROM encoder is not preferable for the current flash ADC design.

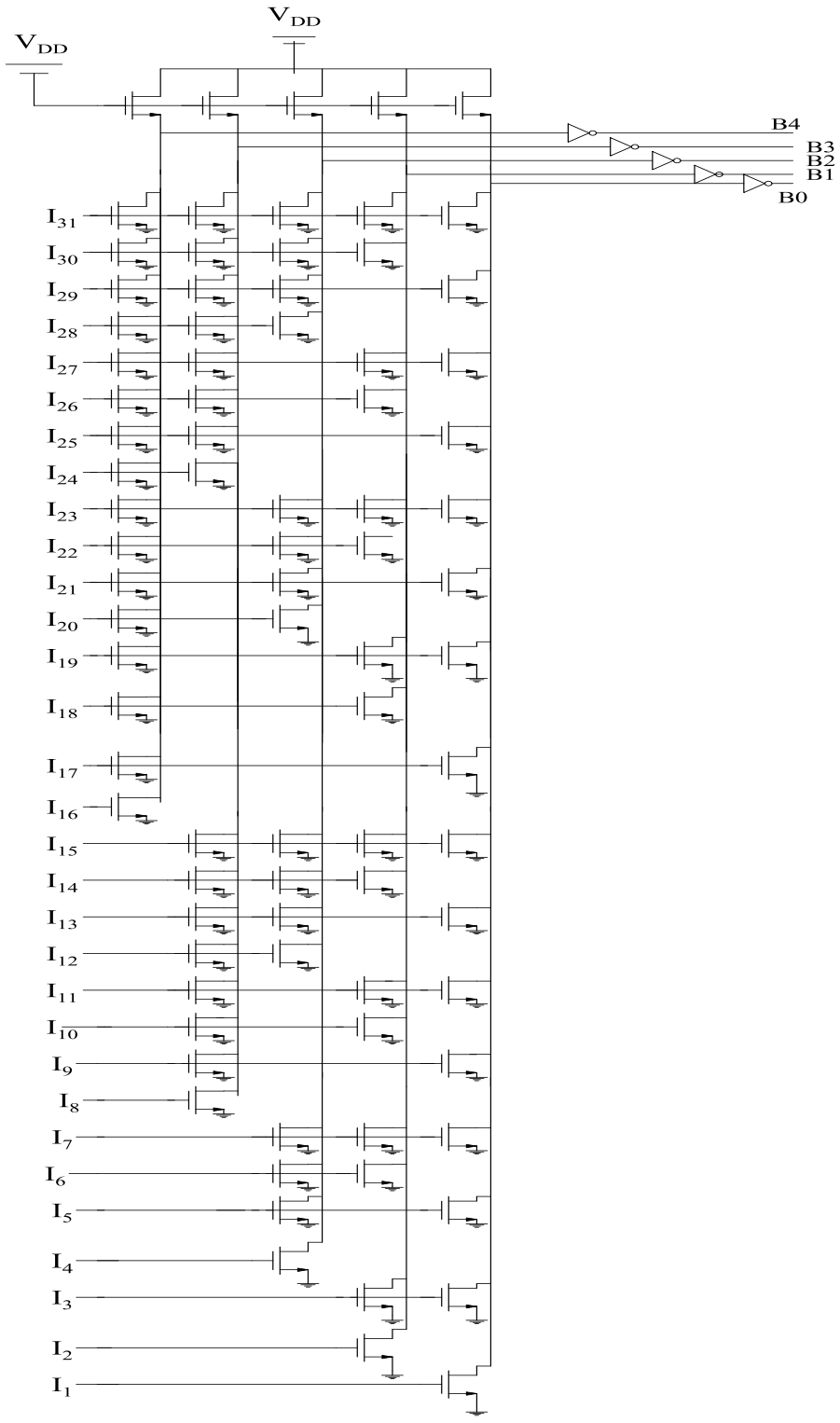


Fig. 4.1 ROM encoder

4.2.2 Fat tree encoder

The thermometer to binary encoding is accomplished in two stages in the fat tree encoder. The block diagram is shown in Fig. 4.2. The first stage translates the thermometer code to 1 out of N code which means there is only single logic high is present in the code. The second stage translates the 1 out of N code to binary code with the help of multiple trees of OR gates which is shown in Fig. 4.3, assuming that 1 out of N code is the input. The binary bits are generated using the equation (1) [82]. Fat tree encoder is having a high speed of operation with less power dissipation in comparison with ROM encoder [79]. Fat tree encoder doesn't require a clock signal or pull up resistors. Noise immunity of the fat tree encoder is higher than that of the ROM encoder. Static CMOS implementation method of fat tree encoder eliminates the static power dissipation. In this way of implementation, fat tree method consumes less power than ROM encoder. But the main disadvantage of the fat tree encoder is the complexity in the layout drawing. The tree structure of fat tree encoder is not as standard as ROM encoder. Even though speed of operation of fat tree encoder is greater than ROM encoder, speed of 5 GHz is not achievable by the fat tree encoder. As a result, fat tree encoder is also not taken into consideration for the current flash ADC design.

$$B_4 = e_0$$

$$B_3 = d_1 + d_0$$

$$B_2 = c_3 + c_2 + c_1 + c_0$$

$$B_1 = b_7 + b_6 + b_5 + b_4 + b_3 + b_2 + b_1 + b_0$$

$$B_0 = a_{15} + a_{14} + a_{13} + a_{12} + a_{11} + a_{10} + a_9 + a_8 + a_7 + a_6 + a_5 + a_4 + a_3 + a_2 + a_1 + a_0 \qquad (4.1)$$

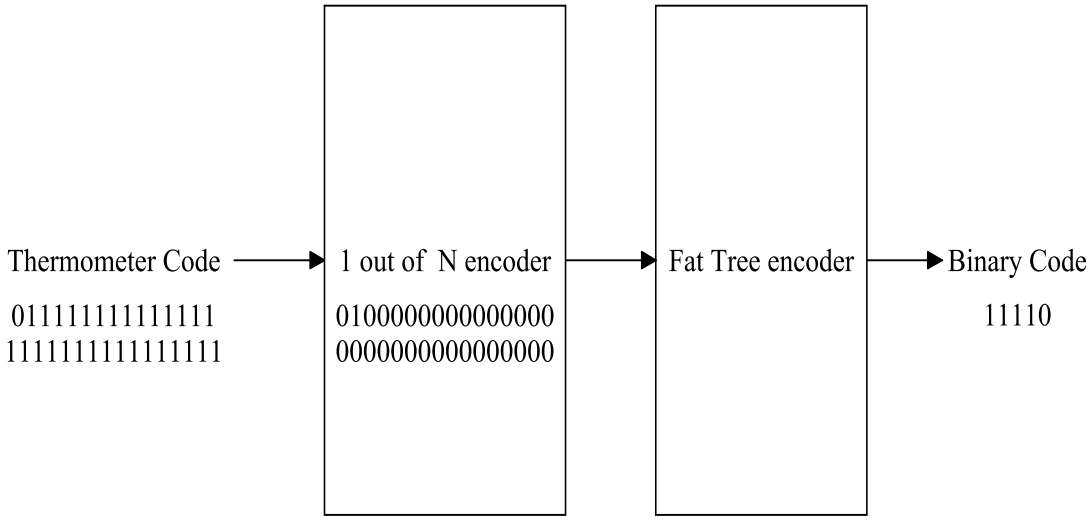
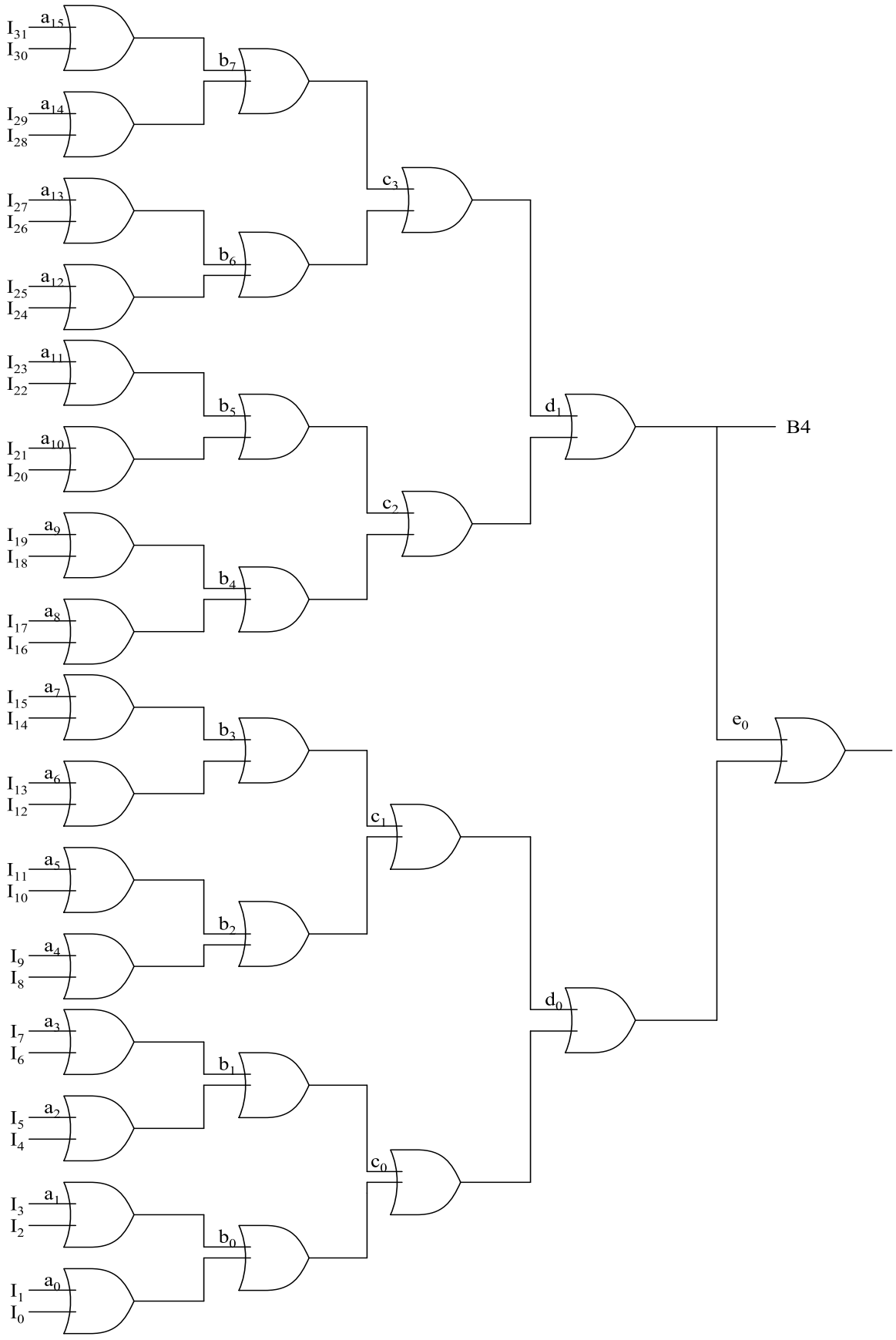
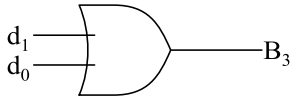


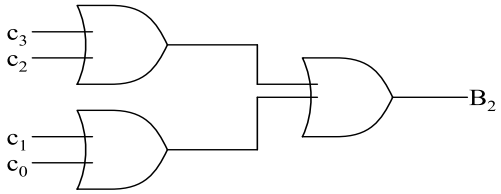
Fig. 4.2 Block diagram of fat tree encoder



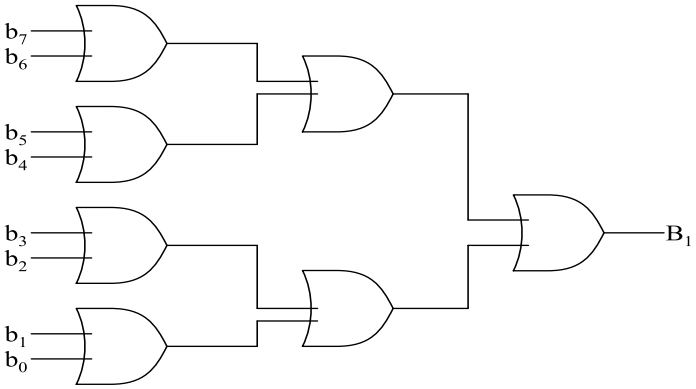
(a) Binary code B_4 (MSB) generation circuit



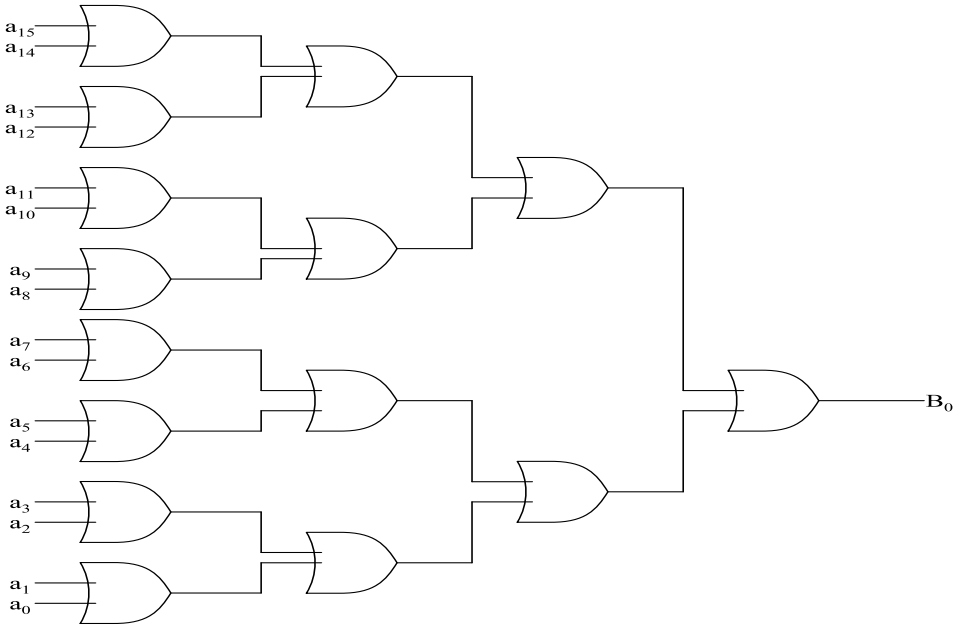
(b) Binary code B_3 generation circuit



(c) Binary code B_2 generation circuit



(d) Binary code B_1 generation circuit



(d) Binary code B_0 generation circuit

Fig. 4. 3 Binary code generation circuit using fat tree encoder

4.2.3 Wallace tree encoder

Wallace tree counts the number of one's available in the output of the comparators [68, 73]. The basic building block of the Wallace tree encoder is full adder cell. The total number of full adders utilized in an encoder of N bit is $2^N - N - 1$. The block diagram representation of five bit wallace tree encoder is shown in Fig. 4.4.

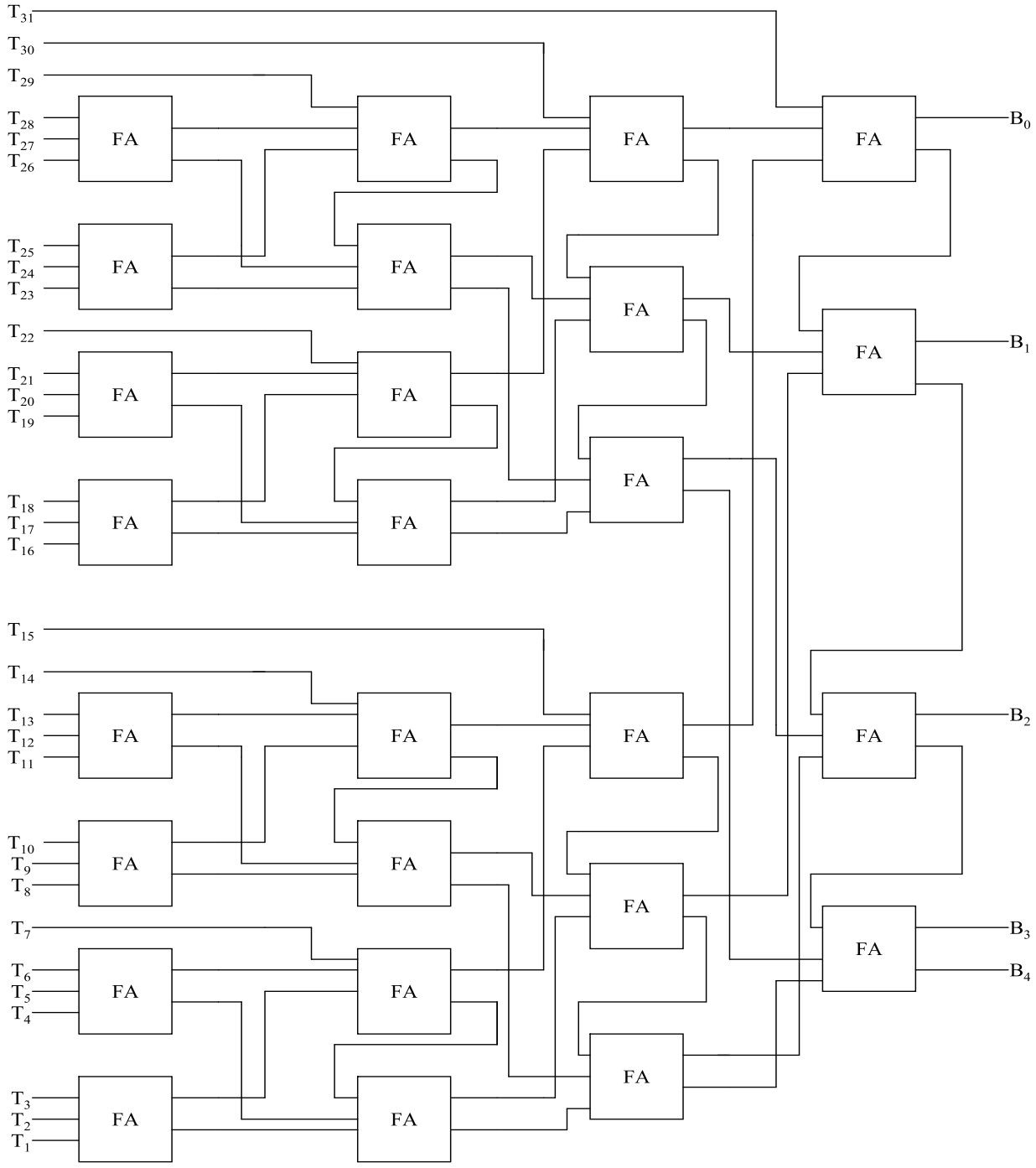


Fig. 4.4 Five bit Wallace tree encoder

At the first logical level, each cell adds up the number of logical one's at its entries and gives an output of two bit binary code. The second stage carries out the adding of two bit words of adjacent cells to give three bit binary outputs and so on with the intention of obtaining the final binary output code for the converter. Wallace tree encoder can correct higher order bubbles [74]. The wallace tree method is originally used to realize high speed multipliers in computer arithmetic units. It simply counts the number of one's present at its inputs and encodes those into binary format. This technique offers global bubble error correction/suppression [72] unlike the fat tree encoder and ROM encoder where bubble errors are usually handled locally using three or higher input NAND gates.

Wallace tree encoding technique is one of the simplest methods to implement thermometer code to binary code conversion [73]. One of the other main advantages of this encoder is that all the inputs in the Wallace tree encoder are traversing through equal number of full adders. So effectively the propagation delay of all the inputs is identical. By establishing pipelining in the encoder, speed of operation of the encoder can be increased. Since full adder cell plays a crucial role in the design of Wallace tree encoder, optimum design of full adder cell improves the performance of the Wallace tree encoder. As the resolution of ADC increases, the number of full adders used in this implementation also increases which in turn increases the die area as well as power dissipation of the total implementation. A modified Wallace tree encoder is proposed in the next part of the section.

4.2.4 Modified five bit Wallace tree encoder for low power application

The main challenges of designing ADC for system on chip applications are high speed, low voltage, and low power consumption. Reducing the power consumption is a major concern in any portable device. Low power techniques are applied to prolong the battery life of a system. Similarly ADCs also require low power technique in the design to reduce the total power consumption of ADC. Speed, power dissipation and resolution are the three crucial parameters of the design of any ADC which cannot be changed once the design is complete. In wireless and mobile communication applications require a high speed ADC with low resolution. The present analysis suggests a competent low power thermometer code to binary code converter anticipated for a 3 GS/s five bit flash analog-to-digital converter. The speed and power are the vital parameters in the design of thermometer to binary code converter. With the aim of medium speed and low power dissipation, the first stage of encoder is designed using dynamic logic. To make the code more resilient to bubble errors, the last stage

is designed in wallace tree fashion with the help of four full adders. With the use of CADENCE tool, the proposed encoder is designed using 90 nm technology with a power supply of 1.2 V.

A. Design of the proposed encoder

Error handling capability and power dissipation are two vital parameters in the design of thermometer to binary code conversion. Offset voltage in the comparator creates bubble error in the thermometer code. There are mainly two methods to minimize the effect of bubble errors. The first method is to convert the thermometer code to gray code (intermediate step) and then convert to binary code [71]. But the accuracy of the gray code decreases steadily as more number of bubble errors is present in the thermometer code. The second method is the use of wallace tree encoder for the implementation. This technique offers a high robustness to bubble error and stuck at fault error because of its inherent global bubble error correction/suppression capability. The disadvantage of this method is the large delay of the encoder. With the purpose of maintaining medium speed and low power dissipation with small amount of bubble error, the first stage of encoder is designed using dynamic logic and the last stage is designed by wallace tree encoder style [75]. In the first stage, conversion of thermometer code into two different four bit binary codes is done. With the help of four full adders and two different four bit binary codes, the final binary code is designed. The truth table which relates the thermometer code and binary code is presented in Table 4.1. The design equations are shown below in (4.2). The equations are imitative from the truth table.

$$b_3 = T_8$$

$$b_2 = T_4\overline{T_8} + T_{12}$$

$$b_1 = T_2\overline{T_4} + T_6\overline{T_8} + T_{10}\overline{T_{12}} + T_{14}$$

$$b_0 = T_1\overline{T_2} + T_3\overline{T_4} + T_5\overline{T_6} + T_7\overline{T_8} + T_9\overline{T_{10}} + T_{11}\overline{T_{12}} + T_{13}\overline{T_{14}} + T_{15}$$

$$a_3 = T_{24} \tag{4.2}$$

$$a_2 = T_{20}\overline{T_{24}} + T_{28}$$

$$a_1 = T_{16}\overline{T_{20}} + T_{22}\overline{T_{24}} + T_{26}\overline{T_{28}} + T_{30}$$

$$a_0 = T_{17}\overline{T_{18}} + T_{19}\overline{T_{20}} + T_{21}\overline{T_{22}} + T_{23}\overline{T_{24}} + T_{25}\overline{T_{26}} + T_{27}\overline{T_{28}} + T_{29}\overline{T_{30}} + T_{31}$$

Table 4.1 Five bit binary encoder truth table

B_4	B_3	B_2	B_1	B_0	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	0	00000000000000000000000000000011
0	0	0	1	1	00000000000000000000000000000111
0	0	1	0	0	00000000000000000000000000001111
0	0	1	0	1	00000000000000000000000000011111
0	0	1	1	0	00000000000000000000000000111111
0	0	1	1	1	00000000000000000000000001111111
0	1	0	0	0	00000000000000000000000011111111
0	1	0	0	1	00000000000000000000000111111111
0	1	0	1	0	00000000000000000000001111111111
0	1	0	1	1	00000000000000000000011111111111
0	1	1	0	0	00000000000000000000111111111111
0	1	1	0	1	00000000000000000001111111111111
0	1	1	1	0	00000000000000000011111111111111
0	1	1	1	1	00000000000000000111111111111111
1	0	0	0	0	00000000000000001111111111111111
1	0	0	0	1	00000000000000011111111111111111
1	0	0	1	0	00000000000000111111111111111111
1	0	0	1	1	00000000000001111111111111111111
1	0	1	0	0	00000000000011111111111111111111
1	0	1	0	1	00000000000111111111111111111111
1	0	1	1	0	00000000001111111111111111111111
1	0	1	1	1	00000000011111111111111111111111

1	1	0	0	0	00000001111111111111111111111111
1	1	0	0	1	00000011111111111111111111111111
1	1	0	1	0	00000111111111111111111111111111
1	1	0	1	1	00001111111111111111111111111111
1	1	1	0	0	00011111111111111111111111111111
1	1	1	0	1	00111111111111111111111111111111
1	1	1	1	0	01111111111111111111111111111111
1	1	1	1	1	11111111111111111111111111111111

The final stage of conversion is shown in Fig. 4.5.

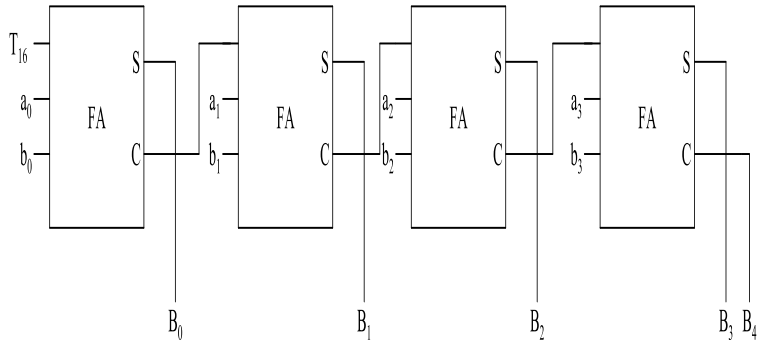


Fig .4.5 Final stage implementation using full adders

B. Implementation of the proposed encoder

There are various methods to implement the design equations for the conversion of thermometer code to binary code. Static CMOS, pseudo NMOS, dynamic logic are the variety of logic styles utilized for the implementation. Static CMOS implementation is having low power dissipation with very low speed and large number of transistors. Pseudo NMOS logic style consumes more power with a good speed of operation and less number of transistors. Dynamic logic style implementation operates with a medium speed with low power dissipation. With the intention of achieving low power with medium speed, the implementation is done using dynamic logic [66].

The basic structure of dynamic logic described in Fig. 4.6. The dynamic logic completes its operation in two phases. The first phase is called precharge and the second phase is evaluation. In the pre-charging phase (when CLK=0), the output node is charged to the supply voltage irrespective of any condition through PMOS pull-up transistor. During this time, the pull down path is disconnected from the supply voltage because of the presence of NMOS transistor whose gate is connected to clock input. In the evaluation phase (CLK=1), the pull-up path is switched off and pull down path is discharged conditionally based on the inputs. As a result the static power dissipation is avoided in the implementation, since pull-up as well as pull down path is not switching on simultaneously. The important thing in the design of dynamic logic is that during the evaluation phase, the input to the gate has to make at most one transition. The schematic implementation of the first stage is shown in Fig. 4.7. The implementation is shown only for b_3, b_2, b_1 and b_0. Similarly a_3, a_2, a_1 and a_0 are designed. The output of the first stage is connected to an array of four full adders which are connected in a sequential manner. The full adder cell is designed using dynamic logic. The schematic implementation is shown in Fig. 4.8. This reduces the overall speed of operation with minimization of bubble errors. Wallace tree encoder adds up the number of one's present at the inputs and encodes it into binary format. This style of implementation provides global bubble error correction/suppression without any extra circuitry. The full adder is also implemented using dynamic logic style. The equivalent (W/L) ratio of pull down transistor is half of the single pull up transistor whose gate is connected to clock. The minimum (W/L) ratio in the design is taken as (120/100) and correspondingly other (W/L) ratios are taken.

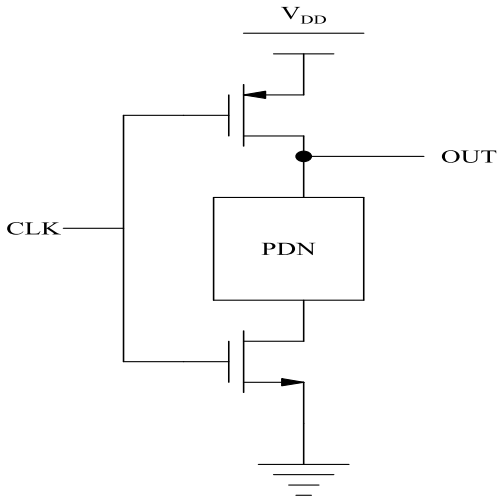
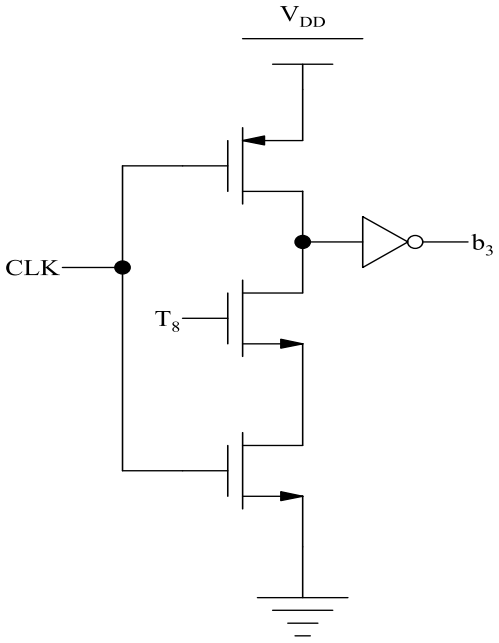
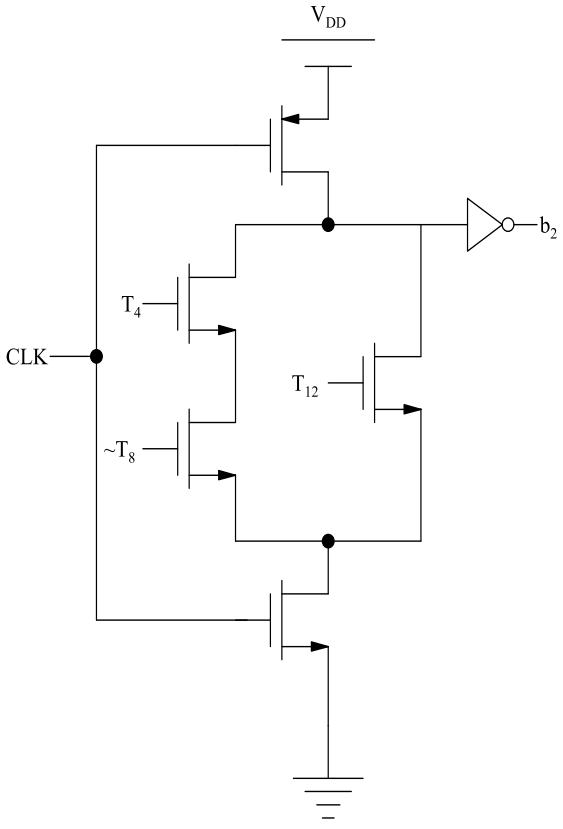


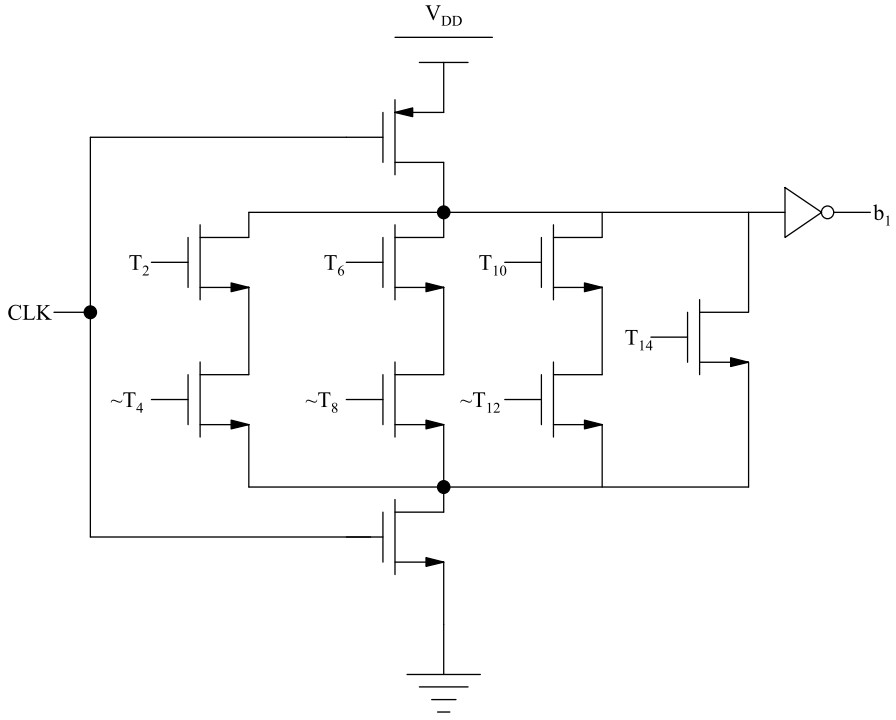
Fig. 4.6 Basic structure of dynamic logic



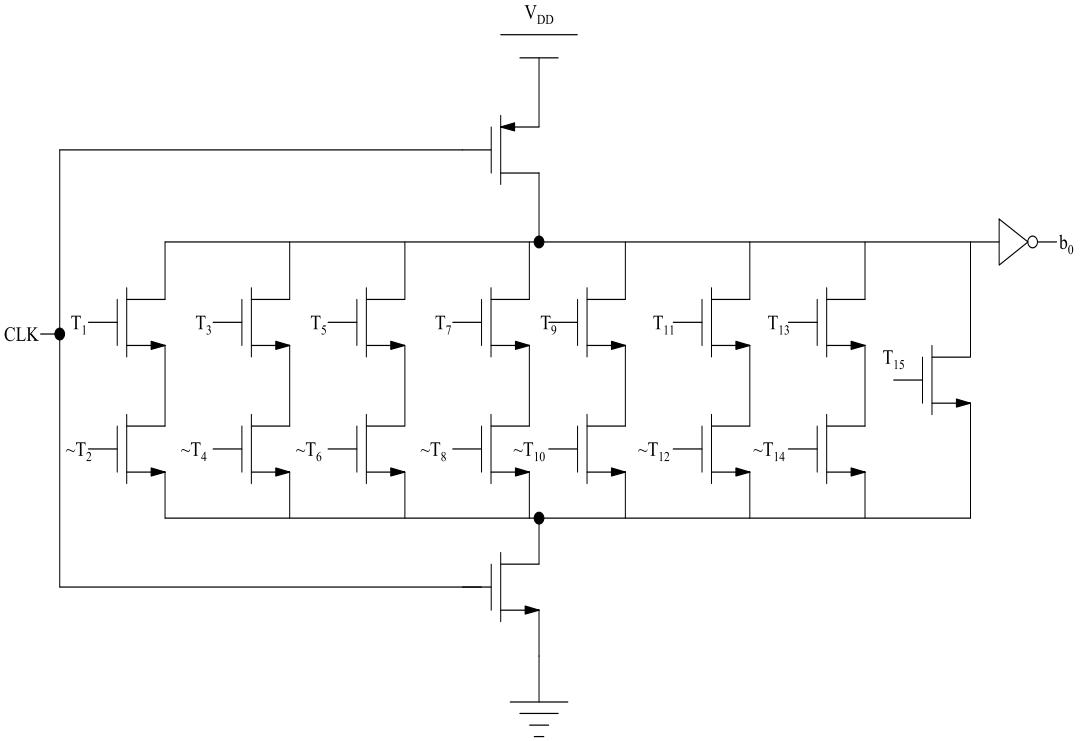
(a) Schematic implementation of b_3 using dynamic logic



(b) Schematic Implementation of b_2 using dynamic Logic

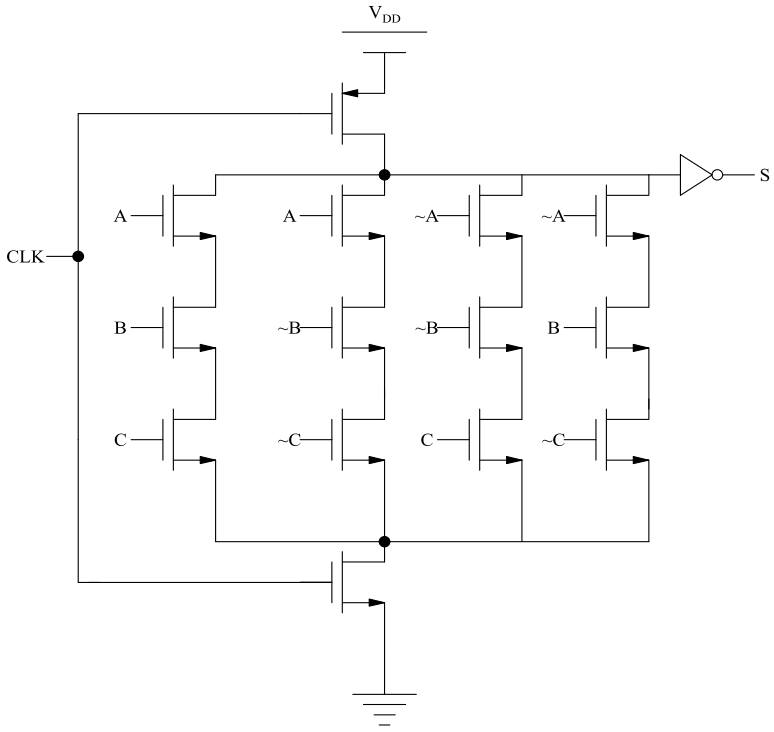


(c) Schematic implementation of b_1 using dynamic logic

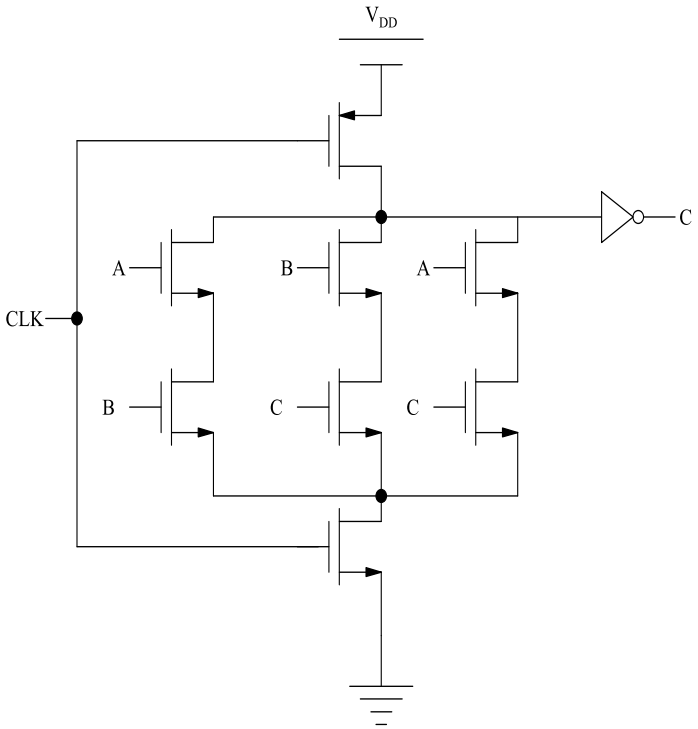


(d) Schematic implementation of b_0 using dynamic logic

Fig. 4.7 Schematic implementation of b_3, b_2, b_1 and b_0 using dynamic logic



(a) Schematic implementation of sum in a full adder using dynamic logic



(b) Schematic implementation of carry in a full adder using dynamic logic

Fig. 4.8 Schematic implementations of sum and carry in a full adder using dynamic logic

C. Reconfigurable property of the proposed encoder [77]

There are two methods to design the proposed encoder to work as a four bit binary encoder. The first method is by making a_3, a_2, a_1, a_0 and T_{16} as zeroes. The output is five bit with MSB as zero. The carry output of the full adder is always zero which propagates to the next stage. Consequently the final output is same as b_3, b_2, b_1, b_0. This method is the most desirable one because all the inputs of the encoder are connected to some specific value. The second method is to take the output from b_3, b_2, b_1 and b_0 and neglect all other inputs. The disadvantage of this method is many inputs of the encoder are left unconnected. Subsequently any noise signal can be easily coupled to the unconnected inputs that propagate to the output and make the output erroneous.

D. Simulation results and discussion

The proposed encoder is designed and tested for all input permutations from the truth table. Result is verified with the help of the truth table. The simulation result is shown in Fig. 4.9. It shows that the encoder can be operated at frequency of 3 GS/s with a power dissipation of 2.424 mW. The proposed encoder is compared with other types of encoders. The comparison table (Table 4.2) shows that the proposed encoder is having medium speed of operation with low power dissipation. The reconfigurable capability of the proposed encoder makes this encoder design adaptable to reconfigurable flash ADC architecture.

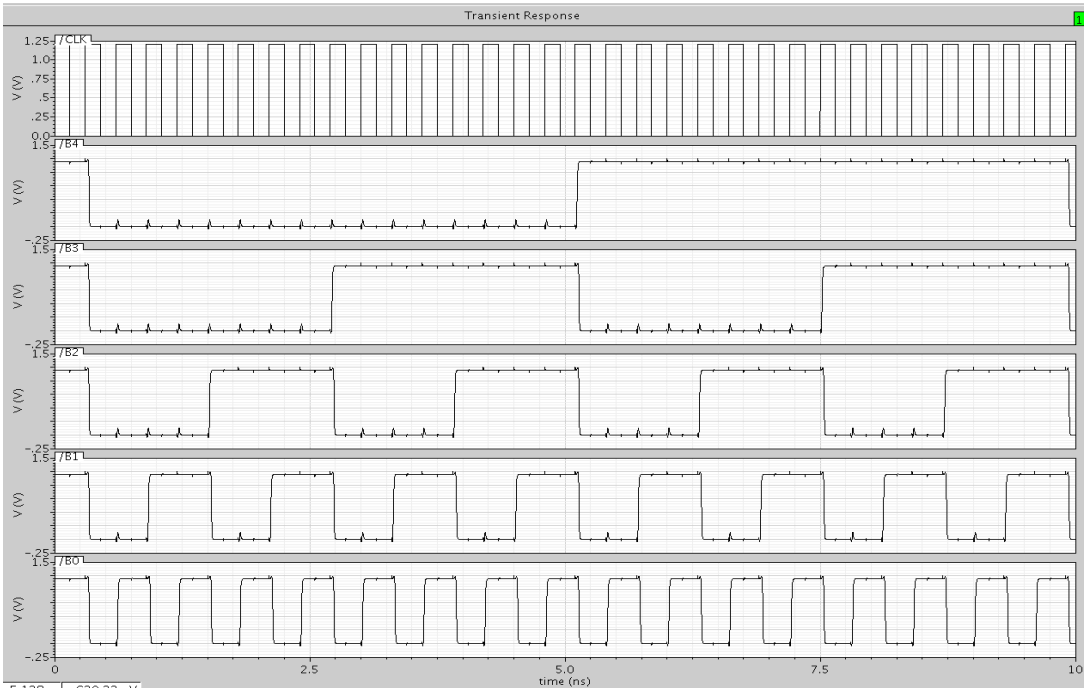


Fig. 4.9 Proposed encoder simulation

Table 4.2 Summary and comparison with other encoders

Results	Current Mode Logic Encoder [60]	[71]	Proposed Encoder
Architecture	Flash	Flash	Flash
Resolution	4 bits	4 bits	5 bits
Technology	180 nm	180 nm	90 nm
Sampling Frequency	5 GHz	2.5 GHz	3 GHz
V_{DD}	1.8 V	1.8 V	1.2 V
Current	2.22 mA	3.055 mA	2.02 mA
Power Dissipation	4 mW	5.5 mW	2.424 mW

4.2.5 Multiplexer based encoder

Multiplexer based encoder needs a smaller amount of hardware and has a smaller critical path than Wallace tree encoder. The regular structure of multiplexer based encoder helps in drawing the layout easily [68, 69]. If half of the outputs in the thermometer code are logic high indicates that most significant bit (MSB) of the binary output is logic high. So MSB is the value of the thermometer output at level of 2^{N-1}. In order to find out the value of second most significant bit, the original thermometer code is separated into two partial thermometer codes spaced by 2^{N-1}. The encoding is done with the help of 2:1 multiplexers. The control input of the multiplexer is the previously encoded binary output. The second most significant bit is calculated with the use of two partial thermometer codes and 2:1 multiplexers. This process is sustained continuously until one 2:1 multiplexer persists. The output of the last 2:1 multiplexer is the least significant bit. The regular structure of the multiplexer based encoder allows the extension to a system of higher resolution. A five bit multiplexer based encoder is shown in Fig. 4.10 which is made by 2:1 multiplexers. The next section of the chapter presents a modified low power multiplexer based encoder for five bit flash ADCs.

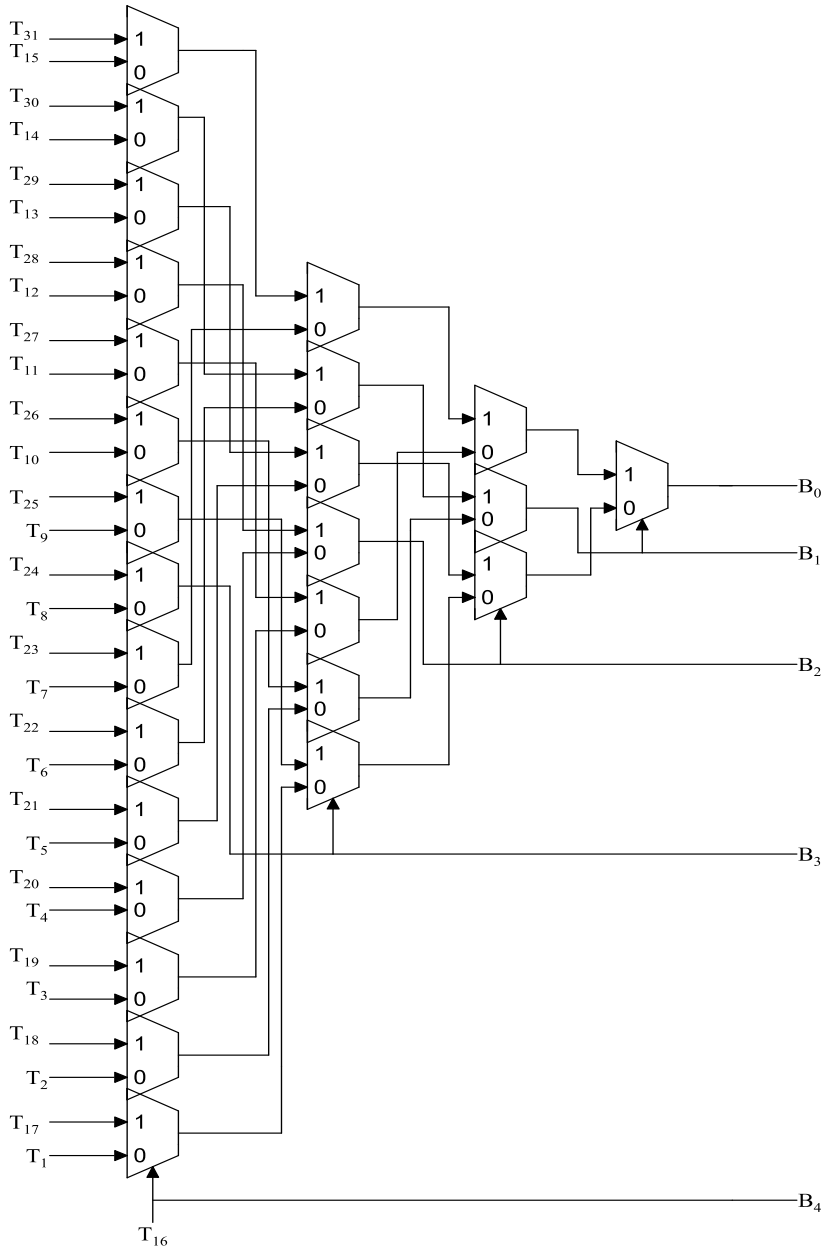


Fig. 4.10 Regular multiplexer based encoder

4.2.6 Modified low power multiplexer based encoder for five bit flash ADCs

The choice of an encoder determines the flash ADC parameters such as latency and robustness to noise. The proposed encoder utilizes a new multiplexer based architecture for the implementation of thermometer to binary code conversion. The present analysis put forward a proficient low power thermometer code to binary code converter anticipated for a 4.44 GS/s five bit flash analog-to-digital converter. The speed and power are the important parameters in the design of thermometer to binary code converter. With the object of modest speed and low power dissipation, a new multiplexer based encoder is proposed. In order to implement with low power and modest speed, the implementation of multiplexer is done

using dynamic logic. Since all the multiplexers are working in parallel, the critical path delay in the implementation reduces. With the use of CADENCE tool, the proposed encoder is designed using 90 nm technology with a power supply of 1.2 V.

A. Design of the proposed encoder

Conversion of thermometer code to binary code with high speed and low power dissipation is a decisive parameter which makes a decision of the overall power dissipation and speed of flash ADC. The proposed encoder is designed using multiplexers and or gates. Since all multiplexers are working in parallel, the critical path delay in the circuit reduces. Critical path in the proposed encoder circuit consists of one multiplexer and an eight inputs or gate. The truth table which provides the relationship between the thermometer code and binary code is indicated in Table 4.1. The design equations are shown below. The equations are obtained from the truth table.

$$B_4 = T_{16}$$

$$B_3 = T_8\overline{T_{16}} + T_{24} \tag{4.3}$$

$$B_2 = T_4\overline{T_8} + T_{12}\overline{T_{16}} + T_{20}\overline{T_{24}} + T_{28}$$

$$B_1 = T_2\overline{T_4} + T_6\overline{T_8} + T_{10}\overline{T_{12}} + T_{14}\overline{T_{16}} + T_{18}\overline{T_{20}} + T_{22}\overline{T_{24}} + T_{26}\overline{T_{28}} + T_{30}$$

$$B_0 = T_1\overline{T_2} + T_3\overline{T_4} + T_5\overline{T_6} + T_7\overline{T_8} + T_9\overline{T_{10}} + T_{11}\overline{T_{12}} + T_{13}\overline{T_{14}} + T_{15}\overline{T_{16}} + T_{17}\overline{T_{18}} + T_{19}\overline{T_{20}} + T_{21}\overline{T_{22}} + T_{23}\overline{T_{24}} + T_{25}\overline{T_{26}} + T_{27}\overline{T_{28}} + T_{29}\overline{T_{30}} + T_{31}$$

The equation can be rewritten as like this in order to make use of multiplexer in the design.

$$B_4 = T_{16}$$

$$B_3 = T_8\overline{T_{16}} + T_{16}T_{24}$$

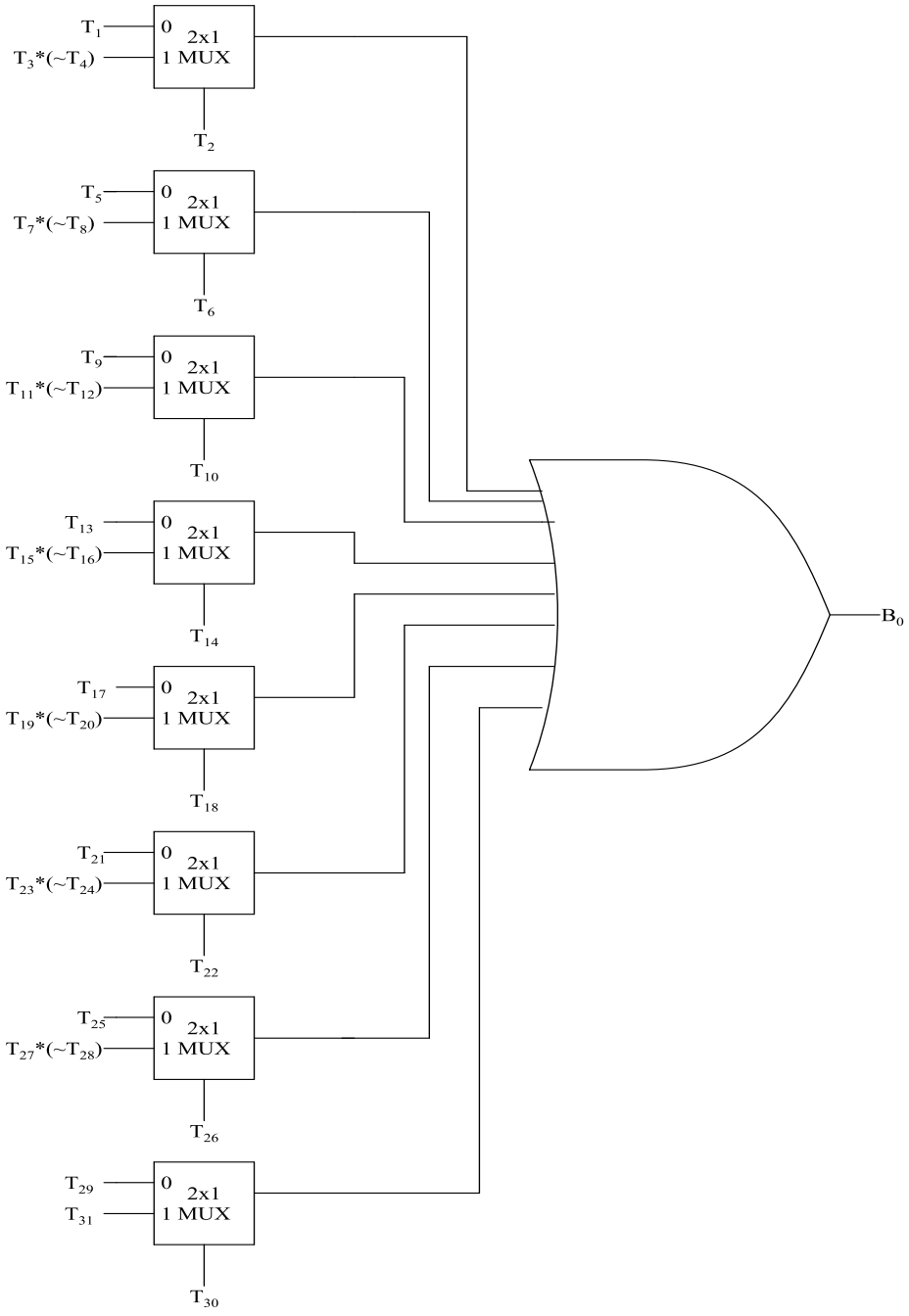
$$B_2 = T_4\overline{T_8} + T_8(T_{12}\overline{T_{16}}) + T_{20}\overline{T_{24}} + T_{24}T_{28} \tag{4.4}$$

$$B_1 = T_2\overline{T_4} + T_4(T_6\overline{T_8}) + T_{10}\overline{T_{12}} + T_{12}(T_{14}\overline{T_{16}}) + T_{18}\overline{T_{20}} + T_{20}(T_{22}\overline{T_{24}}) + T_{26}\overline{T_{28}} + T_{28}T_{30}$$

$$B_0 = T_1\overline{T_2} + T_2(T_3\overline{T_4}) + T_5\overline{T_6} + T_6(T_7\overline{T_8}) + T_9\overline{T_{10}} + T_{10}(T_{11}\overline{T_{12}}) + T_{13}\overline{T_{14}} + T_{14}(T_{15}\overline{T_{16}}) + T_{17}\overline{T_{18}} + T_{18}(T_{19}\overline{T_{20}}) + T_{21}\overline{T_{22}} + T_{22}(T_{23}\overline{T_{24}}) + T_{25}\overline{T_{26}} + T_{26}(T_{27}\overline{T_{28}}) + T_{29}\overline{T_{30}} + T_{30}T_{31}$$

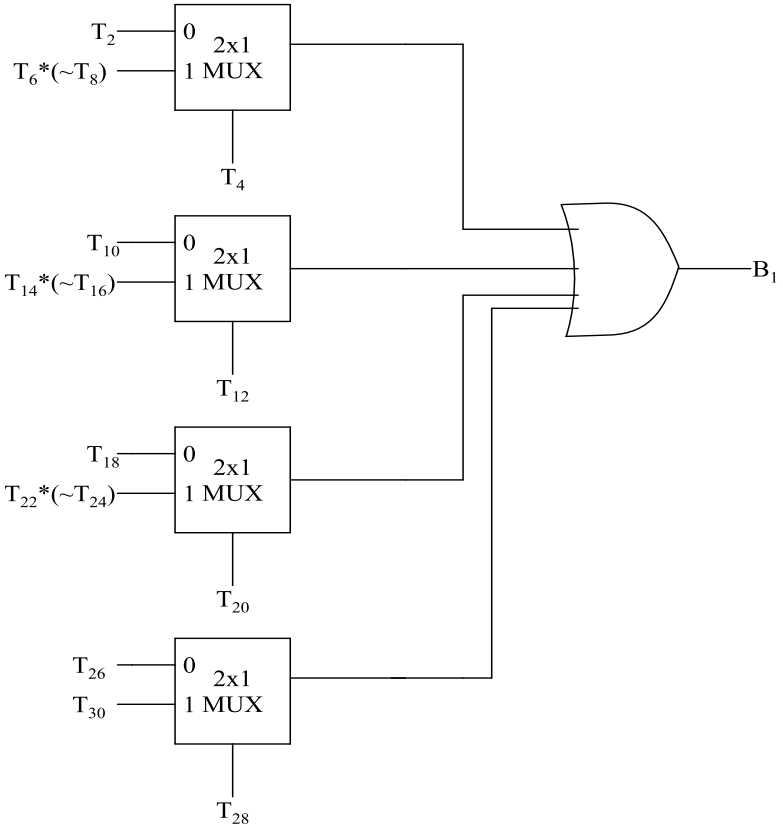
B. Implementation of the proposed encoder

The implementation is done using multiplexers and or gates. General multiplexer based encoder requires 26 multiplexers for the five bit binary code conversion. The proposed encoder requires 15 multiplexers, one two inputs or gate, four inputs or gate and an eight inputs or gate. Accordingly the number of multiplexers used in the implementation is drastically reduced. The schematic implementation of the encoder is shown in Fig. 4.11.

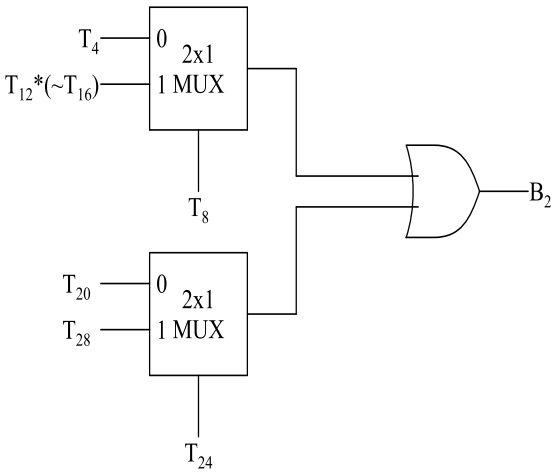


(a) Schematic implementation of B_0

Critical path delay in the general encoder is decided by the delay of four multiplexers in the critical path. The critical path delay in the proposed encoder is considerably reduced because there is only one multiplexer and an eight inputs or gate in the critical path. Therefore the maximum frequency of operation which can be obtained with the help of proposed encoder increases.

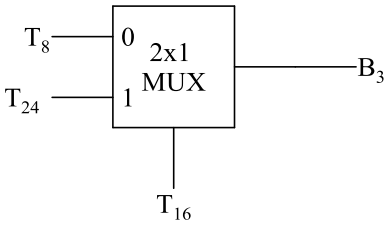


(b) Schematic implementation of B_1

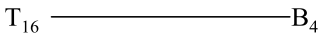


(c) Schematic implementation of B_2

With the purpose of achieving modest speed with low power dissipation, the implementation of the multiplexer is done using dynamic logic [66] (Fig. 4.12). The equivalent (W/L) ratio of pull down transistor is half of the single pull up transistor whose gate is connected to clock. The minimum (W/L) ratio in the design is taken as (120/100) and correspondingly other (W/L) ratios are taken.



(d) Schematic implementation of B_3



(e) Schematic implementation of B_4

Fig. 4.11 Schematic implementations of B_4, B_3, B_2, B_1, B_0

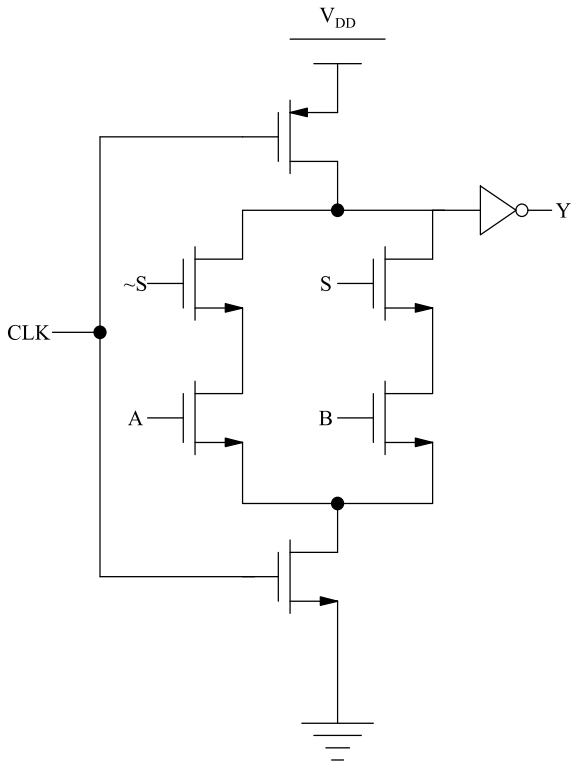


Fig. 4.12 Schematic implementation of multiplexer using dynamic logic

C. Simulation results and discussion

The proposed encoder is designed and examined for all the combinations of the input from the truth table. Result is validated with the assist of the truth table. The simulation result is shown in Fig. 4.13. The result shows that maximum frequency of operation that can be achieved with the help of proposed encoder is 4.44 GHz with a power dissipation of 1.624 mW. Other types of encoders are compared with the proposed encoder. The comparison table is provided in Table 4.3. Comparison results shows that proposed encoder is having the modest speed of operation with low power dissipation. By the help of CADENCE tool, the proposed encoder is designed and simulated using 90 nm technology with a supply voltage of 1.2 V. The combination of having low power consumption, low transistor count and shorter critical path makes the proposed multiplexer based encoder suitable for efficient flash ADC design.

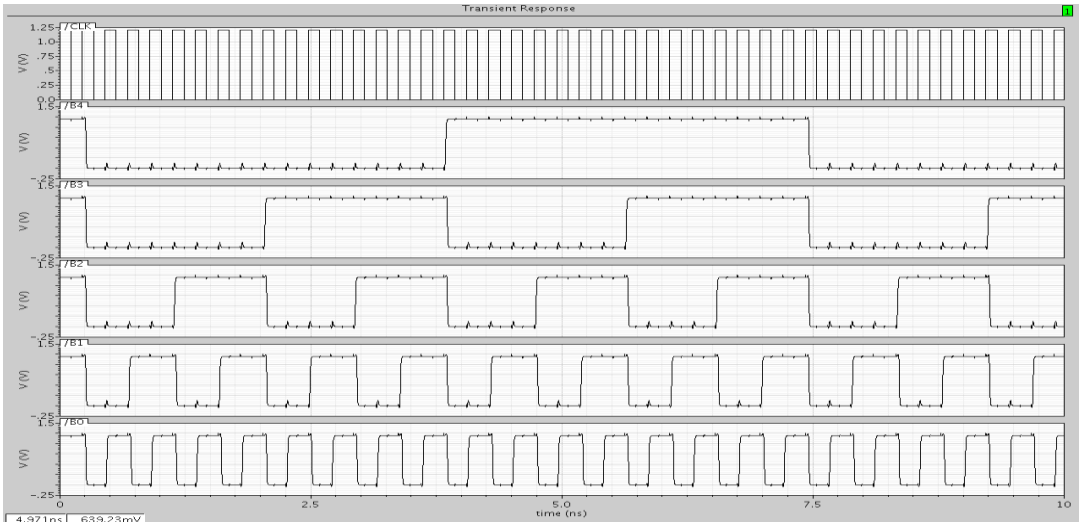


Fig. 4.13 Proposed encoder Simulation

Table 4.3 Comparison with other encoders

Results	Current Mode Logic Encoder [60]	[71]	Proposed Encoder
Architecture	Flash	Flash	Flash
Resolution	4 bits	4 bits	5 bits
Technology	180 nm	180 nm	90 nm
Sampling Frequency	5 GHz	2.5 GHz	4.44 GHz
V_{DD}	1.8 V	1.8 V	1.2 V
Current	2.22 mA	3.055 mA	1.353 mA
Power Dissipation	4 mW	5.5 mW	1.624 mW

4.2.7 High speed reconfigurable encoder for five bit flash ADCs

The present analysis suggests a competent high speed thermometer code to binary code converter anticipated for a 5 GS/s five bit flash analog-to-digital converter. With the intention of high speed, the first stage of encoder is designed using dynamic logic [66]. To enhance the speed of operation, the last stage is designed using multiplexer based implementation. With the use of CADENCE tool, the proposed encoder is designed using 90 nm technology with a power supply of 1.2 V.

A. Design and implementation of the proposed encoder

In the first stage, conversion of thermometer code into two different four bit binary codes is done. With the help of four multiplexers and two different four bit binary codes, the final binary code is designed. Since four multiplexers are working in parallel, the final binary output is obtained in a faster manner. The truth table which narrates the relation between thermometer code and binary code is presented in Table 1. The design equations are shown in (2). The equations are derived from the truth table. With the aim of achieving high speed, the implementation is done using dynamic logic. The schematic implementation of the first stage is shown in Fig. 4.7. The implementation is shown only for b_3, b_2, b_1 and b_0. Similarly a_3, a_2, a_1 and a_0 are designed. The output of the first stage is connected to four multiplexers. Since the output of the four multiplexers is produced at the same time, speed of operation becomes very fast. The multiplexer is designed using dynamic logic in order to increase the speed. The schematic implementation is shown in Fig. 12. The equivalent (W/L) ratio of pull down transistor is half of the single pull up transistor whose gate is connected to clock. The minimum (W/L) ratio in the design is taken as (120/100) and correspondingly other (W/L) ratios are taken.The final stage of conversion is shown in Fig. 4.14.

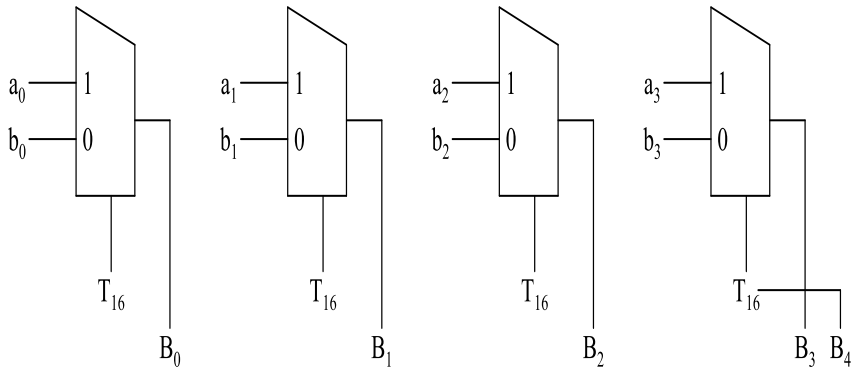


Fig. 4.14 Final stage implementation using multiplexers

B. Reconfigurable property of the proposed encoder [77]

Reconfigurable property means the ability of the system to reconfigure its arrangements to the different situations. The proposed five bit encoder is having the reconfigurable property; that is it can be able to work as a four bit thermometer to binary encoder. This can be done by forcing a_3, a_2, a_1, a_0 and T_{16} as zeroes. Since MSB of the encoder is T_{16}, the output of the encoder contains five bits with MSB as zero. In this method, the reconfigurable property is achieved in the proposed encoder. The switching activity is reduced by a large percentage with this method which reduces the dynamic power consumption in the encoder. Consequently the proposed encoder results in lower power consumption, when it is operated in a lower resolution mode (five to four).

C. Simulation results and discussion

The proposed encoder is designed and tested for all the combinations of input from the truth table. Result is verified with the help of the truth table. The simulation result is shown in Fig. 4.15. It shows that the encoder can be operated at frequency of 5 GS/s with a power dissipation of 2.132 mW. The proposed encoder is compared with other types of encoders. The comparison table (Table 4.4) shows that the proposed encoder is having high speed of operation with low power dissipation. The reconfigurable capability of the proposed encoder makes this encoder design adaptable to reconfigurable flash ADC architecture.

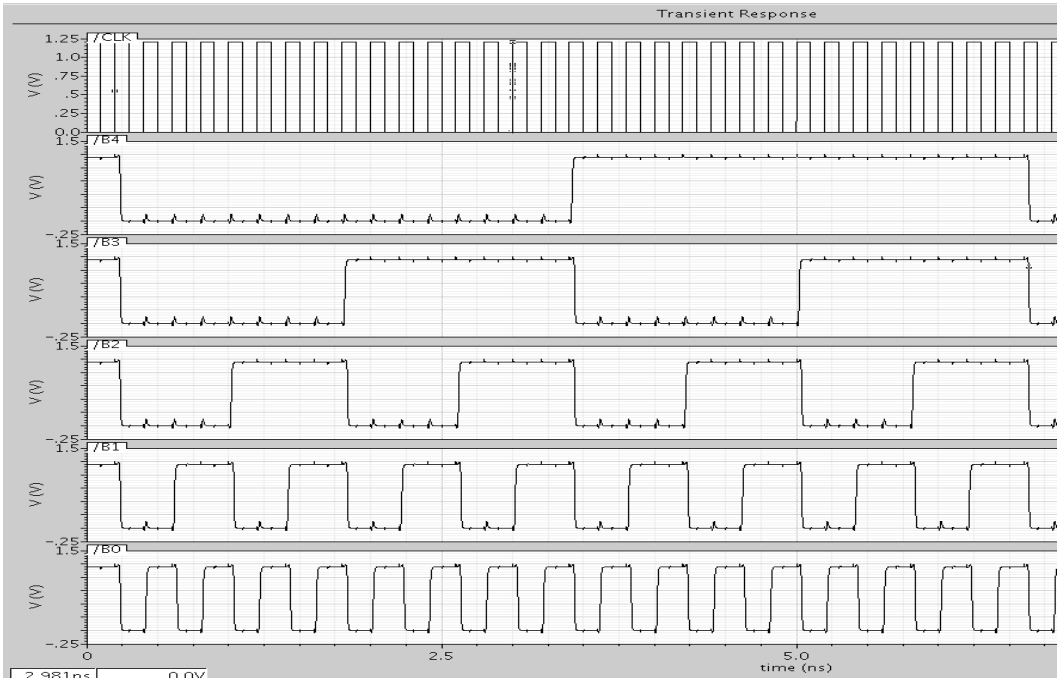


Fig. 4.15 Proposed encoder simulation

Table 4.4 Summary and comparison with other encoders

Results	Current Mode Logic Encoder [60]	[71]	Proposed Encoder
Architecture	Flash	Flash	Flash
Resolution	4 bits	4 bits	5 bits
Technology	180 nm	180 nm	90 nm
Sampling Frequency	5 GHz	2.5 GHz	5 GHz
V_{DD}	1.8 V	1.8 V	1.2 V
Current	2.22 mA	3.055 mA	1.777 mA
Power Dissipation	4 mW	5.5 mW	2.132 mW

4.2.8 High speed low power reconfigurable encoder for five bit flash ADCs

This discussion suggests an improved multiplexer based encoder used for 5 GS/s five bit flash ADC. The design of a thermometer code to binary code encoder plays a crucial role in the design of flash ADC. An encoder in this discussion converts thermometer code to binary code with the help of 18 multiplexers and two 7:3 encoders which is more efficient when compared with the existing multiplexer based encoder that uses 26 multiplexers for the conversion.

To increase the speed of operation, implementation is done using pseudo dynamic CMOS logic. The proposed encoder is designed, simulated and verified using 90 nm technology at 1.2 V power supply using CADENCE tool.

A. Design and implementation of the proposed encoder

In this design, a five bit thermo meter code to binary code conversion can be achieved with the help of 18 multiplexers and two 7:3 encoders (Fig. 4.16). The design equations (4.5) of the 7:3 encoders can be derived from the truth table (Table 4.5).

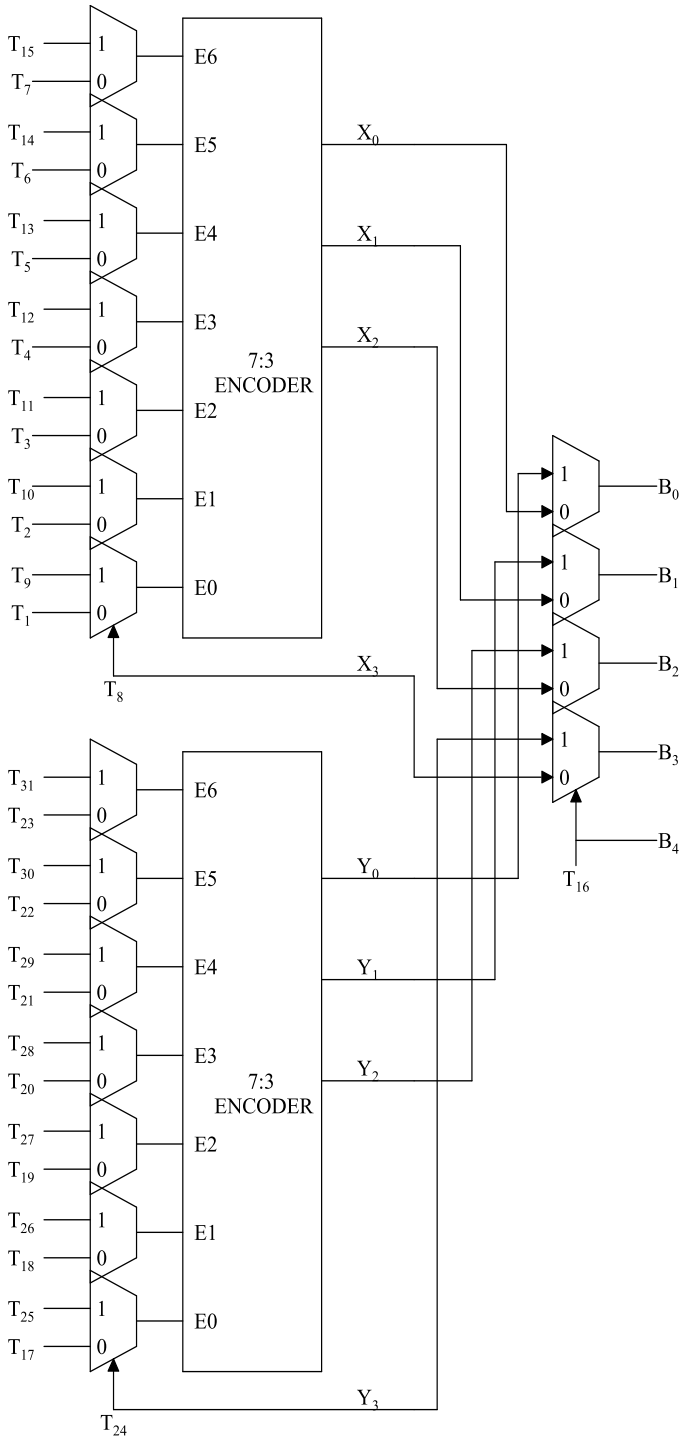


Fig .4.16 Proposed multiplexer based encoder

$X_2 = E_3$

$$X_1 = E_1\overline{E_2} + E_2\overline{E_3} + E_5 + E_6 \tag{4.5}$$

$$X_0 = E_0\overline{E_1} + E_2\overline{E_3} + E_4\overline{E_5} + E_6$$

Table 4.5 Truth table of 7:3 encoder

E_6	E_5	E_4	E_3	E_2	E_1	E_0	$X_2X_1X_0$
0	0	0	0	0	0	0	000
0	0	0	0	0	0	1	001
0	0	0	0	0	1	1	010
0	0	0	0	1	1	1	011
0	0	0	1	1	1	0	100
0	0	1	1	1	1	1	101
0	1	1	1	1	1	1	110
1	1	1	1	1	1	1	111

The operation of the encoder can be explained with an example. Let the thermometer code be 00000000000000011111111111111111 (T_{17} to T_{31} are zeroes and remaining bits are ones). According to encoder operation, X_0, X_1, X_2 and X_3 of the first 7:3 encoder results in logic high value and Y_0, Y_1, Y_2 and Y_3 of the second 7:3 encoder gives logic low value. The output of the 7:3 encoders is given to multiplexer with a select line of T_{16}. Since T_{16} is logic high, it selects Y_0, Y_1, Y_2 and Y_3 and the output is 10000.

In order to achieve high speed of operation, the implementations are done using pseudo dynamic CMOS logic. Pseudo dynamic CMOS logic circuit comprises of a PMOS transistor with gate connected to clock, a group of NMOS transistors for the realization of the logic style in the pull down network and an inverter [65]. The NMOS evaluation transistor which is present in the dynamic logic is not available in the pseudo dynamic logic.

During the pre-charging phase of the dynamic CMOS, the PMOS transistor is on and the NMOS network is switched off and in the evaluation mode the PMOS transistor is switched off and NMOS network is conditionally switched on based on the inputs. Whereas in pseudo

dynamic CMOS logic, the NMOS evaluation block can be enabled during pre-charging phase, since it has no influence on the output voltage due to the presence of inverter. The basic structure of the pseudo dynamic CMOS logic (two input and gate) is shown in Fig. 4.17. During pre-charging phase, if NMOS logic block is enabled, the output comes to settle down to a value decided by a resistive divider of the PMOS pull up and NMOS logic block. It must be ensured that the voltage at the inverter input does not below V_{IH} (Minimum input voltage applied at the input which is taken as a logic one). The size of PMOS and NMOS transistors must be chosen in such a way that the proper functioning of the circuit is maintained. Consider the case with NMOS logic is enabled and clock is low. With proper size of the transistor, the voltage at the input of the inverter is less than $V_{IH,}$ thus maintaining logic at the output of the inverter. If the PMOS transistor size is increased beyond a specific limit, the intermediate voltage exceeds V_{IH} thereby pulling down the inverter output. Finally it results in the malfunctioning of the circuit. Therefore the sizing of transistor is crucial in the implementation design.

The presence of static power dissipation is the one of the disadvantage of the pseudo dynamic CMOS logic [66]. (The power dissipation occurs when a direct current flows between V_{DD} and ground. That is when both pull up and pull own networks are switched on simultaneously). In pseudo NMOS logic, the pull up path is always on. But in the case of pseudo dynamic CMOS logic, static power dissipation is present only when CLK=0. The implementations of each encoder bits using pseudo dynamic CMOS logic are shown in Fig. 4.18 and multiplexer implementation is shown in Fig. 4.19.

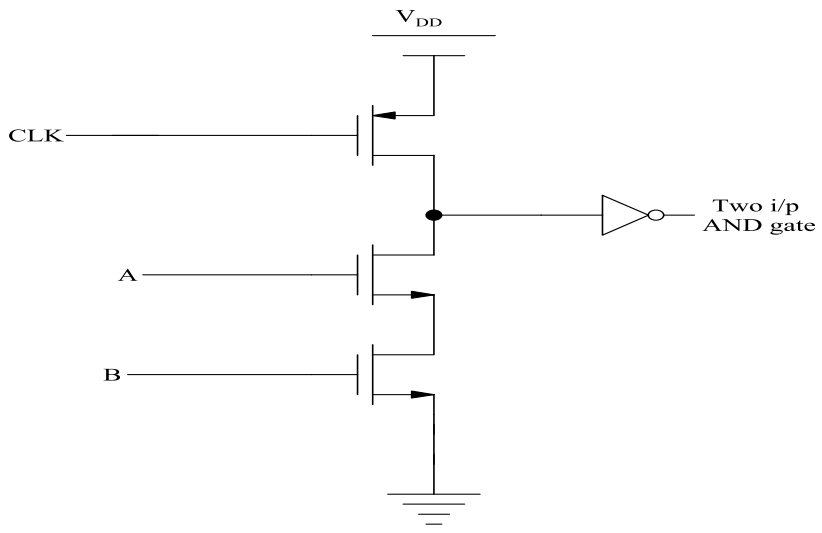
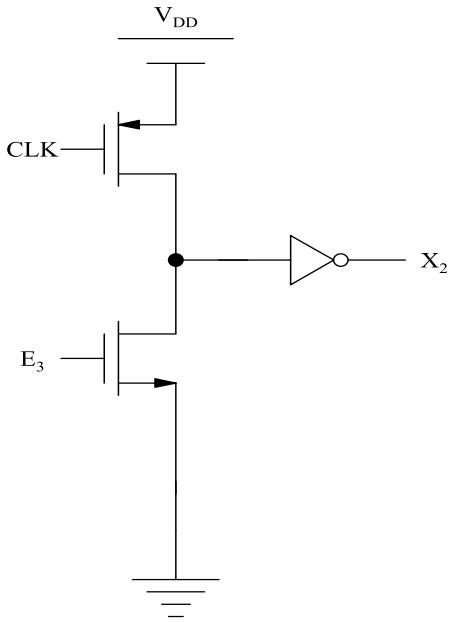
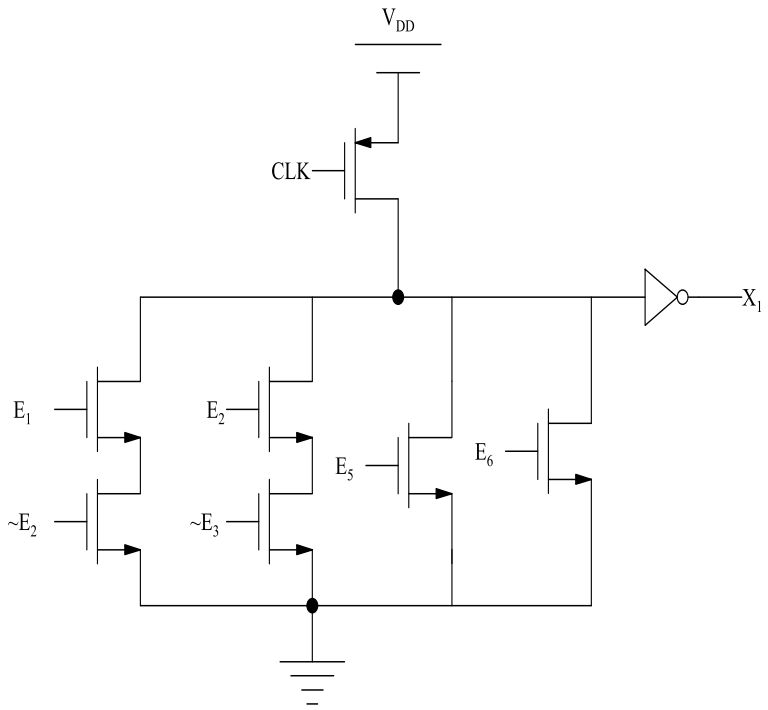


Fig. 4.17 Schematic of two input AND gate using pseudo dynamic CMOS logic

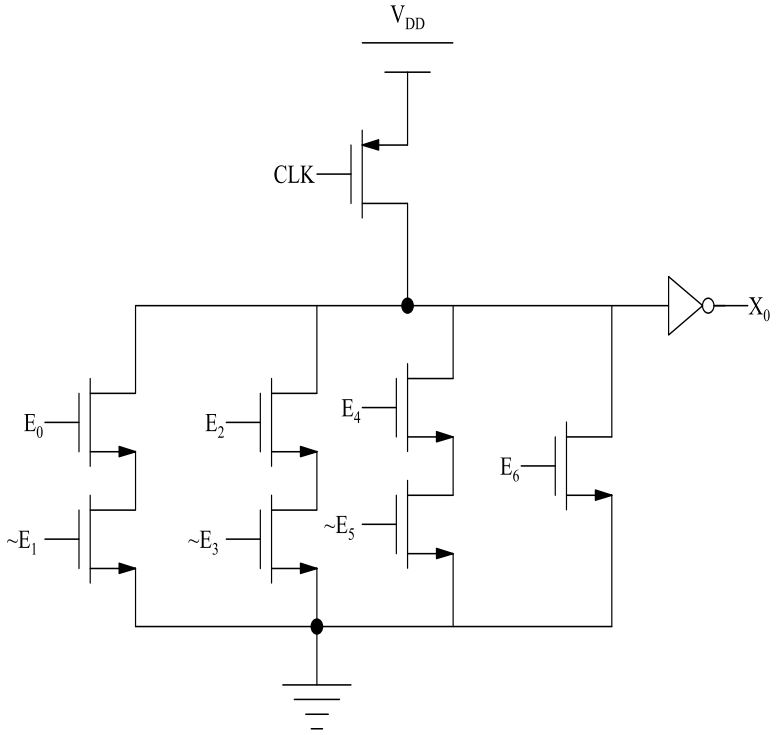


(a) Schematic implementation of X_2 using pseudo dynamic CMOS logic



(b) Schematic implementation of X_1 using pseudo dynamic CMOS logic

The equivalent (W/L) ratio of pull down transistor is half of the single pull up transistor whose gate is connected to clock. The minimum (W/L) ratio in the design is taken as (120/100) and likewise other (W/L) ratios are taken.



(c) Schematic implementation of X_0 using pseudo dynamic CMOS logic

Fig. 4.18 Schematic implementations of X_2, X_1 and X_0 using pseudo dynamic CMOS logic

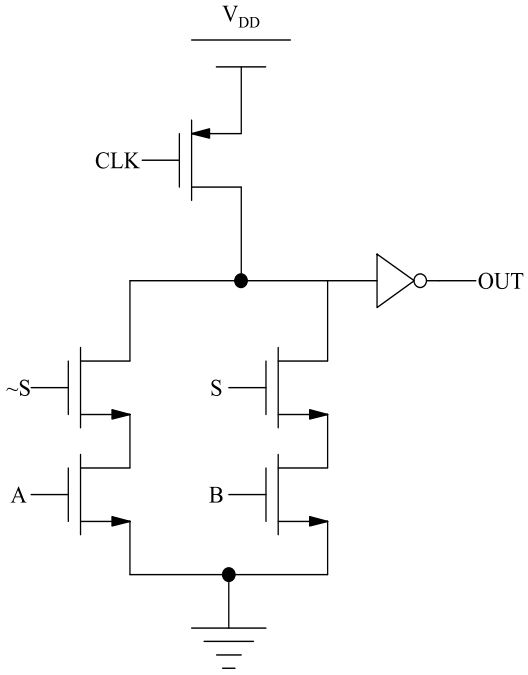


Fig. 4.19 Multiplexer implementation using pseudo dynamic CMOS logic

B. Properties of the implementation

i. Bubble error correction [84]

The dynamic noise due to clock skew (delay) and aperture jitter becomes much more serious with the increasing sampling rate and input frequency. In addition to dynamic noises, device mismatch is another main error source due to process variation. These error sources can be referred to as an input offset voltage, which can greatly distort the performance of the encoder. When the input-referred offset voltage is larger than 0.5 LSB, there may be a logical "1" above a logical *"0"* in the thermometer code at the output of parallel comparators. This is called a "bubble". As the resolution and speed of operation of the ADC increase, the possibility of adding more bubble errors into the thermometer code is very high. The bubble error correction circuit can be added to the proposed encoder circuit to improve the accuracy. The double error correction circuit used in the proposed encoder is shown in Fig. 4.20.

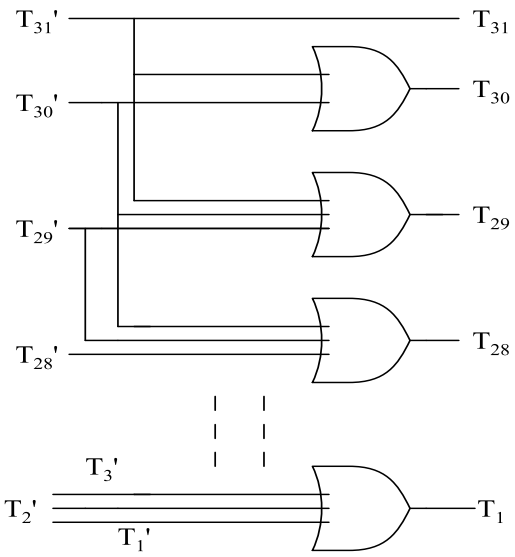


Fig. 4.20 Bubble error correction circuit

ii. Critical path delay [60]

In the existing multiplexer based encoder, the critical path delay is decided by four multiplexers in the critical path. But in the case of the proposed encoder, critical path delay is decided by two multiplexers and one 7:3 encoder which are present in the critical path. The critical path delay in the proposed implementation is less as compared to the existing multiplexer based encoder. The critical path delay is measured to be 0.2 ns. As a result, the maximum frequency of operation that can be achieved with the help of proposed encoder is 5 GHz.

iii. Self Reconfigurable Property [77, 78]

Self reconfigurable property is particularly useful in adaptive resolution analog-to-digital converters. The proposed encoder can be reconfigured to operate on thermometer code with reduced operand length without any extra overhead and is suitable for adaptive resolution ADC designs. The encoder can be configured to operate as four bit thermometer code to binary code by making the MSB bits T_{17} to T_{31} as logic zeroes. Effectively switching activity is greatly reduced as compared with existing multiplexer based encoder. The switching activity is directly related to dynamic power, which forms a major component of the total power dissipation. Accordingly the proposed encoder results in low power consumption when operated for thermometer code with smaller length. The proposed encoder can be configured as two separate four bit encoder also. This can be achieved by first making T_{16} as zero, disconnect T_{17} to T_{31} and connect T_1 to T_{15} with inputs and take the output as $B_3B_2B_1B_0$. Secondly connect T_{17} to T_{31} with inputs, disconnect T_1 to T_{15} and finally make T_{16} as one and take the result as $B_3B_2B_1B_0$. Therefore, the proposed five bit encoder can be configured as a single or double four bit encoder without adding any extra circuitry. As a result, the self reconfigurable property is achieved correctly.

C. Simulation results and comparison

The encoder is designed by combining all the five bits outputs, tested and demonstrated using all the input combinations from the truth table using 90 nm technology with a 1.2 V supply. The simulation result is shown in Fig. 4.21.

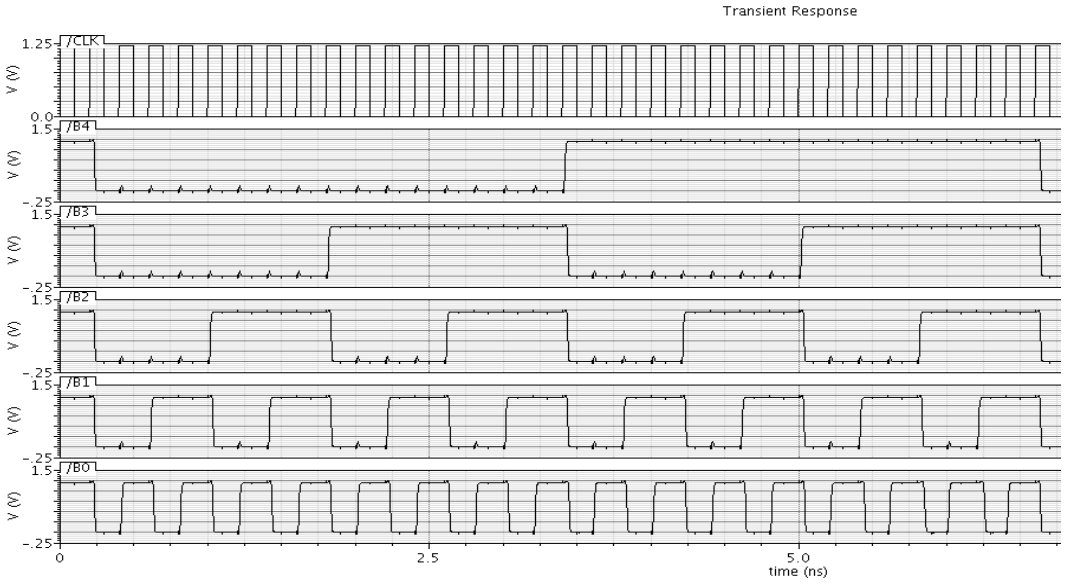


Fig. 4.21 Proposed encoder simulation

The maximum frequency of operation achieved using proposed method for five bit output is 5 GHz with a power dissipation of 1.969 mW from 1.2 V. As the resolution increases, the maximum frequency of operation decreases. The encoder can be reconfigured to operate on thermometer code with reduced length without any extra overhead which is suitable for adaptive resolution analog-to-digital converters. Simulation results indicate that the proposed encoder results in improved performance when compared to the existing encoders in terms of delay. The summary of the encoder simulation results and comparison with the existing encoder are presented in the Table 4.6.

Table 4.6 Comparison with other encoders

Results	Existing Multiplexer based encoder (gray code) [78]	[71]	Proposed Encoder
Architecture	Flash	Flash	Flash
Resolution	5 bits	4 bits	5 bits
Technology	90 nm	180 nm	90 nm
Sampling Frequency	----	2.5 GHz	5 GHz
V_{DD}	1.2 V	1.8 V	1.2 V
Critical path includes	4 Multiplexer	------	2 Multiplexer + one 7:3 encoder
Critical path delay	---	------	0.2 ns
Power Dissipation	69 µW	5.5 mW	1.969 mW

4.2.9 Performance Comparison of five bit Thermometer code to Binary code Conversion using Different Logic Styles

The present investigation compares different logic style implementations of five bit thermometer code to binary code conversion. Static CMOS, Dynamic, Pseudo NMOS and Pseudo Dynamic CMOS [66] are the different logic styles used to implement the conversion. In this discussion, direct conversion method is used without any intermediate stage. Instead of direct conversion method, usage of any other methods (thermometer code to gray code and then gray code to binary code) increases the latency which reduces the overall speed of

operation. All the encoders are designed using 90 nm technology with 1.2 V power supply using CADENCE tool. This contribution compares the different logic style implementations of five bit thermometer code to binary code in terms of power dissipation, maximum operating frequency and power delay product.

A. Design of the proposed Encoder

Conversion of the thermometer code to binary code is one of the essential parts in high speed flash ADC design. There are different methods with which the implementation can be done. To achieve high speed of operation, direct implementation method is used for conversion. In all the circuit implementations, width of the PMOS transistor is taken twice than that of the NMOS transistor in order to equalize the delay. The truth table which represents the correlation between thermometer code and binary code is presented in Table 4.1. The design equations which are developed from the truth table are shown below.

$$
\begin{aligned}
B_4 &= T_{16} \\
B_3 &= T_8\overline{T_{16}} + T_{24} \\
B_2 &= T_4\overline{T_8} + T_{12}\overline{T_{16}} + T_{20}\overline{T_{24}} + T_{28} \\
B_1 &= T_2\overline{T_4} + T_6\overline{T_8} + T_{10}\overline{T_{12}} + T_{14}\overline{T_{16}} + T_{18}\overline{T_{20}} + T_{22}\overline{T_{24}} + T_{26}\overline{T_{28}} + T_{30} \\
B_0 &= T_1\overline{T_2} + T_3\overline{T_4} + T_5\overline{T_6} + T_7\overline{T_8} + T_9\overline{T_{10}} + T_{11}\overline{T_{12}} + T_{13}\overline{T_{14}} + T_{15}\overline{T_{16}} + T_{17}\overline{T_{18}} + T_{19}\overline{T_{20}} + T_{21}\overline{T_{22}} \\
&+ T_{23}\overline{T_{24}} + T_{25}\overline{T_{26}} + T_{27}\overline{T_{28}} + T_{29}\overline{T_{30}} + T_{31}
\end{aligned}
\tag{4.6}
$$

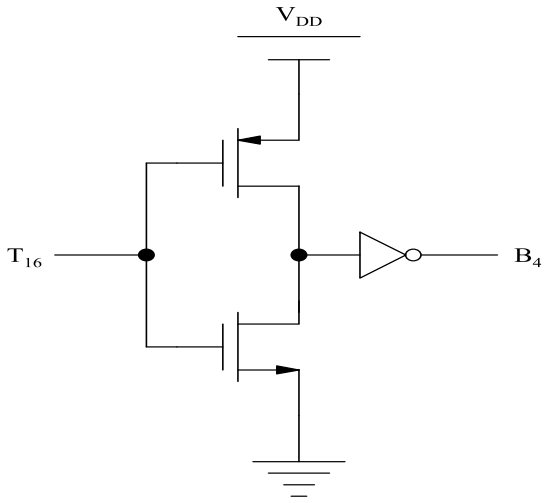
B. Implementation of the encoder using different logic styles

i. Static CMOS [66]

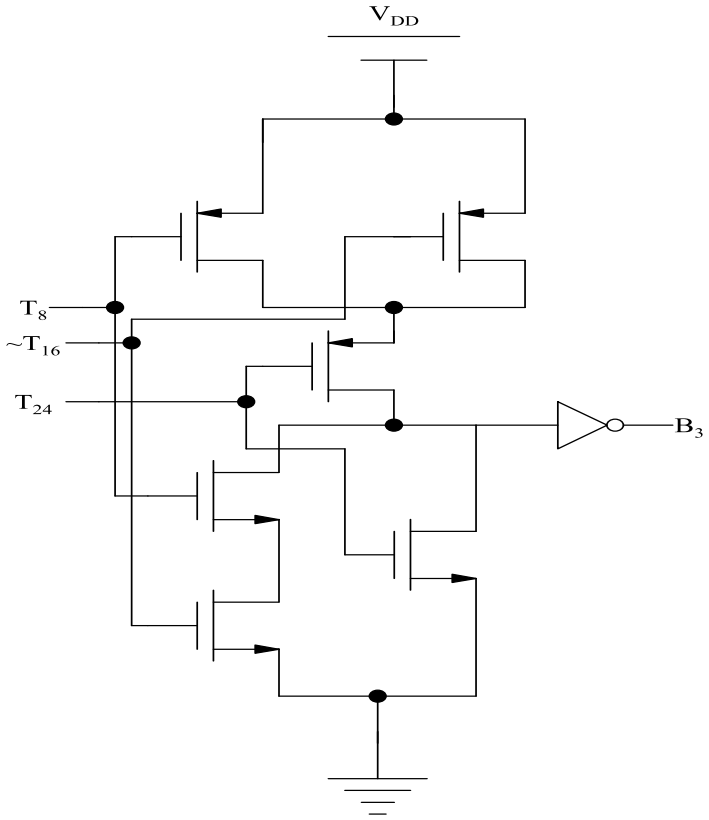
The primary advantages of this implementation are low sensitivity towards noise and low power dissipation. Since there is no static power dissipation, during every switching operation, the output is connected either to V_{DD} or to ground through a low resistance path. For small circuit implementations, static CMOS implementation is considered as the best preferred choice.

As the equation to be implemented is large, the number of transistors used for implementation is very large. This occupies large area in the die. For an N input logic gate, the implementation requires 2N transistors. This limits the speed of operation. Sixteen PMOS transistors in the pull up path and two NMOS transistors in the pull down path effectively

determine the critical path delay. The critical path delay in this implementation is measured to be 1 ns. The schematic implementation of different bits is shown in Fig. 4.22.



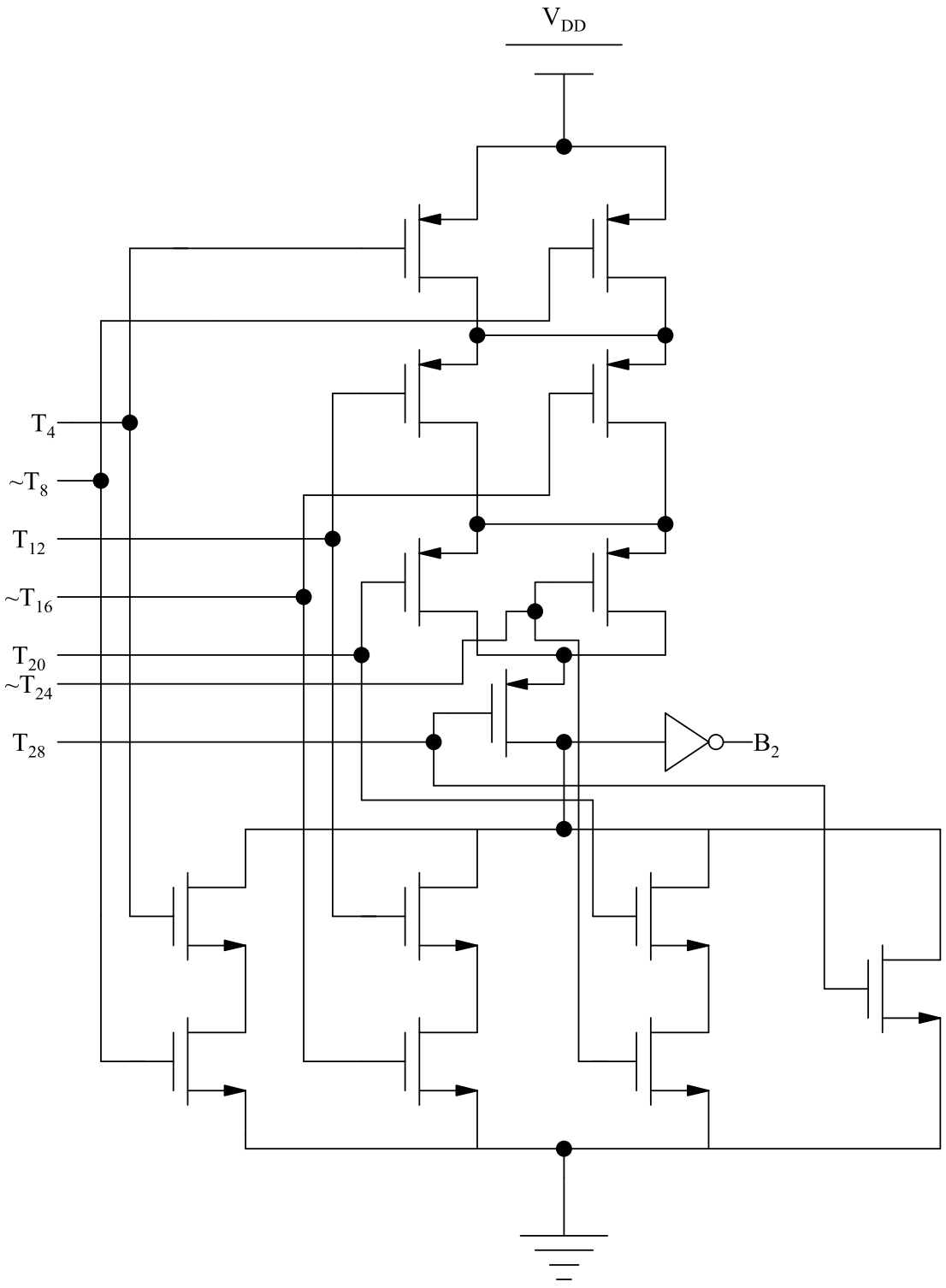
(a) Binary code B_4 generation circuit



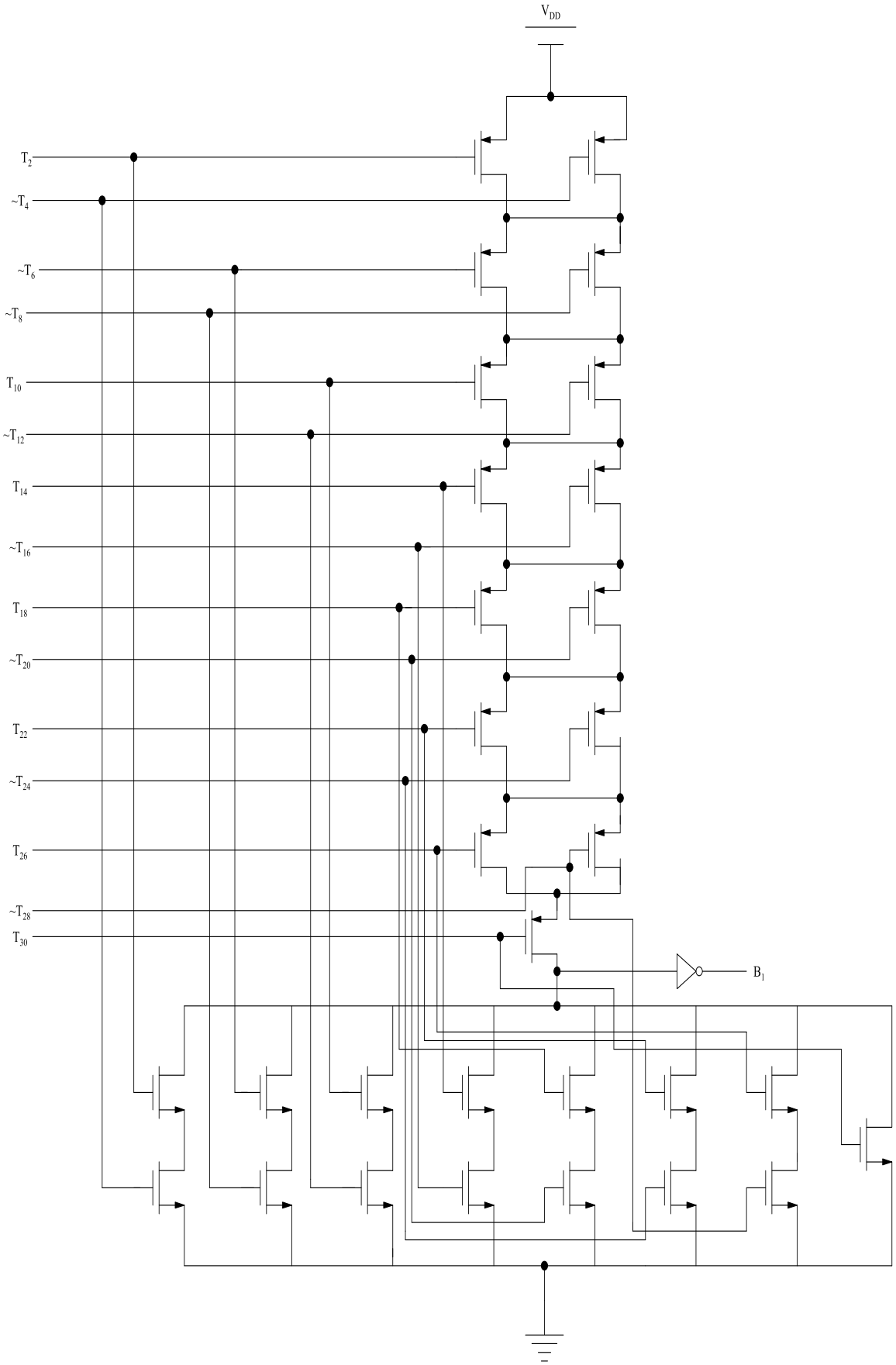
(b) Binary code B_3 generation circuit

The simulation result shows that maximum sampling frequency achieved with static CMOS implementation (Fig. 4.23) CMOS implementation is 1 GHz with a power dissipation of

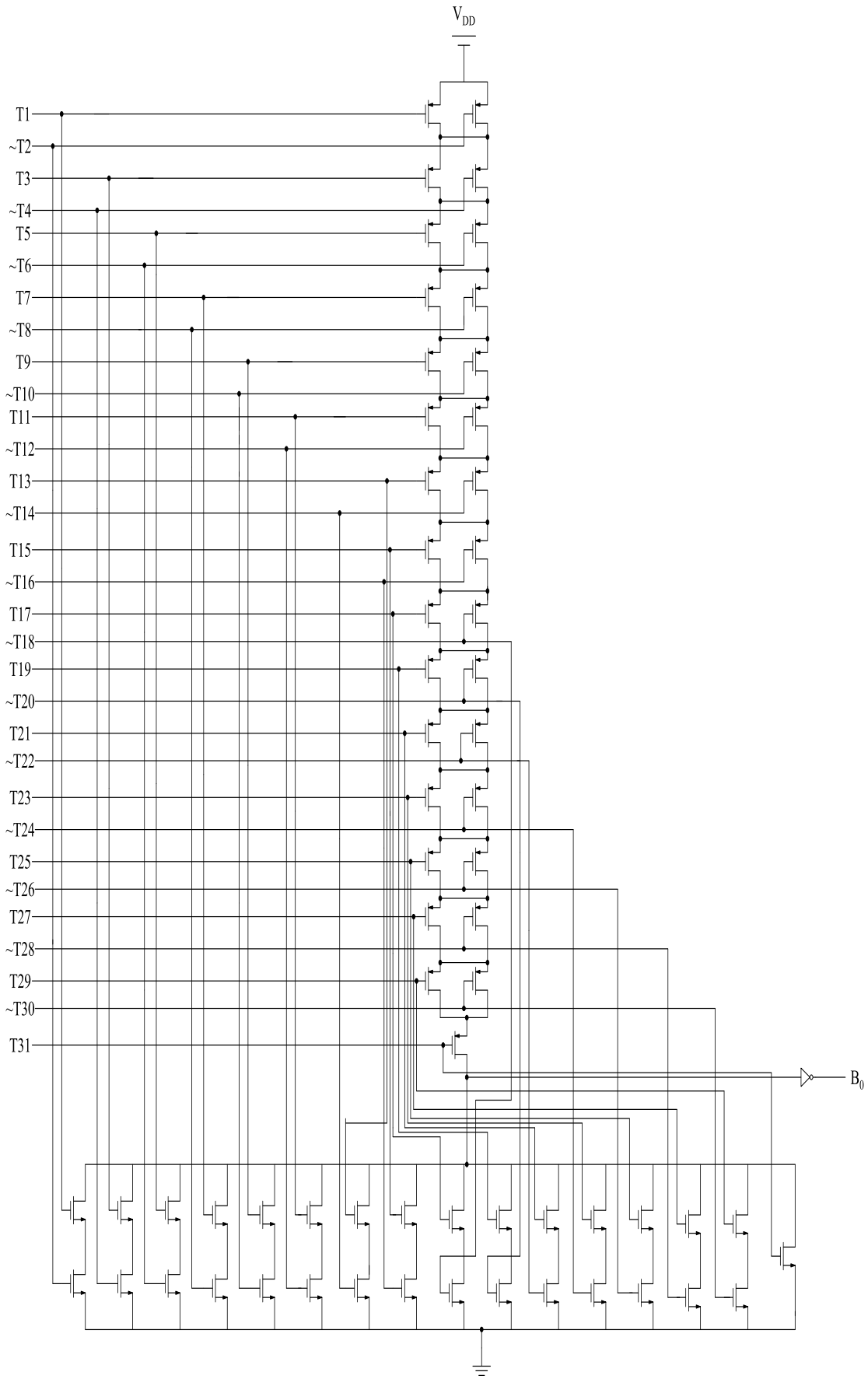
2.362 mW. Due to the large number of transistors used in the pull up as well as pull down path, the maximum frequency of operation achieved is very low. To achieve high frequency of operation, dynamic logic implementation is preferred.



(c) Binary code B_2 generation circuit



(d) Binary code B_1 generation circuit



(e) Binary code B_0 generation circuit

Fig. 4.22 Binary code generation circuit using static CMOS logic

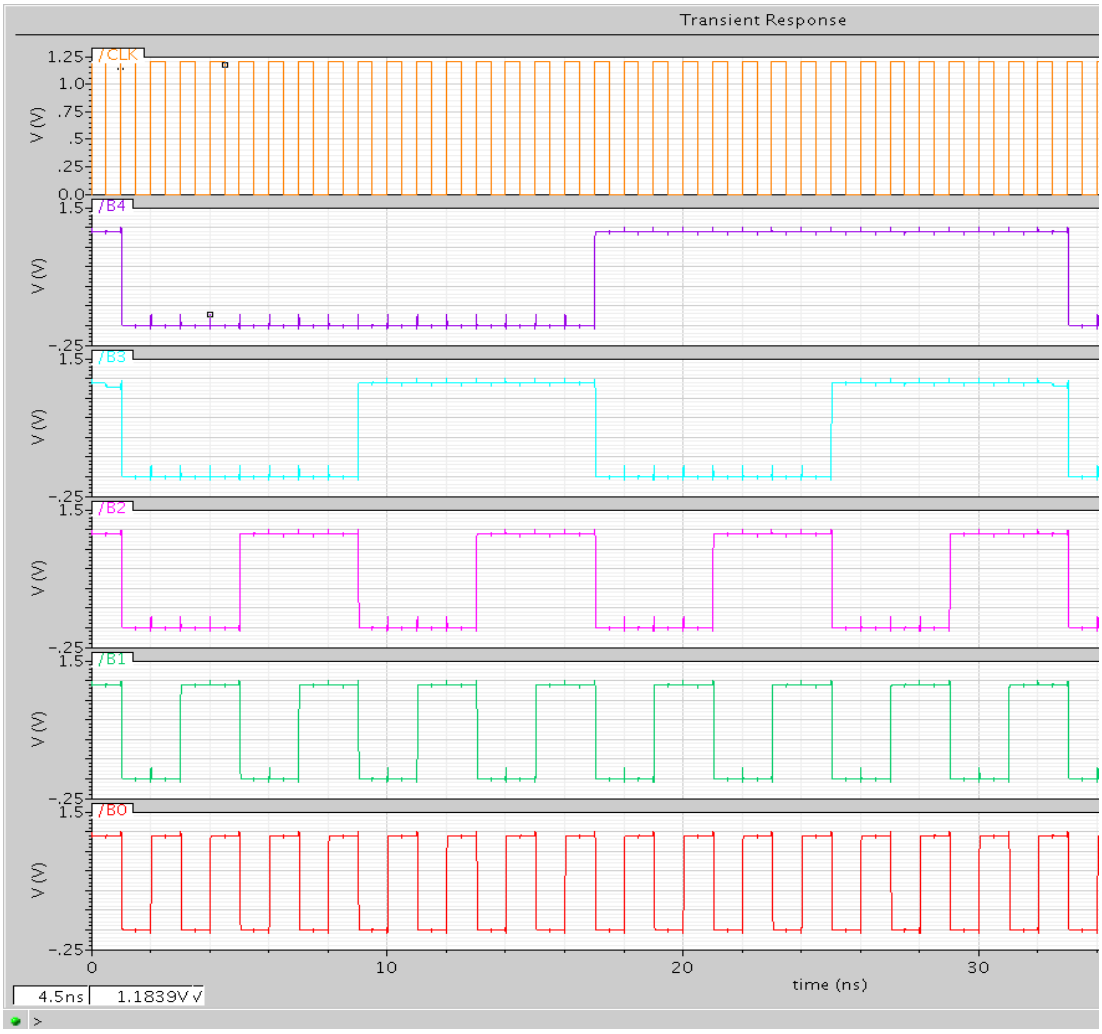
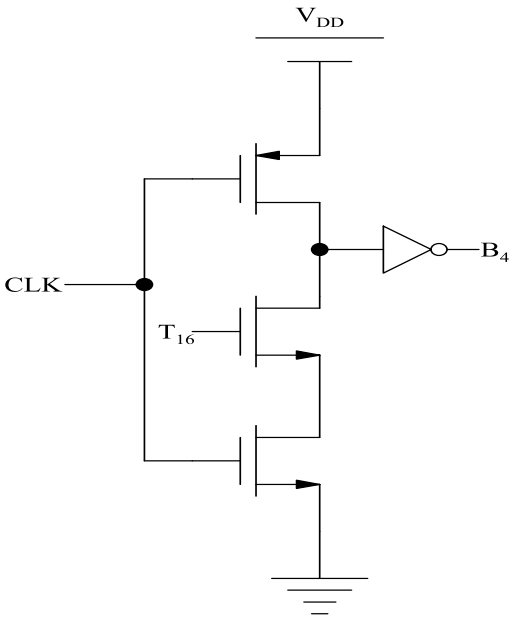


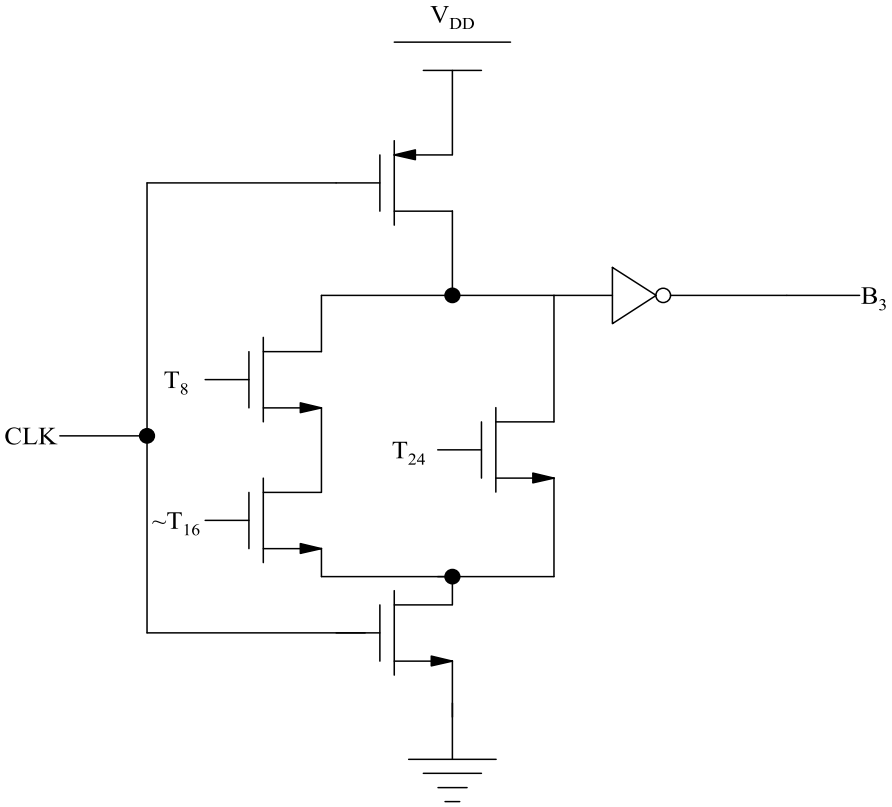
Fig. 4.23 Simulation of binary encode using static CMOS

ii. Dynamic Logic [66]

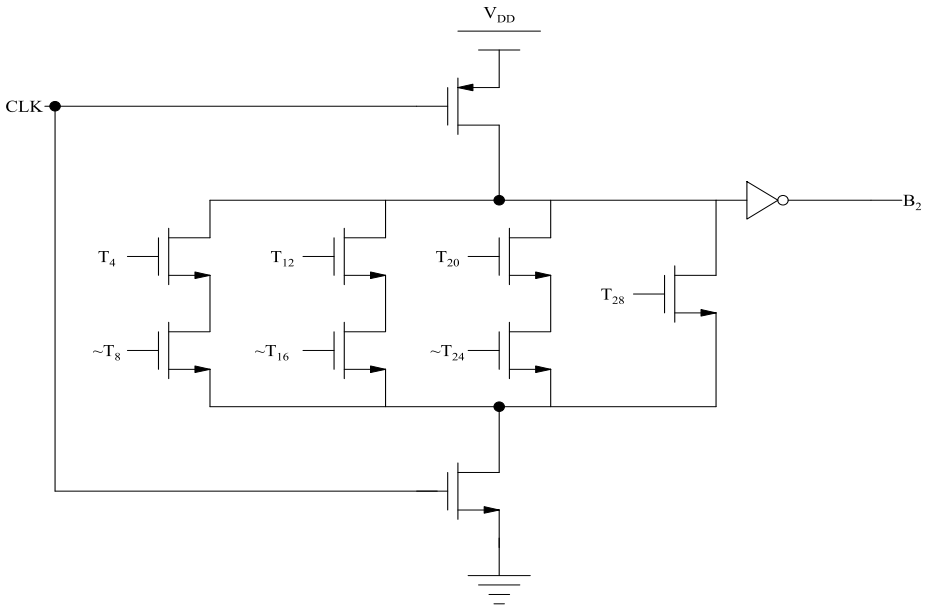
Dynamic logic implementation has faster switching speed in comparison with static CMOS because of the lower number of transistors required for implementation and single transistor load per fan in. The low and high output levels of V_{OL} and V_{OH} are GND and V_{DD}. The schematic implementations of the binary bits are shown in Fig. 4.24. One PMOS transistor (CLK=0) in the pull up path and three NMOS transistors in the pull down path effectively decides the critical path delay. The critical path delay in the dynamic logic implementation is 0.25 ns. The simulation result shows that (Fig. 4.25) the maximum frequency of operation achieved is 4 GHz with a power dissipation of 1.212 mW. With the reduction of number of transistors for the implementation, maximum frequency of operation obtained can be increased by four times as compared with static CMOS implementation. In order to increase the frequency of operation further, pseudo NMOS logic is used.



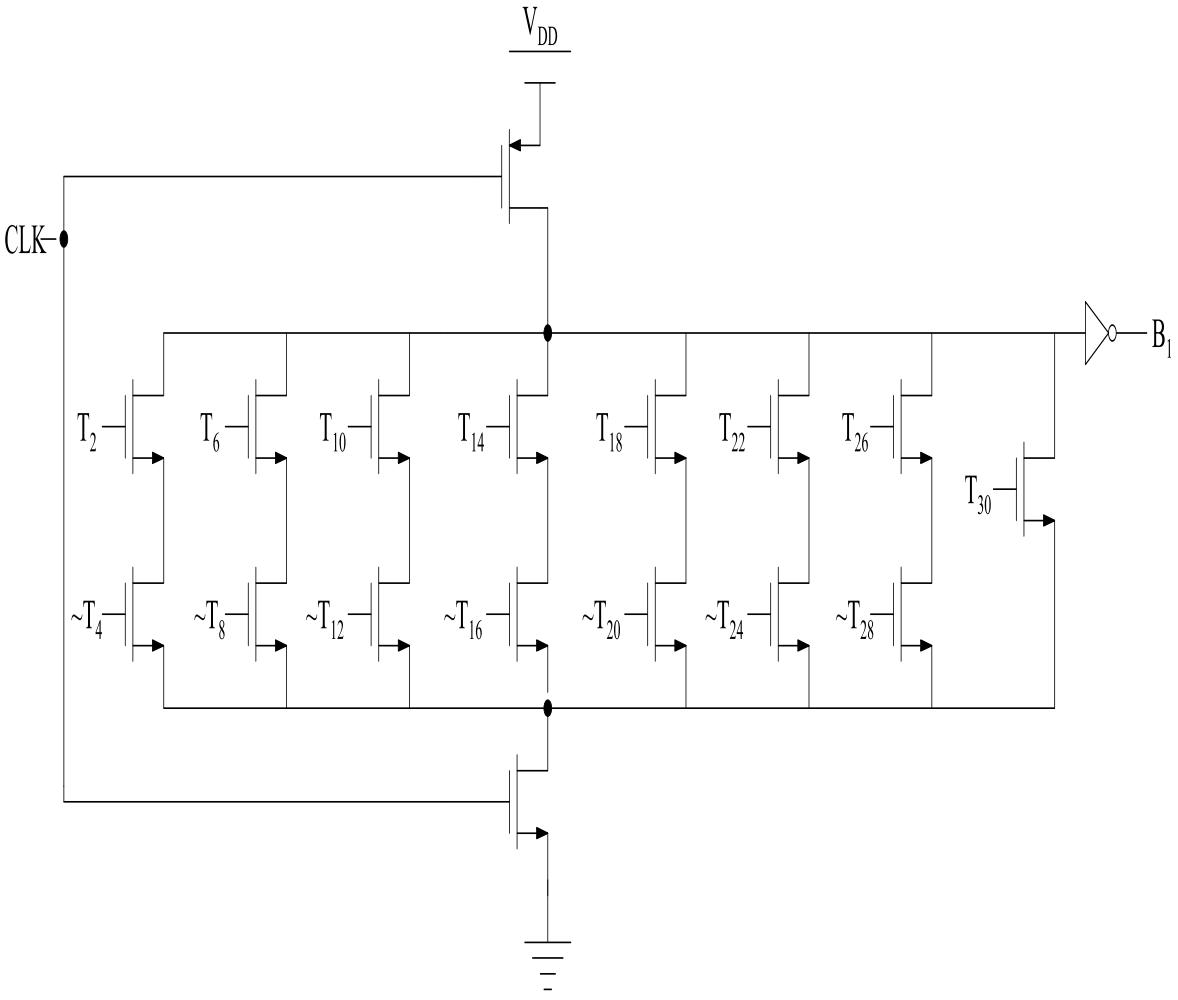
(a) Binary code B_4 generation circuit using dynamic logic



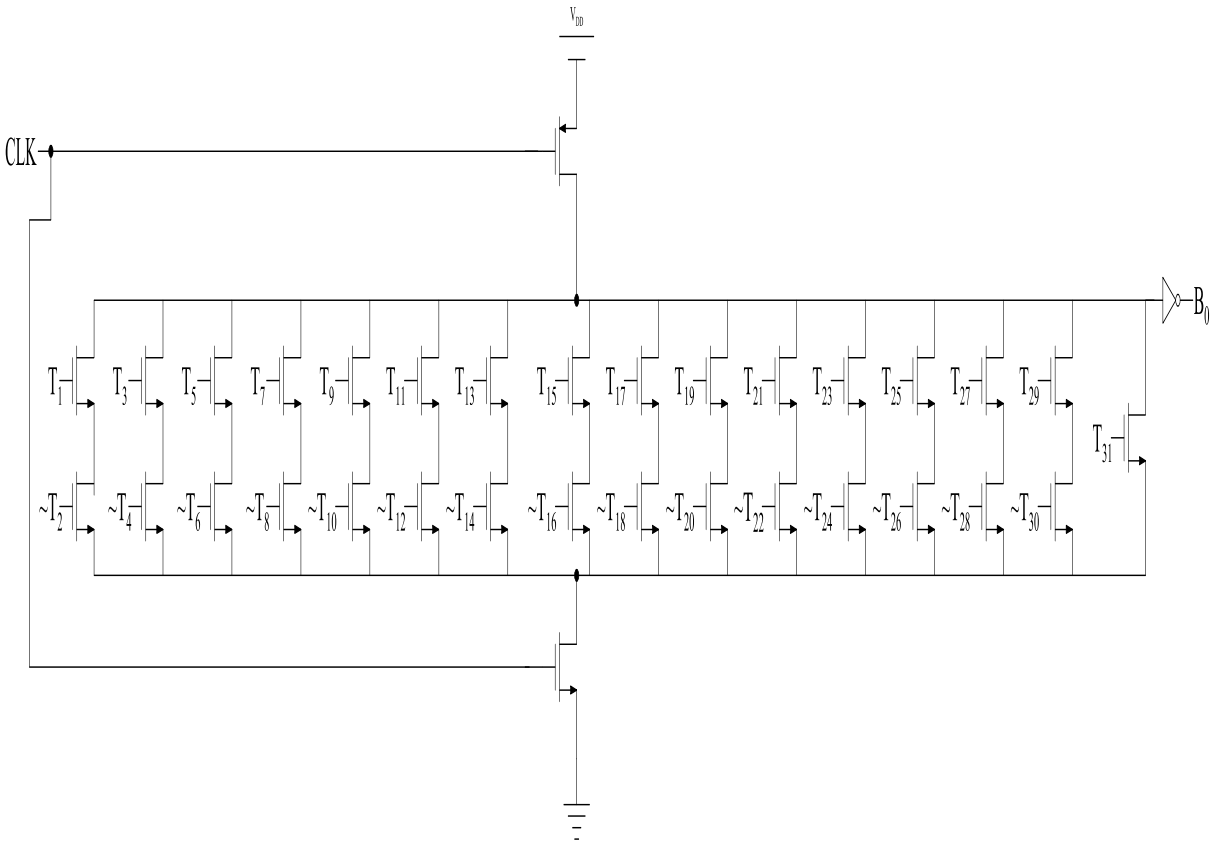
(b) Binary code B_3 generation circuit using dynamic logic



(c) Binary code B_2 generation circuit using dynamic logic



(d) Binary code B_1 Generation circuit using dynamic logic



(e) Binary code B_0 Generation circuit using dynamic logic

Fig. 4.24 Binary code generation circuit using dynamic logic

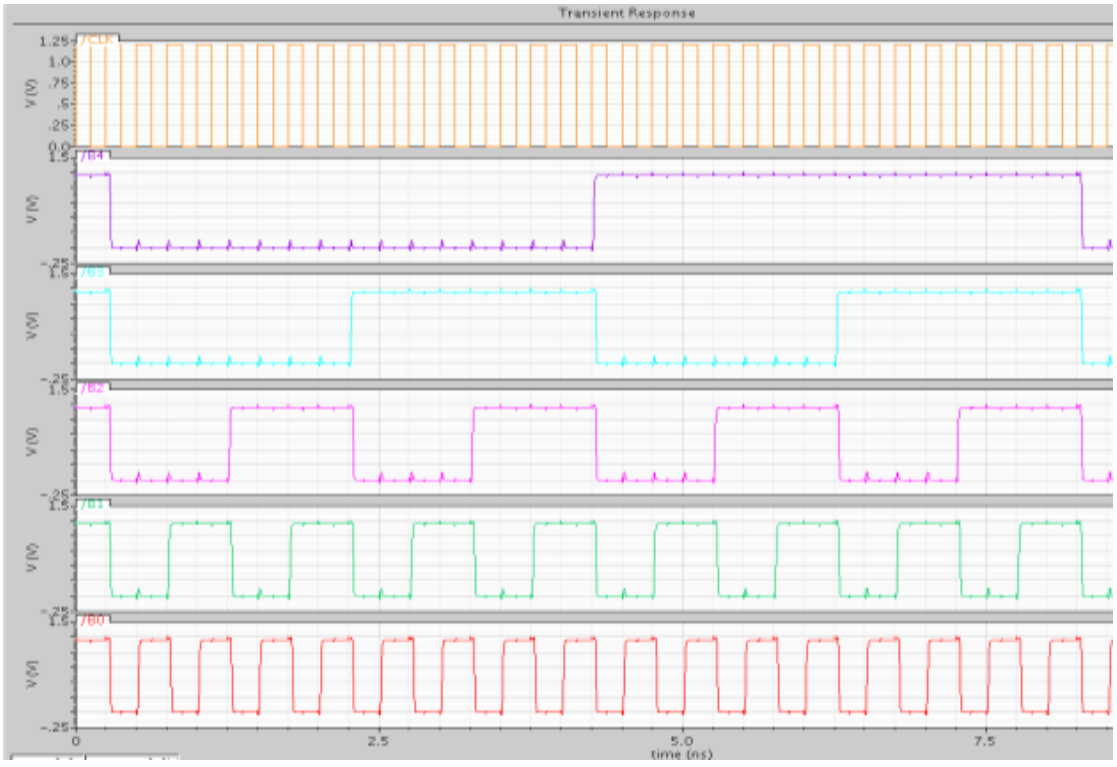
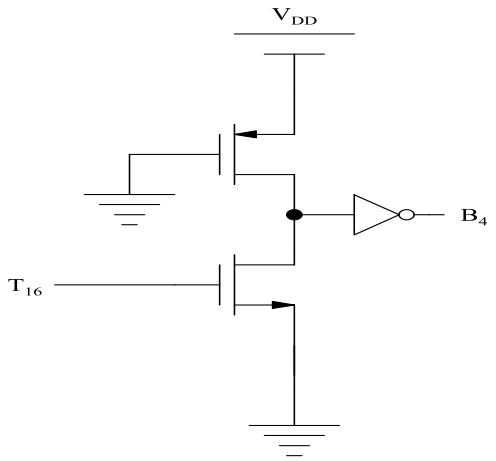


Fig. 4.25 Simulation of binary encoder using dynamic logic

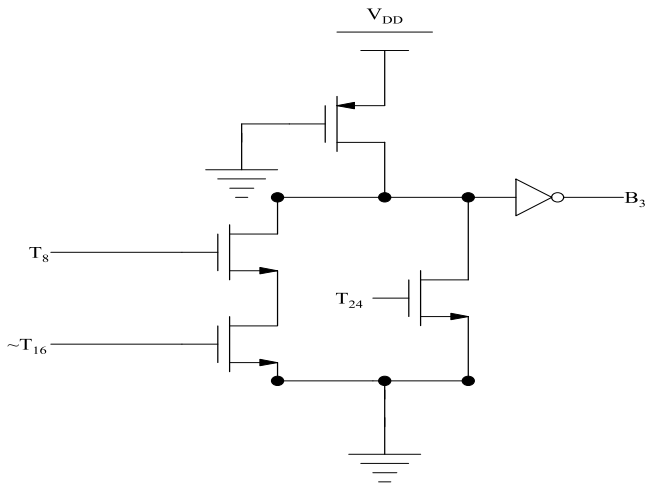
iii. Pseudo NMOS logic [66]

For the implementation of N input logic gate, pseudo NMOS needs N+1 transistors. In pseudo NMOS, only one PMOS transistor is used in the pull up part which is connected to ground. The pull up path is always ON that causes static power dissipation. When the pull up path is ON simultaneously with pull down path, a small amount of current flows from V_{DD} to ground which causes static power dissipation. The nominal high output voltage of (V_{OH}) of pseudo NMOS logic is V_{DD} (Assuming that the pull down network is switched off) and the nominal low output voltage (V_{OL}) is not zero. This results in reduced noise margins. For the implementation of the positive logics (eg: AND, OR gate) a static CMOS inverter is added at the output side. This improves the noise margin of the circuit. The output is evaluated conditionally depending upon the value of the inputs in the pull down network. The inverter on the output transforms the inverted gate to non inverted gate. Since the voltage swing on the output and the overall functionality of the gate depend on the ratio of the NMOS and PMOS sizes, the transistor sizing plays a crucial role in the implementation design.

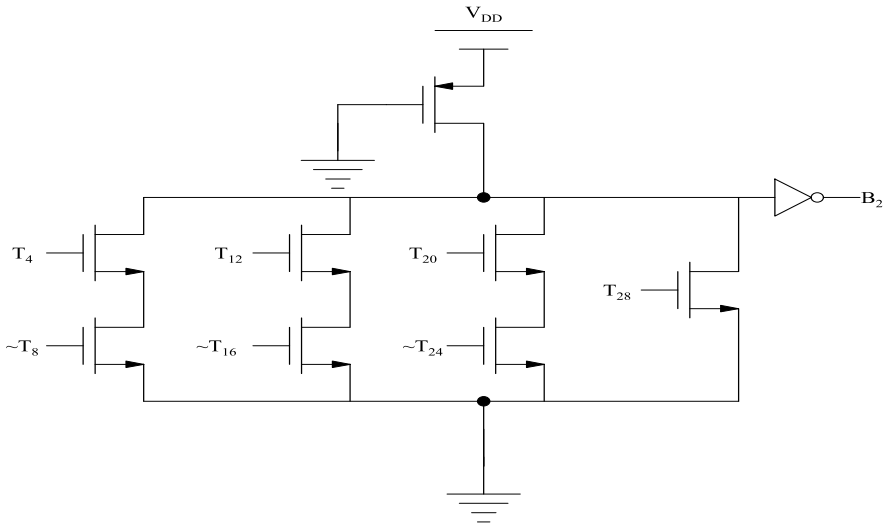
One PMOS transistor in the pull up path and two NMOS transistors in the pull down path effectively calculates the critical path delay. The critical path delay of this implementation is reduced to 0.2 ns with pseudo NMOS logic. The implementation circuits are shown in Fig. 4.26. With the use of less number of transistors and extra power dissipation, maximum frequency of operation achieved is 5 GHz with a power dissipation of 1.823 mW (Fig. 4.27). In order to reduce power dissipation, by keeping the frequency of operation same, pseudo dynamic CMOS logic is preferred.



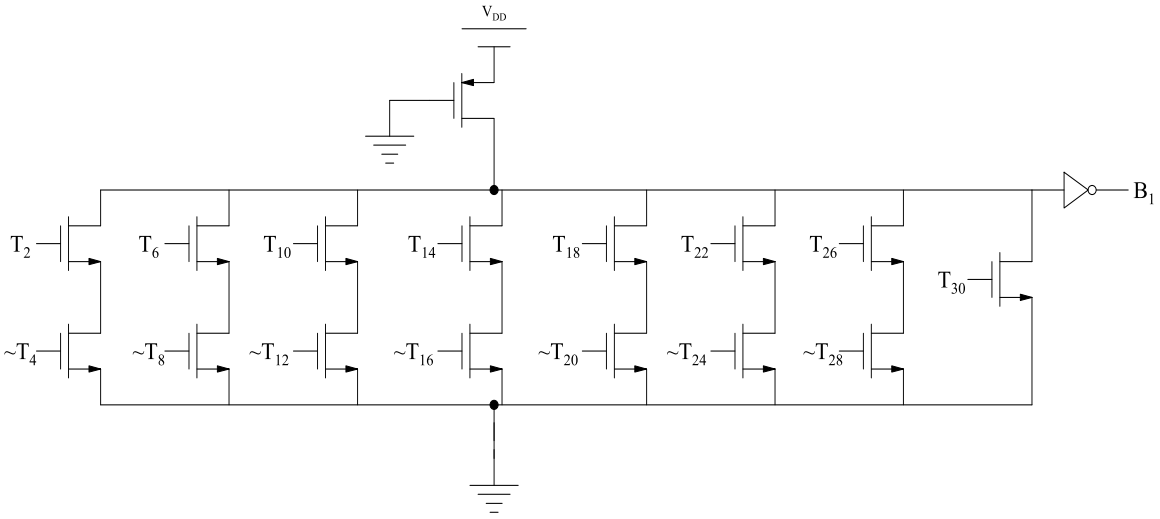
(a) Binary code B_4 generation circuit using pseudo NMOS logic



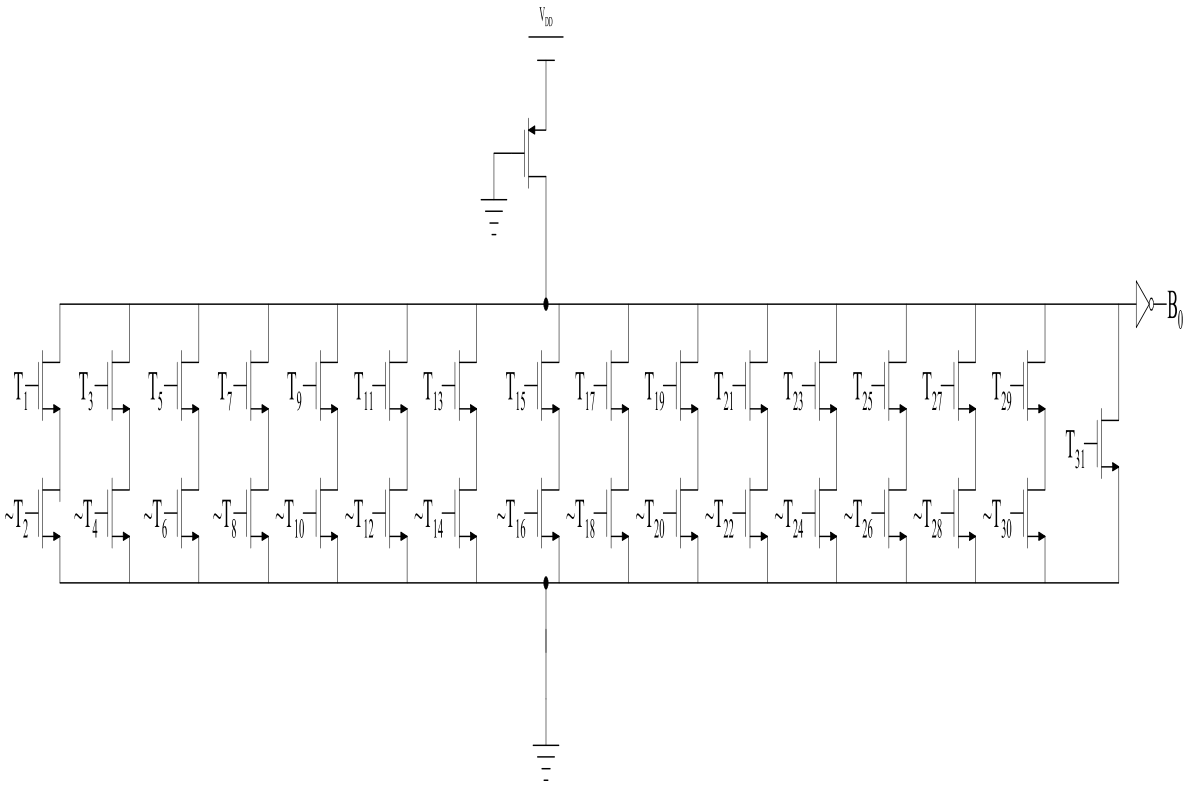
(b) Binary code B_3 generation circuit using pseudo NMOS logic



(c) Binary code B_2 generation circuit using pseudo NMOS logic



(d) Binary code B_1 generation circuit using pseudo NMOS logic



(e) Binary code B_0 generation circuit using pseudo NMOS logic

Fig. 4.26 Binary code B_0 generation circuit using pseudo NMOS logic

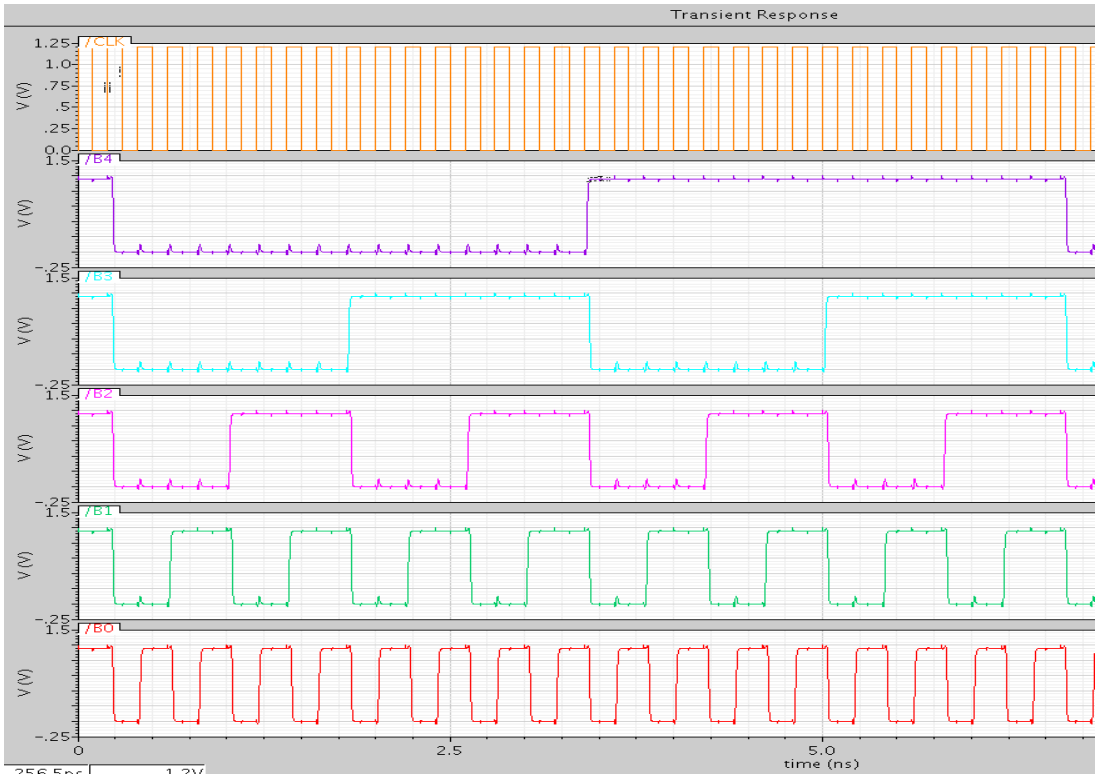
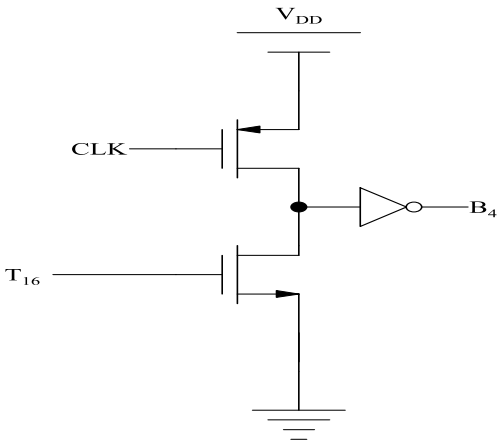


Fig. 4.27 Simulation of binary encode using pseudo NMOS

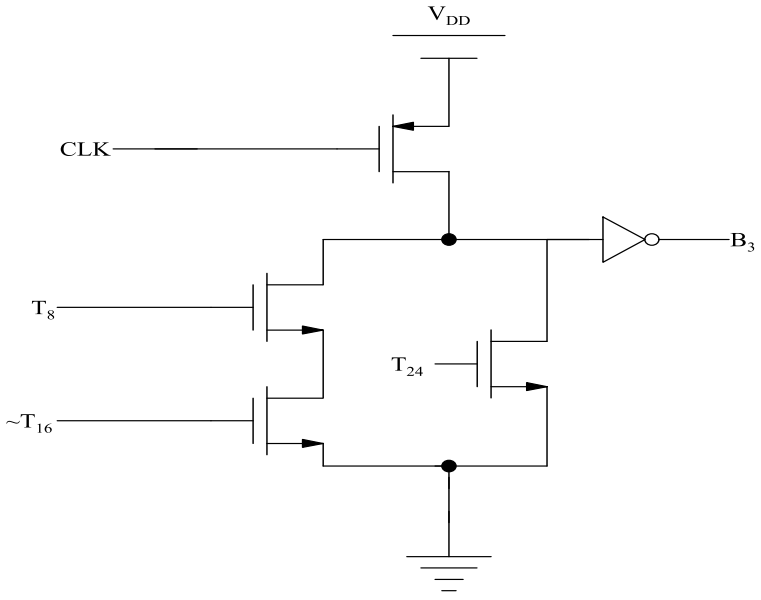
iv. Pseudo dynamic CMOS logic [65]

The number of transistors used for implementation of N input logic gate is same as that of pseudo NMOS logic. Pseudo dynamic CMOS logic circuit comprises of a PMOS transistor with gate connected to clock, a group of NMOS transistors for the implementation of the logic style in the pull down network and an inverter.

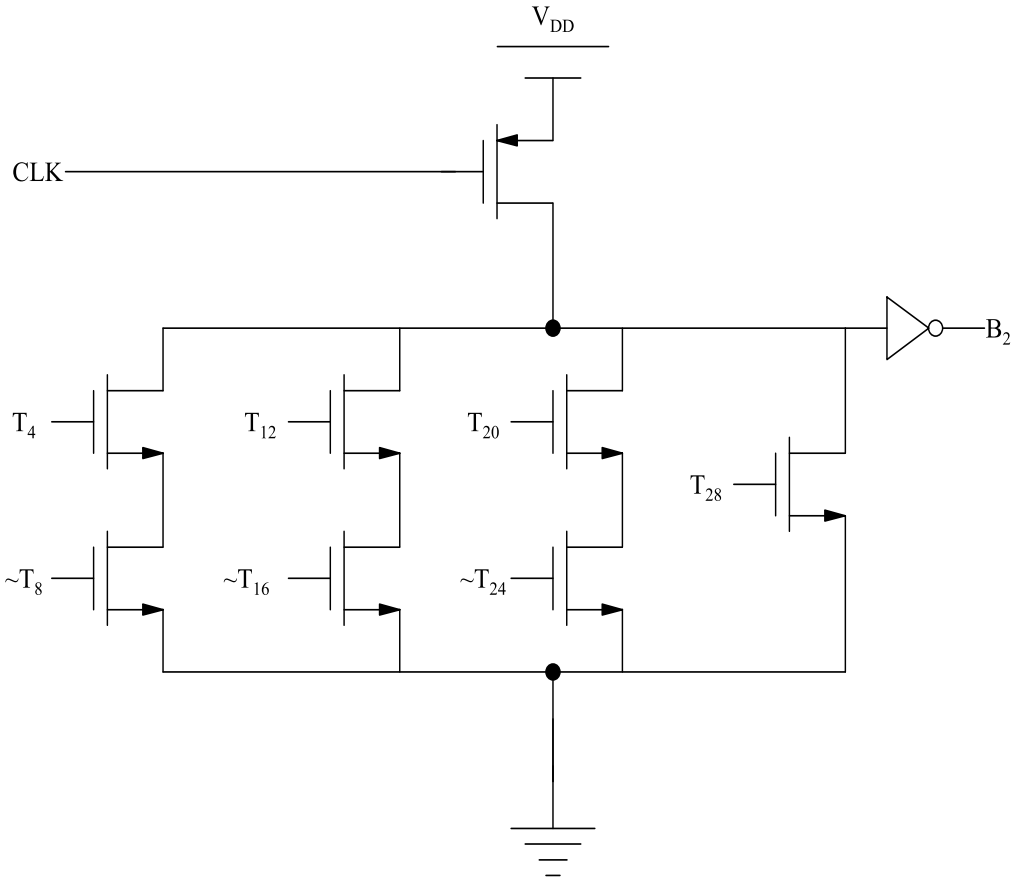
The critical path delay of the implementation is 0.2 ns (same as that of pseudo NMOS logic). The schematic implementation of MSB is shown in Fig. 4.28(a, b, c, d and e). The simulation result (Fig. 4.29) shows that maximum frequency of operation achieved is 5 GHz with a power dissipation of 1.324 mW.



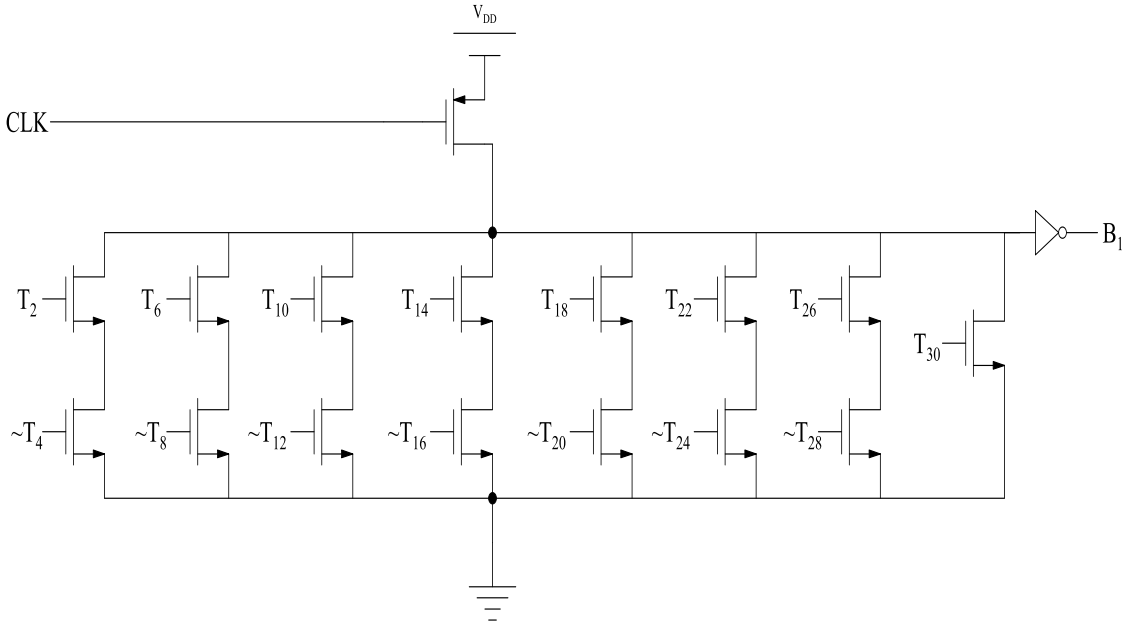
(a) Binary code B_4 generation circuit using pseudo dynamic CMOS logic



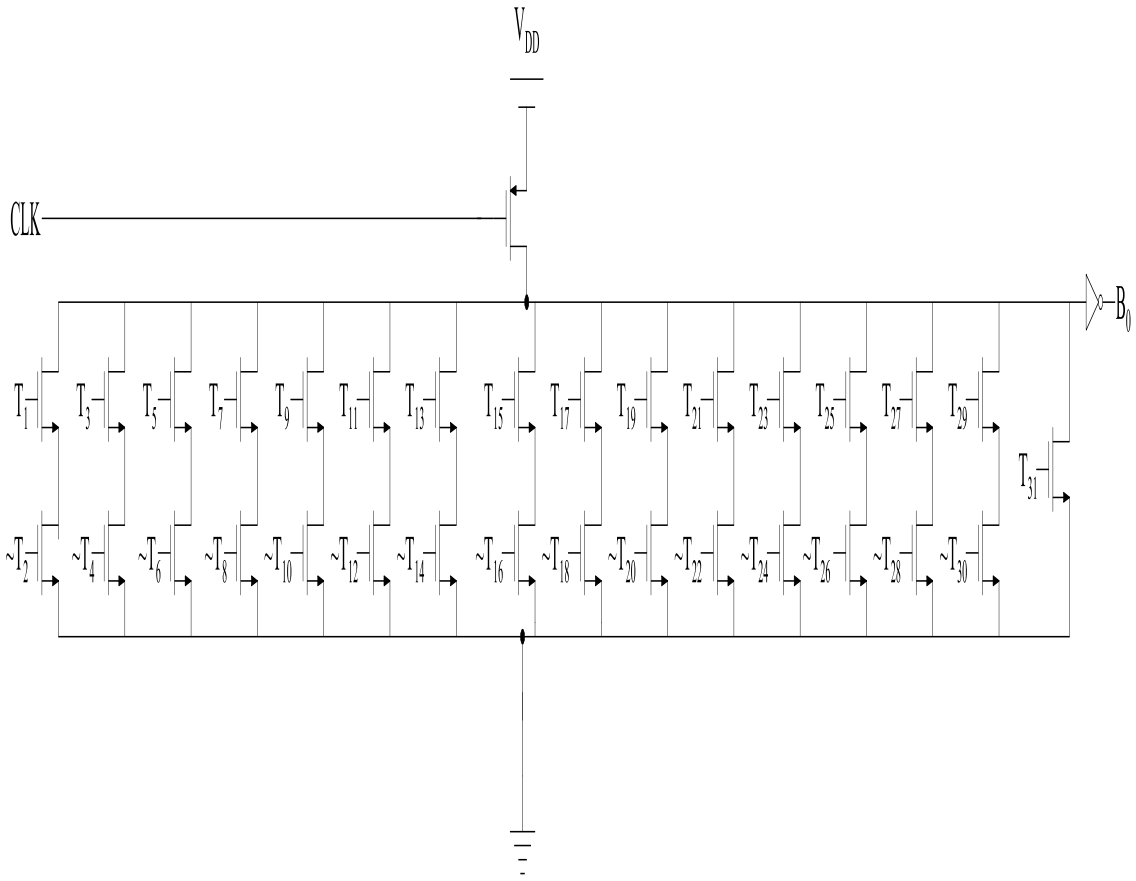
(b) Binary code B_3 generation circuit using pseudo dynamic CMOS logic



(c) Binary code B_2 generation circuit using pseudo dynamic CMOS logic



(d) Binary code B_1 generation circuit using pseudo dynamic CMOS logic



(e) Binary code B_0 generation circuit using pseudo dynamic CMOS logic

Fig. 4.28 Binary code generation circuit using pseudo dynamic CMOS logic

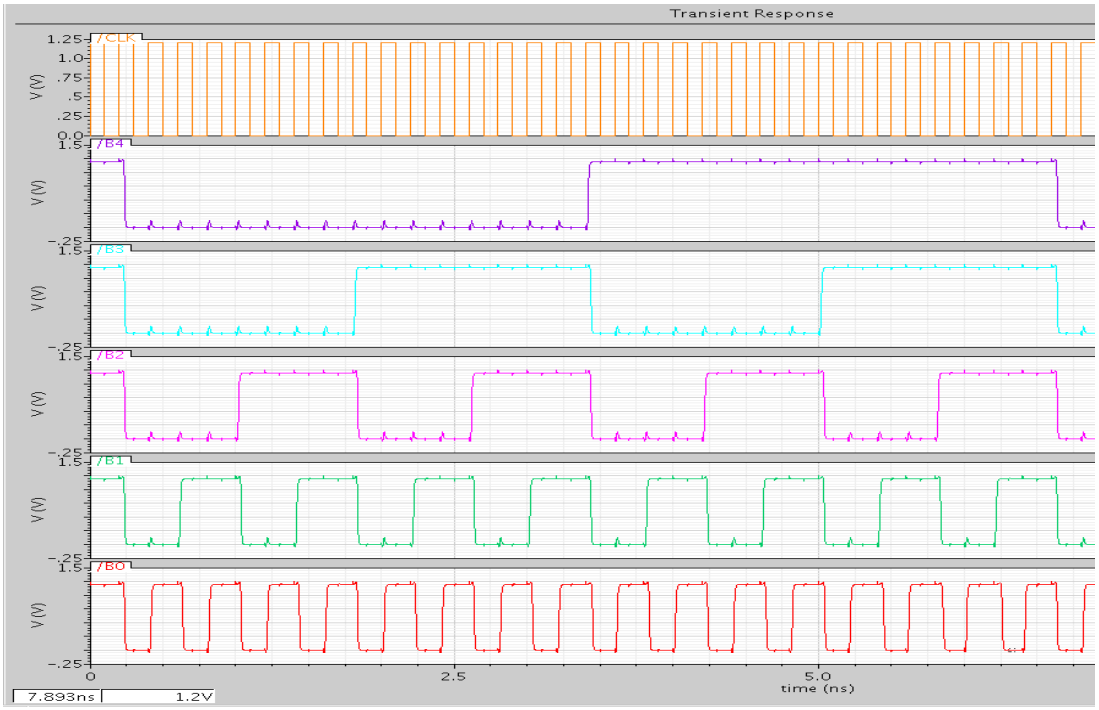


Fig. 4.29 Simulation of binary encoder using pseudo dynamic CMOS logic

C. Comparison of different logic styles of implementation and discussion

Critical path delay, maximum frequency of operation, power dissipation, power delay product for each of the logic style is shown below in Table 4.7. Entire circuit is drawn and simulated in 90 nm technology with a power supply of 1.2 V. In order to equalize the propagation delay (low to high and high to low), size of PMOS transistor is made two times as that of NMOS transistor.

To achieve maximum frequency of operation, direct conversion method is used in this approach. Static CMOS implementation is generally preferred in the noisy environment due to the property of less sensitivity towards the noise. As the circuit size increases, the number of transistor usage also increases largely which increases the power dissipation. The maximum frequency of operation of static CMOS implementation of the conversion is 1 GHz. To improve the speed, dynamic logic implementation is used. With this implementation, maximum of 4 GHz operation is attained. To further improve the speed as well as to reduce the number of transistors, pseudo NMOS logic implementation is used. By using pseudo NMOS logic, maximum of 5 GHz operation is obtained with a very high value of power dissipation. To reduce the power dissipation by keeping the frequency of operation same, pseudo dynamic CMOS logic implementation is used. Smaller critical path delay, low transistor count and medium values of power dissipation and power delay product makes pseudo dynamic CMOS logic implementation a preferable choice over other logic style implementation for high speed flash ADC design.

Table 4.7 Comparison of different logic styles

Parameters	Static CMOS	Dynamic Logic	Pseudo NMOS	Pseudo Dynamic CMOS
Critical Path delay	1 ns	.25 ns	.2 ns	.2 ns
Max. Frequency of Operation	1 GHz	4 GHz	5 GHz	5 GHz
Power Dissipation	2.362 mW	1.212mW	1.823 mW	1.324 mW
Power Delay Product	2.362 pJ	0.303 pJ	0.3646 pJ	0.2648 pJ

The transistor sizes used in all the implementations of the encoder are given in Table 4.8.

Table 4.8 Transistor Sizes

(W/L) PMOS	240 nm/100 nm
(W/L) NMOS	120 nm/100 nm

4.2.10 A High speed noise tolerant encoder for a 5 GS/s five bit flash ADC

The present investigation proposes an efficient high speed encoding scheme intended for a 5 GS/s five bit flash analog-to-digital converter. The conversion of a thermometer code to binary code is one of the demanding issues in the design of a high speed flash ADC. An encoder circuit in this approach translates the thermometer code into the intermediate gray code to reduce the effects of bubble errors [63, 81]. To increase the speed of the encoder, the implementation of the encoder through pseudo dynamic CMOS logic is presented. The proposed encoder is designed using 90 nm technology at 1.2 V power supply using CADENCE tool.

A. Design of the proposed encoder

Conversion of the thermometer code output to binary code is one of the crucial parts in high speed flash ADC design. Bubble error occurrence in the thermometer code is one of the predominant problems which is reduced or removed to enhance the accuracy of the analog-to- digital converter [81, 84]. The bubble error usually results from timing difference between clock and signal lines and it is a situation where a '1' is found above zero in thermometer code. For very fast input signals, small timing difference can cause bubbles in output code. Depending on the number of successive zeroes, the bubbles are characterized as of first, second and higher orders. To reduce the effect of bubbles in thermometer code, one of the widely used methods is to convert the thermometer code to gray code [62, 76 and 80]. The truth table corresponding to five bit gray code is presented in Table 4.9. The relationship between thermometer code, gray code and binary code is given below in (4.7) and (4.8).

$$G_4 = T_{16}$$

$$G_3 = T_8\overline{T_{24}}$$

$$G2 = T_4\overline{T_{12}} + T_{20}\overline{T_{28}}$$

$$G_1 = T_2\overline{T_6} + T_{10}\overline{T_{14}} + T_{18}\overline{T_{22}} + T_{26}\overline{T_{30}} \quad (4.7)$$

$$G_0 = T_1\overline{T_3} + T_5\overline{T_7} + T_9\overline{T_{11}} + T_{13}\overline{T_{15}} + T_{17}\overline{T_{19}} + T_{21}\overline{T_{23}} + T_{25}\overline{T_{27}} + T_{29}\overline{T_{31}}$$

$$B_4 = G_4$$

$$B_3 = G_3 \oplus B_4$$

$$B_2 = G_2 \oplus B_3$$

$$B_1 = G_1 \oplus B_2 \quad (4.8)$$

$$B_0 = G_0 \oplus B_1$$

Table 4.9 Gray code encoder truth table

G_4	G_3	G_2	G_1	G_0	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	1	00000000000000000000000000000011
0	0	0	1	0	00000000000000000000000000000111
0	0	1	1	0	00000000000000000000000000001111
0	0	1	1	1	00000000000000000000000000011111
0	0	1	0	1	00000000000000000000000000111111
0	0	1	0	0	00000000000000000000000001111111
0	1	1	0	0	00000000000000000000000011111111
0	1	1	0	1	00000000000000000000000111111111
0	1	1	1	1	00000000000000000000001111111111
0	1	1	1	0	00000000000000000000011111111111
0	1	0	1	0	00000000000000000000111111111111
0	1	0	1	1	00000000000000000001111111111111
0	1	0	0	1	00000000000000000011111111111111
0	1	0	0	0	00000000000000000111111111111111
1	1	0	0	0	00000000000000001111111111111111
1	1	0	0	1	00000000000000011111111111111111

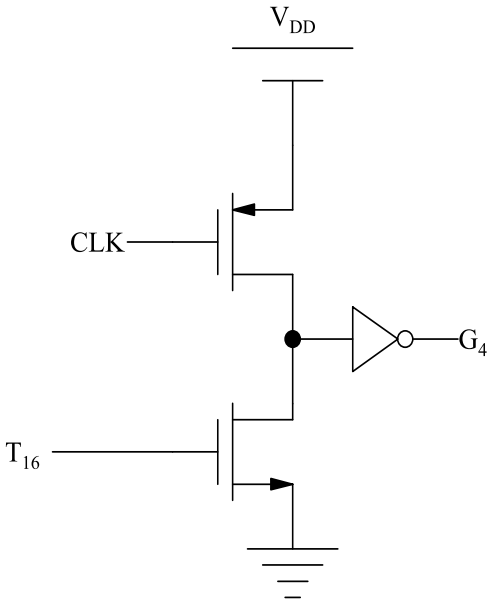
1	1	0	1	1	00000000000001111111111111111111
1	1	0	1	0	00000000000011111111111111111111
1	1	1	1	0	00000000001111111111111111111111
1	1	1	1	1	00000000011111111111111111111111
1	1	1	0	1	00000000111111111111111111111111
1	1	1	0	0	00000001111111111111111111111111
1	0	1	0	0	00000011111111111111111111111111
1	0	1	0	1	00000111111111111111111111111111
1	0	1	1	1	00001111111111111111111111111111
1	0	1	1	0	00011111111111111111111111111111
1	0	0	1	0	00111111111111111111111111111111
1	0	0	1	1	01111111111111111111111111111111
1	0	0	0	1	11111111111111111111111111111111
1	0	0	0	0	11111111111111111111111111111111

The equations for this encoder are derived from the truth table provided in Table 4.9.

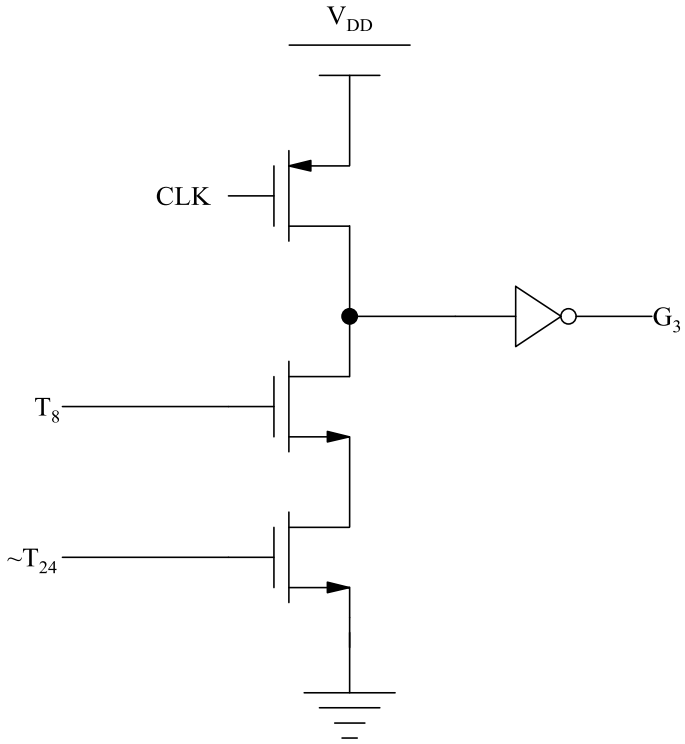
B. Implementation of the proposed encoder

There are different logic styles to implement the encoder design. Generally the implementation is done using static CMOS logic style. The advantage of static CMOS logic style is that it is having the lowest power consumption with a lower speed. For achieving a higher speed, other logic styles are preferred. Here the design is implemented using a logic style called pseudo dynamic CMOS logic. The disadvantage with the pseudo dynamic CMOS logic is that it has static power dissipation [66] (The power dissipation occurs when a direct current flows between V_{DD} and ground. That is when both pull up and pull own networks are switched on simultaneously).

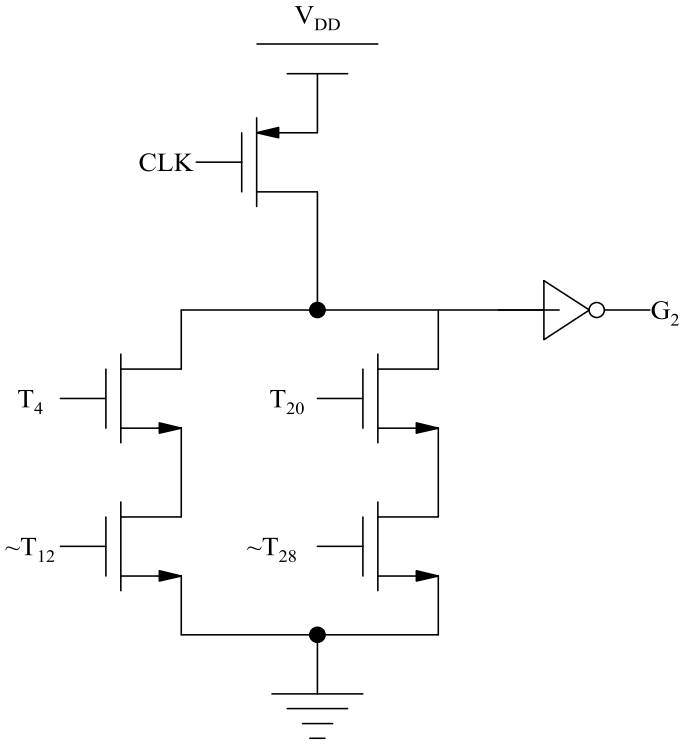
The schematic of the gray code encoder for each bit is designed using proposed circuit is shown in Fig. 4.30. With the help of XOR gate, the gray code is converted to binary code. The schematic of two input XOR gate is shown in Fig. 4.31.



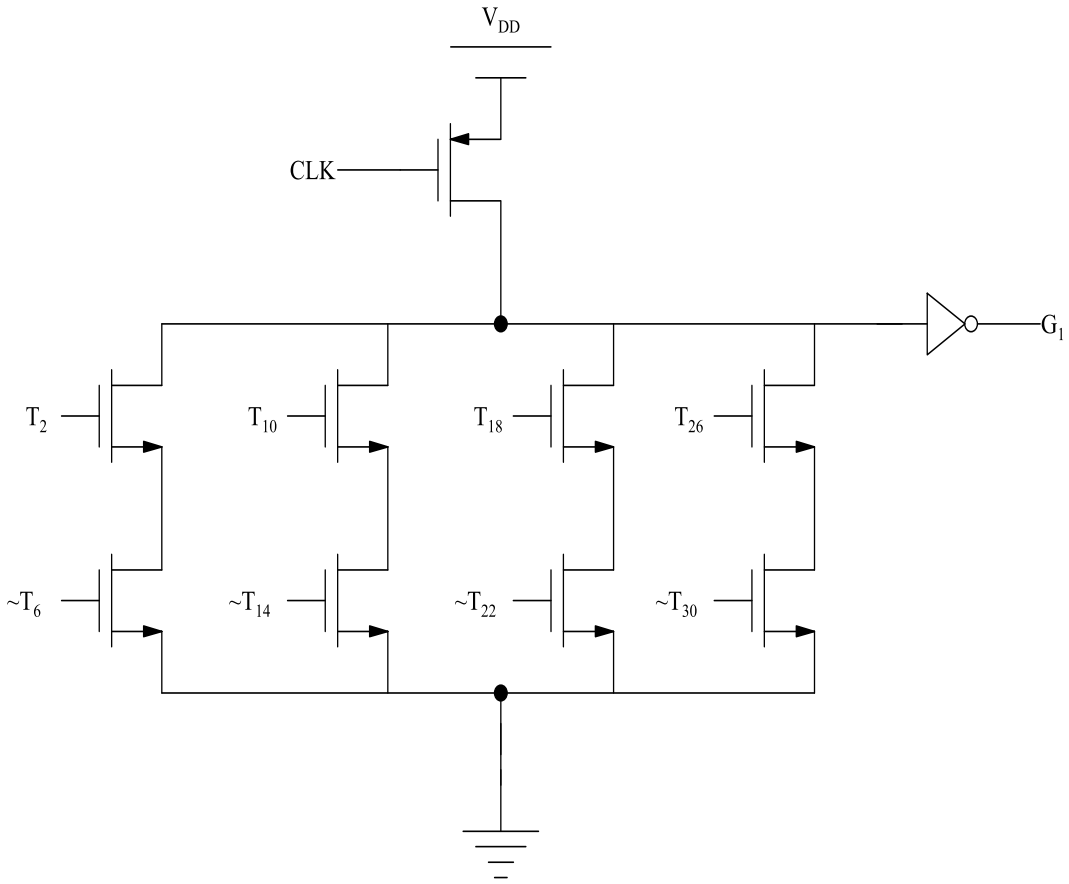
(a) Gray code G_4 generation circuit



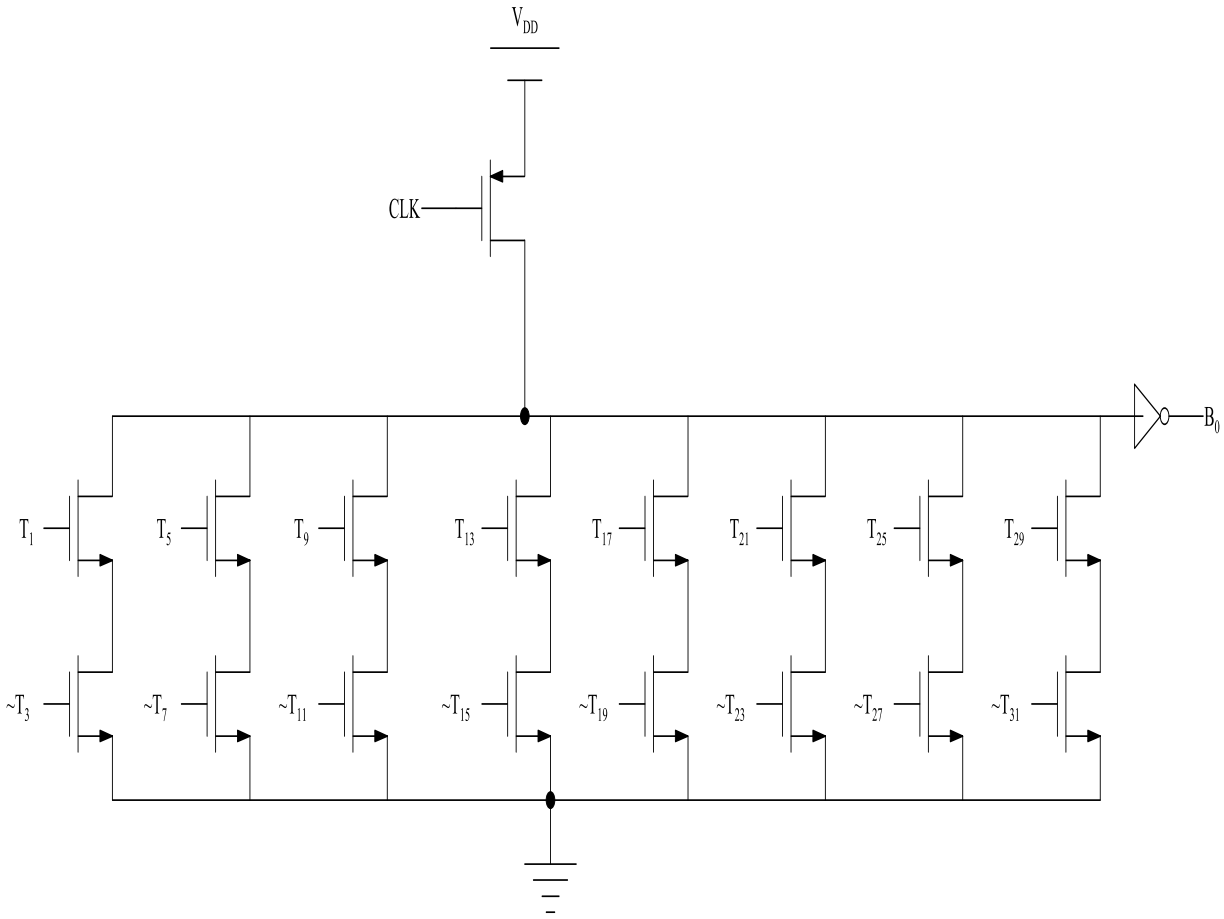
(b) Gray code G_3 generation circuit



(c) Gray code G_2 generation circuit



(d) Gray code G_1 generation circuit



(e) Gray code G_0 generation circuit

Fig. 4.30 Gray code generation circuit using pseudo dynamic logic

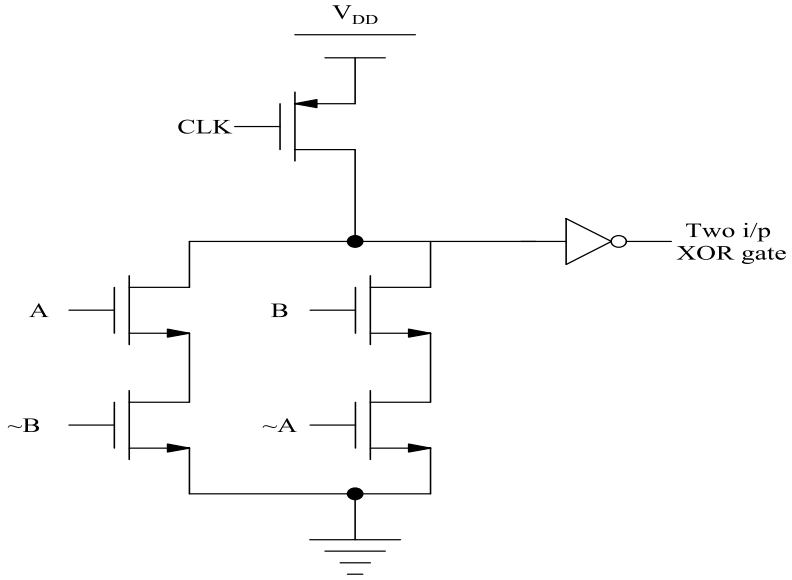


Fig. 4.31Schematic of two input XOR gate

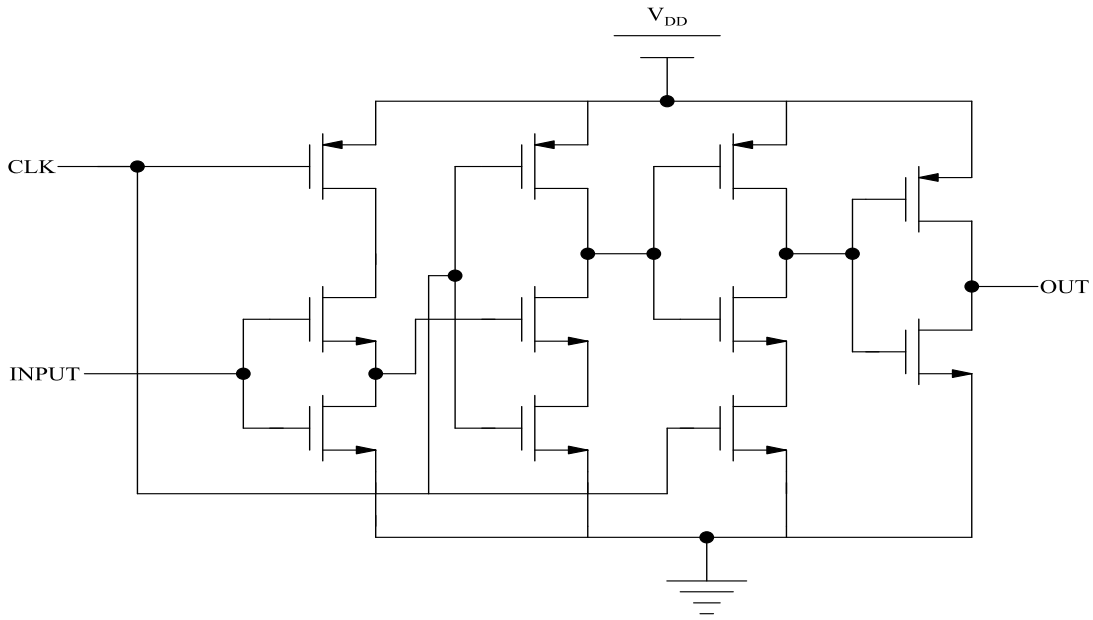


Fig. 4.32 Schematic of D flip-flop

C. Simulation results and discussion

The encoder is designed and tested using all the input combinations from the truth table and verified. At the output of the gray code a D flip flop (Fig. 4.32) is added to get the undistorted waveform. The gray code output is shown in the Fig. 4.33. As derived from the equation (B), the gray code is converted to binary code and the simulation results are shown in Fig.4. 34. The summary of the encoder simulation results is shown in the table. With the use of proposed encoder, maximum sampling frequency of 5 GS/s can be achieved.

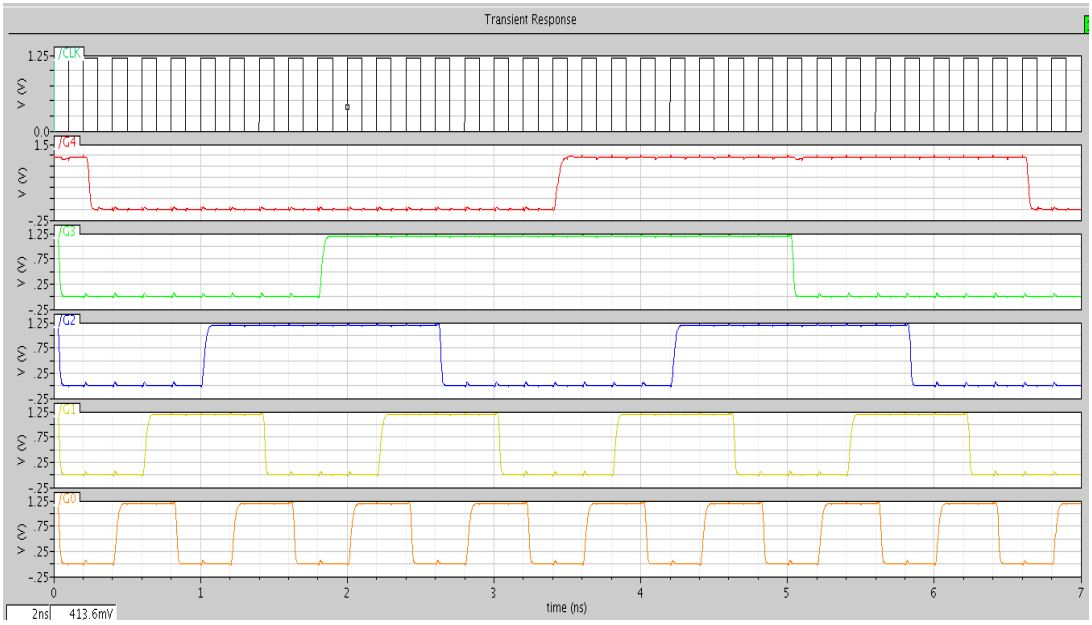


Fig. 4.33 Simulation of gray code encoder

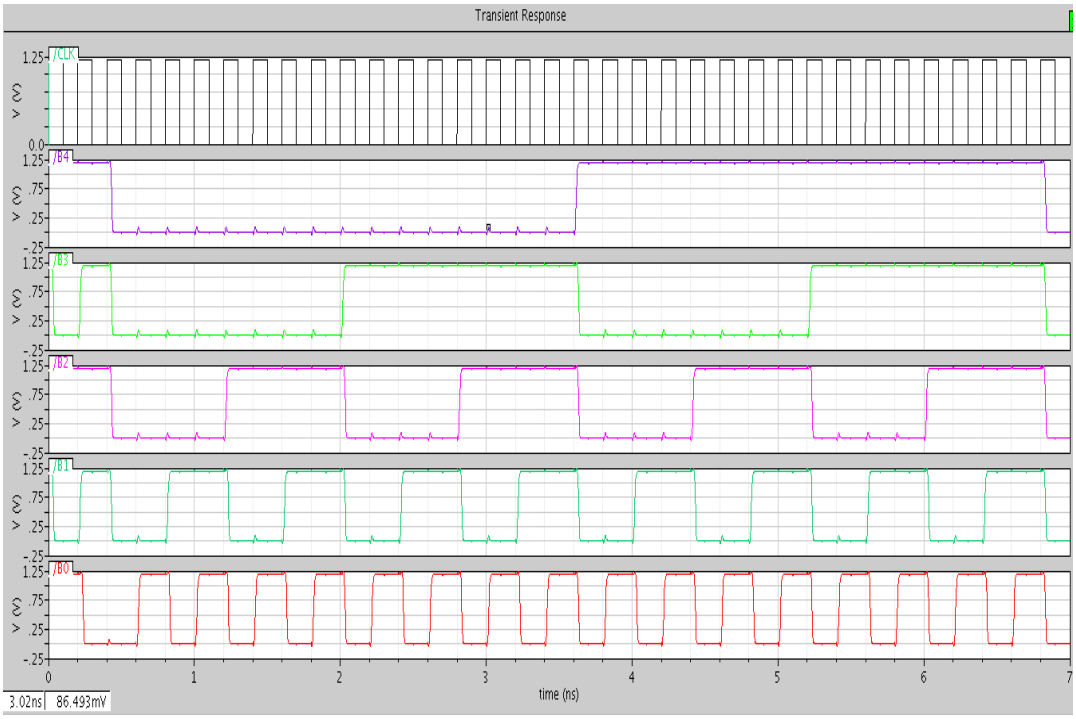


Fig .4.34 Simulation of binary code encoder

In most of the five bit flash ADC's, the maximum sampling frequency can be achieved is below this range. The critical path delay in the proposed implementation is measured to be 0.2 ns. The average power dissipation of the proposed encoder is 1.919 mW. The power delay product of the implementation is 0.3838 pJ.

D. Pre-layout process corner simulation results

Table 4.10 contains the different corner definitions used in the simulation of the encoder which is same as the corner classifications used in the comparator also.

Table 4.10 Corner specifications

Corners	V_{DD} (in Volts)	Temperature (in degree Celsius)
TT	1.20 V	27
SS	1.08 V	80
FF	1.32 V	-20
SF	1.20 V	27
FS	1.21	27

The Table 4.11 gives the pre-layout corner simulation results of the comparator.

Table 4.11 Pre-layout simulation with process corner simulations

Corners	TT	SS	FF	SF	FS
Critical path delay (ns)	0.2	0.25	0.18	0.21	0.19
Maximum frequency of operation (GHz)	5	4	5.55	4.76	5.25
Power dissipation (mW)	1.919	1.524	2.632	1.821	2.235
Power delay product (pJ)	0.3838	0.381	0.47376	0.38241	0.42465

4.2.11 Layout of the proposed encoder

Layout of the proposed encoder is shown in Fig. 4.35. The die area of the proposed layout is 96.5 µm × 58.25 µm.

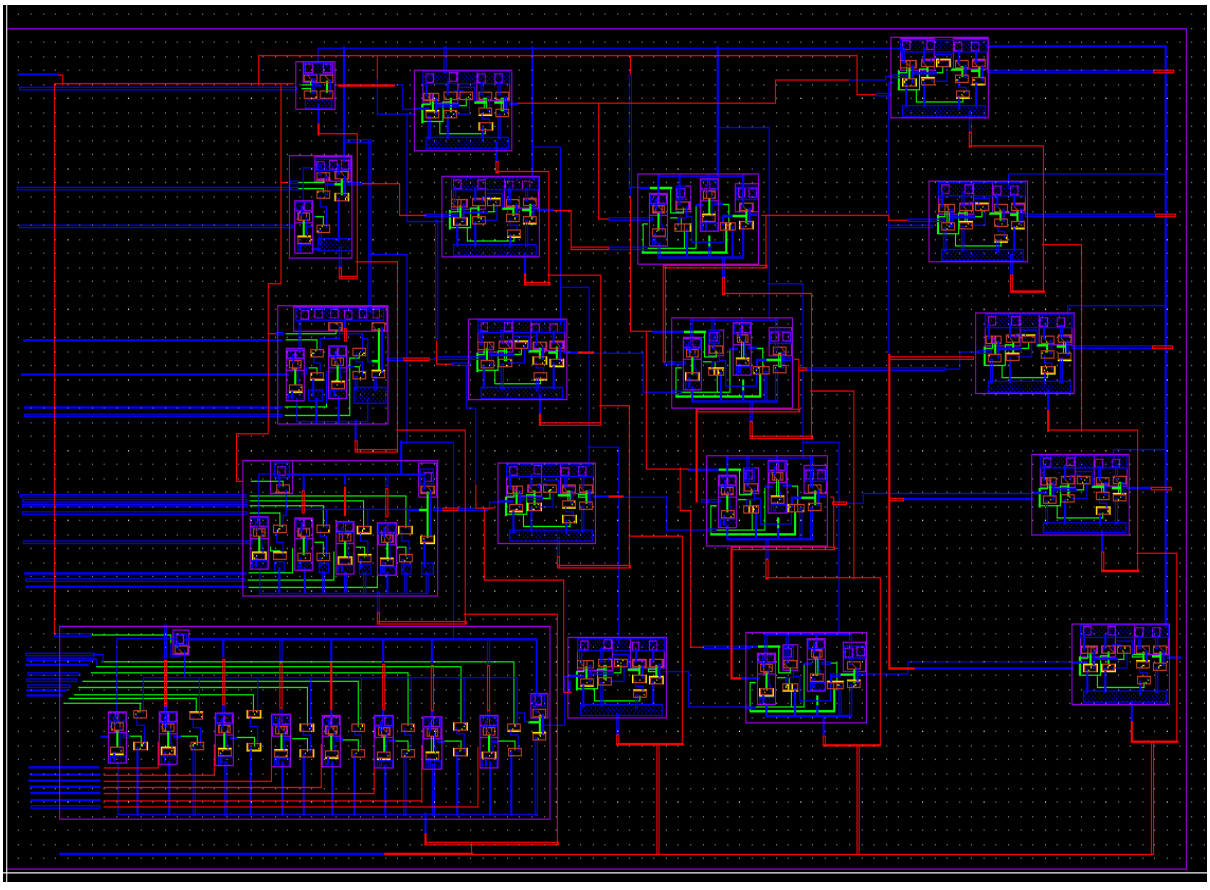


Fig. 4.35 Layout of the proposed encoder

4.2.12 Post layout simulation

The post layout simulation of the transient analysis is shown in Fig. 4.36. The simulation result shows that the proposed encoder is working satisfactorily at a frequency of 5 GHz. As a result of the presence of parasitic capacitors and resistors, power dissipation of the proposed encoder is increased to 1.989 mW in comparison with pre-layout simulation.

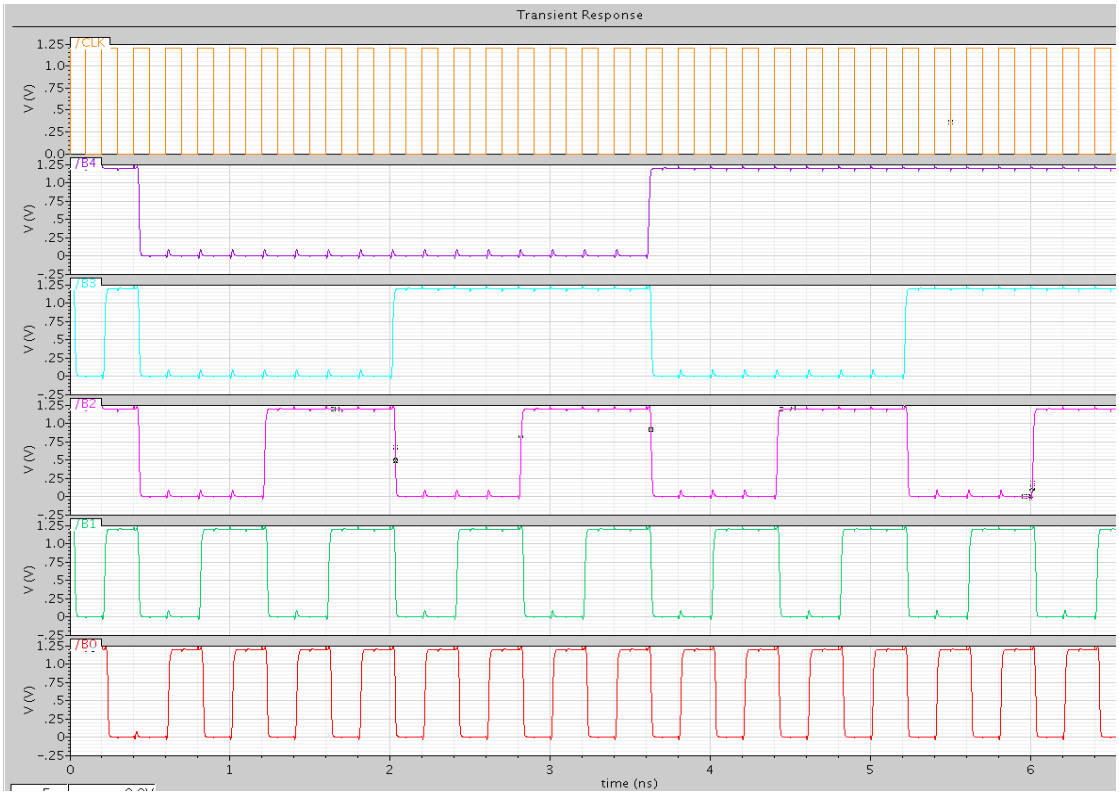


Fig. 4.36 Post layout simulation of the proposed encoder

4.2.13 Post layout corner simulation results of proposed encoder

Table 4.12 gives the post layout corner simulation results of proposed encoder.

Table 4.12 Post-layout simulation with process corner simulations

Corners	TT	SS	FF	SF	FS
Critical path delay (ns)	0.2	0.25	0.18	0.21	0.19
Maximum frequency of operation (GHz)	5	4	5.55	4.76	5.25
Power dissipation (mW)	1.989	1.612	2.943	1.924	2.409
Power delay product (pJ)	0.3978	0.403	0.52974	0.40404	0.45771

The corner "TT" is best suited for the application, since it is having the lowest power delay product among all other corners with a maximum speed of operation of 5 GHz.

4.2.14 Comparison with other encoders

A comparison has been made with other encoders and presented in Table 4.13.

Table 4.13 Comaparison with different encoders

Results	Current Mode Logic Encoder [60]	[71]	Proposed encoder
Architecture	Flash	Flash	Flash
Resolution	4 bits	4 bits	5 bits
Technology	180 nm	180 nm	90 nm
Sampling Frequency	5 GHz	2.5 GHz	5 GHz
V_{DD}	1.8 V	1.8 V	1.2 V
Current	2.22 mA	3.055 mA	1.6575 mA
Power Dissipation	4 mW	5.5 mW	1.989 mW

The result shows that the speed of the proposed design is comparable with other high speed designs with an added advantage of reducing the effect of bubble error. In comparison with other logic type encoders, the proposed encoder contains a reduced number of transistors, thereby reducing the cost of the encoder also.

4.3 Conclusion

The implementation of thermometer code to binary code conversion can be done in different ways. It comprises of ROM type encoder, wallace tree encoder, multiplexer based encoder, fat tree encoder and logic style encoder. Although ROM encoder approach is easy and straight forward to design, it is slow and consumes large power due to a constant static current that is present in the ROM encoder. Although speed of operation of fat tree encoder is greater than ROM encoder, the desired speed for the specific application is not achievable by the fat tree encoder.

In the case of Wallace tree encoder, the number of full adders used in the implementation increases with the increase of resolution. This raises the die area as well as power dissipation

of the total implementation. A modified wallace tree encoder is proposed for a 3 GS/s five bit flash analog-to-digital converter. With the purpose of medium speed and low power dissipation, dynamic logic is used for the design of the first stage. To make the code more resilient to bubble errors, the last stage is designed in wallace tree fashion with the help of four full adders. The reconfigurable capability of the proposed encoder builds this encoder design flexible to reconfigurable flash ADC architecture. The encoder can be operated at frequency of 3 GS/s with a power dissipation of 2.424 mW for 1.2 V.

Multiplexer based encoder requires less hardware and has a shorter critical path than ones counter (Wallace tree) encoder. A modified low power multiplexer based encoder anticipated for a 4.44 GS/s five bit flash analog-to-digital converter is proposed. The maximum frequency of operation that can be attained with the help of this encoder is 4.44 GHz with a power dissipation of 1.624 mW. A high speed reconfigurable encoder for five bit flash ADCs is also proposed in the next stage for a 5 GS/s five bit flash analog-to-digital converter. The simulation result shows that the encoder can be operated at frequency of 5 GS/s with a power dissipation of 2.132 mW. A high speed low power multiplexer based encoder used for 5 GS/s five bit flash ADC with a power dissipation of 1.969 mW from 1.2 V is also designed and verified in the chapter.

Static CMOS, Dynamic, Pseudo NMOS and Pseudo Dynamic CMOS are the different logic styles used to implement thermometer code to binary code conversion. Direct conversion method is utilized without any intermediate stage in this design. Due to the property of less sensitivity towards the noise, static CMOS implementation is generally desired in the noisy environment. The number of transistor usage in the implementation increases largely as the circuit becomes large, that enlarges the power dissipation. The maximum frequency of operation achieved with the help of static CMOS implementation of the conversion is 1 GHz. To improve the speed, dynamic logic implementation is employed. With the use of this implementation, maximum of 4 GHz operation is attained. To further improve speed as well as to decrease transistor count, pseudo NMOS logic implementation is utilized. By using pseudo NMOS logic, maximum of 5 GHz operation is obtained with a very high value of power dissipation. To trim down the power dissipation by keeping frequency of operation identical, pseudo dynamic CMOS logic implementation is used. Smaller critical path delay, low transistor count and medium values of power dissipation and power delay product makes pseudo dynamic CMOS logic implementation a favorable choice over other logic style implementation for high speed flash ADC design.

In the last portion, a high speed bubble tolerant encoder for a 5 GS/s five bit flash ADC is designed and verified. One of the widely used methods is to reduce the effect of bubbles in thermometer code is to convert the thermometer code to gray code. This encoder circuit converts the thermometer code into the intermediate gray code to diminish the effects of bubble errors. XOR gate is used to convert gray code to binary code. Layout of the encoder is drawn and post layout simulation is also done and verified with simulation results. Layout of the encoder occupies an active area of 96.5 µm × 58.25 µm. With the help of proposed encoder, maximum sampling frequency of 5 GS/s can be achieved with a power dissipation of 1.989 mW from 1.2 V with a power delay product of 0.3978 pJ. Out of all the encoders, high speed bubble tolerant encoder is chosen for the specific application of designing of flash ADC due to bubble tolerance, medium power dissipation, medium power delay product and high speed of operation. With the use of high speed bubble tolerant encoder and high speed comparator proposed in the previous chapter, flash ADC is designed which is explained in the next chapter.

CHAPTER 5

FLASH ADC IMPLEMENTATION

5.1 Introduction

The previous chapters describe about pseudo dynamic based high speed comparator and bubble tolerant pseudo dynamic logic based high speed encoder for a five bit flash ADC. The flash ADC comprises mainly three blocks such as resistor ladder, comparators and thermometer to binary code converter [90]. In this chapter, a five bit flash ADC is designed using combining the above mentioned blocks and we describe about its various static and dynamic characteristics. We discuss about the different blocks of ADC in the next sectioin.

5.2 Resistor ladder

The resistor ladder is designed mainly to provide a stable reference voltage to the comparators. The resistor ladder network is formed by 2^N resistors which generates the reference voltage. The reference voltage for all comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. The ladder divides main reference voltage into 2^N equally spaced voltages as shown in Fig. 5.1. In the proposed five bit flash ADC implementation, V_{REF1}= 1.2 V and V_{REF2} = 0.3 V.

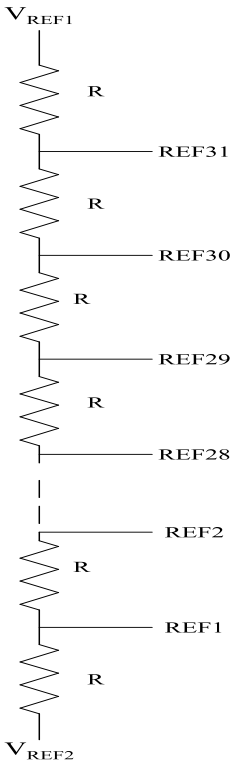


Fig. 5. 1 Resistor ladder

Table 5.1 shows the reference voltage at each node for a five bit flash ADC.

Table 5.1 Reference voltage generated by resistor ladder

Node	Reference Voltage
REF1	0.328125 V
REF2	0.35625 V
REF3	0.384375 V
REF4	0.4125 V
REF5	0.440625 V
REF6	0.46875 V
REF7	0.496875
REF8	0.525 V
REF9	0.553125 V
REF10	0.58125 V
REF11	0.609375 V
REF12	0.6375 V
REF13	0.665625 V
REF14	0.69375 V
REF15	0.721875 V
REF16	0.75 V
REF17	0.778125 V
REF18	0.80625 V
REF19	0.834375 V
REF20	0.8625 V
REF21	0.890625 V
REF22	0.91875 V
REF23	0.946875 V
REF24	0.975 V
REF25	1.003125 V
REF26	1.03125 V
REF27	1.059375 V
REF28	1.0875 V
REF29	1.115625 V
REF30	1.14375 V
REF31	1.171875 V

One of the major problems associated with resistor ladder is the signal feed through of the input signal to the resistor ladder [91]. The Fig. 5.2 shows the input feed through effect from the resistor ladder to the comparator. The parasitic capacitances are present between the

source and gate of the comparator inputs. The gate source capacitance couples the reference voltage (V_{REF}) into input voltage (V_{IN}). The gate source capacitance (C_{GS}) contributes a large amount to the total capacitance (C_{REF}) which is present between input signal and reference signal. This causes a deviation in the reference voltage generated by the resistor ladder. The voltage variation is large if the resistance values are high. At the same time, the feed through effect can be minimized by designing the resistor ladder to get a high bias current to overcome the harmonics at the output which results in a stable voltage along the resistor ladder. This results in the low value of the resistance in the resistor ladder that increases the power dissipation in the ADC design. So an optimum value of the resistance is chosen by considering the above circumstances.

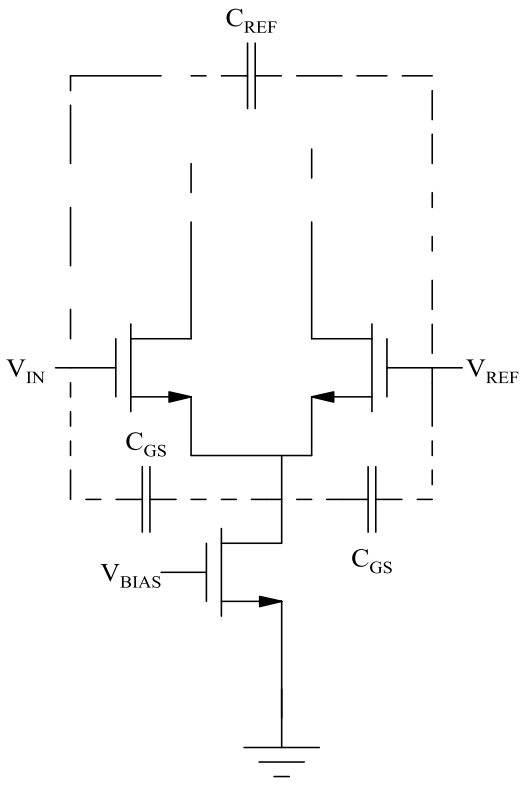


Fig. 5.2 Input feed through effect in the comparator

Fig. 5.3 shows the small signal model of input feed through effect of the reference ladder which is used to find out the optimum value of the resistance. Resistance value is calculated using the formula

$$R_{ladder,\max} = \frac{2}{\pi 2^N f_{in} C_{in,total}} \tag{5.1}$$

By taking the following values, N= 5, $C_{in,total}$ = 90 fF (assumption) and f_{in} = 546.875 MHz

$R_{ladder,max}$ = 400 Ω (12.5 Ω each)

Since the value of the resistance is very small, total power consumed by the resistor ladder is very high that effectively increases the total power consumption of the ADC.

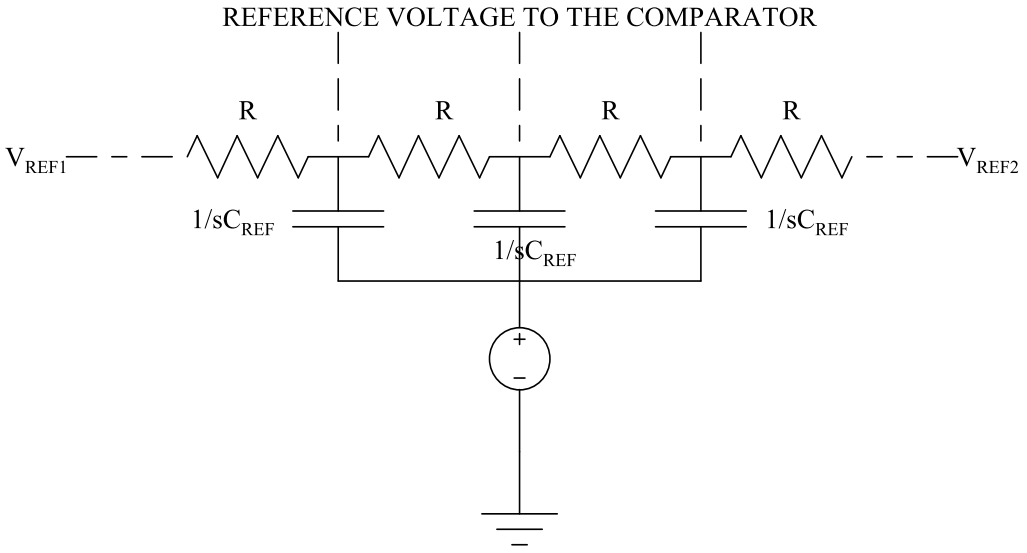


Fig. 5.3 Small signal model of the input feed through effect of resistor ladder

In order to overcome the power problem, a series of dynamic capacitors are introduced to decouple the resistor ladder (Fig. 5.4). The transistor's functioning as dynamic capacitors is used to divide the resistor ladder into eight decoupled sections (decoupling number is four, since after every four resistors, the dynamic capacitor is added). The W/L ratio of the transistor is chosen in such a way that the feed through effect is reduced.

With the help of de-coupling, $R_{ladder,max}$ can be recalculated as

$$R_{ladder,\max} = \frac{2}{\pi \eta_D f_{in} C_{in,total}}, \text{ where } \eta_D = \text{decoupling number} = 4 \qquad (5.2)$$

= 3200 Ω (100 Ω each)

This reduces the power consumption of the resistor ladder by a large extent thereby reducing the total power dissipation of ADC. The power dissipation due to resistor ladder is 2.6 mW.

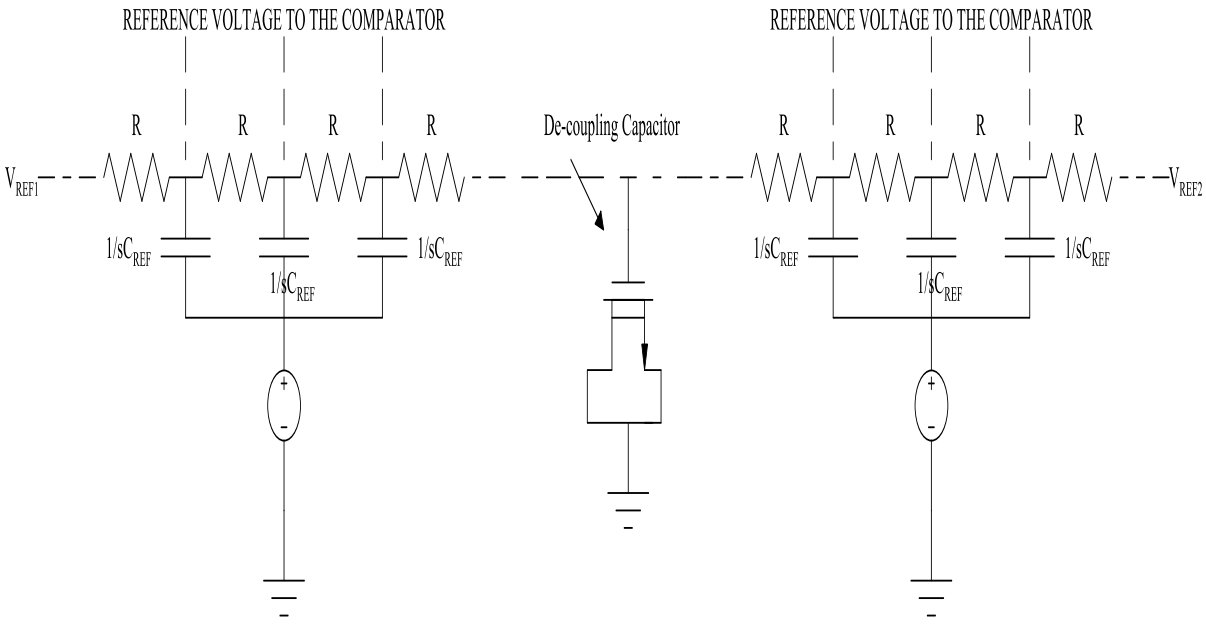


Fig. 5.4 De-coupling the resistor ladder

5.3 Comparator

The comparator compares the input signal with the reference voltages generated by the resistor ladder. The high speed preamplifier based pseudo dynamic latch comparator which is designed in the chapter 3 is used in the five bit flash ADC implementation. The comparator works at a frequency of 8 GHz with an offset voltage of 11.5 mV and a propagation delay of 156 ps. The comparator dissipates a 128.8 µW for a 1.2 V supply.

5.4 Encoder

High speed bubble tolerant encoder is chosen for the specific application of designing a five bit flash ADC due to bubble tolerance, medium power dissipation, medium power delay product and high speed of operation. With the assist of proposed encoder, maximum sampling frequency of 5 GS/s can be attained with a power dissipation of 1.989 mW from 1.2 V with a power delay product of 0.3978 pJ which is discussed in the previous chapter.

5.5 Flash ADC top level implementation

The three blocks (resistor ladder, 31 comparators and thermometer code to binary code converter) and integrated together to get the functionality of five bit flash ADC. The high speed five bit flash ADC is designed, simulated and verified in CADENCE design

environment using 90 nm CMOS technology with a power supply of 1.2 V. Fig. 5.5 shows the block diagram representation of five bit flash ADC.

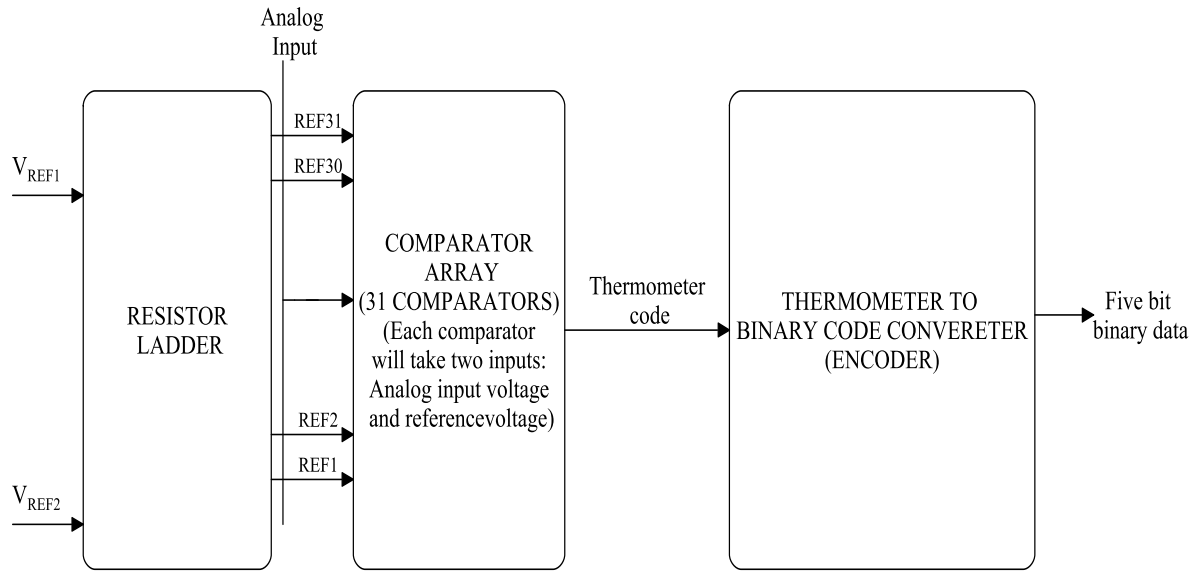


Fig. 5. 5 Block diagram representation of five bit flash ADC

5.6 Layout of ADC

The layout of the comparator and encoder are already drawn and verified using post layout simulation. These two blocks are taken into main layout of the five bit flash ADC to complete the design. The resistor ladder layout is drawn separately and added into the main layout window. All the ground pins are connected together by a wide metal trace using metal 1 layer [101]. In the similar way, all V_{DD} pins are also connected using metal 1 layer. The body of all NMOS transistors are connected to ground and body of all PMOS transistors are connected to V_{DD}. Speed and area are the primary concerns in the implementation of the digital circuit layout [103]. In contrast, while drawing layout of analog circuits, performance characteristics such as speed, power consumption, area and timing should be considered simultaneously. Without proper layout, the mismatches and the coupled noise would be sufficiently high which significantly humiliates the performance of the analog circuits. Moreover, a good shielding is needed to shield critical nodes in analog circuits from being disturbed. All the sub circuits of the ADC, including the different stages in the comparators and gates and latches in the encoder, are enclosed by substrate contact shield to diminish the effect of substrate noise. Approaches regarding minimization of noise are very critical and should be considered. Layout of the five bit flash ADC is shown in Fig. 5.6.

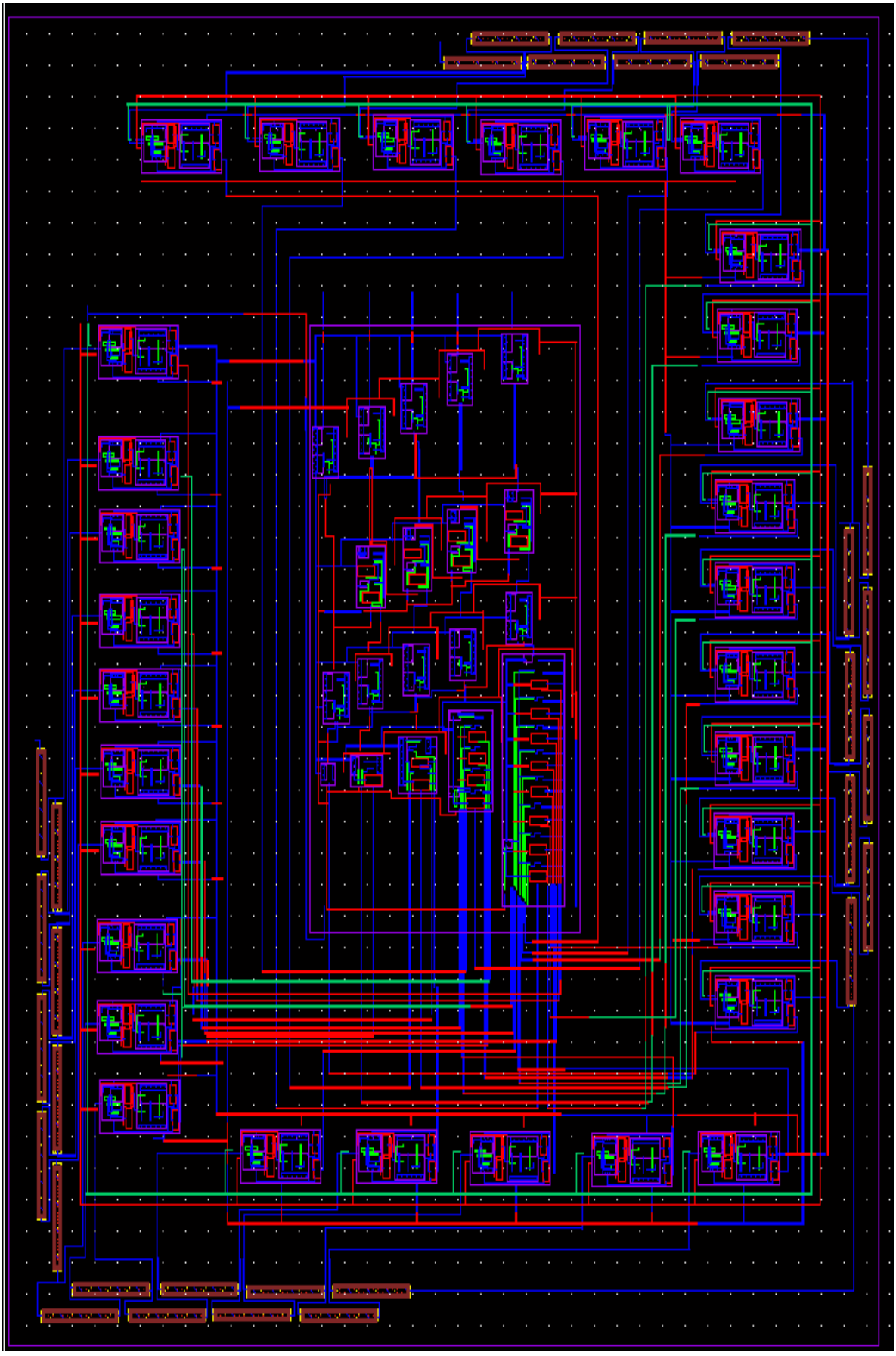


Fig. 5.6 Layout of complete five bit flash ADC.

5.7 Post layout simulation

After drawing layout of complete flash ADC, DRC, LVS and RCX are done. The av_extracted view of layout is available in the working folder. The post layout simulation is performed on the av_extracted view of the layout. Parasitic capacitances and resistors are added into the layout in the av_extracted view which is taken into consideration while performing post layout simulation. The input given is a ramp waveform which is having an initial voltage of 0.3 V and it reaches 1.2 V with a time of 6.4 ns. (Input range of proposed flash ADC is 0.3 V - 1.2 V). The post layout simulation results (Fig. 5.7) shows that proposed flash ADC is working fine for all the inputs in the range between 0.3 V and 1.2 V. Power dissipation of the complete flash ADC implementation is 8.381 mW from a supply of 1.2 V. The propagation delay of the proposed ADC is four clock pulses. A 5 GHz pulse is applied as a clock to the input of the ADC. So duration of the single clock pulse is 0.2 ns. Since the delay of four clock pulses is taken into consideration, the simulation result is coming from 0.8 ns to 7.2 ns.

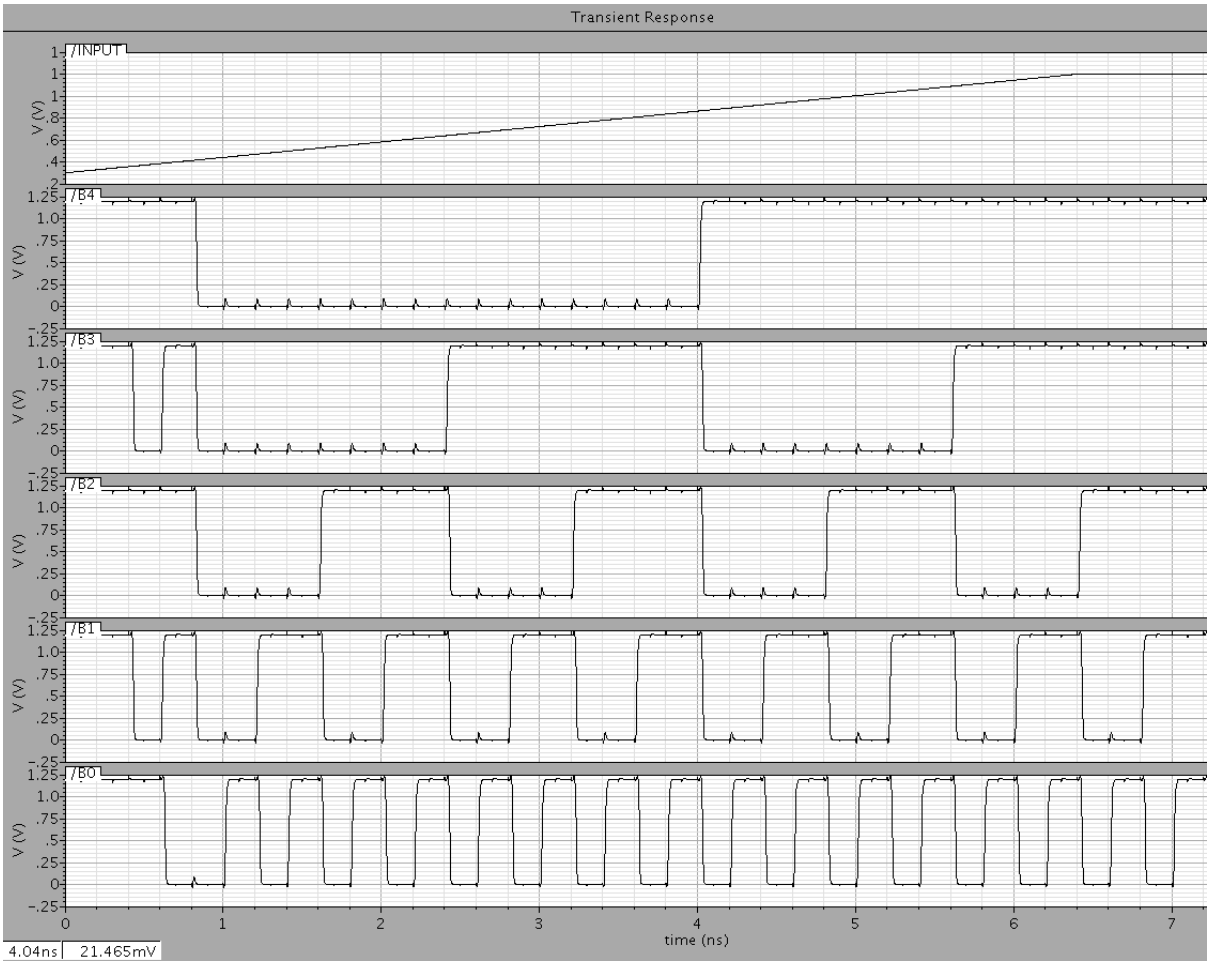


Fig. 5.7 Post layout simulation of proposed five bit flash ADC

5.8 Performance metrics of proposed flash ADC

5.8.1 DNL

The post layout simulation result shows that all the binary codes are present in the flash ADC implementation. A DNL error specification of less than or equal to 1LSB promises a monotonic transfer function with no missing codes [96]. Fig. 5.8 shows DNL plot of proposed ADC. Maximum value of DNL is measured as -0.6 LSB which is occurring for 00110 output code. It confirms that DNL is in the safe range.

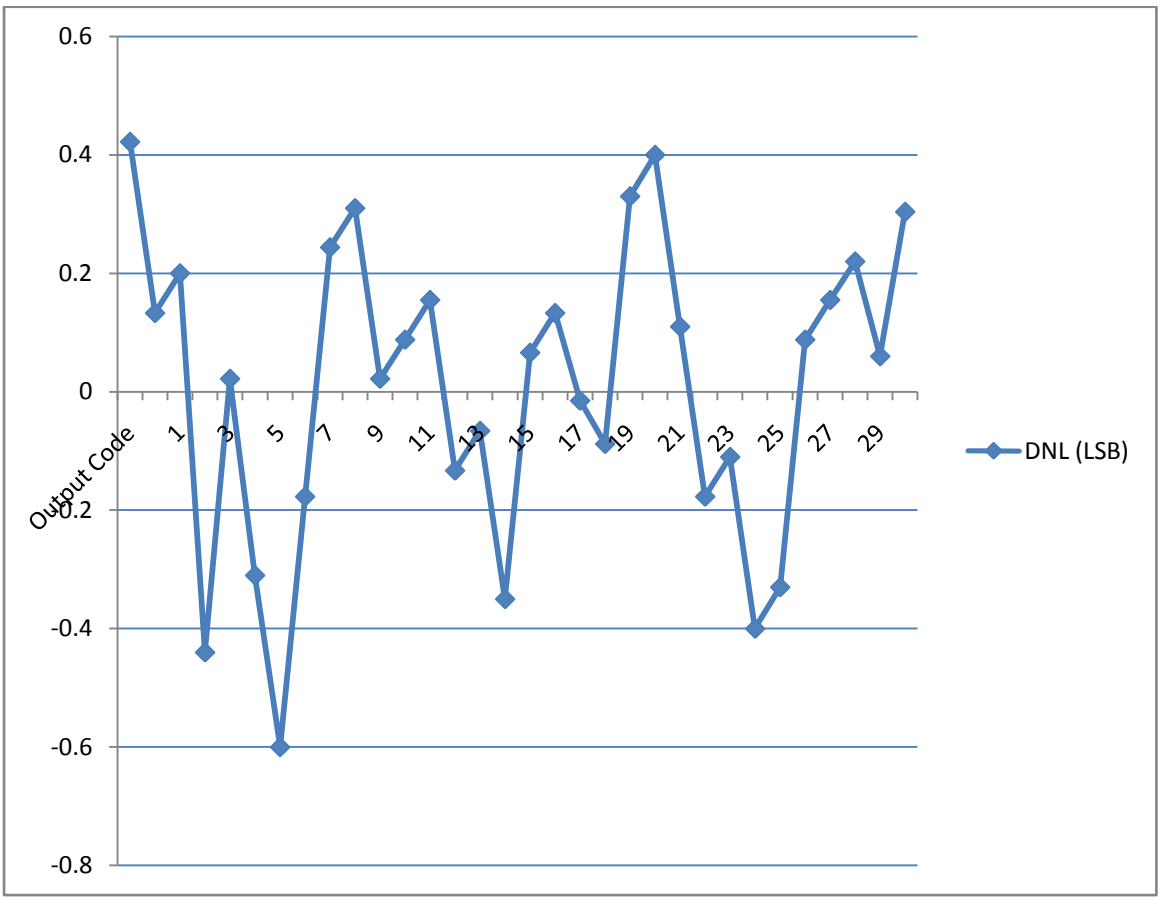


Fig. 5.8 DNL plot of proposed flash ADC

5.8.2 INL

INL is the sum of DNL up to that code [95]. In other words, it is the cumulative sum of DNL. There are different ways with which plotting of DNL and INL can be done. One of the widely used techniques is slow ramp test. A ramp signal provides as an input to the ADC. The time period of the ramp signal is equal to the product of the sampling time and the number of output binary levels. The simulation should run up to sum of the delay of the ADC and the time period of the ramp signal. From the output binary levels, DNL and INL are calculated for each binary output levels. INL plot of the proposed ADC is shown in Fig. 5.9.

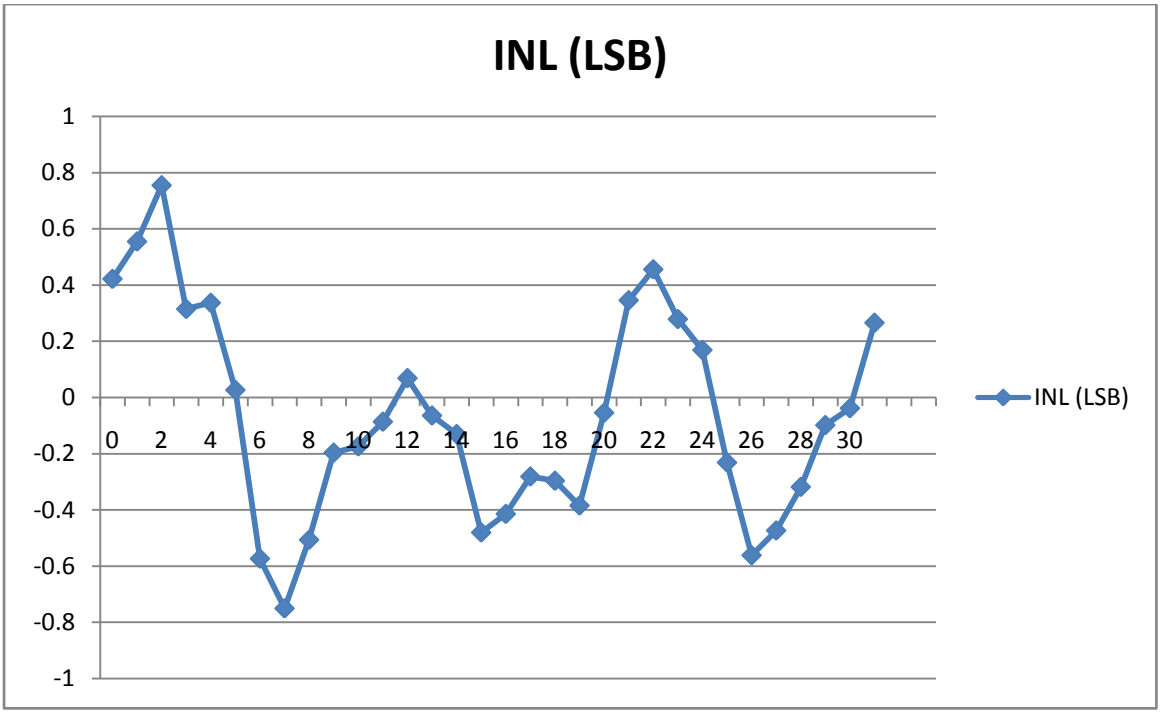


Fig. 5.9 INL plot of proposed flash ADC

5.8.3 Frequency spectrum

Distortion measurement (dynamic characteristics) is obtained by giving an input of sine wave to the system [93]. The frequency of the input sine wave is measured using equation

$f_{in} = \frac{Pf_s}{N}$, where P is an integer number which is a prime, f_s is the sampling frequency and N is the number of samples taken into consideration which is generally power of 2. (5.3)

In this analysis, f_s = 5 GHz, P = 7 and N = 64. So f_{in}= 546.875 MHz

The important thing which should be taken care is that there should not be any common factor between P and N. The processed waveform is converted into its spectrum using fast fourier transform and all the calculations are done from the frequency components. The simulation is performed for different sampling frequencies such as 1.2 GHz, 2 GHz, 3 GHz, 4 GHz and 5 GHz and input signal frequencies used in the simulation are 546.875 MHz, 859.375 MHz, 1.025625 GHz and 2.265625 GHz (Input frequencies are taken by giving P = 7, 11, 13, 29 by keeping sampling frequency as 5 GHz). SFDR, SNDR, ENOB and figure of merit are the main parameters which are derived from the frequency spectrum. The frequency spectrum of the proposed ADC is shown in Fig. 5.10. SFDR is measured to be 38.42 dB at 5 GHz operation.

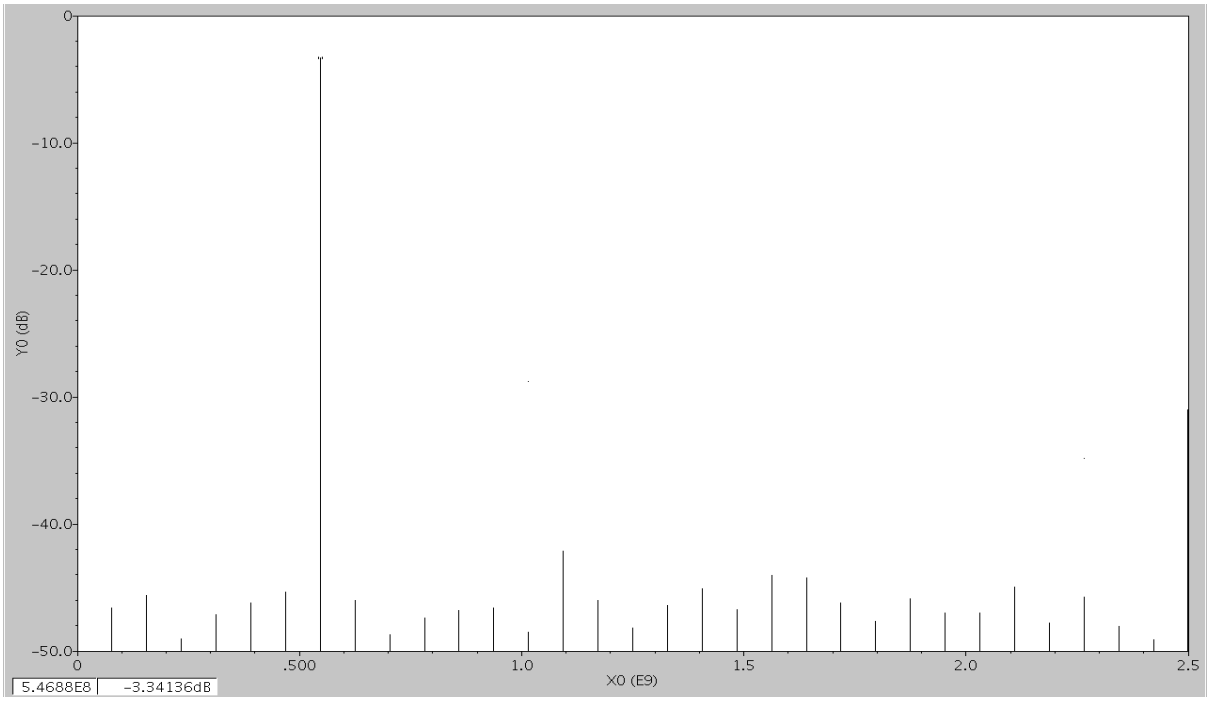


Fig. 5.10 Frequency spectrum of proposed ADC

5.8.4 SNDR

SNDR of the proposed ADC is measured to be 28.42 dB. The distortion components are also taken into consideration along with the noise while calculating SNDR [97]. From the value of SNDR, effective number of bits (ENOB) of flash ADC is measured.

5.8.5 ENOB

ENOB represents minimum permissible resolution of an ADC, for a specific value of SNDR.

ENOB = (SNDR-1.76)/6.02

= 4.43 @ 5 GHz

5.8.6 Figure of merit (FoM)

$FoM = \frac{Power}{2^{ENOB} \times 2 \times f_{in}}$, power dissipation at 5 GHz is 8.381 mW, ENOB = 4.43 and fin = 546.875 MHz

FoM = 0.3554 pJ/conv

5.9 Corner analysis of proposed flash ADC

Corner analysis for high speed five bit flash ADC is carried out and the results are shown in Table 5.2. The corner specification is same as that of the comparator design, since we are using same 90 nm technology. Out of all the corner results, TT is selected in our design.

Table 5.2 Corner analysis of the proposed flash ADC

Corners	TT	SS	FF	SF	FS
Input Voltage Range (V)	0.3-1.2	0.2-1.1	0.38-1.3	0.28-1.18	0.2-1.12
SFDR (dB)	38.42	34.85	35.23	36.12	37.43
SNDR (dB)	28.42	25.96	26.62	25.66	28.00
ENOB (Bits)	4.43	4.02	4.13	3.97	4.36
Power dissipation (mW)	8.381	7.629	9.613	7.935	9.187

5.10 Characteristic curves of proposed flash ADC

5.10.1 Power dissipation Vs Sampling frequency

As the sampling frequency increases for a specific ADC, the power dissipation is also increases [92]. The performance of the flash ADC also degrades with the increase in sampling frequency. Fig. 5.11 shows the curve between sampling frequency and power dissipation. In all these sampling frequency of operations, the input signal frequency is kept as 546.875 MHz

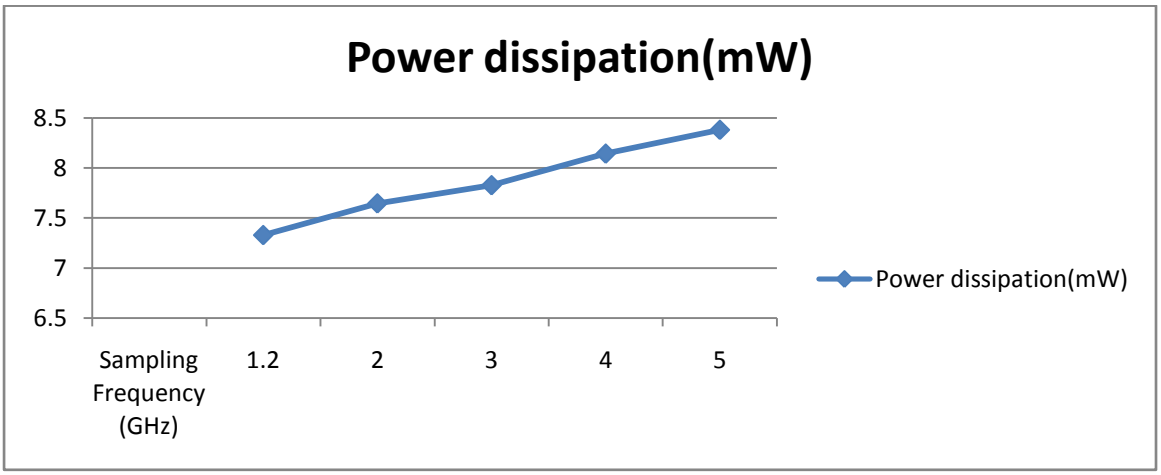


Fig. 5.11 Curve between power dissipation and sampling frequency

5.10.2 ENOB Vs Sampling Frequency

At 1.2 GHz of frequency of operation, ENOB of flash ADC is 4.76. As the frequency increases, ENOB of ADC decreases and it reaches a value of 4.43 when the sampling frequency reaches 5 GHz. Fig. 5.12 shows the curve between ENOB and sampling frequency.

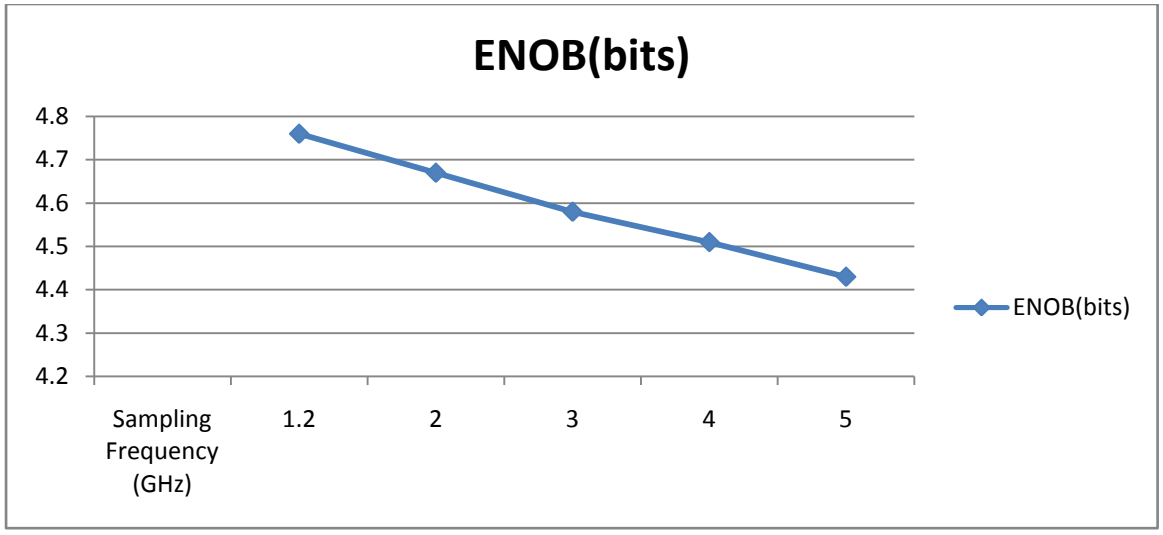


Fig. 5.12 Curve between ENOB and Sampling frequency

5.10.3 ENOB Vs input signal frequency

As the input signal frequency increases, ENOB of ADC drops. It is mainly due to limited bandwidth of ADC. As the input frequency increases, the input signal is attenuated at different stages of ADC. So there is a chance of missing code in the ADC. Moreover as the frequency increases, internal sub-block performance is also degraded. Fig. 5.13 shows the curve between ENOB and input signal frequency. In this analysis, the sampling frequency is fixed as 5 GHz.

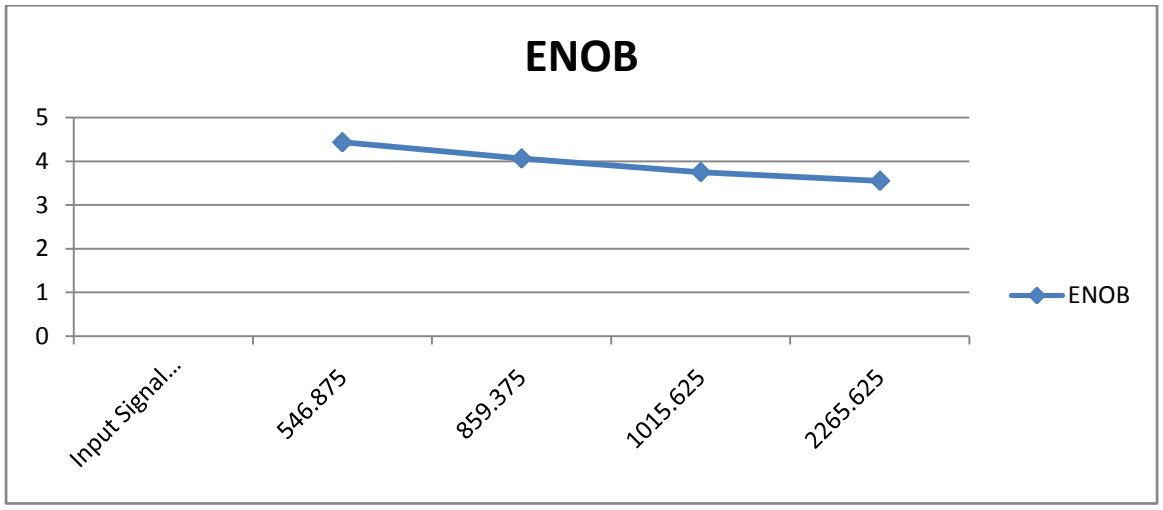


Fig. 5.13 Curve between ENOB and input signal frequency

5.10.4 SFDR Vs clock frequency and SFDR Vs input signal frequency

SFDR value also decreases as the clock frequency increases [93]. Probability of occurring largest spur increases as the clock frequency increases which reduces the SFDR value. In this analysis, the input signal frequency is fixed to 546.875 MHz. Fig. 5.14 shows the curve between SFDR and clock frequency. In the similar way, by keeping sampling frequency as a fixed one and increasing input signal frequency also results in reduced SFDR. In this analysis, the clock frequency is set as 5 GHz. Fig. 5.15 shows the curve between SFDR and input signal frequency.

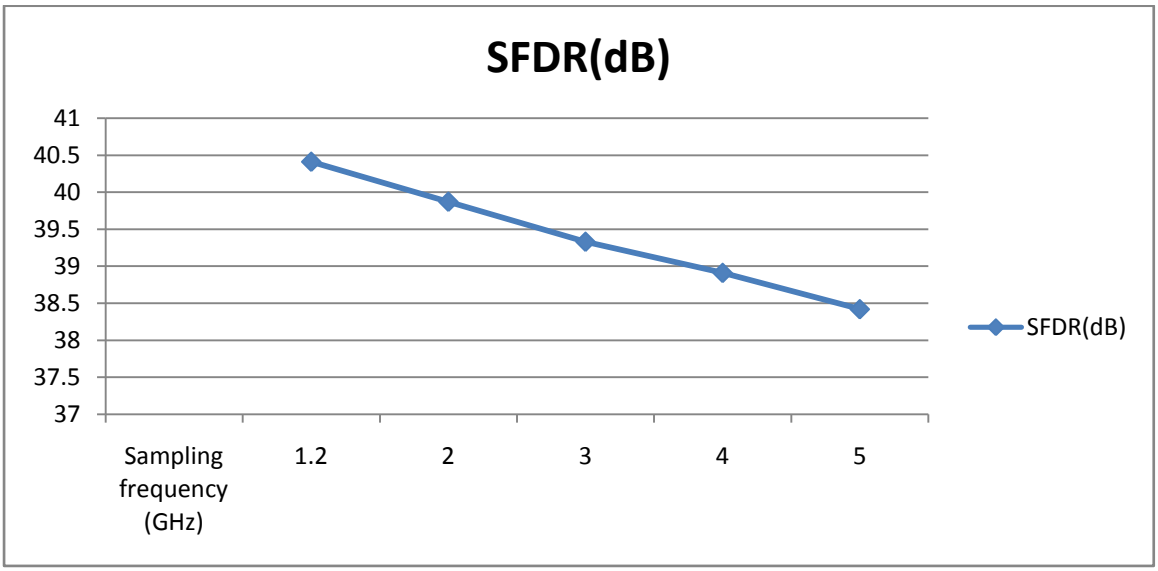


Fig. 5.14 Curve between SFDR and sampling (clock) frequency

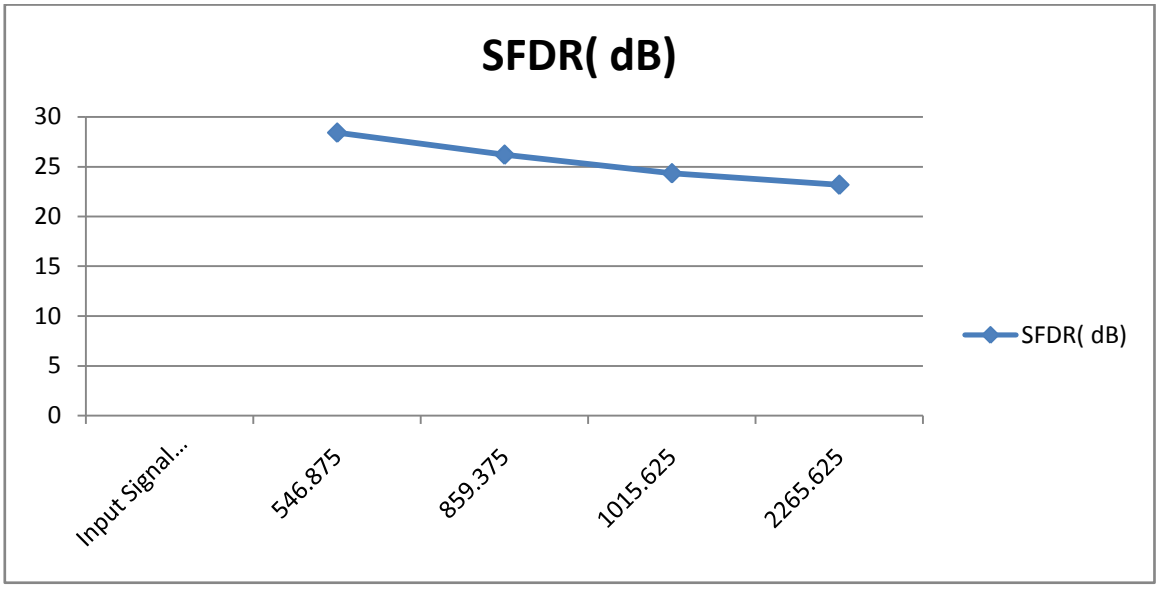


Fig. 5.15 Curve between SFDR and input signal frequency

5.11 Summary of the performance of the proposed five bit flash ADC

Table 5.3 Summary of the performance of the proposed flash ADC

Parameter	Flash ADC
Input signal range (V)	0.3 - 1.2 (0.9)
Input frequency of operation (MHz)	546.875
Resolution (bits)	5
Supply voltage (V)	1.2
Sampling frequency (GHz)	5
Maximum DNL (LSB)	-0.6
Maximum INL (LSB)	0.755
SFDR (dB)	38.42
ENOB (bits)	4.43
Power consumption (mW)	8.381
Die area (mm^2)	0.039
Technology (nm)	CMOS 90
Supply voltage (V)	1.2

Table 5.3 summarizes the performance of the proposed flash ADC. The die area of the proposed flash ADC is 186 µm × 210 µm (0.039 mm^2). The design is verified using CADENCE tool with 90 nm CMOS technology with a supply voltage of 1.2 V.

5.12 Comparison with other works

Table 5.4 shows the comparison result of the proposed flash ADC with other similar works.

Table 5.4 Comparison with other works

	[88]	[85]	[87]	[86]	[89]	[62]	This work
Technology	CMOS 0.18 µm	CMOS 65nm	CMOS 65nm	CMOS 90nm	CMOS 130 nm	CMOS 90 nm	CMOS 90nm
Architecture	Time-domain Flash	Time-interleaved SAR	SAR + Flash	Inverter-based Flash	Flash ADC	Flash ADC	Flash ADC
Sampling Rate	500MS/s	250M, 500MS/s	800MS/s	300M, 600MS/s	1 GS/s	3.5 GS/s	5 GHz
Resolution (bits)	5	5	5	5	5	5	5
ENOB	4.13	4.10, 4.04	4.40	4.45, 4.08	4.73	4.28	4.43
Peak DNL/INL (LSB)	0.43/0.58	0.26/0.16	0.56/0.62	0.4/0.54, 0.31/0.87	---	----	-0.6/ 0.755
Supply Voltage (V)	1.8	1.2	1	0.8, 1	1.2	1.4	1.2
Power Consumption (mW)	8	1.8, 5.9	1.97	3.2 , 6.7	46	227	8.381
Area(mm^2)	0.132	0.91	0.018	0.11	0.20	0.66	0.039
FOM(pJ/conv)	0.91	0.44, 0.75	0.116	0.49, 0.66	1.8	5.84	0.3554

The proposed flash ADC is having highest sampling frequency of operation with a medium power dissipation of 8.381 mW. Area of implementation of proposed flash ADC is 0.039 mm^2 which is a good figure among the other ADC architectures. FOM of the proposed ADC is 0.3554 which is a very good value in comparison with other ADC architectures. Our target of SFDR and ENOB are >35 dB and > 4 respectively. Both the characteristics are achieved. Therefore the proposed flash ADC can be strongly recommended for DS-UWB applications

especially biomedical as well as in home wireless applications. The sampling frequency and accuracy of information is very important in these applications which can be achieved with the help of proposed five bit flash ADC.

5.13 Conclusion

The chapter describes the implementation of a high speed five bit flash ADC used for DS-UWB applications. The chapter starts with detailed design of the resistor ladder along with the issues that comes in during the design of the ADC. Since comparator and encoder are already discussed in detail in the previous chapters, integration of the three blocks (resistor ladder, 31 comparators and thermometer to binary code converter) is given more significance. Layout of the proposed ADC is drawn and post layout simulation is performed and verified with the results. The high speed flash ADC is designed and verified using CADENCE tool with CMOS 90 nm technology. The total power dissipation of the ADC is 8.381 mW from power supply of 1.2 V. The static and dynamic characteristics of proposed ADC are found out and different characteristic curves are also discussed in the last sections. Overall performance of the proposed ADC is displayed in the Table 5.2. Finally proposed work is compared with other similar works and conclusions are drawn. The next chapter discusses about working and implementation of a low power reconfigurable ADC architecture.

CHAPTER 6

DESIGN OF A RECONFIGURABLE FIVE BIT FLASH ADC AND ITS CHIP TAPE OUT

6.1 Introduction

In a reconfigurable ADC, output resolution of the ADC is not constant and it can be changed according to input data conditions [99]. In reconfigurable ADC, the output binary bits can work both as inputs as well as output. One of the binary bits is computed first and with the help of that binary bit, reaming binary bits are calculated.

One of the major disadvantages of flash ADC is the 2^N-1 comparators used in the design which plays a crucial role in deciding the total power consumption of the flash ADC implementation. This is largely reduced in the proposed reconfigurable flash ADC; since there is only 2^{N-2} + 2 comparators are used in the proposed design. Die area is minimised by a huge amount, since number of comparators used is very less. The complexity of the thermometer code to binary code conversion also plays a decisive role in the design of flash ADC. As compared to regular flash ADC, the complexity of the encoder in the proposed ADC is very less.

This chapter describes about a reconfigurable five bit flash ADC specially designed for DS-UWB applications. This chapter explains the functioning of a five bit reconfigurable flash ADC and its characteristics. Layout of the proposed reconfigurable flash ADC has been drawn and post layout simulation is performed. Once the functionality of layout is verified, final chip tape out has been made. The design target of the proposed reconfigurable ADC architecture is shown in Table 6.1.

Table 6.1 Design target of proposed ADC architecture

Communication standard used	DS-UWB
Input frequency range	500MHz- 2.5 GHz
Sampling frequency	1 GHz- 5GHz
Resolution	2 to 5 bits
Architecture of ADC	Reconfigurable Full flash ADC
Technology used	CMOS Technology 90/180 nm

6.2 Architecture of reconfigurable flash ADC.

It mainly consists of two blocks such as resistor ladder and a reconfigurable block. The resistor ladder block is designed in the same that was used in the earlier flash ADC design. Reconfigurable block consists of comparators, multiplexers and an encoder. Fig. 6.1 shows the representation of reconfigurable block. The input to the reconfigurable block is coming from the resistor ladder.

The working principle of proposed flash ADC is explained with an example. Let us assume that the input is greater than $22V_{REF}/32$ and less than $23\ V_{REF}/32$. So the first comparator compares the input with $16V_{REF}/32$ and gives an output bit of logic high. So B_4 is logic high (1). That logic high is given as the select line of the 2X1 multiplexer. The multiplexer takes two inputs ($8V_{REF}/32$, $24V_{REF}/32$). Since multiplexer select line is one, multiplexer picks the $24\ V_{REF}/32$ and compare with analog input and return a logic low value. Hence B_3 is logic low (0). The B_4 and B_3 are given as an input to the 4X1 multiplexer and B_2 is generated. In this, the comparator picks up $20V_{REF}/32$ and provides a logic high value to the output of multiplexer. Hence B_2 is logic high (1). In the next step B_4, B_3 and B_2 (101) are given as an input to the three 8X1 multiplexers and output is taken out. The output of the multiplexers provides a value of 011. This is given to the 3:2 encoder. The 3:2 encoder encodes the three bit binary data into 10 which is taken as B_1 and B_0. Hence the binary data is 10110 which is a correct value for an analog input which is in the range between $22V_{REF}/32$ and $23V_{REF}/32$. In the similar way, all the inputs are verified using the proposed reconfigurable block. The 3:2 encoder truth table is shown in Table 6.2 and output equations are shown in (6.1) and (6.2). The reconfigurable flash ADC operation is shown as a flow chart in appendix.

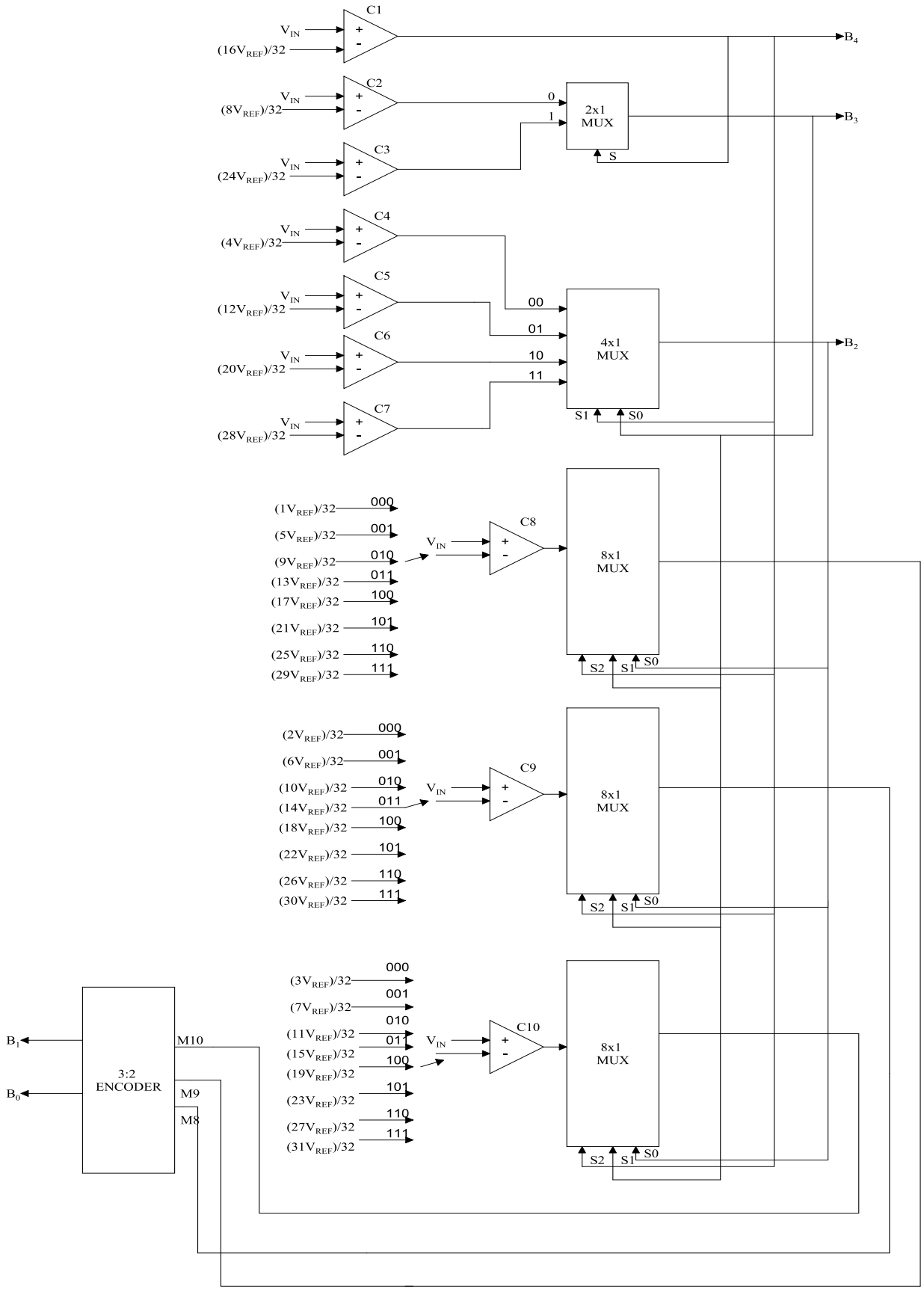


Fig. 6. 1 Reconfigurable block architecture

Table 6.2 3:2 Encoder truth table

M_{10}	M_9	M_8	B_1	B_0
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

$$B_1 = M_9 \tag{6.1}$$

$$B_0 = \overline{M_9} M_8 + M_{10} \tag{6.2}$$

6.3 Implementation of the reconfigurable block

The sub-blocks of the reconfigurable ADC are comparator, 2X1 multiplexer, 4X1 multiplexer and 8X1 multiplexer and a 3:2 encoder. Each block is designed separately and finally combination provides reconfigurable block.

6.3.1 Comparator

A high speed pseudo dynamic comparator is designed using CMOS 90 nm technology in the third chapter of the thesis. The maximum frequency of operation of the comparator is 8 GHz. The comparator is redesigned for 180 nm technology using the same equations which is used in the chapter 2. So the same comparator architecture is used in the reconfigurable flash ADC also.

6.3.2 2X1 multiplexer

There are different logic styles such as static CMOS, dynamic logic, pseudo NMOS and pseudo dynamic logic used for the implementation of 2X1 multiplexer. From chapter 4(Encoder implementation), the maximum frequency of operation can be achieved with the help of pseudo dynamic logic with medium power dissipation. In order to achieve the maximum frequency of operation, 2X1 multiplexer is designed using pseudo dynamic logic. Fig. 6.2 shows the implementation of 2X1 multiplexer using pseudo dynamic logic

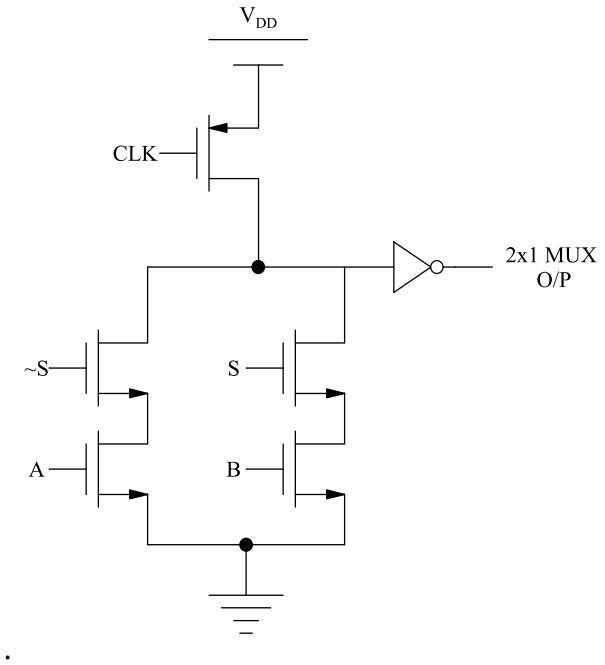


Fig. 6.2 Implementation of 2X1 multiplexer using pseudo dynamic logic

6.3.3 4X1 multiplexer

There are different ways with which the implementation of 4X1 multiplexer can be done. Directly using the Boolean expression, implementation can be done. But in this implementation, 4X1 multiplexer can be implemented using three 2X1 multiplexer. The block diagram of implementation is shown in Fig. 6.3.

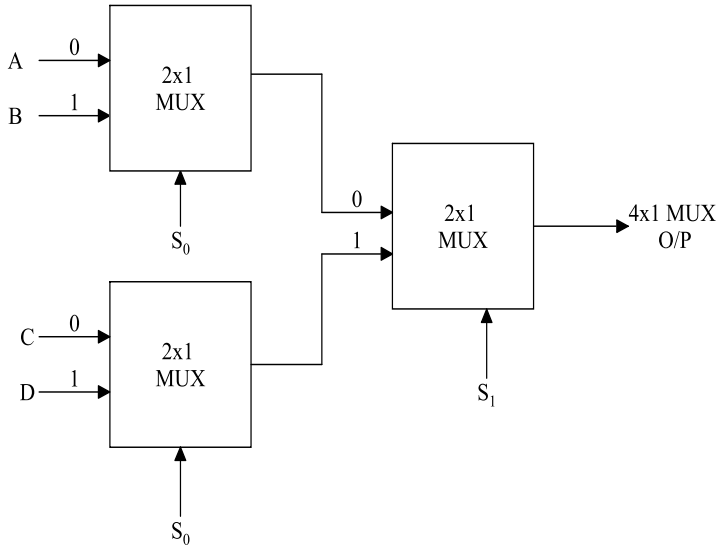


Fig. 6.3 4X1 multiplexer using 2X1 multiplexers

6.3.4 8X1 multiplexer

8X1 multiplexer is designed using 4X1 multiplexer and a 2X1 multiplexer (Fig.6.4).

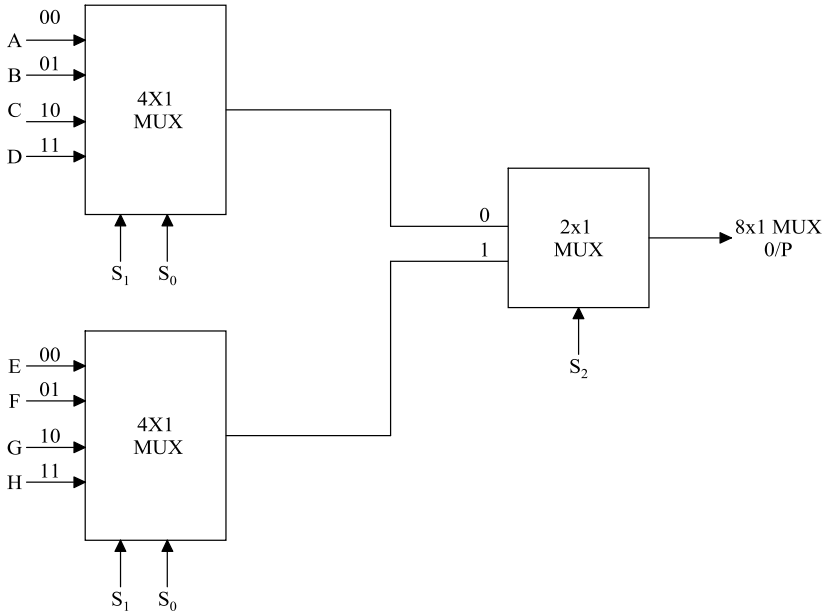


Fig. 6.4 8X1 multiplexer using 4X1 multiplexer and a 2X1 multiplexer

6.3.5 3:2 Encoder implementation

3:2 encoder equations are provided in (1) and (2). The implementation (Fig. 6.5 and Fig. 6.6) is done using pseudo dynamic logic.

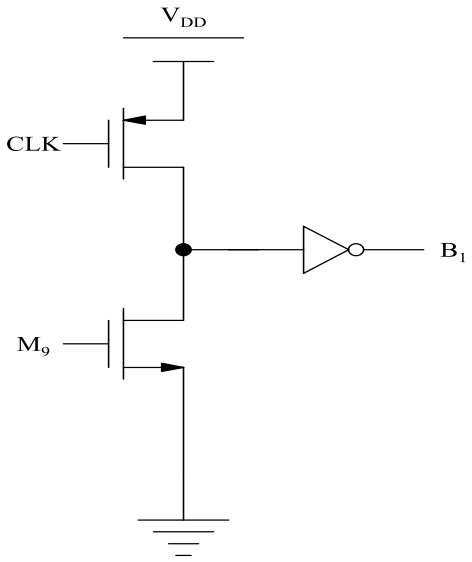


Fig. 6.5 Implementation of B_1 using pseudo dynamic logic

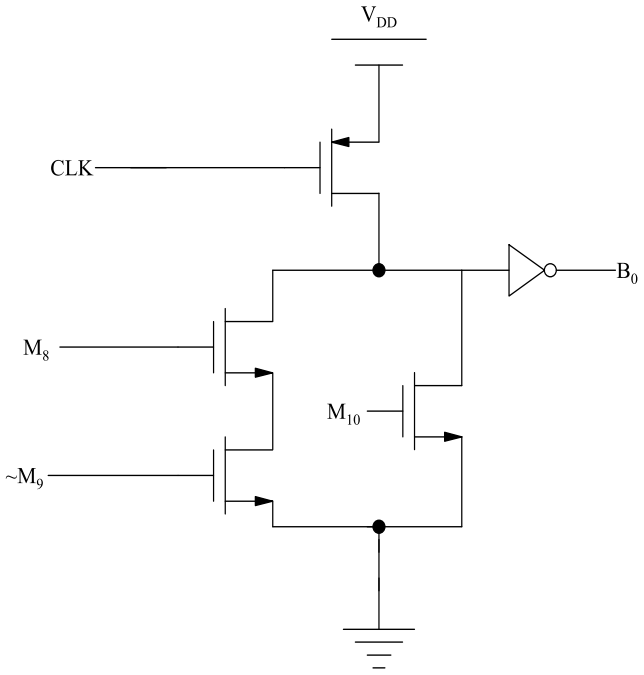


Fig. 6.6 Implementation of B_0 using pseudo dynamic logic

6.4 Clocking mechanism in the proposed flash ADC

Time shifted skewed mechanism is used in the clock design for the proposed flash ADC [99]. A very small duty cycle is used for triggering comparators in the reconfigurable ADC. The clock waveform used in the reconfigurable flash ADC is shown in Fig. 6.7.

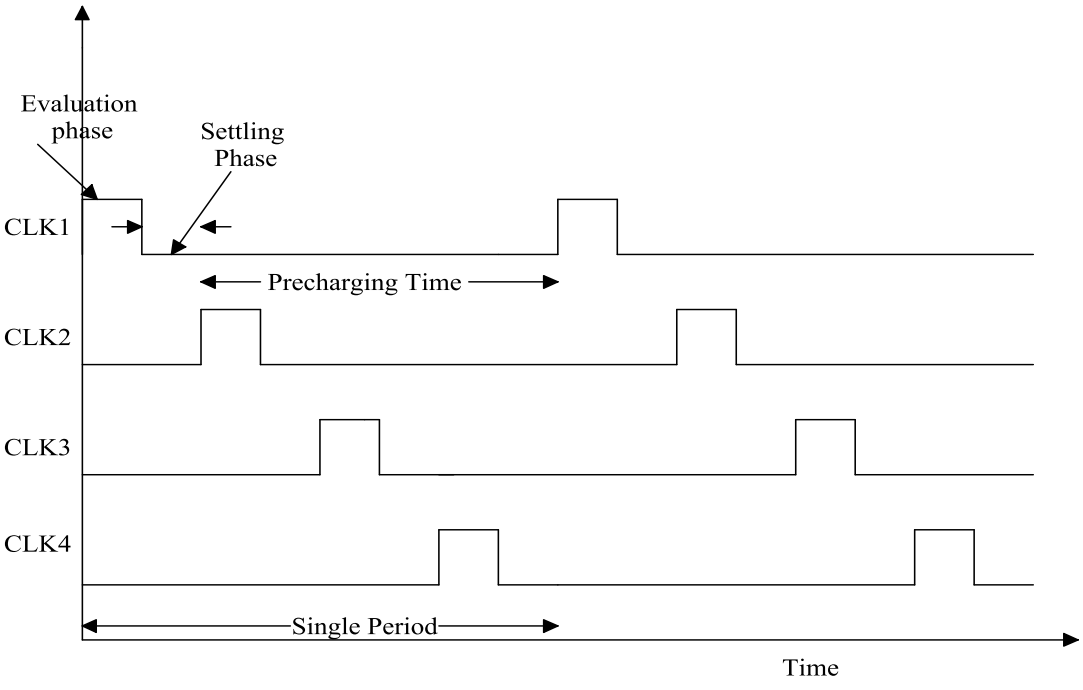


Fig. 6.7 Time shifted skewed clocking mechanism in Reconfigurable ADC

In Fig.6.7, there are total four different clocks. Different comparators in the design are triggered using different clocks. The total period of the clock is also shown in the Fig. 6.7. One evaluation phase and settling phase determines comparator maximum frequency of operation. Since the comparator is working well at 8 GHz frequency, the maximum clock frequency with which the reconfigurable ADC can be worked is 2 GHz (8/4, since there are four different clocks). CLK1 triggers comparator 1 only (C_1). CLK2 is used to trigger C_2, C_3 and 2X1 multiplexer. CLK3 is utilized for triggering C_4, C_5, C_6, C_7 and 4X1 multiplexer. CLK4 is employed for triggering three 8X1 multiplexers and a 3:2 encoder. So in one single clock cycle, entire operation is finished. The disadvantage of this skewed clocking mechanism is the reduction in the frequency of operation of ADC.

6.5 Layout of the implementation

Layout of the reconfigurable ADC has been drawn using virtuso of CADENCE tool and it is shown in Fig. 6.8. All NMOS transistors substrates are connected to ground and that of all PMOS transistors are connected to V_{DD} [101, 103].

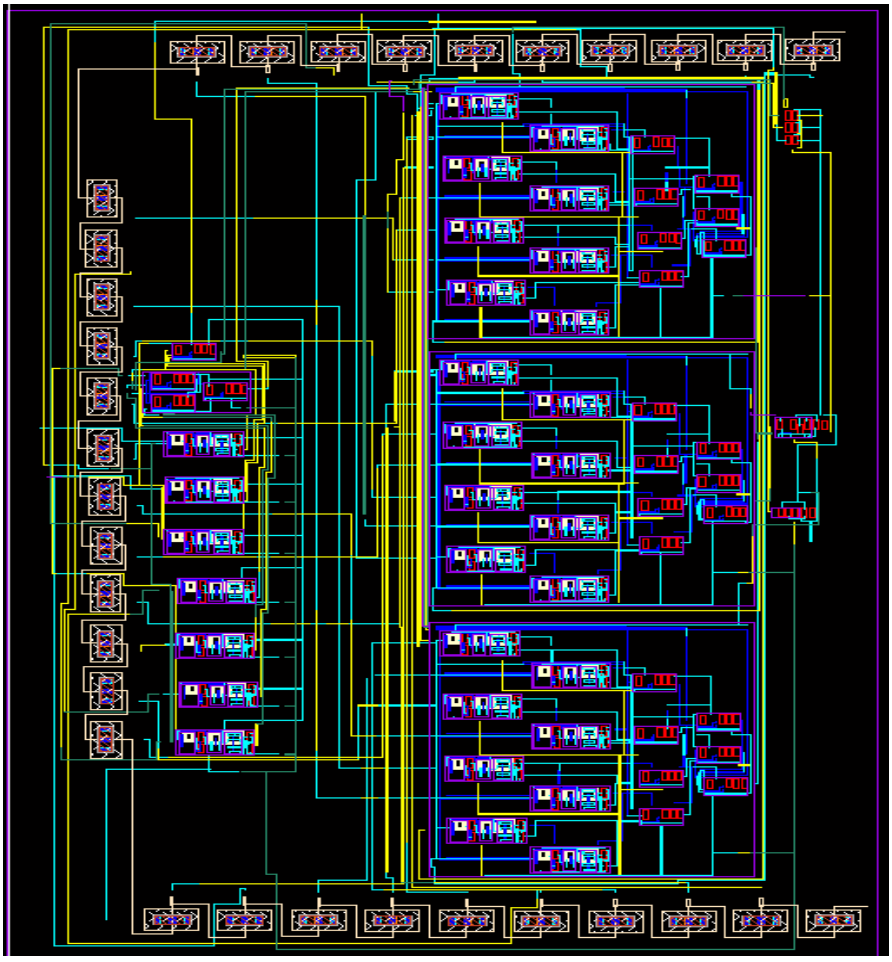


Fig. 6.8 Layout of the reconfigurable flash ADC

6.6 Post layout simulation

After completion of layout, the input and output pins which are present in schematic are added to layout along with V_{DD} and GND.

6.6.1 DRC check

DRC is used to check all process-specific design rules. There are process specific design rules which describe how closely the layers can be placed together. These rules provide the minimum requirement to avoid failure of circuit due to fabrication fault. If the layout is done perfectly then it shows no DRC error as in the following Fig. 6.9.

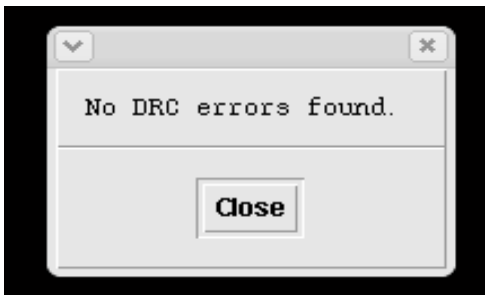


Fig. 6. 9 DRC error window

6.6.2 LVS Check

The comparison between layout and schematic is performed by LVS check. If all the connections and components in schematic and layout are matched properly, then this LVS run shows that the schematic and layout matched, as shown in following Fig. 6.10.

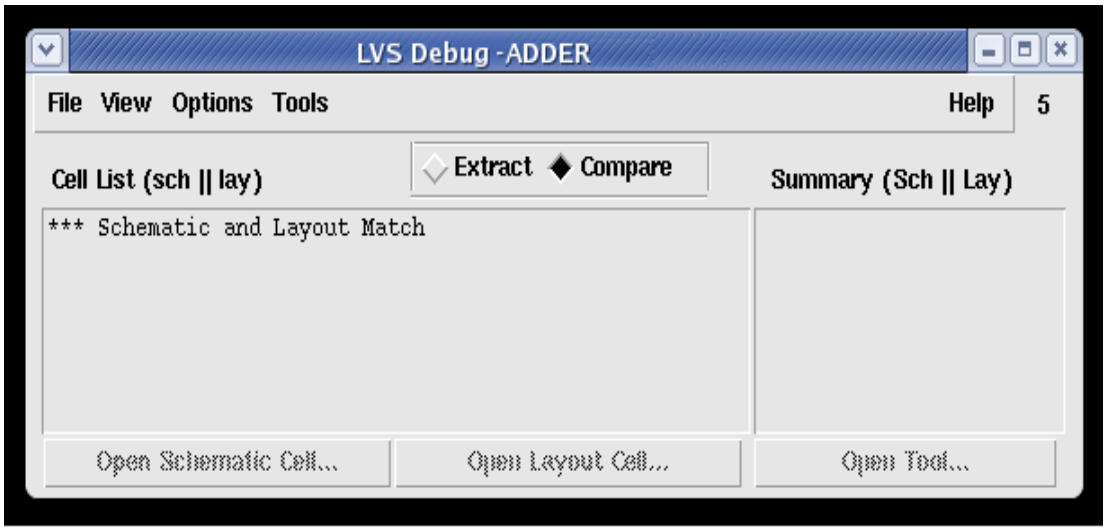


Fig. 6.10 LVS run window

6.6.3 RCX extraction

The parasitic resistance and capacitance of layout is extracted by performing RCX extraction. After RCX, a file called av_extracted is generated in the working directory. The post layout simulation is performing on av_extracted view of the layout which consists of parasitic capacitances and resistances. The input given is a ramp waveform based on the input range of flash ADC (Input range of proposed flash ADC is 0.5 V - 1.4 V). The post layout simulation results (Fig. 6.11) shows that proposed flash ADC is working fine for all the inputs in the range between 0.5 V and 1.4 V. Power dissipation of the complete flash ADC implementation is 11.71 mW from a supply of 1.8 V. The propagation delay of the proposed ADC is single clock pulse. But the duration of the single clock pulse is 0.5 ns.

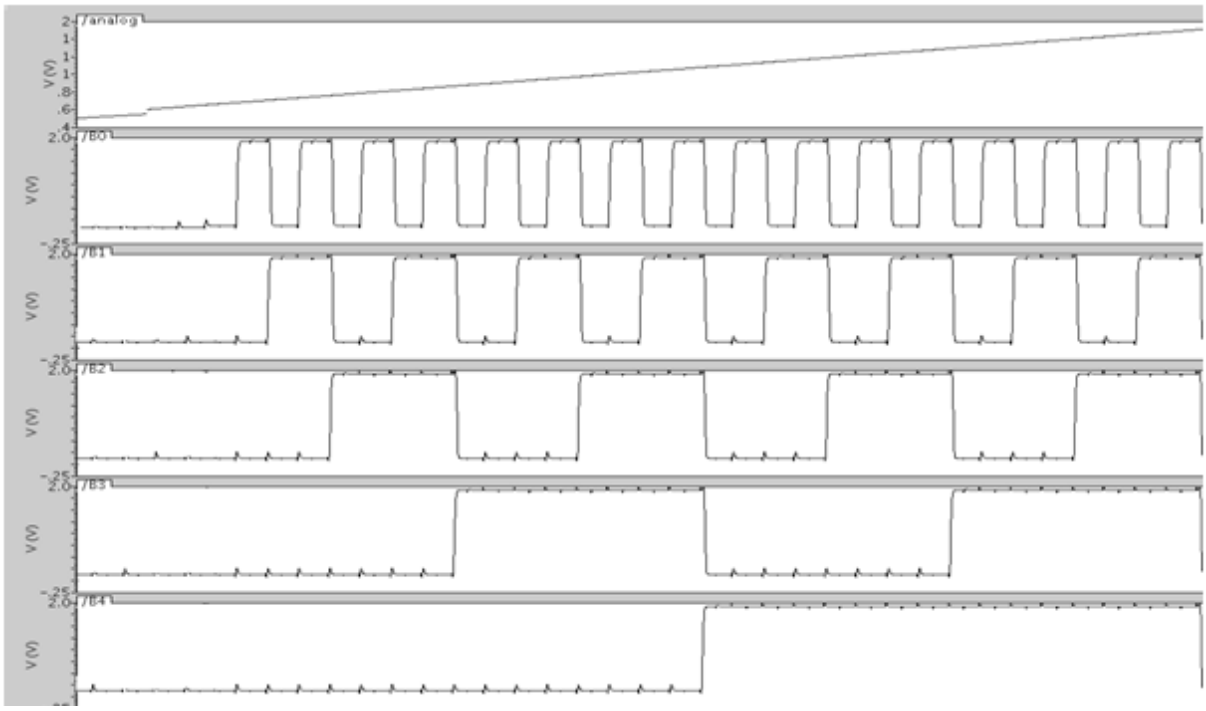


Fig. 6.11 Post layout simulation of reconfigurable flash ADC

6.7 Performance metrics of proposed reconfigurable ADC

6.7.1 DNL

Maximum value of DNL is measured as 0.355 LSB which is occurring for 01111 output code. All the binary output values are available in the output of the reconfigurable ADC which ensures the proper functioning of ADC. Fig. 6.12 shows the DNL curve of a reconfigurable flash ADC.

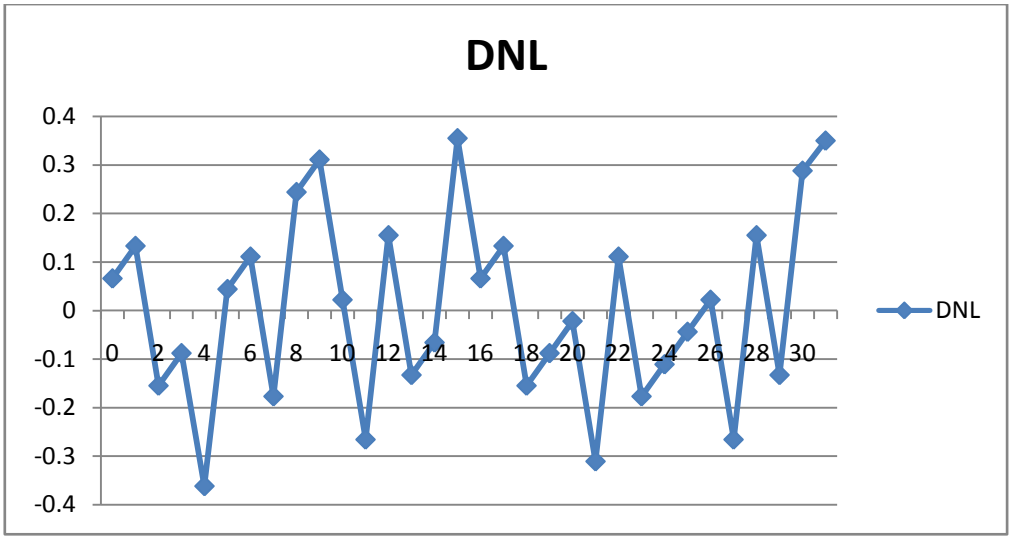


Fig. 6.12 DNL plot of reconfigurable ADC

6.7.2 INL

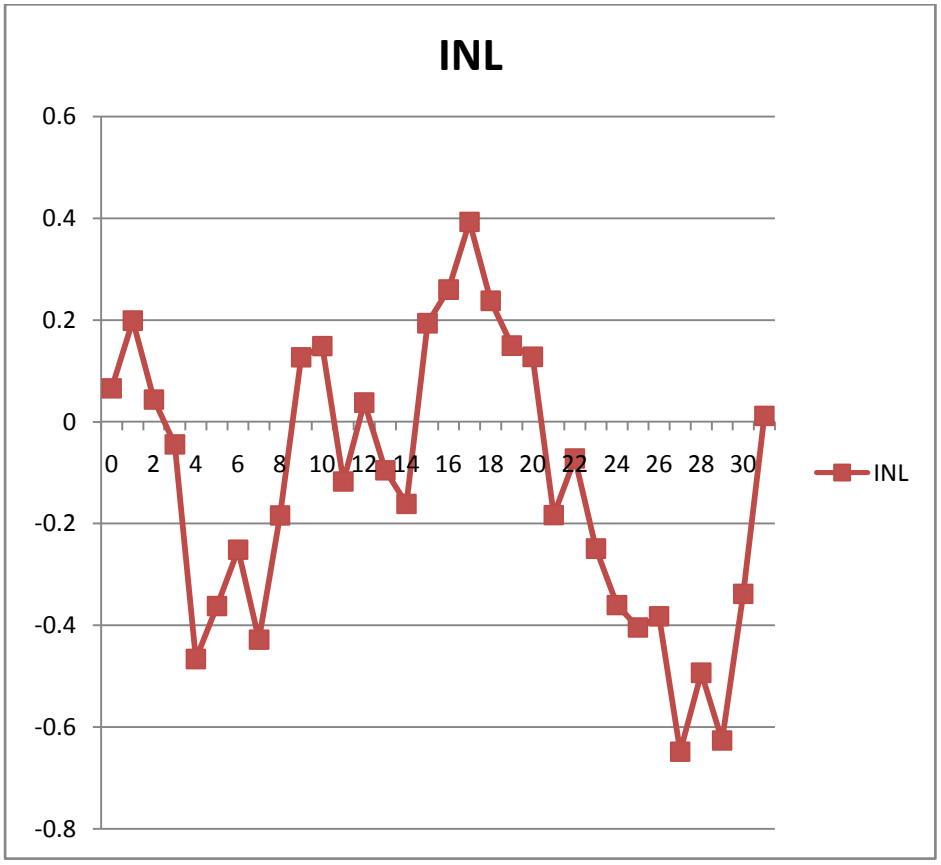


Fig. 6.13 INL plot of reconfigurable ADC

INL is the running sum of DNL up to that code [104]. Maximum value of INL is -0.648 LSB which is occurring for 11011 output code. The INL plot is shown in Fig. 6.13.

6.7.3 Frequency spectrum

The dynamic characteristics of an ADC is measured using frequency domain analysis or with the help of frequency spectrum. A sinusoidal signal is used for the analysis of the dynamic characteristics. The frequency of the input sine wave is measured using equation

$f_{in} = \frac{Pf_s}{N}$, where P = 29, f_s = 1.25 GHz and N = 64

So f_{in}= 566.40 MHz

The frequency spectrum is shown in Fig. 6.14. SFDR of the reconfigurable ADC at 1.25 GHz is measured to be 40.12 dB.

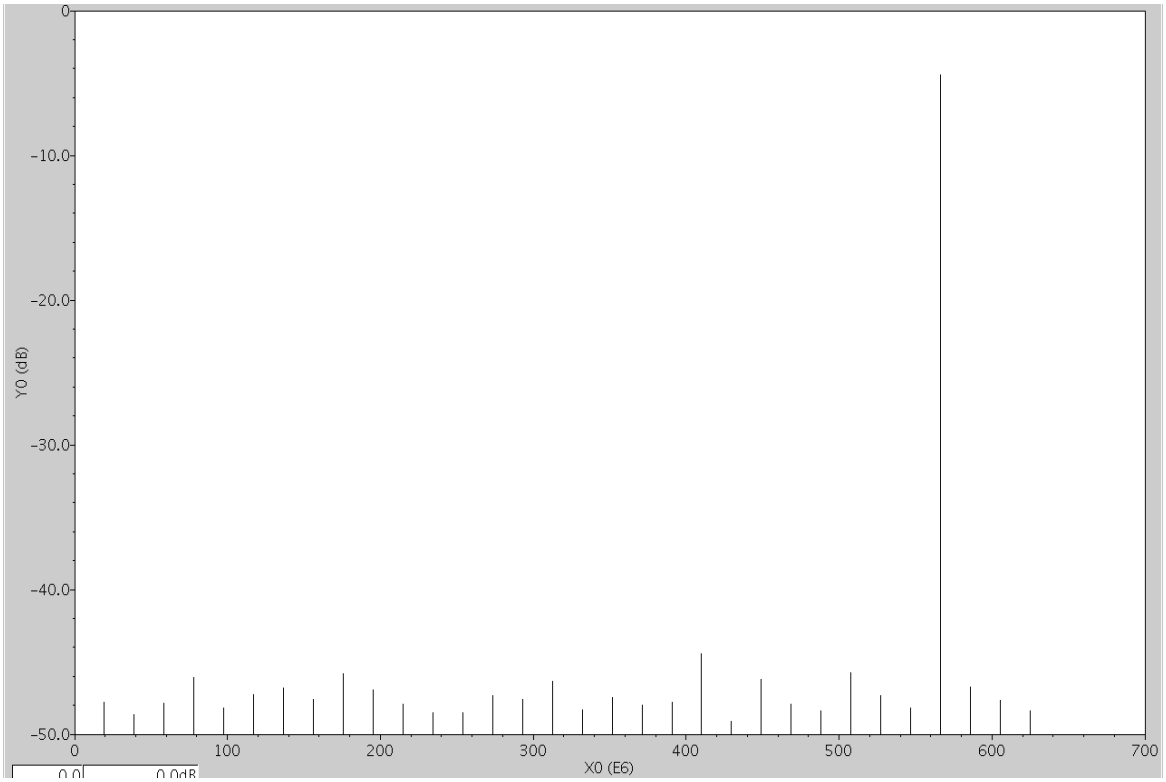


Fig. 6.14 Frequency spectrum of reconfigurable ADC

6.7.4 SNDR

From the frequency spectrum, SNDR is also calculated which is found out to be 30.53 dB. ENOB is determined from the value of SNDR.

6.7.5 ENOB

ENOB = (SNDR-1.76)/6.02

= 4.78

6.7.6 Figure of merit (FOM)

The main objective of FoM is to compare the performance of different ADCs. A low value of figure of merit indicates a high performance ADC.

$$FoM = \frac{Power}{2^{ENOB} \times 2 \times f_{in}}$$

= 0.376 pJ/conv

6.8 Corner analysis of the proposed reconfigurable flash ADC

Since reconfigurable flash ADC is designed in UMC 180 nm technology, different corner parameters should be used. The corner parameters are shown in Table 6.3.Corner analysis is shown in Table 6.4.

Table 6.3 Process corners of reconfigurable five bit flash ADC

Corners	V_{DD} (in Volts)	Temperature (in degree Celsius)
TT	1.80 V	27
SS	1.62 V	80
FF	1.98 V	-20
SF	1.80 V	27
FS	1.80 V	27

Table 6. 4 Corner analysis of the proposed reconfigurable flash ADC

Corners	TT	SS	FF	SF	FS
Input Voltage Range (V)	0.5-1.4	0.4-1.3	0.6-1.5	0.47-1.37	0.41-1.31
SFDR (dB)	40.12	38.34	39.12	38.37	39.27
SNDR (dB)	30.53	27.76	28.79	27.46	29.63
ENOB (Bits)	4.78	4.32	4.49	4.27	4.63
Power dissipation (mW)	11.71	10.64	13.73	11.15	12.47

In this corner analysis also, TT is selected in our design.

6.9 Reconfigurable operation

In regular flash ADCs, the output pins cannot be accessed as inputs. So the resolution (number of output bits) is a constant value in these ADCs. But in reconfigurable ADCs, the output pins can either act as an input or output pins. In order to work as a reconfigurable one, the flash ADC can be made to work at lower resolution. The operation of a reconfigurable ADC can be described using an example. The proposed ADC is a having a resolution of five bits. Assume that the input voltage is in the range of $13V_{REF}/32$ and $14V_{REF}/32$ and a resolution of four bits required. In order to implement a four bit ADC, first force MSB (B_4) of ADC to be logic zero and perform the remaining operation. Since B_4 is connected as a select line to the 2X1 multiplexer, the analog input is compared with $8V_{REF}/32$and produce logic high in B_3. B_4 and B_3 are sourced to 4X1 multiplexer and input signal is compared with $12V_{REF}/32$ and produce logic high again in B_2 ($B_4B_3B_2 = 011$). In the last stage, B_4, B_3 and B_2 are sourced to three 8X1 multiplexers simultaneously. These multiplexers compare the analog input with $13V_{REF}/32$, $14V_{REF}/32$ and $15V_{REF}/32$ respectively and produce output of 001 in $C_{10}C_9C_8$ which is encoded to 01 by 3:2 encoder. Finally the binary output is 01101 which is a correct value for an analog input with a range of $13V_{REF}/32$ and $14V_{REF}/32$. In the similar way, the reconfigurable ADC can work as a three bit as well as two bit ADC by making B_4 and B_3 to zero and by making B_4, B_3 and B_2 to zero respectively. When the reconfigurable ADC is operating in a lower resolution mode, the power dissipation would reduce by a large amount. This is because of the large reduction in the switching activities of the operation [100]. The characteristics curves such as power dissipation Vs sampling frequency, ENOB Vs Sampling Frequency, ENOB Vs input signal frequency, SFDR Vs clock frequency and SFDR Vs input signal frequency are following the same path as discussed in the previous chapter.

6.10 Performance summary of the proposed reconfigurable ADC

Table 6.5 describes the performance summary report of the proposed flash ADC. The ADC is simulated and verified using UMC 180 nm technology from a power supply of 1.8 V. The die area of the implementation is 432 µm × 720 µm (0.31104 mm^2). To summarize the table, proposed reconfigurable five bit flash ADC is having an excellent ENOB with a lower sampling frequency of 1.2 GHz. The power dissipation of the proposed reconfigurable flash ADC is 11.71 mW.

Table 6. 5 Performance summary of reconfigurable five bit flash ADC

Parameter	Flash ADC
Input signal range (V)	0.5 - 1.4 (0.9)
Input frequency of operation (MHz)	566.40 MHz
Resolution (bits)	5
Supply voltage (V)	1.8
Sampling frequency (GHz)	1.25
Maximum DNL (LSB)	0.355
Maximum INL (LSB)	-0.648
SFDR (dB)	40.12
ENOB (bits)	4.78
Power consumption (mW)	11.71
Die area (mm^2)	0.31104
Technology (nm)	UMC 180
Supply voltage (V)	1.8

6.11 Comparison with other works

Table 6.6 shows the comparison table between the proposed ADC with other reconfigurable architectures. The proposed reconfigurable ADC is having a better ENOB (4.78) in comparison with the chapter 5 with a sampling frequency of 1.2 GHz (4.76). The comparison table shows that the proposed work is best suited for DS-UWB applications where lower sampling frequency (in the range of 1-1.5 GHz) is used. The other works which is having same resolution ([88], [89]), the proposed flash ADC is having the highest sampling

frequency with medium power dissipation. So the proposed ADC is best suited for low power applications with a higher sampling frequency.

Table 6. 6 Comparison table of reconfigurable ADC with other similar works

	[99] (Reconfig)	[98] (Reconfig.)	[88]	[89]	This work
Technology	CMOS 90 nm	CMOS 180 nm	CMOS 180 nm	CMOS 130 nm	UMC 180 nm
Architecture	Flash ADC	Flash ADC	Time-domain Flash	Flash ADC	Flash ADC
Input signal frequency	2.1 GHz	400 MHz	---	----	566.40 MHz
Sampling Rate	5GS/s	528 MS/s	500MS/s	1 GS/s	1.25 GHz
Resolution (bits)	4	6	5	5	5
ENOB	3.9	5.4	4.13	4.73	4.78
Peak DNL/INL (LSB)	0.66/0.62	1.24/0.74	0.43/0.58	---	0.355/-0.648
Supply Voltage (V)	1	1.8	1.8	1.2	1.8
Power Consumption (mW)	197	63	8	46	11.71
Area(mm^2)	0.2821	N/A	0.132	0.20	0.31104

6.12 Chip Tape out implementation of reconfigurable ADC

The basic design flow of an analog IC design [61] is shown in Fig. 6.15. Each of the blocks in the design flow is explained briefly.

6.12.1 System requirements and design specifications

The IC design flow generally starts with system requirements and design specifications. The specification normally describes the anticipated functionality of the proposed block, the die area, the maximum allowable delay times and other properties such as power consumption. For example, in the case of an ADC, the specification contains technology used, resolution, architecture employed, input signal frequency, sampling frequency, power dissipation and static and dynamic characteristics of ADC. The design specification gives significant liberty to select the circuit topology, component placements, placements of output and input pins and (W/L) ratio of MOSFETs.

6.12.2 Schematic capture

Designing of the circuit is the fundamental step in the IC design flow. The electronic schematic of the designed circuit is done with the help of a schematic editor. Generally the circuits are drawn first on a paper and inserted into computer using schematic editor. So schematic capture is called front end operation of the design flow. Schematic capture contains power supply, ground connections, as well as output and input pins of the circuit. With the help of complete schematic, net-list is created for the complete circuit which is used in the later stage of the design.

6.12.3 Simulation

Once the complete schematic drawing is over, the circuit functionality should be confirmed through simulation. If the simulation is not coming correctly, it confirms that the design is incorrect. In that case, redesign the circuit and get the simulation results correctly.

6.12.4 Physical design

The circuit performance such as speed, area and power dissipation is connected with physical layout design [102]. The layout of the circuit automatically generates parasitic capacitances and resistances which are taken into consideration while doing post layout simulation. There are some specific design rules for drawing of layout. These design rules should not be violated during the drawing of the layout.

6.12.5 Design rule check (DRC)

After completion of the layout, the design rule check operation should be performed. If the layout contains any design rule errors, it should be corrected and the final layout should not contain any DRC errors.

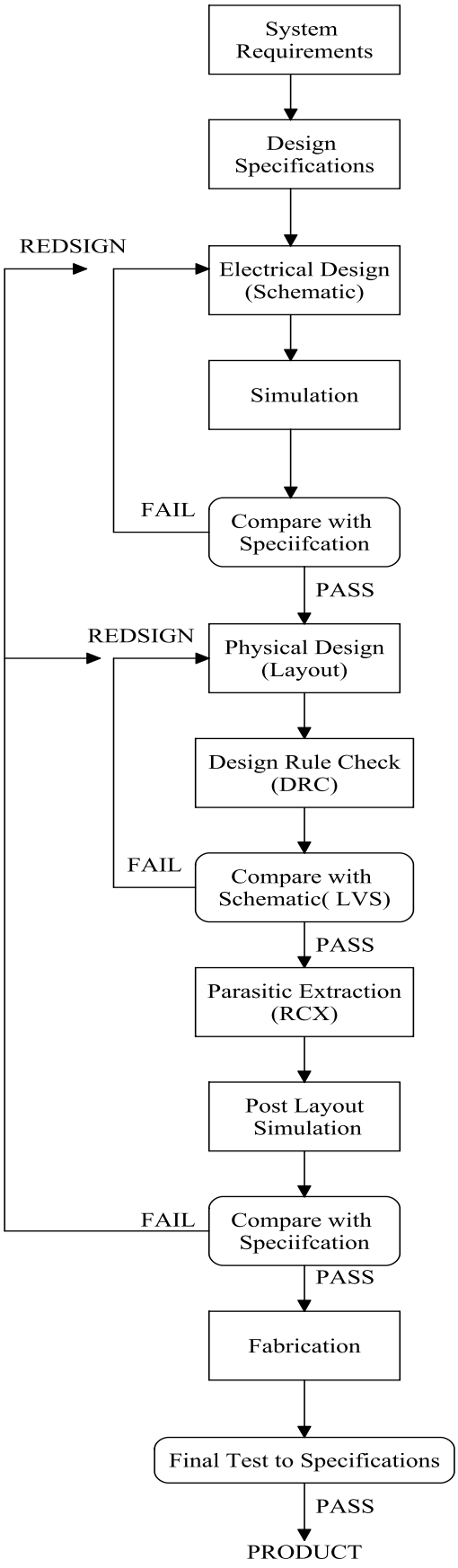


Fig. 6.15 Analog IC design flow

6.12.6 LVS (Layout Vs Schematic matching)

After completion of the layout, it should be matched with schematic. This testing is called LVS. LVS provides a guarantee that the layout which is drawn using the tool is matched in the topology with the schematic of the circuit. It is not giving any guarantee that the circuit functions properly, if LVS is passed successfully. If any errors are there in LVS, it should be corrected before proceeding to the next step.

6.12.7 Parasitic capacitance and resistance extraction (RCX)

The parasitic capacitances and resistors are extracted from the layout with the help of this process which should be considered in the post layout simulation. Due to this parasitic capacitances and resistors, post layout simulation power is more than the pre layout simulation power.

6.12.8 Post layout simulation

The post layout simulation is performed on RCX extracted view of the layout (av_extracted). This is highly essential step before fabrication. If the post layout simulation is not coming correctly, rework should be done in layout or schematic so that the correct functionality should be achieved.

6.12.9 Fabrication

A satisfactory result in post-layout simulation is still no guarantee for a completely successful product; the actual performance of the chip can only be verified by testing the fabricated prototype. Adding pads to the circuits is the final step in the IC design flow. After successfully adding pads to the circuit, the chip is send to fabrication lab for manufacturing. Even though the parasitic extraction step is used to identify the realistic circuit conditions to a large degree from the actual mask layout, most of the extraction routines and the simulation models used in modern design tools have inevitable numerical limitations. This should always be one of the main design considerations, from the very beginning.

6.12.10 Final testing

After chip is manufactured, the final testing is done on chip to check the functionality. If the functionality is properly matched, then the chip is provided to the customer.

The chip tape out of the proposed reconfigurable ADC design is shown in Fig. 6.16

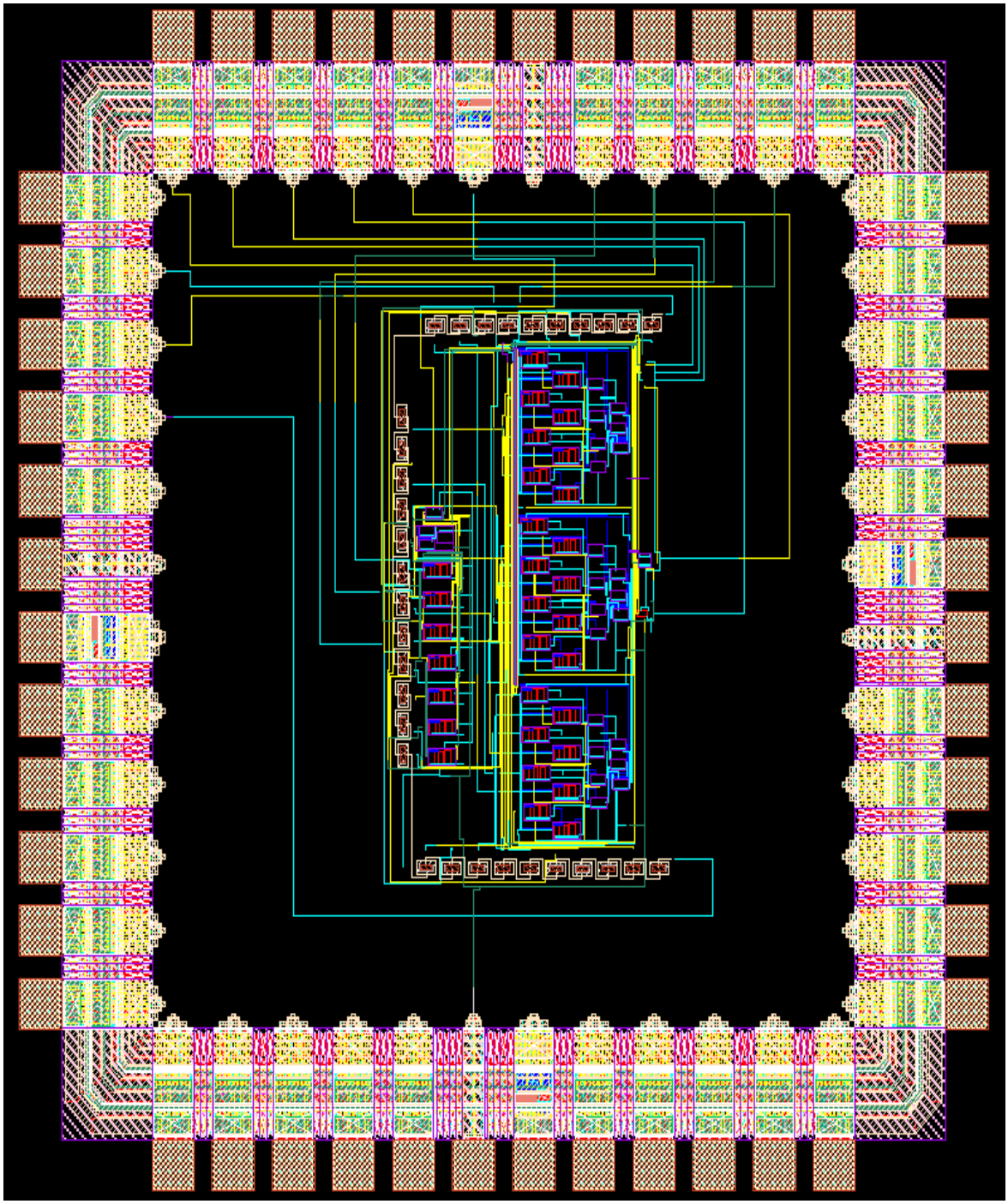


Fig. 6.16 Final chip tape out of proposed reconfigurable flash ADC

6.13 Conclusion

The chapter describes about the implementation of a reconfigurable five bit flash ADC used for DS-UWB applications. The chapter starts with brief discussion about reconfigurable flash ADC. Reconfigurable flash ADC contains resistor ladder, comparators and multiplexers. The architecture is explained in detail with an example. The implementation of each block is presented. Once the schematic simulation is over and verified, layout of the circuit is drawn.

DRC, LVS and RCX are performed on the design. Post layout simulation is performed on the av_extracted view of the layout. The reconfigurable flash ADC is designed and verified using CADENCE tool with UMC 180 nm technology. The total power dissipation of the ADC is 11.71 mW from power supply of 1.8 V. Static and dynamic characteristics of proposed ADC is discussed in the subsequent section of the chapter. Reconfigurable operation of the proposed ADC is also explained. Performance summary of the proposed ADC and comparison with other similar works are reported in next section. The analog IC design flow is explained in the last section of the chapter along with the chip tape out of the proposed reconfigurable ADC.

CHAPTER 7

CONCLUSION & FUTURE SCOPE

7.1 Conclusion

With the advancement of technology, digital signal processing has progressed significantly in recent years. However, the development of technology has not provided same level of benefit for the analog integrated circuit design. In order to extract the advantages of digital signal processing, there is a trend of shifting signal processing from analog to more capable digital domain and interacting with the analog signals only in the input as well as in the output stages. The advancement in the wireless communication technology is one of the motivation factors of development in analog electronics field. Modern communication systems necessitate higher data rates which have increased the demand for the high speed transceivers. For a system to work efficiently, all blocks of that system should be fast. It can be seen that the analog interfaces are main bottleneck in the whole system in terms of speed and power. This fact has led researchers to develop and implement high speed analog-to-digital converters (ADCs) with low power consumption.

This thesis demonstrated a high speed five bit flash ADC used for DS-UWB applications. The design presented in this work was an attempt to implement a converter for DS-UWB scheme, due to its high bandwidth and sampling constraints. The designed converter is a practical approach targeted at low power high speed ultra wideband communications specifically directed towards Direct Sequence UWB communication applications such as biomedical, wireless in home connectivity. The first design is a flash based analog-to-digital converter with a finite output resolution of five bits and with a sampling rate of 5 GS/s. The high speed flash ADC is designed and verified using CADENCE tool with CMOS 90 nm technology. The flash converter has an effective maximum power consumption of 8.381 mW, occupying an active total chip die area of 0.039 mm^2.

This thesis also presented the implementation of a variable five bit converter to satisfy the ever increasing technological and operating requirements of DS-UWB. The second design implemented is a reconfigurable five bit flash analog-to-digital converter. The reconfigurable property has been implemented with the help of high speed comparators, multiplexers and a 3:2 encoder. The reconfigurable flash ADC is designed and verified using CADENCE tool with UMC 180 nm technology. The total power dissipation of the ADC is 11.71 mW from power supply of 1.8 V

with an active total chip die area of 0.31104 mm^2. The reconfigurable converter outperforms previously designed flash ADC in terms of ENOB at a lower frequency of 1. 25 GHz. The chip tape out has been made for the reconfigurable five bit flash ADC and which is send to fabrication.

7.1.1 Research contributions

ADC is a significant block in UWB receiver. The different types of ADCs used in the receiver are studied and flash ADC is taken as the best architecture for the specified application. Regular flash ADC contains 2^N-1 comparators. In view of that a high speed pseudo dynamic logic based CMOS comparator is designed and implemented. The outputs of the comparators are coming in a special fashion called thermometer code. The thermometer code is converted into binary code using an encoder in flash ADC. Accordingly a high speed noise tolerant encoder has been designed and implemented. Regular flash ADC architecture contains three different blocks such as resistor ladder, 2^N-1 comparators and an encoder. The resistor ladder is designed and implemented separately. With the help of combining resistor ladder, comparators and an encoder, a high speed flash ADC is implemented. The proposed flash ADC is analysed and compared with other research papers which is having same resolution and concluded that it is having the highest speed of operation with medium power dissipation. A reconfigurable flash ADC is also designed and implemented. Comparison has been made with similar architectures and generates the chip tape out design.

7.2 Future Scope

All the parameters of reconfigurable flash ADC can be considered for lower resolution and compare its characteristics with other low resolution ADCs. Offset cancellation technique can be adopted in order to reduce the offset in the comparator which improves the efficiency of the total flash ADC. Calibration technique shows great potential in high speed and low power flash ADC design. This technique can be adopted in order to simplify the design.

Bibliography

[1] M. Z. Win and R. A. Scholtz, "Impulse radio: how it works," *IEEE Communications Letters*, vol. 2, pp. 36-38, 1998.

[2] I. Oppermann, *et al.*, "UWB: Theory and Applications," *WILEY Publishers*, Edition 2004.

[3] K. Mandke, *et al.*, "The Evolution of Ultra Wide Band Radio for Wireless Personal Area Networks," Technology Report for University of Texas, Austin, September 2003.

[4] J. Reed, et al., "Introduction to UWB: Impulse Radio for Radar and Wireless Communications," Presentation by Mobile and Portable Radio Research Group, 2004.

[5] J. Ryckaert, et al., "A CMOS ultra-wideband receiver for low data- rate communication", IEEE Journal of Solid State Circuits, vol. 42, pp. 2515-2527, Nov 2007.

[6] L. Yang and G. B. Giannakis, "Ultra-wideband communications: an idea whose time has come," *IEEE Signal Processing Magazine*, vol. 21, pp. 26-54, Nov 2004.

[7] J. M. Wilson, "Ultra-Wideband / a Disruptive RF Technology?" *Industry report for Intel*, September 2002.

[8] C. Shih-Lu, *et al.*, "A wireless body sensor network system for healthcare monitoring application", *IEEE Conference on Biomedical Circuits and Systems*, pp 243-246, Nov 2007.

[9] I. Gresham, *et al.*, "Ultra-wideband radar sensors for short-range vehicular applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2105-2122, Sep 2004.

[10] H. Sheng, *et al.*, "On the spectral and power requirements for ultra-wideband transmission", *IEEE International Conference on Communications*, vol. 1, pp. 738-742, May 2003.

[11] R. Blazquez, *et al.*, "Digital architecture for an ultra-wideband radio receiver" *58th IEEE Vehicular Technology Conference*, vol.2, pp. 1303-1307, Oct 2003.

[12] D. D. Wentzloff, R.l Blazquez, F. S. Lee, B. P. Ginsburg, J. Powell and A. P. Chandrakasen, "System design considerations for ultra-wideband communication," *IEEE Communication Magazine*, vol. 43, no. 8, pp. 114-121,Aug. 2005.

[13] M. Verhelst, *et al.*, "Architectures for low power ultra-wideband radio receivers in the 3.1-5GHz band for data rates < 10Mbps," *Proceedings of the 2004 International Symposium on Low Power Electronics and Design*, pp. 280-285, Aug 2004.

[14] W. Namgoong, "A channelized DSSS ultra-wideband receiver," *IEEE Radio and Wireless Conference*, pp. 105-108, Aug 2001.

[15] V. Ghazi-Moghadam, "MBOA and DS-UWB proposals for UWB standard A system level comparison," *Presentation MWRF*, 2004.

[16] M. Vogels and G. Gielen, "Architectural selection of A/D converters," *Proceedings of Design Automation Conference*, pp. 974-977, June 2003.

[17] K. Uyttenhove and M. Steyaert "Design of high-speed analog-to-digital interface in digital technologies", *8th IEEE International Conference on Electronics, Circuits and Systems*, vol.1, pp. 493-496, Sep 2001.

[18] Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, *Oxford Indian 2nd Edition*, 2010.

[19] Ili Shairah Abdul Halim, NurulAisyah nadiahBinti Zainal Abidin, A'Zraa Afhzan Ab Rahim, "Low power CMOS charge sharing dynamic latch comparator using 0.18µm technology", *IEEE Regional symposium on micro and nano electronics (RSM)*,pp 156-160, Sep 2011.

[20] M. Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, "A Low-Noise Self- Calibrating Dynamic Comparator for High-Speed ADCs," *IEEE Asian solid state conference*, pp. 269-272, Nov. 2008.

[21] Zhaohui Huang, Peixin Zhong , "An adaptive analog-to-digital converter based on low-power dynamic latch comparator," *IEEE International conference on electro information technology*, pp1- 6, May 2005.

[22] Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 53, no. 12, pp. 1398- 1402, Dec 2006.

[23] Mohamed Abbas, Yasuo Furukawa, Satoshi Komatsu, Takahiro J. Yamaguchi, and Kunihiro Asada, "Clocked Comparator for High-Speed Applications in 65nm Technology" *IEEE Asian solid state circuits conference*, pp. 1-4, Nov. 2010.

[24] Carlos J Solis, Gladys O. Ducoudray, "High Resolution Low power 0.6µm CMOS 40MHz Dynamic Latch Comparator," *53rd IEEE International Midwest symposium on circuits and systems*, pp. 1045-1048, Aug. 2010.

[25] Riyan Wang Kaihang Li Jianqin Zhang Bin Nie "A High-Speed High Resolution Latch Comparator for Pipeline Analog-to-Digital Converters," *IEEE International workshop on Anti counterfeiting, security, identification*, pp.28-31, April 2007.

[26] P. Cusimato et al., "Analysis of the behavior of a dynamic latch comparator", *IEEE Transactions on Circuits and Systems-I: Theory and Applications*, vol. 45, no. 3, pp. 294-298, Mar. 1998.

[27] HeungJun Jeon, Yong Bin Kim, " A CMOS low power low offset and high speed fully dynamic latched comparator", *IEEE International SOC conference*, pp 285-288, Sep 2010.

[28] Santhosh Kumar Patnaik, Swapna Banerjee, "Noise and error analysis and optimization of a CMOS latched comparator", *International conference on communication technology and system design, Elsevier proceedia engineering*, pp 210-217, June 2012.

[29] X. P. Fan and P. K. Chan, "A CMOS high-speed multistage preamplifier for comparator design", *International symposium on circuits and systems*, pp 545-548, May 2004.

[30] L. Bouzerara, M.T. Belaroussi, "Low-Voltage, Low-Power and High Gain CMOS Operational Transconductance Amplifier," *IEEE International Symposium on Circuits and Systems*, pp. 325-328, May 2002.

[31] Eiji Shirai, "CMOS Multistage Preamplifier Design for High- Speed and High-Resolution Comparators", *IEEE transactions on circuits and systems II*, vol. 54, issue 2, Feb 2007.

[32] M. Bazes, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers," *IEEE journal of Solid-State Circuits*, vol. 26, pp. 165-168, Feb 1991.

[33] S. Park and M. P. Flynn, "A regenerative comparator structure with integrated inductors," *IEEE Transactions on Circuits and Systems I*, vol. 53, pp.1704–1711, Aug. 2006.

[34] Guo Yongheng, Cai Wei, Lu Tiejun, Wang Zongmin, " A Novel 1GSPS low offset comparator for high speed ADC", *5th International joint conference on INC, IMS and IDC*, pp 1251-1254, Aug 2009.

[35] Pedro M.Figueiredo, Joao C.Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparator", *IEEE Transactions on Circuits and Systems*, vol.53, no.7, pp.541-545, July 2006.

[36] Jia Chen, S. Kurachi, Shimin Shen, Haiwen Liu, T. Yoshimasu, et al, "A Low-Kickback-Noise Latched Comparator for High-Speed Flash Analog-to-Digital Converters," *IEEE international symposium on communications and information technology*, vol. 1, pp. 250-253, Oct. 2005.

[37] V. Boonsobhak, A. Worapishet, and 1. B. Hughes, "Reduced Kickback Regenerative Current Comparator for High-Speed Switched-Current Pipeline Analogue-To-Digital Converters", *IEEE Electronics Letters*, vol. 39, no. 1, pp. 4-5, Jan. 2003.

[38] Ali Baradaranrezaeii, Roozbeh Abdollahi, Khayrollah Hadidi, Abdollah Khoei, "A 1GS/s low power low kick back noise comparator in CMOS process", *20th European conference on circuit theory and design*, pp 106-109, Aug 2011.

[39] J. Chen, S. Kurachi, S. M. Shen, H. W. Liu, T. Yoshimasu, and Y. J. Suh, "A low-kickback-noise latched comparator for high-speed flash analog-to-digital converter", *IEEE international symposium on Communications and Information Technology*, pp. 259-262, Oct. 2005.

[40] T. Sundstrom, A Alvandpour, "A Kick-Back Reduced Comparator for a 4-6-Bit 3-GS/s Flash ADC in a 90nm CMOS Process", *International conference on mixed design of integrated circuits and systems*, pp. 195-198, June 2007.

[41] Xinbo Qian and T. Hui Teo, "A Low-power Comparator with Programmable Hysteresis Level for Blood Pressure Peak Detection," IEEE *Region 10 Conference, TENCON*, pp.1-4, Jan2009.

[42] S. Kale and R. S. Gamad, "Design of Low Power and High Speed CMOS Comparator for A/D Converter Application", *International Journal of Electronic Engineering Research*, vol. 2, no. 1, pp. 29-34, 2010.

[43] K. Moolpho, J. Ngarmnii, S. Sitjongsataporn, "A High Speed Low Input Current Low Voltage CMOS Current Comparator", *International symposium on circuits and systems*, pp 433-436, May 2003.

[44] A. Mohan, A. Zayegh, A. Stojcevski, R. Veljanovski, "High Speed Ultra Wide Band Comparator in Deep Sub-Micron CMOS", *IEEE International Symposium on Integrated Circuits*, pp. 386-389, Sep 2007.

[45] B. Han, Y. Yang, Z. Zhu, "A novel 1.2GSPS ultra High-Speed comparator in 0.18μm CMOS", *9th International Conference on Solid- State and Integrated-Circuit Technology*, pp. 1957-1960, Oct 2008.

[46] Song Ye, Jie Wu, "An Ultra high speed comparator for ADC in 90nm CMOS Technology", *3rd IEEE Symposium on microwave, Antenna, Propagation and EMC technologies*, pp 1131-1134, Oct 2009.

[47] S. Sheikhaei, Sh. Mirabbasi, and A. Ivanov, "A 0.35μm CMOS comparator circuit for High-Speed ADC applications", *International symposium on circuits and systems*, Vol. 6, pp. 6134-6137, May 2005.

[48] P. Amaral, J. Goes, and N. Paulino, "An improved low voltage low-power CMOS comparator to be used in high speed pipeline ADCs," *IEEE International Symposium on circuits and systems*, pp. 141–144, May 2002.

[49] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 0.35μm CMOS Comparator Circuit for High-Speed ADC Applications," *IEEE International Symposium on Circuits and Systems*, pp. 6134-6137, May 2005.

[50] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high resolution comparators", *IEEE Journal of Solid State Circuits*, vol. 27, pp. 1916– 1926, Dec. 1992.

[51] Amalan Nag, K.L.Baishnab, "Low power high precision and reduced size CMOS comparator for high speed ADC design", *5th International conference on industrial and information systems*, pp 219-222, Jul 2010.

[52] Shaozhen Zhang, Zheying Li, Bo Ling, "Design of High speed and low power comparator in flash ADC", *International workshop on information and electronics engineering, Elsevier Proceedia Engineering*, pp 687-692, 2012.

[53] Vinayashree hiremath, Saiyu Ren, " An ultra high speed encoder for 5 GSPS flash ADC", *IEEE conference on instrumentation and measurement technology*, pp 136-141, May 2010.

[54] Yu Qi, Guohe Zhang , Shao, Zhibiao , Bo Wang, "A low kick back noise latched comparator for high speed folding and interpolating ADC ", *IEEE Asia Pacific Conference on Circuits and Systems*, pp 272-275, Nov 2008.

[55] Jinda Yang, Xu Cheng ; Yawei Guo ; Zhang Zhang, "A novel low-offset dynamic comparator for high-speed low-voltage pipeline ADC ", 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp 548-550, Nov 2010 .

[56] M.J.T.Marvast , M.A.M.Ali, " High speed comparator for flash ADC and UWB application in 130 nm CMOS technology", IEEE International Conference on Signal and Image Processing Applications" , pp 402-405, Nov 2009.

[57] M.Abbas, Y.Furukawa,S. Komatsu J.Y.Takahiro, "Clocked comparator for high-speed applications in 65nm technology ", IEEE Asian Solid State Circuits Conference , pp 1-4, Nov 2010.

[58] A.Matsuzawa, "High speed and low power ADC design with dynamic analog circuits", 8th IEEE International Conference on ASIC pp 218-221, Oct 2009.

[59] D.Lee, J.Yoo, K.Choi and J. Ghaznavi, "Fat-tree encoder design for ultrahigh speed flash analog- to-digital converters" *IEEE Midwest Symposium on Circuits and Systems*, pp 233-236, Aug 2002

[60] S. Sheikhaei, S. Mirabbasi, A. Ivanov, "An Encoder for a 5GS/s 4bit flash A/D converter in 0.18um CMOS", *Canadian Conference on Electrical and Computer Engineering*, pp 698-701, May 2005.

[61] R.Baker, H.W.Li, and D.E. Boyce, CMOS Circuit Design, Layout and Simulation. *Prentice Hall* 2000.

[62] Sunghyun Park, Yorgos Palaskas, Ashoke Ravi, Ralph.E.Bishop, and Michael P. Flynn, " A 3.5 GS/s 5-b Flash ADC in 90nm CMOS", *IEEE Custom Integrated Circuits Conference*, pp. 489-492, Sep 2006.

[63] Niket Agrawal, Roy Paily, "An Improved ROM Architecture for Bubble error Suppression in High Speed Flash ADCs", *Annual IEEE Conference*, pp 1-5, Feb 2008.

[64] Mustafijur Rahman, K.L. Baishnab, F.A. Talukdar, "A Novel ROM Architecture for Reducing Bubble and Meta-stability Errors in High Speed Flash ADCs", *20th International Conference on Electronics, Communications and Computers*, pp 15-19, 2010.

[65] Vinayashree Hiremath, "Design of High Speed ADC", *M.S. Thesis, Wright State University*, 2010.

[66] Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits, a design perspective", *second edition, Prentice Hall* 2011.

[67] Madhumati, G.L., Rao, K.R., Madhavilatha, M., "Comparison of 5-bit Thermometer-to-Binary Decoders in 1.8V, 0.18µm CMOS Technology for flash ADC ", *International conference on Signal Processing Systems*, pp 516-520, May 2009.

[68] Erik Sail, Mark Vesterbacka, "A multiplexer based decoder for flash analog-to-digital converter", *IEEE region 10 TENCON conference*, volume 4, pp 250-253, Nov 2004.

[69] Erik Sail, Mark Vesterbacka,"Comparison of two thermometer to binary decoders for high performance flash ADCs", *23rd NORCHIP conference*, pp 253-256, Nov 2005.

[70] Erik Sail, Mark Vesterbacka,"Thermometer to binary decoders for flash analog-to-digital converters", *18th European conference on circuit theory and design,* pp 240-243, Aug 2007.

[71] Khalid ali shehata, Hnadey hussein, Hani Fekri Rgai, "Design and implementation of 2.5 GBPS pipelined digital encoder for flash A/D converter", *2nd international conference on signals, circuits and systems*, pp 1-5, Nov 2008.

[72] E.Sail et al, "A study of digital decoders in flash analog-to-digital converters", *IEEE symposium on circuits and systems,* vol. 1, pp 132-134, May 2004.

[73] F. Kaess, R. Kanan, B. Hochet, and M. Declercq, "New encoding scheme for high-speed flash ADC's," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 5–8, June 1997.

[74] P. Pereira, J. R. Fernandes, and M. M. Silva, "Wallace tree encoding in folding and interpolation ADCs," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 509–512, May 2002.

[75] R. Kanan, F. Kaess, and M. Declercq, "A 640 mW high accuracy 8-bit 1 GHz flash ADC encoder," IEEE International Symposium on Circuits and Systems, pp. 420-423, July1999.

[76] Yao-Jen Chuang, Hsin-Hung Ou, and Bin-Da Liu "A Novel Bubble Tolerant Thermometer-to-Binary Encoder for Flash A/D converter", IEEE International Symposium on VLSI-TSA, pp. 315 – 318, April 2005.

[77] Vudadha, Chetan et al."Low-Power Self Reconfigurable Multiplexer Based Decoder for Adaptive Resolution Flash ADCs." *25th International conference on VLSI designs*, pp. 280-285, Jan 2012.

[78] Y Gupta, et al."Design of low power and high speed multiplexer based thermometer to gray encoder." *International symposium on intelligent signal processing and communication systems*, pp 501-504, Nov 2013.

[79] Akashe, Shyam, Vinod Rajak, and Gunakesh Sharma. "Optimization of fat tree encoder for ultra high speed analog-to-digital converter using 45 nanometer technology." *Optik-International Journal for Light and Electron Optic,* Vol. 124, Issue 20, pp. 4490–4492, Oct. 2013.

[80] Ili Shairah Abdul Halim, Siti Lailatul Mohd Hassan, Nurul Dalila binti Mohd Akbar, Azraa Afhzan Ab. Rahim "A Comparative Study of Comparator and Encoder in a 4-bit Flash ADC using 0.18m CMOS Technology" , *IEEE International Symposium on Computer Applications and Industrial Electronics*, pp. 35-38, Dec. 2012.

[81] Jungwook Yang, West Nyack, "Bubble and Meta-stability error immune gray-code encoder for high-speed A/D converters", *U.S. patent No. US6388602 B1*, 2002

[82] Daegyu, Y. Jincheol, C. Kyusun, and Ghaznavi, "Fat tree encoder design for ultra-high speed flash ADC converters," *45th Midwest Symposium on circuits and systems*, pp. 87-90, Aug 2002.

[83] Portmann, C. L. and Meng, T. H. Y., "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters", *IEEE Journal of Solid-State Circuits*, Vol.31, No.8, pp.1132-1140. Aug 1996.

[84] Bui Van Hieu; Seunghyun Beak; Seunghwan Choi; Jongkook Seon; Jeong, T.T. , "Thermometer-to-binary encoder with bubble error correction (BEC) circuit for Flash Analog-to-Digital Converter (FADC)," *3rd International Conference on Communications and Electronics*, pp. 102-106, Aug. 2010.

[85] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65nm CMOS with split capacitor array," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739-747, Apr. 2007.

[86] J. E. Proesel and L. T. Pileggi, "A 0.6-to-1V inverter-based 5-bit flash ADC in 90nm digital CMOS," *IEEE Custom Integrated Circuits Conference*, pp. 153-156, Sept. 2008.

[87] Y. Lin, S.Jyh Chang, Y.Liu, C.Liu and G. Huang, "A 5b 800MS/s 2mW asynchronous binary-search ADC in 65nm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 80-81, Feb. 2009.

[88] Young-Jae Min, "A 5-bit 500-MS/s Time-Domain Flash ADC in 0.18µm CMOS", *13th International Symposium on integrated circuits*, pp. 336-339, Dec 2011.

[89] O. Viitala et al, "A 5-bit 1-GS/s Flash-ADC in 0.13-µm CMOS Using Active Interpolation", *Proceedings of the 32nd European Solid-State Circuits Conference*, pp. 412-415, Sep 2006.

[90] Li Shiwen, Dang Hua et al "Design and implementation of a CMOS 1Gsps 5bit Flash ADC with offset calibration", *IEEE International Conference on Green Computing*, pp 1829-1833, Aug 2013.

[91] A. G. W. Venes and R. J. van de Plassche, "An 80-MHz, 80-mW,8-b CMOS folding A/D converter with distributed track-and-hold pre-processing," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 1846–1853, Dec 1996.

[92] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, G.Van der Plas, "A 2.2 mW 1.75 GS/s 5 Bit Folding Flash ADC in 90 nm Digital CMOS", *IEEE Journal of .Solid-State Circuits*, vol. 44, no. 7, pp. 874–882, Feb. 2009.

[93] D. Draxelmayr, "A 6 b 600 MHz 10 mW ADC array in digital 90 nm CMOS," *IEEE International Solid-State Circuits conference*, pp. 264-265, Feb. 2004.

[94] C. Sandner, M. Clara, A. Santner, T. Hartig and F. Kuttner, "A 6-bit 1.2-GS/s low-power flash-ADC in 0.13- m digital CMOS," *IEEE Journal of. Solid-State Circuits*, vol. 40, no. 7, pp. 1499-1505, Jul. 2005.

[95] Guanzhong Huang et al, "A 5-bit 125-MS/s 367-µW ADC in 65-nm CMOS" IEEE 55th International Midwest Symposium on circuits and systems, pp 1-4, Aug 2012.

[96] Junjie Yao et al, "A 5-GS/s 4-bit flash ADC with triode-load bias voltage trimming offset calibration in 65-nm CMOS", IEEE Custom Integrated Circuits Conference , Sep 2011

[97] M.Miyahara et al, "A 0.5 V, 1.2 mW, 160 fJ, 600 MS/s 5 bit Flash ADC", IEEE Asian Solid State Circuits Conference, pp 1-4, Nov 2010.

[98] E.M.I. Gustafsson et al, "Design of a reconfigurable ADC for UWB/Bluetooth radios", IEEE Northeast workshop on Circuits and Systems, pp 205-208, June 2008.

[99] A. Mohan, "Performance Comparison of Flash and Reconfigurable ADC for UWB Applications", International Conference on Modelling and Simulation (ASME 2010), Prague, 2010.

[100] Cheng-Chung Hsu et al, "A 7b 1.1GS/s Reconfigurable Time-Interleaved ADC in 90nm CMOS", IEEE symposium on VLSI circuits, pp 66-67, June 2007.

[101] B. Razavi, "Design of Analog CMOS Integrated Circuits*", McGraw-Hill Education*, 2000.

[102] Zhiheng Cao, Shouli Yan, "Low-Power High-Speed ADCs for nanometer CMOS Integration", *Springer Science & Business Media*, 2008.

[103] A. Hastings, "The Art of Analog Layout", *Pearson Prentice Hall*, 2nd edition, 2006.

[104] Willy M. C. Sansen , " Analog Design Essentials", *Springer publishers*, 2006.

[105] M. Gustavsson, et al., "CMOS Data Converters for Communications", Kluwer *academic publishers*, 2000.

List of Publications

Conferences

[1]. George Tom Varghese, K. K. Mahapatra, "A high speed encoder for a 5GS/s 5 bit flash ADC", *3rd International conference on Computing Communication & Networking Technologies (ICCCNT)*, pp. 1-5, July 2012.

[2]. George Tom Varghese, K. K. Mahapatra, "A high speed low power encoder for a 5 bit flash ADC", *International conference on Green Technologies (ICGT)*, pp. 41- 45, Dec 2012.

[3]. Y. Lavania, George Tom Varghese, K. K. Mahapatra, "An ultra low power encoder for 5 bit flash ADC", *International conference on Emerging Trends in VLSI, Embedded System, Nano Electronics and Telecommunication System (ICEVENT)*, pp. 1-5, Jan 2013.

Journals

[1]. George Tom Varghese, K. K. Mahapatra," A High Speed Preamplifier based Pseudo Dynamic Latched Comparator for High Speed ADCs", *International Journal of electronics* (Taylor and Francis) (Communicated)

[2]. George Tom Varghese, K. K. Mahapatra, "A High Speed Low Power Reconfigurable Encoder for Five Bit Flash ADCs", *IETE Journal of Research* (Communicated)

[3]. George Tom Varghese, K. K. Mahapatra," "A Low Power Multiplexer based Encoder for Five Bit Flash ADCs", *IEI*-Springer *Journal* (Communicated)

Letters

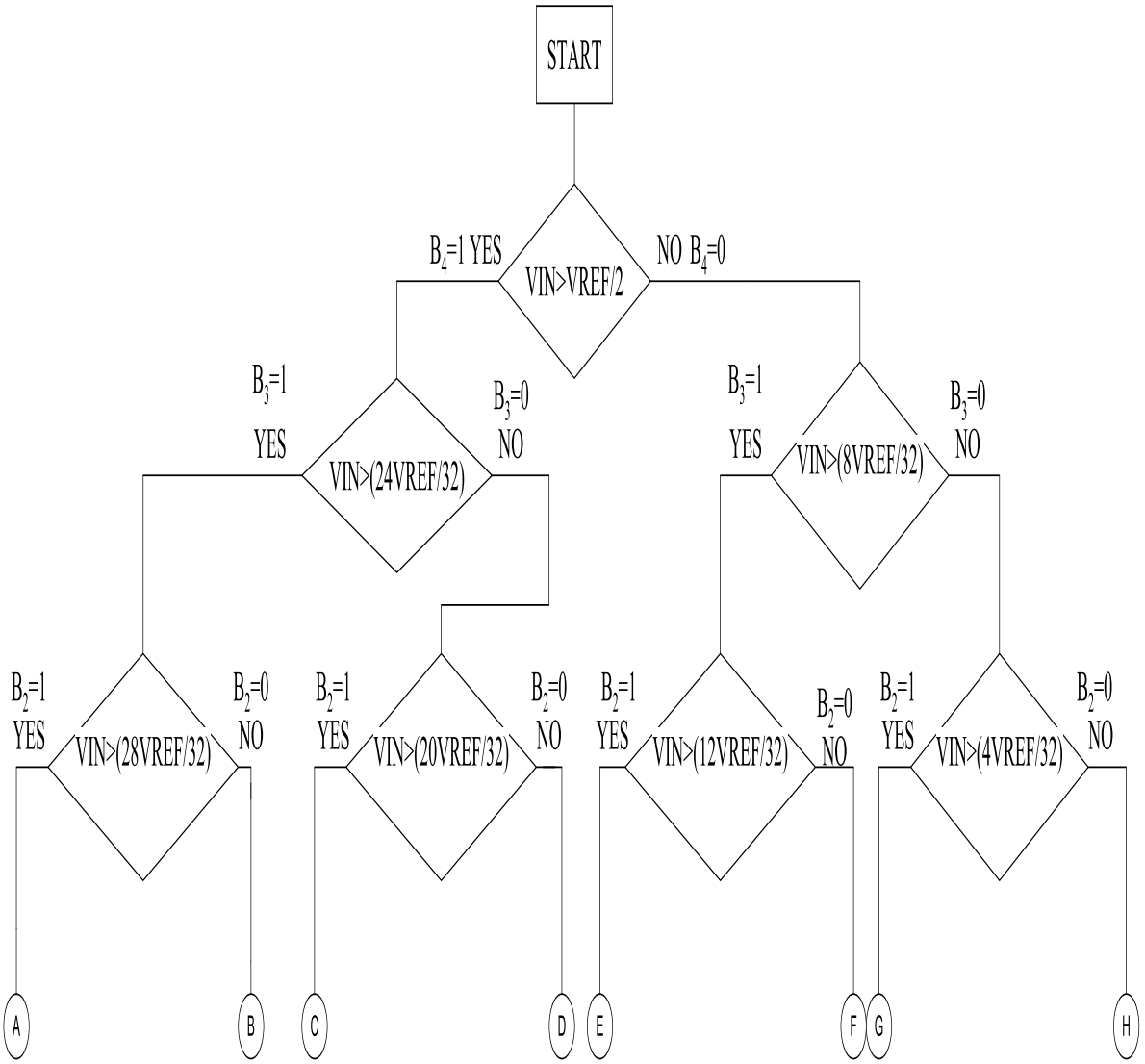
[1]. George Tom Varghese, K. K. Mahapatra," Performance Comparison of 5 bit Thermometer code to Binary code Conversion", *International Journal of Electronics Letters* (Taylor and Francis) (Communicated)

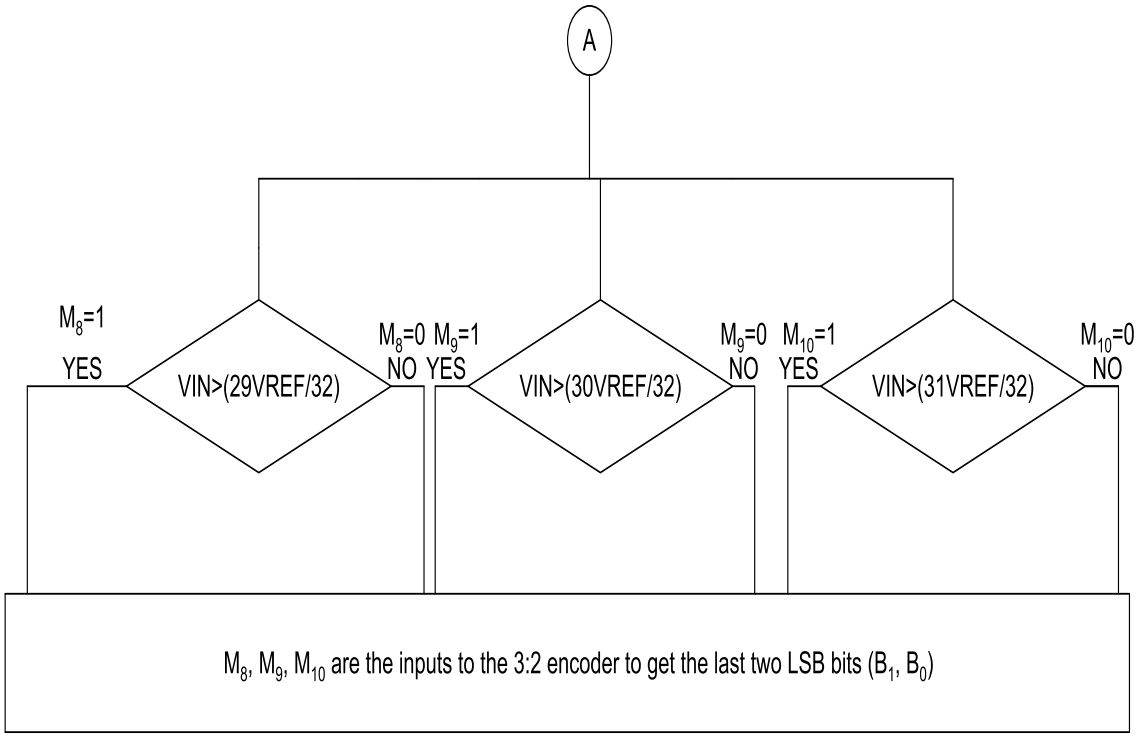
[2]. George Tom Varghese, K. K. Mahapatra," A High Speed Self Reconfigurable Multiplexer based Encoder for Flash ADCs", *International Journal of Electronics Letters* (Taylor and Francis) (Communicated)

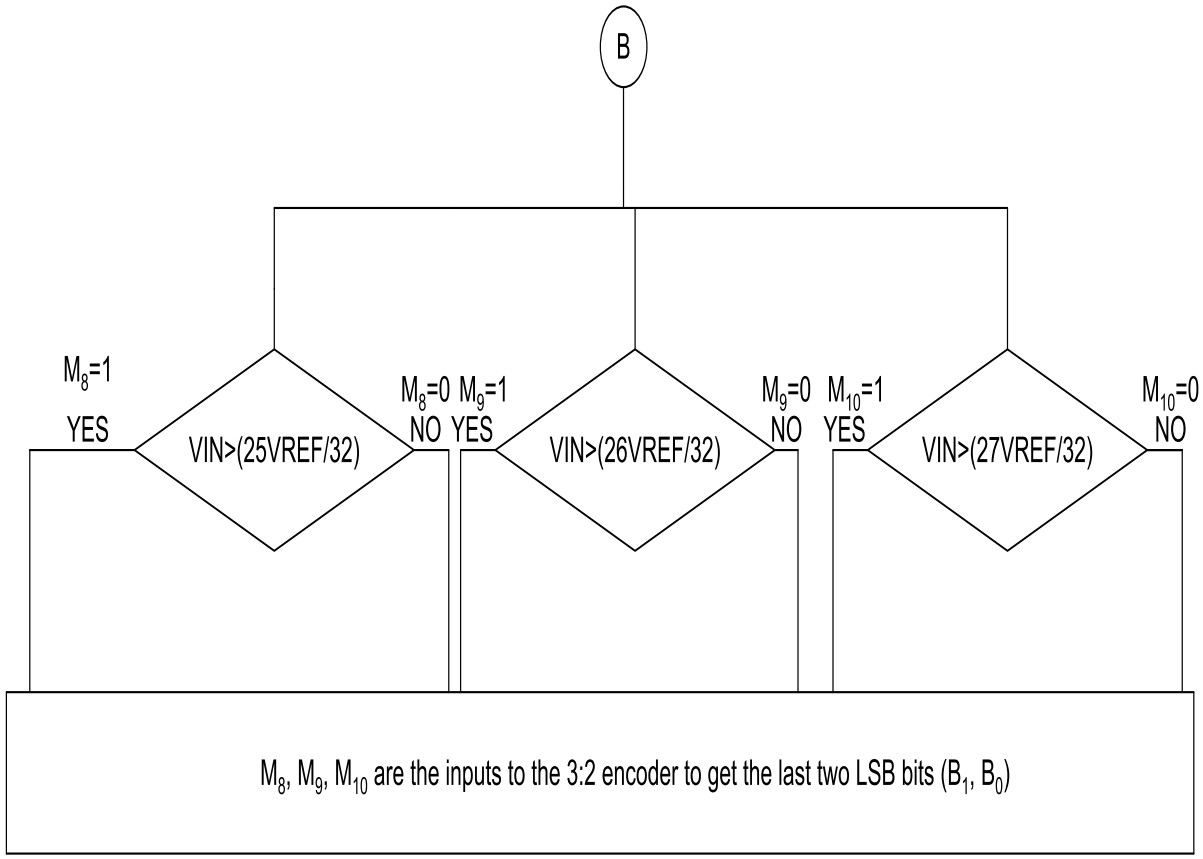
[3]. George Tom Varghese, K. K. Mahapatra," A Low Power Reconfigurable Encoder for Flash ADCs", *International Journal of Electronics Letters* (Taylor and Francis) (Communicated)

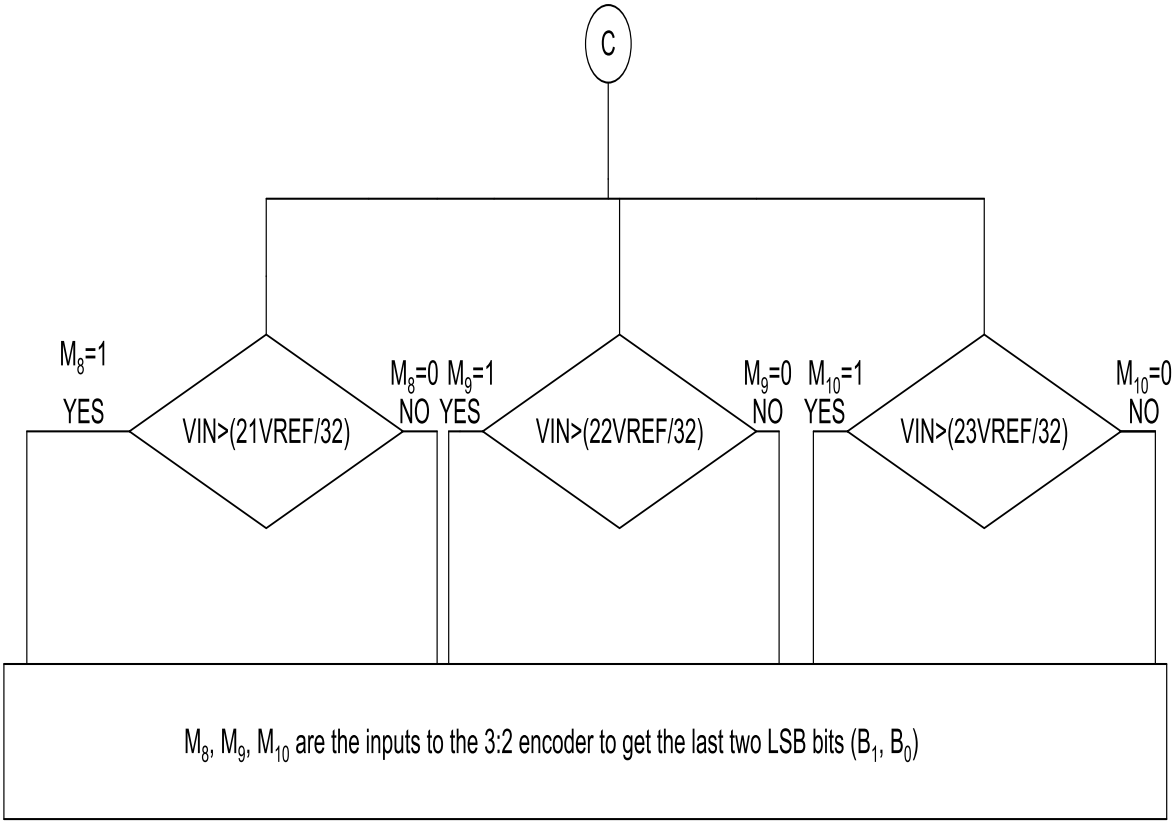
APPENDIX

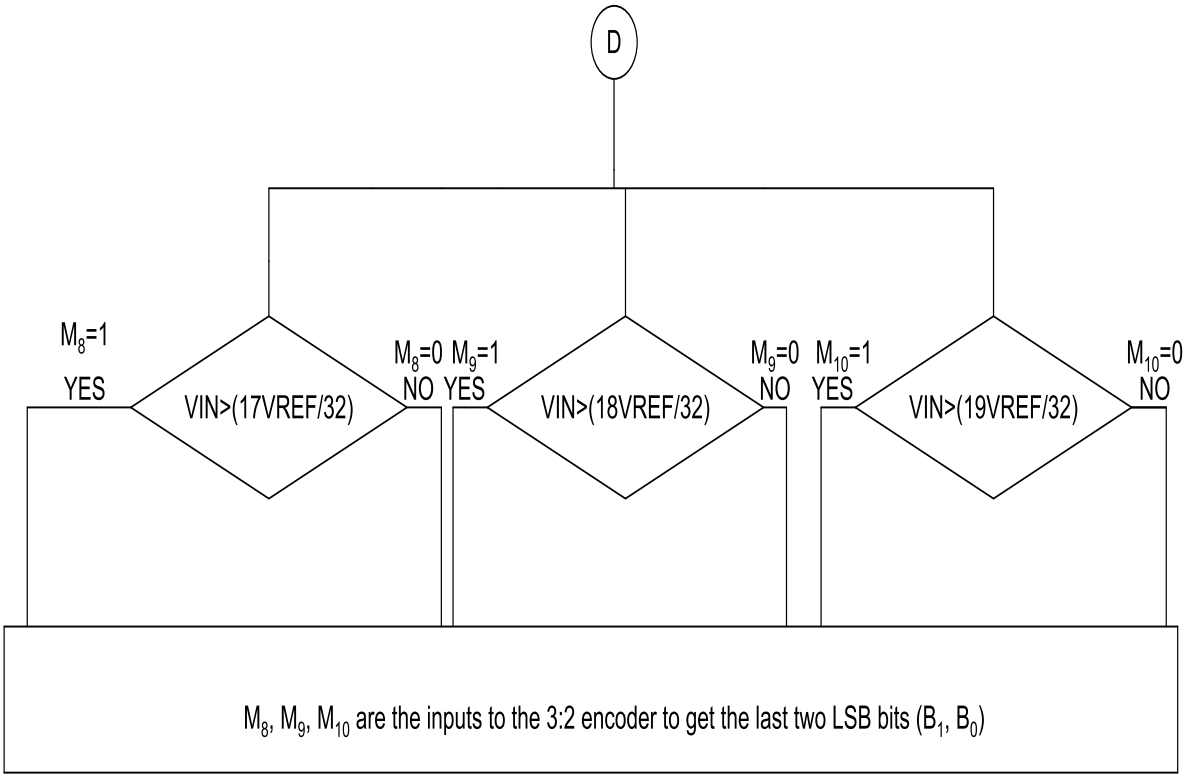
Reconfigurable flash ADC operation

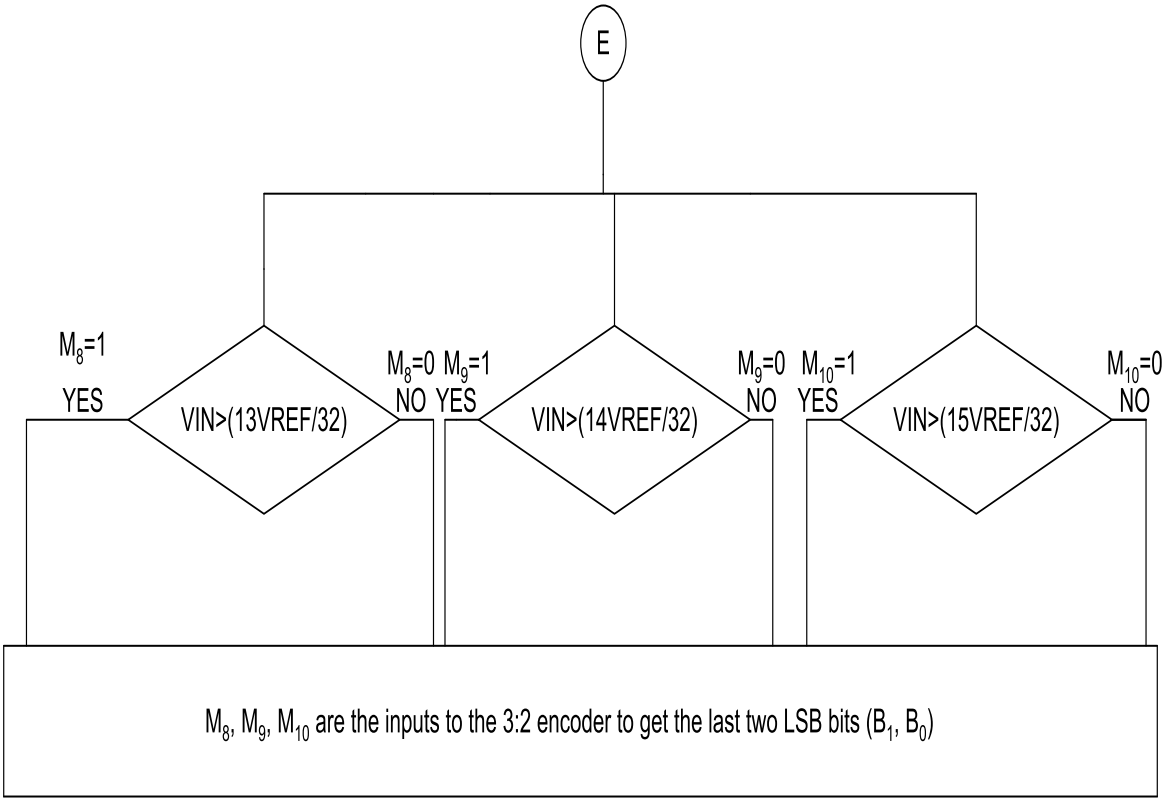


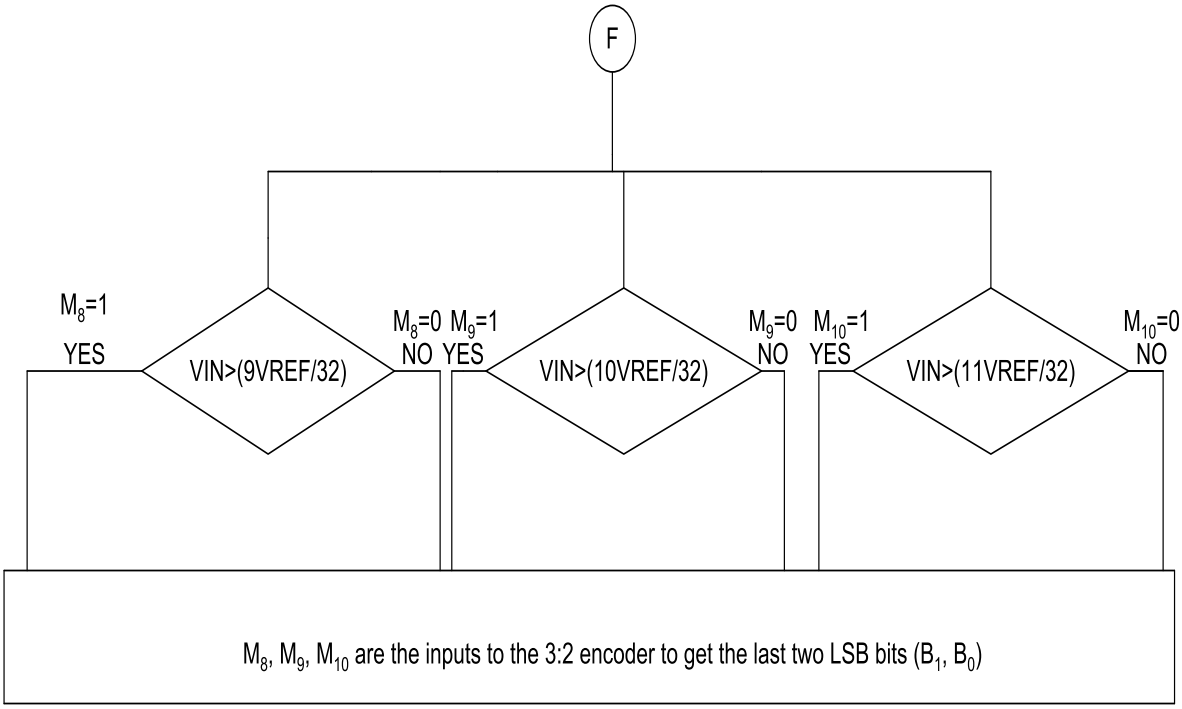

A
M8=1
YES
VIN>(29VREF/32)
M8=0
NO
M9=1
YES
VIN>(30VREF/32)
M9=0
NO
M10=1
YES
VIN>(31VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)

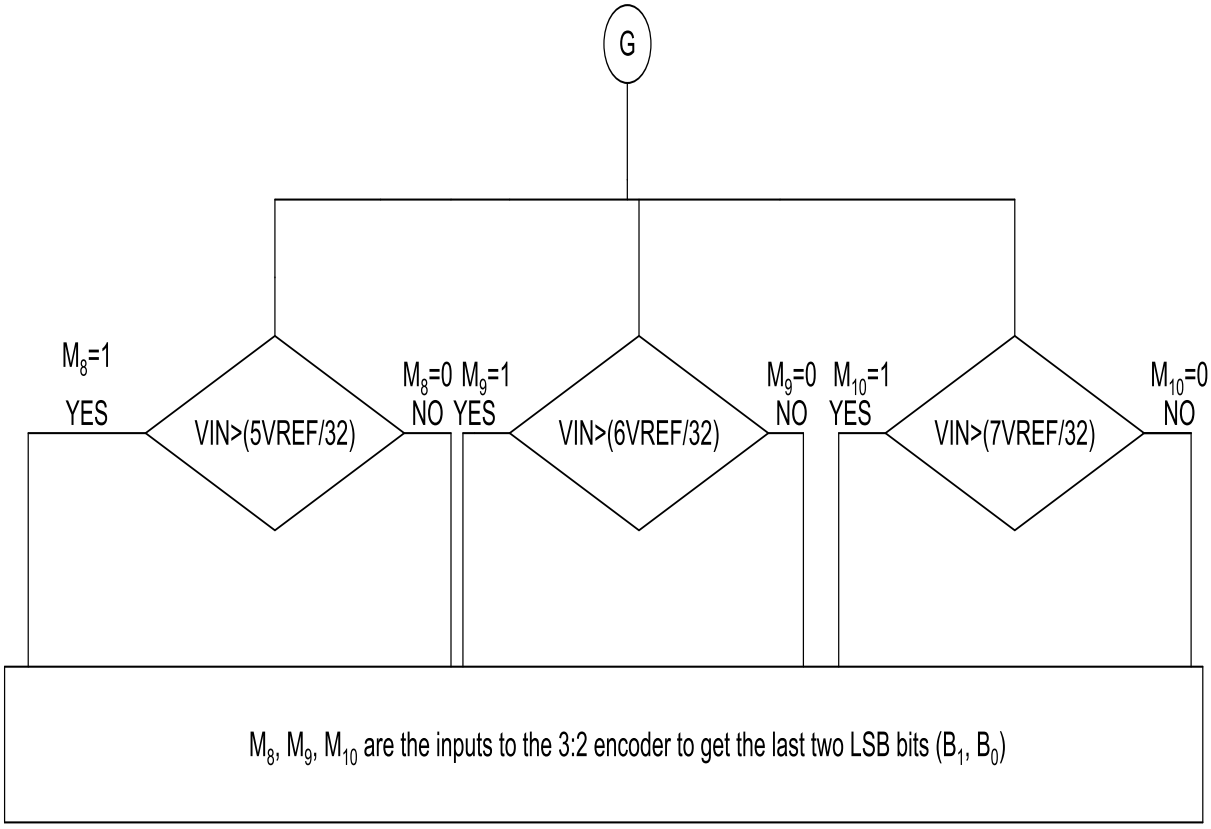

B
M8=1
YES
VIN>(25VREF/32)
M8=0
NO
M9=1
YES
VIN>(26VREF/32)
M9=0
NO
M10=1
YES
VIN>(27VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)

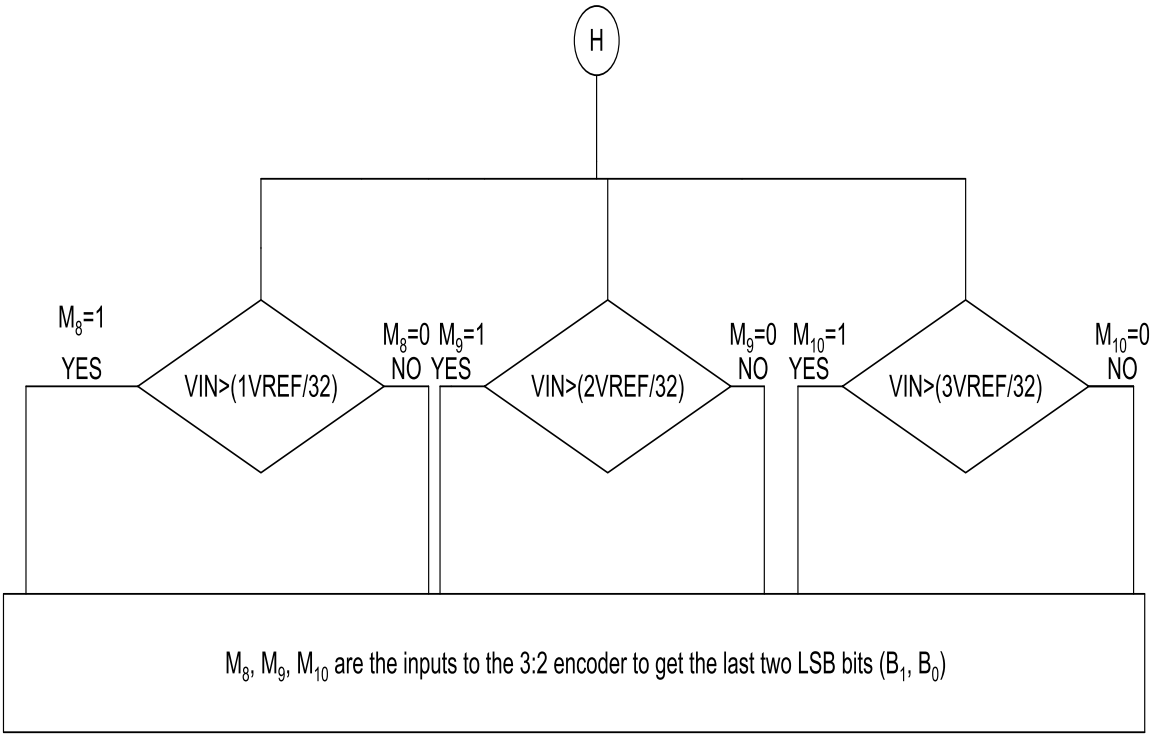

C
M8=1
YES
VIN>(21VREF/32)
M8=0
NO
M9=1
YES
VIN>(22VREF/32)
M9=0
NO
M10=1
YES
VIN>(23VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)


D
M8=1
YES
VIN>(17VREF/32)
M8=0
NO
M9=1
YES
VIN>(18VREF/32)
M9=0
NO
M10=1
YES
VIN>(19VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)


E
M8=1
YES
VIN>(13VREF/32)
M8=0
NO
M9=1
YES
VIN>(14VREF/32)
M9=0
NO
M10=1
YES
VIN>(15VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)


F
M8=1
YES
VIN>(9VREF/32)
M8=0
NO
M9=1
YES
VIN>(10VREF/32)
M9=0
NO
M10=1
YES
VIN>(11VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)


G
M8=1
YES
VIN>(5VREF/32)
M8=0
NO
M9=1
YES
VIN>(6VREF/32)
M9=0
NO
M10=1
YES
VIN>(7VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)


H
M8=1
YES
VIN>(1VREF/32)
M8=0
NO
M9=1
YES
VIN>(2VREF/32)
M9=0
NO
M10=1
YES
VIN>(3VREF/32)
M10=0
NO
M8, M9, M10 are the inputs to the 3:2 encoder to get the last two LSB bits (B1, B0)