Fast and Robust Design of CMOS VCO for Optimal Performance

Dissertation submitted in partial fulfillment of
the requirements for the award of
Doctor of Philosophy

by

PRAKASH KUMAR ROUT

Under the supervision of

Prof. (Dr.) D. P. Acharya
Prof. (Dr.) G. Panda

ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
ROURKELA
INDIA

"Dedicated to the Human Society"

ACKNOWLEDGEMENTS

I take this opportunity to express my reverence to my supervisors Prof. (Dr.) D. P. Acharya and Prof. (Dr.) G. Panda for their guidance, inspiration and innovative technical discussions all during the course of this work. I find words inadequate to thank them for enabling me to complete this work in spite of all obstacles.

I am also thankful to all faculty members and research students of ECE Department, NIT Rourkela. Special thanks go to Prof.(Dr.) K.K.Mohapatra, Prof.(Dr.) S.K.Patra and Prof.(Dr.) S.Meher for their constructive criticism and motivation during the course of my work.

I am thankful to Prof.A.K.Swain, Prof.A.K.Sahoo and Prof.U.K.Sahu for their support and help at times of need. It is my pleasure to show my indebtedness to my friends at NIT like Umakanta, Debasish, Dandpat Sir, Vijay Sharma, Tom, Sudheendra, Srinivas, Pallab, Soubhagya and Jagannath for their help during the course of this work.

I am also thankful to my colleagues at Silicon Institute of Technology, Bhubaneswar for their kind help and support at times of need.

I find words inadequate to express any form of acknowledgement to my father, mother, brothers and sisters who have been an emblem of blessings in all my steps of life.

(Prakash Kumar Rout)

TABLE OF CONTENTS

1. Introduction 1
1.1 Motivation 1
1.2 Scope of the Thesis 2
1.3 Structure and Chapter wise Contribution of the Thesis 3
1.4 List of Publications Related to Thesis 7
1.5 Summary of Publications Related to Thesis 9
2. Advances in Analog Integrated Circuit Optimization: A Brief Overview ... 13
2.1 Introduction 13
2.2 Analog IC Design Flow 14
2.3 Scope for Analog IC Design Optimization 17
2.4 Methodologies for Analog IC Optimization 20
2.5 Conclusion 29
3. Rapid Prototyping Methodology for High Performance Nano-CMOS VCO based on NSGA-II Optimization 31
3.1 Introduction 31
3.2 Design Objectives for the Nano-CMOS VCO 33
3.2.1 CMOS Ring Oscillator 33
3.2.2 Current Starved VCO 40
3.2.3 Differential VCO 41
3.3 NSGA – II Optimization Kernel 44
3.4 Design Flow of Energy Efficient Low Phase Noise CMOS Voltage Controlled Oscillator 47
3.5 Performance Analysis 49
3.6 Conclusion 63
4. IDEA Based Fast Design Methodology of Nano-CMOS VCO for Performance Optimization 65
4.1 Introduction 65
4.2 Infeasibility Driven Evolutionary Algorithm (IDEA) 66
4.3 IDEA based Parasitic Aware Design Methodology of VCO for Performance Optimization 69
4.4 Performance Analysis 72
4.4.1 CMOS Ring Oscillator 73
4.4.2 CMOS Current Starved VCO 77
4.4.3 Differential VCO 81
4.5 Conclusion 84
5. Process Variation Aware Fast Design of VCO with Performance Optimization 87
5.1 Introduction 87
5.2 Fabrication Process Variations 88
5.3 Fast Design Methodology for Optimized Parasitic and Process Variation Aware (PPVA) VCO 88
5.4 Performance Analysis 91
5.4.1 CMOS Ring Oscillator 91

5.4.2 CMOS Current Starved VCO 95
5.4.3 Differential VCO 100
5.5 Conclusion 105
6. Design of Robust Analog Integrated Circuit based on Process Corner Performance Variability Minimization 107
6.1 Introduction 107
6.2 Manufacturing Process Fluctuation Robust Design Methodology 109
6.3 Performance Analysis of the Proposed PCPVM based Robust Methodology 113
6.3.1 Current Starved VCO 113
6.3.2 Differential VCO 119
6.4 Conclusion 123
7. Conclusions and Scope for Future Research 125
7.1 General Conclusions 125
7.2 Scope for Future Research 126
References 129

LIST OF FIGURES

Figure 2. 1 Analog IC Design Performance Octagon 15
Figure 2. 2 Analog IC Design Flow 15
Figure 2. 3 The Manual Analog Circuit Design Process 18
Figure 2. 4 The Anaconda Synthesis Architecture 26
Figure 2. 5 Parasitic Aware Optimization 28

Figure 3. 1 General Structure of ring oscillator 34
Figure 3. 2 A five stage CMOS ring oscillator 34
Figure 3. 3 The Frequency Spectrum of an Ideal and Actual Oscillator 37
Figure 3. 4 The Phase Noise calculation per unit bandwidth 38
Figure 3. 5 A typical phase noise plot for a free running oscillator 38
Figure 3. 6 Circuit schematic of CSVCO 40
Figure 3. 7 A four-stage Differential Voltage Controlled Oscillator 41
Figure 3. 8 Circuit Schematic of the Delay Cell of Differential VCO 42
Figure 3. 9 Crowding distance calculation 45
Figure 3. 10 The NSGA – II Optimization Routine 47
Figure 3. 11 The Design Flow for Optimal CMOS VCO 48
Figure 3. 12 Pareto Curve of Phase Noise and Power Consumption for 5-stage Parasitic Aware Ring Oscillator 50
Figure 3. 13 Physical Layout of Parasitic Aware Five stage CMOS Ring Oscillator 51
Figure 3. 14 The Oscillations produced by Parasitic Aware Five stage CMOS Ring Oscillator 51
Figure 3. 15 Phase Noise plot for Parasitic Aware Five stage CMOS Ring Oscillator 52
Figure 3. 16 Power Estimation plot for Parasitic Aware Five stage CMOS Ring Oscillator 52
Figure 3. 17 Physical Layout of Parasitic Aware Seven stage CMOS Ring Oscillator 54
Figure 3. 18 The Oscillations produced by Parasitic Aware Seven Stage CMOS Ring Oscillator 54
Figure 3. 19 Phase Noise plot for Parasitic Aware Seven Stage CMOS Ring Oscillator 54
Figure 3. 20 Power Estimation plot for Parasitic Aware Seven Stage CMOS Ring Oscillator 55
Figure 3. 21 Physical Layout of Parasitic Aware Eleven stage CMOS Ring 56
Figure 3. 22 The Oscillations produced by Parasitic Aware Eleven Stage CMOS Ring Oscillator 56
Figure 3. 23 Phase Noise plot for Parasitic Aware Eleven Stage CMOS Ring Oscillator 56
Figure 3. 24 Power Estimation plot for Parasitic Aware Eleven stage CMOS Ring Oscillator 57

Figure 3. 25 Physical Layout of Parasitic Aware Thirteen Stage Current Starved VCO 58
Figure 3. 26 Oscillations generated from the Parasitic Aware Current Starved VCO 59
Figure 3. 27 Phase Noise Plot of the Parasitic Aware Current Starved VCO 59
Figure 3. 28 Power Consumption of the Parasitic Aware Current Starved VCO 59
Figure 3. 29 Physical Layout of Parasitic Aware CMOS DVCO 61
Figure 3. 30 Oscillations generated from the Parasitic Aware CMOS DVCO 61
Figure 3. 31 Phase Noise Plot of the Parasitic Aware CMOS DVCO 62
Figure 3. 32 Power Consumption of the Parasitic Aware CMOS DVCO 62

Figure 4. 1 The IDEA based Parasitic Aware VCO design flow 72
Figure 4. 2 Physical Layout of Five-Stage Parasitic Aware Ring Oscillator designed using IDEA 73
Figure 4. 3 Oscillations generated from the Five-Stage Parasitic Aware Ring Oscillator designed using IDEA 74
Figure 4. 4 Phase Noise plot of the Five-Stage Parasitic Aware Ring Oscillator designed using IDEA 74
Figure 4. 5 Power Estimation plot of the Five-Stage Parasitic Aware Ring Oscillator designed using IDEA 75
Figure 4. 6 Corner Analysis plots for Frequency, Phase Noise and Power of IDEA Optimized Five-Stage RO 76
Figure 4. 7 The optimized parasitic and process variation aware physical layout of 13 stage CSVCO 78
Figure 4. 8 Oscillations produced by Parasitic Aware CSVCO (IDEA based) 78
Figure 4. 9 Phase Noise plot for Parasitic Aware CSVCO (IDEA based) 79
Figure 4. 10 Power Estimation plot of the Parasitic Aware CSVCO (IDEA based) 79
Figure 4. 11 Corner analysis of the final Parasitic Aware CSVCO 80
Figure 4. 12 Physical Layout of the Parasitic Aware DVCO (IDEA based) 82
Figure 4. 13 Oscillations generated from the Parasitic Aware DVCO (IDEA based) 82
Figure 4. 14 Phase Noise plot of the Parasitic Aware DVCO (IDEA based) 82
Figure 4. 15 Power Estimation plot of the Parasitic Aware DVCO (IDEA based) 83
Figure 4. 16 Corner analysis plots for oscillations, frequency, power consumption and phase noise 83

Figure 5. 1 Design flow of IDEA based Parasitic and Process Variation Aware VCO 89
Figure 5. 2 Physical Layout of Parasitic & Process Variation Aware CMOS Ring Oscillator 92
Figure 5. 3 Oscillations generated from the Parasitic & Process Variation Aware CMOS Ring Oscillator 92
Figure 5. 4 Phase Noise Plot of the Parasitic & Process Variation Aware CMOS Ring Oscillator 92

Figure 5. 5 Power Consumption of the Parasitic & Process Variation Aware Optimal CMOS Ring Oscillator..... 93
Figure 5. 6 The manufacturing process corner variation analysis of waveform, frequency, phase noise and power of parasitic and process variation aware ring oscillator..... 94
Figure 5. 7 Physical Layout of the Optimized Parasitic and Process Variation Aware Thirteen-Stage CSVCO 96
Figure 5. 8 Oscillations produced by the Optimized Parasitic and Process Variation Aware CSVCO..... 96
Figure 5. 9 Phase Noise plot of the Optimized Parasitic and Process Variation Aware CSVCO 97
Figure 5. 10 Power estimation of the Optimized Parasitic and Process Variation Aware CSVCO..... 97
Figure 5. 11 Variation of oscillation frequency with control voltage of the Optimized Parasitic and Process Variation Aware CSVCO..... 98
Figure 5. 12 Corner analysis of the Parasitic and Process Variation Aware CSVCO 98
Figure 5. 13 Physical Layout of Parasitic & Process Variation Aware DVCO..... 101
Figure 5. 14 Oscillations generated from the Parasitic & Process Variation Aware DVCO 101
Figure 5. 15 Phase Noise plot of the Parasitic & Process Variation Aware DVCO 102
Figure 5. 16 Power Consumption of the Parasitic & Process Variation Aware DVCO 102
Figure 5. 17 Control Voltage versus Oscillation Frequency plot of the Parasitic & Process Variation Aware DVCO 103
Figure 5. 18 Corner Analysis plots for oscillations, frequency, power consumption and phase noise 104

Figure 6. 1 Fabrication Process Corner Performance Variability Minimization (PCPVM) landscape..... 111
Figure 6. 2 Physical Layout of Robust CSVCO 114
Figure 6. 3 Oscillations generated from the Robust CSVCO 115
Figure 6. 4 Phase Noise plot of the Robust CSVCO 115
Figure 6. 5 Power Consumption of the Robust CSVCO 116
Figure 6. 6 Oscillation Frequency of CSVCO for Conventional and Robust Designs 117
Figure 6. 7 Phase Noise of CSVCO for Conventional and Robust Designs..... 117
Figure 6. 8 Average Power Consumption of CSVCO for Conventional and Robust Designs..... 118
Figure 6. 9 Tuning Range plot of Robust CSVCO 118
Figure 6. 10 Physical Layout of the Robust Optimal DVCO 119
Figure 6. 11 Oscillations generated from the Robust DVCO 120
Figure 6. 12 Phase Noise plot of the Robust DVCO 120
Figure 6. 13 Power Consumption of the Robust DVCO 120

Figure 6. 14 Oscillation Frequency of DVCO for Conventional and Robust Designs 121
Figure 6. 15 Phase Noise of DVCO for Conventional and Robust Designs 121
Figure 6. 16 Average Power Consumption of DVCO for Conventional and Robust Designs 122
Figure 6. 17 Tuning Range plot of Robust DVCO.....123

LIST OF TABLES

Table 3. 1 Design Parameters for Five stage CMOS Ring Oscillator 51
Table 3. 2 Performance Summary of Five Stage CMOS Ring Oscillator 53
Table 3. 3 Design Parameters for Seven Stage CMOS RO 53
Table 3. 4 Performance Summary of Seven stage CMOS Ring Oscillator 55
Table 3. 5 Design Parameters for Eleven stage CMOS RO 55
Table 3. 6 Performance Summary of Eleven stage CMOS Ring Oscillator 57
Table 3. 7 Design parameters for CMOS CSVCO 58
Table 3. 8 Performance Summery of the Parasitic Aware CSVCO 60
Table 3. 9 Design Parameters for CMOS Differential VCO 60
Table 3. 10 Performance Summery of Parasitic Aware CMOS DVCO 63

Table 4. 1 Tuning Parameters of IDEA Algorithm 72
Table 4. 2 Design Parameters of IDEA Optimized Parasitic Aware Nano-CMOS Ring Oscillator 75
Table 4. 3 Performance Indices of Parasitic Aware IDEA Optimized Nano-CMOS Ring Oscillator 75
Table 4. 4 Comparison of Performance Parameters of Parasitic Aware Five-Stage RO 77
Table 4. 5 Design Parameters from IDEA Based Method 77
Table 4. 6 Performance Indices of Parasitic Aware Optimized Nano CMOS CSVCO 80
Table 4. 7 Comparison of Performance Parameters of CSVCO 80
Table 4. 8 Design Parameter of IDEA Optimized Nano-CMOS Differential VCO. 81
Table 4. 9 Performance Indices of Parasitic Inclusive IDEA Optimized Nano-CMOS Differential VCO 84
Table 4. 10 Comparison of Performance Parameters of Parasitic Aware DVCO ... 84

Table 5. 1 Design Parameters of Parasitic and Process Variation Aware CMOS RO 91
Table 5. 2 Performance Indices of Parasitic & Process Variation Aware Optimized Nano-CMOS Ring Oscillator 93
Table 5. 3 Summary of Process Corner Performance Analysis 93
Table 5. 4 Performance Summary of Energy Efficient Low Phase Noise Robust CMOS Ring Oscillator 94
Table 5. 5 Design Parameters of Parasitic and Process Variation Aware CSVCO .. 95
Table 5. 6 Final Optimized Performance Indices of PPVA CSVCO 96
Table 5. 7 Performance Summary and Comparison of PPVA CSVCO 99
Table 5. 8 Design Parameter of Optimized PPVA Nano-CMOS Differential VCO 100
Table 5. 9 Summary of the DVCO Design Environment 103

Table 5. 10 Performance Indices of Parasitic & Process Variation Inclusive Optimized Nano-CMOS Differential VCO.....104

Table 6. 1 Design Parameters of Robust CSVCO.....114
Table 6. 2 Performance Parameters of Optimized Robust Nano-CMOS CSVCO..116
Table 6. 3 Design Parameters of Optimized Robust Nano-CMOS DVCO.....119
Table 6. 4 Performance Parameters of Optimized Robust Nano-CMOS DVCO....121

ACRONYMS

ADE	Analog Design Environment
ASIC	Application Specific Integrated Circuit
BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CSVCO	Current Starved Voltage Controlled Oscillator
DE	Differential Evolution
DVCO	Differential Voltage Controlled Oscillator
FPAA	Field Programmable Analog Array
FPGA	Field Programmable Gate Array
GA	Genetic Algorithm
GPDK	Generic Process Design Kit
IC	Integrated Circuit
IDEA	Infeasibility Driven Evolutionary Algorithm
ISM	Industrial Scientific and Medical
NSGA-II	Non-dominated Sorting Genetic Algorithm-II
PCPV	Process Corner Performance Variation
PCPVM	Process Corner Performance Variability Minimization
PLL	Phase Locked Loop
PSO	Particle Swarm Optimization
PSRR	Power Supply Rejection Ratio
RFIC	Radio Frequency Integrated Circuit
RO	Ring Oscillator
SA	Simulated Annealing
SoC	System on Chip
SPICE	Simulation Program for Integrated Circuit Emphasis
SQP	Sequential Quadratic Programming
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Network

ABSTRACT

The exponentially growing design complexity with technological advancement calls for a large scope in the analog and mixed signal integrated circuit design automation. In the automation process, performance optimization under different environmental constraints is of prime importance. The analog integrated circuits design strongly requires addressing multiple competing performance objectives for optimization with ability to find global solutions in a constrained environment. The integrated circuit (IC) performances are significantly affected by the device, interconnect and package parasitics. Inclusion of circuit parasitics in the design phase along with performance optimization has become a bare necessity for faster prototyping. Besides this, the fabrication process variations have a predominant effect on the circuit performance, which is directly linked to the acceptability of manufactured integrated circuit chips. This necessitates a manufacturing process tolerant design.

The development of analog IC design methods exploiting the computational intelligence of evolutionary techniques for optimization, integrating the circuit parasitic in the design optimization process in a more meaningful way and developing process fluctuation tolerant optimal design is the central theme of this thesis. Evolutionary computing multi-objective optimization techniques such as Non-dominated Sorting Genetic Algorithm-II and Infeasibility Driven Evolutionary Algorithm are used in this thesis for the development of parasitic aware design techniques for analog ICs. The realistic physical and process constraints are integrated in the proposed design technique.

A fast design methodology based on one of the efficient optimization technique is developed and an extensive worst case process variation analysis is performed. This work also presents a novel process corner variation aware analog IC design methodology, which would effectively increase the yield of chips in the acceptable performance window. The performance of all the presented techniques is demonstrated through the application to CMOS ring oscillators, current starved and

differential voltage controlled oscillators, designed in Cadence Virtuoso Analog Design Environment.

Introduction

1.1 Motivation

The persistent miniaturization in electronics industry, with special emphasis to production of complex mixed-signal systems-on-chip (SoC), is highly dominated by nano-scale effects. Besides the ever growing demand for superior performance, the industry is driven by three main dynamics, time-to-market, productivity, and managing complexity. With faster technological advancements, the designers face exponentially growing complexity, which affects the performance and productivity. The analog and mixed-signal system design automation has immense scope for developments in divergent dimensions.

In a system, though the analog circuits occupy very less space but they require more design time than the digital circuits. This is due to the fact that the number of performance measures of an analog circuit is more than those of digital circuits. Besides this the analog circuit performances are highly sensitive to the design parameters and the fluctuations in the design and fabrication environment. Predicting and improving the performance, robustness and overall cost of such systems is a major concern in the process of automation. In the automation process, optimization of performances subjected to a verity of environmental constraints is the central task.

After the schematic capture of an analog circuit, the physical circuits are designed by drawing their geometrical layouts. The device, interconnects and package parasitics have significant effects on the circuit performances. Hence while doing circuit sizing for performance optimization, the circuit parasitics need to be included in the design technique. The fabrication process variations also have a predominant effect on the performance of circuits even on the same wafer. The randomness involved in fabrication is a cause for rejecting a chip owing to its unacceptable performance degradation. This calls for a design methodology, which is manufacturing process variation tolerant.

Though several efficient analog circuit-sizing techniques for optimal performance have been reported in literature, they find scopes for improvements in following dimensions.

Optimization of Multiple Performance Objectives:

The optimization techniques used for analog circuit design so far, are conventional like gradient based or evolutionary in nature. Addressing multiple competing objectives for optimization with ability to find global solutions in the constrained environment is a strong requirement to improve the analog IC performance. Naturally, the use of new optimization techniques suitable for such applications would yield performance close to the real optimum values.

Parasitic Aware Design using Efficient Optimization:

Many efforts have been reported to make analog IC design parasitic aware but there exists better ways to integrate the optimization algorithms for inclusion of realistic circuit parasitics generated from an initially optimized circuit.

Fabrication Process Variation Tolerant Design:

In literature, most of the designs are claimed to be process variation aware but they mostly check for the worst-case conditions for their optimal performance. These methods need to be someway or other modified to minimize the effect of process variations on nominal case so that the yield is improved.

1.2 Scope of the Thesis

This thesis was born out of the need to develop analog IC design methods which exploit the computational intelligence of evolutionary techniques, integrate the circuit parasitics in the design optimization process in a more meaningful way and develop fabrication process variation tolerant design for performance optimization. Hence, the followings are outlined as the scope of this thesis.

1. To develop novel methods for analog integrated circuit design using efficient multi-objective evolutionary computation techniques. The use of evolutionary computation based optimizations explores the design space by

considering all the constraints. This also ensures the convergence of the algorithm to a good approximation to the global optimum in an acceptable computation time.

2. To develop better methodologies which include more realistic circuit parasitics in the optimization algorithms that is expected to arrive at near optimal performances of the IC.

3. To develop a methodology with fast design cycle based on one of the efficient optimization techniques and carry out an extensive worst case process variation analysis.

4. To come out with a method which can be designated as true process corner variation aware analog IC design methodology. Unlike many other cases, where only worst case analyses are reported, in this work a novel methodology is developed for design of analog IC which would increases the number of chips in the acceptable performance window.

5. The performance of all the techniques reported in the thesis are demonstrated for the design of different CMOS voltage controlled oscillator circuits.

The structure and chapter wise contributions of the proposed thesis are detailed below.

1.3 Structure and Chapter wise Contribution of the Thesis

Chapter-I

Introduction

The motivation behind the analog integrated circuit optimization problem is introduced. The reported work on this topic is reviewed in this chapter. The summary of the contributions is also outlined.

Chapter-II

Advances in Analog Integrated Circuit Optimization: A Brief Overview

In this chapter the basic philosophy behind the analog integrated circuit optimization is discussed. The role and abilities of various optimization techniques are outlined. The applications of optimization algorithms to different analog/mixed signal integrated circuits as have been reported are presented. Varieties of analog IC design automation tools with their capabilities are described. The works reported till date on these areas are extensively reviewed.

Chapter-III

Rapid Prototyping Methodology for High Performance Nano-CMOS VCO based on NSGA-II Optimization

A fast prototyping methodology which uses NSGA-II based performance optimization is proposed in this chapter and applied to CMOS VCO circuits. This technique finds the design parameters in a single run and hence the time to design the first prototype is greatly reduced. The CMOS voltage controlled oscillators are considered here for optimization of phase noise and power consumption with a goal to achieve a targeted frequency of oscillation in a technology constrained environment. Acceptably manageable model equations which include the parasitic are considered as optimization objectives. The design parameters obtained from the multi-objective constrained optimization NSGA-II technique are used to perform a schematic and physical layout level CMOS voltage controlled oscillator design in the Cadence Virtuoso Analog Design Environment. Since the methodology is newly applied to CMOS VCOs, to the best of our knowledge there is no other benchmark result available for direct comparison. Hence for the demonstration of the methodology, the circuit performance parameters are estimated from the transient and noise analysis in Cadence Virtuoso analog design tool and are compared with their predicted optimal values. The circuits considered here are CMOS ring

oscillators with different number of stages, current starved voltage controlled oscillator (CSVCO) and differential voltage controlled oscillator (DVCO).

Chapter-IV

IDEA Based Fast Design Methodology of Nano-CMOS VCO for Performance Optimization

There has been a continuous strive towards development of more efficient computationally intelligent algorithms. Though NSGA-II is a standard multi-objective optimization algorithm, still a better technique available would be an obvious choice among the designers. Infeasibility driven evolutionary algorithm (IDEA) is a recently developed multi-objective optimization algorithm, which has been reported to offer superior performance. Inspired by Moore's law, integrated circuits always need to offer better performance. Under such a situation more efficient optimization technique like IDEA come as a rescue to the designers' burden of achieving a better performance in a given process technology. Therefore, here IDEA is employed as a multi-objective optimization technique for the design of CMOS VCO circuit. This chapter is similar to the previous one except that the new technique IDEA enables the designer to produce the ICs with higher indices of performance measures. The design is also parasitic aware and works within various process constraints.

Chapter-V

Process Variation Aware Fast Design of VCO with Performance Optimization

In the manufacturing process of ICs there are variations in different parameters which are not under the control the designer. With the device dimensions shrinking down to nano-scale regime the IC fabrication uncertainties influence greatly their performance. This leads to increase in non performing ICs in a batch of production and hence the yield in the fabrication process is reduced. If the process variation

extremities can be taken care in the design phase itself then the number of ICs whose performance is outside the expected performance boundaries can be greatly reduced.

Along with the parasitic aware optimization using IDEA, the design is subjected to the worst case process variations. This proposed technique is validated through examples of CMOS ring oscillator, current starved voltage controlled oscillator and differential voltage controlled oscillator. Though the methodology is applied to VCOs, it can be extended for optimal design of any RFIC with multiple performance objectives including practical constraints.

Chapter-VI

Design of Robust Analog Integrated Circuit based on Process Corner Performance Variability Minimization

One novel practical approach of performance optimization along with fabrication process fluctuations tolerance of integrated circuits is proposed in this chapter. It is well known that the probability of having chip being manufactured under normal process environment is higher than the other corner process environments since it follows a Gaussian distribution. In this proposed approach process corner performance variability minimization (PCPVM) is carried out simultaneously with performance optimization. In PCPVM the statistical performance deviations of the corner cases from the nominal case is minimized by considering the actual SPICE parameters of different process corners for evaluation of performance. The design proposed here is robust by optimizing the circuit performance in the nominal case and also minimizing the difference between chip performance in normal and worst case corner environments. This approach is expected to improve the performance of the ICs manufactured even under extreme process corner conditions.

Chapter-VII

Conclusions and Future Work

The overall contributions of the thesis are listed with reference to their limitations. The scope for future research activities is also outlined.

1.4 List of Publications Related to Thesis

Published/Accepted:

Journals:

[P 1] P.K.Rout, D.P.Acharya and G.Panda, "A Multi-Objective Optimization Based Fast and Robust Design Methodology for Low Power and Low Phase Noise Current Starved VCO", *IEEE Trans. On Semiconductor Manufacturing*, vol.27, no.1, pp.43-50, Feb.2014.

[P 2] P.K.Rout, D.P.Acharya and G.Panda, "Design of Optimal Nano-CMOS Differential VCO for RF Applications", *International Journal of Circuits and Architecture Design, Inderscience Publishers (In Press).*

Conferences:

[P 3] P.K.Rout, D.P.Acharya and G.Panda, "Constrained Multiobjective Optimization based Design of CMOS Ring Oscillator", *International Conference on Computer Communication and Informatics (ICCCI -2014), Jan. 03 – 05, 2014, Coimbatore, INDIA.*

[P 4] P.K.Rout, D.P.Acharya, G.Panda and D.Nayak, "Process Corner Variation Aware Design of Low Power Current Starved VCO", *IEEE International Conference on Electronics and Communication System (ICECS-2014), Feb. 2014.*

[P 5] P.K.Rout, D.P.Acharya and G.Panda, "IDEA Based Robust Design of High Performance Current Starved VCO," *The Asia-Pacific Conference on Postgraduate Research in Microelectronics & Electronics (Prime Asia) 2013*

Communicated:

1. P.K.Rout, D.P.Acharya and G.Panda, "Design of Robust Analog Integrated Circuit based on Process Corner Performance Variability Minimization," Communicated to *IEEE Trans. on Semiconductor Manufacturing*.

2. P.K.Rout, D.P.Acharya and G.Panda, "Fast Physical Design of CMOS VCOs for Optimal Performances using Constrained NSGA-II," Communicated to *Microelectronics Journal, Elsevier.*

1.5 Summary of Publications Related to Thesis

[P 1] This paper presents a novel design methodology for design of optimal and robust current starved voltage controlled oscillator (CSVCO) circuit. A recently developed multi-objective optimization technique infeasibility driven evolutionary algorithm (IDEA) is used to minimize the power and the phase noise of the circuit at its schematic and physical level. The multi-objective optimization is carried out by taking into account the extracted parasitics that would be present in the physical integrated circuit and the random variations of parameters during fabrication in foundry. The method would help the designer in semiconductor industry by effectively reducing several time-consuming design iterations to a single iteration ensuring the near optimal performance of the CSVCO. The performance of the circuit is validated by carrying out simulations for transient and noise analysis in Cadence tools using 90nm 1P 9M CMOS process.

[P 2] In the design of radio frequency (RF) circuits, fast prototyping with optimal performance is a challenging task for designers. The noise consideration in the differential voltage controlled oscillator (DVCO) is very much vital in its design. The present work focuses on the design of low phase noise and low power robust nano-CMOS differential voltage controlled oscillator (DVCO) for a desired frequency of oscillation 2.4 GHz. Constrained multi-objective optimization, infeasibility driven evolutionary algorithm (IDEA) is used to minimize the phase noise and power consumption simultaneously. In this work, the phase noise is formulated to inherently account for the flicker noise along with the thermal noise and optimized along with power consumption by IDEA. The optimal performing circuit is synthesized using GPDK-90 nm 1P 9M process library. The frequency of oscillation obtained in the parasitic inclusive design of the differential VCO is 2.39951 GHz, which is in good agreement with the target frequency with negligible deviation and the corresponding optimum values of

power consumption and phase noise recorded are 845.5095 μW and 79.67 dBc/Hz at 1 MHz offset, respectively.

[P 3] In this paper a popular multiobjective optimization Non-dominated Sorting Genetic Algorithm (NSGA-II) based integrated circuit design methodology using simple equation models is presented. The method is applied to CMOS ring oscillator circuit where the design parameters are estimated so that the circuit offers optimal performance. The circuit is designed using these parameters in Cadence Virtuoso Analog Design Environment (ADE) with GPDK 90nm process to test the predicted performance. The proposed method saves the design cycle time ensuring the optimal performance of the CMOS ring oscillator in a constrained environment.

[P 4] Conventionally the integrated circuit designer first carries out the design to achieve the required performance specifications and observes the worst case performance through simulations. If the worst case performance falls well inside the acceptable range then that design is designated as a process variation tolerant design. In such case the design is not truly robust against actual process variations. The randomness of process variations is hardly included in the design phase to minimize their effects on the performance of the fabricated chips. In the present work a novel approach is proposed which minimizes the process corner performance variation (PCPV) so that the performances of the extreme corner case chips are very close the nominal fabrication case. The nominal case design is also subjected to performance optimization along with the process corner variability. Evolutionary algorithm is suitably employed for simultaneous optimization of all the objectives. The proposed design technique is applied to a CSVCO circuit as a case study and the performance improvement results of Cadence simulation are reported.

[P 5] A new methodology for design of optimal and high performance current starved voltage controlled oscillator (CSVCO) circuit is presented here. A recently developed multi-objective optimization technique infeasibility driven evolutionary algorithm (IDEA) is used to minimize the power and the phase noise of the circuit at its schematic level. The method helps the designer in

semiconductor industry by effectively reducing several time-consuming design iterations to a single iteration ensuring the near best performance of the CSVCO. The performance of the circuit is validated by carrying out simulations for transient and noise analysis in Cadence tools using 90nm 1P 9M CMOS process.

Advances in Analog Integrated Circuit Optimization: A Brief Overview

2.1 Introduction

Advances in semiconductor manufacturing technology have resulted in ultra large scale integration (ULSI) of circuits. The complex system-on-chip contains mixed digital and analog circuits. Although analog circuits occupy a small fraction of silicon area but it is highly difficult to design these circuits due to their complexity, noise sensitivity and performance tradeoffs. It is worth noting that the real world is analog and the analog signals need to be processed in integrated circuits (IC). Whatever may be the advancements in digital IC designs the performance of the system is always dictated by the analog part of the integrated circuit. Without automation and optimization the analog IC design suffers from long design time, high complexity, high cost and suboptimal performance. It is no wonder that building efficient analog integrated circuits is said to involve some amount of black magic. Because of this, analog design requires skilled craftsmen who are in short supply. The average analog circuit takes longer to implement than it's usually much larger digital counterpart. Problems multiply if the analog design is destined to be a block on a mixed-signal or system chip. Hence there have been great efforts not only for design automation but for performance optimization too. When automation helps in handling the design complexity, optimization helps to attain near-best performance in a very less time, which can be accomplished by acceptably moderate skilled designers. Here optimization techniques and their applications to analog integrated circuits are reviewed.

The major building blocks of the analog circuits are operational amplifiers, filters, oscillators, low noise amplifiers, power amplifiers and current and voltage sources. The optimization techniques are generally applied to these circuits to estimate their design parameters for obtaining best possible performance. Many

researchers designate this process as circuit sizing. This has two major purposes: first it replaces cumbersome and ad hoc manual tradeoffs by automatic evaluation of design parameters, second, it solves problems, which are difficult for hand design. Moreover, the optimization algorithms also take into account the constraints in the design space.

The organization of this chapter is as follows. Section 2.2 provides a bird's view on the analog IC design flow. The scope for various optimizations therein is described in section 2.3. The conventional and evolutionary technique based analog IC optimizations are discussed in section 2.4. Finally, section 2.5 provides the summary and concluding remarks.

2.2 Analog IC Design Flow

2.2.1 The Complexity of the Analog IC Design

The parameters of analog integrated circuits are very much detrimental in the system performance. The specification contains requirements on the various performance metrics of the circuit. Here the performance metric are measures of properties that are used to characterize the behavior of an analog IC. For example, an amplifier is characterized by gain, speed, power consumption, linearity and the like. All these performance metrics are very often competing in nature and hence present challenging tradeoffs in the design. This is represented as a generic analog design octagon, which is illustrated in Figure 2.1. An IC designer always desires to achieve the best in terms of these performance indices. However, while achieving one performance the other may tend to deteriorate which is designated as trade off in design.

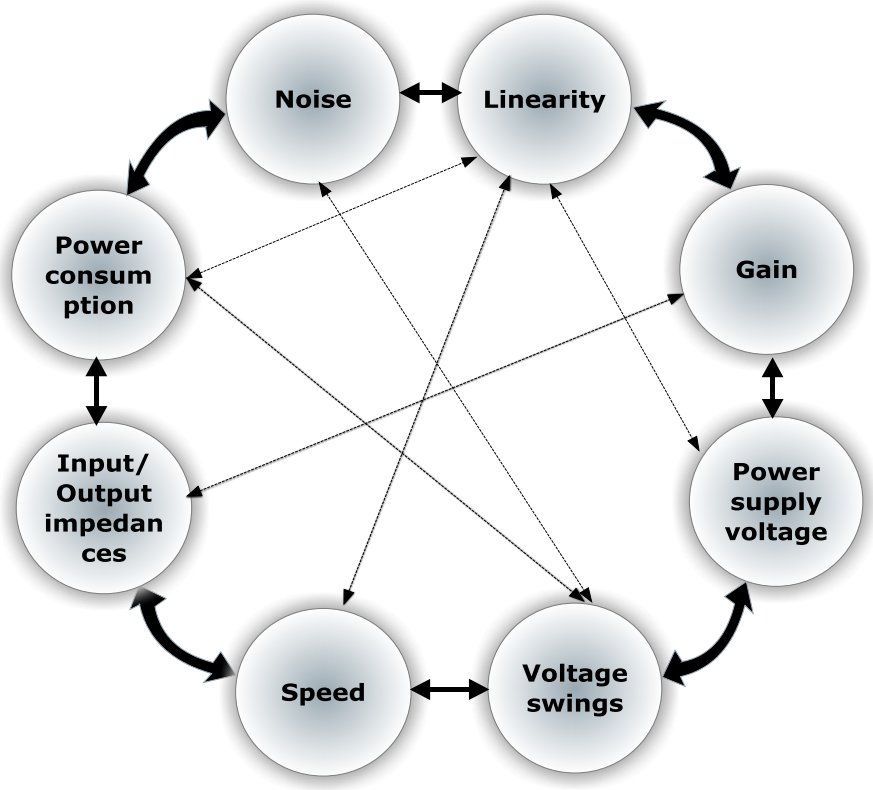

Figure 2. 1 Analog IC Design Performance Octagon

2.2.2 The Analog IC Design Process

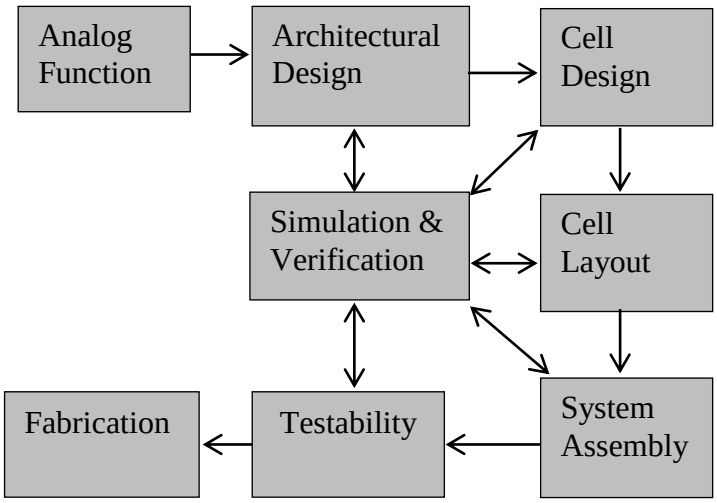

Figure 2. 2 Analog IC Design Flow

The analog design starts with the specifications and the functionality to be implemented which is mapped onto an architectural description for the design. In this process, the decomposition of the required function is carried out until we arrive at easily manageable analog building modules or blocks, usually called as cells. High-level models are used to perform simulations to validate the functionality of the concept. The specifications on the low-level modules or cells are extracted from these simulations. The cells are realized by designing the low-level building blocks, which comply with the performance requirements. After the physical design of all the required cells the analog system is assembled. The assembled system layout is released for fabrication. The post fabrication testing and verification confirms the release of the product prototype for field deployment. This flow of analog IC design is depicted in Figure 2.2.

The design of an analog cell first involves the choice of possible topology to implement the functionality in an efficient way. The next step design process (Figure 2.3) is the circuit sizing. Generally, an analog circuit has many real-valued parameters, which must be set to meet its specifications. The process of setting these parameters is called circuit sizing. For instance, a two-stage opamp has around twelve parameters including the width and length of all transistors and passive component values which have to be set to achieve the specifications such as gain, bandwidth, power, area, noise, CMMR (common mode rejection ratio), offset, settling time, slew rate and PSRR (power supply rejection ratio). The simulation experiments are carried out iteratively until the specifications are met. With these circuit parameter values, the physical layout of the circuit is designed and the circuit parasitics are extracted. The simulation studies and performance evaluation of the circuit are performed by considering these extracted parasitics. The circuit layout is iteratively redrawn until acceptable performance values are obtained.

Throughout the design process, many simulations and validation steps are required. If the circuit fails to meet the specification at some level, the preceding design steps must be revised. This may include back annotating several steps in the design process.

2.3 Scope for Analog IC Design Optimization

A close look at the analog design hexagon reveals that it is highly desirable for the multiple performance objectives to be simultaneously optimized. In analog and mixed-signal systems very often, one uses a single objective function, which is a weighted combination of all objectives or the multi objective method.

2.3.1 Circuit Sizing

In the recent past, circuit sizing has been projected as an optimization problem. This optimization problem has two dimensions: modeling the design problem as an optimization problem and solving the modeled problem. These steps are interdependent and influence each other, for instance, the model of the problem will decide the optimization method that can be used.

The most accurate performance of integrated circuits is measured with the chip fabricated on silicon. Due to the non-availability of the chip, during the design process, the designer uses a simulation engine, which models the characteristics of the silicon elements and runs computational algorithms to estimate the performance of the IC. SPICE is the industry standard widely accepted simulator. Hence, the correctness of SPICE is the final validation-point in the circuit-sizing problem. The highest precision model for optimization uses SPICE as a black-box estimator to which one gives the circuit parameters and gets the IC performance specifications.

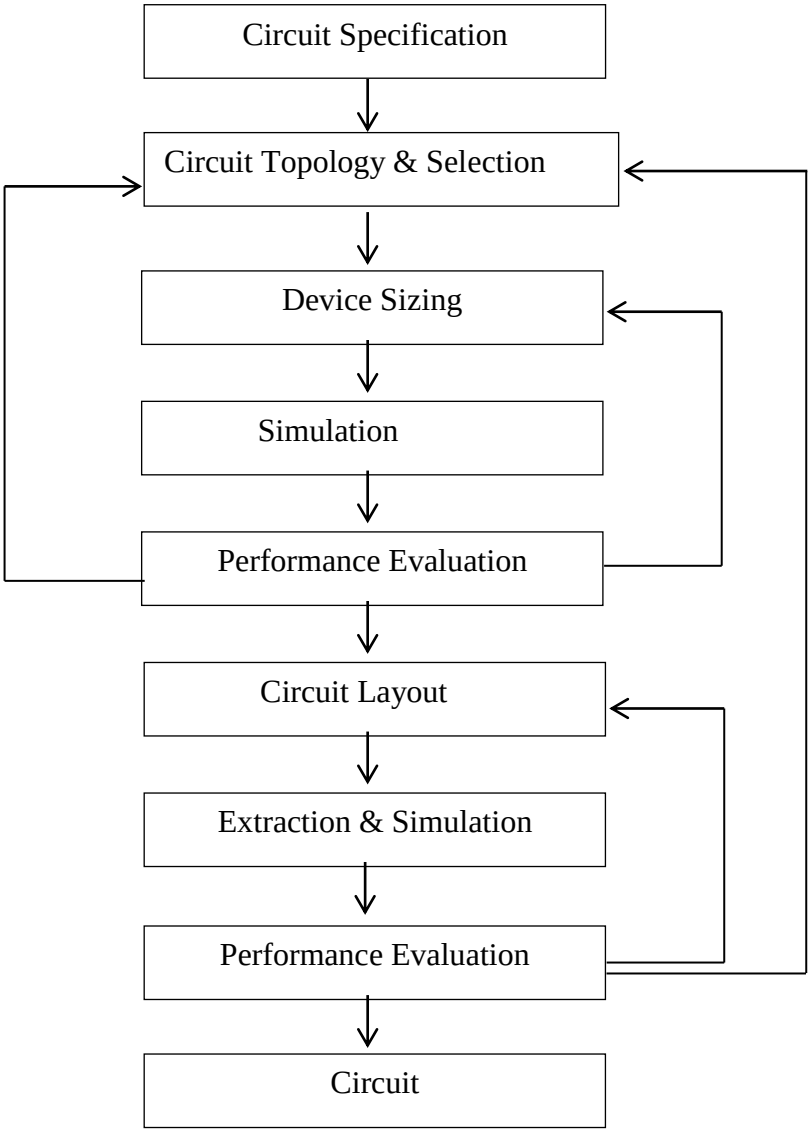

Figure 2. 3 The Manual Analog Circuit Design Process

Besides this, the designer has access to the governing equations describing the IC behavior. These equations are derived from nodal current and voltage expressions in the circuit with certain assumptions on the transistor behavior. The circuit performances are derived from these equations much faster than SPICE. But their accuracy is less than the SPICE, due to the approximated transistor behavior and approximations made in circuit analysis.

The above two models i.e. SPICE based and equation based models evaluate the IC performance specifications.

2.3.2 Physical Layout Design

In the design process soon after the circuit sizing, the physical layout of the IC is designed. This involves drawing of the geometrical structures of all circuit elements like transistor, diode, resistor, capacitor and inductor and the metal layers for interconnects. For a given requirement, there is a possibility of many geometries from which the geometry offering the optimal performance needs to be selected. In addition to this, the placement of the components and the routing of their interconnects has immense requirements for optimization.

In the layout design phase, the effect of actual circuit parasitics surfaces. These parasitics have a significant impact on the performance, which needs to be included in the process of all optimizations. This is popularly known as parasitic aware optimization. The basic principle behind the parasitic-aware optimization technique is that device and package parasitics are considered as a natural part of the design process from the beginning of the overall design cycle. When all parasitic effects are taken into account, the complete circuit becomes highly complicated for hand analysis, even with help of circuit simulators, so finding the optimum solution is nearly impossible.

2.3.3 Process Variations

The integrated circuits should be designed in such a way that the manufactured ICs must meet the performance specifications under all operating conditions. The random fluctuations in the fabrication process results in the deviation of the performance. Besides this, the variations in the operating conditions like supply voltage and temperature affect the IC performance. These performance deviations reduce the yield significantly and hence the chip unit cost increases. Therefore, one of the major design objectives is to minimize the impact of process variations on the chip performance. This calls for a process variation tolerant IC design methodology.

2.4 Methodologies for Analog IC Optimization

Apart from the performance specification measurement during simulation, the use of optimization engine and setting up the optimization problem also has a great impact on the final IC performance. Optimization is concerned with the finding of minima and maxima of functions, subject to many process and other real constraints. There is no single method available for solving all optimization problems efficiently. Hence a number of optimization methods have been developed for solving different types of optimization problems.

To solve problems, people use algorithms that terminate in a finite number of steps, or iterative methods that converge to a solution (on some specified class of problems), or heuristics that may provide approximate solutions to some problems (although their iterates need not converge).The popular optimization techniques are direct search method, Newton's method, conjugate gradient method, gradient descent method, simplex method [1], neural networks [2] and the like. The gradient based techniques most often get trapped in local optima. Apart from this the non-quadratic non-differentiable functions find difficulty in the above mentioned techniques. In such cases heuristic algorithms like Simulated Annealing [3] [4], Genetic Algorithms [5], Particle Swarm Optimization [6], Differential Evolution [7], Artificial Bee Colony Optimization [8], Bacteria Foraging Optimization [9] and many hybrids of these are capable of approximate global optimal solutions. These heuristics are also known as the Evolutionary Algorithms.

Optimization problems are many times multi-modal i.e. they possess multiple good solutions. They could all be globally good (same cost function value) or there could be a mix of globally good and locally good solutions. Obtaining all (or at least some of) the multiple solutions is the goal of a multi-modal optimizer.

Classical optimization techniques due to their iterative approach do not perform satisfactorily when they are used to obtain multiple solutions, since it is not guaranteed that different solutions will be obtained even with different starting points in multiple runs of the algorithm. Evolutionary Algorithms are however very popular approaches to obtain multiple solutions in a multi-modal optimization task.

There could be many variations to this such as the optimization problem can have multiple objectives and multiple constraints; one objective and multiple constraints; a series of optimization problems with one objective and multiple constraints.

The optimization complexity is increased when more than one objective is added to the problem. The set of trade-off designs that cannot be improved upon according to one criterion without hurting another criterion is known as the Pareto set. The curve generated by plotting the competing objectives of the best designs is known as the Pareto frontier. A design is judged to be "Pareto optimal" if it is not dominated by any other design. If it is worse than another design in some respects and no better in any respect, then it is dominated and is not Pareto optimal. The choice to determine the "favorite solution" from among Pareto optimal solutions is left with the decision maker or designer.

2.4.1 Conventional Techniques for Analog IC Optimization

The conventional methods used in the design optimization of analog integrated circuits include local unconstrained optimization, constrained optimization, stochastic optimization and simulated annealing. Many algorithms have been developed to estimate the optimal value of the objective functions. Simplex method is used in analog design in [10] where a new multiple criteria constrained performance optimizer for analog integrated circuits, based on non-linear programming and heuristic techniques is presented. A modified Parkinson Hutchinson Simplex algorithm and Guided Random Search technique are used to perform optimization based only on cost function evaluations. These optimization techniques are combined to combat numerical difficulties faced during circuit simulation and gradient based optimization. The results are well verified with real life circuits at Texas Instruments Inc. to ascertain the consistent improvements in circuit performance. One of the popular tools OPASYN [11] uses the steepest descent algorithm for optimization of basic two-stage operational amplifier, folded cascade operational amplifier and can be extended to any type of analog circuit. The parametric optimization proceeds by developing analytic circuit models, reduction

of the dimensionality and size of the search domain, by defining a minimal set of independent design parameters and set reasonable upper and lower bounds on their range. Due to smoothness of the resulting search spaces simple numerical optimization algorithms can be used effectively. The steepest descent optimization algorithm used is simple and efficient but needs a differentiable search space with a continuous first derivative. Apart from this, the tool performs layout generation too. OAC [12] use gradient-based methods for opamp compilation with performance optimization. A parametric optimization consisting of several interactive improvement steps based on circuit simulation and gradient evaluation is given in [13]. DELIGHT.SPICE [14] is the combination of the DELIGHT interactive optimization based computer aided design system and the SPICE circuit analysis program. Using the DELIGHT.SPICE tool, circuit designers can employ recent powerful optimization algorithms and methodology that emphasizes designer intuition and man-machine interaction in a manner in which designer and computer are complementary to each other to adjust parameters of electronic circuits automatically to improve their performance. They may optimize any performance objective and also study complex tradeoffs between multiple competing objectives, simultaneously satisfying multiple constraint specifications. Jiffy Tune [15] is a gradient based approach for circuit optimization. A set theoretic approach for robust design of analog circuits is presented in [16]. In the AMGIE system [17], there is a provision for the user to select the optimization algorithm as one of the options to be chosen in the specification sheet window. Global-optimization algorithms, like very fast simulated re-annealing (VFSR), and local-optimization algorithms, like Hooke-Jeeves, min-max, or sequential quadratic programming (SQP), can be chosen here. After the sizing optimization in the AMGIE system, the resulting optimal device sizes are automatically back annotated onto the schematic of the circuit under design.

BLADES [18], is a prototype design environment which uses a divide and conquer method, is capable of designing a wide range of sub-circuit functional blocks as well as a limited class of integrated bipolar operational amplifiers. This is believed to be the first successful design expert system in the analog design domain.

It uses different levels of abstraction depending on the complexity of the design task under consideration. The importance of the abstraction level lies in the fact that once design primitives are defined, the problem of extracting the knowledge (design rules) becomes less complex. All circuits designed and tested using BLADES are observed to be stable.

In [19] convex optimization procedure is used to construct optimization environments for pipelined and delta sigma analog to digital converters. Methods of analog and radio frequency integrated circuit design using optimization with recourse including ellipsoidal uncertainty are provided in [20]. Geometric programming (GP) is used for device-circuit co-optimization of mixed mode circuit designs in [21]. In this methodology, GP-based circuit optimization technique is used to improve performance by blending different type of devices in a circuit. The benefit of mixing different type of devices by co-optimizing device and circuit is demonstrated by designing a track-and hold amplifier. The circuit sizing is again modeled as a geometric program [22] where op-amp design is implemented in C language using GPGLP library for GP solver [23]. The design objectives here are maximization of unity-gain bandwidth, DC gain and minimization of input referred noise and power consumption. In [24] improved sigma delta data converter is calibrated through convex optimization. Using the promising methodology of geometric programming and formulation of circuit problems in posynomial form tools like GPCAD [25] are developed. Geometric Programming is successfully applied for two stage operational amplifier sizing by Mandal and Viswanathan in [26] where the opamp design is formulated as a sequence of convex programming problems. The objective and the constraints functions for optimization are modeled as posynomial in design variables, which is solved as a convex optimization problem. Then a sequence of convex programs are formulated and solved to address the second order effects. In this novel work, the use of accurate model makes the sizing technique robust. Iterative Sequential Geometric Programming (ISGP) [27] is used for robust analog circuit sizing.In this work, for each parameter of the geometric programming (GP) compatible device and performance model, a correction factor has been introduced. The SPICE simulation is used to update the

correction factors after every iteration of the sequential geometric programming (SGP) optimization. Advantages of SGP based optimization, such as, fast convergence and efficient optimum design are utilized and simultaneously the design point is fine tuned using SPICE simulation by rectifying inaccuracy that may exist in device and performance models.

A sequential quadratic programming technique is used to solve the nonlinear analog circuit optimization problem [28]. To ensure a good solution the optimization is restarted with different initial values. Here a current mirror operational transconductance amplifier is taken as the design example.

MARS [29] presents a novel approach for automatic computation of matching constraints for analog circuit sizing. It uses a min-max principle for feasibility, nominal and yield optimization. It can be applied with any available optimization method for sizing. This approach firstly detects automatic matching conditions for sizing in analog circuit using a symmetry computation.

Simulated annealing estimates optimal dimensions without the derivatives and hence has been successfully applied to size general analog circuits in VCOs [30], sigma delta modulators [31], radio frequency receivers [32] and operational amplifiers [33]. An automatic synthesis tool which uses simulated annealing as its optimizer, for a cascade low noise amplifier (LNA) is proposed in [34].

2.4.2 Evolutionary Techniques for Analog IC Optimization

Evolutionary techniques are search algorithms that operate by evolving a population of solutions through repeated transformations. These are used to solve big size problems with multiple criteria. Though they do not guarantee to arrive at an optimal solution in an exact way but provide an acceptable approximation in an affordable computing time. Kruiskamp and Leenarts [35] developed DARWIN where GA is used for topology selection and circuit sizing of CMOS operational amplifier. In DARWIN, from an initial set of randomly generated opamps a set evolves in which the transistor sizes and topologies of the opamps are adapted to the performance specifications.

The GA is used in [36] for automatic analog synthesis and in [37] for optimization of analog building blocks. The design automation environment GENOM [38] has been developed by combining optimization algorithm GA along with a supervised learning strategy based on support vector machine (SVM) to create feasibility models in order to reduce the overall number of evaluations. Optimization of a nano-CMOS voltage controlled oscillator using polynomial regression and genetic algorithm is reported in [39]. A novel methodology for generation of performance models for sizing of analog high level topology is presented in [40] where optimal values of the model hyper parameters are determined through a grid search-based technique and a genetic algorithm- (GA) based technique. The high-level models of the individual component blocks are combined analytically to construct the high-level model of a complete system. The accuracy, fastness, genericness and less model construction time are the novelties of the method.

Tawdross and Konig [41] introduced particle swarm optimization (PSO) in place of GA for field programmable analog scalable device array reconfiguration. An operational amplifier with design constraints was designed using PSO taking into account the external constraints in the above work which was further extended for a three bit flash ADC [42]. Current conveyor circuits are optimized in [43] using particle swarm optimization (PSO). Thakker et.al. [44] designed low power low voltage analog circuits applying hierarchical PSO. Hierarchical PSO (HPSO), an extended version of PSO algorithm is employed here to design a CMOS Miller OTA (operational transconductance amplifier), whose performance is reported to be better than the manual design and GA based design.PSO also finds application for analog circuit sizing in [45] and [46].

M.Barari et.al. [47] combined GA with PSO for the design and optimization of analog integrated circuits (ICs). This paper investigates an evolutionary-based designing system for automated sizing of analog ICs. Two evolutionary algorithms, genetic algorithm and PSO algorithm, are employed to design analog ICs with practical user-defined specifications. HSPICE and MATLAB are combined together to link the circuit performances, evaluated through electrical simulation, to the

optimization system, for the selected topology. Two-stage opamp and folded cascade amplifier are designed as case study to show the superiority in terms of the quality, efficiency and robustness of this methodology over the available methods like genetic algorithm.

Differential evolution is a population based evolutionary computation technique, which uses a simple differential operator for new candidate solution creation and one-to-one competition scheme for greedy selection of new candidates. B.Liu et.al. [48] proposed competitive co-evolutionary differential evolution for automated sizing of analog integrated circuits with practical user defined specifications. In another work [49] analog filter is designed using differential evolution method.

Artificial Bee Colony (ABC) optimization is applied to nano-CMOS phase locked loop (PLL) [50]. Ali Jafari et.al. [51] proposed a new hybrid shuffled frog leaping (NHSFL) algorithm to deal with the constraints and obtain the device sizes optimizing the performance of the circuits.

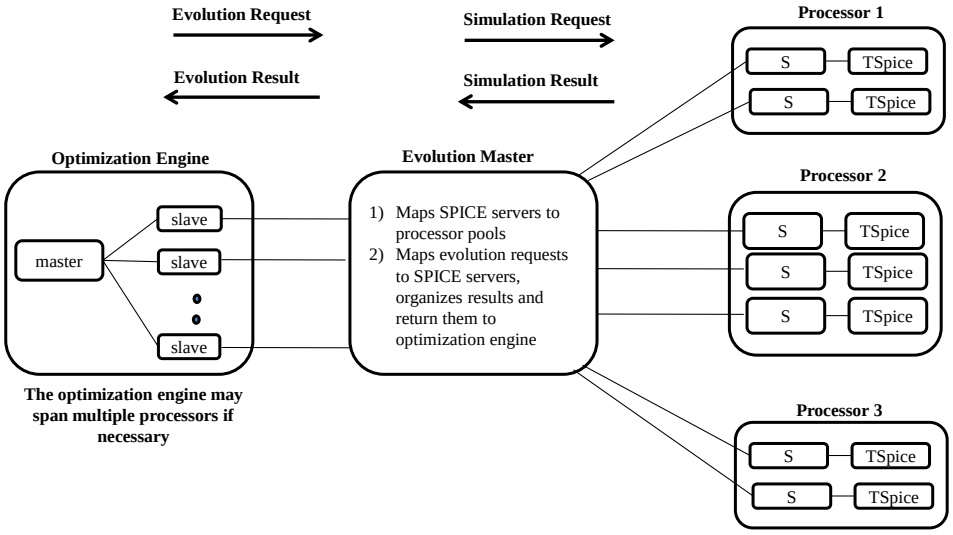

Figure 2. 4 The Anaconda Synthesis Architecture [55]

A simulation-based analog circuit synthesis methodology is proposed and validated in [52] which optimizes both the simulator and the search algorithm. It uses an accelerated simulator, SPASE, and a modified version of self-adaptive evolutionary strategies for quicker convergence of the algorithm. The performances

of genetic algorithm, artificial bee colony optimization and particle swarm optimization in analog active filter design and optimization are evaluated in [53] by applying each algorithm to realize two different filter structures. Multi-objective analog circuit design methodology proposed in [54] is used in prototyping system on reconfigurable platforms like Field Programmable Analog Arrays (FPAAs) and Field Programmable Gate Arrays (FPGAs) where lot of gains in total design time are achieved compared with simulation based methodologies. The simulation-based analog circuit synthesis tool ANACONDA [55] illustrated in Figure 2.5 combines the population of solutions from evolutionary algorithms with a variant of stochastic pattern search to synthesize a circuit using the same industrial-strength simulation environment created to validate the circuit.

In one of the related work [56], a novel optimization methodology incorporating a geostatistics inspired metamodelling technique and a gravitational search algorithm for analog and mixed signal circuit and system design is presented. This proposed methodology is used in the design optimization of a 45 nm CMOS-based thermal sensor. Two nature inspired metaheuristics, differential evolution (DE) and harmony search (HS) algorithms are utilized [57] for optimal filter design of different topologies and manufacturing series. The feasible solutions provided by a multi-objective evolutionary algorithm (MOEA) in the optimal sizing of analog integrated circuits (ICs) can be very sensitive to process variations. To choose low sensitive optimal MOSFET sizes multi-parameter sensitivity analysis is carried out. The multi-parameter sensitivity analysis verified through the optimization of a recycled folded cascode (RFC) operational transconductance amplifier (OTA) [58] show that the optimal sizes, selected after executing the sensitivity approach, guarantee the lowest sensitivities values while improving the performances of the RFC OTA.

2.4.3 Parasitic Aware Analog IC Optimization

The performance degradations due to device and package parasitic components are counter acted by use of parasitic aware synthesis for achieving optimum performance. The benefits gained from optimization of RF circuits design

by considering chip and package parasitic as an integral part of the design process are demonstrated in [59]. In [60], a 0.6um digital-CMOS technology with three metal layers is considered to design a 0.5-5.5GHz distributed amplifier by considering the package parasitics and using the on-chip inductors as the basis for the delay lines. In this design the parasitic-laden on-chip inductors are considered as an integral part of design from the beginning by using a parasitic-aware optimization methodology based on the simulated annealing technique. The classic detail of the parasitic aware optimization is illustrated in [61] [62]. The methodology comprises three major modules linked via a netlist: an optimization core, a parasitic-aware compact model generator, and a standard circuit simulator (Figure 2.3). The optimization core estimates the design variables in the netlist according to an optimization algorithm. The netlist is simultaneously updated with information from the compact model generator. The parasitic-laden netlist is then simulated by any user-specified circuit simulator like HSPICE or SPECTRE. After the simulation, the outputs are fed back to the optimization core for evaluation and generation of the new netlist variables. The optimization core is the most critical component in parasitic-aware synthesis. Simulated annealing (SA) and particle swarm optimization (PSO) algorithms have been used to implement the core optimizer in [61].

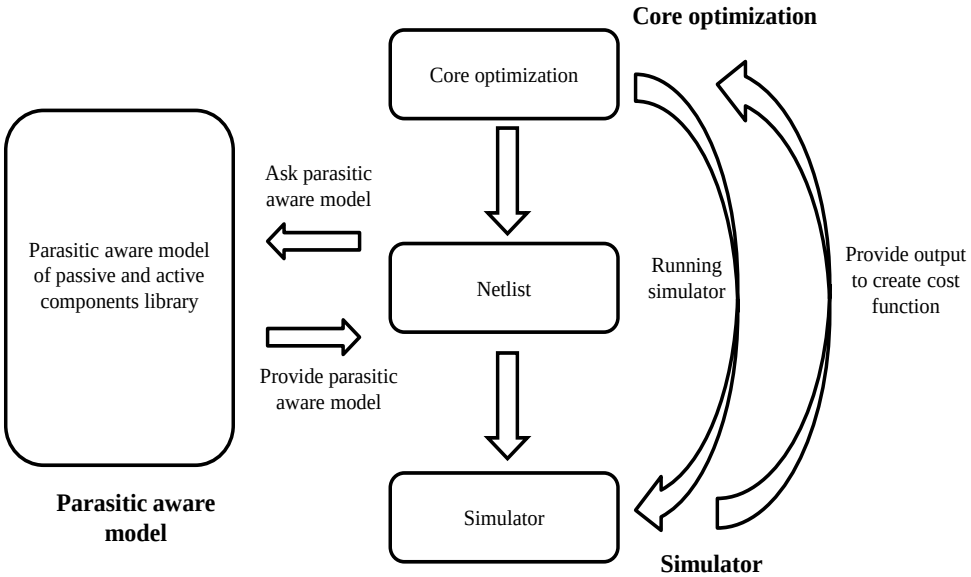

Figure 2. 5 Parasitic Aware Optimization

2.5 Conclusion

The real world is analog in nature and the analog signals need to be processed by integrated circuits(IC). The performance of the system is always driven and dictated by the analog part of the integrated circuit. It is highly difficult to design analog circuits due to their complexity, noise sensitivity and multiple performance tradeoffs. So there is a desperate need of some algorithms which can help the designer to meet the desired specifications by circuit sizing and optimization of multiple complex and sensitive performance parameters dictated by technology constraints. In general the analog IC design problem is highly complex, multi-objective, multi-modal and multi-constraints based. Along with optimization the design algorithm must be parasitic and process variation aware to make the IC robust enough for targeted application and high yielding for economic viability. Evolutionary algorithm based optimization tools are highly suitable in comparison to conventional gradient based techniques as the problem is multi-modal with multiple competing objectives. Direct search method, Newton's method, conjugate gradient method, gradient descent method, simplex method etc are gradient-based algorithms and are very efficient but may lead to sub optimal solutions. IC design automation techniques based on evolutionary algorithms like Genetic Algorithms, Particle Swarm Optimization, Differential Evolution etc are efficient in optimization of performance objectives but they would be more efficient and precise in circuit sizing if better constraint handling method would be incorporated. NSGA-II is a well-established efficient multi-objective optimization algorithm, which can be used for circuit sizing and performance optimization of the analog ICs. Other recently developed multi-objective algorithms, which could handle constraints more efficiently, can be tried for optimal analog IC design.

Normally the worst-case process is considered while designing to make the analog IC robust against process variations. However, practically the IC is used in nominal environment in most of the cases, so to make the IC robust and optimal; some different methodology must be thought of to address the problem.

Rapid Prototyping Methodology for High Performance Nano-CMOS VCO based on NSGA-II Optimization

3.1 Introduction

Ring oscillators find wide use in communication circuits and clock synthesis. The CMOS voltage controlled oscillators (VCO) are the circuits used in phase locked loops and many other vital applications. In the nano-scale technology it is highly desired to design these circuits in high precision in radio frequency operating range offering very low noise and low power consumption. The parasitic components in radio frequency integrated circuits (RFIC) have a significant effect on the device performances. Circuit parasitics affect the speed, power consumption, area and many other performances. In high performance integrated circuits (IC) it is very much needed to consider the parasitic effects during the design phase of the circuit. Inclusion of parasitic components makes, the complete circuit too much complex for hand analysis. Hence finding design parameters manually for optimal circuit performance by the designer is very difficult. The complexity of the problem is further elevated when there is a necessity to optimize multiple competing performance objectives. The complex design landscape not only makes it difficult to arrive at an optimum performance but also consume lot of designer's time to have the first prototype.

In the conventional parasitic cognizant optimization a parasitic aware model library is provided to the netlist on which single objective optimization is carried out. The extracted parasitics for a circuit is provided to the circuit netlist which is subjected to single objective metaheuristic optimization like simulated annealing [4] or global optimization like swarm intelligence [63] [64]. In most of these cases the parasitics are generated from a circuit initially which may not be yielding optimal performance and hence the parasitics that are considered for further circuit

optimization may not be proper in their values. Hence just a parasitic aware optimization of circuits as has been reported in many cases may not yield performance close to the optimum value. To circumvent this problem the parasitics should be extracted from an initially optimized circuit so that the parasitic values are more realistic for consideration in further optimization.

Another concern in the design optimization process is the accuracy of the optimization objective models. Ideally one should consider the SPICE device models like BSIM4 [65] for optimization but they involve hundreds of variables. Directly working with these models is highly impracticable by a designer in industry. A tractable equation based optimization necessitates low-dimensional models with less complexity yet offering sufficient accuracy in the circuit behavior.

Apart from this it is always desirable that multiple design objectives should be optimized in integrated circuits. For such requirements, the single objective methods are inadequate. So it is motivating to apply efficient multi-objective optimization techniques like Non-dominated Sorting Genetic Algorithm-II (NSGA-II) [66] [67] to CMOS VCO circuits in a constrained environment. The RF integrated circuits designed in [68] has a scope to be made robust if the circuit parasitics are implicitly considered in the design phase.

In the proposed design methodology the above three issues are collectively considered for predictably near optimal performance. Besides this, the technique finds the design parameters in a single run and hence the time to design the first prototype is greatly reduced. The CMOS voltage controlled oscillators are considered here for optimization of phase noise and power consumption with a goal to achieve a targeted frequency of oscillation in a technology constrained environment. Acceptably manageable model equations, which include the parasitics, are considered as optimization objectives. The design parameters obtained from the multi-objective constrained optimization NSGA-II technique are used to design schematic and physical layout level CMOS voltage controlled oscillators in the Cadence Virtuoso Analog Design Environment (ADE) [69]. Since the methodology is newly applied to CMOS VCOs, to the best of our knowledge there is no other benchmark result available for direct comparison. Hence, for the demonstration of

the methodology, the circuit performance parameters are estimated from the transient and noise analysis in Cadence tool and are compared with their estimated values obtained from optimization. The circuits considered here are CMOS ring oscillators with different number of stages, current starved voltage controlled oscillator (CSVCO) and differential voltage controlled oscillator (DVCO).

The remaining part of the chapter is organized as follows. The next Section describes the design objectives for different nano-CMOS VCO topologies. In Section 3.3 the NSGA-II optimization kernel is described. Section 3.4 presents the proposed design flow of energy efficient, low phase noise CMOS VCO to achieve a target frequency. In Section 3.5 the performance of the optimized circuit is analyzed. Finally in Section 3.6 the conclusion of the chapter is drawn and scope for further research work is outlined.

3.2 Design Objectives for the Nano-CMOS VCO

The desired frequency of oscillation, phase noise and power consumption are the objective functions for the nano CMOS ring oscillator (RO) and voltage controlled oscillators (VCO), considered in this work as case studies. Details of different VCOs are described below.

3.2.1 CMOS Ring Oscillator

The ring oscillator comprises of a number of delay stages, with the output of the last stage fed back as the input to the first. To achieve sustained oscillations, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages and the remaining phase shift is provided by a dc inversion. This indicates that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages provided that the feedback lines are swapped. The general structure of the ring oscillator is depicted in Figure 3.1. The

transistor level circuit schematic of five-stage CMOS ring oscillator is shown in Figure 3.2.

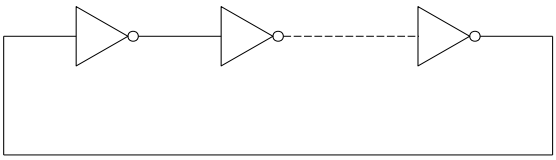

Figure 3. 1 General Structure of ring oscillator

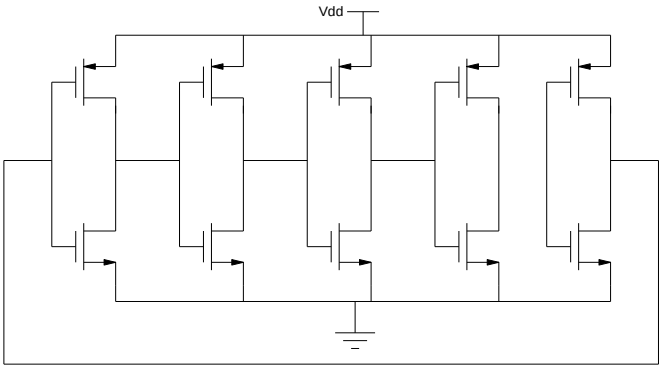

Figure 3. 2 A five stage CMOS ring oscillator

The performance parameters of the ring oscillator are as follows.

A. Frequency of Oscillations

Assuming that each stage provides a delay of t_d, an expression for the oscillation frequency is arrived. The signal goes through each of the N delay stages once to provide the first π phase shift in a time of Nt_d. Then the signal must go through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2Nt_d$.

Therefore, the frequency of oscillation is given by

$$f_{osc} = \frac{1}{2Nt_d}$$

The nonlinearities and parasitics of the circuit makes it difficult to estimate t_d and hence the frequency value. The frequency of oscillation for an N-stage CMOS ring oscillator [70] [71] [72] taking circuit parasitics into consideration, is precisely modeled as

$$f_{osc} = \frac{I_D}{N \times V_{DD} \times C_{tot}} \quad (3.1)$$

Where

$$\mathrm{C_{tot}} = \mathrm{C_{in}} + \mathrm{C_{gd_p}} + \mathrm{C_{db_p}} + \mathrm{C_{gdov_n}} + \mathrm{C_{db_n}} + \mathrm{C_{gsov_n}} + \mathrm{C_{gbov_n}}$$

$$\mathrm{C_{in}} = \frac{2}{3}\mathrm{C_{ox}W_nL_n}$$

$$\mathrm{C_{gd_p}} = \mathrm{C_{gdchannel_p}} + \mathrm{C_{gdov_p}}$$

$$\mathrm{C_{gdchannel_p}} = \frac{1}{2}\mathrm{C_{ox}W_pL_p} \ ,$$

$$\mathrm{C_{db_n}} = \frac{\mathrm{Cj_n\ Ad_n}}{\left(1+\frac{\mathrm{V_{DD}}}{\mathrm{pb_n}}\right)^{\mathrm{mj_n}}} + \frac{\mathrm{Cjsw_n\ Pd_n}}{\left(1+\frac{\mathrm{V_{DD}}}{\mathrm{pbsw_n}}\right)^{\mathrm{mjsw_n}}}$$

$$\mathrm{C_{gdov_n}} = \left(1+\cos\left(\frac{\pi}{\mathrm{N}}\right)\right)\mathrm{W_nC_{gdo_n}}$$

$$\mathrm{C_{db_p}} = \mathrm{Cj_p\ Ad_p} + \mathrm{Cjsw_p\ Pd_p}\ , \mathrm{C_{gdov_p}} = \mathrm{W_pC_{gdo_p}}$$

$$\mathrm{C_{gsov_n}} = \mathrm{W_nC_{gso}}\ ,\ \mathrm{C_{gbov_n}} = 2\mathrm{L_nC_{gbo}}$$

$$C_{in} = \frac{2}{3}C_{ox}W_nL_n$$

$$C_{gd_p} = \frac{1}{2}C_{ox}W_pL_p$$

$$C_{db_n} = \frac{Cj_n\ Ad_n}{\left(1+\frac{V_{dd}}{pb_n}\right)^{mj_n}} + \frac{Cjsw_n\ Pd_n}{\left(1+\frac{V_{dd}}{pbsw_n}\right)^{mjsw_n}}$$

$$C_{gdov_n} = \left(1+\cos\left(\frac{\pi}{N}\right)\right)W_nC_{gdo_n}$$

$$C_{db_p} = 2Cj_p\ Ad_p + 2Cjsw_p\ Pd_p$$

$$C_{gdov_p} = W_pC_{gdo_p}$$

$$C_{gsov_n} = W_nC_{gso}$$

$$C_{gbov_n} = 2L_nC_{gbo}$$

The major parameters used above are C_j: zero-bias area junction capacitance, C_{jsw}: zero-bias sidewall junction capacitance, C_{gdo}: gate-drain overlap capacitance pb: p-n junction potential, $pbsw$: p-n junction sidewall potential, m_j: area junction grading coefficient, $mjsw$: sidewall junction grading coefficient, A_d: drain area, P_d:

drain perimeter, V_{DD}: the positive power supply voltage, and I_D: the drain current flowing through a single inverter stage.

B. Power Dissipation

The power dissipation in general CMOS circuits is classified as static power and dynamic power consumption. The static power dissipation in CMOS is due to leakage currents and is small in comparison to other components. In the operation of CMOS inverter current flow consists of two components, one due to output capacitor charging and discharging and the other due to current flowing straight from V_{DD} to ground. The power dissipated in charging and discharging the load capacitances is known as the switching power. The component of the power dissipation due to the flow of current from V_{DD} to ground is called the short-circuit power dissipation.

The total power dissipated in any CMOS circuit is given by

$$P_{Total} = P_{Dynamic} + P_{ShortCircuit} + P_{Static} \quad (3.2)$$

The average dynamic power dissipated [73] by N-stage CMOS ring oscillator circuit is given by

$$P_{avg} = \eta V_{DD} I_D = \eta N V_{DD} q_{max} f_{osc} \quad (3.3)$$

Where $q_{max} = C_{tot} * V_{DD}$, $I_D = N C_{tot} V_{DD} f_{osc}$ and P_{avg}= average dynamic power dissipated by the CMOS ring oscillator and η is a characteristic constant usually chosen between 0.75 and 1. Here the short-circuit power and static power for ring oscillator are very small and hence are not considered here in the estimation of the total power.

C. Phase Noise

Practical oscillators experience fluctuations in amplitude and frequency. Short-term frequency instabilities of an electrical oscillator are mainly due to noise and interference sources. Thermal, shot and flicker noise are examples of the former, while substrate and supply noise are in the latter group. These sources result in frequency instabilities, which are termed as phase noise.

An ideal oscillator output is generally expressed as $V_{out}(t) = V_0\cos[\omega_0 t + \emptyset_0]$ where the amplitude V_0, the frequency ω_0 and phase reference $\emptyset_0$ are all constants. The one-sided spectrum of the ideal oscillator with no random fluctuations has an impulse at ω_0 as shown in Figure 3.3. The output of an actual oscillator is generally expressed as

$$V_{out}(t) = V_0.[1 + A(t)].f[\omega_0 t + \emptyset(t)] \quad (3.4)$$

Where $\emptyset(t)$ and $A(t)$ are functions of time, V_0 is the maximum voltage swing and f is a periodic function which represents the shape of the steady-state output waveform of the oscillator. If the waveform is not sinusoidal the output spectrum has power around harmonics of ω_0. Due to the fluctuations represented by $\emptyset(t)$ and $A(t)$, the spectrum of a practical oscillator has sidebands close to the frequency of oscillation, and its harmonics, as shown in Figure 3.3. These sidebands are generally referred to as phase noise sidebands.

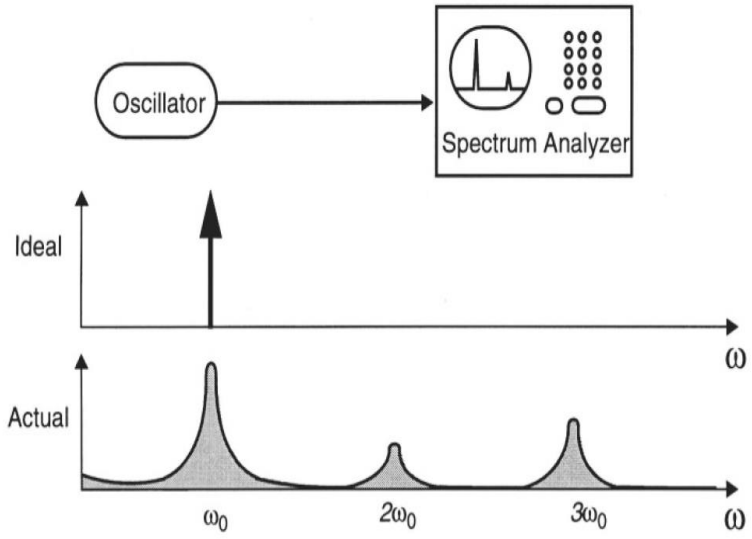

Figure 3. 3 The Frequency Spectrum of an Ideal and Actual Oscillator [74]

Visualized in the frequency domain, an oscillator's short-term instabilities are usually characterized in terms of the single sideband noise spectral density. Conventionally the unit of phase noise is decibels below the carrier per hertz (dBc/Hz) and it is defined as (Figure 3.4)

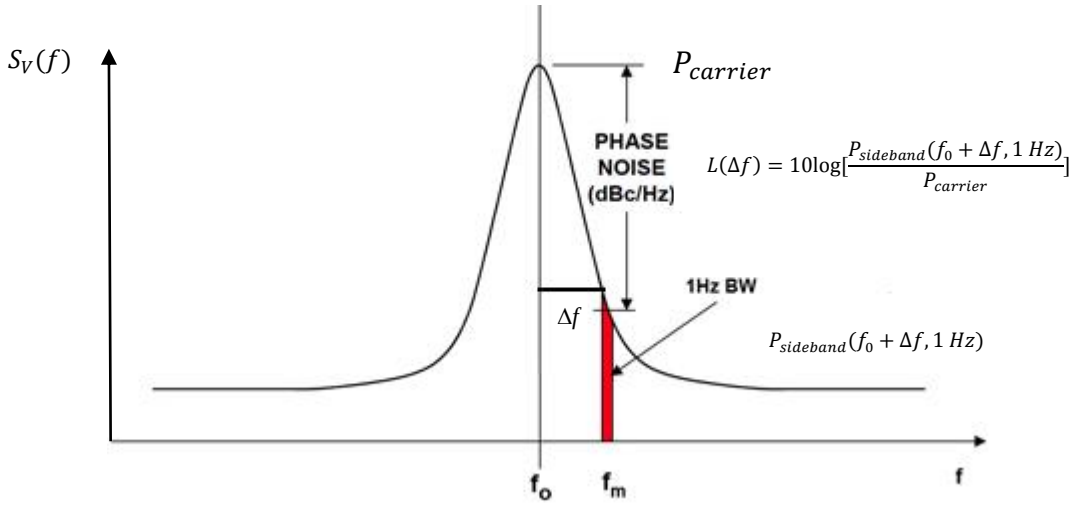

Figure 3. 4 The Phase Noise calculation per unit bandwidth

$$L\{\Delta f\} = 10.\log\left[\frac{P_{sideband}(f_0 + \Delta f, 1Hz)}{P_{carrier}}\right] \qquad (3.5)$$

Where $P_{sideband}(f_0 + \Delta f, 1Hz)$ represents the single sideband power at a frequency offset Δf, from the carrier in a measurement bandwidth of 1Hz as shown in Figure 3.4, and $P_{carrier}$ is the total power under the power spectrum. Spectral density is usually specified at one or a few offset frequencies. A meaningful representation of phase noise specifies both the noise density and the offset.

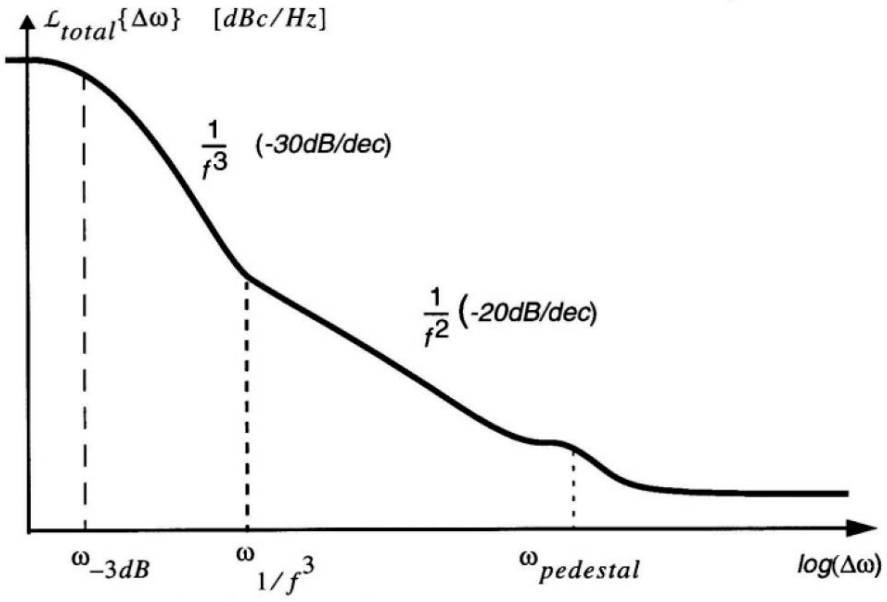

Figure 3. 5 A typical phase noise plot for a free running oscillator

In a plot of spectral density as a function of $\Delta\omega$ on logarithmic scales for free running oscillator (Figure 3.5) regions with different slopes are observed. At large offset frequencies, there is a flat noise floor. At small offsets, there are regions with a slope of $\frac{1}{f^2}$ and $\frac{1}{f^3}$ where the corner between the $\frac{1}{f^2}$ and $\frac{1}{f^3}$ regions is called $\omega_{\frac{1}{f^3}}$.Finally, the spectrum becomes flat again at very small offset frequencies.

The maximum total channel noise from PMOS and NMOS devices in a single ended CMOS ring oscillator, when both input and output are at $\frac{V_{DD}}{2}$, is given by

$$\frac{\bar{i}_n^2}{\Delta f} = \left(\frac{\bar{i}_n^2}{\Delta f}\right)_P + \left(\frac{\bar{i}_n^2}{\Delta f}\right)_N = 4kT\gamma\mu_{eff}C_{ox}\frac{W_{eff}}{L}\Delta V \qquad \textbf{(3. 5)}$$

Where

$\frac{\bar{i}_n^2}{\Delta f}$ is the single sideband power spectral density of the noise current source.

$W_{eff} = W_n + W_p$ and $\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p}$

ΔV is the gate over drive voltage in the middle of the transition and is given by

$\Delta V = \left(\frac{V_{DD}}{2}\right) - V_T$

k is the Boltzmann constant

T is the absolute temperature

and γ is a characteristic coefficient which is 2/3 for long channel devices in saturation and two to three times larger for short channel devices [74] [75] [76].The expression for total phase noise of the circuit is

$$\mathcal{L}\{\Delta f\} = \frac{8}{3\eta}\frac{kT}{P_{avg}}\frac{V_{DD}}{V_{char}}\frac{f_{osc}^2}{\Delta f^2} \qquad \textbf{(3. 6)}$$

Where $V_{char} = \frac{\Delta V}{\gamma}$ and Δf is the offset frequency from the carrier at which the phase noise is measured.

D. Figure of Merit

The figure of merit (FOM) [77] is a performance index which integrally represents frequency of oscillations, the phase noise and the power consumption.

The FOM is used here to have a combined performance index for measurement. This is expressed as

$$FOM = 10\ log_{10}\left[L(\Delta f) \times \left(\frac{\Delta f}{f_{osc}}\right)^2 \times \frac{P_{Total}}{10^{-3}}\right] \qquad (3.\ 7)$$

The unit of FOM is dBc/Hz ($L(\Delta f)$ times a dimensionless factor). A smaller FOM corresponds to a better VCO design.

3.2.2 Current Starved VCO

The operation of Current Starved VCO (CSVCO) is similar to the ring oscillator. Figure 3.6 shows the schematic of an N stage Current Starved VCO. Middle PMOS and NMOS together operate as inverter, while upper PMOS and lower NMOS operate as current sources. The current sources limit the current available to the inverter, in other words, the inverter is starved of current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. PMOS and NMOS drain currents are the same and are set by the input control voltage [71]. The frequency of oscillation and the phase noise expressions remain the same as the CMOS ring oscillator case. The expression for the power consumption is modified in this case and is given below.

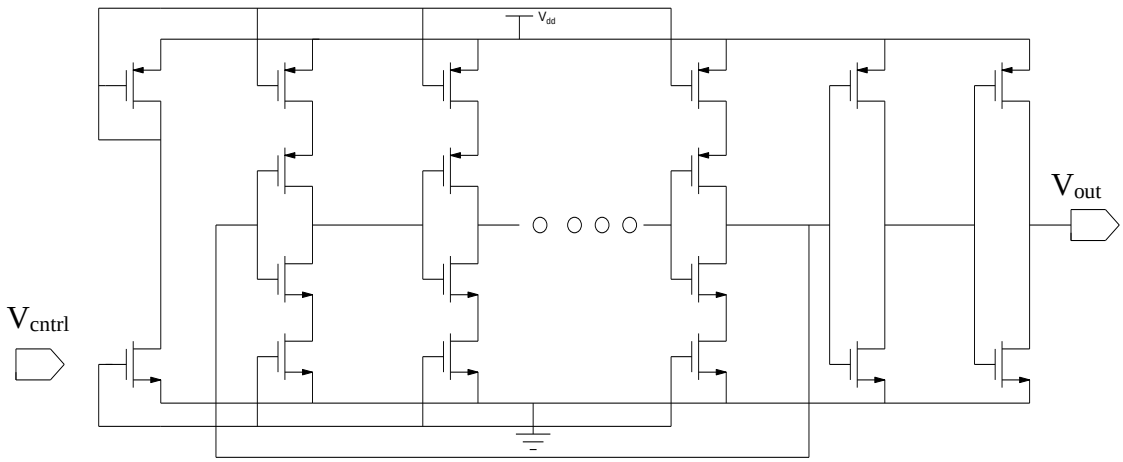

Figure 3. 6 Circuit schematic of CSVCO

Power Consumption

The total power dissipated [78] [79] [80] by N-stage CSVCO circuit is given by

$$P = P_{avg} + P_{SC} \tag{3. 8}$$

Where

P_{avg}= Average dynamic power dissipated by the CSVCO

P_{SC}= Short circuit power dissipation which is given as

$$P_{SC} = \frac{1}{12}\mu_n C_{ox}\frac{W_n}{L_n}(V_{DD} - V_T)^2\frac{\tau}{T} \tag{3. 9}$$

τ is the average rise and fall time and T is the time period of the oscillations. In case of current starved VCO the short circuit power cannot be neglected in comparison to the average dynamic power however, the static power can be neglected.

3.2.3 Differential VCO

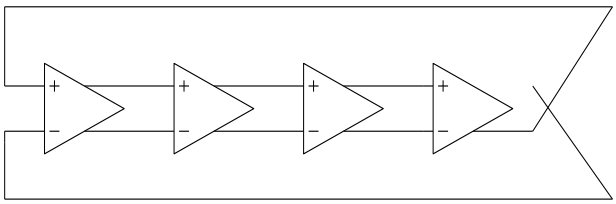

Figure 3. 7 A four-stage Differential Voltage Controlled Oscillator

The Differential VCO (DVCO) considered here is a four-stage one as shown in Figure 3.7. The delay cell of the DVCO given in [81] is depicted in Figure 3.8. As described in [82] [83] it contains a source coupled-differential pair and symmetric loads which provide good control over delay and high dynamic supply noise rejection.

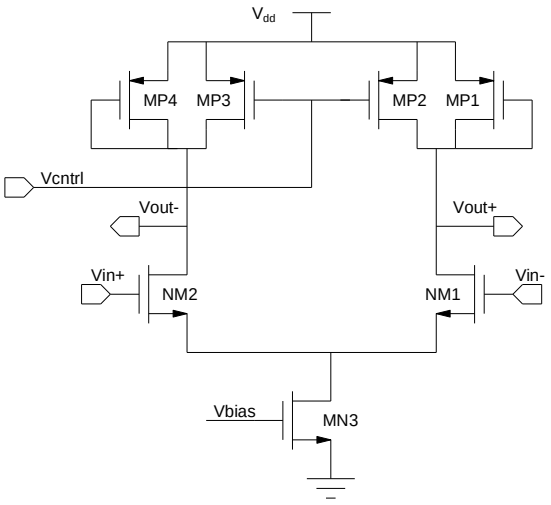

Figure 3. 8 Circuit Schematic of the Delay Cell of Differential VCO

The frequency of oscillation for an N-stage differential VCO, taking [70] into consideration can be modeled as

$$f_{osc} = \frac{I_{tail}}{2N \times V_{sw} \times \left(C_{in} + C_{gd_p} + C_{db_p} + C_{gdov_n} + C_{db_n}\right)} \qquad (3.\ 10)$$

Where $C_{in} = \frac{2}{3} C_{ox} W_n L_n$

$C_{gd_p} = \frac{2}{3} C_{ox} W_n L_n = C_{gdchannel_p} + C_{gdov_p}$

$C_{gdchannel_p} = \frac{1}{2} C_{ox} W_p L_p$

$C_{db_n} = \frac{Cj_n \, Ad_n}{\left(1+\frac{V_{DD}}{pb_n}\right)^{mj_n}} + \frac{Cjsw_n \, Pd_n}{\left(1+\frac{V_{DD}}{pbsw_n}\right)^{mjsw_n}}$

$C_{gdov_n} = \left(1 + \cos\left(\frac{\pi}{N}\right)\right) W_n C_{gdo_n}$

$C_{db_p} = Cj_p \, Ad_p + Cjsw_p \, Pd_p$

$C_{gdov_p} = W_p C_{gdo_p}$

$C_{gsov_n} = W_n C_{gso}$

$C_{gbov_n} = 2L_n C_{gbo}$

Where Cj : Zero-bias area junction capacitance, $Cjsw$: Zero-bias sidewall junction capacitance, $Cgdo$: Gate-drain overlap capacitance, pb: p-n junction potential,

$pbsw$: p-n junction sidewall potential, mj: Area junction grading coefficient, $mjsw$:Sidewall junction grading coefficient, Ad: Drain area, Pd : Drain perimeter.
The power consumption of differential VCO circuits is expressed as [73] [77] [79] and [84].

$$P_{avg} = NI_{tail}V_{DD} \tag{3. 11}$$

$$P_{Total} = P_{avg} + P_{SC} \tag{3. 12}$$

where P_{avg} is the average dynamic power dissipated by the differential VCO and P_{SC} is the short circuit power dissipation as described in (3.10). The static power is also neglected in this case as it is very small in comparison to the average dynamic and short circuit power.

The single side band (SSB) phase noise due to thermal noise in the differential VCO circuit [74] and [75] is expressed as

$$\mathcal{L}\{\Delta f\}_{thermal} = \frac{8}{3\eta}\frac{kT}{P_{avg}}\left(\frac{V_{DD}}{V_{char_n}} + \frac{V_{DD}}{V_{char_p}}\right)\frac{f_{osc}^2}{\Delta f^2} \tag{3. 13}$$

The flicker noise is also associated with differential pair in the VCO which appears due to up conversion. This noise speeds up or slows down every delay stage in a concerted manner over many cycles of oscillation, accumulating into a large variance in phase.

The SSB phase noise due to flicker noise in the differential VCO circuit [85] and [86] is

$$L(\Delta f)_{flicker} = A\frac{K_f}{WLC'_{ox}\,\Delta f}\left(\frac{1}{V_{efft}^2}\right)\frac{f_0^2}{\Delta f^3} \tag{3. 14}$$

Where A= width ratio of the tail MOSFET and diode connected MOSFET, V_{efft}= effective gate voltage at the tail MOSFET, K_f= the flicker noise parameter. The total phase noise is a combination of both thermal and flicker noise contributions.

$$L\{\Delta f\} = L\{\Delta f\}_{thermal} + L\{\Delta f\}_{flicker} \tag{3. 15}$$

3.3 NSGA – II Optimization Kernel

The Non-dominated Sorting Genetic Algorithm-II (NSGA-II) is a multi-objective evolutionary global optimization algorithm, which can optimize many competing or conflicting objectives along with efficient handling of a number of constraints. The NSGA-II [66] has the following three properties:

1. It uses an elitist principle;
2. It uses an explicit diversity preserving mechanism;
3. It emphasizes the non-dominated solutions.

For the fast non-dominated sorting approach two entities need to be computed: (i) domination count n_p, the number of solutions which dominate the solution p; and (ii) S_p, a set of solutions that the solution p dominates. The solutions with $n_p = 0$, represent the first nondominated front. Then, for each solution with $n_p = 0$ (thus from the first non-dominated front), we visit each member (q) of its set S_p and reduce its domination count by one (thus we remove solution p from n_q). For any member for which domination count becomes zero $(n_q = 0)$, we put in a separate list Q. Then Q represents the second domination front. These procedures are repeated for each member of Q to identify the third front, and we continue until all fronts are identified.

To obtain a density estimation of solutions surrounding a particular solution, we compute the average distance of two points on either side of the point along each of the objectives. This quantity $i_{distance}$ serves as an estimate of the perimeter of the cuboid formed by using the nearest neighbors as the vertices (this is the crowding distance). Figure 3.9 shows the crowding-distance of the i^{th} solution in its front (marked with filled circles) which is the average side length of the cuboid (shown with a dashed box). The following algorithm is used to calculate the crowding-distance for each point in set I:

1. Call the number of solutions in I as $l = |I|$. For each i in the set, first assign $I[i]_{distance} = 0$;
2. For each objective m, sort the set in ascending order;

3. For each objective m, assign a large distance to the boundary solutions, or $I[1]_{distance} = I[l]_{distance} = \infty$, and for all other solutions $i = 2\ to\ (l-1)$, assign

$$I[i]_{distance} = I[i]_{distance} + \frac{I(i+1)_m - I(i-1)_m}{f_m^{max} - f_m^{min}} \tag{3.17}$$

Thus the crowding-distance computation requires first to sort the population in ascending order for each objective. Then for each objective function are the boundaries set to infinity, and for all other (intermediate) solutions the distance is the absolute normalized difference in the function values of two adjacent solutions. The last is repeated for all other objectives. Then the total crowding-distance is the sum of individual distance values corresponding to each objective, with each objective being normalized.

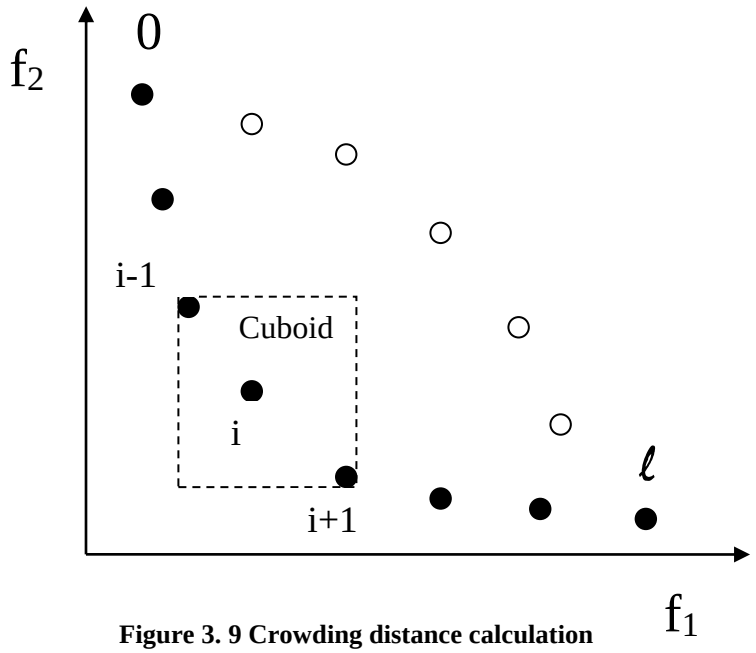

Figure 3. 9 Crowding distance calculation

The crowded-comparison operator $(\succ_n)$ ensures a uniform spread-out of the Pareto front during the various stages of the algorithm. Assume that every individual i has the following two attributes: non-domination rank (i_{rank}), and crowding distance $(i_{distance})$. Then the partial preorder $(\succ_n)$ is defined as $i \succ_n j$ if $(i_{rank} < j_{rank})$ OR $\big((i_{rank} = j_{rank})$ AND $(i_{distance} > j_{distance})\big)$. Thus

in order for a solution to be preferred to another one, it needs a better rank (a better non-domination front) or a better crowding distance in case of the same rank.

The main loop of NSGA-II starts with the initialization of a random parent population P_0 sorted based on the non-domination. First the offspring Q_0 of size N will be created using the usual binary tournament selection, recombination and mutation operators. Algorithm given below and the Figure 3.10 describe the procedure for the t^{th} generation. First, we combine the parents and the offspring($R_t = P_t \cup Q_t$), which has the size *2N*. Then we sort the population R_t according to their non-domination. Elitism is ensured because the current as well as the previous members are included in R_t.The new population (P_{t+1}) will be filled with the best fronts (first F_1, then F_2, etc.), until the size of the next front (F_l) is bigger than the number of open spots in P_{t+1}. To have exactly N members in the new population and the diversity preservation (i.e. a good spread of solutions is maintained in the obtained solution set), the front F_l will be ordered based on the crowding-distance and the first $N - |P_{t+1}|$ (i.e. the number of open spots) solutions will be added to end up with exactly N solutions in P_{t+1}. Then we start again to make an offspring (Q_{t+1}) of P_{t+1} and we repeat this algorithm until the stopping criterion is met.

The NSGA-II Algorithm

$NSGA - II\ Algorithm\ \{$
$Random\ Population\ initialization\ \ P_0$
$Evaluate\ the\ objective\ functions$
$(Phase\ noise\ and\ Power\ consumption)$
$set\ P_0 = (F_1, F_2, \dots) = non\_dominated\_sorting(P_0)$
$for\ all\ F_i \in P_0$
$crowding\_distance\_assignment\ (F_i)$
$set\ t = 0$
$while\ t = 0 \rightarrow Max\_Gen \quad \{$
$generate\ child\ population\ Q_t\ \ from\ \ P_t$
$(by\ crossover\ and\ mutation)$
$set\ R_t = P_t \cup\ Q_t$
$set\ F = (F_1, F_2, \dots) = non\_dominated\_sorting(R_t)$
$set\ P_{t+1} = 0$
$set\ i = 1$
$while\ |P_{t+1}| + |F_i| < N \quad \{$
$crowding\_distance\_assignment\ (F_i)$
$set\ P_{t+1} = P_{t+1} \cup\ F_i$
$set\ i = i + 1$
$\}$

$sort\ F_i on\ crowding\ distances$
$set\ P_{t+1} = P_{t+1} \cup\ F_i[1:(N - |P_{t+1}|)]$
$set\ t = t + 1$
}
$return\ F_1$
}

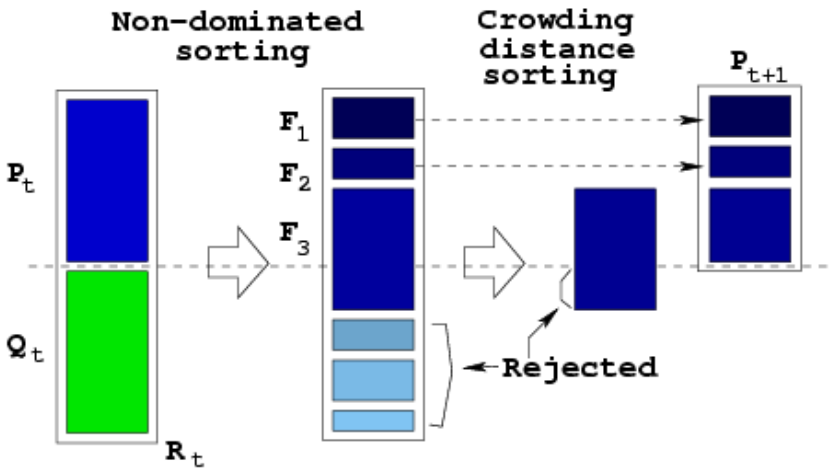

Figure 3. 10 The NSGA – II Optimization Routine

In the above algorithm P_0 is the initial population with size N. The $non\_dominated\_sorting$ is a procedure which involves comparing the objective values of every solution to the objective values of all other solutions in the population and $crowding\_distance\_assignment$ procedure involves the sorting of the elements in pareto fronts F_i one time for every objective.

3.4 Design Flow of Energy Efficient Low Phase Noise CMOS Voltage Controlled Oscillator

The proposed NSGA-II based optimization method in general can be stated as

$$\left.\begin{array}{l} minimize\ F_i(x_j)\ ; i = 1,2,\dots,M; j = 1,2,\dots,N \\ subject\ to\ G_i(x_j) > 0 \\ H_i(x_j) = 0, \\ x_j \in [x_{min}, x_{max}] \end{array}\right\} \quad (3.18)$$

For our case of CMOS voltage controlled oscillator the objectives F_i are power consumption and phase noise. The inequality constraint G_i is $|g_{mn} - g_{mp}| - \delta < 0$ and the equality constraint H_i is $f_{osc} = 2$ GHz. It may be here noted that the

frequency objective is formulated as a constraint. Here g_{mn} and g_{mp} are the transconductance parameters of NMOS and PMOS transistors respectively and δ is small positive definite real number such that $\delta \in (0, 10^{-6})$. The design parameters x_j are $[W_n, L_n, W_p, L_p]$. These parameters are bounded by the maximum and minimum values dictated by the process technology. The proposed method for design of CMOS VCO for optimal performance is depicted in Figure 3.11. The required specifications like operating frequency, the design space constraints and the reference circuit model are the inputs to the NSGA-II optimizer block. The main objective of this optimizer is to determine the design parameters of all transistors in the circuit under consideration. The simple equations of power consumption and phase noise are the optimization objectives for the NSGA-II.

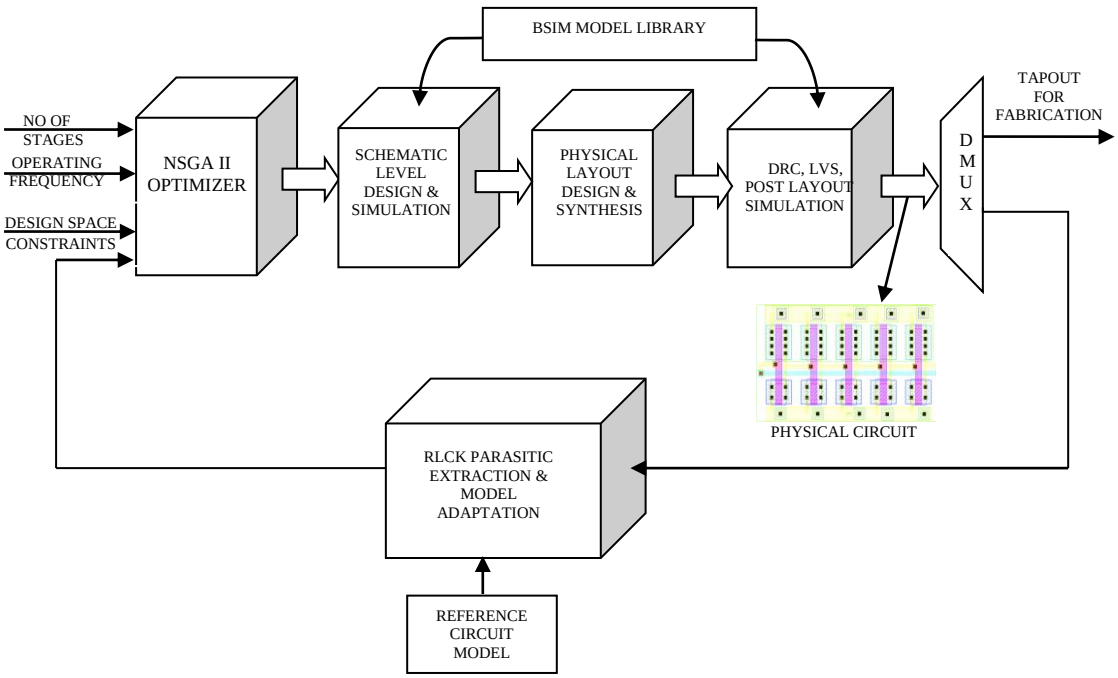

Figure 3. 11 The Design Flow for Optimal CMOS VCO

This optimization method explores the optimal solutions in a constrained design space with a very marginally tolerable frequency drift around the desired frequency. With these initial optimized design parameters obtained from NSGA-II optimizer, the CMOS VCO schematic and the physical layout are designed in Cadence Virtuoso Analog Design Environment.

In most of the parasitic aware design methods, the parasitics are extracted from a layout, which is not optimized to yield better performance. Hence, there is always a finite probability that the parasitic values considered in the design are far away from the parasitic values of the optimal design. To overcome this inadequacy, in the initial attempt the physical layout generated from the first optimization is subjected to RCLK (Resistance, Capacitance, Inductance and Mutual inductance) parasitic extraction. The circuit model adaptively includes the extracted parasitics. This adapted circuit model is again fed back to the NSGA-II optimizer for second and final optimization. This guides the optimizer with a realistic parasitic model of the circuit, which includes the logic parasitics as well as interconnect parasitics. Hence, the final design parameters for the parasitic aware performance optimized CMOS VCO circuit are obtained. These design parameters are then used to generate the physical layout, which can be taped out for fabrication.

3.5 Performance Analysis

The design parameters obtained for the physical layout of the circuit and different performance measures are reported here. Case studies of three oscillator circuits are presented below for demonstration of the proposed methodology.

3.5.1 CMOS Ring Oscillator

The CMOS ring oscillator has identical inverter stages. If the number of stages is prefixed then the only parameters in the hand of the designer are the geometrical sizes of the NMOS and PMOS in the inverter i.e. the width and length of NMOS W_n, L_n , width and length of PMOS W_p, L_p. Conventionally the lengths are put to be equal for both NMOS and PMOS i.e. $L_n = L_p = L$. Since a 90 nm process is used for design, the minimum device dimensions are constrained to be 100 nm. Besides this the algorithm is provided with an upper bound for the device dimensions as an intuitive coarse performance tuning. These upper and lower limits are the geometrical constraints to the algorithm, which in turn restricts the area of the IC.

Case 1: Five Stage Ring Oscillator

The initial design parameters of the five-stage ring oscillator optimized for better performance with a desired frequency of 2 GHz are reported in Table 3.1. The pareto curve of two competing objectives i.e. phase noise and power obtained from the proposed methodology is depicted in Figure 3.12. As per the specification on power and phase noise, a suitable point on the pareto curve can be chosen for the design of the ring oscillator. The parasitic aware optimized circuit design parameters at set 1 point of the pareto curve are taken up for the design which are also provided in Table 3.1. Considering these values the five-stage ring oscillator is designed in Cadence Virtuoso Analog Design Environment whose physical layout is depicted in Figure 3.13.

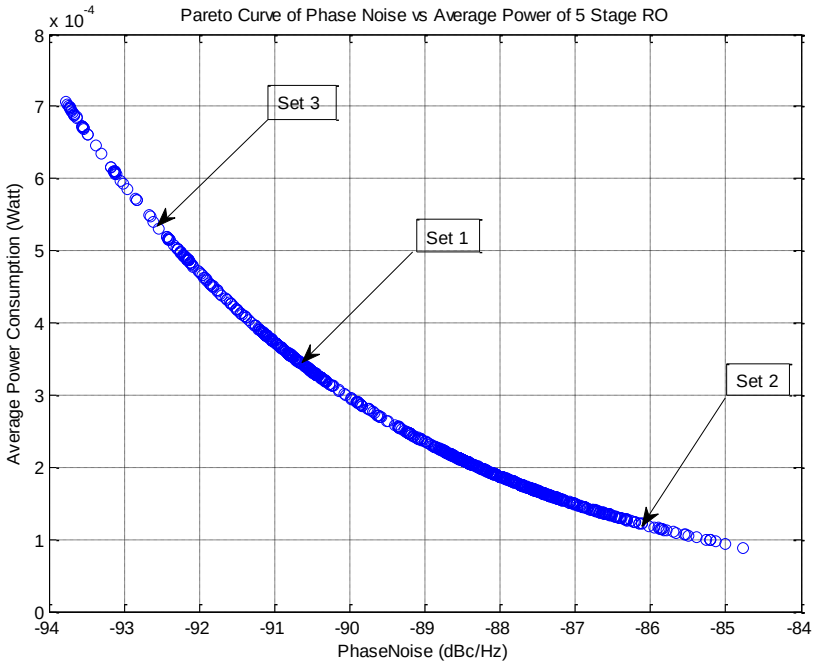

Figure 3. 12 Pareto Curve of Phase Noise and Power Consumption for 5-stage Parasitic Aware Ring Oscillator

Table 3. 1 Design Parameters for Five stage CMOS Ring Oscillator

Design Parameters	Lower Limit	Upper Limit	Initial Value	Parasitic Aware Value
W_n(nm)	120	1000	486	655
W_p (nm)	200	2000	810	1090
L (nm)	100	300	296	285

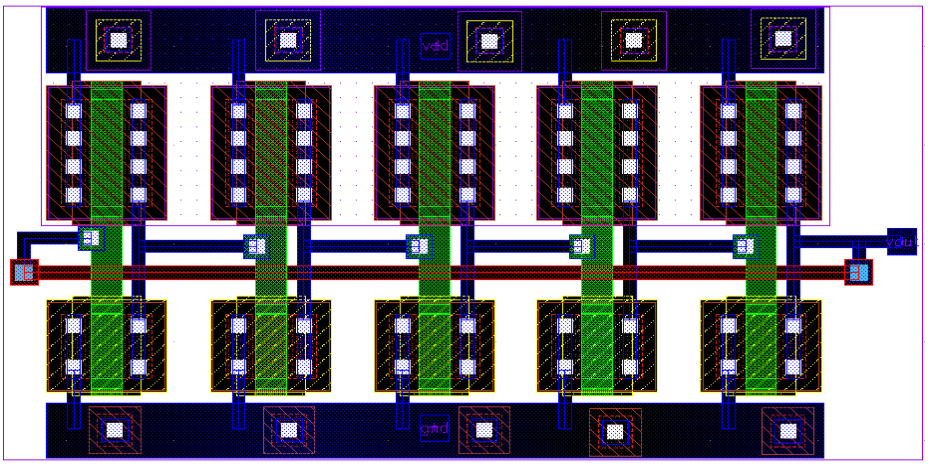

Figure 3. 13 Physical Layout of Parasitic Aware Five stage CMOS Ring Oscillator

The oscillation observed in the post layout simulation is shown in Figure 3.14. The phase noise plot with different offset frequencies and the estimation of power consumption are illustrated in Figures 3.15 and 3.16 respectively.

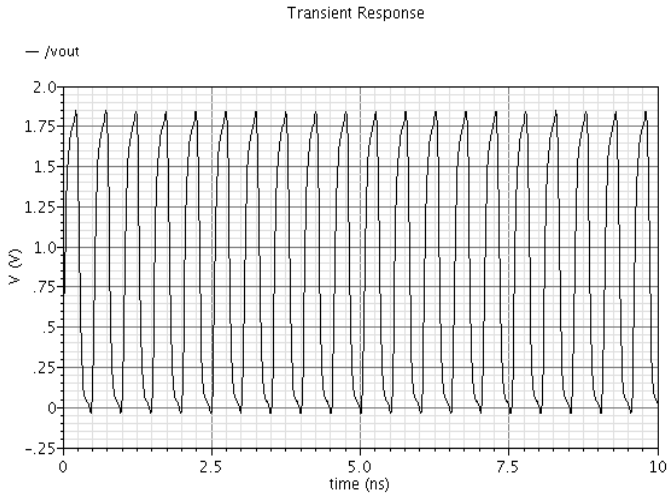

Figure 3. 14 The Oscillations produced by Parasitic Aware Five stage CMOS Ring Oscillator

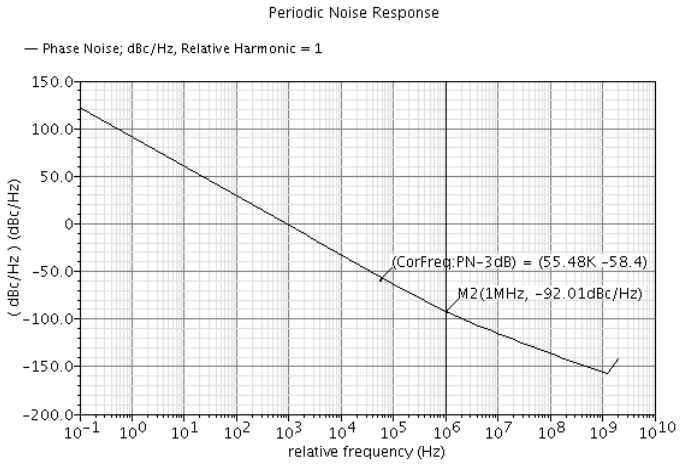

Figure 3. 15 Phase Noise plot for Parasitic Aware Five stage CMOS Ring Oscillator

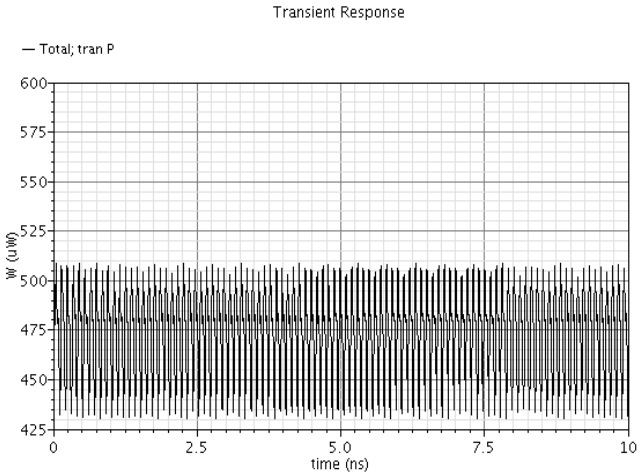

Figure 3. 16 Power Estimation plot for Parasitic Aware Five stage CMOS Ring Oscillator

The five stage ring oscillator targets a 2 GHz frequency and achieves 1.98644 GHz frequency, when parasitics are considered as compared to 1.8526 GHz without consideration of parasitics. The phase noise measured at 1 MHz offset frequency is 92.01 dBc/ Hz and the power consumption by the circuit is 474.1408 μW. Table 3.2 summarizes the detailed performances frequency, phase noise, power consumption and FOM for the five stage CMOS ring oscillator. The achieved performance is in good agreement with the estimated performance.

Table 3. 2 Performance Summary of Five Stage CMOS Ring Oscillator

Performance Indices	Initial Design			Final Design		
	NSGA-II Estimated	Schematic Level Simulation	Post Layout Simulation	NSGA-II Estimated	Schematic Level Simulation	Post Layout Simulation
Oscillation Frequency (GHz)	2.0	2.0006	1.8526	2.0	2.1311	1.9864
Phase Noise (dBc/Hz at 1 MHz offset)	-90.64	-90.72	-91.37	-92.0859	-91.4	-92.01
Power Consumption (µW)	344	342.4	340.2273	480	477.7038	474.1408
Figure of Merit (FOM) (dBc/Hz)	-161.2950	-161.3981	-161.4079	-161.2940	-161.1808	-161.2124

Case II: Seven Stage Ring Oscillator

For the seven-stage CMOS ring oscillator the design parameters for all the transistors found from NSGA –II based design method are given in Table 3.3. The seven stage CMOS RO physical layout, oscillations generated, phase noise and power consumption measurements are shown in Figures 3.17, 3.18 3.19 and 3.20 respectively. The schematic and layout level performance parameters for initial optimized circuit and parasitic inclusive optimized circuit are presented in Table 3.4.

Table 3. 3 Design Parameters for Seven Stage CMOS RO

Design Parameters	Lower Limit	Upper Limit	Initial Value	Final Value
W_n(nm)	120	1000	549.6	780
W_p(nm)	200	2000	916	1300
L(nm)	100	300	242	230

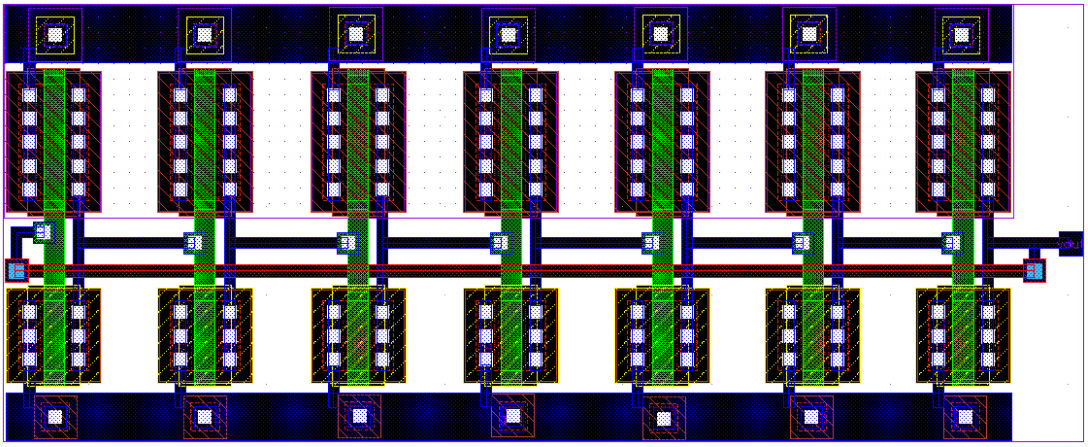

Figure 3. 17 Physical Layout of Parasitic Aware Seven stage CMOS Ring Oscillator

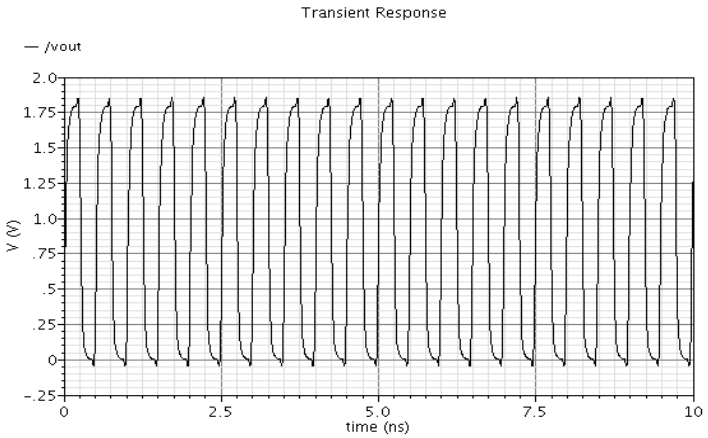

Figure 3. 18 The Oscillations produced by Parasitic Aware Seven Stage CMOS Ring Oscillator

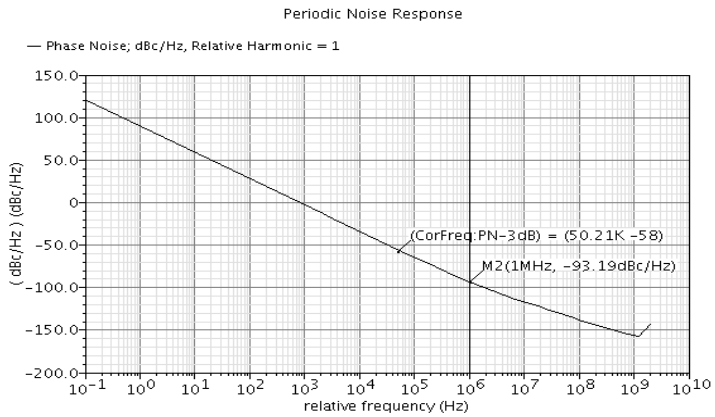

Figure 3. 19 Phase Noise plot for Parasitic Aware Seven Stage CMOS Ring Oscillator

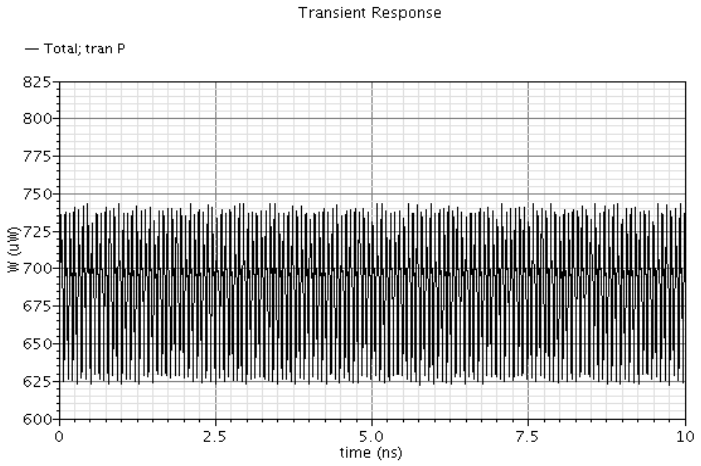

Figure 3. 20 Power Estimation plot for Parasitic Aware Seven Stage CMOS Ring Oscillator

Table 3. 4 Performance Summary of Seven stage CMOS Ring Oscillator

Performance Indices	Initial Design			Final Design		
	NSGA-II Estimated	Schematic Level Simulation	Post Layout Simulation	NSGA-II Estimated	Schematic Level Simulation	Post Layout Simulation
Oscillation Frequency (GHz)	2.0	1.9918	1.8466	2.0	2.1649	2.0108
Phase Noise (dBc/Hz at 1 MHz offset)	-92.34	-91.88	-92.49	-94.3658	-92.57	-93.19
Power Consumption (µW)	476	466.4	465.5934	711	694.4198	688.3375
Figure of Merit (FOM) (dBc/Hz)	-161.5845	-161.1775	-161.1376	-161.8677	-160.8626	-160.8796

Case III: Eleven Stage Ring Oscillator

The design parameter summery for eleven-stage CMOS RO is given in Table 3.5. The layout design, oscillations, phase noise plot and power consumption measurements are depicted in Figures 3.21, 3.22, 3.23 and 3.24 respectively. The performance of eleven-stage CMOS ring oscillator is summarized in Table 3.6.

Table 3. 5 Design Parameters for Eleven stage CMOS RO

Design Parameters	Lower Limit	Upper Limit	Initial Value	Parasitic Value
W_n(nm)	120	1000	399.8	385
W_p(nm)	200	2000	666.3	645
L(nm)	100	300	184	170

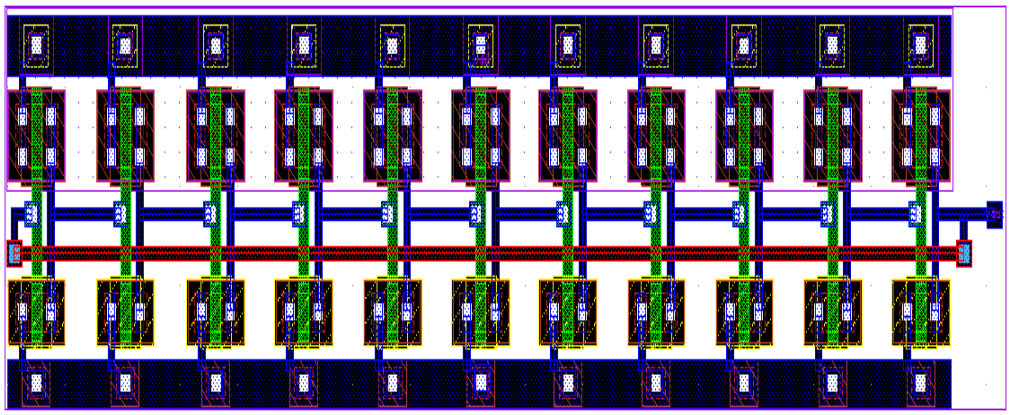

Figure 3. 21 Physical Layout of Parasitic Aware Eleven stage CMOS Ring

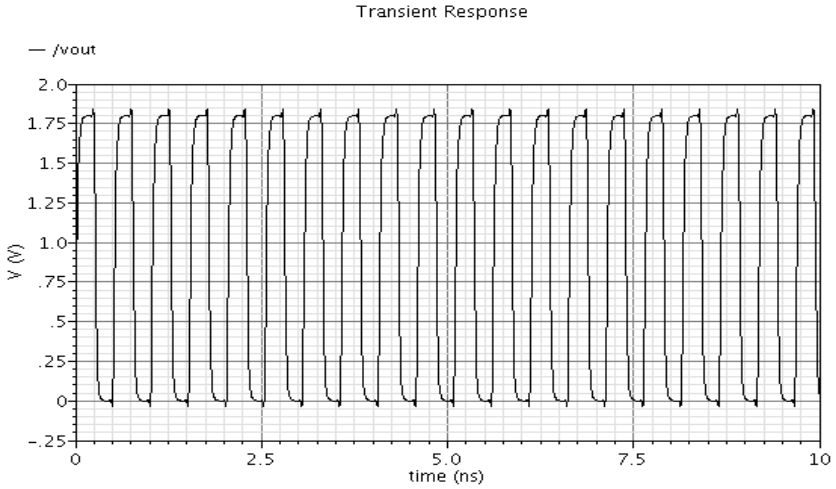

Figure 3. 22 The Oscillations produced by Parasitic Aware Eleven Stage CMOS Ring Oscillator

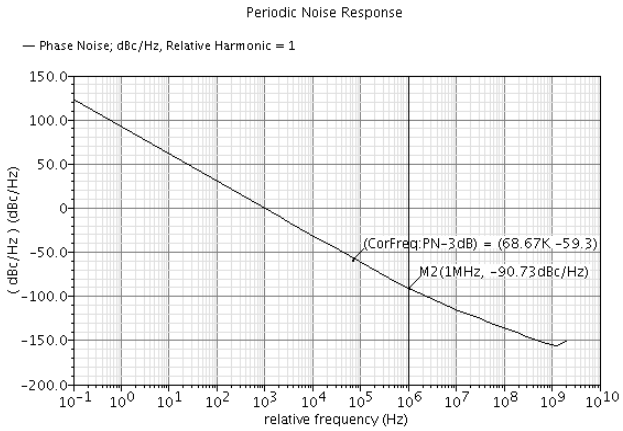

Figure 3. 23 Phase Noise plot for Parasitic Aware Eleven Stage CMOS Ring Oscillator

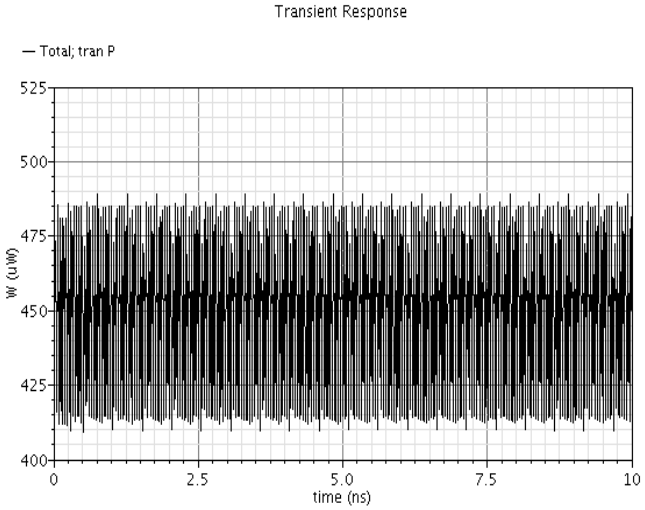

Figure 3. 24 Power Estimation plot for Parasitic Aware Eleven stage CMOS Ring Oscillator

Table 3. 6 Performance Summary of Eleven stage CMOS Ring Oscillator

Performance Indices	Initial Design			Final Design		
	NSGA-II Estimated	Schematic Level	Post Layout	NSGA-II Estimated	Schematic Level	Post Layout
Oscillation Frequency (GHz)	2.0	2.0003	1.7261	2.0	2.2792	1.9667
Phase Noise (dBc/Hz at 1 MHz offset)	-92.55	-91.01	-92.26	-92.9927	-89.53	-90.73
Power Consumption(μW)	455	437.6	429.3359	472	455.7637	449.9002
Figure of Merit (FOM) (dBc/Hz)	-161.9904	-160.6211	-160.6733	-162.2738	-160.0985	-160.0738

All the three cases for CMOS ring oscillators show good agreement of estimated and observed parameter values and also the improvement in performance when actual parasitics are taken into account in the design optimization process.

3.5.2 Current Starved VCO

The next circuit considered is the case of a thirteen stage current starved voltage controlled oscillator (CSVCO) which finds many applications. The frequency of the oscillation to be generated by this circuit is again taken 2 GHz as in the case of CMOS ring oscillator. Here apart from the geometrical dimensions of the inverter MOSFETs, the geometrical dimensions of the current starving NMOS and PMOS

transistors are the design parameters. As earlier the length of all transistors are kept identical. The geometrical limiting constraints are different from the ring oscillator case. The current starving transistors are set to have higher value of design parameters to allow better control of current for each of inverting stages. The final parasitic aware optimal design values along with the geometrical parameter constraints for CSVCO are presented in Table 3.7. Figure 3.25 elucidates the physical layout of the parasitic aware CSVCO circuit optimized for superior performance.

Table 3. 7 Design parameters for CMOS CSVCO

Design Parameter	Lower Limit	Upper Limit	Parasitic Aware Value
Wn	200 nm	500 nm	435 nm
Wp	400 nm	1 µm	940 nm
Wncs	1 µm	5 µm	1.26 µm
Wpcs	5 µm	20 µm	5 µm
L	100 nm	110 nm	105 nm

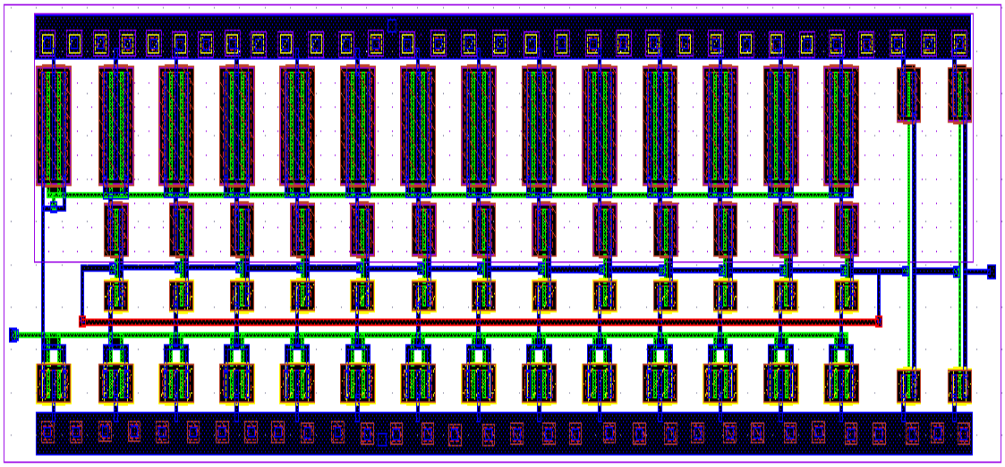

Figure 3. 25 Physical Layout of Parasitic Aware Thirteen Stage Current Starved VCO

The CSVCO designed here generates oscillations (Figure 3.26) of frequency 1.9561GHz. The phase noise measured at 1MHz offset is -90.29 dBc/Hz and power consumed by the circuit is 564.123 μW. The reported figure of merit (FOM) is -158.6462. Figures 3.27 and 3.28 demonstrate the phase noise plot and power consumption by the CSVCO. The performance of the CSVCO is summarized in Table 3.8.

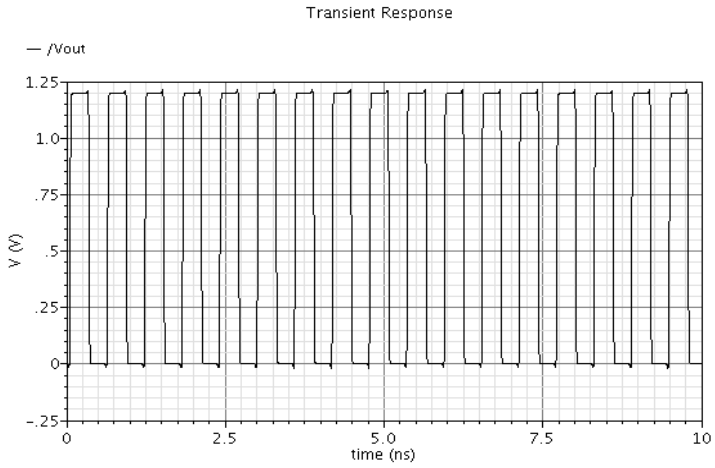

Figure 3. 26 Oscillations generated from the Parasitic Aware Current Starved VCO

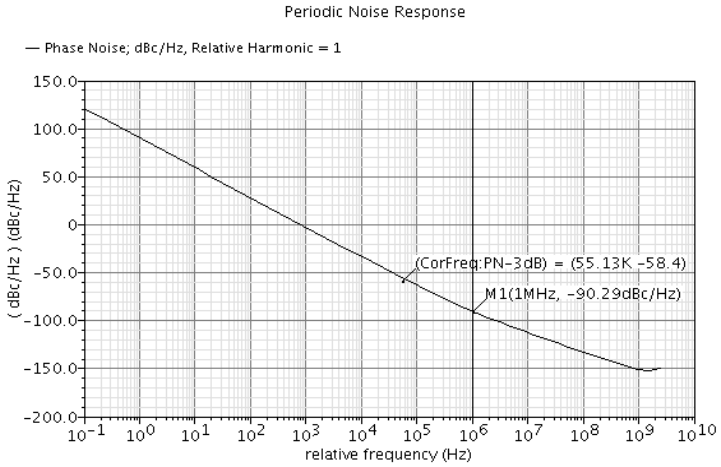

Figure 3. 27 Phase Noise Plot of the Parasitic Aware Current Starved VCO

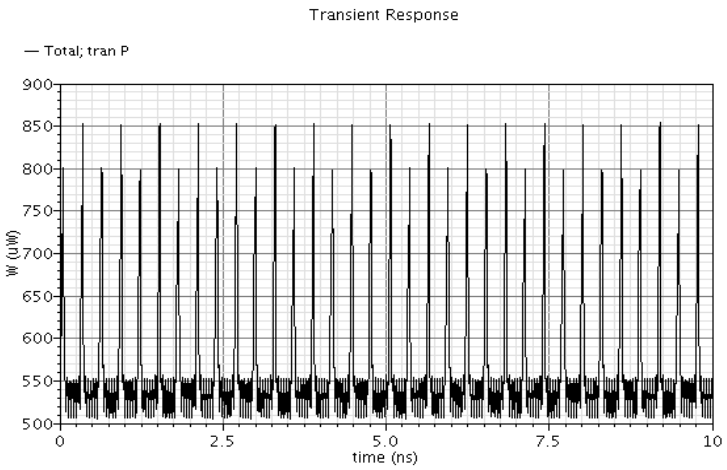

Figure 3. 28 Power Consumption of the Parasitic Aware Current Starved VCO

Table 3. 8 Performance Summery of the Parasitic Aware CSVCO

Performance Index	NSGA-II Estimated	Post Layout Simulation
Oscillation Frequency (GHz)	2.0	1.9656
Phase Noise (dBc/Hz at 1 MHz offset)	-91. 92	-90.29
Power Consumption(µW)	548	564.123
Figure of Merit (FOM) (dBc/Hz)	-160.5527	-158.6462

3.5.3 Differential VCO

Now the parasitic aware differential VCO is designed for a different frequency i.e. 2.4 GHz used for ISM (Industrial Scientific and Medical) applications. The design parameters for the NMOS, PMOS and tail NMOS transistors are provided along with their limits in Table 3.9. A four-stage differential VCO is designed whose layout for optimal performance is illustrated in Figure 3.29. The oscillations of the designed circuit (Figure 3.30) are of frequency 2.35888 GHz as compared to the expected 2.4 GHz.

Table 3. 9 Design Parameters for CMOS Differential VCO

Design Parameters	Lower Limit	Upper Limit	Parasitic Aware Value
W_p	120 nm	500 nm	310 nm
W_n	120 nm	10 µm	4.72 µm
W_{tail}	120 nm	10 µm	1.345 µm
L	100 nm	110 nm	105 nm

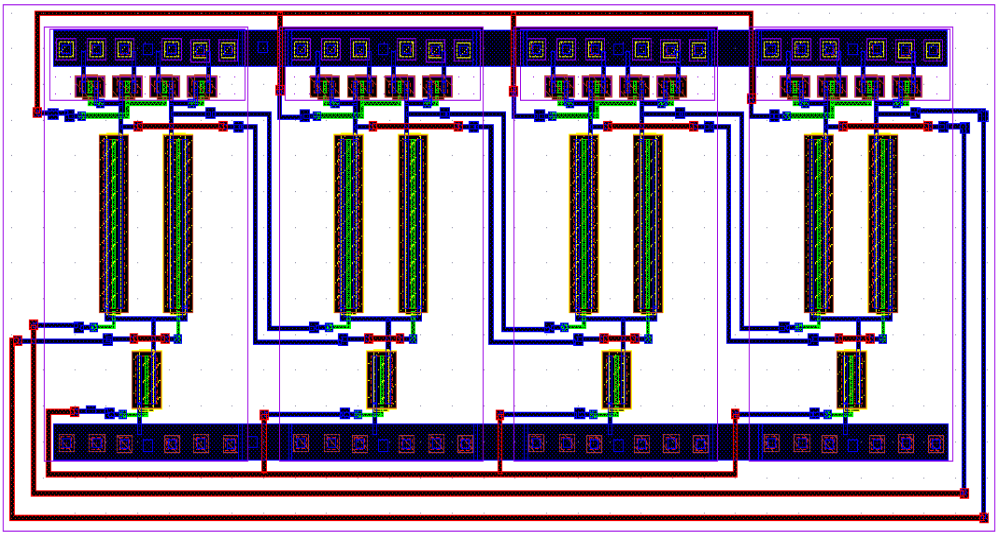

Figure 3. 29 Physical Layout of Parasitic Aware CMOS DVCO

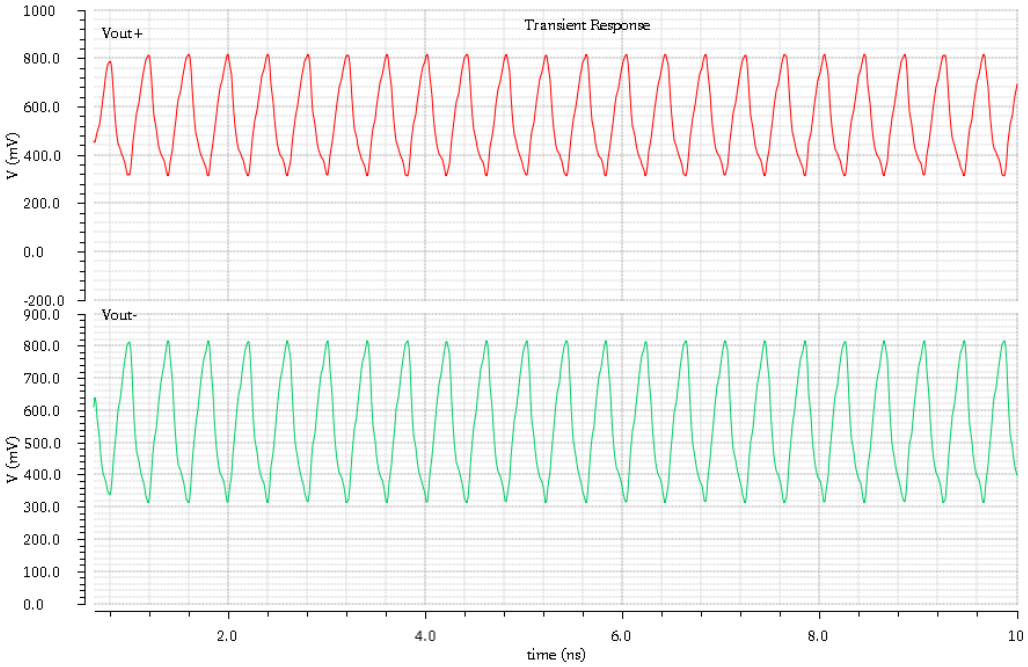

Figure 3. 30 Oscillations generated from the Parasitic Aware CMOS DVCO

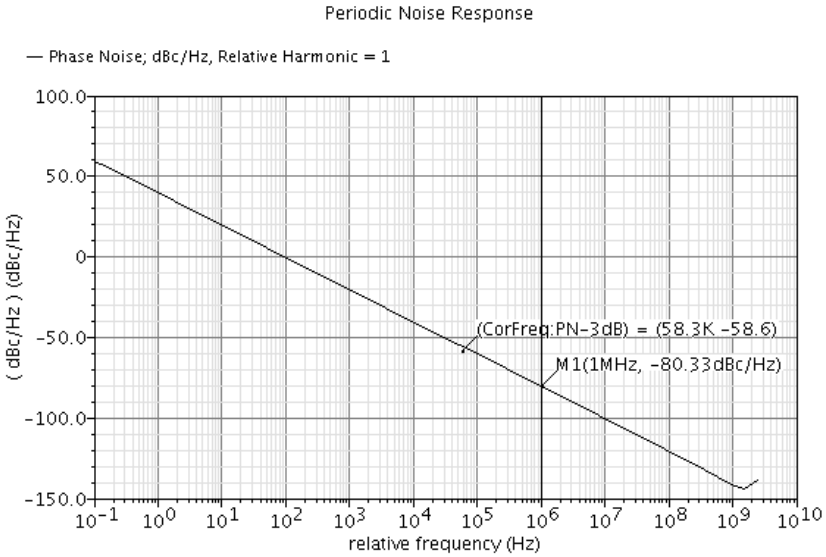

Figure 3. 31 Phase Noise Plot of the Parasitic Aware CMOS DVCO

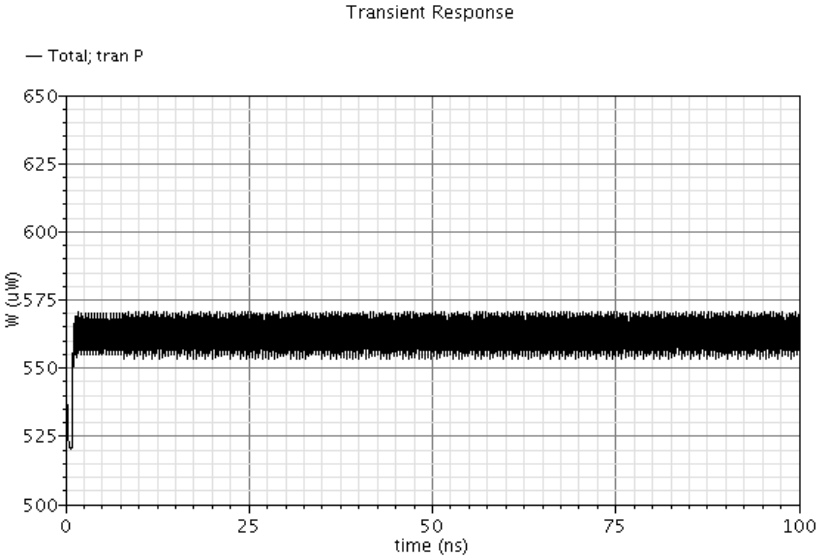

Figure 3. 32 Power Consumption of the Parasitic Aware CMOS DVCO

The pareto optimal values of phase noise at 1MHz offset and power consumption of the Differential VCO are -80.33 dBc/Hz (Figure 3.31) and 561.709 μW (Figure 3.32) respectively. The performance indices obtained through the design of the CMOS DVCO are given in Table 3.10.

Table 3. 10 Performance Summery of Parasitic Aware CMOS DVCO

Performance Index	Estimated by NSGA-II	Post Layout Simulation
Oscillation Frequency (GHz)	2.4	2.3588
Phase Noise (dBc/Hz at 1 MHz offset)	-78.70	-80.33
Power Consumption(μW)	606	561.709
Figure of Merit (FOM) (dBc/Hz)	-148.4794	-150.2890

3.6 Conclusion

The work of this chapter presents a novel design methodology for fast prototyping of CMOS VCOs with near optimal performance in nano scale regime. This methodology is based on multi-objective evolutionary technique NSGA-II where the parasitic effects are included during the design cycle. The design is fast because with a single run of the algorithm one gets the parameters of the optimized circuit for superior performance. This saves the design cycle time which is normally spent in hit and trial to attain higher performance. CMOS ring oscillators (RO), Current Starved VCO (CSVCO) and Differential VCO (DVCO) are designed with a specification frequency of 2 or 2.4 GHz for minimal phase noise and power consumption performance by using this methodology. The degrading effects of parasitics on oscillating frequency are taken care of efficiently in the two phases of optimization process to achieve the target frequency while simultaneously minimizing competing objectives, the phase noise and the power consumption with acceptable trade off. The application of this methodology on different VCO circuits for design and the subsequent analyses reveal that the proposed design methodology is very efficient and can seamlessly be extended to design any analog integrated circuit. This design approach helps the designer in industry to deliver a product with superior performance in significantly less time.

IDEA Based Fast Design Methodology of Nano-CMOS VCO for Performance Optimization

4.1 Introduction

There has been a continuous strive towards development of more efficient evolutionary computing optimization algorithms. Though NSGA-II is a standard multi-objective optimization algorithm, still a better technique available would be an obvious choice among the designers. Infeasibility driven evolutionary algorithm (IDEA) is a recently developed multi-objective optimization algorithm which has been reported [87] [88] [89] to offer superior performance. Inspired by Moore's law, integrated circuits always need to offer better performance. Under such a situation more efficient optimization technique like IDEA come as a rescue to the designers' burden of achieving a better performance in a given process technology. Therefore here IDEA is employed as a multi-objective optimization technique in the design of CMOS VCO circuit. This chapter in fact is similar to the previous one except that the new technique IDEA enables the designer to produce the ICs with better indices of performance measures. The design is also parasitic aware and works within various process constraints.

The remaining part of the chapter is organized as follows. The next section describes about the infeasibility driven evolutionary algorithm (IDEA). Section 4.3 elaborates proposed IDEA based design methodology for the CMOS VCO circuit for performance optimization. In Section 4.4, the performance analysis of the optimized circuit is presented. Finally, the finding of the study has been concluded in Section 4.5.

4.2 Infeasibility Driven Evolutionary Algorithm (IDEA)

The optimal solutions of the constrained multi-objective optimization problems very often lie along the constraint boundary. To effectively search along the constraint boundary, the original k objective constrained optimization problem is reformulated as k + 1 objective unconstrained optimization problem as given in (4.1). The first k objectives are the same as in the original constrained problem where as the additional objective is a measure of constraint violation, referred to as "violation measure".

The main steps of IDEA are outlined as follows.

Algorithm: Infeasibility Driven Evolutionary Algorithm (IDEA)
Require: N {Population Size}
Require: $N_G > 1$ {Number of Generations}
Require: $0 < \alpha < 1$ {Proportion of infeasible solutions}
1: $N_{inf} = \alpha * N$
2: $N_f = N - N_{inf}$
3: pop_1 = Initialize ()
4: Evaluate ($pop1$)
5: **for** $i = 2$ to N_G **do**
6: *child* pop_{i-1} = Evolve (pop_{i-1})
7: Evaluate (*child* pop_{i-1})
8: (S_f ,S_{inf}) = Split (pop_{i-1} +*child* pop_{i-1})
9: Rank (S_f)
10: Rank (S_{inf})
11: $pop_i = S_{inf}(1,N_{inf}) + S_f(1,N_f)$
12: **end for**

$$Minimize\ f_1'(x) = f_1(x), \ldots\ldots, f_k'(x) = f_k(x)$$
$$f_{k+1}'(x) = \text{Constraint Violation Measure} \quad (4.1)$$

Just like NSGA-II, an offspring population is evolved from parents selected by binary tournament using the crossover and mutation operations. The simulated binary crossover (SBX) [90] as given in (4.2) is used by IDEA.

$$y_i^1 = 0.5[(1+\beta_{q_i})x_i^1 + (1-\beta_{q_i})x_i^2]$$
$$y_i^2 = 0.5[(1-\beta_{q_i})x_i^1 + (1+\beta_{q_i})x_i^2] \quad (4.2)$$

Where β_{q_i} is estimated by (4.3)

$$\beta_{q_i} = \begin{cases} (2u_i)^{\frac{1}{(\eta_c+1)}}, & \text{if } u_i \le 0 \\ \left(\frac{1}{2(1-u_i)}\right)^{\frac{1}{\eta_c+1}}, & \text{if } u_i > 0 \end{cases} \quad (4.3)$$

And here u_i is an uniform random number and $u_i \in [0, 1)$ and η_c is the user defined parameter *Distribution Index for Crossover*. The polynomial mutation operator y_i has been used in this algorithm [91] defined as in (4.4)

$$y_i = x_i + (\overline{x_i} - \underline{x_i})\overline{\delta}_i \quad (4.4)$$

where $\overline{\delta}_i$ is calculated as

$$\overline{\delta}_i = \begin{cases} (2r_i)^{1/(\eta_m+1)} - 1 & \text{if } r_i < 0.5 \\ 1 - [2(1-r_i)]^{1/(\eta_m+1)} & \text{if } r_i \ge 0.5 \end{cases} \quad (4.5)$$

Where r_i is the uniform random number and $r_i \in [0, 1)$ and η_m is the user defined parameter *Distribution Index for Mutation*.

Crowding distance sorting [66] is used for preserving diversity among the population members which is described as follows.

Crowding Distance Mechanism

Algorithm: Crowding distance mechanism
Require: *F* {Non-dominated set}

1: *Ns* = |*F*| {Number of solutions in the non-dominated set}
2: *M* = Number of objectives
3: *F* (*i*).*dist* = 0 ∀ *i* = 1, 2, . . .*Ns* {Initialize distance}
4: **for** *m* = 1 to *M* **do**
5: *F* = *sort* (*F*, *m*) {Sort based on objective value}
6: *F* (1).*dist* = *F* (*Ns*).*dist* = ∞ {Assign infinity to the corner points}
7: **for** *i* = 2 to (*Ns* −1) **do**
8: *F* (*i*).*dist* = *F* (*i*).*dist* + (*F* (*i* + 1, *m*) − *F* (*i* − 1, *m*))/ ($f\,max_m - f\,min_m$)
{calculate *F(i).dist* based on neighboring points}
9: **end for**
10: **end for**
11: Higher *dist* ⇒Higher rank

IDEA differs from NSGA-II mainly in the mechanism for elite preservation. In IDEA, a few infeasible solutions are retained in the population at every generation. Individual solutions in the population are evaluated as per the original problem definition and marked infeasible if any of the constraints are violated. The solutions of the parent and the offspring population are divided into two sets, a feasible set (S_f) and an infeasible set (S_{inf}).The solutions in the feasible and the infeasible sets are both ranked using non-dominated sorting and crowding distance sorting of k + 1 objectives. NSGA-II, on the other hand, uses non-dominated sorting and crowding distance for ranking feasible solutions and ranks infeasible solutions in the increasing value of maximum constraint violation. For the feasible solutions, non-dominated sorting using k + 1 objectives is equivalent to the non-dominated sorting the original k objectives as the additional objective value (which is based on the constraint violations) for feasible solutions is always 0.

In the next step the solutions that form the population for the next generation are chosen. In IDEA, a user-defined parameter α is used to identify the proportion of the infeasible solutions to be retained in the population. The numbers N_f ($= (1 - \alpha\ ) \times N$) and N_{inf} ($= \alpha\ \times N$) denote the number of feasible and infeasible solutions in the population respectively, where *N* is the population size. If the infeasible set S_{inf} has more than N_{inf} solutions, then first N_{inf} solutions are selected based on the rank; otherwise all the solutions from S_{inf} are selected. The rest of the solutions are selected from the feasible set S_f , provided there are at least N_f number of feasible solutions. If S_f has fewer solutions, all the feasible solutions are selected and the rest are filled with infeasible solutions from S_{inf}. The solutions are ranked from 1 to *N* in order of their selection. That is how; the infeasible solutions that get selected first (at most S_{inf}), get higher rank than the feasible solutions.

In NSGA-II, the elite preservation mechanism weeds out the infeasible solutions from the population. To retain the infeasible solutions in the population, an alternate mechanism is required. In IDEA, the infeasible solutions are ranked higher than the

feasible solutions, thus adding selection pressure to generate better infeasible solutions. Presence of infeasible solutions with higher ranks than the feasible solutions translates into an active search through the infeasible space. This feature of IDEA accelerates the movement of solutions towards the constraint boundary. With the modified problem definition and ranking of the infeasible solutions higher than the feasible solutions, IDEA can find the solutions to the original problem more efficiently.

The constraint violation measure in the IDEA differentiates its performance from NSGA-II. The additional objective in the modified problem formulation is based on the amount of relative constraint violation among the population members. The constraint violation measure of a solution is based on the constraint violation levels for all constraint values for that solution. All the solutions in the population are sorted in ascending order based on the value of the constraint violation for constraint g_i. The solutions that do not violate the constraint g_i are assigned constraint violation value of 0 (and g_i do not contribute to the violation measure of those solutions). Rest of the solutions are assigned a constraint violation level for constraint g_i based on the sorted list, starting with rank 1 for the solution with least constraint violation. Solutions with the same value of constraint violation get the same rank. This ranking procedure is repeated for all the constraints. The constraint violation measure for each solution is then calculated as the sum of the ranks (based on constraint violation level) obtained for all the constraints.

4.3 IDEA based Parasitic Aware Design Methodology of VCO for Performance Optimization

The proposed IDEA based design flow of VCO performance optimization is depicted in Figure 4.1 and illustrated below.

The required specifications, the design space constraints and the reference circuit model are the inputs to the IDEA processing block. The primary goal of this processor is to determine the design parameters of all transistor elements in the VCO circuits. The implicitly parasitic dependant analytic equations of power consumption

and phase noise constitute the optimization objectives of the IDEA processor. This processor is allowed to explore the optimal solutions in a limited design space with a very marginally tolerable frequency drift around the target frequency of the VCO. With these initial optimized design parameters the VCO schematic and subsequent physical layout are designed in Cadence Virtuoso Analog Design Environment (ADE). The physical layout so generated is subjected to RCLK (Resistance, Capacitance, Inductance, and Mutual Inductance) parasitic extraction. The algorithm starts with the reference circuit model (with SPICE parameters), and in every iteration of design, the design parameters are obtained. The layout of the circuit is drawn and the post layout RCLK parasitic extraction is performed. Then the circuit model parameters are modified with the inclusion of the extracted parasitics. These modified circuit model parameters are used as the input to the IDEA processor block in place of the reference circuit model in the next iteration of the design. This provides the IDEA processor with a near exact parasitic aware model of the circuit which includes not only the logic parasitics but also the interconnect parasitic estimates. Hence the IDEA block provides the final level parasitic aware performance optimized design parameters for the VCO circuit. These design parameters are utilized to generate the physical layout of the circuit with near optimum performance, which can be taped out for fabrication.

Therefore, the final design parameters obtained from this methodology meets the desired specifications along with global best optimal performance parameters.
The IDEA based optimization processing can be stated as

$$Minimize \quad \underset{P}{\mathcal{L}\{\Delta f\}}$$

$$Subject\ to \quad \left.\begin{array}{l} f_{osc} = f_{\ Specification} \\ W_{min} < W < W_{max} \\ L_{min} < L < L_{max} \\ \left|g_{mn} - g_{mp}\right| \leq \delta \end{array}\right\} \tag{4. 6}$$

Where g_{mn} and g_{mp} are the transconductance parameters of NMOS and PMOS respectively, δ is a very small positive definite constant. Simulated binary crossover (SBX) and polynomial mutation operators are used in IDEA to generate offspring from a pair of parents selected using binary tournament. Individual

solutions in the population are evaluated using the problem definition (4.6) and the infeasible solutions are identified. The solutions in the parent and offspring population are divided into a feasible set S_f and an infeasible set S_{inf}. The solutions in the feasible set and the infeasible set are ranked separately using the non-dominated sorting and crowding distance sorting based on the objectives

IDEA based Design Methodology of VCO for Performance Optimization

---

Set: N {Population Size}
Set: $N_G > 1$ {Number of Generations}
Set: $0 < \alpha < 1$ {Proportion of infeasible solutions}
1: $N_{inf} = \alpha * N$
2: $N_f = N - N_{inf}$
3: ***while*** Parameter Constraints C = [$W_{min} < W < W_{max}$, $L_{min} < L < L_{max}$] ***do***
4: pop1 = Initialize () *subject to C*
5: Evaluate $[L\{\Delta f\}\ (pop_1), P_{avg}(pop_1)]$
6: ***for*** $i = 2$ to N_G ***do***
7: $childpop_{i-1}$ = Evolve (pop_{i-1})
8: Evaluate $[L\{\Delta f\}\ (childpop_{i-1}), P_{avg}(childpop_{i-1})]$
9: $Compute\ D = |f_{osc} - f_{target}|$
10: ***if*** $D \leq \epsilon$ *then* S_f
else S_{inf}
end if
11: (S_f, S_{inf}) = Split ($pop_{i-1} + childpop_{i-1}$)
12: Rank(S_f)
13: Rank(S_{inf})
14: $pop_i = S_{inf}(1 : N_{inf}) + S_f(1 : N_f)$
15: ***end for***
16: ***end while***

---

as per (4.6). The solutions for the next generation are selected from both the sets to maintain infeasible solutions in the population. The infeasible solutions are ranked higher than the feasible solutions to provide a selection pressure to create better infeasible solutions resulting in an active search through the infeasible search space. The marginally infeasible solutions in IDEA very often prove beneficial trade-offs for the integrated circuit design. Hence the technique is more attractive than NSGA-II for application in IC design optimization problem.

The tuning parameters in IDEA algorithm are listed in Table 4.1

Table 4. 1 Tuning Parameters of IDEA Algorithm

Parameter Name	*Parameter Value*
Population size	200
No. of generations	100
Probability of crossover	0.9
Probability of mutation	0.1
Crossover index	10

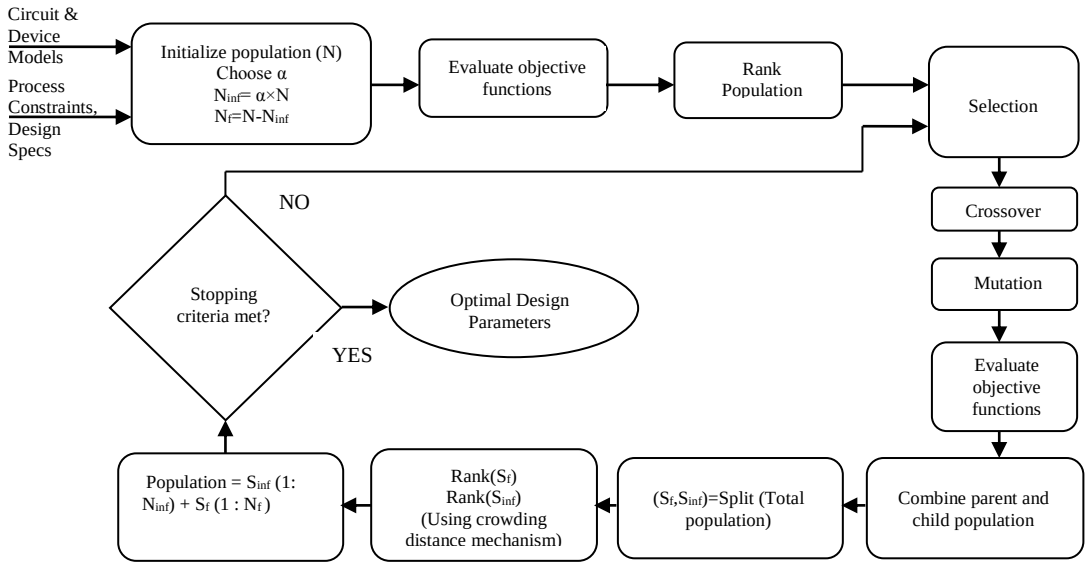

Figure 4. 1 The IDEA based Parasitic Aware VCO design flow

It is worth noting here that the final design is accomplished with only two runs of the IDEA algorithm and the designer has to draw the physical layout only once before the final physical layout taped out for fabrication. Hence the design process is very fast with almost no trials by the designer and also achieves performance optimization.

4.4 Performance Analysis

As has been carried out in the previous chapter, here three circuits of VCO viz. ring oscillator, current starved VCO and differential VCO are considered to validate

the proposed design methodology. The results of the design and simulation are compared with those presented by NSGA-II based methodology.

4.4.1 CMOS Ring Oscillator

For the five-stage CMOS RO the upper and lower limit constraints of design parameters are given in Table 4.2. The layout of the five-stage CMOS RO is presented in Figure 4.2 which yields oscillations (Figure 4.3) of frequency 2.0064 GHz. The phase noise at 1 MHz offset and power consumption are -93.37 dBc/Hz and 663.633 µW respectively. The phase noise plot and power consumption plot are depicted in Figures 4.4 and 4.5 respectively. The optimized performances for the circuit are presented in Table 4.3.

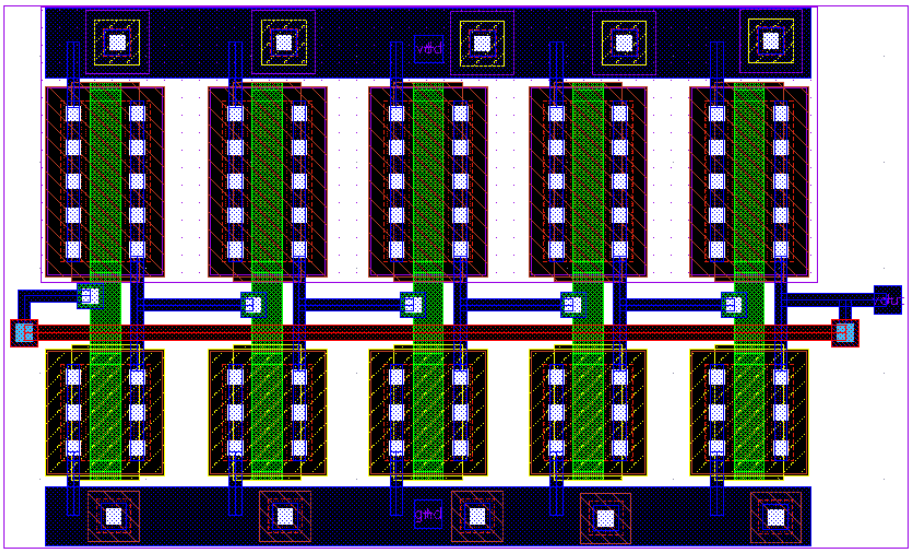

Figure 4. 2 Physical Layout of Five-Stage Parasitic Aware Ring Oscillator designed using IDEA

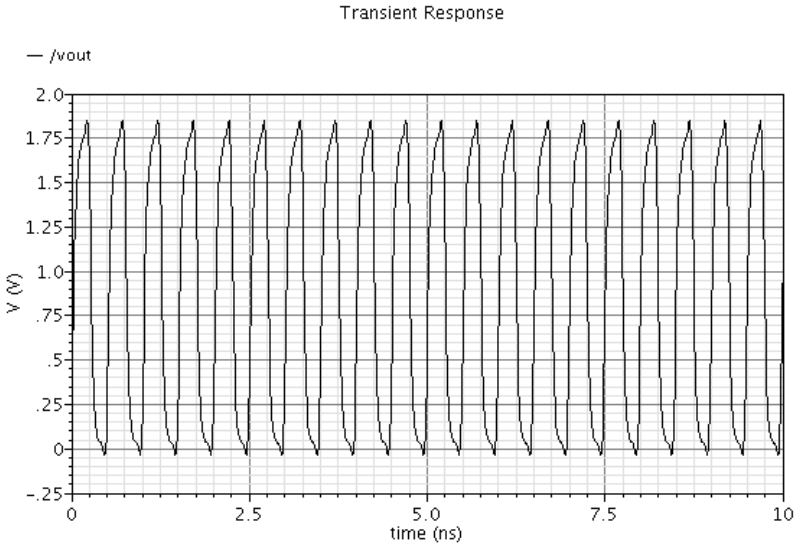

Figure 4. 3 Oscillations generated from the Five-Stage Parasitic Aware Ring Oscillator designed using IDEA

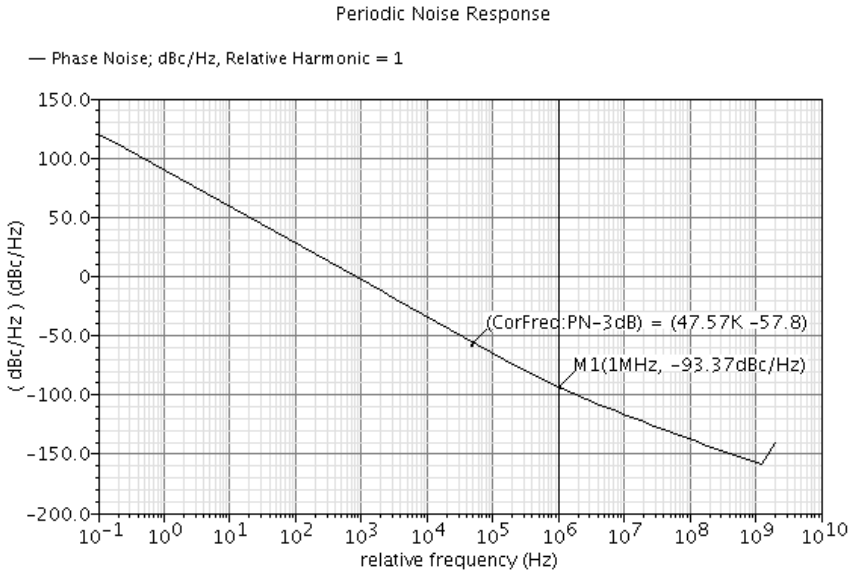

Figure 4. 4 Phase Noise plot of the Five-Stage Parasitic Aware Ring Oscillator designed using IDEA

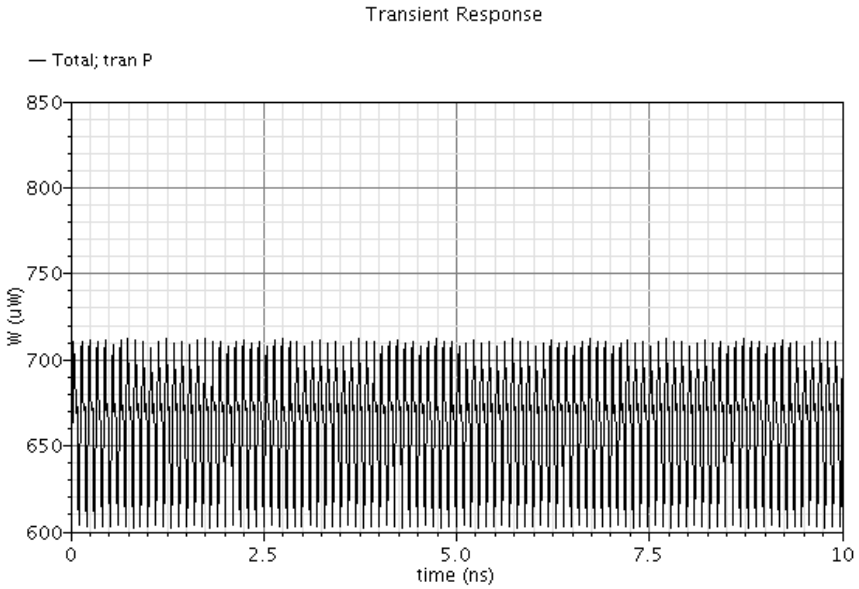

Figure 4. 5 Power Estimation plot of the Five-Stage Parasitic Aware Ring Oscillator designed using IDEA

Table 4. 2 Design Parameters of IDEA Optimized Parasitic Aware Nano-CMOS Ring Oscillator

Design Parameters	Lower Limit	Upper Limit	Parasitic Aware Optimal Value
Wn	120 nm	2 µm	915 nm
Wp	120 nm	10 µm	1.525 µm
L	100 nm	300 nm	285 nm

Table 4. 3 Performance Indices of Parasitic Aware IDEA Optimized Nano-CMOS Ring Oscillator

	Frequency of Oscillation (GHz)	Phase Noise (dBc/Hz at 1 MHz offset)	Power Consumption (µW)	FOM
IDEA Predicted	2	-93.65	665.714	-161.4424
Schematic Level	2.1202	-92.91	668.686	-161.1856
Post-layout level	2.0064	-93.37	663.693	-161.1987

The performance parameters of CMOS RO are observed in different process corners viz. SS, SF, FS, and FF apart from the normal NN case (shown in Figure 4.6).The frequency variation is maximum in SS and FF cases and a minimum in all other cases. The phase noise remains almost the same in all cases and maximum power is consumed in FF case. Table 4.4 presents a comparison of IDEA optimized performance with NSGA-II optimized performance. It can be observed that the frequency obtained from IDEA based method is more close to the target frequency, which is an important parameter of an oscillator, as compared to the NSGA-II based method. This is due to the fact that in both methods frequency objective is taken as a constraint and since IDEA is infeasibility driven and handles constraints more efficiently than NSGA-II, a better precision is achieved. Phase noise is improved but the power consumption is deteriorated due to trade off between them.

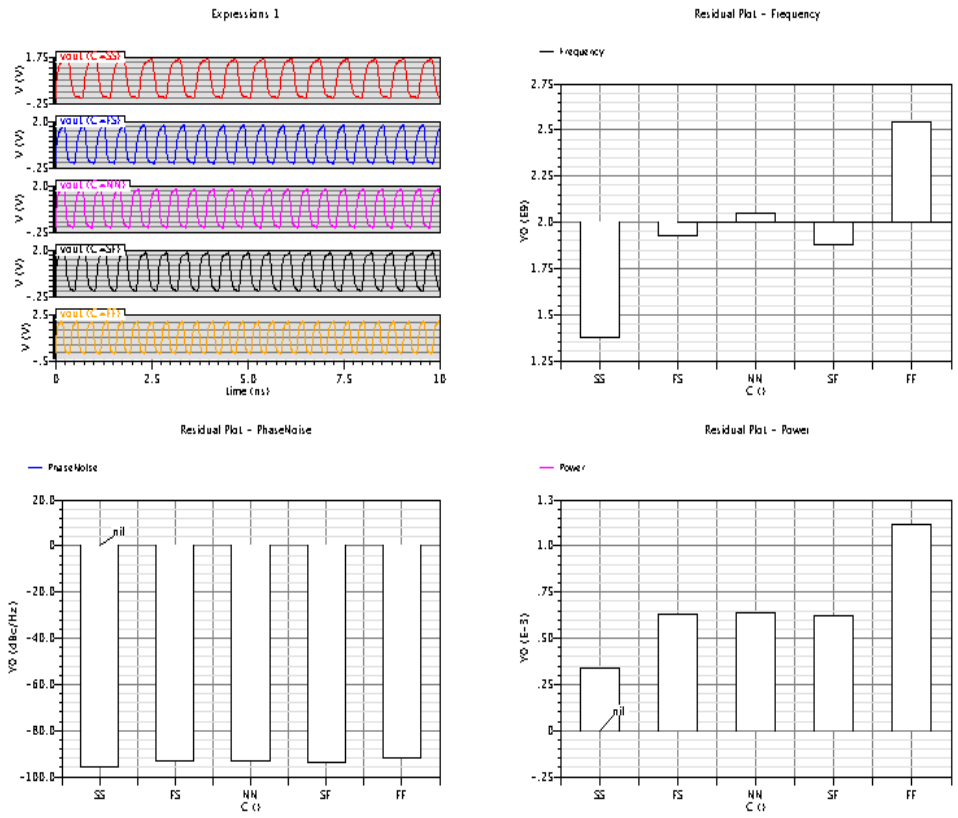

Figure 4. 6 Corner Analysis plots for Frequency, Phase Noise and Power of IDEA Optimized Five-Stage RO

Table 4. 4 Comparison of Performance Parameters of Parasitic Aware Five-Stage RO

Performance Measure	NSGA-II based Method	IDEA based Method
Frequency (GHz)	1.9864	2.0064
Phase Noise(dBc/Hz at 1 MHz offset)	-92.01	-93.37
Power (µW)	474.1408	663.6930
FOM (dBc/Hz)	-161.2124	-161.1987

4.4.2 CMOS Current Starved VCO

The current starved voltage controlled oscillator when subjected to parasitic aware IDEA based optimization for its power consumption and phase noise performance with target frequency and design parameter limits as constraints yields design parameter values listed in Table 4.5. Considering these parameters the physical layout is designed in Cadence Virtuoso Analog Design Environment (Figure 4.7).This design gives oscillations (Figure 4.8) of frequency 1.98846 GHz as compared to NSGA-II based technique which yields 1.96561 GHz. (in the same 90 nm process)

Table 4. 5 Design Parameters from IDEA Based Method

Design Parameter	Lower Limit	Upper Limit	Parasitic Aware Optimal Value
Wn	200 nm	500 nm	300 nm
Wp	400 nm	1 µm	505 nm
Wncs	1 µm	5 µm	1 µm
Wpcs	5 µm	20 µm	12.07 µm
L	100 nm	110 nm	100 nm

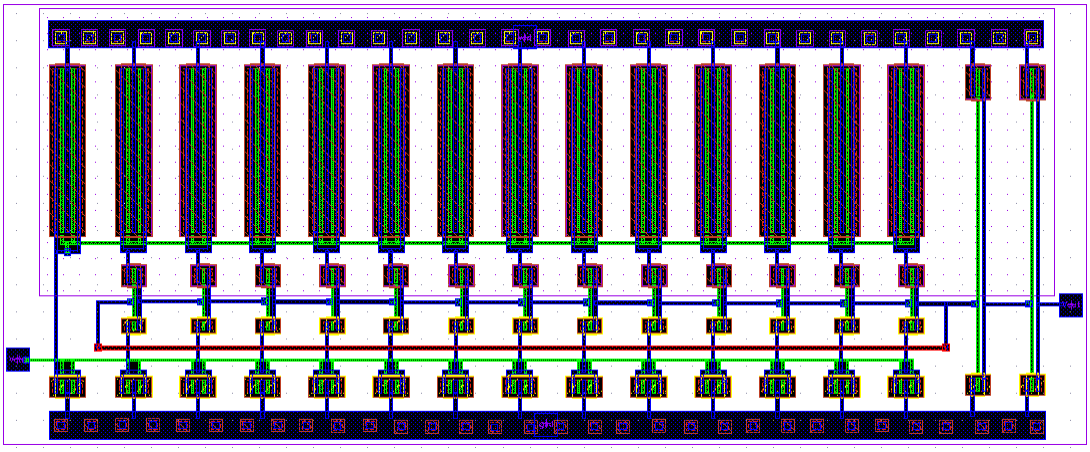

Figure 4. 7 The optimized parasitic and process variation aware physical layout of 13 stage CSVCO

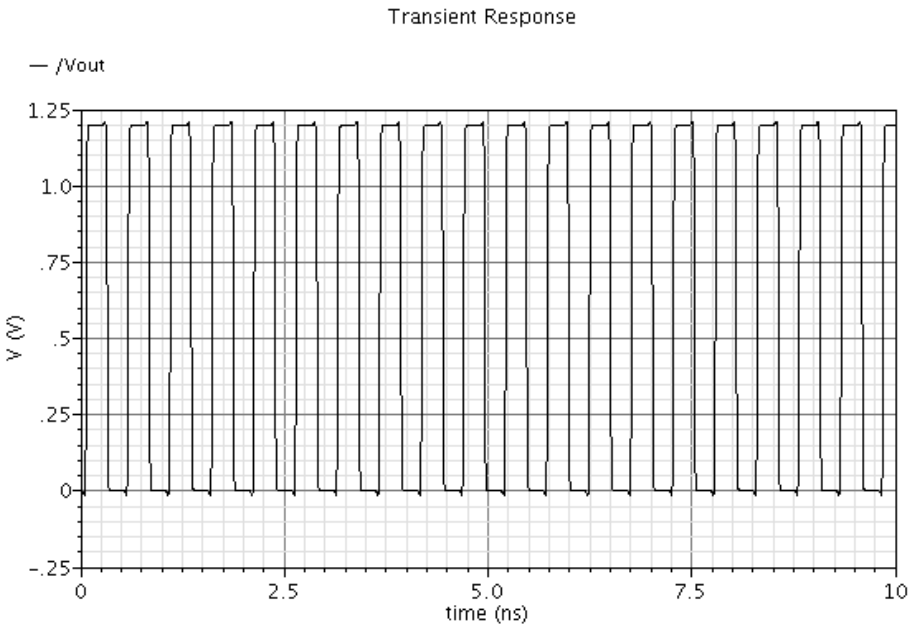

Figure 4. 8 Oscillations produced by Parasitic Aware CSVCO (IDEA based)

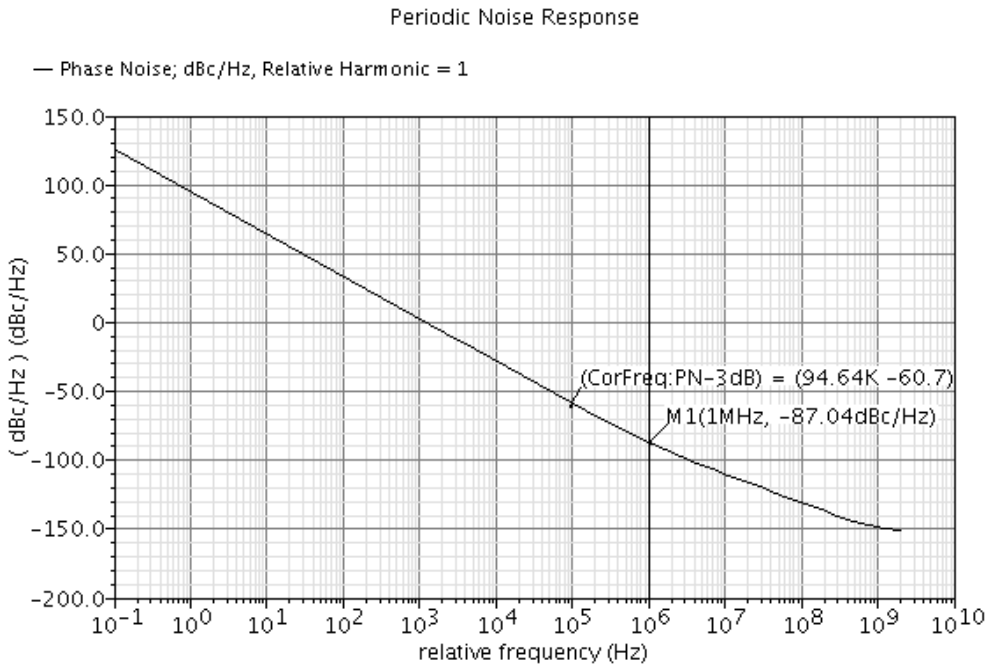

Figure 4. 9 Phase Noise plot for Parasitic Aware CSVCO (IDEA based)

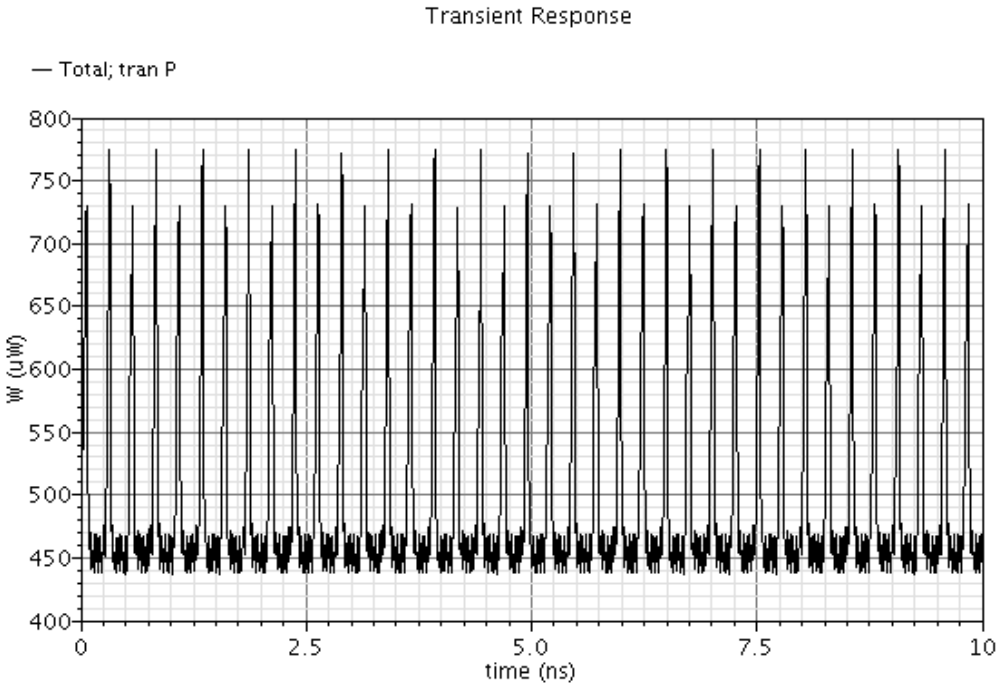

Figure 4. 10 Power Estimation plot of the Parasitic Aware CSVCO (IDEA based)

Figure 4.9 shows the phase noise plot of CSVCO where the phase noise value at 1 MHz offset frequency is -87.04 dBc/Hz. The average power consumption by the

CSVCO (Figure 4.10) is 496.0658 µW. Table 4.6 summarizes the performance of CSVCO at schematic and layout levels. The comparison of performance parameters obtained using IDEA based method and NSGA-II based method is provided in Table 4.7.

Table 4. 6 Performance Indices of Parasitic Aware Optimized Nano CMOS CSVCO

	Frequency of Oscillation (GHz)	Phase Noise (dBc/Hz at 1 MHz offset)	Power Consumption (µW)	FOM (dBc/Hz)
IDEA Estimated	2	-87.64	498.4632	-156.6842
Schematic Level	2.5385	-85.08	494.7281	-156.2281
Post-layout level	1.9884	-87.04	496.0658	-156.0550

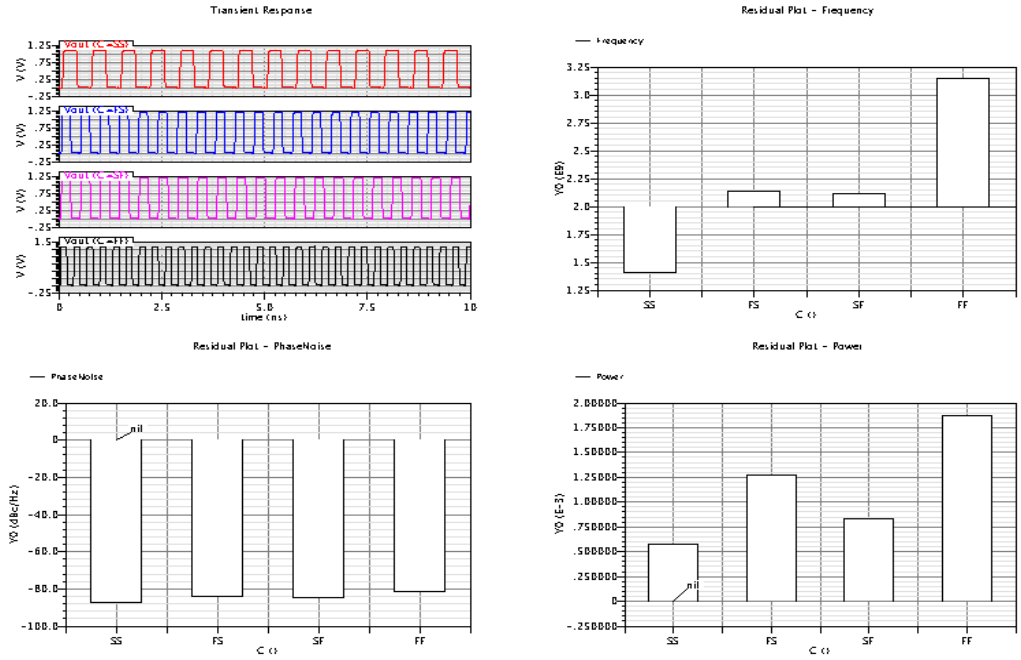

Figure 4. 11 Corner analysis plots for oscillations, frequency, phase noise and power consumption of the final Parasitic Aware CSVCO

Table 4. 7 Comparison of Performance Parameters of CSVCO

Performance Measure	NSGA-II based	IDEA based
Frequency (GHz)	1.9656	1.9884
Phase Noise (dBc/Hz at 1 MHz offset)	-90.29	-87.04
Power (µW)	564.1230	496.0658
FOM (dBc/Hz)	-158.6462	-155.8685
Convergence Time (seconds)	124.910	79.873

In IDEA constraint violation measure is more efficient so that the post layout simulated frequency is more closure to the target frequency which is set as an equality constraint in the optimization problem. The process corner analysis of the CSVCO is depicted in Figure 4.10 that demonstrates the frequency deviation in SS and FF corners which is quite natural. There is almost no deviation in phase noise.

4.4.3 Differential VCO

The design parameters obtained for differential VCO from the proposed IDEA based method are given in Table 4.8. The physical layout of the DVCO is shown in Figure 4.12 and oscillation obtained from the post layout simulation using Cadence Virtuoso Analog Design Environment is depicted in Figure 4.13.

The post layout frequency of oscillations of parasitic aware optimized DVCO circuit is 2.3995 GHz which is very near to the desired value. This is as expected because of the consideration of parasitic effects and better constraint handling in IDEA. The phase noise at 1MHz offset and power consumption are observed to be -79.67 dBc/Hz and 845.5095 µW respectively. Figure 4.14 shows the phase noise plot and Figure 4.15 shows the power estimation for the DVCO.

Table 4.9 lists the performance summary of the designed DVCO circuit. The IDEA based DVCO performance is compared with NSGA-II based circuit in Table 4.10. Here again the improved performance in frequency can be clearly observed. The corner analysis shown in Figure 4.16 also conforms the similar trend as observed in cases of CMOS RO and CSVCO.

Table 4. 8 Design Parameter of IDEA Optimized Nano-CMOS Differential VCO

Design Parameters	Lower Limit	Upper Limit	Parasitic Aware Value
W_p	120 nm	500 nm	491 nm
W_n	120 nm	10 µm	7.513 µm
W_{tail}	120 nm	10 µm	1.772 µm
L	100 nm	110 nm	101 nm

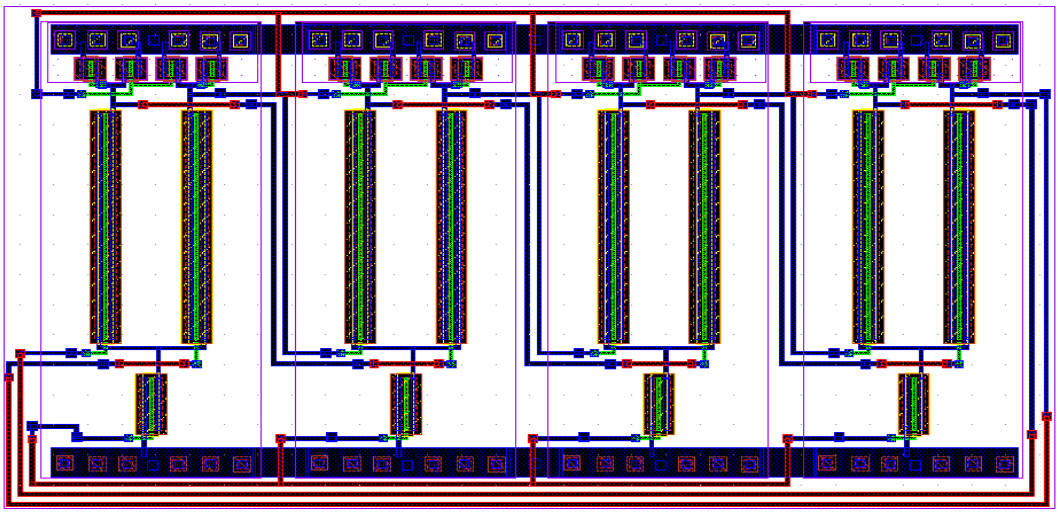

Figure 4. 12 Physical Layout of the Parasitic Aware DVCO (IDEA based)

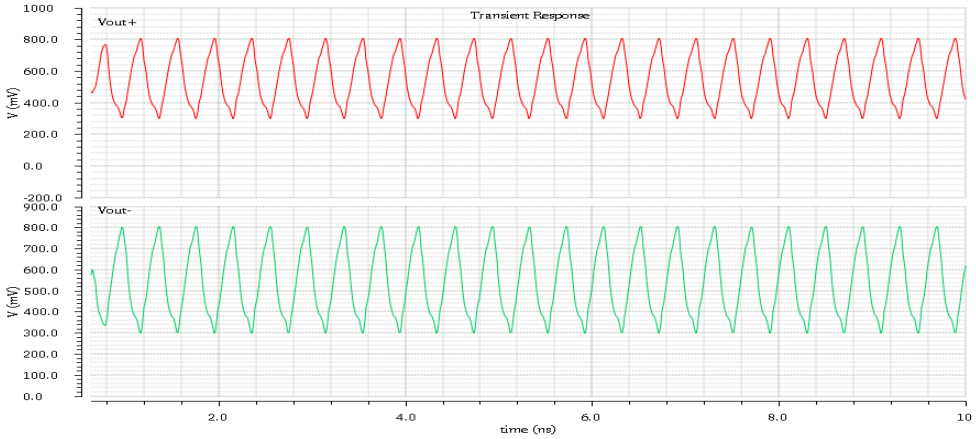

Figure 4. 13 Oscillations generated from the Parasitic Aware DVCO (IDEA based)

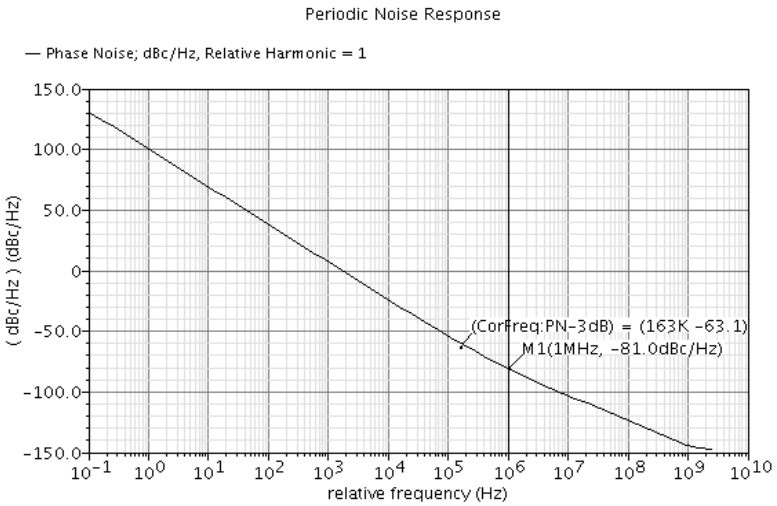

Figure 4. 14 Phase Noise plot of the Parasitic Aware DVCO (IDEA based)

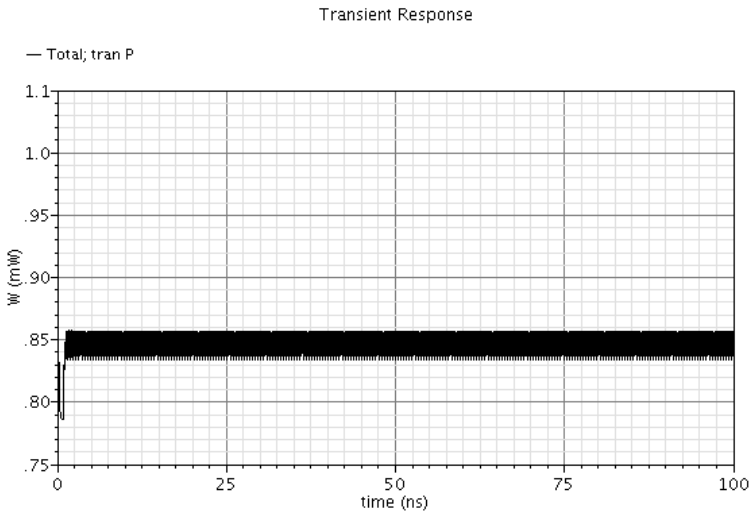

Figure 4. 15 Power Estimation plot of the Parasitic Aware DVCO (IDEA based)

The above reported values are listed in Table 4.9 where the FOM values are in good proximity with estimated values. The performance of the differential VCO designed using IDEA is compared with that designed using NSGA-II in Table 4.10. The frequency of oscillation in IDEA based design is observed to be more close to the required frequency.

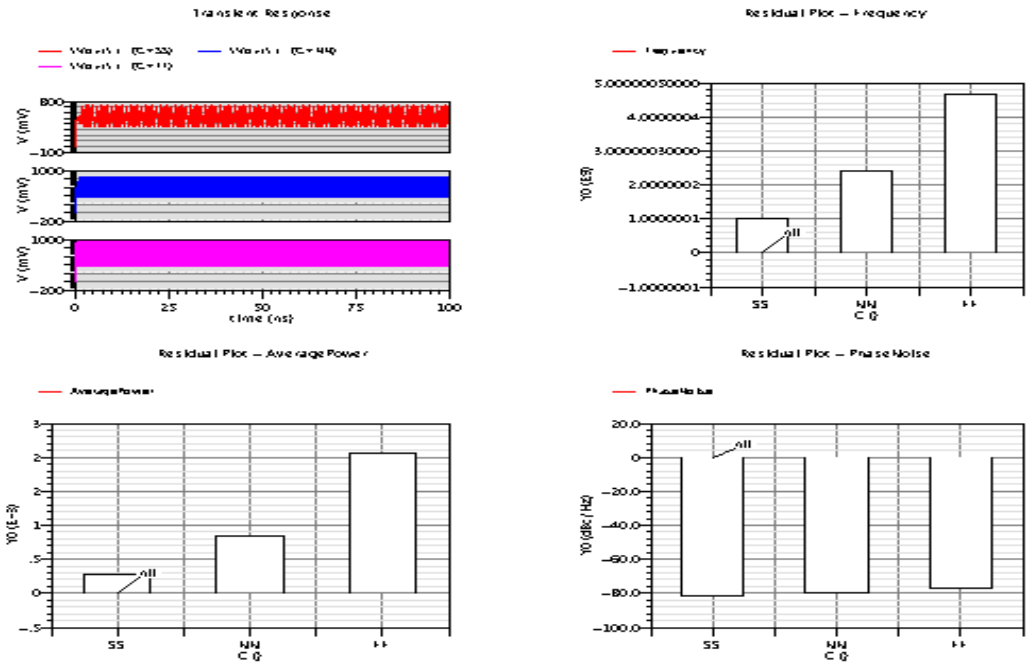

Figure 4. 16 Corner analysis plots for oscillations, frequency, power consumption and phase noise

Table 4. 9 Performance Indices of Parasitic Inclusive IDEA Optimized Nano-CMOS Differential VCO

	Frequency of Oscillation (GHz)	Phase Noise (dBc/Hz at 1 MHz Offset)	Power Consumption (μW)	FOM (dBc/Hz)
IDEA Estimated	2.4	-80.0757	841.416	-148.4298
Schematic Level	3.0778	-77.88	863.697	-148.3141
Post-layout level	2.3995	-79.67	845.509	-148.0515

Table 4. 10 Comparison of Performance Parameters of Parasitic Aware DVCO

Performance Measure	NSGA-II based Method	IDEA based Method
Frequency (GHz)	2.3588	2.3995
Phase Noise(dBc/Hz at 1 MHz offset)	-80.33	-79.67
Power (μW)	561.7090	845.5095
FOM (dBc/Hz)	-150.2890	-148.0515

4.5 Conclusion

A novel IC design methodology based on the efficient multi-objective optimization IDEA is presented. This technique predicts the performance behavior and the required design parameter values in a single run of the algorithm, providing a rapid way of first prototyping for complex ICs. The methodology is validated with three different VCO circuits viz. CMOS RO & CSVCO for 2 GHz frequency and differential VCO for 2.4 GHz frequency. The predicted behaviors are found to be in good agreement with the observed behaviors obtained from Cadence Virtuoso Analog Design Environment.

The IDEA based design methodology offers superior frequency precision as compared to NSGA-II based method. This is due to the better constraint handling and in the infeasibility driven procedure followed in IDEA, frequency of oscillation

is taken as an equality constraint. The other two performance parameters i.e. phase noise and power consumption are optimized and almost like NSGA-II based values in accordance to their pareto optimal behaviors.

Process Variation Aware Fast Design of VCO with Performance Optimization

5.1 Introduction

In the manufacturing process of ICs there are variations in different parameters which are not under the control the designer. With the device dimensions shrinking down to nano scale regime the IC fabrication uncertainties influence greatly their performances. This leads to increase in non performing ICs in a batch of production and hence the yield in the fabrication process is reduced. If the process variation extremities can be taken care of in the design phase itself then the number of ICs whose performance is outside the expected performance boundaries can be greatly reduced.

In [92] a conjugate gradient optimization method (integrally available in Cadence Virtuoso tools) is used for design of a voltage controlled oscillator. Here the design is reported to be parasitic and process variation aware with only objective of frequency of oscillations. This design method has very wide scope for improvement by use of efficient optimization techniques for multiple performance objectives.

In this work along with the parasitic aware optimization using IDEA the design is subjected to the worst case process variations. The proposed technique is validated through examples of CMOS ring oscillator, current starved voltage controlled oscillator and differential voltage controlled oscillator. Though the methodology is applied to VCO circuits here, it can be extended for design of any RFIC with multiple performance optimizations with practical constraints.

The remaining part of the chapter is organized as follows. Next section describes the fabrication process variations. Section 5.3 elaborates the proposed IDEA based process variation aware design methodology. In section 5.4, the

performance analyses of the optimized circuits have been carried out. Finally, the finding of the study has been concluded in section 5.5.

5.2 Fabrication Process Variations

The fabrication process of CMOS integrated circuits [93] is very much complex. They use a number of masks for many chemical process steps to deposit oxide layers and photoresist materials to transfer mask patterns to wafer with photo lithography, followed by chemical etchings. Although the fabrication steps are controlled by computers for high precision there remains some deviations in mask alignment, doping or implantation of targeted amounts of impurities, chemical etching of polysilicon gate lengths of MOS transistors and gate oxide thickness control. The parameters of the transistors vary from wafer to wafer or even among transistors of same die, depending upon the position.

The fluctuations like impurity concentration densities, oxide thickness and diffusion depths result in variations in values of sheet resistance and threshold voltage. Due to limitations in photolithographic process, device dimensions like widths and lengths of transistors and widths of interconnect wires also vary randomly [94].

Worst-case analysis is the most commonly used technique in industry for considering fabrication process tolerances in the design phase of integrated circuits. At any design point, uncontrollable fluctuations in the circuit parameters cause circuit performance to deviate from their nominal designated values. The objective of worst case analysis is to determine the worst values the performances that the IC may have under these statistical random fluctuations.

5.3 Fast Design Methodology for Optimized Parasitic and Process Variation Aware (PPVA) VCO

The proposed IDEA based fabrication process variation aware design flow of VCO for optimized performance is depicted in Figure 5.1. The process variation

aware design consists of two parts, the first one being *design optimization* and the other one *design robustification*.

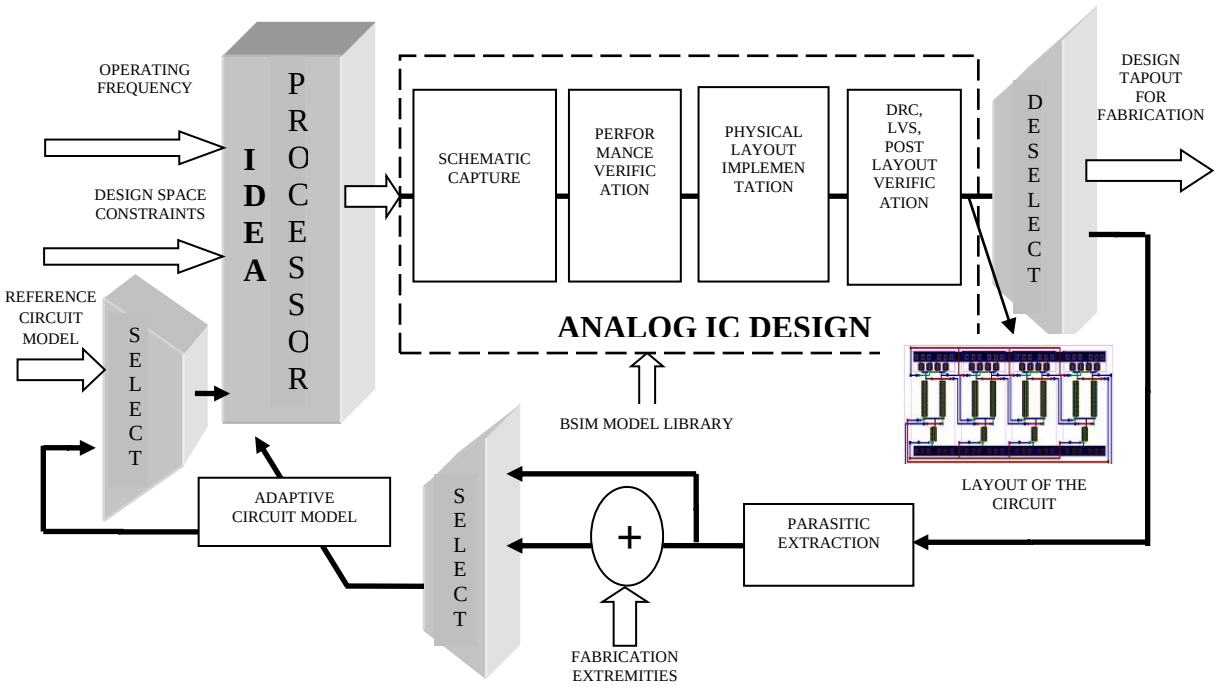

Figure 5. 1 Design flow of IDEA based Parasitic and Process Variation Aware VCO

A. Design Optimization

The required specifications, the design space constraints and the reference circuit model are the inputs to the IDEA processing block. The primary goal of this processor is to determine the design parameters of all transistor elements in the VCO for optimal performance. The implicitly parasitic dependant analytic equations of frequency, power consumption and phase noise constitute the optimization objectives of the IDEA processor. This processor is allowed to explore the optimal solutions in a limited design space with a very marginally tolerable frequency drift around the target frequency of VCO. With these initial optimized design parameters the VCO schematic and subsequent physical layout are designed in Cadence Virtuoso Analog Design Environment (ADE). The physical layout so generated is subjected to RCLK (Resistance, Capacitance, Inductance and Mutual Inductance) parasitic extraction. The algorithm starts with the reference circuit model (with SPICE parameters), and in every iteration of design, the design parameters for

optimal performance are obtained and the post layout RCLK parasitic extraction is performed. Then the circuit model parameters are adapted or modified with the inclusion of the extracted parasitic and process variation parameters. These modified circuit model parameters are used as the input to the IDEA processor block in place of the reference circuit model in the next iteration of the design. This provides the IDEA processor with a near exact parasitic aware and process variation aware model of the circuit which includes not only the logic parasitics and the interconnect parasitic estimates but also process variation parameters. Hence the IDEA block provides the final level parasitic and process variation aware, performance optimized design parameters for the VCO circuit. These design parameters are utilized to generate the optimized physical layout, which can be taped out for fabrication.

Therefore, the final design parameters obtained from this methodology meets the desired specifications along with possible best optimal performance parameters. The IDEA based optimization processing can be stated as

$$\begin{aligned} &Minimize \quad P^{\mathcal{L}\{\Delta f\}} \\ &Subject\ to \quad \left.\begin{array}{l} f_{osc} = f_{Specification} \\ W_{min} < W < W_{max} \\ L_{min} < L < L_{max} \\ \left|g_{mn} - g_{mp}\right| \leq \delta \end{array}\right\} \end{aligned} \tag{5.1}$$

where $g_{mn}$and g_{mp} are the transconductance parameters of NMOS and PMOS respectively, δ is a very small positive definite constant. $\mathcal{L}\{\Delta f\}$ and P are phase noise at Δf offset frequency and power consumption respectively. The frequency performance objective is included as a constraint to be handled by IDEA. It is worth noting here that IDEA handles the constraints very efficiently as compared to any other optimization algorithm. For CMOS ring oscillator and current starved VCO case f_{osc} considered is 2 GHz. However for the differential VCO case the f_{osc} is set to be 2.4 GHz. It may be mentioned here that the design parameters W and L for all the transistors are constrained to work within the specified limits.

B. Design Robustification

This part of the design is additional to the design presented in previous chapters and is the central contribution of this chapter. To make the circuit robust enough to work under random variations due to fluctuations in manufacturing processes and operating conditions, the possible process variations of the fabrication are incorporated in circuit model adaptation. The process parameters like V_{thn},V_{thp}, t_{oxn} ,t_{oxp} and external parameters like V_{DD} and T are allowed to vary between +10% and -10% and imposed as constraints in the IDEA optimization algorithm. The worst case analysis is performed on the VCO circuit designed with the parameters obtained from the IDEA processor to validate the robustness of the circuit.

It is worth noting here that the final design is accomplished with only two runs of the IDEA processing cycle and the designer has to draw the physical layout only once before the final physical layout taped out for fabrication. Hence the design process is very fast with almost no trials by the designer and the design is robust against process variations.

5.4 Performance Analysis

5.4.1 CMOS Ring Oscillator

The ring oscillator is designed to achieve 2 GHz oscillation frequency whose design parameters obtained from IDEA are given in Table 5.1.With these design parameters the physical layout drawn in Cadence environment is shown in Figure 5.2. The simulated oscillations, phase noise plot and power consumption are depicted in Figures 5.3, 5.4 and 5.5 respectively.

Table 5. 1 Design Parameters of Parasitic and Process Variation Aware CMOS RO

Design Parameters	Lower Limit	Upper Limit	Parasitic & Process Variation Aware Value(Obtained from IDEA)
Wn	120 nm	2 µm	710 nm
Wp	120 nm	10 µm	1.185 µm
L	100 nm	300 nm	275 nm

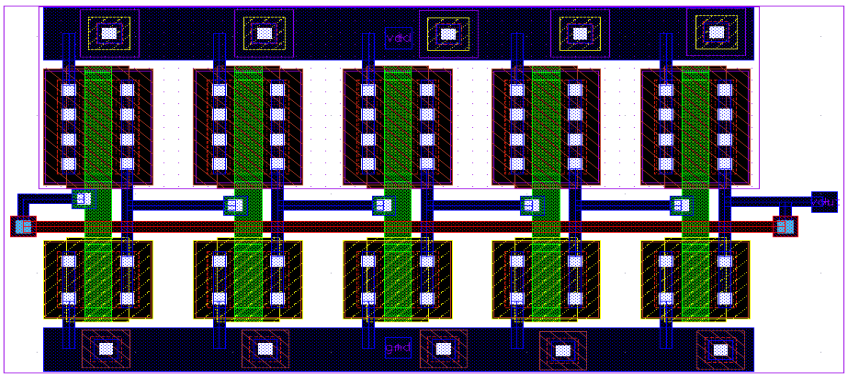

Figure 5. 2 Physical Layout of Parasitic & Process Variation Aware CMOS Ring Oscillator

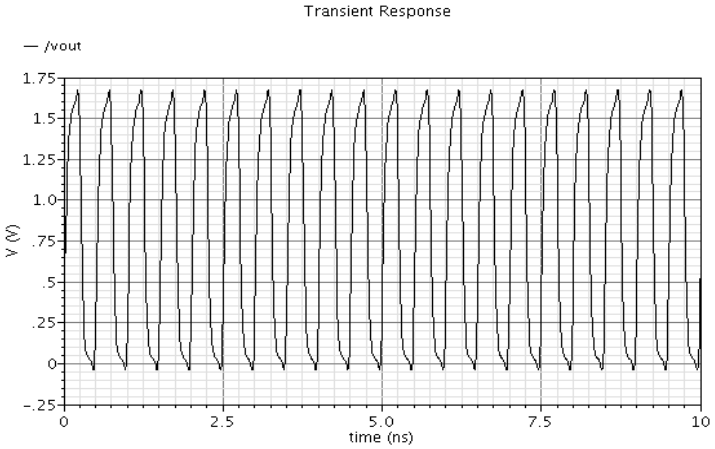

Figure 5. 3 Oscillations generated from the Parasitic & Process Variation Aware CMOS Ring Oscillator

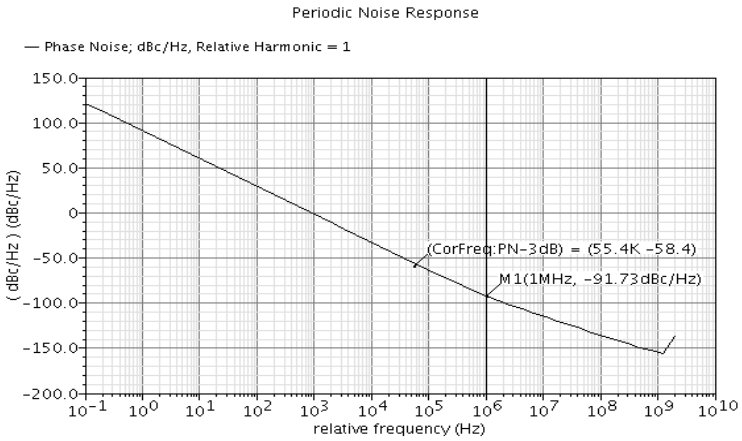

Figure 5. 4 Phase Noise Plot of the Parasitic & Process Variation Aware CMOS Ring Oscillator

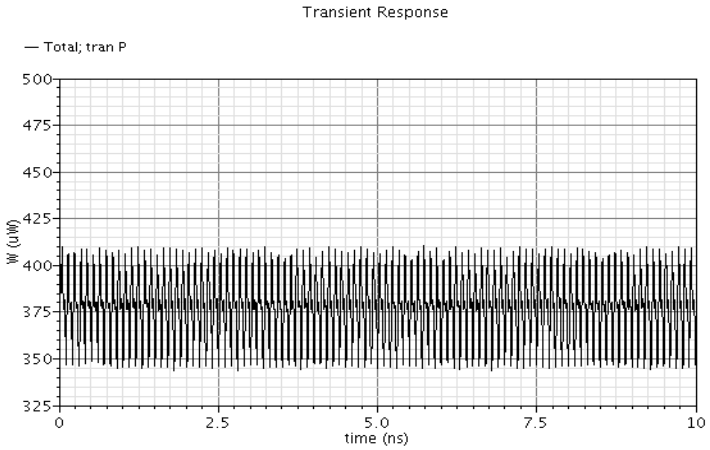

Figure 5. 5 Power Consumption of the Parasitic & Process Variation Aware Optimal CMOS Ring Oscillator

Table 5. 2 Performance Indices of Parasitic & Process Variation Aware Optimized Nano-CMOS Ring Oscillator

	Frequency of Oscillation (GHz)	Phase Noise (dBc/Hz at 1 MHz offset)	Power Consumption (µW)	FOM (dBc/Hz)
IDEA Estimated	2	-91.74	386.163	-161.8999
Schematic Level	2.1491	-91.15	380.758	-161.9887
Post-layout Level	2.0030	-91.73	377.836	-161.9909

Table 5.2 provides the performance indices of the CMOS RO. The post layout frequency of oscillation of the RO is 2.0030 GHz which is very close to the desired 2 GHz value and same is the case for phase noise measured at 1 MHz offset. The manufacturing process corner variations of waveform, frequency, phase noise and power consumption for NN, SS, SF, FS and FF cases are depicted in Figure 5.6. The exact measurements of process corners are given in Table 5.3. In Table 5.4, the complete performance summary is provided.

Table 5. 3 Summary of Process Corner Performance Analysis

Performance Parameter	SS	SF	FS	FF
Frequency (GHz)	1.3728	1.9267	1.8754	2.5458
Phase noise (dBc/Hz at 1 MHz offset)	-95.5776	-93.2659	-93.9610	-91.7960
Power Consumption (µW)	339.2	632.1	625.0	1117.0

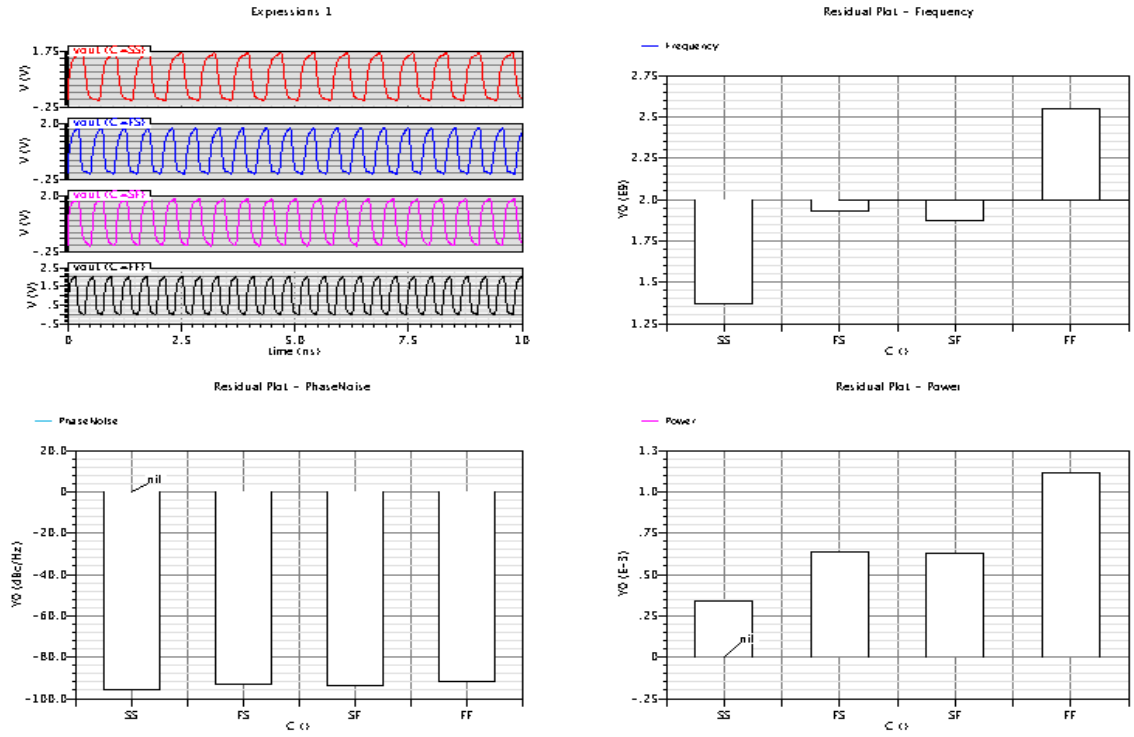

Figure 5. 6 The manufacturing process corner variation analysis of waveform, frequency, phase noise and power of parasitic and process variation aware ring oscillator

Table 5. 4 Performance Summary of Energy Efficient Low Phase Noise Robust CMOS Ring Oscillator

Parameter Name	Reported in this work
Technology	$90nm\ CMOS\ Salicide\ 1.2V/2.5V\ 1P\ 9M$
Supply Voltage (V_{DD})	$1.2\ V$
The Design Variables	$3(Wn, Wp, L)$
Number of Objectives	$3(f_{osc} >= 2GHz\ \&\ Minimize\ Phase\ Noise, Power)$
Initial Nominal Oscillation Frequency	$1.90665\ GHz$
PVT Variation Parameters	$V_{DD}(-10\%), V_{Th\_n}(+10\%), V_{Th\_p}(+10\%), T_{oxn}(+10\%), T_{oxp}(+10\%), Temperature$
Oscillation Frequency (Worst-Case PVT @ 27 ℃)	$2.0030\ GHz$
Phase Noise (Worst-Case PVT @ 27 ℃)	$-91.73\ dBc/Hz\ \ @\ 1\ MHz\ \ offset$
Average Power (Worst-Case PVT @ 27 ℃)	$377.836\ \mu W$

5.4.2 CMOS Current Starved VCO

The initial IDEA optimized circuit schematic is simulated in Cadence Virtuoso Analog Design environment. In the current design the IDEA processor targets the CSVCO circuit to produce oscillations of frequency 2 GHz. The schematic level estimated frequency of oscillations is 2.0009 GHz with the phase noise value of -88.33 dBc/Hz at 1MHz offset and the power consumption of 452.71 µW. The design parameters are listed in Table 5.5. It is clearly noticeable that the worst-case post layout oscillation frequency is 2.0064 GHz, which is very close to the IDEA estimation. The phase noise at 1 MHz offset is -87.71 dBc/Hz and power consumption is 765.641 µW which are in well acceptable agreement with the estimations.

Table 5.6 summarizes the performance of the parasitic and process variation aware CSVCO circuit. Table 5.7 compares those performances with other novel approaches on the same circuit reported in [92] [95] and [96]. The design approach presented here is entirely different from [92] and hence the performance achievement is considerable in the following aspects. Firstly, the difference between the target frequency and the frequency reported in this work is 6.42 MHz, which is very less in comparison to the difference of 90 MHz between the target frequency and the frequency reported in [92]. Secondly, the methodology presented here optimizes two other important IC design objectives phase noise and power consumption. Thirdly, this work reports CSVCO to occupy significantly less area in the same 90 nm process for its efficient optimization strategy.

Table 5. 5 Design Parameters of Parasitic and Process Variation Aware CSVCO

Design Parameters	Lower Limit	Upper Limit	Initial Value (Obtained from IDEA)	Parasitic and Process Variation Aware Value (Obtained from IDEA)
W_n	200 nm	500 nm	340 nm	355 nm
W_p	400 nm	1 µm	670 nm	740 nm
W_{ncs}	1 µm	5 µm	1 µm	3.5 µm
W_{pcs}	5 µm	20 µm	15.06 µm	5 µm
L	100 nm	110 nm	110 nm	100 nm

Table 5. 6 Final Optimized Performance Indices of PPVA CSVCO

Simulation Environments	Oscillation Frequency (GHz)	Phase Noise (dBc/Hz at 1 MHz offset)	Power Consumption (µW)
Nominal Case	2.3056	-87.20	1062.580
Worst Case (Predicted by IDEA)	2 .0	-87.68	798.364
Worst Case (Measured in Cadence)	2.0064	-87.71	765.641

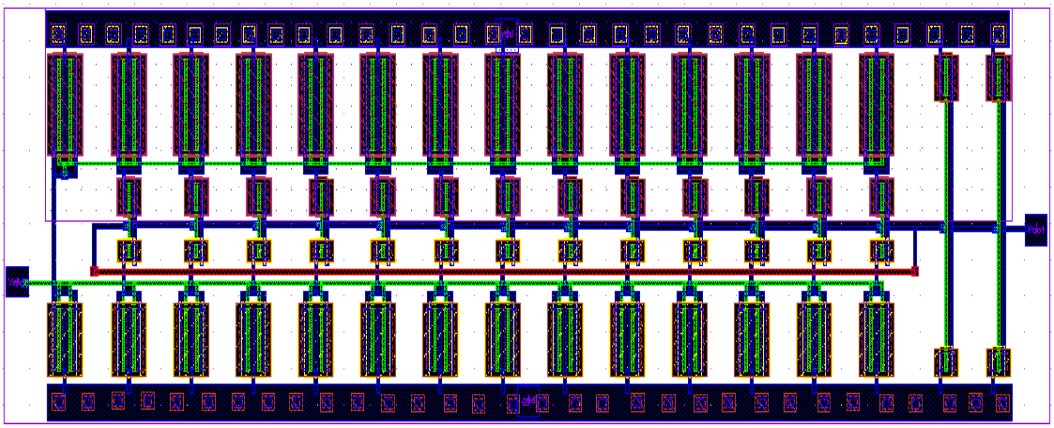

Figure 5. 7 Physical Layout of the Optimized Parasitic and Process Variation Aware Thirteen-Stage CSVCO

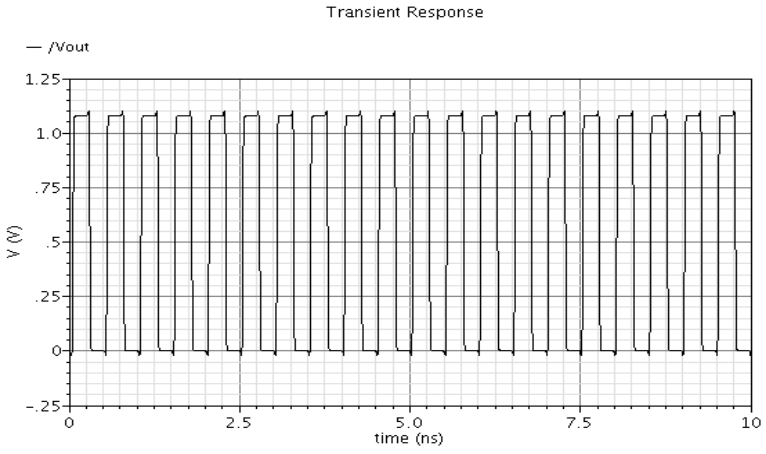

Figure 5. 8 Oscillations produced by the Optimized Parasitic and Process Variation Aware CSVCO

In [95] and [96] optimization is performed to minimize power with frequency constraint where 100 MHz frequency is targeted. In our proposed approach we report a substantially less deviation of 0.0485% (for 2 GHz) as compared to the deviation of 0.1% (for 100 MHz) reported in [95] in schematic level. The VCO

power deviation in this work is close to that reported in [95]. The power consumption in the proposed technique is expected to reduce further if we accept a little higher value of phase noise, which is a trade off case with the power consumption.

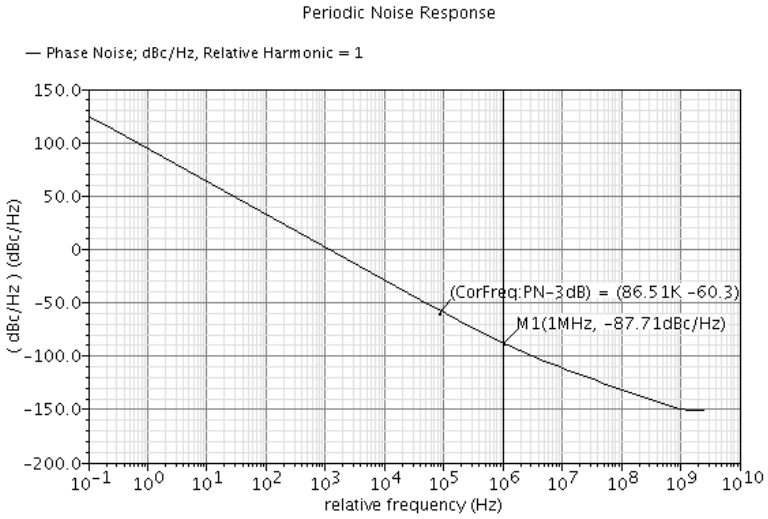

Figure 5. 9 Phase Noise plot of the Optimized Parasitic and Process Variation Aware CSVCO

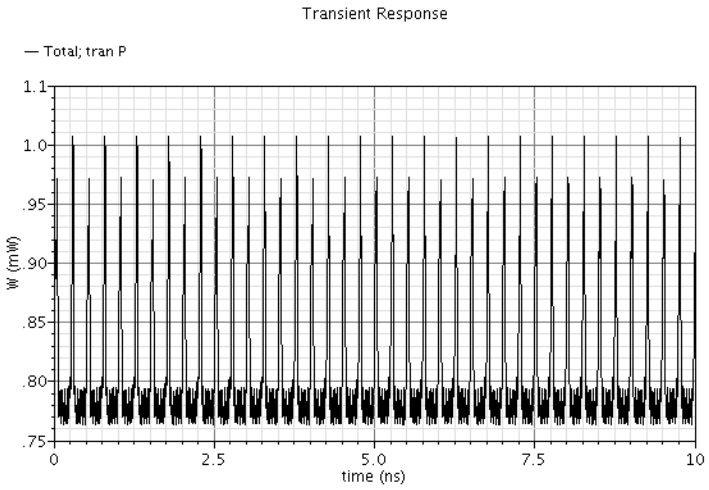

Figure 5. 10 Power estimation of the Optimized Parasitic and Process Variation Aware CSVCO

It is worth noting that the simultaneous minimization of VCO power and phase noise with process variations are the extra considerations in our report. More over the proposed technique is very much generic one which can also be seamlessly applied to design any other IC with some other Process Design Kit (PDK). The optimized parasitic and process variation aware physical layout of the thirteen-stage CSVCO is depicted in Figure 5.7. The simulation of final optimized physical design

yields the oscillations depicted in Figure 5.8. Figure 5.9 shows the phase noise plot. The power measurements in Cadence environment is given in Figure 5.10 and the oscillation frequency variation with control voltage is shown in Figure 5.11 and the tuning range is found out to be 1.15 GHz which is 57.5 % of the center frequency.

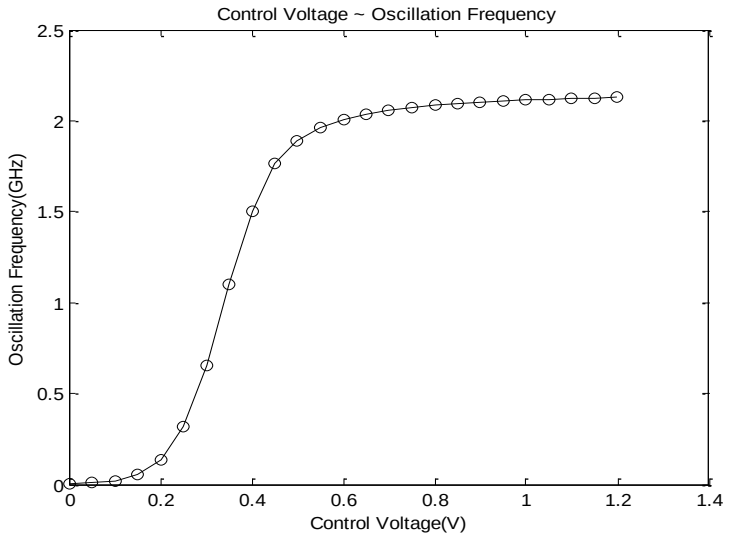

Figure 5. 11 Variation of oscillation frequency with control voltage of the Optimized Parasitic and Process Variation Aware CSVCO

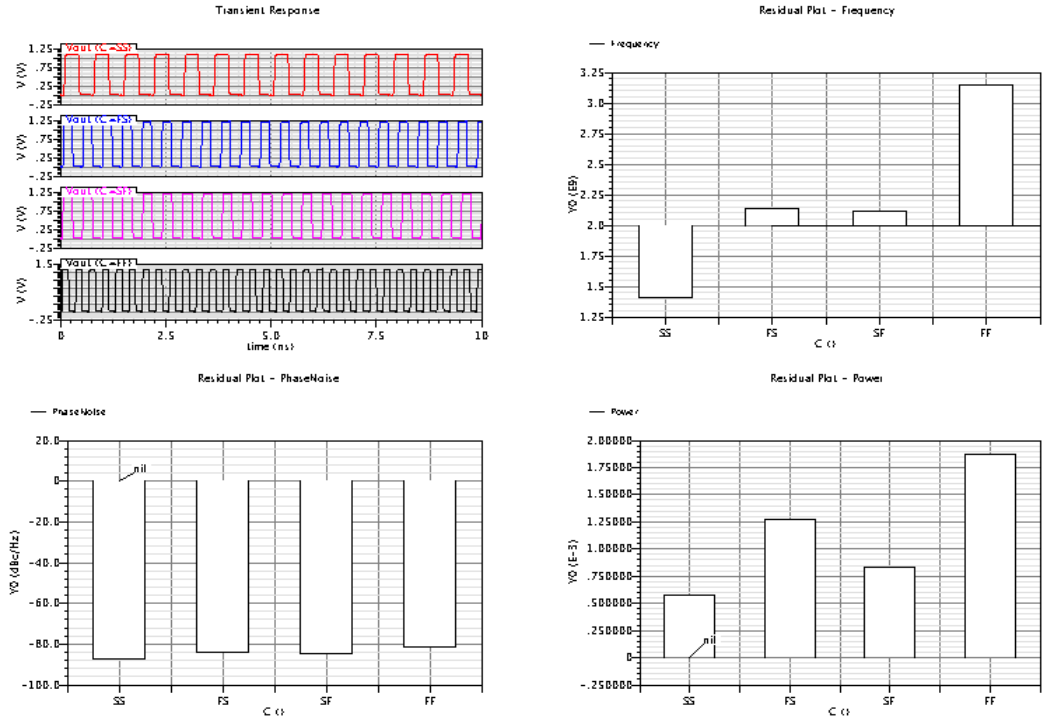

Figure 5. 12 Corner analysis of waveform, frequency, phase noise and power the Parasitic and Process Variation Aware CSVCO

Table 5. 7 Performance Summary and Comparison of PPVA CSVCO

Parameter	Reported in this work	Reported in [92]	Reported in [95] [96]
Technology	$90nm$ $CMOS\ Salicide\ 1.2V/2.5V\ 1P\ 9M$	$90nm$ $CMOS\ Salicide\ 1.2V/2.5V\ 1P\ 9M$	$45nm$ $CMOS\ Salicide\ 1V/2V\ 1P\ 9M$
Optimization Algorithm	IDEA	Conjugate gradient	Polynomial regression based GA
Desired Frequency of Oscillation (GHz)	2	2	0.100
Optimized Schematic Level Oscillation Frequency	2.0009 GHz (Deviation = 0.0485 %)	1.95 GHz (Deviation = -2.5 %)	0.1054 (Deviation = 0.1 %)
Optimized Schematic Level Power (μW)	412.710 (Deviation = 4.93 %)	–	50 (Deviation = 2.38 %)
Optimized Schematic Level Phase Noise ($dBc/Hz\ \ at\ 1\ MHz\ \ offset$)	-88.33	–	–
PVT Variation Effects	Included	Included	Not Included
Nominal Oscillation Frequency (GHz)	2.3056	2.54	–
Worst-Case Oscillation Frequency (*GHz*)	2.0064 *(Deviation = 0.321 %)*	1.91 *(Deviation = - 4.5 %)*	–
Phase Noise ($dBc/Hz\ at\ 1\ MHz\ \ offset$)	-87.71	–	–
Average Power Consumption (μW)	765.641	–	–
Physical Layout Area (μm^2)	0.9595	2.408	Layout Not Drawn
No. of Design Objectives	**3**(Frequency of Oscillation, Phase Noise & Power)	**1**(Frequency of Oscillation)	**1(**Weighted sum of Power and Frequency of Oscillation**)**

The comparison of performances of CSVCO with other works reported in literature presented in Table 5.7 shows that the difference in oscillation frequency between nominal case and worst case is 299.18 MHz as compared to 630 MHz reported in [92]. Apart from the significant improvement in frequency precision, the phase noise and the power consumption values are found to be -87.71 dBc/Hz and 765.641 μW respectively. These values are very close to the IDEA predicted global minimum values at the desired frequency of oscillations. The process corner variation analysis of the final optimal CSVCO is depicted in Figure 5.11, which verifies its robustness.

The comparison with other related works in literature has been carried out for CSVCO but could not have been done for RO or the DVCO presented next because of the non-availability of the related results in the literature.

5.4.3 Differential VCO

The DVCO is considered here for optimization of phase noise and power consumption with a goal to achieve a targeted frequency 2.4 GHz which can be used in WLAN transceiver equipments. Table 5.8 lists the design parameter values for parasitic and process variation aware DVCO.

Table 5. 8 Design Parameter of Optimized PPVA Nano-CMOS Differential VCO

Design Parameters	Lower Limit	Upper Limit	Parasitic & Process Variation Aware optimal value
W_p	120 nm	500 nm	460 nm
W_n	120 nm	10 µm	3.325 µm
W_{tail}	120 nm	10 µm	1.165 µm
L	100 nm	110 nm	110 nm

The final physical design of the parasitic and process variation aware optimal differential VCO has been realized by using the design parameters obtained from the second level optimization in a generic 90 nm Salicide 1.2V/2.5V 1P 9M (one poly nine-metal) CMOS process. The optimized parasitic and process variation inclusive physical layout of the four-stage differential VCO is depicted in Figure 5.13. Care has also been taken to minimize the area overhead by using multi-fingered MOSFETs in the physical layout.

The oscillations generated by the parasitic and process variation aware DVCO are shown in Figure 5.14. Figures 5.15 and 5.16 show the phase noise plot and power consumption respectively of the DVCO designed here.

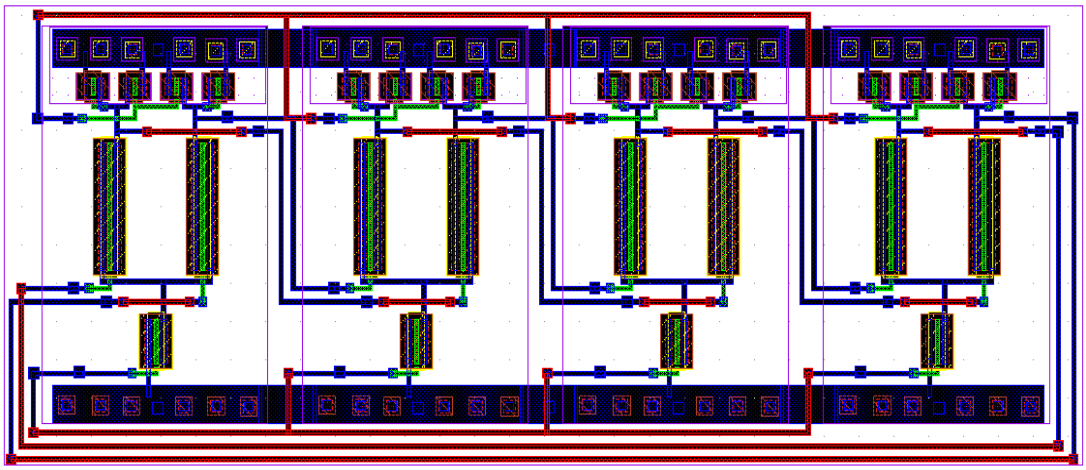

Figure 5. 13 Physical Layout of Parasitic & Process Variation Aware DVCO

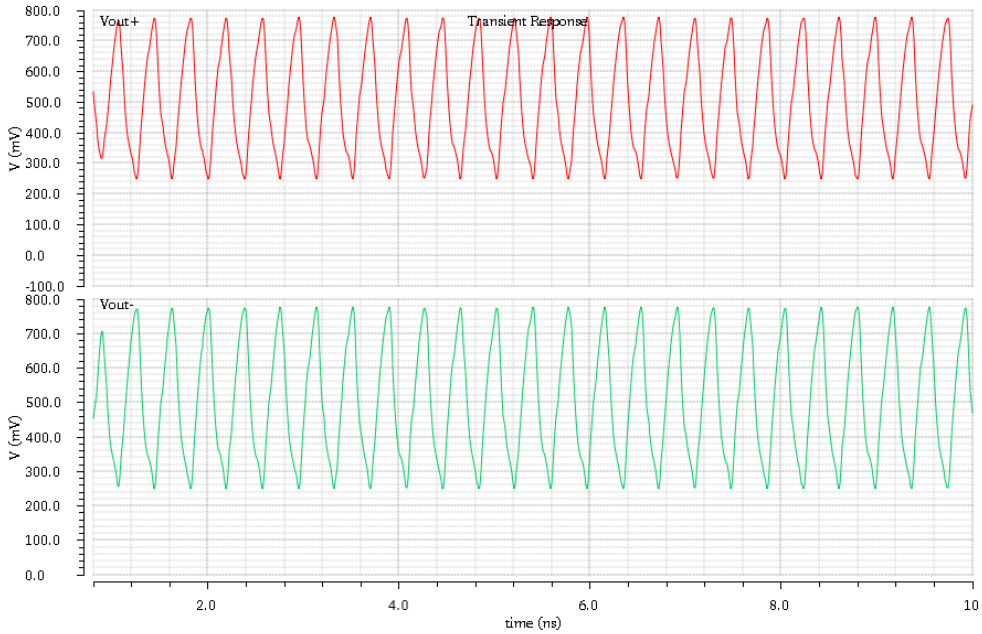

Figure 5. 14 Oscillations generated from the Parasitic & Process Variation Aware DVCO

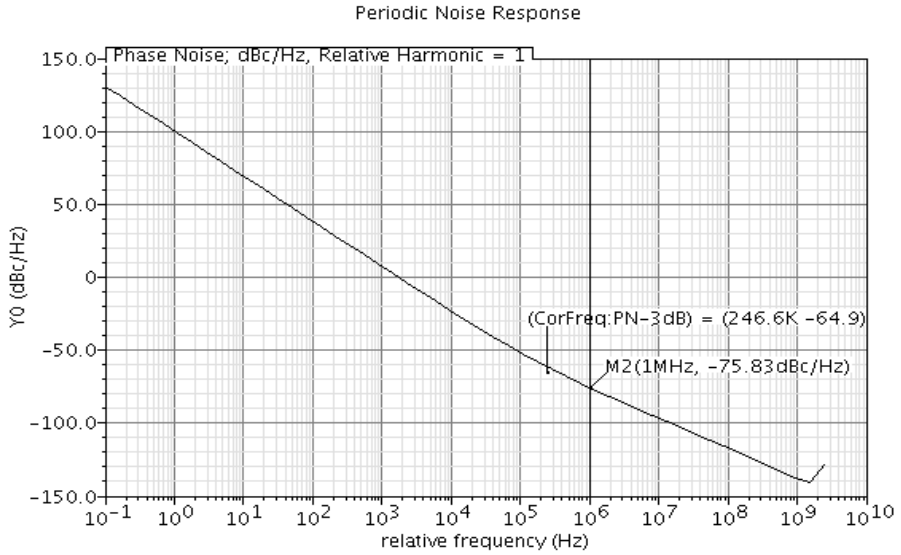

Figure 5. 15 Phase Noise plot of the Parasitic & Process Variation Aware DVCO

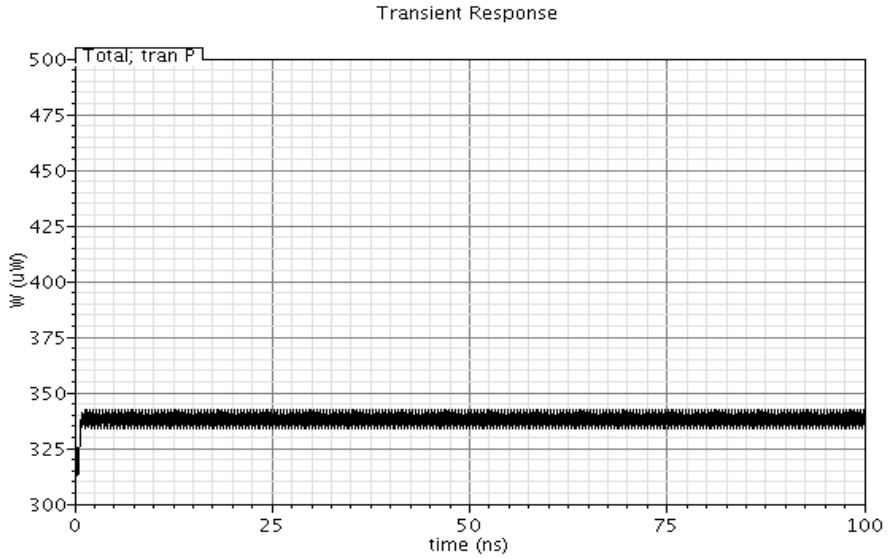

Figure 5. 16 Power Consumption of the Parasitic & Process Variation Aware DVCO

The plot of control voltage with oscillation frequency is depicted in Figure 5.17 from which the tuning range is found out to be 250 MHz i.e. 10.41 % of the center frequency.

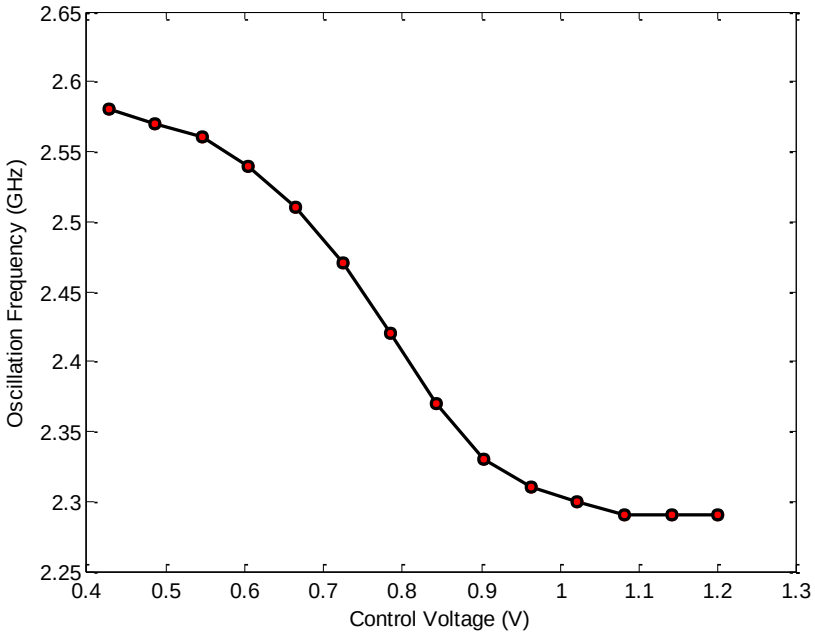

Figure 5. 17 Control Voltage versus Oscillation Frequency plot of the Parasitic & Process Variation Aware DVCO

The comprehensive summary of the design environment of DVCO is given in Table 5.9. The frequency of oscillation, phase noise and average power consumption estimated by IDEA, and observed from the physical level simulation in worst-case environment are enumerated in Table 5.10. Figure 5.18 depicts the process corner variations of frequency, power consumption and phase noise. The frequency for NN case is very close to the desired 2.4 GHz. The phase noise is almost immune to the corner variations.

Table 5. 9 Summary of the DVCO Design Environment

Serial No.	Parameter	The values used in this work
1	Technology	$90nm\ CMOS\ Salicide\ 1.2V/2.5V\ 1P\ 9M$
2	Supply Voltage (V_{DD})	$1.2\ V$
3	Process/Supply Variations	$V_{DD}(-10\%)$, $V_{Thn}(+10\%)$, $V_{Thp}(+10\%)$, $T_{oxn}(+10\%)$, $T_{oxp}(+10\%)$
4	The Design Variables	$4(Wn, Wp, Wntail, L)$
5	Number of Objectives	$3(f_{osc} >= 2.4\ GHz\ \&\ Minimize\ Phase\ Noise, Power)$

Table 5. 10 Performance Indices of Parasitic & Process Variation Inclusive Optimized Nano-CMOS Differential VCO

	Frequency of Oscillation (GHz)	Phase Noise (dBc/Hz at 1 MHz offset)	Power Consumption (µW)	FOM
IDEA Predicted	2.4	-77.838	380.469	-149.6398
Schematic Level	3.4363	-74.060	346.8435	-149.3984
Post-layout Level	2.5648	-75.830	338.697	-148.7396

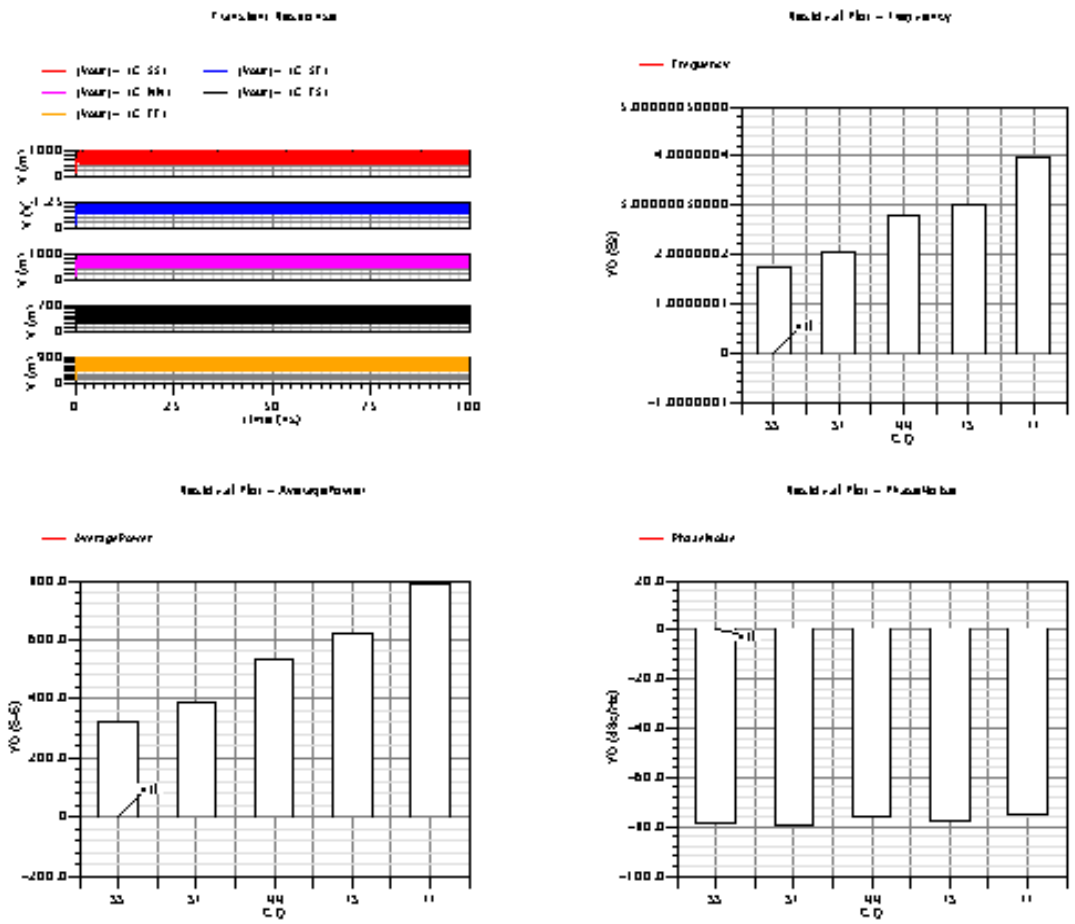

Figure 5. 18 Corner Analysis plots for oscillations, frequency, power consumption and phase noise

5.5 Conclusion

The integrated VCO circuits are designed for optimal performance by using an effective multi-objective evolutionary technique IDEA. In the first phase the parasitics are extracted from an optimized layout which is drawn using design parameters obtained from the first phase of optimization where parasitic aware model based objectives were inserted. The circuit and design objective models of the VCOs are adapted to be more realistic with the inclusion of the parasitics extracted from the first phase optimized layouts. Again the process variation parameters are also included in the circuit and objective models to make the methodology process variation aware so that it would provide design parameters for VCOs that would be robust against fabrication process variations. Thus the VCOs would be robust against both the circuit parasitics and variations in process parameters by carrying out parasitic and process variation aware design. These parasitic and process variation aware (PPVA) VCO circuit and objective models are then fed to the IDEA based design algorithm for second phase optimization of phase noise and power dissipation with a specified target frequency along with other process constraints. Then the final optimized parasitic and process variation aware VCO is designed using the parameters obtained from the second phase of optimization.

The proposed design methodology is validated with CMOS RO, CSVCO and DVCO circuits. In case of the RO the achieved post layout frequency of oscillation is 2.003079 GHz which is very much closer to the target frequency of 2 GHz along with the optimal phase noise and power dissipation. The performance parameters of the designed optimal CSVCO offers superior performance in comparison to other reported works. The difference in frequency from the worst case to nominal case observed from the post layout simulation of the CSVCO circuit is 299.18 MHz only, which shows the robustness of the design. A four stage differential VCO of 2.4 GHz oscillation frequency is designed for yielding low phase noise and minimum power consumption by using this IDEA based design methodology. The frequency of oscillation obtained in the parasitic and worst-case process variation environment deviates from the desired frequency by 0.319 % only. The difference in frequency

observed from the worst case to nominal case in physical layout level is 165.365342 MHz only, which again demonstrates the robustness of the design against process variations.

Design of Robust Analog Integrated Circuit based on Process Corner Performance Variability Minimization

6.1 Introduction

The fluctuations in the environmental operating conditions of the manufacturing process of integrated circuits are inevitable [97].The performance of nano scale integrated circuits (IC) is greatly affected due to these random fluctuations in different parameters of the semiconductor manufacturing process. In conventional process variation aware techniques the designers carry out a performance driven design and subject it to worst case process variations. In this method circuit tolerance to the variation in process are estimated using simulation analysis and the design is said to be process variation tolerant when the performances are found within an acceptable range. This worst-case modeling is highly unrealistic in many of the high performance integrated circuits whose performance acceptability range is very narrow. Moreover, if in a specified design, the worst-case performance does not fall in the acceptable range then the designer has no control over it even if the design offers good performance in nominal process. In such a case designer has to reject that design option. In [98] a technique that determines the worst-case process with an assigned probability value is presented. The impact of this unrealistic worst case modeling on the performance of VLSI circuits in submicron CMOS technologies is analyzed in [99].The realistic worst case SPICE file generation method is given in [100] where the BSIM3 models are considered. The worst case modeling is made more realistic by assigning probability to the process corners in deep submicron CMOS technology. The parametric manufacturability of the product is evaluated in [101]. The worst case analysis is carried out in terms of a set of statistically independent process distributions in [102]. A more practical approach to maximize the yield is to minimize the

performance variations due to process and environmental fluctuations. The worst case value of the circuit performance variability is minimized and specifications on the nominal value of the performance measures are handled simultaneously in [103] [104] [105] and [106]. In the worst case variability minimization technique the standard deviation of the performance is estimated from the Monte Carlo sampling of the noise parameters and the performance optimization is carried out by using gradient techniques like Simplex method and Quadratic Programming method. One novel practical approach of performance optimization of integrated circuits is proposed in this work. It is well known that the probability of having chip being manufactured under normal process environment is higher than the other corner process environments since it follows a Gaussian distribution. In our proposed approach we carry out process corner performance variability minimization (PCPVM) simultaneously along with performance optimization. In PCPVM the statistical performance deviations of the corner cases from the nominal case is minimized by considering the actual SPICE parameters of different process corners for evaluation of performances. The design proposed here is robust by optimizing the circuit performance in the nominal case and minimizing the difference between chip performances in normal and worst case corner environments. This approach is expected to improve the performance of the ICs manufactured even under extreme process corner conditions.

Simultaneous optimization methods have been developed [107] for process dependant fluctuation in different circuit performance parameters. In [107] fuzzy set theory is used to construct a single objective function for a weighted combination of different objectives and applied gradient based technique. The choice of weights for competing objectives makes the formulation of such an objective function somewhat ambiguous. In [106] it was single objective gradient-based optimization and in [107] though there is a mention regarding multiple objective optimizations but effectively the problem has been solved in a single objective gradient approach. Considering the spirit of [107] and our proposed formulation, a more appropriate way is to use the multi-objective multi-criteria optimization techniques. Besides this, the use of gradient-based optimization approach is inefficient in handling multimodal objective

functions for which evolutionary approaches are suitable. In this chapter a multi-objective evolutionary technique is used for the optimization of multiple statistically formulated performance process variability objective functions along with the nominal performance objectives simultaneously.

The remaining part of the chapter is organized as follows. In section 6.2 the proposed robust design methodology along with the formulation of the optimization objectives are presented. The performance analysis of the proposed design technique for demonstrative examples is carried out in section 6.3. Concluding remarks are provided in section 6.4.

6.2 Manufacturing Process Fluctuation Robust Design Methodology

A. Methodology Overview

The design methodology proposed here makes the integrated circuit robust due to (i) the optimization of the performance measures of IC under the nominal fabrication conditions and (ii) minimization of the random variability of extreme process performances from the nominal case. The above processes are carried out simultaneously using a multi-objective evolutionary technique. The outline of the proposed methodology is as follows.

1) The parasitic aware and fluctuation variability tolerant objective functions with specification constraints are formulated.

2) Circuit performance parameters of the nominal (NN) process are subjected to optimization using multi-objective evolutionary algorithm (MOEA), by integrating the SPICE model parameters of the process in the optimization engine.

3) The performance measures like frequency, phase noise and power of other process corners FF, SF, FS and SS, are computed using respective SPICE model parameters. Their statistical deviations from the NN process circuit model (obtained in step 2) constitute another set of optimization objectives, which are injected into the same MOEA in an iterative manner.

4) After the statistical deviations are minimized to meet the specified tolerance limits, the process variation robustified and parasitic aware optimized circuit design parameters are extracted for final design.

5) The final design parameters (obtained in step 4) are used for design and verification of the circuit performances in schematic and post layout level. Extensive simulations are carried out using ADE GXL and Assura tools from Cadence.

B. Objective Formulation

In the performance optimization, the objective functions are precisely the performance indices of the IC to be designed. In the present case studies on current starved voltage controlled oscillator and differential voltage controlled oscillator the performance measures are the phase noise, power consumption and the target frequency precision.

For convenience we can have a mathematical representation for NN, FF, FS, SF and SS as j=0, 1, 2, 3 and 4 respectively. In the nominal (NN) case of the VCO the performance objectives for optimization are

$$F_1 = \mathcal{L}\{\Delta f\} = PN(0) \tag{6.1}$$

$$F_2 = P = P(0) \tag{6.2}$$

$$F_3 = \left|\hat{f}_{osc}(0) - f_{osc}\right| \tag{6.3}$$

Where $PN(0)$ and $P(0)$ are the phase noise and power dissipation of the VCO in NN corner. The target frequency oscillation is represented by f_{osc} and $\hat{f}_{osc}(0)$ is the estimated frequency for the nominal case. The expressions for phase noise, power consumption and frequency of oscillation used here are as described in previous chapters.

The second part of optimization is for process corner performance variability minimization (PCPVM). The proposed work formulates the objectives in such a manner that the effective performance variation of corner cases from the nominal case is subjected to minimization. This concept is depicted in Figure 6.1 where the optimization engine is trained to orient the design such that the worst case corners are pushed towards the nominal case.

Since there are three performance measures for the VCO circuit under consideration, there would be three variability objectives. The phase noise variability is

$$F_4 = \left\{\sum_{j=1}^{4} |\widehat{PN}(0) - \widehat{PN}(j))|^2\right\}^{\frac{1}{2}} \quad (6.4)$$

Where, $\widehat{PN}(0)$ is the estimated phase noise for normal case and $\widehat{PN}(j)$ is the estimated phase noise for other cases based on the value of j. Similarly, the power consumption and frequency of oscillation variability objectives respectively can be formulated as

$$F_5 = \left\{\sum_{j=1}^{4} |\hat{P}(0) - \hat{P}(j))|^2\right\}^{\frac{1}{2}} \quad (6.5)$$

$$F_6 = \left\{\sum_{j=1}^{4} \left|\hat{f}_{osc}(j) - f_{osc}\right|^2\right\}^{\frac{1}{2}} \quad (6.6)$$

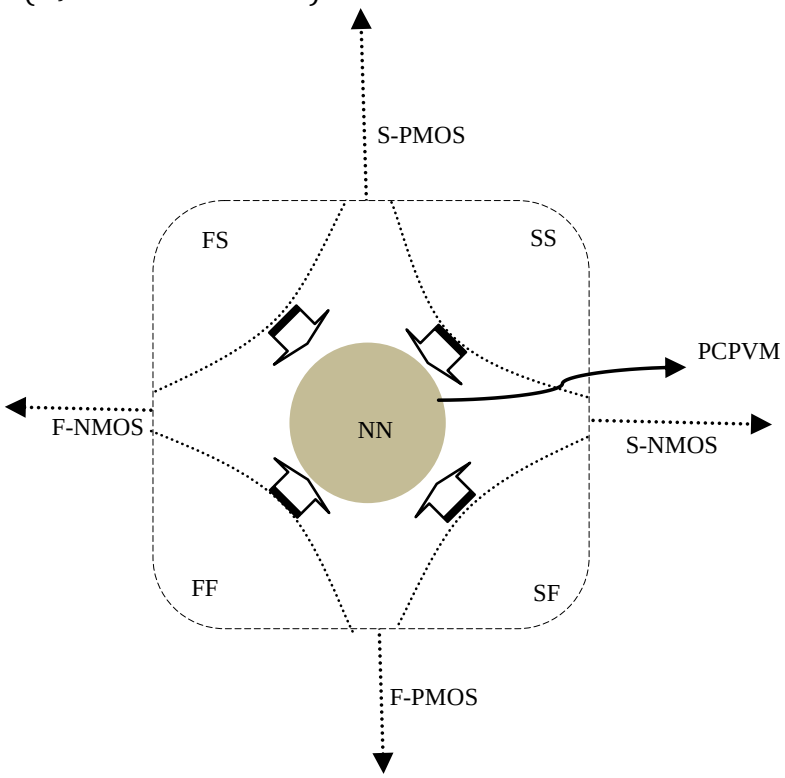

Figure 6. 1 Fabrication Process Corner Performance Variability Minimization (PCPVM) landscape

C. The Multiobjective Optimization

The optimization problem can be stated as

$$\begin{aligned} &Minimize\ F_k\ \ \forall k \in \{1,\dots,6\} \\ &Subject\ to \left.\begin{array}{l} f_{osc} = f_{Specification} \\ W_{min} < W < W_{max} \\ L_{min} < L < L_{max} \\ \left|g_{mn} - g_{mp}\right| \le \delta \end{array}\right\} \\ &\text{where } F_k = F_k\left(W, L, V_t, t_{ox}, V_{dd,} T\right) \end{aligned} \tag{6.7}$$

In the above expression W is the width of the transistor, L is the length, V_t is threshold voltage, $V_{dd,}$ supply voltage, t_{ox} oxide thickness and T is the absolute temperature and W_{min}, L_{min}, W_{max} and L_{max} are lower and upper bounds of width and length respectively, g_{mn} and g_{mp} stand for the NMOS and PMOS transconductances with δ as a very small positive value. In the above mentioned methodology many MOEAs have the scope for being used. However the most efficient and recently developed evolutionary algorithm, Infeasibility Driven Evolutionary Algorithm (IDEA), which has been extensively used in this thesis is deployed here for multi-objective optimization. A brief outline of IDEA based optimization for this formulation is as follows.

Infeasibility Driven Evolutionary Algorithm (IDEA) based Robust IC Design using PCPVM

Set: N {Population Size}
Set: $N_G > 1$ {Number of Generations}
Set: $0 < \alpha < 1$ {Proportion of infeasible solutions}
1: $N_{inf} = \alpha * N$
2: $N_f = N - N_{inf}$
3: $while\ Parameter\ Constraints\ C = [W_{min} < W < W_{max}, L_{min} < L < L_{max}]\ \ do$
4: pop1 = Initialize () *subject to C*
5: Evaluate $[F_k(pop_1), \forall k \in \{1,\dots,6\}]$
6: for $i = 2$ to N_G do
7: $childpop_{i-1}$ = Evolve (pop_{i-1})
8: Evaluate $[F_k(childpop_{i-1}), \forall k \in \{1,\dots,6\}]$
9: $Compute\ D = \left|f_{osc} - f_{target}\right|$

10: $if\ D \leq \epsilon\ then\ S_f$
else S_{inf}
$end\ if$
11: (S_f, S_{inf}) = Split $(pop_{i-1} + childpop_{i-1})$
12: Rank(S_f)
13: Rank(S_{inf})
14: $pop_i = S_{inf}(1 : N_{inf}) + S_f(1 : N_f)$
15: end for
16: *end while*

In the above pseudo code *Evolve* is the procedure of crossover, mutation and non-dominated sorting. S_f and S_{inf} represent the feasible and infeasible sets of solutions and N_f and N_{inf} are their modulus respectively which have been discussed in great detail in previous chapters.

6.3 Performance Analysis of the Proposed PCPVM based Robust Methodology

The proposed design methodology is validated through two circuit design examples viz. current starved VCO and differential VCO as described below.

6.3.1 Current Starved VCO

The robust PCPVM design methodology targets to optimize the performance objectives viz. phase noise and power consumption with desired frequency precision as described in previous chapters. The CSVCO design targets to achieve a frequency of 2 GHz. The five design parameters (Wn, Wp, Wncs, Wpcs, L) obtained from the proposed IDEA based parasitic inclusive robust methodology are used to design the CSVCO in the Cadence Virtuoso Analog Design Environment [69]. The design parameters of the robust CSVCO are listed in Table 6.1 and the corresponding physical layout is depicted in Figure 6.2. Design and simulation is carried out with 90 nm CMOS Salicide 1.2V/2.5V 1P 9M technology with a supply voltage of 1.2 V at room temperature using the BSIM model library [65].The post layout simulation results viz. oscillations, phase noise plot and power dissipation for the robust CSVCO for nominal process are depicted in Figures 6.3, 6.4 and 6.5 respectively.

The robust circuit is subjected to process corner variations and the frequency of oscillations, phase noise and power consumption performances are estimated at different process corners. Their values for a conventional (Parasitic and Process Variation Aware) optimized design and robust design are summarized in Table 6.2.

Table 6. 1 Design Parameters of Robust CSVCO

Design Parameter	Lower Limit	Upper Limit	Robust Value
Wn	120 nm	1 µm	300 nm
Wp	120 nm	2 µm	996.12 nm
Wncs	120 nm	5 µm	4.362 µm
Wpcs	120 nm	20 µm	5 µm
L	100 nm	110 nm	100 nm

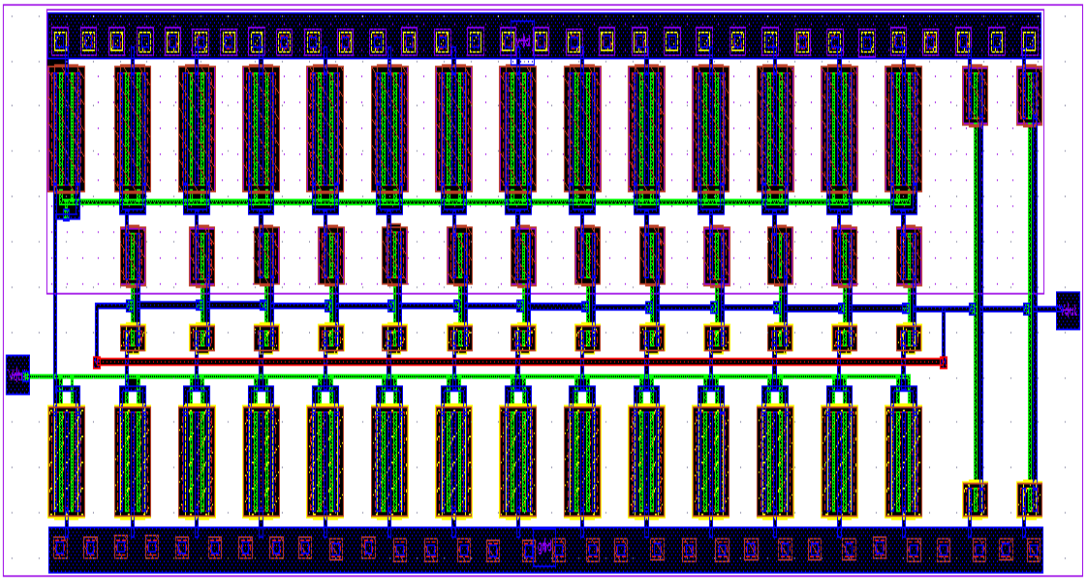

Figure 6. 2 Physical Layout of Robust CSVCO

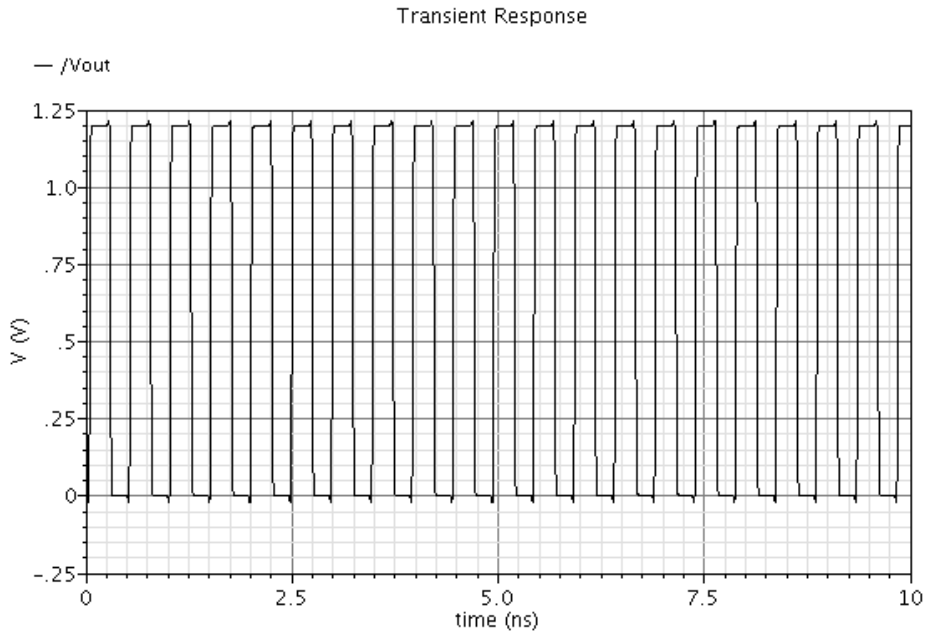

Figure 6. 3 Oscillations generated from the Robust CSVCO

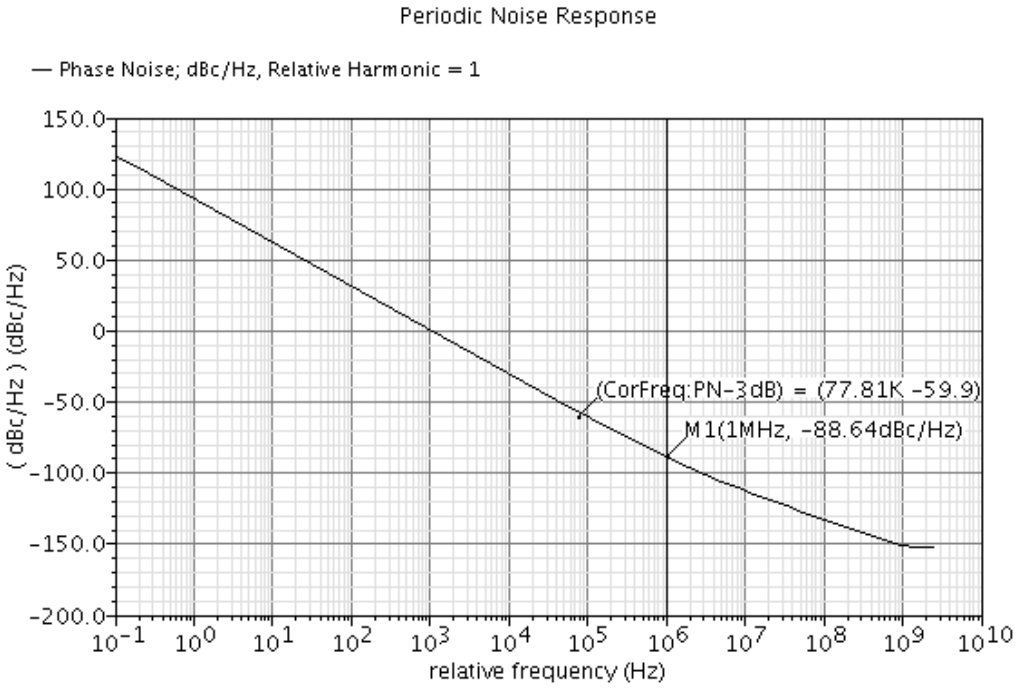

Figure 6. 4 Phase Noise plot of the Robust CSVCO

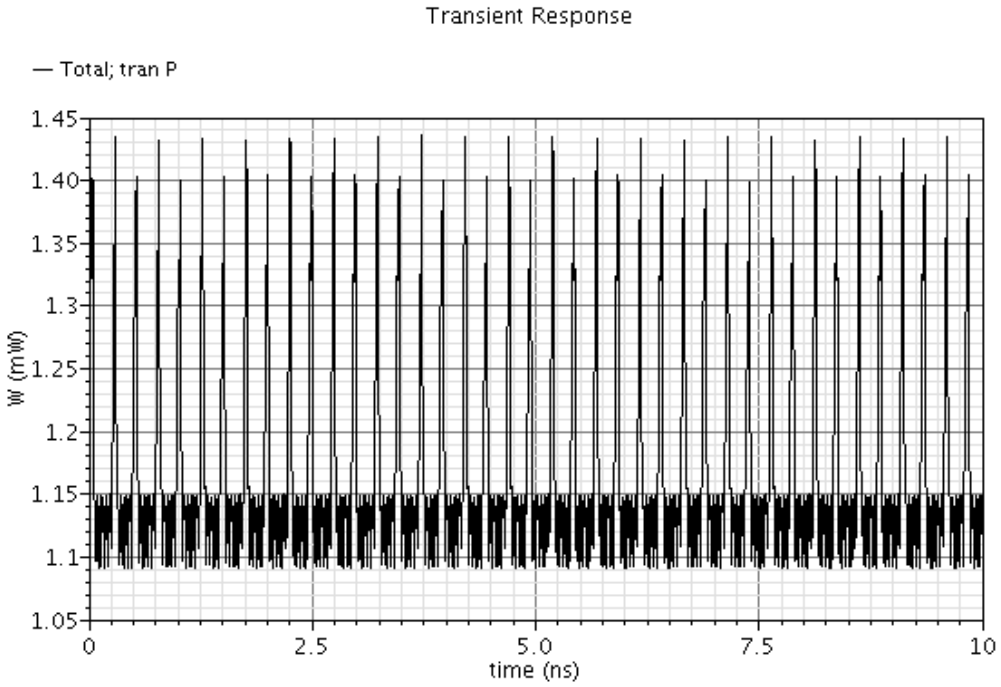

Figure 6. 5 Power Consumption of the Robust CSVCO

Table 6. 2 Performance Parameters of Optimized Robust Nano-CMOS CSVCO

Process Corners	Oscillation Frequency in GHz		Phase Noise in dBc/Hz at 1MHz offset		Average Power in mW	
	Conventional Design	Robust Design	Conventional Design	Robust Design	Conventional Design	Robust Design
NN	2.305	2.0405	-87.2	-88.64	1.589	1.1660
FF	3.15	2.596	-80.5	-86.39	2.226	1.875
FS	2.14	2.114	-81.0	-86.99	1.745	1.275
SF	2.11	1.997	-81.25	-88.7	0.8	0.7842
SS	1.4	1.972	-83.75	-90.01	0.575	0.7453

Figure 6.6 shows the comparative plot of the frequency of oscillations obtained using the proposed robust design and that using the conventional parasitic and process variation aware one. In each corner case the proposed robust design achieves frequency which is more close to the target frequency. In the FF case of the robust design there is more deviation from the target value which is very much expected. However in other corner cases the observed frequency shows a better trend of matching with the expected frequency. In the nominal case the frequency of oscillation is 2.0405 GHz which is very close to the target frequency 2 GHz which shows 13.225 % shift towards the target frequency in comparison to the conventional design.

Figure 6.7 depicts the comparative analysis of the phase noise of the CSVCO measured at 1MHz offset. The robust design offers better phase noise compared to the conventional one in all the corner cases. In the nominal case robust design shows 1% phase noise performance improvement. In all other cases, there is more than 7% improvement.

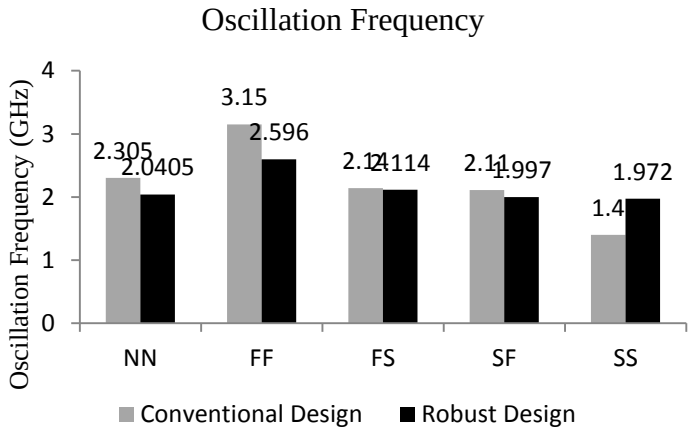

Figure 6. 6 Oscillation Frequency of CSVCO for Conventional and Robust Designs

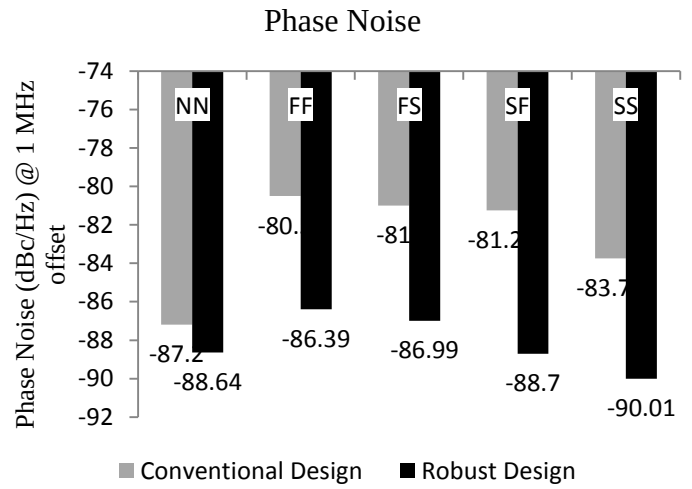

Figure 6. 7 Phase Noise of CSVCO for Conventional and Robust Designs

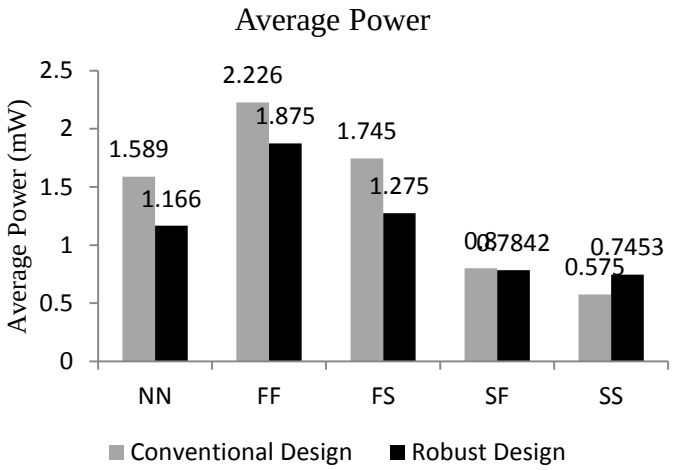

Figure 6. 8 Average Power Consumption of CSVCO for Conventional and Robust Designs

It is clear from the histogram shown in Figure 6.8 that in general the average power consumption of the robust CSVCO is less than the conventional one. The robust design achieves a 33 % power reduction as compared to the conventional case. In robust NN case there is a considerable power reduction compared to the reduction in other corner cases except SS case where there is a little increase in power. This little increase is due to the increase in frequency from 1.4 GHz in conventional case to 1.972 GHz in robust case. Hence, the effect of frequency on power consumption is pronounced which should be carefully considered for drawing any inference.

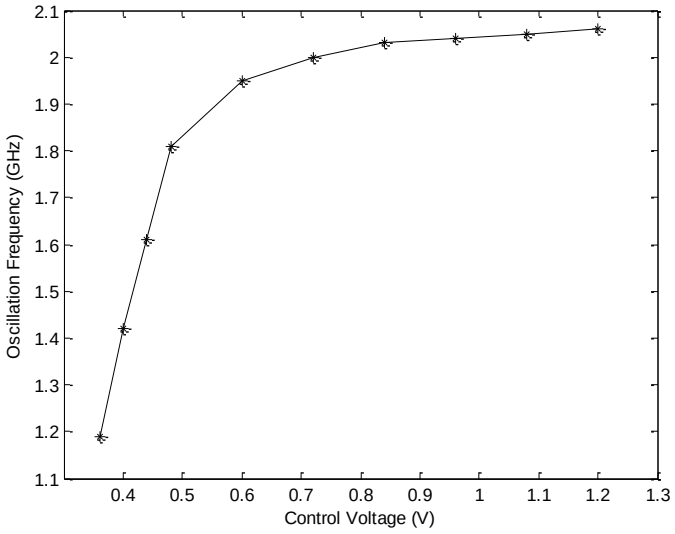

Figure 6. 9 Tuning Range plot of Robust CSVCO

Figure 6.9 depicts the tuning range plot of the robust CSVCO circuit. The estimated tuning range is about 600 MHz which is 30 % of the center frequency.

6.3.2 Differential VCO

Similarly design of a four-stage differential VCO targeted to produce frequency of oscillation 2.4 GHz is carried out using the parameters obtained from the proposed IDEA based PCPVM robust methodology. The design parameters $W_{p,}$ $W_{n,}$ W_{tail} and L estimated by IDEA based robust optimization methodology are depicted in Table 6.3. These parameters are used to realize the physical layout of four-stage differential VCO (shown in Figure 6.10) with CMOS Salicide 1.2V/2.5V 1P 9M 90 nm technology. Supply voltage of 1.2 V is used to perform simulation studies at room temperature. The post layout simulation results viz. oscillations, phase noise and power dissipation are depicted in Figures 6.11, 6.12 and 6.13 respectively of the robust differential VCO for nominal process.

Table 6. 3 Design Parameters of Optimized Robust Nano-CMOS DVCO

Design Parameter	Lower Limit	Upper Limit	Robust Value (Estimated by IDEA)
W_p	120 nm	2 µm	430 nm
W_n	120 nm	5 µm	4.965 µm
W_{tail}	120 nm	5 µm	1.44 µm
L	100 nm	110 nm	110 nm

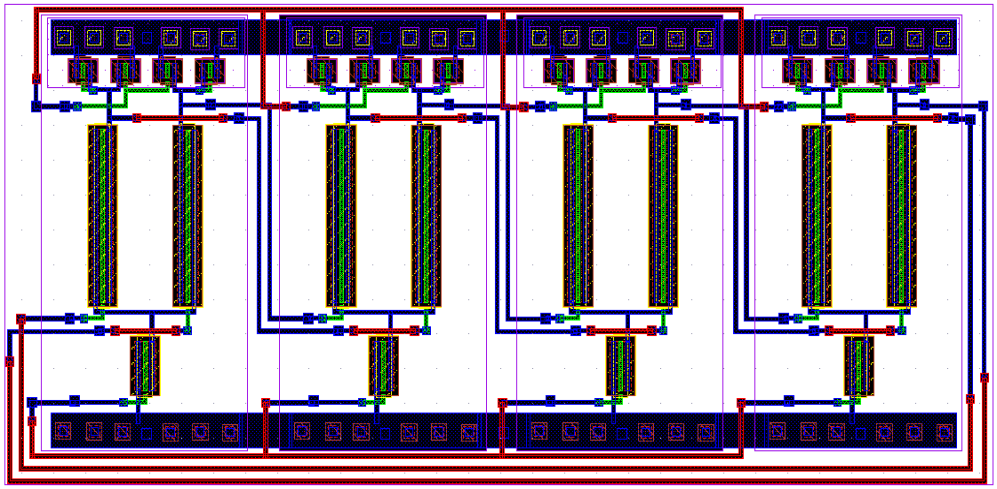

Figure 6. 10 Physical Layout of the Robust Optimal DVCO

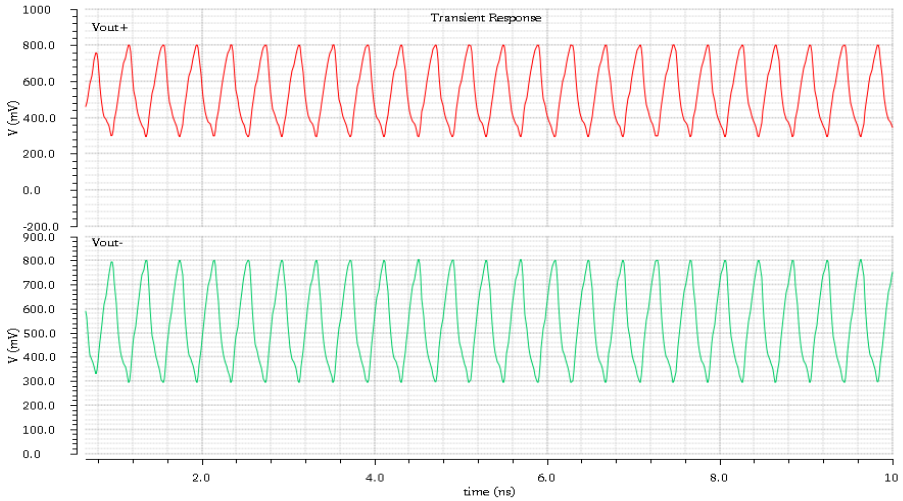

Figure 6. 11 Oscillations generated from the Robust DVCO

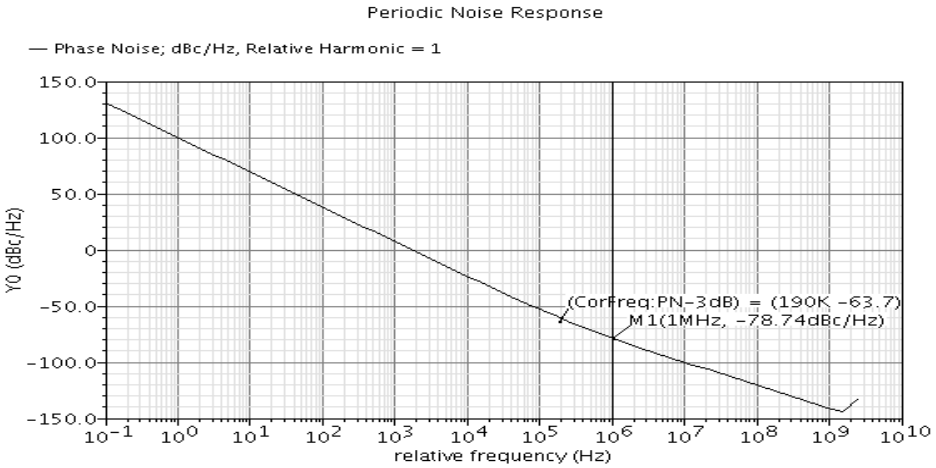

Figure 6. 12 Phase Noise plot of the Robust DVCO

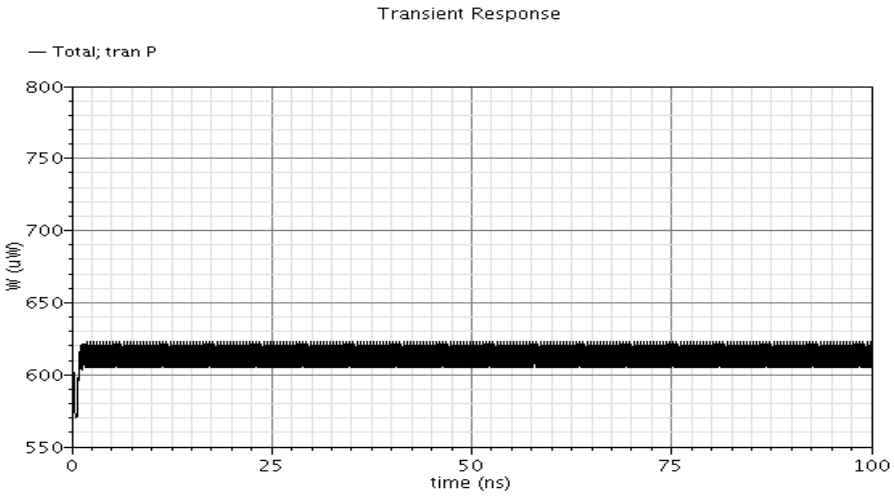

Figure 6. 13 Power Consumption of the Robust DVCO

Table 6. 4 Performance Parameters of Optimized Robust Nano-CMOS DVCO

Process Corners	Oscillation Frequency in GHz		Phase Noise in dBc/Hz at 1MHz offset		Average Power in mW	
	Conventional Design	Robust Design	Conventional Design	Robust Design	Conventional Design	Robust Design
NN	2.7910	2.4144	-76.54	-78.74	0.533	0.513
FF	3.9918	3.3643	-75.03	-77.29	0.790	0.757
FS	3.0290	2.6117	-77.95	-80.10	0. 623	0.616
SF	2.0402	2.1120	-79.89	-81.27	0. 384	0. 350
SS	1.7219	1.8313	-78.64	-80.63	0. 323	0.371

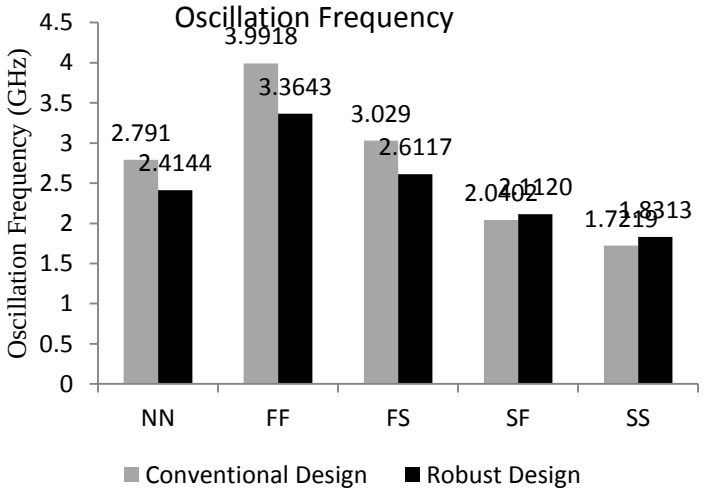

Figure 6. 14 Oscillation Frequency of DVCO for Conventional and Robust Designs

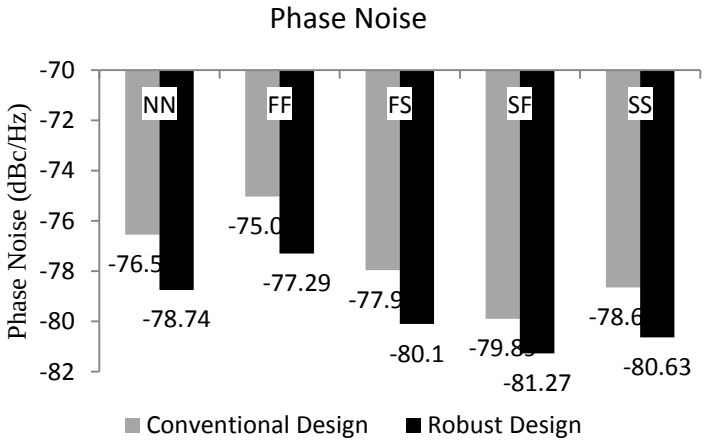

Figure 6. 15 Phase Noise of DVCO for Conventional and Robust Designs

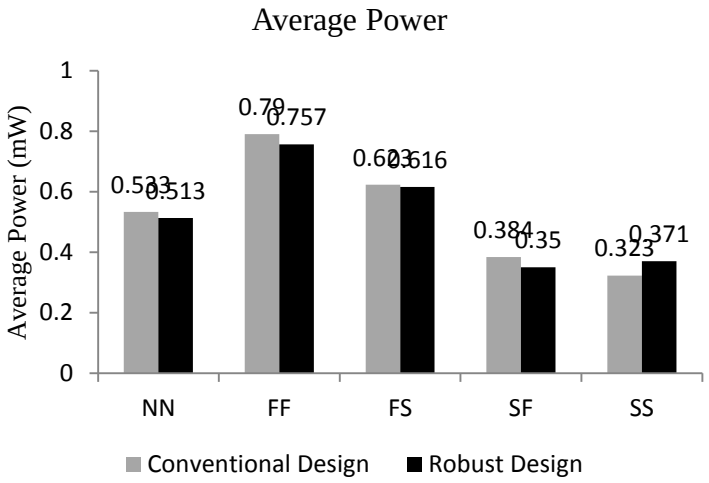

Figure 6. 16 Average Power Consumption of DVCO for Conventional and Robust Designs

Table 6.4 presents the detailed comparison of different performance indices for robust design and conventional design of the differential VCO.

The oscillation frequency comparison between the robust design and conventional design is shown in Figure 6.14. In each process corner the proposed robust design achieves frequency which is closer to the target frequency. In the FF case of the robust design there is more deviation from the target value which is very much expected. However, in other corner cases the observed frequency shows a better trend of matching with the expected frequency. In the nominal case of the robust design, the frequency of oscillation is 2.4144 GHz which is very close to the target frequency 2.4 GHz which shows a shift of 15.69 % towards the target frequency in comparison to the conventional design and validates the robustifying effect of the proposed methodology.

Figure 6.15 and 6.16 depicts the comparative analysis of the phase noise at 1MHz offset and power dissipation respectively for the robust and conventional designs of the DVCO. The robust design offers better phase noise in all the corners and less power dissipation in all the corners except SS (could be attributed to the higher frequency in robust design) case compared to the conventional one with better frequency precision.

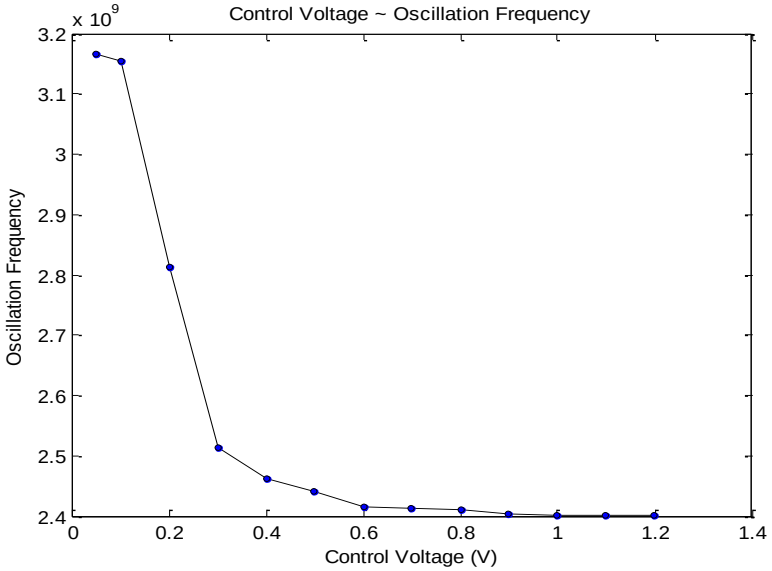

Figure 6. 17 Tuning Range plot of Robust DVCO

The control voltage versus oscillation frequency plot (Tuning Range plot) of the robust differential VCO is shown in Figure 6.17. The estimated tuning range is about 640 MHz i.e. 26.66 % of the center frequency.

6.4 Conclusion

This work proposes a novel design methodology for a robust analog integrated circuit which has been validated through design of current starved voltage controlled oscillator (CSVCO) and differential voltage controlled oscillator (DVCO) circuit. The robustification includes the nominal fabrication case performance optimization and process corner performance variability minimization (PCPVM). The technique optimizes the performance of the integrated circuit in nominal case and also guides the design in such a way that the other corner cases tend to behave closer to the nominal case. This method of design helps in maximizing the yield of integrated circuit. The method also reduces the statistical design complexity of conventional techniques. This methodology can seamlessly be used for any other RFIC and can further be extended to include other process corners and performance indices.

Conclusions and Scope for Future Research

7.1 General Conclusions

The research studies presented in this thesis, developed a novel constrained non-dominated sorting genetic algorithm II based parasitic aware analog IC design methodology and also infeasibility driven evolutionary algorithm based fast and robust IC design technique for achieving optimal performance. The techniques have been successfully applied to different CMOS voltage controlled oscillators for minimization of power consumption and phase noise with an objective to achieve a desired frequency of oscillation. The design is carried out within the geometrical and fabrication process constraints. The IDEA based design is subjected to manufacturing process fluctuations and the worst case performance analysis is demonstrated and compared with different reported results. A new design technique considering the manufacturing process corner variations, yet achieving the optimal performance is reported in this work.

The investigations conducted in this research work yield the following important conclusions.

1. The multi-objective evolutionary computing based optimization techniques like NSGA-II and IDEA have been successfully applied to CMOS VCO design. In this approach, the circuit parasitics which includes the device and interconnect parasitcs are implicitly integrated in the design phase. The use of multi-objective constrained optimization effectively handles the design complexity with very high precision and in a very less design time. This saves the valuable designers' time in industry simultaneously offering the possible best performance.

2. The IDEA based technique is observed to perform superior to the NSGA-II based technique due to its better constraint handling and infeasibility driven search capability.
3. The IDEA based design is robustified during each iteration to meet the required specification with better performance than other techniques reported earlier. The worst-case analysis reveals this enhanced performance of the ICs as demonstrated in all cases of CMOS VCOs.
4. The process corner performance variability minimization (PCPVM) design technique increases the number of VCO ICs with acceptable performance along with their superior individual performance in terms of power consumption, phase noise and frequency of oscillations.
5. The proposed techniques can be seamlessly applied to any analog / mixed signal integrated circuit or radio frequency integrated circuits because of their capability of providing very precise desired behavior.

7.2 Scope for Future Research

It is a fact that much work still remains to be carried out in the analog IC design automation domain. This thesis has been devoted to performing the design optimization of analog ICs with realistic constraints. The proposed research can be extended in the following dimensions.

1. The approach proposed in the thesis can be more extensively validated by taking many other standard analog building blocks.
2. Recently reported computationally intelligent techniques can also be applied to achieve efficient analog IC optimization.
3. The additional performance objectives such as area, yield can also be considered in the proposed design.
4. In nano-scale regime, the ICs are very much sensitive to the temperature fluctuations. The design techniques for making the integrated circuits temperature variation tolerant is another important domain of future research work.

5. The design optimization may be taken up along with the development of metamodels for individual analog blocks so as to mimic the performances with higher precision.

References

[1] J. Nelder and R. Mead, "A simplex method for function optimization," *Computer Journal,* vol. 7, no. 4, p. 308–313, 1965.

[2] S. Haykin, Neural Networks A Comprehensive Foundation, Prentice Hall International Inc., 1998.

[3] S. Kirkpatrick, C. Gelatt and M. Vecchi, "Optimization by simulated annealing," *Journal of Science,* vol. 220, pp. 671-680, 1983.

[4] R.A. Rutenbar, "Simulated annealing algorithms: An overview," *IEEE Circuits and Devices Magazine,* pp. 19-26, 1989.

[5] D. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Reading, MA: Addison-Wesley, 1989.

[6] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. IEEE international conference on neural networks*, 1995.

[7] Kenneth Price, Rainer M. Storn and Jouni A. Lampinen, "Differential Evolution: A Practical Approach to Global Optimization," in *Natural Computing Series*, Springer, 2005.

[8] D. Karaboga, "An idea based on Honey Bee Swarm for numerical optimization," Dept. of Computer Engineering, Engineering Faculty, Erciyes University, 2005.

[9] K. M. Passino, "Biomimicry of Bacterial Foraging for distributed optimization and control," *IEEE Control Syst. Magazine,* vol. 22, no. 3, pp. 52-67, 2002.

[10] N. S. Nagaraj, "A new optimizer for performance optimization of analog integrated circuits," in *IEEE/ACM Design Automation Conference (DAC)*, Dallas, Texas, 1993.

[11] H.Y. Koh, C.H. Sequin and P.R. Gray, "OPASYN: A Compiler for CMOS Operational Amplifiers," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 9, no. 2, pp. 113-125, 1990.

[12] H. Onodera, H. Kanbara, K. Tamaru, "Operational-amplifier compilation with performance optimization," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 466-473, 1990.

[13] J. P. Harvey, M. I. Elmasry and B. Leung, "STAIC: An Interactive Framework for Synthesizing CMOS and BiCMOS Analog Circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 11, no. 11, 1992.

[14] W. Nye, D.C. Riley, A. Sangiovanni-Vincentelli and A.L. Tits, "DELIGHT.SPICE: an optimization-based system for the design of integrated circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 7, no. 4, pp. 501-519, 1988.

[15] A.R. Conn, P.K. Coulman, R.A. Haring, G.L. Morrill, C. Visweswariah and C.W. Wu, "JiffyTune: circuit optimization using time-domain sensitivities," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,*

vol. 17, no. 12, p. 1292–1309, 1995.

[16] O. Altun and M. Bocko, "Robust analog circuit design: a set theoretic approach," in *IEEE International Symposium on Circuits and Systems*, 2006.

[17] G.V. Plas, G. Debyser, Francky Leyn, K. Lampaert, J. Vandenbussche, G. G. E. Gielen, W. Sansen, P. Veselinovic, and D. Leenaerts, "AMGIE- A Synthesis Environment for CMOS Analog Integrated Circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 20, no. 9, pp. 1037-1058, 2011.

[18] F. El-Turky and E. Perry, "BLADES: an artificial intelligence approach to analog circuit design," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 8, no. 6, p. 680–692, 1989.

[19] K. Matsukawa, T. Morie, Y. Tokunaga, S. Sakiyama, Y. Mitani, M. Takayama, T. Miki, A. Matsumoto, K. Obata and S. Dosho, "Design methods for pipeline & delta-sigma A-to-D converters with convex optimization," in *Asia and South Pacific Design Automation Conference*, 2009.

[20] X. Li, Y. Xu, K.L. Hsiung, L. Pileggi and S. Boyd, "Regular Analog/RF Integrated Circuits Design Using Optimization With Recourse Including Ellipsoidal Uncertainty," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 28, no. 9, p. 623–637, 2009.

[21] J. Kim, R. Jhaveri, J. Woo and C. Yang, "Device-Circuit Co-Optimization for Mixed-mode Circuit Design via Geometric Programming," in *IEEE/ACM International Conference on Computer-Aided Design*, 2007.

[22] T. Soorapanth, "Gaining Insights in Analog Design via Geometric Programming," in *IEEE International Symposium on Information and Communication Technologies*, 2007.

[23] "GPGLP Library : ftp//ftp.pitt.edu/dept/ie/GP".

[24] F. Yang and M. Gan, "Robust Calibration of an Improved Delta-Sigma Data Converter Using Convex Optimization," *IEEE Journal of Selected Topics in Signal Processing,* vol. 1, no. 4, p. IEEE Journal of Selected Topics in Signal Processing, 2007.

[25] M. Hershenson, S.Boyd and T.Lee, "GPCAD: a tool for CMOS opamp synthesis," in *Proc. of IEEE/ACM International Conference on CAD (ICCAD)*, 1998.

[26] P. Mandal and V. Visvanathan, "CMOS Op-Amp Sizing Using a Geometric Programming Formulation," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 20, no. 1, pp. 22-38, 2001.

[27] S. Kundu and P. Mandal, "ISGP: Iterative Sequential Geometric Programming for Precise and Robust Analog Circuit Sizing," *Integration, the VLSI Journal,* vol. 47, pp. 510-531, 2014.

[28] E. Hjalmarson, R. Hagglund and L. Wanhammar, "An equation-based optimization approach for analog circuit design," in *International Symposium on Signals, Circuits and Systems*, 2003.

[29] M. Eick and H. Graeb, "MARS: Matching-Driven Analog Sizing," *IEEE*

Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, no. 8, pp. 1145-1158, 2012.

[30] C.R.C. De Ranter, G. Van der Plas, M.S.J. Steyaert, G.G.E. Gielen and W.M.C. Sansen, "CYCLONE: automated design and layout of RF LC-oscillators," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 21, no. 10, p. 1161–1170, 2002.

[31] J. Ruiz-Amaya, J. de la Rosa, F.V. Fernandez, F. Medeiro, R. del Rio, B. Perez-Verdu, and A. Rodriguez-Vazquez, "High-level synthesis of switched-capacitor switched-current and continuous-time SD modulators using SIMULINK-based time-domain behavioral models," *IEEE Trans. on Circuits and Systems-I: Regular Paper,* vol. 52, no. 9, p. 1795–1810, 2005.

[32] J. Crols, S. Donnay, M. Steyaert and G. Gielen, "A high-level design and optimization tool for analog RF receiver front-ends," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* San Jose, California, USA, 1995.

[33] A. Torralba, J. Chavez, L.G. Franquelo, "FASY: a fuzzy-logic based tool for analog synthesis," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems,* vol. 15, no. 7, p. 705–715, 1996.

[34] G. Tulunay and S. Balkir, , "A synthesis tool for CMOS RF low noise amplifiers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 27, no. 5, pp. 977-982, 2008.

[35] W. Kruiskamp and D. Leenaerts, "DARWIN: CMOS opamp synthesis by means of a genetic algorithm," in *Proc. ACM/IEEE Design Automation Conference (DAC),* 1995.

[36] G. Gielen and R. A. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," in *Proceedings of the IEEE*, 2000.

[37] N. Paulino, J. Goes, A. Steiger-Garcao, "Design methodology for optimization of analog building blocks using genetic algorithms," in *The 2001 IEEE International Symposium on Circuits and Systems (ISCAS 2001),* 2001.

[38] M. Barros, J. Guilherme and N. Horta, "Analog circuits optimization based on evolutionary computation techniques," *Integration, the VLSI journal,* vol. 43, pp. 136-155, 2010.

[39] D. Ghai, S. Mohanty, G. Thakral, "Fast optimization of nano-CMOS voltage-controlled oscillator using polynomial regression and genetic algorithm," *Microelectronics Journal,* vol. 44, p. 631–641, 2013.

[40] S. Pandit, C. Mandal and A. Patra, "A Methodology for Generation of Performance Models for the Sizing of Analog High-Level Topologies," *Int. Journal VLSI Design, Hindwai Pub,* 2011.

[41] P. Tawdross and A. Koning, "Investigation of Particle Swarm Optimization for dynamic reconfiguration of field programmable analog circuits," in *Proc. of 5th Conference on hybrid intelligent systems,* 2005.

[42] P. Tawdross, and A. König, "Particle swarm optimization for reconfigurable sensor electronics-case study: 3 Bit Flash ADC," in *4th IEEE international*

workshop on intelligent solutions in embedded systems (WISES'06), 2006.

[43] Y. Cooren, M. Fakhfakh, M. Loulou and P. Siarry, "Optimizing second generation current conveyors using particle swarm optimization," in *The IEEE 19th international conference on microelectronics*, 2007.

[44] R. A. Thakker, M. S. Baghini and M. B. Patil, "Low-power low-voltage analog circuit design using hierarchical particle swarm optimization," in *Proc. IEEE 22nd international conference on VLSI design*, 2009.

[45] M. Fakhfakh, Y. Cooren, A. Sallem, M. Loulou and P. Siarry, "Analog circuit design optimization through the particle swarm optimization technique," *Analog Integrated Circuits and Signal Processing*, vol. 63, pp. 71-82, 2010.

[46] R. Vural and T. Yildirim, "Analog Circuit Sizing via Swarm Intelligence," *Int. J. Electron. Commun. (AEÜ)*, vol. 66, no. 9, p. 732–740, 2012.

[47] M. Barari, H. R. Karimi and F. Razaghian, "Analog Circuit Design Optimization Based on Evolutionary Algorithms," *Mathematical Problems in Engineering, Hindawi*, 2014.

[48] B. Liu, Y. Wang, Z. Yu, L. Liu, M. Li, Z. Wan, J. Lu and F. Fernandez, "Analog circuit optimization system based on hybrid evolutionary algorithms," *Integration, the VLSI journal*, vol. 42, p. 137–143, 2009.

[49] A. F. Sheta, "Analogue filter design using differential evolution," *Int. J. Bio-Inspired Computation*, vol. 2, no. 3-4, p. 233–241, 2010.

[50] O. Garitselov, S. Mohanty, E. Kougianos and Priyadarsan Patra, "Bee Colony Inspired Metamodeling Based Fast Optimization of a Nano-CMOS PLL," in *2011 International Symposium on Electronic System Design (ISED)*, 2011.

[51] A. Jafari, E. Bijami, H. Bana and S. Sadri, "A design automation system for CMOS analog integrated circuits using New Hybrid Shuffled Frog Leaping algorithm," *Microelectronics Journal*, vol. 43, no. 11, p. 908–915, 2011.

[52] O. Sonmez and G. Dundar, "Simulation-based analog and RF circuit synthesis using a modified evolutionary strategies algorithm," *Integration, the VLSI Journal*, vol. 44, no. 2, p. 144–154, 2011.

[53] R. Vural, T. Yildirim, T. Kadioglu and A. Basargan, "Performance evaluation of evolutionary algorithms for optimal filter design," *IEEE Transactions on Evolutionary Computation*, vol. 16, no. 1, pp. 135-147, 2012.

[54] K.Ghali, L. Dorie, O. Hammami, "Dynamically Reconfigurable Analog Circuit Design Automation Through Multiobjective Optimization and Direct Execution," in *the 17th International Conference on Microelectronics*, 2005.

[55] R. Phelps, M. Krasnicki, R. Rutenbar, L. R. Carley and J. R. Hellums, "ANACONDA: simulation-based synthesis of analog circuits via stochastic pattern search," *IEEE Trans.on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 6, pp. 703-717, 2000.

[56] O. Okobiah, S. Mohanty and E. Kougianos, "Geostatistical-inspired fast layout optimisation of a nano-CMOS thermal sensor," *Circuits, Devices & Systems, IET*, vol. 7, no. 5, pp. 253-262, 2013.

[57] R. Vural, U. Bozkurt and T. Yildirim, "Analog active filter component selection with nature inspired metaheuristics," *Int. J. Electron. Commun. (AEÜ)*, vol. 67, p. 197– 205, 2013.

[58] I. Gomez, E. Cuautle and Luis G. Fraga, "Richardson extrapolation-based sensitivity analysis in the multi-objective optimization of analog circuits," *Applied Mathematics and Computation*, vol. 222, p. 167–176, 2013.

[59] R.Gupta and D.J.Allstot, "Parasitic-Aware Design and Optimization of CMOS RF Integrated Circuits," in *IEEE Radio Frequency Integrated Circuits Symposium*, 1998.

[60] Brian M. Ballweber, Ravi Gupta, and David J. Allstot, "A Fully Integrated 0.5-5.5-GHz CMOS Distributed Amplifier," *IEEE Transactions on Solid-State Circuits*, vol. 35, no. 2, pp. 231-239, 2000.

[61] D.J.Allstot, K.Choi and J.Park, Parasitic-Aware Optimization of CMOS RF Circuits, Kluwer Academic Publishers, 2003.

[62] M. Chu, D. Allstot, J. Huard and K. Wong, "NSGA-Based Parasitic-aware Optimization of a 5 GHz Low-noise VCO," in *Design Automation Conference, Asia and South Pacific*, 2004.

[63] J. Kennedy, R. C. Eberhart, and Y. Shi, Swarm Intelligence, San Francisco, CA: Morgan Kaufmann, 2001.

[64] N. V. George and G. Panda, "A Particle Swarm Optimization based Decentralized Nonlinear Active Noise Control System," *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 12, pp. 3378-3386, 2012.

[65] www-device.eecs.berkeley.edu/bsim/.

[66] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A Fast Elitist Multi-Objective Genetic Algorithm: NSGA-II," *IEEE Transactions on Evolutionary Computation*, vol. 6, no. 2, pp. 182-197, 2002.

[67] K. Deb, Multi-objective Optimization using Evolutionary Algorithms, New York: 1st Edition, Wiley, 2001.

[68] G.Nicosia, S. Rinaudo and E. Sciacca, "An Evolutionary algorithm-based approach to robust analog circuit design using constrained multi-objective optimization," *Knowledge Based Systems*, vol. 21, p. 175–183, 2008.

[69] www.cadence.com.

[70] S. Docking and M. Sachdev, "An Analytical Equation for the Oscillation Frequency of High-Frequency Ring Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 533-537, 2004.

[71] M. Alioto and G. Palumbo, "Oscillation Frequency in CML and ESCL Ring Oscillators," *IEEE Trans on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 48, no. 2, pp. 210-214, 2001.

[72] N. H. E. Weste and K. Eshraghian, PRINCIPLES OF CMOS VLSI DESIGN: A Systems Perspective, 2nd ed., Addison-Wesley, 2002.

[73] R.J.Baker, H. W. Li, and D. E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, 2002.

[74] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and Phase Noise in Ring Oscillators," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 6, pp. 790-804, 1999.

[75] A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 8, pp. 1803-1816, 2006.

[76] A. A. Abidi , "High-frequency noise measurements on FET's with small dimensions," *IEEE Trans.on Electron Devices,* vol. 33, no. 11, pp. 1801-1805, 1986.

[77] X. Gao, Eric A.M Klumperink, Paul F .J. Geraedts and Bram Nauta, "Jitter Analysis and Benchmarking Figure-of-Merit for Phase-Locked Loops," *IEEE Trans on Circuits and Systems-II: Express Briefs,* vol. 56, no. 2, pp. 117-121, 2009.

[78] H. J. M. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits," *IEEE Journal of Solid-State Circuits,* Vols. Sc-19, no. 4, pp. 468-473, 1984.

[79] S. R. Vemuru and N. Scheinberg, "Short-circuit power dissipation estimation for CMOS logic gates," *IEEE Trans. on Circuits and Systems-I: Fundamental Theory and Applications,* vol. 41, no. 11, pp. 762-765, 1994.

[80] K. Roy and S. C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley & Sons, Inc., 2000.

[81] J.G.Meneatis and M.A.Horowitz, "Precise Delay Generation using Coupled Oscillators," *IEEE Journal of Solid-State Circuits,* vol. 28, no. 12, pp. 1273-1282, 1993.

[82] J.G. Meneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE Journal of Solid-State Circuits,* vol. 31, no. 11, pp. 1723-1732, 1996.

[83] L. Dai and R. Harjani, "Design of Low Phase Noise CMOS Ring Oscillators," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing,* vol. 49, no. 5, pp. 328-338, 2002.

[84] L. Bisdounis, S. Nikolaidis, and O. Koufopavlou, "Propagation Delay and Short-Circuit Power Dissipation Modeling of the CMOS Inverter," *IEEE Trans. on Circuits and Systems-I: Fundamental Theory and Applications,* vol. 45, no. 3, pp. 210-214, 1998.

[85] J. Chang, A. A. Abidi and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures," *IEEE Transactions on Electron Devices,* vol. 41, no. 11, pp. 1965-1971, 1994.

[86] M. Grozing and M. Berroth, "Derivation of single-ended CMOS inverter ring oscillator close-in phase noise from basic circuit and device properties," in *Radio Frequency Integrated Circuits(RFIC) Symposium*, 2004.

[87] T. Ray, H. K. Singh, A. Isaacs, and W. Smith, "Infeasibility Driven Evolutionary Algorithm for Constrained Optimization, Constraint-Handling in Evolutionary Optimization," in *Studies in Computational Intelligence Series 198*, Eds, Efrén Mezura-Montes, Springer, 2009, pp. 145-165.

[88] H. K. Singh, A. Isaacs, T. T. Nguyen, T. Ray, and Yao Xin, "Performance of infeasibility driven evolutionary algorithm (IDEA) on constrained dynamic single objective optimization problems," in *Proc. IEEE Congress on Evolutionary Computation(CEC)*, 2009.

[89] A. Saha, T. Ray, and W. Smith, "Towards practical evolutionary robust multi-objective optimization," in *Proc. IEEE Congress on Evolutionary Computation (CEC)*, 2011.

[90] K. Deb and S. Agrawal, "Simulated binary crossover for continuous search space," *Complex Systems*, vol. 9, p. 115–148, 1995.

[91] K. Deb, and M. Goyal, "A combined genetic adaptive search (GeneAS) for engineering design," *Computer Science and Informatics*, vol. 26, p. 30–45, 1996.

[92] D.Ghai, S.P.Mohanty, and E.Kougianos, "Design of Parasitic and Process-Variation Aware Nano-CMOS RF Circuits: A VCO Case Study," *IEEE Trans on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 9, pp. 1339-1342, 2009.

[93] S. M. Sze, VLSI Technology, 2nd Edition, Tata McGraw-Hill, 2003.

[94] J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits A Design Perspective, Singapore: 2nd Edition, Pearson Education Pte. Ltd, 2005.

[95] D. Ghai, S. P. Mohanty, and G. Thakral, "Fast Optimization of Nano-CMOS Voltage-C ontrolled Oscillator using Polynomial Regression and Genetic Algorithm," *Microelectronics Journal*, vol. 44, no. 8, pp. 631-641, 2013.

[96] D. Ghai, S. P. Mohanty, and G. Thakral, "Fast Analog Design Optimization using Regression based Modeling and Genetic Algorithm: A Nano-CMOS VCO Case Study," in *Proc. of the 14th International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, C A, USA, 2013.

[97] S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits Analysis and Design, New Delhi: Tata McGraw-Hill Publishing Company Limited, 2003.

[98] A. Dal Fabbro, B. Franzini, C. Guardiani, "An assigned probability technique to derive realistic worst case timing models of digital standard cells," in *32nd ACM/IEEE Design Automation Conference*, 1995.

[99] Nardi, A. Neviani, E. Zanoni, M. Quarantelli, and C. Guardani, "Impact of unrealistic worst case modeling on the performance of VLSI circuits on deep submicron CMOS technologies," *IEEE Trans. on Semiconductor Manufacturing*, vol. 12, no. 4, pp. 396-402, 1999.

[100] J. C. Chen, C. Hu, Z. Liu and P. K. Ko, "Realistic Worst-Case Spice File Extraction Using BSIM3," in *Proc. IEEE Custom Integrated Circuits Conference*, 1995.

[101] M. Bolt, M. Rocchi and J. Engel, "Realistic Statistical Worst-Case Simulations of VLSI Circuits," *IEEE Transactions on Semiconductor Manufacturing*, vol. 4, no. 3, pp. 193-198, 1991.

[102] S. R. Nassif, A. J. Strojwas and S. W. Director, "A Methodology for Worst-Case Analysis of Integrated Circuits," *IEEE Transactions on Computer-Aided*

Design of Integrated Circuits and Systems, vol. 5, no. 1, pp. 104-113, 1986.

[103] A. Dharchoudhury and S. M. Kang, "An integrated approach to realistic worst-case design optimization of MOS analog circuits," in *Proc. 29th ACM/IEEE Design Automation Conference*, 1992.

[104] M. A. Styblinski and J. C. Zhang, "Circuit performance variability reduction: Principles, problems and practical solutions," in *Proc. IEEE ICCAD*, Santa Clara, CA, 1991.

[105] A. Dharchoudhury and S. M. Kang, "Performance-Constrained Worst-Case Variability Minimization of VLSI Circuits," in *Proc. 30th ACM/IEEE Design Automation Conference*, 1993.

[106] A. Dharchoudhury and S. M. Kang, "Worst-Case Analysis and Optimization of VLSI Circuit Performances," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, no. 4, pp. 481-492, 1995.

[107] Ayhan A. Mutlu, Charles Kwong, Abir Mukherjee, and Mahmud Rahman, "Statistical Circuit Performance Variability Minimization under Manufacturing Variations," in *Proceedings of ISCAS*, 2006.