DESIGN AND ANALYSIS OF IMPROVED DOMINO LOGIC WITH NOISE TOLERANCE AND HIGH PERFORMANCE

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DESIGN AND ANALYSIS OF IMPROVED DOMINO LOGIC WITH NOISE TOLERANCE AND HIGH PERFORMANCE

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CERTIFICATE

This is to certify that the thesis entitled "**DESIGN AND ANALYSIS OF IMPROVED DOMINO LOGIC WITH NOISE TOLERANCE AND HIGH PERFORMANCE**" submitted to National Institute of Technology, Rourkela by **Mrs. Preetisudha Meher**, bearing Roll No. **509EC102** for the award of the degree of **DOCTOR OF PHILOSOPHY** in Electronics and Communication Engineering is a bonafide record of research work carried out by her under my supervision and guidance.

This candidate has fulfilled all the prescribed requirements.

This thesis is based on candidate's own work, has not submitted elsewhere for the award of degree/diploma.

In my opinion, the thesis is in standard fulfilling all the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY** in Electronics and Communication Engineering.

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Dedicated To

My Family

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ABSTRACT

The demands of upcoming computing, as well as the challenges of nanometer-era of VLSI design necessitate new digital logic techniques and styles that are at the same time high performance, energy efficient and robust to noise and variation. Dynamic CMOS logic gates are broadly used to design high performance circuits due to their high speed. Conversely, the vital demerit of dynamic logic style is its high noise sensitivity. The main reason for this is the sub-threshold leakage current flowing through the pull down network. With continuous technology scaling, this problem is getting more and more severe.

In this thesis, a new noise tolerant dynamic CMOS circuit technique is proposed. In the proposed work, we have enhanced the behavior of the domino CMOS logic. This technique also gets benefit in terms of delay and power. This thesis describes the new low power, noise tolerant and high speed domino logic technique and presents a comparison result of this logic with previously reported schemes. Simulation results prove that, in 180 nm CMOS technology when we used this logic style to realize wide fan-in logic gates, it could achieve maximum level of noise robustness as compared to its basic counterpart. In addition, the logic also works efficiently with sequential circuits.

The feasibility of this new technique is demonstrated by means of a real hardware, we have built a custom test-chip in the UMC 180 nm process technology with an ALU core, using the proposed domino logic style for each design block. In this thesis, we have also described the design and implementation of this chip. In addition to this, we have also presented initial power and delay performance comparisons between the circuit level simulated ALU and test-chip implemented in the proposed domino logic style.

Finally we conclude that, the thesis contributes a very efficient logic style for wide fan-in gates, which is not only noise robust but also energy efficient and high speed.

ABBREVIATION

14TCMOS	-	14 transistor complementary metal–oxide–semiconductor
ALU	-	Arithmetic logic unit
ANTE	-	Average noise threshold energy
CDL	-	Conventional dynamic logic
CLK	-	Clock
CMOS	-	Complementary metal–oxide–semiconductor
CPL	-	Conventional pass transistor logic
CSL	-	Conventional static logic
DC	-	Direct current
DRC	-	Design rule check
ERC	-	Electrical rule check
FF	-	Flip-flop
GDI	-	Gate diffusion input
GND	-	Ground
LVS	-	Layout versus schematic
NIC	-	Noise injection circuit
NMOS	-	N-type metal-oxide-semiconductor
OUT	-	Output
PDN	-	Pull-down network

PDP	-	Power delay product
PMOS	-	P-type metal-oxide-semiconductor
PUN	-	Pull up network
SFEG	-	Source following evaluation gate
TFA	-	Transmission function full adder
TGCMOS	-	Transmission gate complementary metal–oxide–semiconductor
UMC	-	United Microelectronics Corporation
UNG	-	Unity noise gain
VLSI	-	Very large scale integration

Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The modern technologies move towards smaller, faster, and cheaper computing systems. This has been facilitated by exponential increase in device density and operating frequency through VLSI technology scaling. This has led to an increase in power consumption that has reached limits of reliability and cost. In addition, continued scaling into the nanometer system has brought design robustness issues such as soft error, signal integrity, and process variability. In addition, the issues of power consumption and robustness are affected with time. This has created a predicament in computer system design that intimidated to be an uncertain block to future advancement.

Researchers of pioneer computing systems have found that power consumption and design robustness must be taken into account at every level of design. For any design in circuit level, the choice of logic styles is very significant as it directly affects power, performance, and robustness. Static CMOS and domino logic do not fully meet the needs of future computing. Two basic CMOS circuit designs are static logic and dynamic logic. Static CMOS is better energy-efficient and robust but is very slow to be used in critical and massive designs. Domino logic is fast but consumes loads of power and is not at all robust. Also, domino logic scales poorly so that its speed advantage is much narrowed. Its power and robustness are worst and having a lot of inconvenience. We therefore require improved digital logic technique and style which is at the same time energy efficient, fast and noise robust.

In this thesis, we have proposed semi-domino logic for footed logic circuit implementation. Using this logic, unwanted pulses of the dynamic node, which are generated during the precharge process, are prevented to pass to the output node, as is in the conventional case. As a result a lot of power is saved as compared to other domino gate logic circuits. This logic is again modified using keeper and some footer transistors to get a better energy-efficient, robust and high speed logic.

In this thesis, this logic gate is peer analyzed and compared with the same circuit designed with other logic styles. This logic design is also applied to comparator and adder. To demonstrate advantages of the proposed logic in real hardware, we built a custom test-chip using a full custom design with UMC 180 nm process.

1.2 PARAMETERS OF ENHANCEMENT

CMOS technology is the dominant logic style in today's IC design because of its high speed, low power and high packaging density. With continuous technology scaling i.e. reduction in feature size leads to high packaging density which leads to increase in current density as well as power density. Large increase in current or power density causes serious reliability problems for scaled transistors like oxide breakdown, hot carrier injection [1] [2] [3] [4]. This increase in power density can be reduced by supply voltage (V_{DD}) scaling because of the quadratic relationship between power and V_{DD}, but rate of supply voltage scaling is not as fast as rate at which device dimensions are scaled because of various physical limitations like built in junction potential or silicon band gap which can't be scaled further.

1.2.1 POWER

Ideally, in CMOS circuits the output node is either connected to V_{DD} or GND. Due to absence of direct path between V_{DD} and GND CMOS circuits dissipates zero static power. But practically MOS transistor never acts as perfect switch. There is always a leakage current which leads to static power dissipation. The various sources of power dissipation [5] [6] in CMOS are,

- Static Power Dissipation
- Dynamic power Dissipation

The total power in a static CMOS is given by [5]

$$P_{Total}=P_{Static}+P_{Switching}+P_{ShortCircuit} \quad (1.1)$$

1.2.2.1 STATIC POWER DISSIPATION (P_{STATIC})

It is the power dissipated when there is no switching activity within a circuit. Ideally, CMOS circuit dissipates no static power, since there is no direct path from V_{DD} to GND. But practically MOS transistor never acts as perfect switch. There is always leakage current which flows when the input(s) to and the outputs of a gate are not changing, leads to static power dissipation. But as the supply voltage is being scaled down to reduce dynamic power, low V_{TH} transistors are used to maintain performance. Reduction in V_{TH} of transistor leads to greater leakage current [5].

Static power dissipation is given by

$$P_{Static} = V_{DD} * I_{Leakage} \quad (1.2)$$

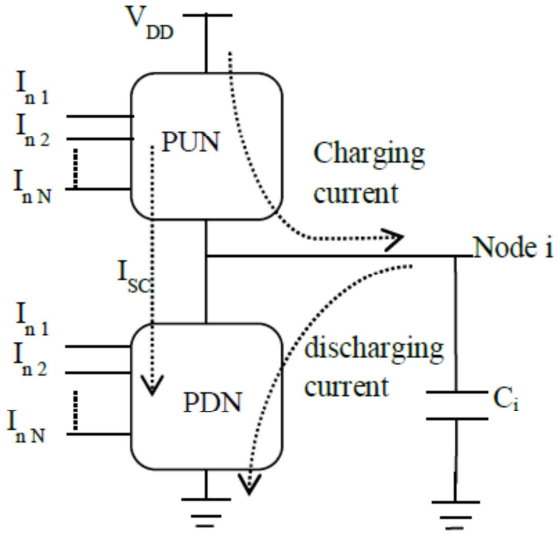


Fig.1.1 Switching and short-circuit current elements in static CMOS

1.2.2.2 DYNAMIC POWER DISSIPATION

It is the dominant portion of power dissipation which occurs due to transit ion at gate outputs. It consist two components of power dissipation.

1) Switching Power dissipation ($P_{Switching}$)
2) Short Circuit Power Dissipation ($P_{ShortCircuit}$)

1) Switching Power dissipation ($P_{Switching}$)

As the nodes in a digital CMOS circuit transition back and forth between two logic levels, the capacitance associated with the nodes gets charged and discharged. Power

dissipated during this process is called as switching power and it is a major source of power dissipation in CMOS circuits. For a static CMOS circuit with N switching nodes operating at clock frequency f_{clk}, the switching power is given by [7].

$$P_{Switching} = \sum_{i=1}^{N} \alpha_i C_i V_{DD} V_{Swing} f_{clk} \quad (1.3)$$

Where α_i = switching activity at node i

V_{DD} = supply voltage

V_{Swing} = Voltage swing at node i

$\alpha_i C_i$ is the effective switch capacitance per cycle at node i

2) Short Circuit Power Dissipation ($P_{ShortCircuit}$)

This is due to short circuit current (I_{SC}) which flows directly from V_{DD} to GND when both PMOS and NMOS transistor are ON. When input to the gate gets stable at either logic level only PMOS or NMOS transistors are ON. Hence no short circuit current flows. But when output of a gate switches in response to change in inputs, both PMOS and NMOS transistors conduct simultaneously for a short interval of time. This interval of time depends upon rise or fall time of input signal and causes short circuit power dissipation.

$$P_{ShortCircuit} = V_{DD} * I_{SC} \quad (1.4)$$

1.2.2 PROPAGATION DELAY

The dependency of propagation delay on circuit parameter is given by [8]

$$T_d \, \alpha \frac{C_L V_{DD}}{k(V_{DD} - V_{TH})^{\alpha}} \quad (1.5)$$

Where α is the velocity saturation index

k depends upon W/L

From equation 1.3 and 1.5, the power dissipation and propagation delay both depends upon the supply voltage (V_{DD}). The scaling of supply voltage causes the reduction in power whereas the propagation delay significantly increases. So for each design depending upon its application there exist a tradeoff between power and delay.

1.2.3 NOISE

Continuous scaling of CMOS technology makes noise become an equally important metric like power, performance and area. To maintain performance with the scaling of supply voltage threshold voltage is also scaled down, resulting in reduction of noise margin. In current CMOS technology with reduced spacing between interconnect and higher operating frequency makes capacitive and inductive coupling [9] to increase significantly resulting in severe side effects on signal integrity.

Hence various logic styles are used to construct logic gates depending upon its application in terms of power, speed, noise robustness and area.

1.3 MOTIVATION FOR THE WORK

1.3.1 NEED FOR LOW-POWER

Fast advancement of VLSI CMOS circuit technology is satisfied by increased use of small sized and wireless systems with very low power consumption. Due to the continued scaling of supply/threshold voltage and technology, leakage power is becoming very significant in power dissipation of nano-scale CMOS circuits. Consequently, the total power consumption is a critical factor while designing low power digital circuits [10].

1.3.2 NEED FOR HIGH SPEED

Rapidly increasing demand for higher speeds in the areas of signal processing, high-speed computing, communication, and related instrumentation includes an urgent requirement for very high-speed integrated circuits. Availability of sub-100-ps VLSI circuits and volume production are having great impact on these areas. The time delay related with interconnections is becoming an important factor for the calculation of total chip delay per gate in high-speed VLSI circuits [11].

1.3.3 NEED FOR NOISE-IMMUNITY

Now-a-days technology is scaled down into the deep sub-micron system, due to which, noise immunity is becoming a significant issue in VLSI chips design [12] [13] [14]. Noise in the digital circuit design is defined as any possible event which can cause the voltage at node to vary from actual value. Various sources of noise like crosstalk, variation in charge sharing, leakage current and supply voltage are present in VLSI chip design [15] [16]

[17] [18] [19] [20]. The leakage current through the transistors of a digital circuit is increasing exponentially with technology scaling.

1.3.4 NEED FOR LESS-AREA

Size minimization with increased application is now the major demand in recent world. This demand has really given rise to VLSI [21] [22] [23]. In every field like wireless systems, mobile systems to the daily use equipment, there is an aggressive need of minimizing area or size.

1.4 OBJECTIVE OF THE RESEARCH WORK

Recent technology scaling and use of various logic families provides techniques to achieve power consumption at the cost of performance. Power, speed and robustness are so critical to leading edge designs that they need to be taken care of each level of design. The choice of logic styles is a very important constraint at the circuit level. Logic styles differ in terms of energy, delay, area and robustness. Because every design requires compromises and trade-offs, designers need to pick and choose circuits from different points on an energy-delay-robustness envelope to meet each circuit need. Among other things, meeting the needs of future computing will require logic style that satisfies high-performance, low-power, high-robustness in the form of noise and variability, ease of implementation and verification. In addition to that, we want to use logic styles that are compatible for all types of logic implementation for further improvement in robustness. In the following chapters we will show why existing logic styles do not meet these needs and how the proposed logic can fill the void. The objective of this research work is to modify and improve domino logic that can provide further improvement in power consumption, performance, noise margin and area overhead.

1.5 THESIS ORGANIZATION

This thesis is organized in such a way as to properly layout a detail investigation and results of the research work.

In chapter 1 objective of the thesis with a summary of thesis organization are presented.

Chapter 2 provides the background of CMOS logic styles and recent proposed works to upgrade dynamic logic.

In Chapter 3 the proposed logic has been described. A peer analysis of the proposed logic is presented. Furthermore, we have to compare the same with previous logic styles recently proposed by other researchers and conclude with merit and demerit of the proposed circuit.

Chapter 4 shows the noise analysis of the proposed circuit. In this chapter, we have simulated and compared the proposed logic style with various logic styles and shown how the proposed logic proves to be noise tolerant as compared to the other logic styles.

Chapter 5 describes some applications of proposed domino logic. Comparator and adder circuits are designed with the proposed logic and are analyzed with respect to the previous proposed comparator and adder circuits.

Chapter 6 demonstrates advantages of proposed logic in real hardware; we built a custom test-chip in the UMC 180nm process with the proposed logic styles. We describe the design, implementation, operation, and testing of this chip. We also present initial energy delay performance comparisons between the simulated one and the real hardware.

Chapter 7 summarizes the contributions of this thesis and discusses possible perspectives for future work.

Chapter 2

BACKGROUND LOGIC STYLES

2.1 DIFFERENT LOGIC STYLES

2.1.1 STATIC CMOS LOGIC

Static CMOS circuits consist of a pull up network (PUN) and a pull down network (PDN) as depicted in Fig.2.1(a) [1], [24]. The PUN block consists of PMOS transistors, which pull up the output node (OUT) to V_{DD} and the PDN block consist of NMOS transistors, which pull down the OUT node to GND. At any instant of time either the pull up or pull down block is on; so that the OUT node remains either at V_{DD} or GND. The size of PMOS devices is larger than NMOS devices, because the mobility of PMOS is lower than the mobility of NMOS. The structure of a CMOS inverter is shown in Fig.2.1 (b). It consists of a PMOS and a NMOS transistor. The operation of the circuit is as follows; when INPUT A is HIGH (V_{DD}), T_N is ON and T_P is OFF. A direct path exists from node Y to ground, resulting 0 V at the output node Y. When A is LOW (0 V), T_P is ON and T_N is OFF, resulting in a steady voltage of V_{DD} at node Y.

Properties

1. A transistor operates as a ‘switch’ controlled by its gate.
2. PMOS transistors are used to construct the PUN; while the NMOS devices construct the PDN.
3. Parallel connected NMOS transistors represent an OR function; series connected NMOS transistors represent an AND function.
4. 2N numbers of transistors are required to implement an N-input logic.

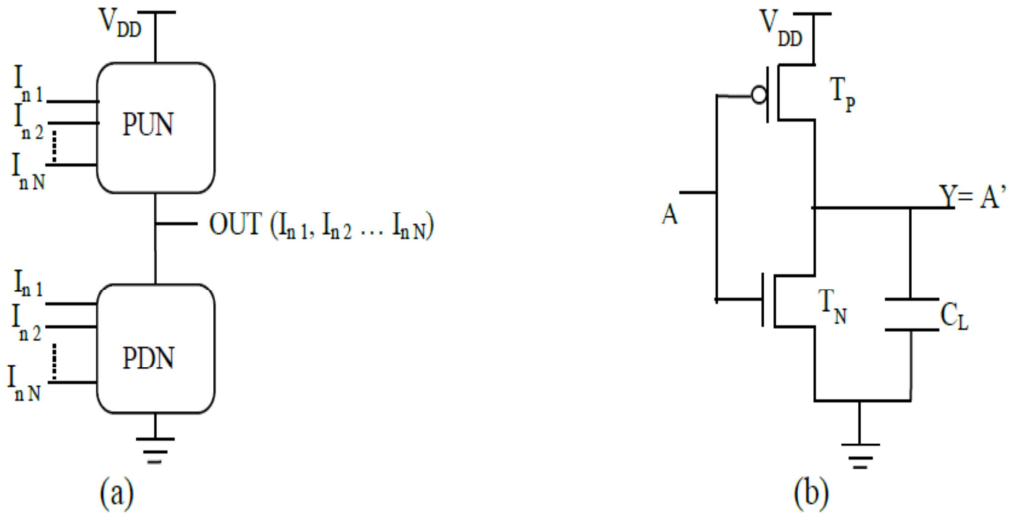


Fig.2.1(a) CMOS logic gates as a combination of PUN and PDN (b) CMOS inverter [25]

Advantages

1. In static logic, the voltage swing at node OUT is equal to either the supply voltage V_{DD} or GND [1]. Such characteristic of the CMOS circuits result in high noise margin [2].
2. The logic levels of static CMOS logics are independent of relative size of the transistors, so that the transistors can have minimum size [26]. Logic circuits having this property are known as 'Ratio-less Logic circuits', where the relative dimensions of the composing transistors do not determine logic levels of the circuit.
3. In steady state, a path always remains with finite resistance between either output node (OUT) to V_{DD} or GND. Therefore, CMOS inverter has low output impedance.
4. Low impedance of the circuit makes the circuit noise tolerant [1].
5. As the gate of a CMOS transistor works as an insulator, the input resistance becomes very high. Therefore, it consumes no DC current. The input of inverter is only connected to a gate of the transistor. In the steady state input current is nearly zero.
6. There is absence of direct path between V_{DD} and GND. This means that, the gate does not consume any static power.
7. Switching threshold of the circuit is $V_{DD}/2$. Therefore the circuit becomes more robust.

Limitations

1. When the input signal is having finite rise or fall time, both the NMOS and PMOS transistors are ON during a very short interval of time leads to short circuit current [1] [26].
2. In this logic a fan-in of N requires 2N devices results in larger circuit area.

2.1.2 DIFFERENT TYPES OF STATIC LOGIC

2.1.2.1 PSEUDO N-MOS

Fig.2.2 shows a modified form of CMOS inverter. Here only Q_N is driven by the input voltage. The gate of Q_P is grounded and acts as an active load for Q_N. The load is called as the "Pseudo NMOS Load" [1] [24] as depicted in Fig.2.2. This inverter circuit is another form of NMOS logic that consists of a driver transistor Q_N and a load transistor Q_P. Hence the name is 'Pseudo NMOS'.

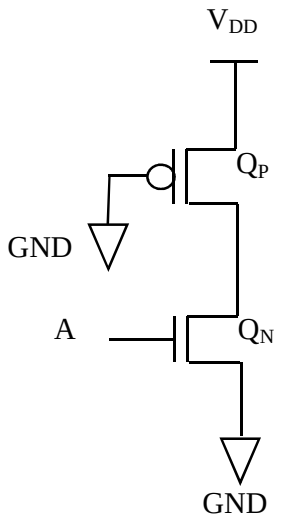


Fig.2.2 Pseudo-NMOS logic

Advantage

In Pseudo-NMOS logic a fan-in of N requires only N + 1 number of transistors. This transistor count is nearly half to the static logic.

Disadvantage

1. This circuit has less noise margin so it is very sensitive to noise.
2. It consumes more static power compared to static CMOS because of the presence of a PMOS transistor which is always ON.

2.1.2.2 PASS TRANSISTOR LOGIC

Pass transistor logic is a widely used option of complementary-CMOS, because it tries to minimize transistor count needed for implementing a function by letting the inputs to drive gate terminals as well as source or drain terminals. This phenomenon is very much different than other logic styles that we have discussed in the above literature, which the gate terminals of MOSFETs are only driven by the primary inputs [27] [28] [29] [30] as depicted in Fig.2.3.

Advantages

1. It reduces the transistor count required to implement the same logic which allows the inputs to drive the gate, source and drain terminals of MOSFET [27].
2. Reduction in the number of devices also reduces the output capacitance of the circuit.

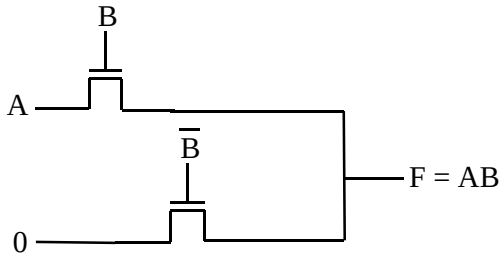


Fig.2.3 Static Pass-transistor logic

Disadvantage

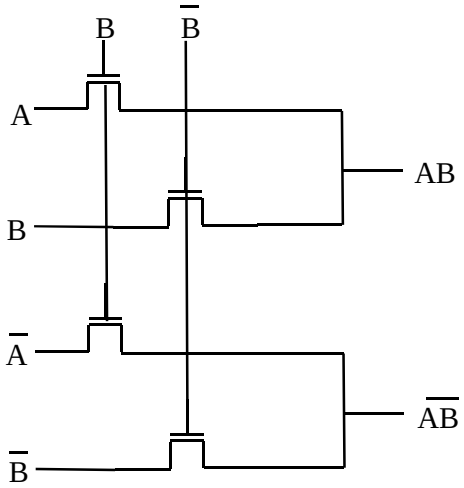
1. Pass transistor logic cannot be cascaded.

2.1.2.3 COMPLEMENTARY PASS-TRANSISTOR LOGIC

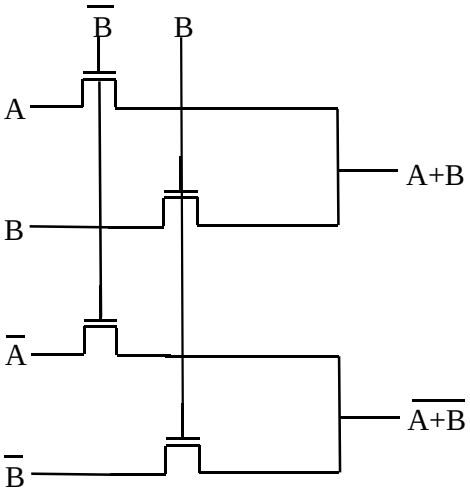
In high performance logic design this logic family, called Complementary-PTL or Differential-PTL, is generally used [31] [32] [33] [34]. The basic idea is to accept the complementary input and produce complementary output as depicted in Fig.2.4.

Advantages

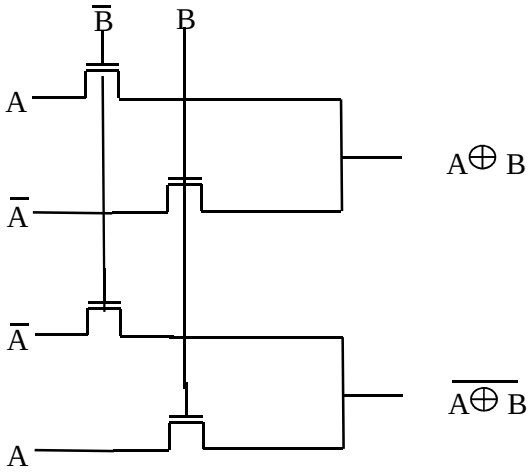
1. With this logic complex CMOS gates like XOR, XNOR and adders with less numbers of transistors can be implemented [31].
2. In this logic gates, as the output nodes are either connected to V_{DD} (power supply) or GND over a low resistance path [32].



AND/NAND



OR/NOR



XOR/XNOR

Fig.2.4 Static Complementary-PTL

Disadvantages

1. In complementary pass transistor logic, there is a presence of static power dissipation [31].
2. Noise margin is reduced as compared to static pass transistor logic [1].

2.1.2.4 GATE-DIFFUSION-INPUT (GDI)

GDI is a new technique of realizing CMOS static logic technique, which is based on the use of a simple cell structure. A first look towards the basic cell looks like standard CMOS inverter. Important properties of GDI cell are : GDI cell contains inputs G (common gate input of NMOS and PMOS), N (input to the source/drain of NMOS) and P (input to the source/drain of PMOS) [35] [36] [37] [38] [39] as depicted in Fig.2.5.

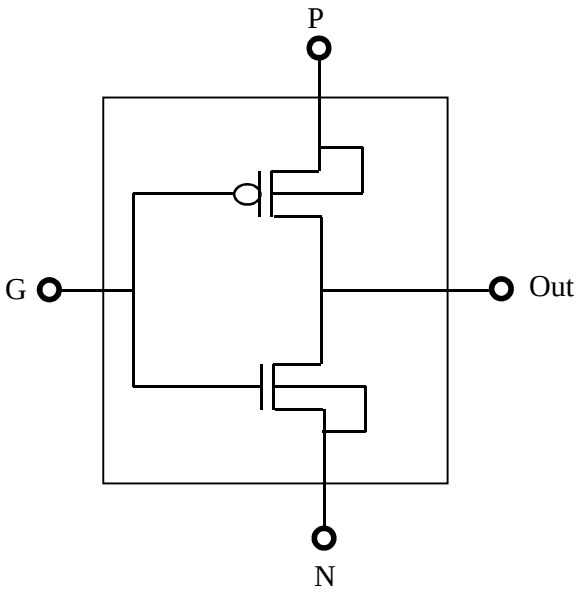


Fig.2.5 Gate-Diffusion-Input logic

Advantages

1. This gate diffusion input circuit technique requires very less number of transistors [35].
2. Due to presence of less number of devices, the circuit requires less power to operate [36].

Disadvantage

This circuit technique is not convenient for large logic designs [37].

2.2 DYNAMIC CMOS LOGIC

The pseudo NMOS logic style needs N + 1 number of transistors for realizing an N-input logic gate. This logic has more static power dissipation. Dynamic logic uses a clock input, by which it experiences a series of precharge and conditional evaluation phases as shown in Fig.2.6 [1] [40] [41] [42] [43].

Precharge phase:

When the CLK is 0, the node OUT precharges to V_{DD} through T_P, PDN is disabled because T_E is OFF.

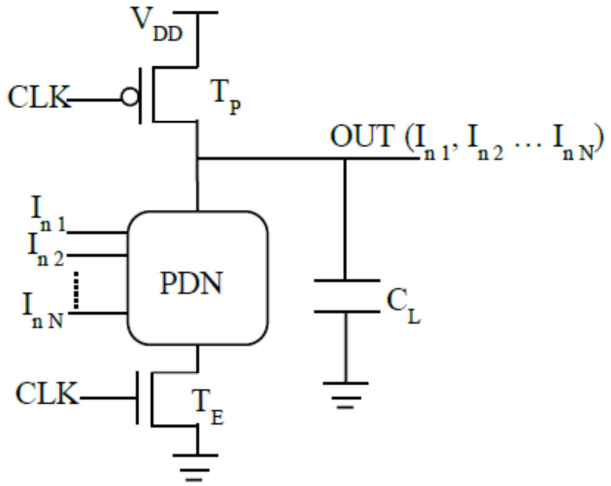


Fig.2.6 Dynamic logic

Evaluation phase:

When CLK=1, T_P is OFF and T_E is ON. The node OUT conditionally discharges based upon input value to the pull down network. Throughout evaluation phase, the only possible path from node OUT is only ground (GND). The output node (OUT) can only discharge in evaluation phase and charges to V_{DD} during precharge phase [41].

Advantages

1. The logic function is result of the parallel and series arrangements of NMOS pull down network.

2. N + 2 number of transistors required to implement dynamic logic, which is less than that of static logic [1].
3. This logic is non-ratioed. The size of the PMOS devices is not important for realizing correct functionality of the circuit.
4. This logic gates consume only dynamic power. In ideal condition, the static current path never exists between the supply voltage V_{DD} and GND.
5. Gates designed with this logic have faster switching speeds [42]. This is because of reduced load capacitance attributed to the lower number of transistors per gate absence of short circuit current in the dynamic gate.

Limitations

1. It has low noise margin due to reduction in switching threshold.
2. Output is in high impedance state, if PDN is turned off during evaluation phase.
3. This logic circuit suffers from charge leakage and charge sharing.

2.2.1 ISSUES IN DYNAMIC LOGIC

The dynamic logic results in high performance solutions as compared to its static counterpart. If one needs dynamic circuits to operate properly, there are numerous important things that must be considered. This includes charge sharing, charge leakage, back gate or capacitive coupling, and clock feed through. In this section we have discussed these issues briefly.

2.2.1.1 CHARGE LEAKAGE

The operations of dynamic gate depend on charge stored in dynamic node capacitor [1]. If pull down network is conditionally off, the output should ideally remain at high in evaluation phase. But, charge of the dynamic node gradually leaks away due to leakage currents, eventually resulting in a malfunctioning of the gate. Fig.2.7 depicts the source of leakage for the basic dynamic logic circuit. This phenomenon is also presented in [44] [45] [46] [47] [48].

The reverse-biased diode and sub-threshold leakage of the NMOS pull-down device M_1 are responsible for the charge leakage in dynamic circuits. The charge of the output capacitor C_L leaks away due these above mentioned sources of leakage. This phenomenon degrades the circuit performances. It can be noted that the PMOS precharge device also contributes some leakage current due to the reverse bias diode and the subthreshold

conduction. The leakage current of the PMOS counteracts the leakage of the pull down path to some extent.

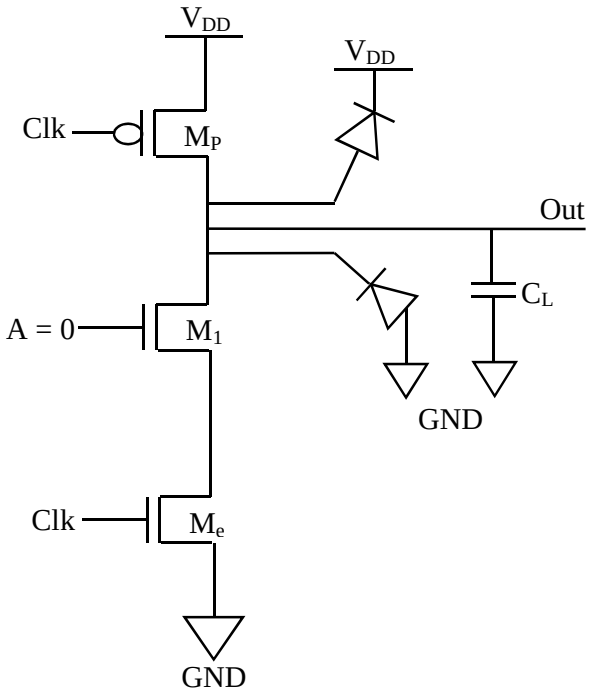


Fig.2.7 Charge leakage

2.2.1.2 CHARGE SHARING

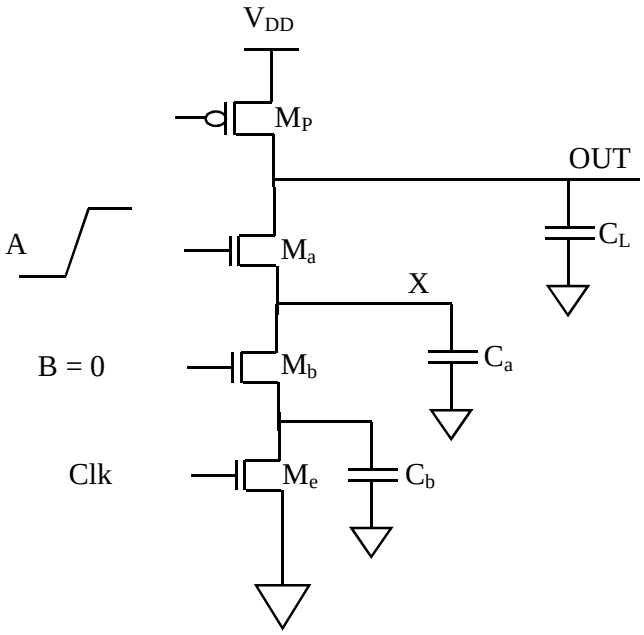


Fig.2.8 Charge sharing

Charge sharing in dynamic logic is a vital concern in dynamic logic [48] [49] [50] [51] [52] [53]. Assuming output node is precharged to V_{DD} during the precharge phase. Let's consider that, during precharge all the inputs are set to logic zero so the capacitance C_a gets discharged. Let's further consider that, input B stays at zero during the evaluation, while input A makes a transition from 0 to 1. By doing this, M_a will get on [1]. When M_a will get ON, the charge stored at C_L will be distributed over C_L and C_a. this results in drop in the output voltage and cannot be recovered due to the dynamic nature of the circuit as depicted in Fig.2.8.

2.2.1.3 CAPACITIVE COUPLING

The high impedance of output node makes the circuit very sensitive towards crosstalk noise as shown in Fig.2.9. A wire routed over a dynamic node may couple capacitively and destroy the state of the floating node i.e. Out_1. One more important form of capacitive coupling is back gate (or output-to-input) coupling [54] [55] [56] [57] [36] [37] [38] [39] [58].

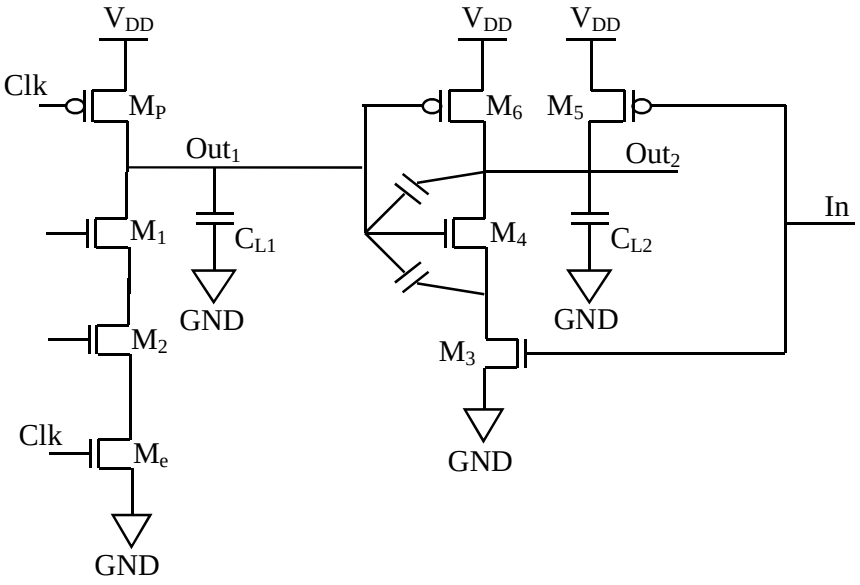


Fig.2.9 Capacitive coupling

2.2.1.4 CLOCK-FEEDTHROUGH

This is a special case of capacitive coupling, which is called as clock feedthrough [59] [60] [61] as depicted in Fig.2.10. During precharge phase (Clk = 0) the output node goes to V_{DD}. By assuming evaluation transistors are in OFF state, when Clk makes a transition from

low to high, due to the coupling capacitance between gate of M_P and output node (Out_1); the output of the dynamic node to rise above V_{DD}. This is depicted as clock feed through [1].

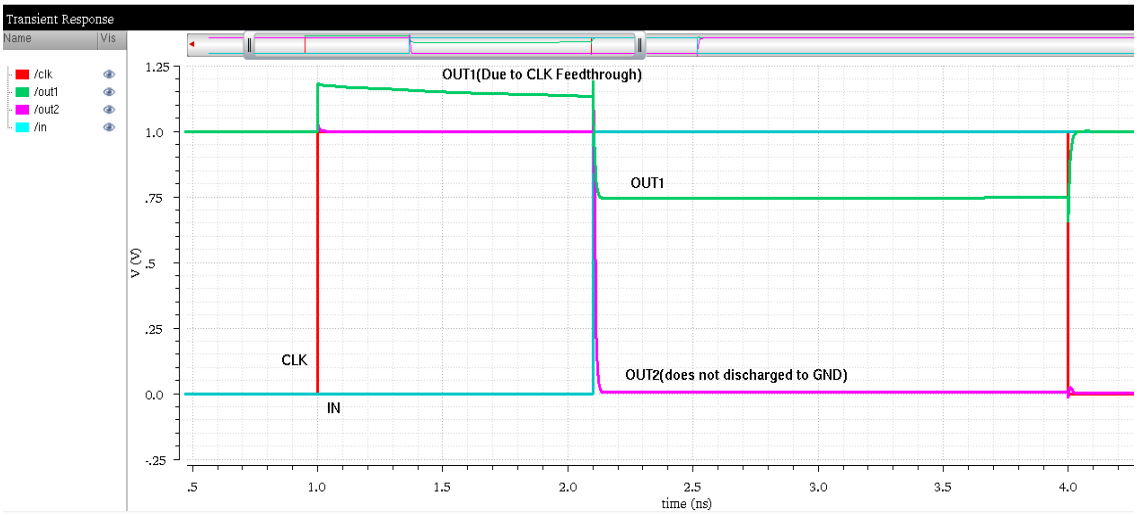


Fig.2.10 Clock feed-through

2.3 DOMINO LOGIC

The domino logic [62] [21] [63] [64] [65] [66] [41] [67] [68] structure is similar to that of dynamic logic along with a static CMOS inverter that is used to avoid cascading problem as shown in Fig.2.11. During precharge phase (CLK = 0), output is charged to V_{DD} and output of inverter becomes zero. In the evaluation phase (CLK = 1), the node OUT makes only transition from 0 to 1. Since in the precharge phase the node OUT discharges to logic 0, hence the false evaluation is avoided during cascading of various domino blocks. As it uses static inverter only non-inverting logic can be realized and it increases propagation delay.

Property

The domino gate contains a static inverter, so, non-inverting logic can only be implemented using this logic [1] [63].

Advantage

Domino logic gates can achieve very high speed. The inverters can be sized to match the fan-out, which are much smaller than in complimentary static CMOS, as only the gate capacitance has to be accounted for per fan-out gate [66].

Limitation

Only the non-inverting logic can be implemented [66].

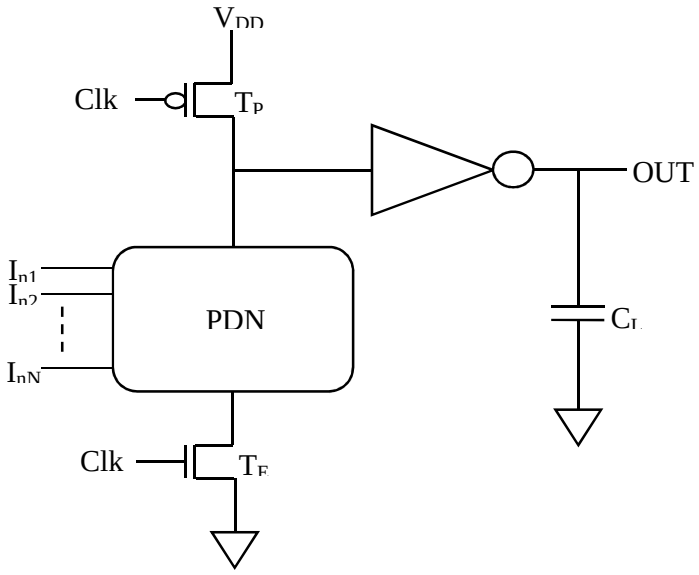


Fig.2.11 Domino CMOS Logic

2.3.1 RACE CONDITION IN DOMINO LOGIC

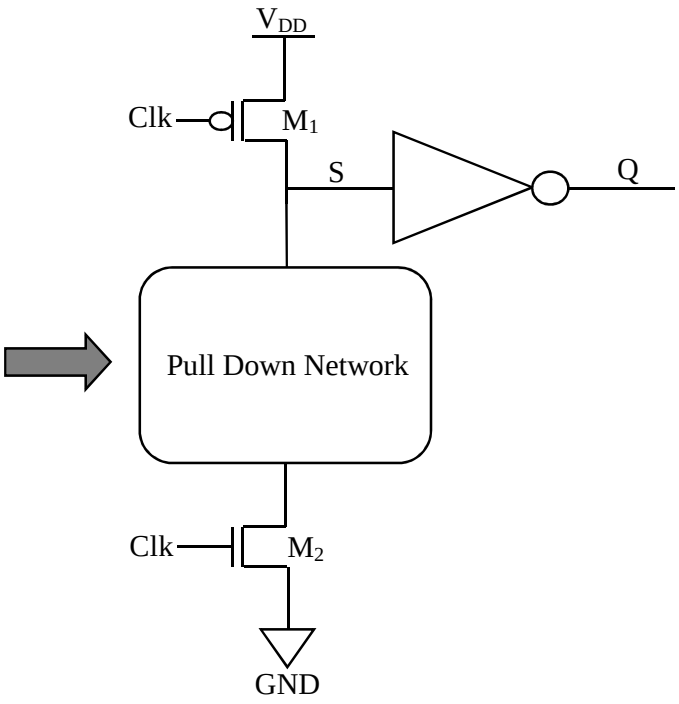
The possibility of race conditions is high in domino logic, when clock is slow. The slow clocks, in domino logic based sequential circuits there present a time window where NMOS and PMOS are conducting. This will lead to path between input and output, which can disturb the functionality of the circuit.

Not only in slower clocks, the race conditions also occur for long rise time and fall times. The domino logic based sequential circuit functionality and performance will be intact as long as the clock rise time and fall time is smaller than 3 to 5 times of the propagation delay of the application circuit. This criterion is easy to achieve in larger circuits and in smaller circuits, designer has to take care propagation delay, rise time, fall time and frequency of the clock to avoid race condition.

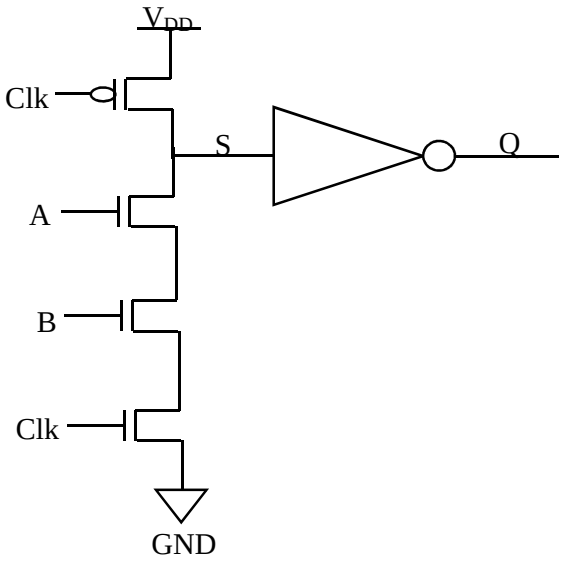
2.4 OVERVIEW OF PREVIOUS WORKS

Noise in digital integrated CMOS circuit is becoming one of the principal problems in deep submicron technology [69] [70]. In past three decades, researchers have developed many circuit techniques to develop the noise tolerance of domino logic gates. For discussing most of the previous proposed techniques, in this section we have presented a summary of some of the significant methods. In this section, we have classified all previous proposed techniques into four main groups depending upon their circuit modifications and principle of operations:

1. Keeper implementation
2. Precharge of internal nodes
3. Source voltage raising
4. Complementary p-network



(a)



(b)

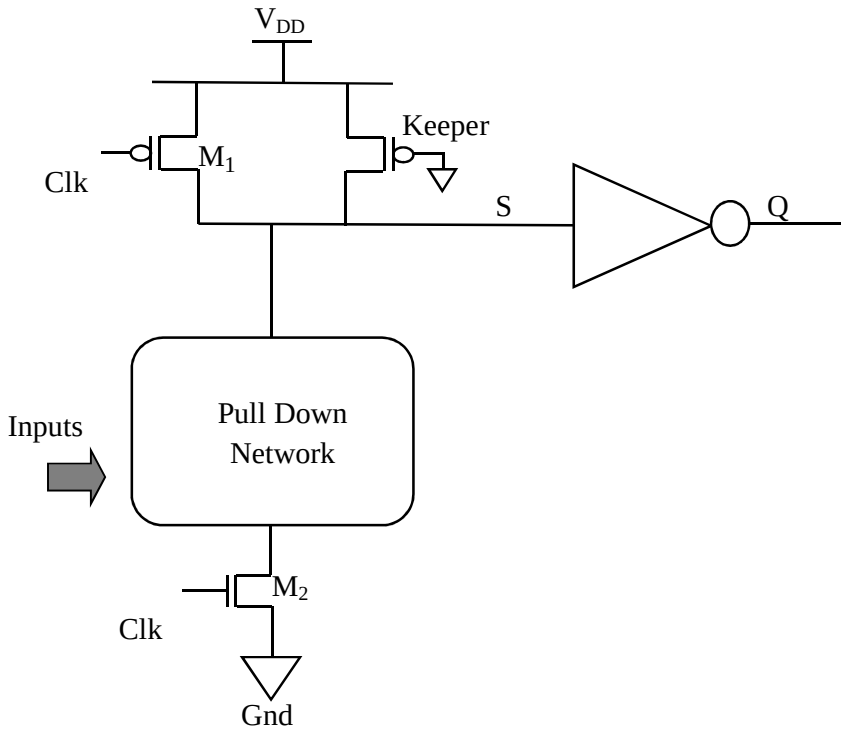
Fig.2.12 CMOS domino logic (a) Schematic of domino circuit (b) Schematic of 2 - input domino AND gate

2.4.1 KEEPER IMPLEMENTATION

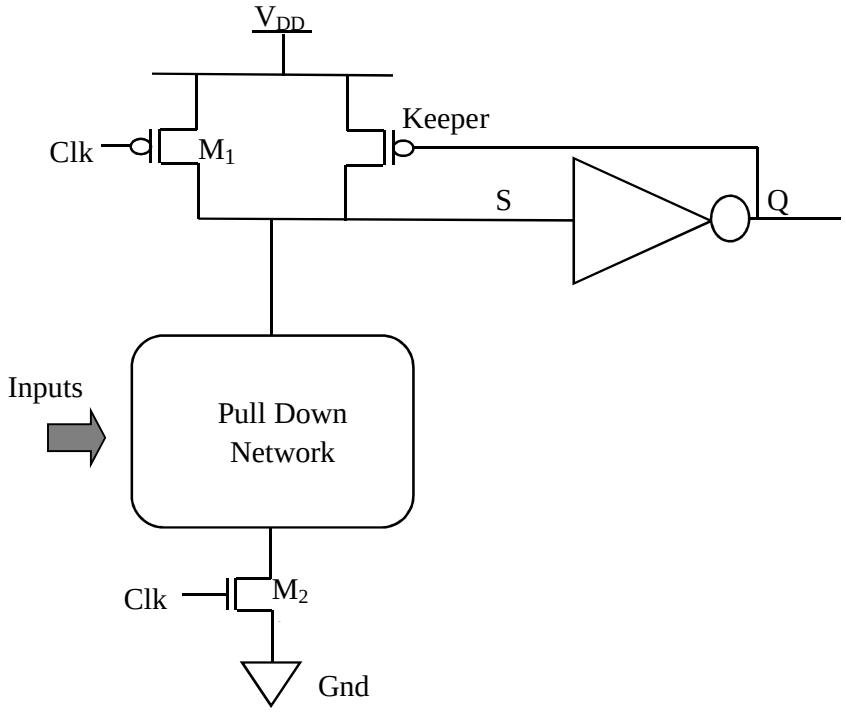
This technique is the easiest method for domino CMOS logic circuit to improve its noise tolerance performance. This technique was based on employing a weak transistor, which is called as "keeper transistor", connected from V_{DD} to dynamic node as depicted in Fig.2.12. To maintain charge stored in the dynamic logic, keeper transistor provides a small amount of current from V_{DD} to dynamic node of the domino logic. In basic domino logic circuit [71], gate of keeper transistor was connected to the GND, as depicted in Fig.2.13(a). This type of connection keeps the keeper transistor in always ON state. After some years, feedback keeper technique was used, which is depicted in Fig.2.13(b). This technique was more broadly used because it could be able to eliminate a potential dc power consumption problem, which was a vital problem in the evaluation phase of always-on keeper of domino logics [72].

Keeper transistor causes lots of contention problem, when the PDN gets ON through evaluation phase, which results in slower gate performance. When we design a high fan-in gate with deep submicron technology; we need a very strong keeper transistor to compensate the large amount of leakage current flowing through the PDN of the logic gate. These strong keeper transistors have serious contention problem. Anis et al. in [73] and [74] as depicted in Fig.2.13(c) and Alvndpour et al. in [75] and [76] as depicted in Fig.2.13(d) have proposed two new types of keeper design techniques. Both the circuit techniques operate on the same basic principle, (i.e. they temporarily disable the keeper transistor for a very small time, when switching takes place at dynamic gate). Both the methods are extremely effective in noise tolerance enhancement of the dynamic logic gates against leakage noise. Still, these gates with large keepers are very much effective to external noise as dynamic node is not protected when the gate switches.

To reduce the internal and external noise P. Mazumder et. al in [77] as depicted in Fig.2.14(a,b) have designed a noise tolerant circuit technique using circuitry having an effect of negative differential resistance. An inverter is places to produce feedback signal instead of straight connecting it to output. This result in response time of feedback keeper transistor becomes independent upon output load. In this way, this technique independently optimizes the feedback inverter without concerned about the gate output.


V_{DD}
Keeper
M_1
Clk
S
Q
Pull Down
Network
Inputs
M_2
Clk
Gnd

(a)


V_{DD}
Keeper
Clk
M_1
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Network
Inputs
Clk
M_2
Gnd

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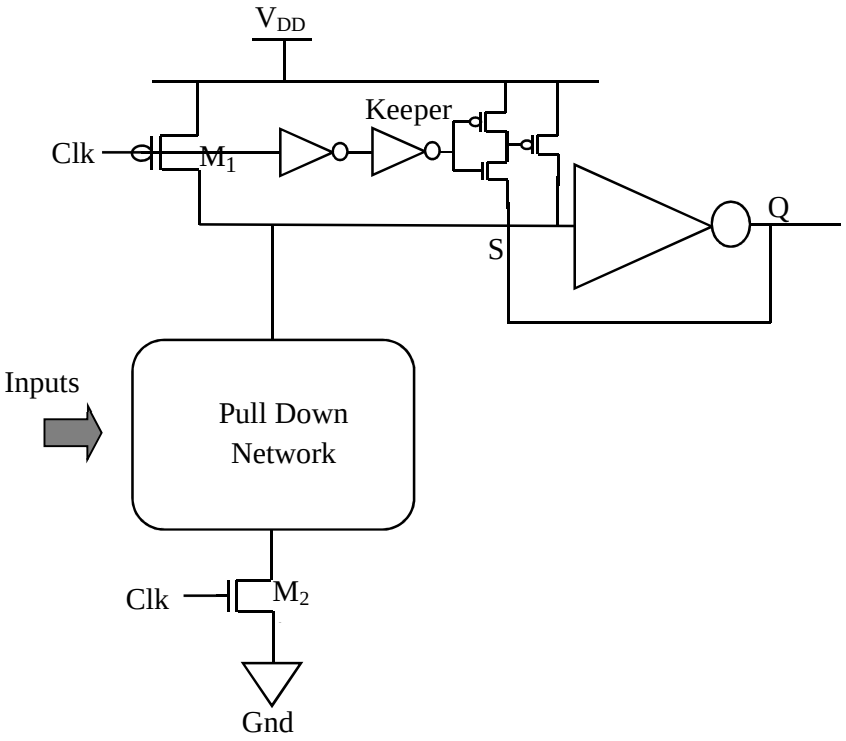
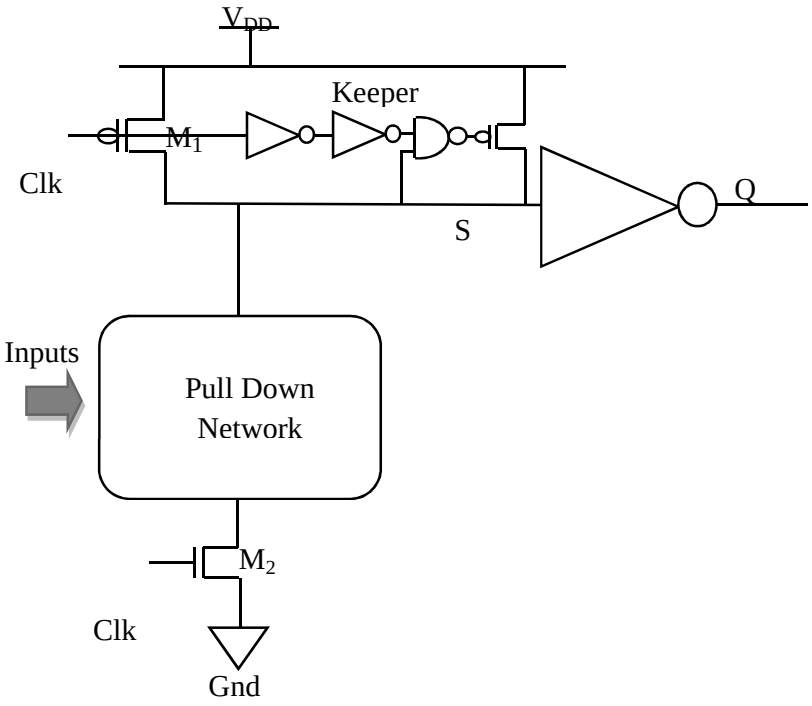
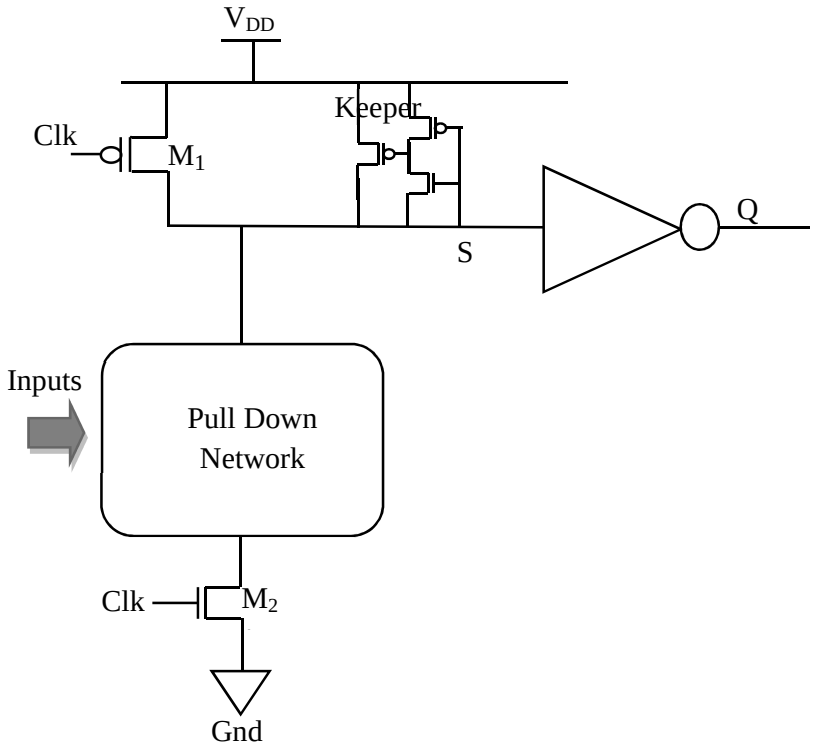


(c)

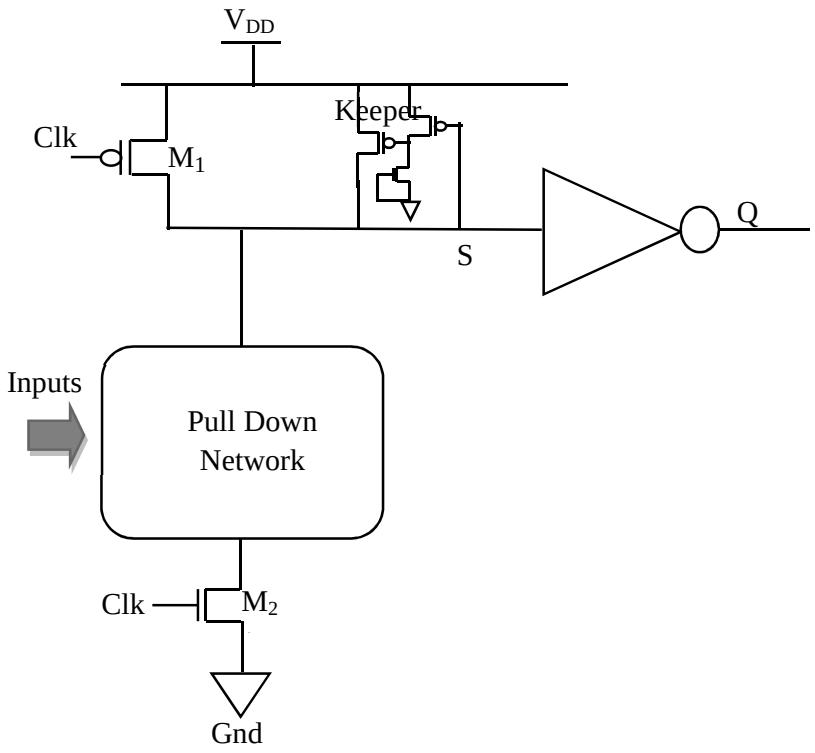


(d)

Fig.2.13 Keeper implementation (a) Implemented as constantly ON keeper [71](b) Implemented as feedback keeper [72] (c) High Speed feedback keeper implementation [73](d) Conditional keeper implementation [75]

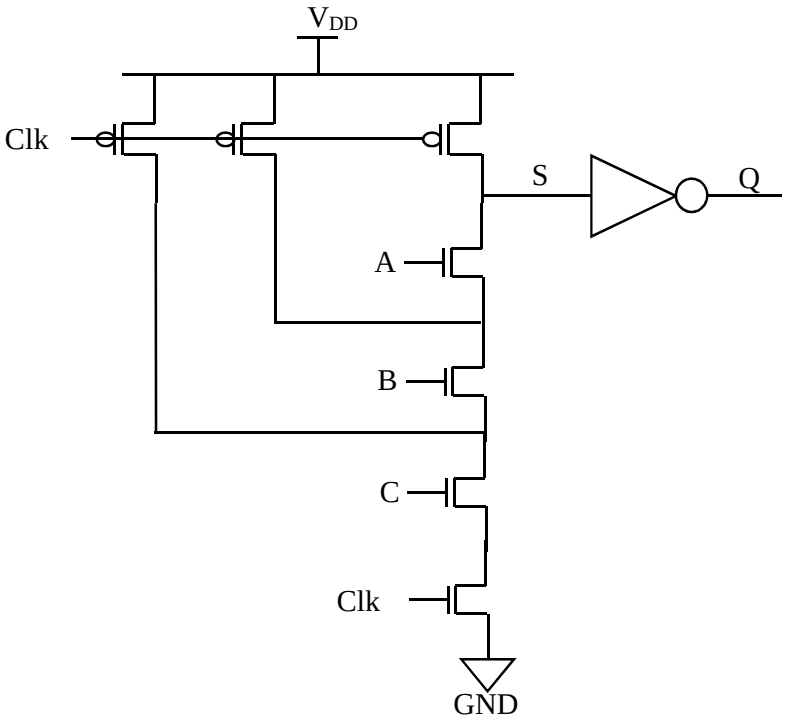


(a)

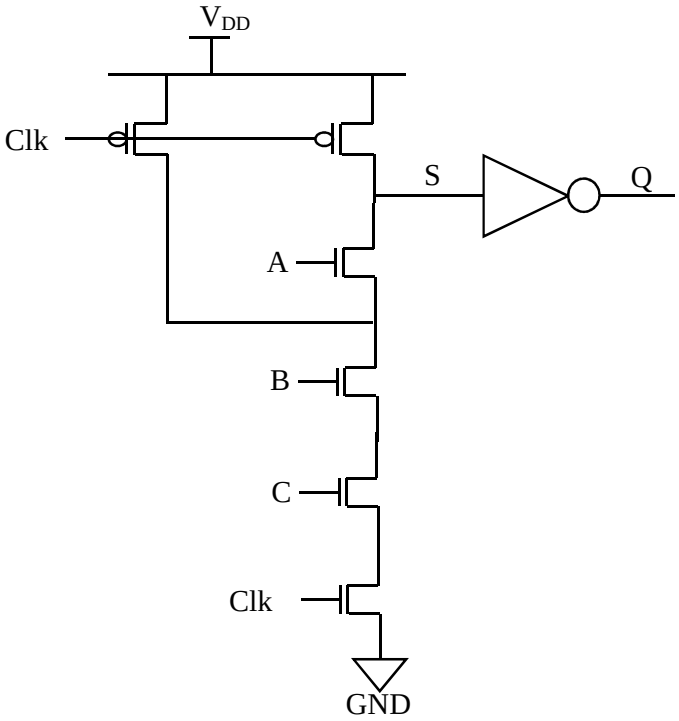


(b)

Fig.2.14 Implementation of optimized keeper (a) Implemented as inverter feedback (b) Implemented as pseudo PMOS inverter feedback



(a)



(b)

Fig.2.15 Precharging internal nodes implemented on AND3 gate, (a) Precharging every internal nodes [78], (b) Precharging some internal nodes [79]

2.4.2 PRECHARGE OF INTERNAL NODES

Logic gates having large fan-in have charge sharing among internal nodes in the PDN and dynamic node which results in false gate switching and output logic change. To avoid this charge sharing problem we can precharge the internal nodes along with dynamic node. [78] [79]. A dynamic AND3 gate designed with this technique has been shown in Fig.2.15(a). This technique could eliminate charge sharing problem in an expense of huge chip area, when all internal nodes get precharged. Partial precharge can also be done to the circuits as depicted in Fig.2.15(b), where not all but some of the internal nodes are precharged along with the dynamic node. This technique is a tradeoff between over chip area and noise immunity. If cost of inverter to produce the complementary clock signal can be justified, then to precharge all internal nodes, NMOS transistors can also be used. Meanwhile as the internal nodes are precharged, thus NMOS precharge transistors can decrease the dynamic power consumption of the logic gate and also reduce the discharging time. Thus it can be said that precharging internal node technique is not a very effective technique against noise.

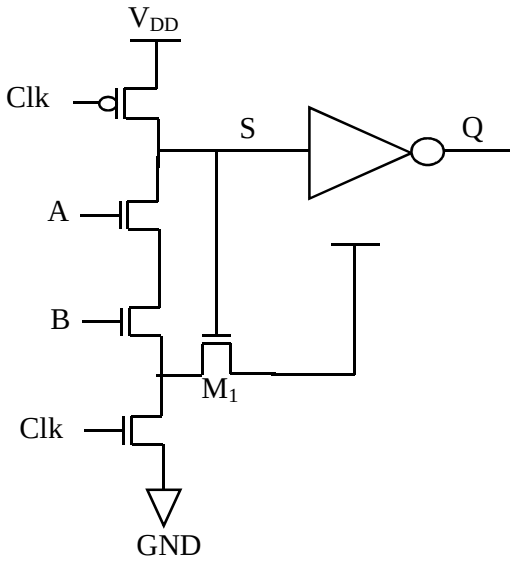
2.4.3 SOURCE VOLTAGE RAISING

Raising source voltage is one of the very efficient ways to minimize both external and internal noises. As the sum of transistor threshold voltage and source voltage should be lesser than the gate voltage to turn on a transistor, thus increase in source voltage can directly increase turn-on voltage of the gate. Furthermore, the threshold voltage of the transistor is increases with increase in the source voltage due to body effect,. This also contributes towards improvement of turn on voltage of the gate.

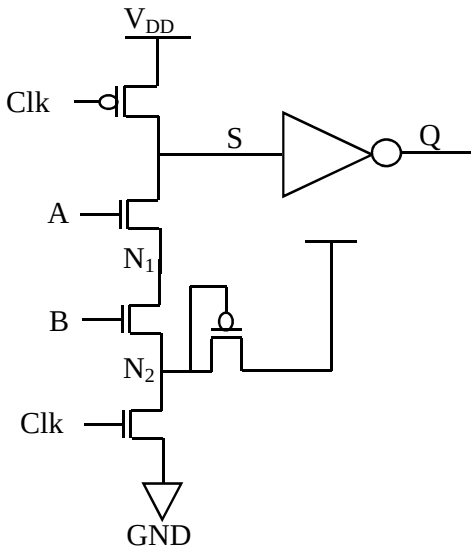
The PMOS pull up method of raising source voltage [80] as depicted in Fig.2.16(b). In this technique one PMOS transistor is employed at the internal node N_2 which forms a voltage divider having a clock controlled transistor. Switching threshold voltage of the domino gate is controlled by the voltage level of node N_2. Voltage level of node N_2 can be controlled with the size of PMOS pull up transistor. Due to the presence of resistive voltage divider this circuit consumes a large amount of DC power. It can be seen that, the voltage of the dynamic node cannot be less than the node N_2 voltage level, so there is no rail to rail voltage swing at node N_2. Gate output may also do not comprise a rail to rail swing if the PMOS pull-up transistor is large in size which actually raises noise immunity of the gate.

The method shown in Fig.2.16(c) is an improved method to control noise. In this method a feedback controlled pull-up transistor is employed in the circuit [81]. To make the internal node voltage high, an NMOS transistor is used. Gate of that transistor is connected to dynamic node of the logic circuit. When voltage of the dynamic node becomes low, the pull-up transistor becomes off; then, the dynamic node experiences rail to rail voltage swing. Similarly, up to some extent the DC power consumption is minimized. This happens only under some combinations of input which do not turn on PDN. In this technique, one PMOS transistor can also be used in similar way with a condition that gate of PMOS transistor should be connected to output.

A feedback NMOS transistor is employed in the mirror technique. This feedback transistor is employed in exactly similar way like the NMOS pull up technique [82]. This duplicates the PDN to decrease the power consumption and increase the noise tolerance performances. In Fig.2.16(d) a domino AND2 gate was designed with the above mentioned mirror technique. The mirror network is OFF whenever the pull down network goes OFF, which cuts off DC conducting path from the NMOS pull up transistor through the clocked transistor. In this manner, this circuit totally eliminates the DC power consumption. But, this mirror technique stretches the discharge path significantly in the PDN, this condition probably slows the circuit operation. This logic style sufficiently increases circuit active area which leads to increase the size of the circuit.



(a)



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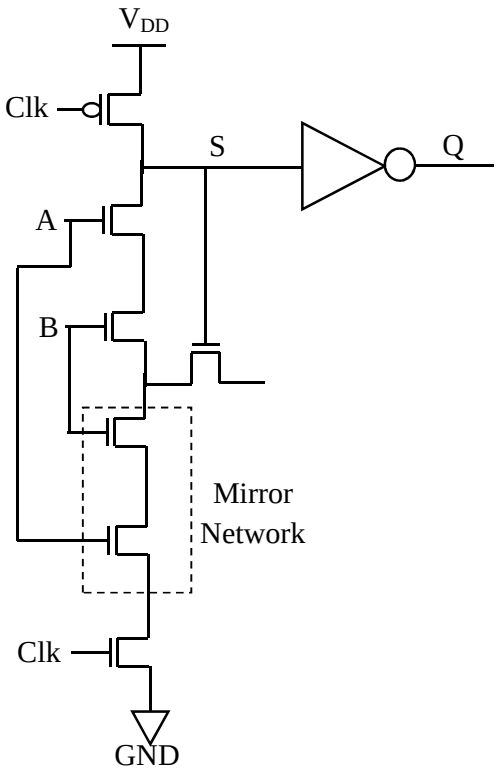

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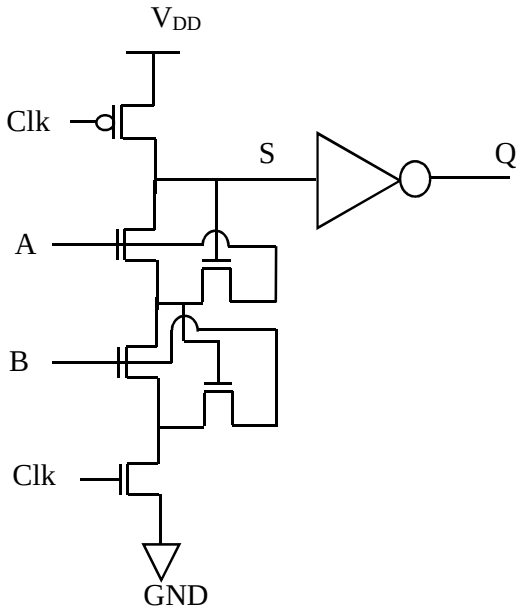
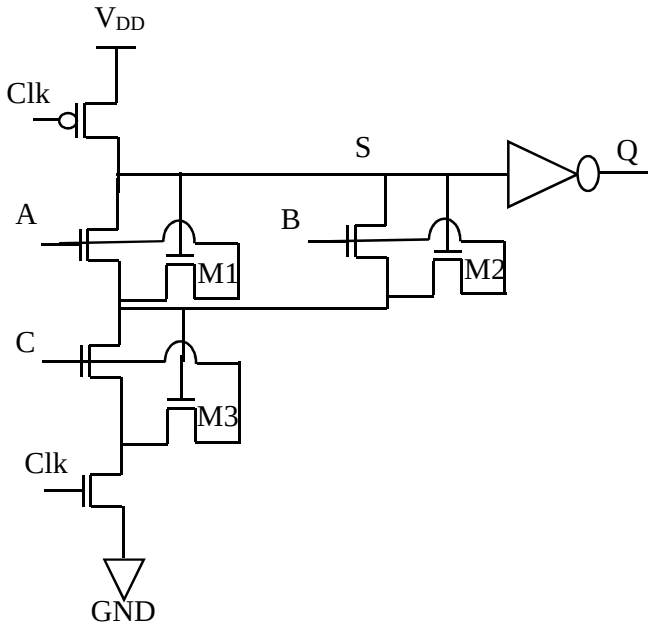


(d)

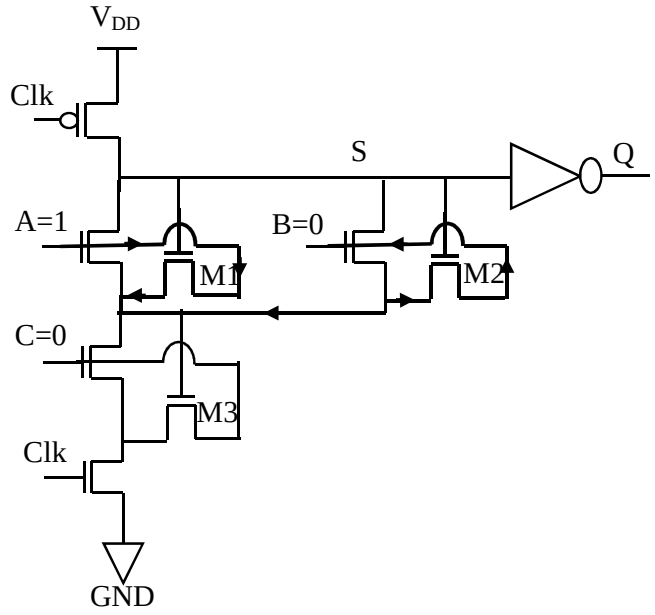
Fig.2.16 Raising source voltage of AND2 gate, (a) PMOS pull up technique [80], (b) NMOS pull up technique with feedback [81], (c) Mirror technique [82], (d) Twin transistor technique [83]

The twin transistor technique [83] [84] is a method to raise the source voltage of the dynamic gate. This technique contains a NMOS pull up transistor at each internal node for improvement of noise immunity of dynamic logic. Furthermore, the drain of each of the NMOS pull up transistor is connected to input in place of V_{DD}, as explained in

Fig.2.16(d). This activity avoids the unnecessary addition of current by the pull up transistor, which results in less power consumption. Conversely, this technique increases input capacitance of gate which leads to slow down the gate switching ability in further stages. Similarly, this technique is inappropriate for implementation of some logic functions. Fig.2.17(a) shows a 3 input gate, which is a mixed function of OR and AND gates. This circuit implements logic function F = {(A+B).C}. Let's assume inputs B and C are low while input A is high. As C is low, dynamic node remains at high logic level. At that time, no discharge path exists between the dynamic node and ground. In this condition, a conducting path present between the input B and input A, as depicted in Fig.2.17(b). At this instant of time, the logic levels at node A or B become uncertain.



(a)



(b)

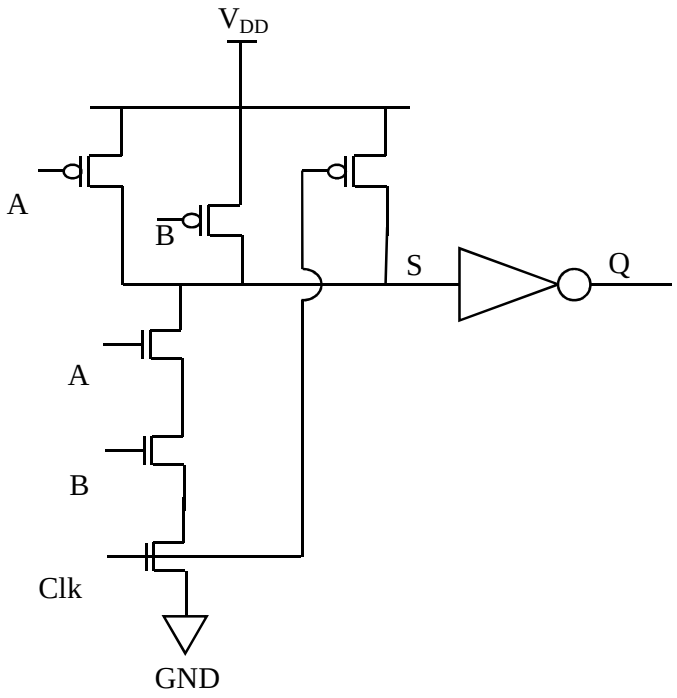
Fig.2.17 Twin transistor technique with short circuit problem, (a) A OR-AND gate, (b) OR-AND gate showing direct conducting path

2.4.4 COMPLEMENTARY P-NETWORK

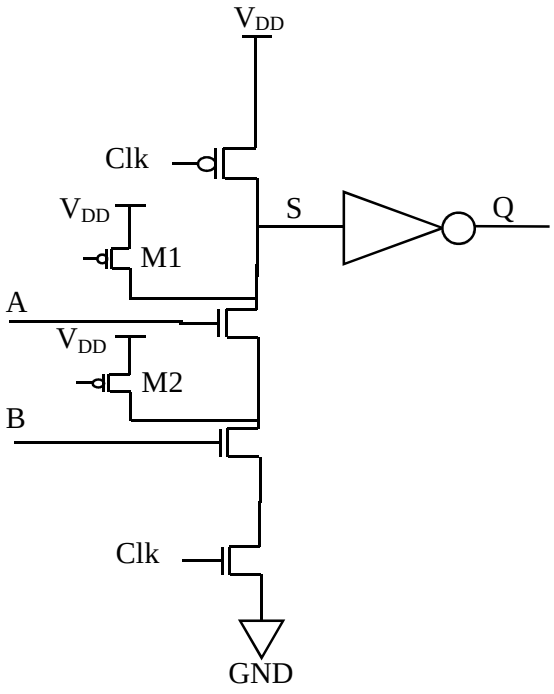
This complementary PMOS technique consists of a weak PMOS network, which can avoid the dynamic node to float in evaluation phase. This technique [85] [86] is shown in Fig.2.18(a). This gate functions similarly like basic domino gate at precharge period. When evaluation period starts, this circuit performs as a skewed CMOS logic. This circuit technique also has a silicon area overhead. The key drawback of this technique is it is quite ineffective in implementing in large logic gates. In case of high fan-in OR gates, the dynamic logic styles performs better than the static logic gates in its performance.

In CMOS inverter technique the complementary PMOS transistor can be implemented at transistor level, which is depicted in Fig.2.18(b) [87]. Here, the relative size of PMOS transistor was varied to adjust the threshold voltage of the logic gate. A vital benefit of this technique is that this technique can be applied selectively to some of the inputs if we found that subset of inputs to be noisy. The vital disadvantage of this technique is that, because of serious dc current, it is not appropriate for OR gates below certain input combinations. Also let's use this circuit for simple 3 input AND– OR logic. Let, input B is low and input A and C are high, a direct conducting path present between V_{DD} and GND, as depicted in Fig.2.18(b). Voltage level of the dynamic node is determined by the relative strength of the pull up transistor M_2 and that of the discharging path transistors. So this circuit is more hazardous than the previous one. The logic style fails switching when this pull up transistor is strong enough for recovering gate noise tolerance.

In both of the above two techniques, dynamic node can be reset falsely in some combinations of input. In Fig.2.18(b), let, input A becomes ON and input B comes from ON to OFF state in the evaluation phase, at that time, dynamic node may be go high by the pull up PMOS transistor. To solve this type of wrong reset problem, scientists in [88] used an extra transistor M_3, presented in Fig.2.18(c). M_3 becomes ON, when the gate output remains low. In evaluation phase the output goes high at that time, transistor M_3 is turns off, which detaches the pull up transistors from the V_{DD}. Similarly complementary p-network technique can also be improved. It can be seen that this this technique could not resolve the dc conduction problem for the logic circuits completely.



(a)



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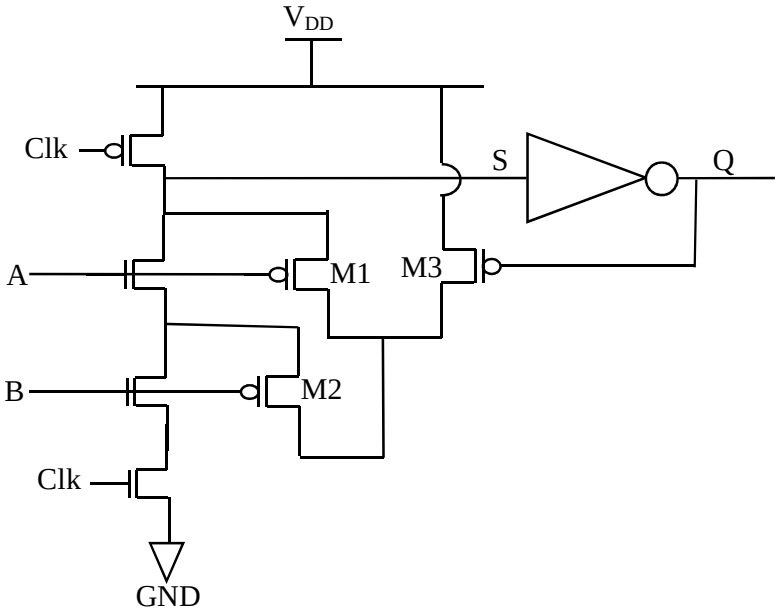
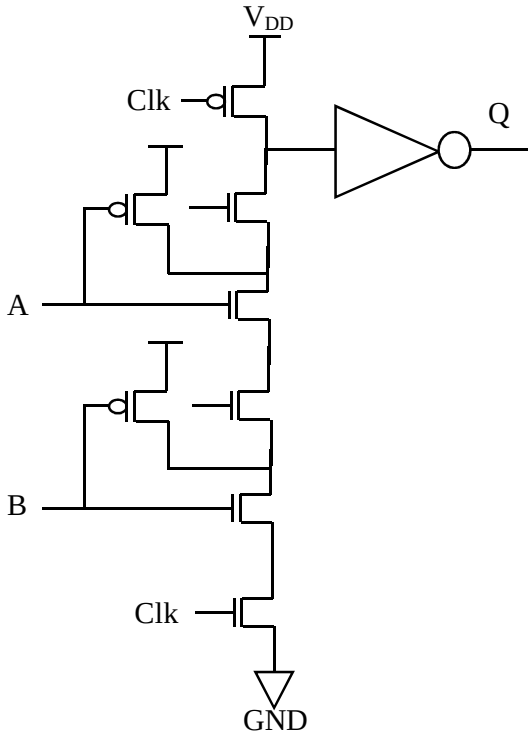
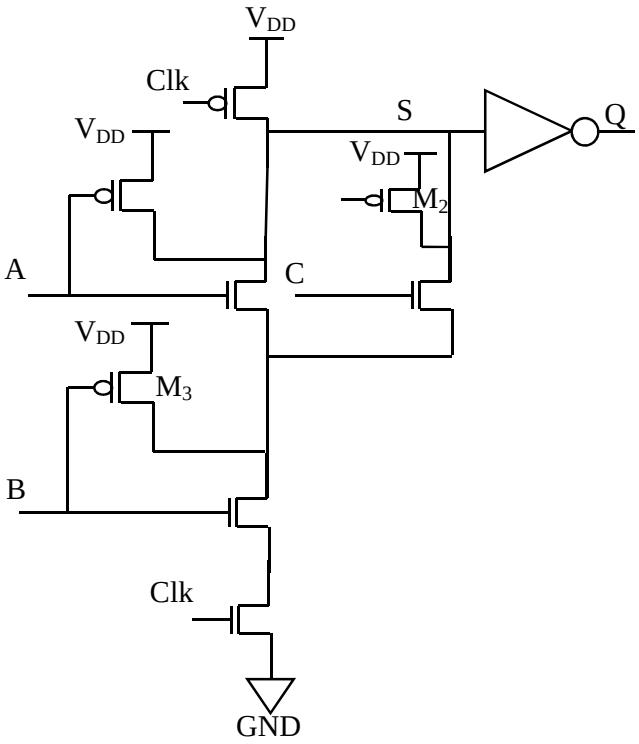


(c)

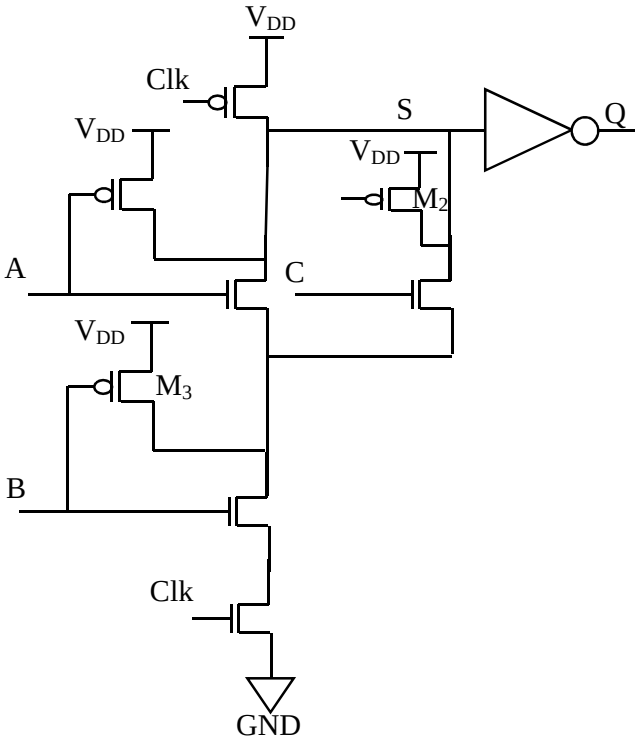


(d)

Fig.2.18 Constructing complementary PMOS networks for AND2 gate, (a) Construction of complementary PMOS network technique [85], (b) CMOS inverter technique [87], (c) Gated CMOS inverter technique [88], (d) Triple transistor technique [89]



(a)



(b)

Fig.2.19 Short circuit problems in inverter technique, (a) A 3-input OR-AND gate, (b) Direct conducting path

A new noise tolerant AND2 gate designed with triple transistor technique [89] is depicted in Fig.2.18(d). In this technique, each of the NMOS transistors in PDN of a basic dynamic logic is substituted by three numbers of transistors. This technique is considered as a variation of the CMOS inverter technique. In this method, in the evaluation network an extra NMOS transistor is added to control the power dissipation through the DC conducting path. This technique significantly increases discharge paths of PDN, like mirror technique. This logic performs well for wide logic gates. This circuit cannot be applied universally because of its large size and performance.

2.5 OTHER MODIFICATIONS

2.5.1 SFEG (SOURCE FOLLOWING EVALUATION GATE) TECHNIQUE

Source following evaluation gate technique is also called as SFEG technique, which is demonstrated in [90] [91] [92], and shown in Fig.2.20. The basic idea of this technique is, implementation of the logic functions by means of an NMOS PUN, noise immunity of the gate increases. Leakage currents which flow through evaluation network charges the dynamic node A. This results in reducing V_{GS} of the NMOS transistors. This reduces V_{GS} reduces the leakage current of the circuit exponentially. Additionally, the critical node leakage current (I_{LEAK}) is only because of the transistor M_4 in this technique because the critical node driving the final static inverter and the dynamic node are not the same nodes. A big demerit of this technique is that the NMOS PUN is unable to charge the dynamic node up to V_{DD} rather it can charge the dynamic node only up to $V_{DD}–V_{TH}$ during a switching of the gate. The pull up PMOS transistor M_2 compensates the threshold voltage drop. Though, Transistor M_2 gets ON with a delay of the feedback loop. Therefore, short circuit current flowing through the path M_4 and M_5 during the switching of the gate causes a lot of power dissipation.

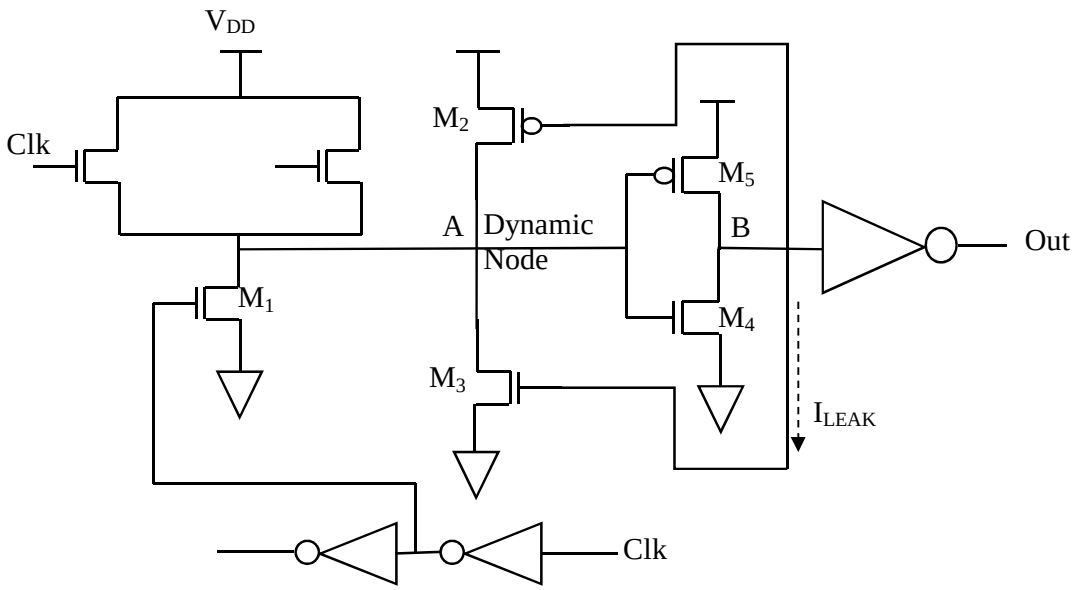


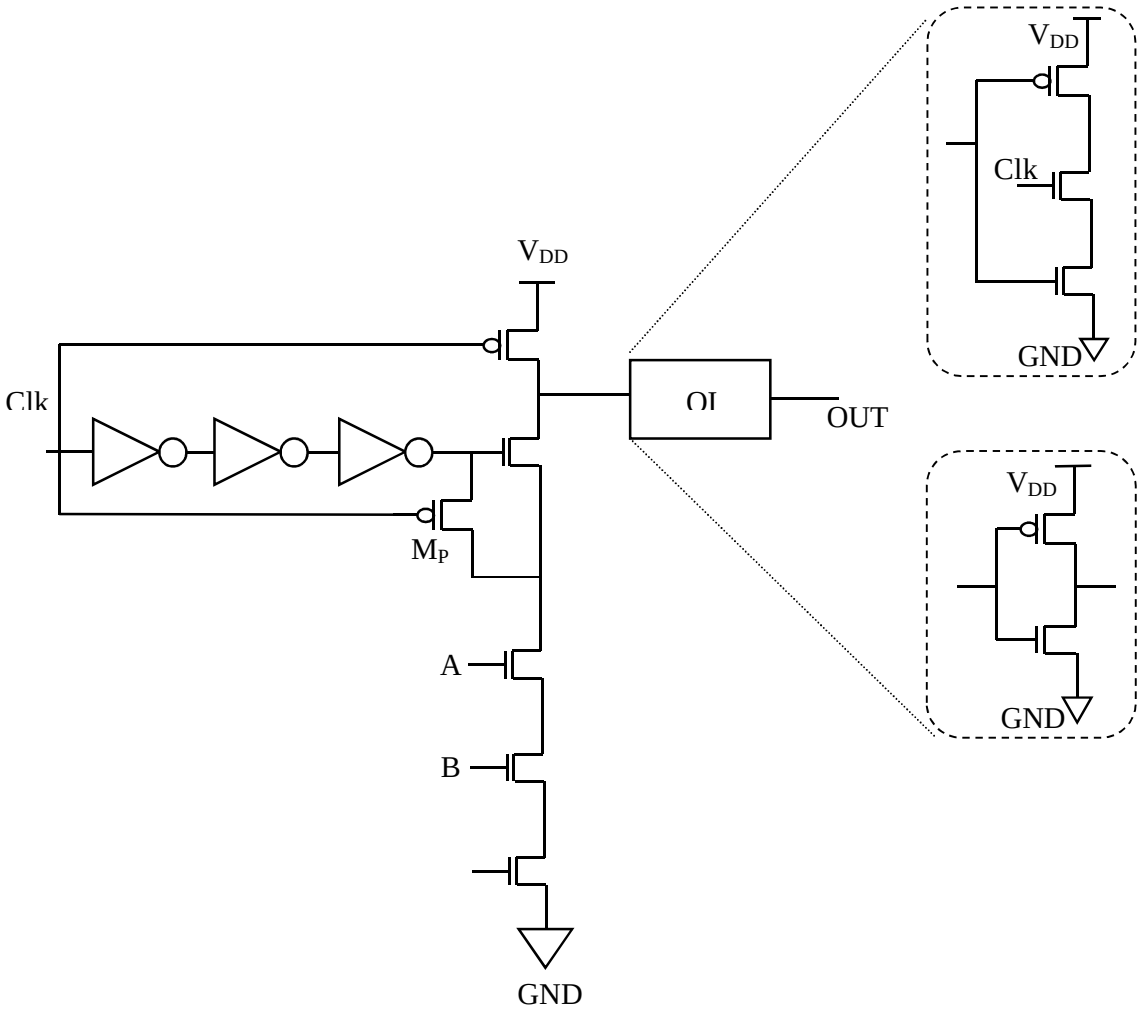
Fig.2.20 SFEG dynamic logic circuit design [91] [92]

2.5.2 MENDOZA'S DOMINO LOGIC

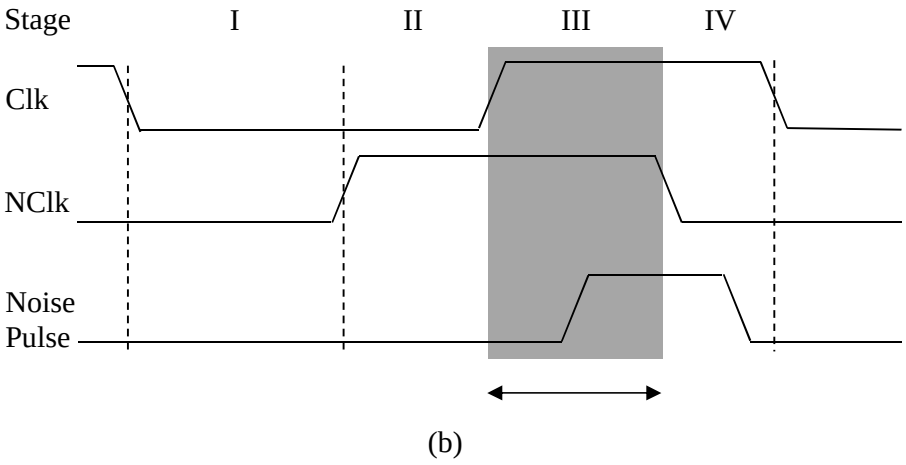
To increase the noise immunity of domino logic Mendoza in [93] depicted in Fig.2.21, inserted an NMOS transistor M_n between the precharge node P_1 and the PDN. A delay stage, which can be constructed with three cascaded static inverters, was used to locally generate the NCLK signal from the clock Clk, and a PMOS transistor M_p is added between node NCLK and node P_2. The inputs are not used to precharge any of internal nodes in the PDN. This phenomenon is advantageous as the capacitive loads at the input nodes stay the same. However, some drawback exists with area and propagation delay. Due to the presence of the inverters M_n and M_p the propagation delay is makes the circuit slower.

2.5.3 MODIFIED SFEG

To increase noise tolerance modified SFEG was proposed by Frustaci in [90] [94] as depicted in Fig.2.22. This scheme runs very much dissimilar from the SFEG technique in having large value of noise tolerance then the normal SFEG technique. This design is a trade-off between noise tolerance performance and power dissipation. A big drawback of this circuit is that, it is having NMOS-based PUN which also evaluates the logic gate; which exploits the principle of dynamic logic style. Its delay- UNG performances show below average results.



(a)



(b)

Fig.2.21 Two-input dynamic AND-gate implemented with noise-tolerant dynamic circuit method, (a) Gate can be domino [static output inverter (OI)] or TSPC (NC2MOS output inverter), (b) Timing diagram

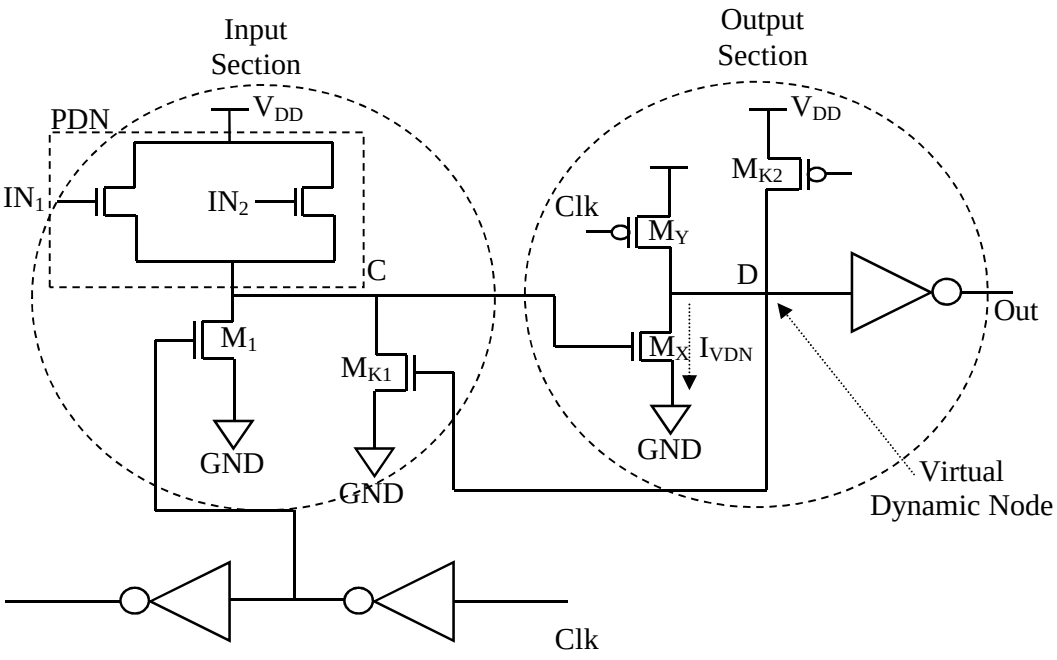


Fig.2.22 Modified SFEG circuit design

2.5.4 DIODE-FOOTED DOMINO

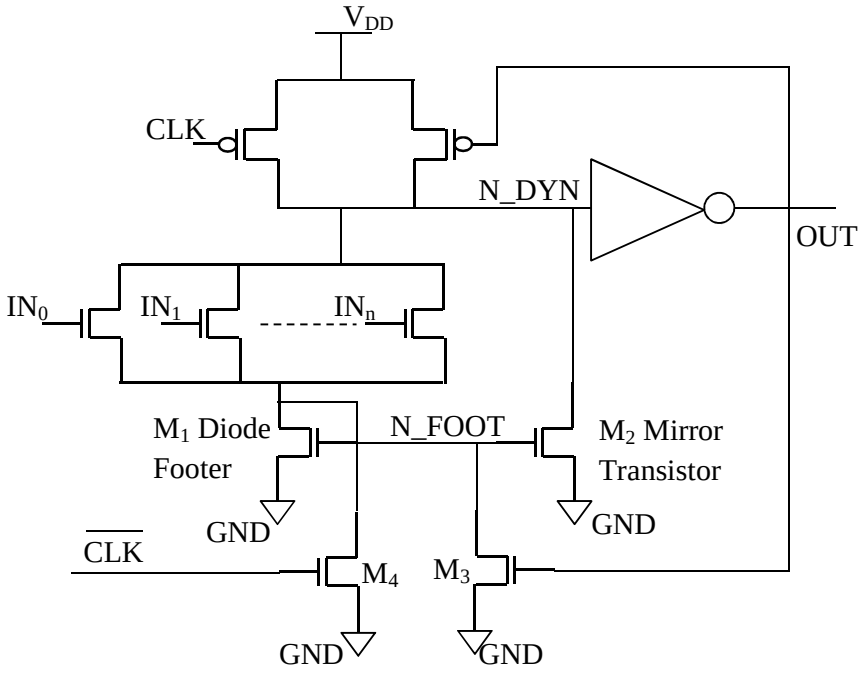


Fig. 2.23 Diode footed Domino [95]

In diode-footed domino [95] an NMOS transistor is there in a diode configuration i.e. gate and drain terminals connected together in series with the evaluation network, as shown in Fig. 2.23. A diode connected transistor is exploited in this design in which the leakage flowing through PDN in evaluation phase causes the voltage drop across the diode transistor. Which makes the V_{GS} negative and leakage reduces. The performance degradation can be compromised by the mirror network. By varying the size of mirror, noise immunity can be made. But when we compare it with standard footless domino this scheme is very slower. Also the inverse clock increases the capacitive load of the clock driver.

2.6 CONCLUSION

Static CMOS performs very well in terms of robustness and energy, but is not good in terms of delay. Domino CMOS logic performs very well in terms of delay, but is not good in terms of robustness and energy. A slight noise present in the input of the domino logic modifies the output logic level. In domino logic style present a static CMOS inverter at the output of the dynamic node. Due to this, noise immunity of the circuit increases and capacitance at the output node reduces. In this thesis, as we proceed further, we have proposed a novel circuit technique for domino logic. This circuit technique is more noise robust, has very less power dissipation and operates with high speed as compared to the previous reported logic styles. The new proposed logic is also compared with the previous proposed ones to show its enhancements and advantages.

Chapter 3

PROPOSED DOMINO LOGIC

3.1 INTRODUCTION

The fast improvement of VLSI CMOS circuit technique is due to the wireless systems with low power budgets and increased use of small sized gadgets and very high speed processors. To attain this requirement, the supply voltages and size of transistors are scaled with technology. Due to larger number of devices per chip, the interconnection density increases. The interconnection density along with high clock frequency increases capacitive coupling of the circuit [96]. Therefore, the noise pulses are generated leading to logic failure and delay of the circuit [96]. Again, when supply voltage is scaled, the threshold voltage of the device needs to be scaled to preserve the circuit performance, which leads to increase in the leakage current of the device.

Due to low device count and high speed especially compared to complementary CMOS, dynamic-logic circuits are broadly used in a wide range of applications including dynamic memory, digital signal processors and microprocessors [97]. Dynamic circuit contains a pull-down network which realizes our desired logic functions. According to the basic dynamic circuit operation, the dynamic node precharges at every clock cycle. As the clock signal frequency is high, the circuit generates a lot of noise which consumes extra power and slows the circuit.

In this thesis, we have proposed a novel circuit method which can reduce the noise of dynamic logic dramatically. This circuit increases speed and decreases the power dissipation of the circuit as compared to other existing domino logic styles in the literature.

3.2 BASIC DOMINO GATE

Fig.3.1 is an example of footless domino gate. In precharge period when the clock remains at LOW, precharging PMOS gets ON, at that time dynamic node is connected to V_{DD} and gets precharged to V_{DD}. When clock goes high, the evaluation phase starts.The output gets evaluated with the pull-down network and conditionally gets discharged if the PDN is conducting. During evaluation period when the PDN is not conducting, the dynamic node should be at logic 1. But due to subthreshold leakage, the high fan-in NMOS PDN leaks the stored charge present in the capacitance of the dynamic node. This lost charge is usually compensated by PMOS keeper, which targets to recover the voltage level of the dynamic node. However, when an impulse of noise occurs at gate input, the keeper may not always be able to recover the voltage level of the dynamic node. The subthreshold leakage current is exponentially dependent on V_{GS}. So, in the presence of noise impulse, the gate voltage increases and the dynamic node gets wrongly discharged.

As compared to the static CMOS logic gates, domino gates have higher noise sensitivity because of its low switching threshold voltage. The switching threshold voltage is equal to the V_{TH} of the pull-down NMOS devices [98]. In the design of high fan-in gates, noise immunity has become a great concern. This is because of the high number of transistors and circuit branches, which cause more possible paths for gate and sub-threshold leakage currents.

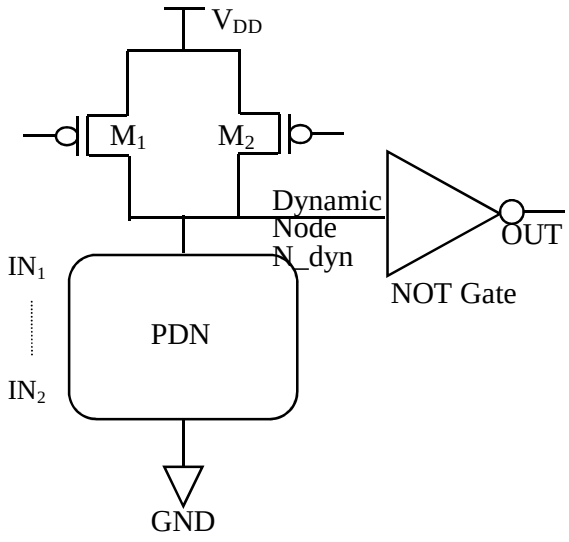


Fig.3.1 A typical footless Domino gate

Noise of domino gates is now more important than the area, delay and power dissipation issues, therefore various techniques have been proposed [95] [90] recently to reduce the noise of dynamic circuits. Besides noise sensitivity in domino logic, there are also many other issues with area, power dissipation and delay.

3.3 PROBLEM DESCRIPTION IN DOMINO LOGIC

The schematic of a basic footed domino logic circuit with a traditional buffer is depicted in Fig.3.2 [99]. The logic function implemented in the circuit is 'Out = (A + B) C + A B'. According to basic operation of classical domino logic, the logic level of node 'a' should always be held as 'High', when the PDN is non-conducting. In domino logic, has two operation phases: 1) precharge and 2) evaluation.

1) Precharge phase:- In the precharge period, when the Clk signal is LOW, at that time the NMOS clock transistor remains in OFF state and the PMOS clock transistor remains ON. Therefore, the dynamic node i.e. node 'a' will be charged to '1' irrespective of the logic state of the PDN. If the pull down network is conducting, the N_FOOT i.e. node 'b' will also be 'High' along with node 'a'.

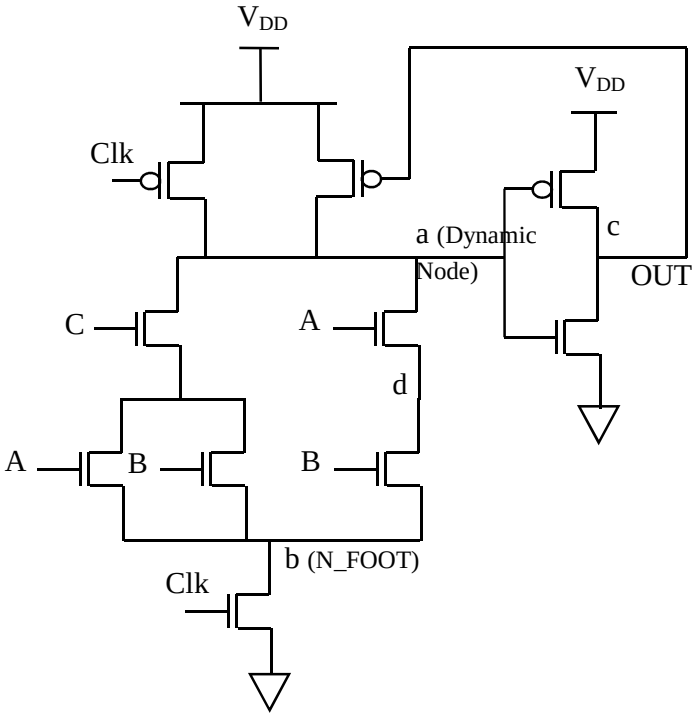
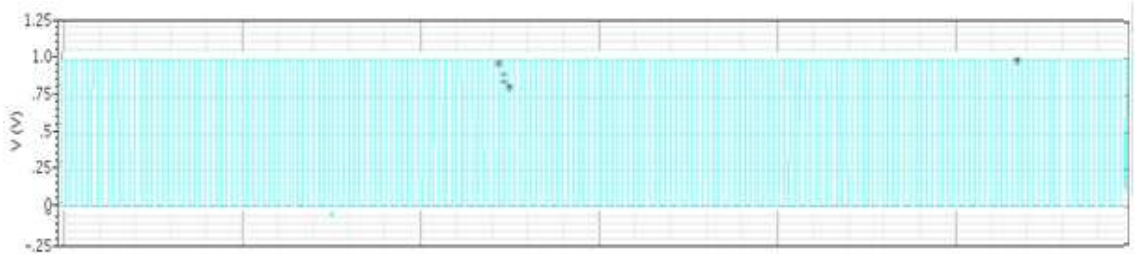
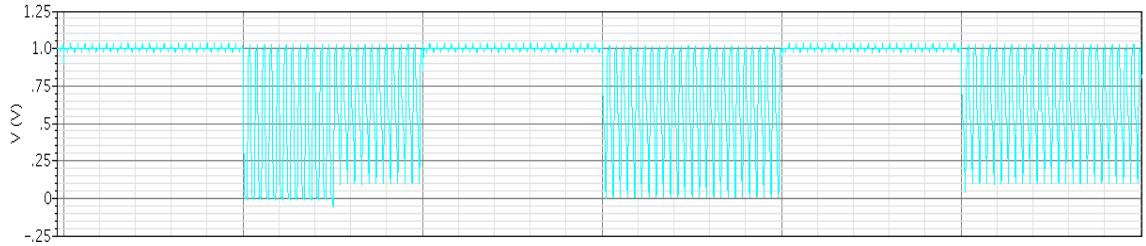


Fig.3.2 Logic function realized with conventional domino logic

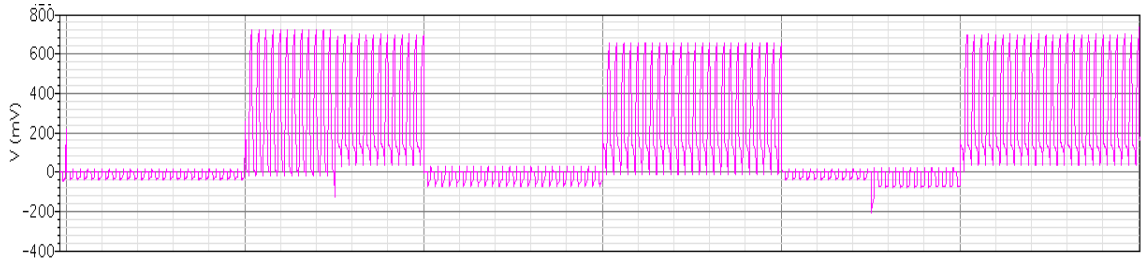
2) Evaluation Phase:- Evaluation phase of domino logic is more complicated than the precharge period. During the evaluation period, as the Clk is ON, the PMOS precharge transistor is OFF disconnecting the dynamic node from V_{DD}. On the other hand, the gate of NMOS stacking transistor is at 'high'. So the node 'b' will be shorted to ground. As a result, if the pull-down network is on, the node 'a' will also be discharged and the logic level of 'a' will decrease to 'LOW' as shown in Fig.3.3 (a, b, c).



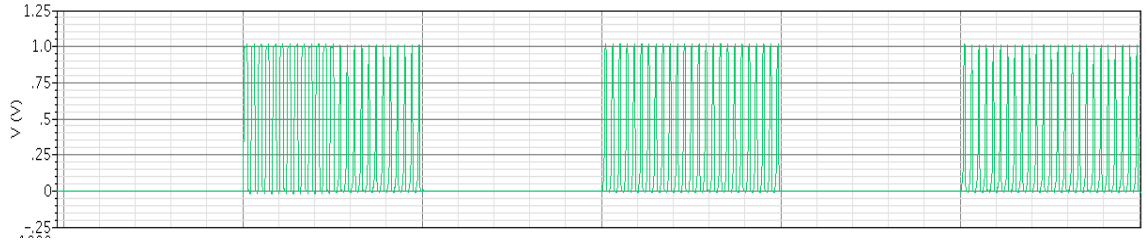
(a) Clock (Clk)



(b) Node 'a'



(c) Node 'b'



(d) Node 'c'

Fig.3.3 Output waveforms of Clk and node a, b, c for the circuit described in Fig.3.2

According to the theory, the output i.e. node 'c' is only the inverted waveform of the dynamic node i.e. node 'a' as shown in Fig.3.3. During precharge period, the NMOS transistor of the buffer will be turned OFF for sure. In the evaluation it turns ON conditionally. The turning ON of NMOS of the buffer depends on the combination logic functions and input values.

To describe clearly, a simulation was done taking Z function as vehicle. Where Z = ((A + B) . C + A . B). This simulation was done using cadence specter 180 nm technology with a clock frequency of 500 MHz and a temperature of 27^0 C. When ((A + B) C + A . B) equals to 'Low', node 'a' i.e. the dynamic node should be at 'High'. However, conventional domino logic, there are many pulses in the dynamic node 'a' as a result of the precharge process as shown in (b). Fig.3.3 (a) shows the Clk input with a frequency of 500 MHz. As the Clk switches frequently, the 'High' level of node 'a' also switches frequently with Clk. Because of the presence of pulses at the dynamic node, output node 'c' also comprise of several pulses as shown in Fig. 3(d).

These pulses are not expected in the output node of a CMOS domino logic circuit, so it will cause various problems:

1) Pulses can change the logic level of output - As a result of the presence of many pulses at the output, the output always changes and remains at 1 for very less time. These pulses only add noise to the domino logic circuit.

2) The power consumption of the circuit increases - If input logic is on because of the pulse, the number of switching operation of the buffer in evaluation phase will be as frequent as the clock signal. Therefore a high current will flow through the buffer, this process results in increase in power consumption of the circuit. For each switching, Power Consumption = V_{DD}*I, where, V_{DD} denotes the supply voltage and I denotes short circuit current flowing through the buffer from V_{DD} to GND.

Recently, several researchers have proposed several techniques to reduce the noise, delay and power of wide fan-in domino gates [3] [95] [90] [100] [101] [102] [103] [104] [105] [106]. All the existing techniques try to improve the noise robustness of domino gates at a significant cost in terms of delay or energy consumption. Moreover, the degradation in speed and the increase in energy dissipation seem to become more and more troublesome.

As described above, the most vital problem of basic domino logic is the frequent switching output node due to precharge phase. While we can't stop the precharge phase of the domino logic, we can certainly minimize pulses at the output, thus we can improve the domino circuit in order to reduce noise and power consumption. In this thesis, we have made adopted a novel approach to mitigate this problem. The proposed approach also provides better performance in terms of power, delay, PDP, and noise tolerance at the cost of 2 extra footer transistors in the logic. This would increase the area of the circuit for low fan-in domino gates, but for higher fan-in domino logic based circuits, relative percentage of increase in area also reduces.

3.4 THE NOVEL APPROACH

3.4.1 CIRCUIT DESCRIPTION

In this section, we have presented a new scheme for the design of noise tolerant domino logic technique. This circuit contains a precharge transistor, an evaluation network, footer transistors and semi-dynamic inverter as depicted in Fig. 3.4. In the precharge period when the clock is LOW, the precharge PMOS gets ON and dynamic node is connected to V_{DD} and gets precharged to V_{DD}. When clock goes high, the evaluation phase starts and output gets evaluated with pull-down network that conditionally gets discharged if the PDN is ON. During evaluation period when all the inputs are at logic 0, the dynamic node stays at logic 1. However, in case of wide fan-in circuits, due to the subthreshold leakage PDN network leaks the charge stored in the capacitance at the dynamic node. When a noise voltage impulse occurs at gate input, voltage level of the dynamic node decreases resulting is change in output logic. To stop that, the footer transistors (M_2, M_3 and M_4) are connected. M_3 acts as stacking transistor. At the evaluation period, when the dynamic node should be discharged, at that time M_2 makes a charge discharge path.

In basic domino logic, the output pulses persist in the circuit, due to the precharge act. The pulses of output node N_FOOT always propagated because of turning on the NMOS transistor present in the buffer by precharge pulse in the dynamic node. Therefore it can be easily said that we can avoid the precharge pulse propagating to the output of the buffer, if we can turn off the NMOS transistor of the buffer during precharge. Following this method, this unique circuit technique is proposed.

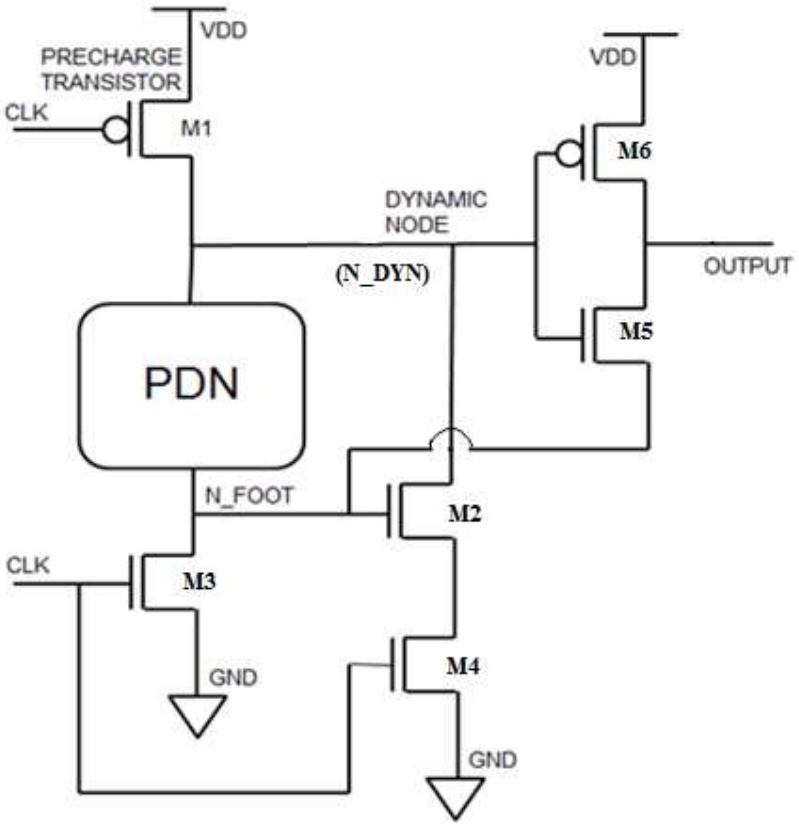


Fig. 3.4 Proposed Circuit

3.4.2 CIRCUIT ANALYSIS

The proposed novel domino circuit scheme is shown in Fig. 3.4. Transistor M_3 is used as stacking transistor. Due to voltage drop across M_3, gate-to-source voltage of the NMOS transistor in the PDN decreases (stacking effect [103]). The proposed circuit has additional evaluation transistor M_4 with gate connected to the CLK. When M_3 has voltage drop due to presence of noise-signals, M_2 starts leaking which causes a lot of power dissipation. This makes the circuit less noise robust. In proposed scheme, the transistor M_4 causes the stacking effect [107]; which makes gate-to-source voltage V_{GS} of M_2 smaller (M_3 less conducting). Hence circuit becomes more noise robust and less leakage power consuming.

(Stacking effect – The subthreshold leakage current which flows through the stack of series-connected transistors reduces, when many transistors in the stack are turned off. This effect is called as the stacking effect.)

We now connect the source of the M_5 to drain of the NMOS clock transistor (N_FOOT) in place of ground. When a dynamic circuit is followed by a buffer, it is called

domino logic. This proposed approach is a novel modification of domino logic, where the source of NMOS of the buffer is not connected to GND rather it is connected to the N_FOOT. This state of circuit is referred as 'semi-domino' state.

Fig.3.5 depicts the simulated waveform of proposed circuit showing wave form of the input, output, clock, N_DYN node, N_FOOT node simulated at 1 Volt, 500 MHz frequency and at 27^0 C using cadence specter. This simulation waveform illustrates the waveform when the circuit enters to evaluation period. In the evaluation period of the circuit conditionally when any one input of the OR gate goes high, the dynamic node i.e. N_DYN starts discharging. When N_DYN discharges to 0, due to the presence of the buffer, the output goes high. There is a small delay between the discharging of N_DYN and the charging of output node.

The Fig.3.5 presents the Clk, input (A), N_DYN, N_FOOT and output (Out) waveforms. This shows that, the logic operates similar to the basic domino logic, although it is in semi-domino state and having 2 numbers of extra transistors.

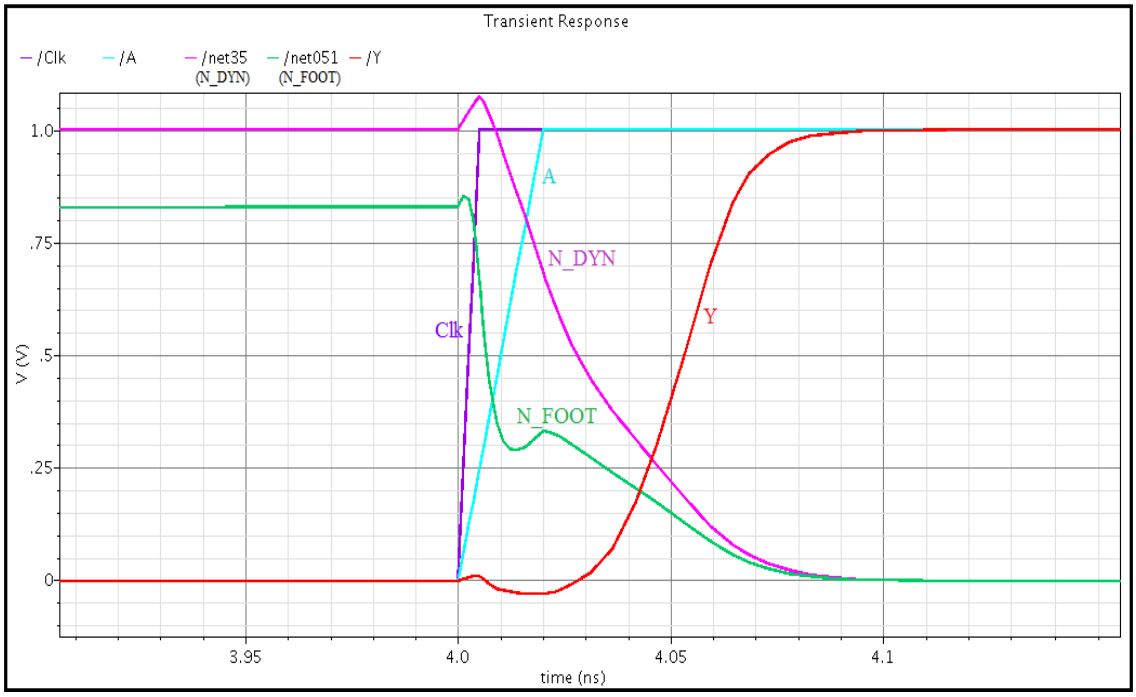


Fig.3.5 Simulated waveform of proposed scheme

3.4.3 NOISE ANALYSIS

When PDN is OFF and the N_DYN is at high voltage, at that time the N_FOOT stays at low voltage. Due to the high voltage level of dynamic node, the gate of the NMOS (M_5) goes high and the low level of N_FOOT makes the source of the M_5 to 0. This makes M_5 ON and voltage of buffer output becomes same as the voltage of N_FOOT. It can be easily verified that if the NMOS transistor of buffer can be turned off permanently, by doing this, the pulses propagating to the output can be avoided [101].

In the evaluation period, when the NMOS M_3 is ON, N_FOOT gets discharged to 0. When PDN is ON the N_DYN also gets discharged to ground. This makes the V_{GS} of buffer NMOS M_5 to 0 as $V_{GS}=V_G-V_S=0$. This results in switching OFF the NMOS and the buffer output gets completely charged through PMOS M_6.

In precharge the dynamic node will get charged to high, when PDN is ON the voltage of the N_FOOT is nearly same as N_DYN, as the NMOS M_3 is OFF. The V_{GS} of the buffer NMOS will be $V_G - V_S < V_{TH}$ which keeps the NMOS of the buffer at turned OFF stage. The PMOS of the buffer is also OFF due to the high level of N_DYN node. This makes the output of buffer LOW.

3.4.4 POWER ANALYSIS

The proposed structure uses semi-domino buffer structure. So the output node OUT has no pulses in precharge stage as shown in Fig.3.6. In the figure the first waveform shows the clock the second and third wave form shows the waveform of the 2 input signals namely A and B. The 4^{th} waveform shows the output plotted for the basic domino gate. The 5^{th} and 6^{th} waveform shows the outputs of the two reference circuit structures. The last or the 7^{th} waveform shows the output of the proposed circuit.

It can be seen that the 4, 5 and 6 waveforms i.e. the output of the reference circuits contains the pulses in the ON stage, but the proposed output does not contain such pulses, which means that the buffer does not get on and off frequently, therefore current through the buffer reduced sufficiently then the counterpart.

As demonstrated before, the buffer is operating on and off as frequently as the clock single as there are many pulses in the conventional structure. So the current through the buffer will also be large, which is consistent with the current curve simulation.

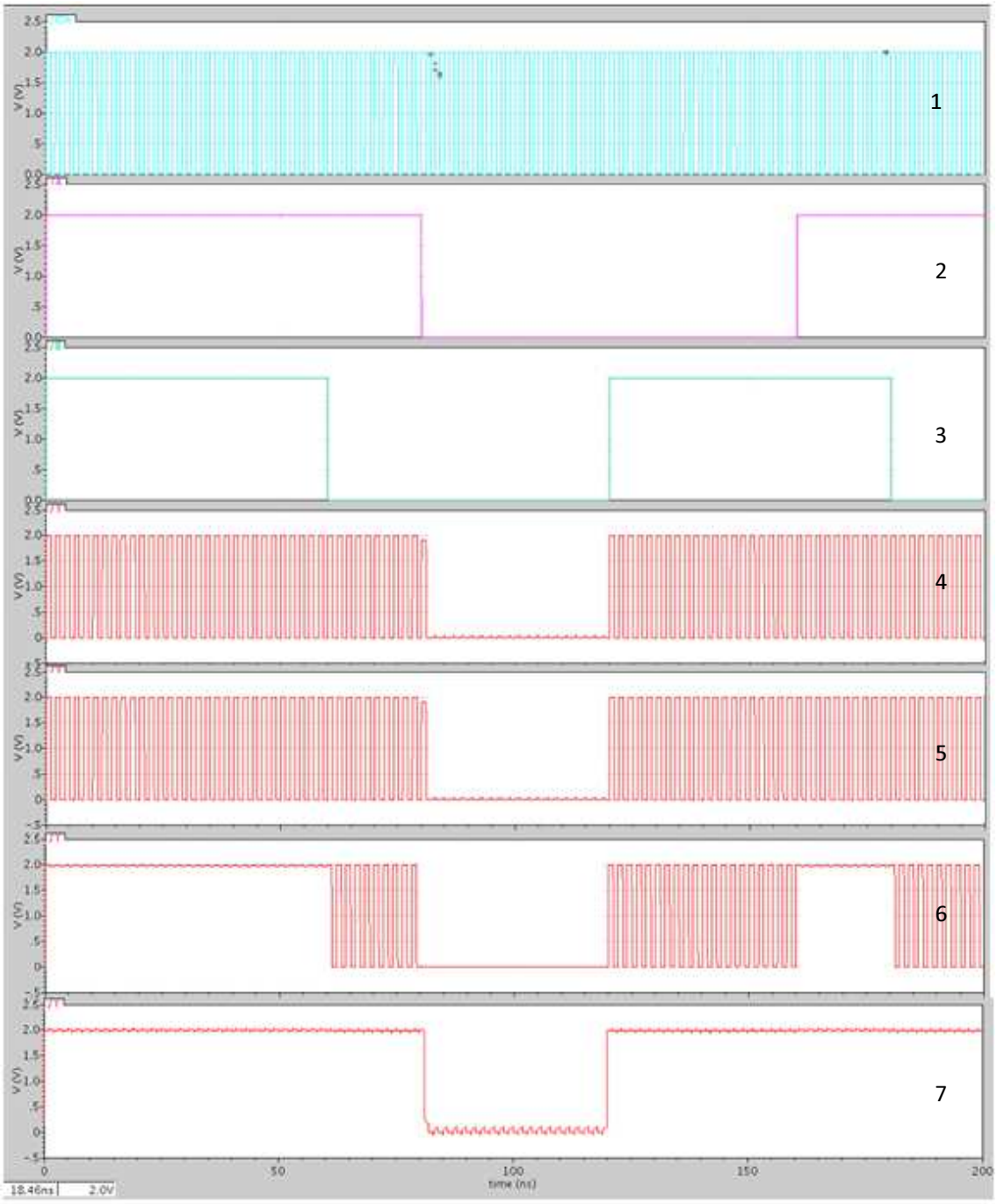
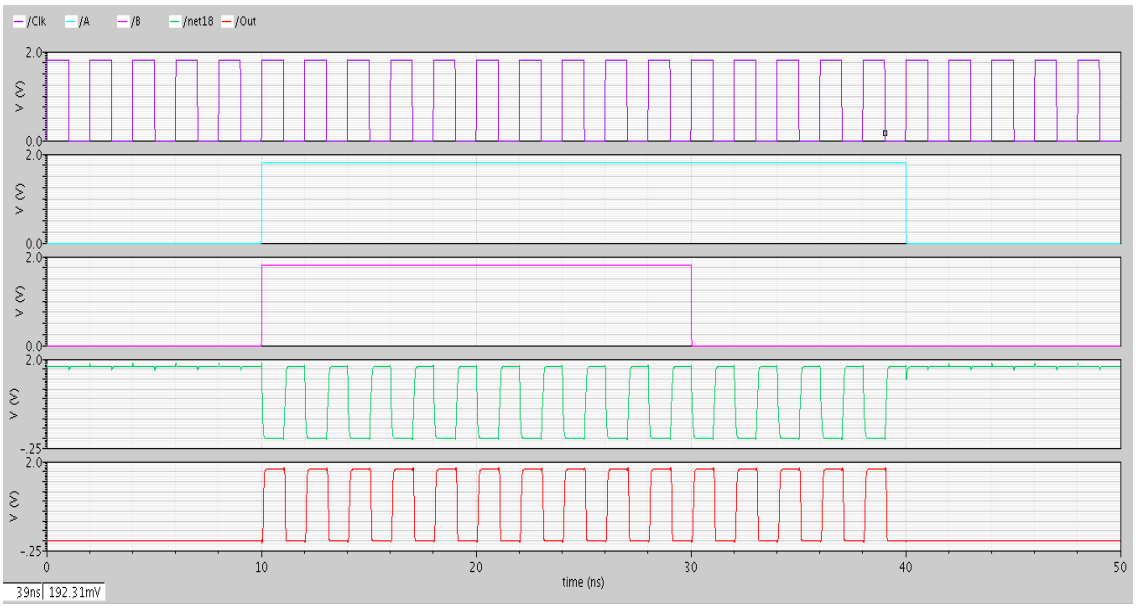
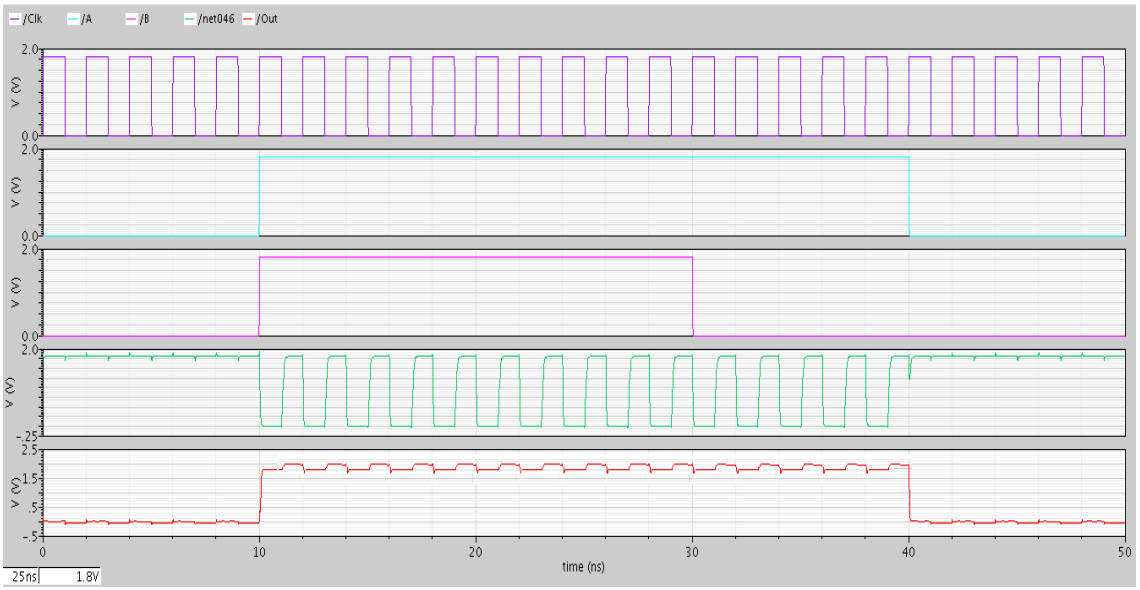


Fig.3.6 Waveform simulated for OR gate

1. Clock Input
2. Input A
3. Input B
4. Output for basic circuit
5. Output for [95]
6. Output for [90]
7. Output for Proposed circuit



(a)



(b)

Fig. 3.7 Waveform simulated for OR gate

(a) basic footed domino
(b) Proposed domino

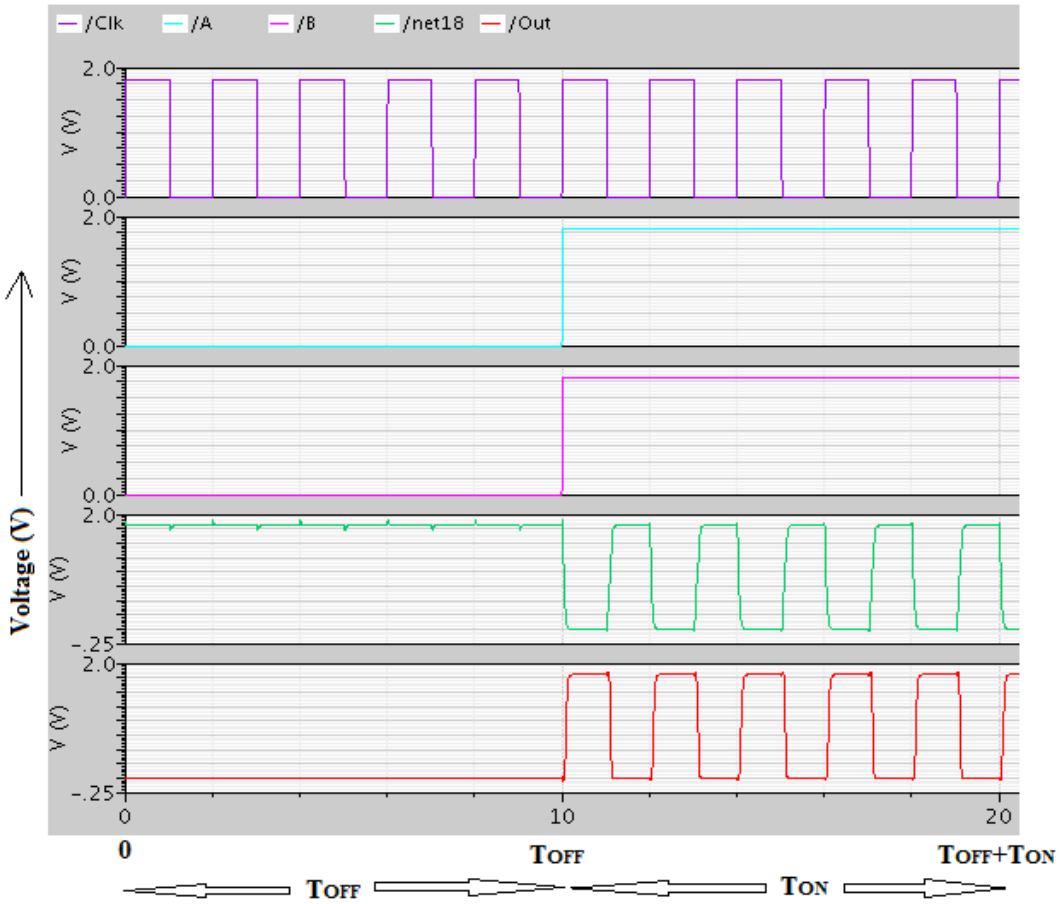
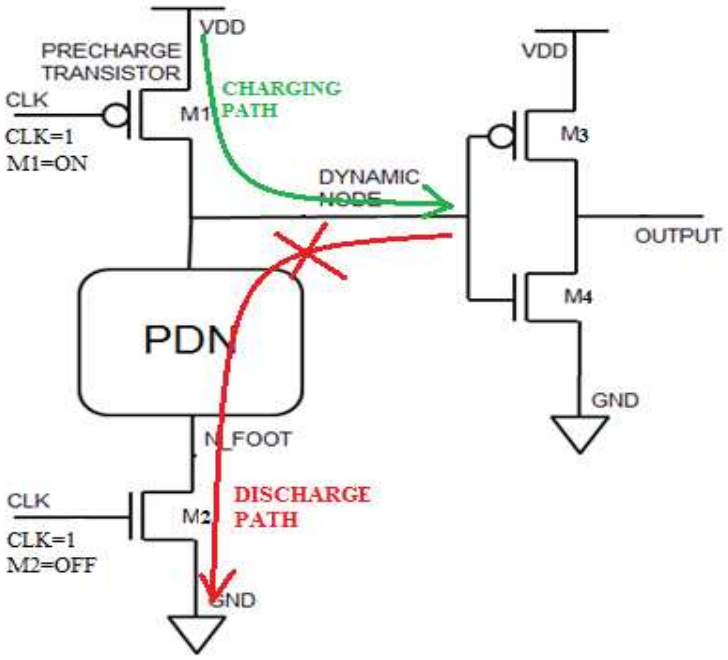
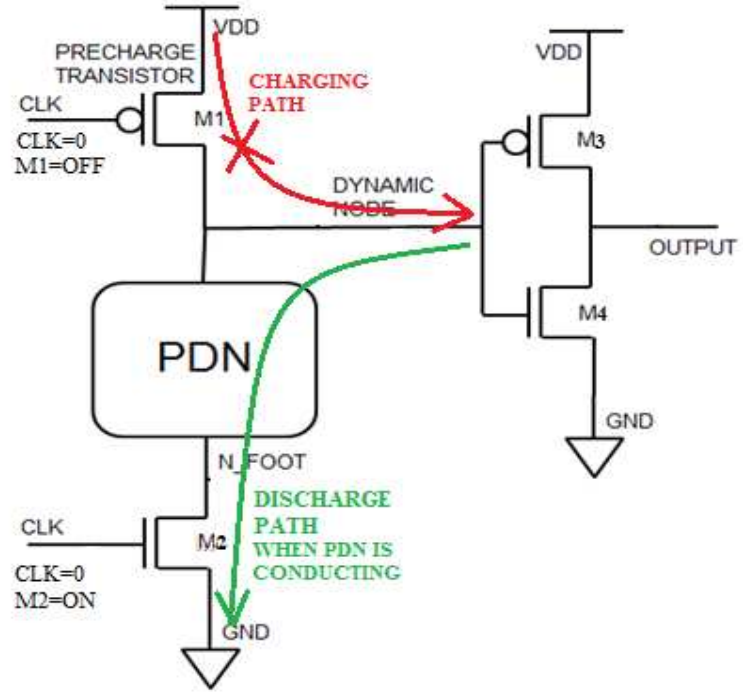


Fig. 3.8 Waveform simulated for the basic OR gate demonstrating T_{OFF} and T_{ON}



(a)



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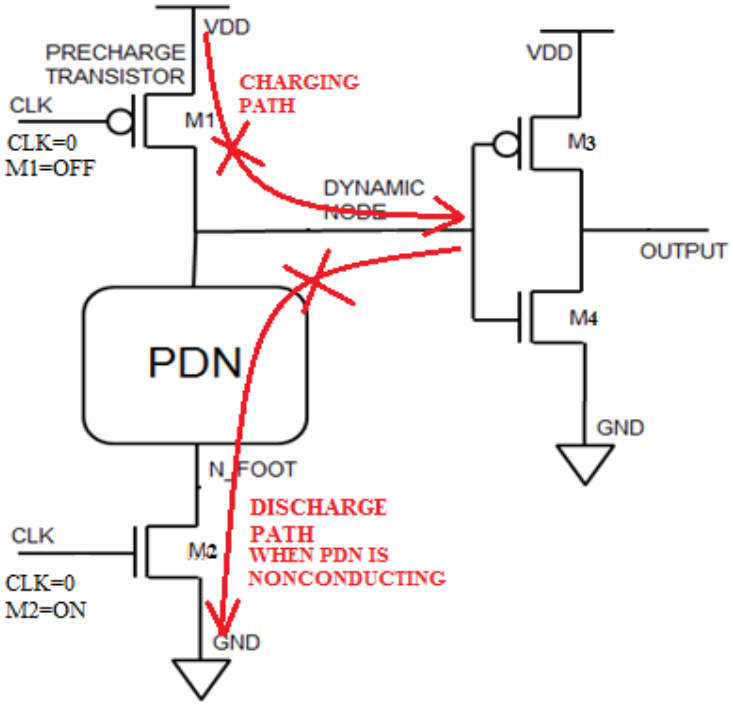


(c)

Fig. 3.9 Domino logic circuits showing charging and dis-charging paths (a) precharging stage (b) evaluation stage when PDN is conducting (c) evaluation stage when PDN is non conducting

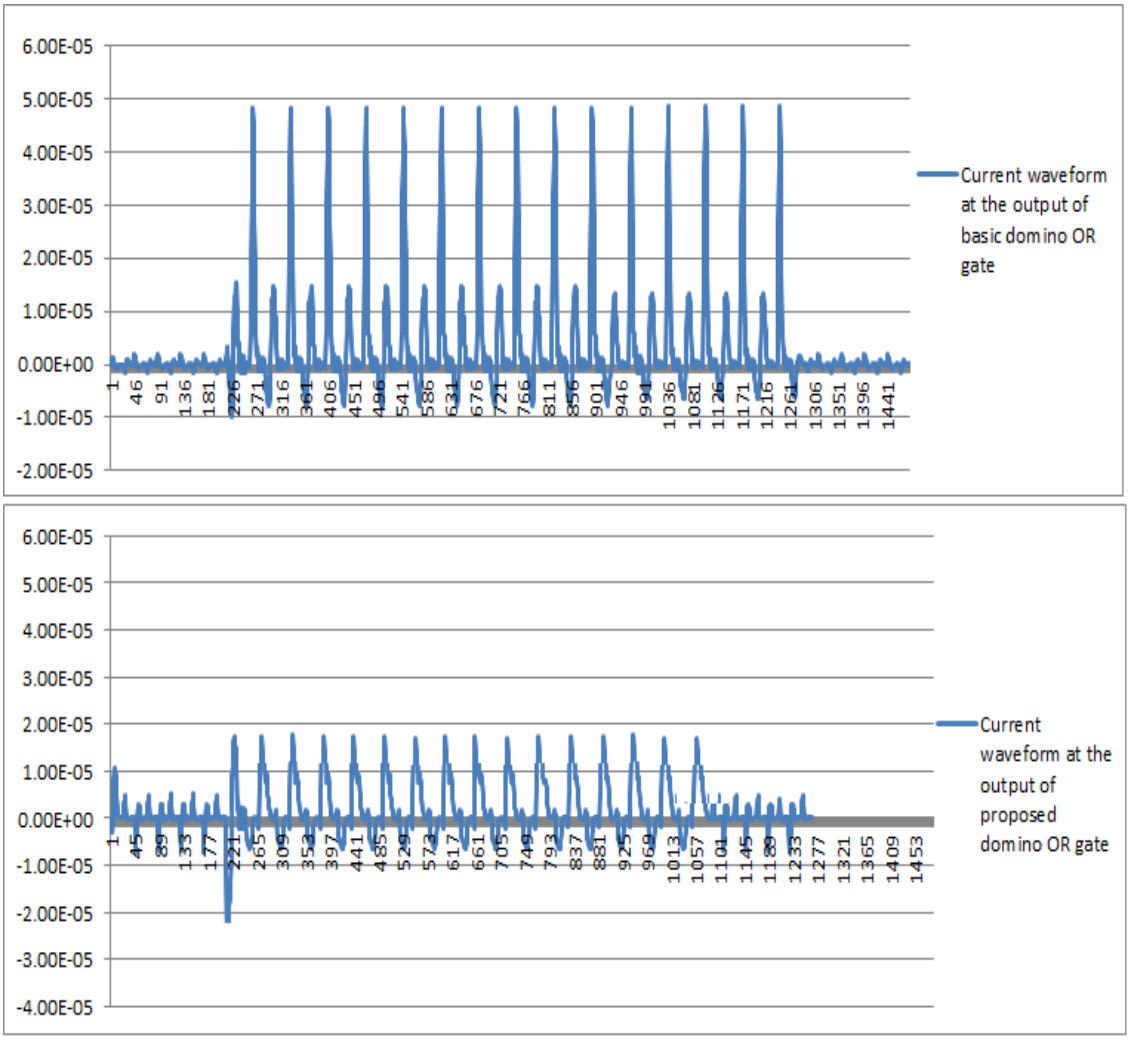


Fig. 3.10 Current waveform simulated for 2-input OR gate

Fig. 3.7 shows the simulated waveforms clearly, where Fig. 3.7 (a) shows the waveforms for the 2-input OR gate designed with basic footed domino logic and Fig. 3.7 (b) shows the waveforms for the 2-input OR gate designed with the proposed logic. Both the figures Fig. 3.7 (a) and (b) show five waveforms each i.e. Clk, input A, input B, waveform at N_DYN and waveform at output node respectively from top to bottom. It can be clearly seen that in basic OR gate the dynamic node and the output contain a lot of pulses, which come with the switching of the Clk input. On the other hand, the output waveform of the proposed logic does not switch frequently with the precharge pulse. So the current flow through the buffer of the proposed circuit is very less as compared to the current flow through the buffer of basic domino. Fig. 3.8 shows the waveform simulated for the basic OR gate demonstrating T_{OFF} and T_{ON}.

In this section, we have calculated the power saved by the proposed logic in comparison with the basic domino logic. The domino logic circuit family only consumes dynamic power. In ideal condition, no static current path ever exists between V_{DD} and GND as depicted in Fig. 3.9 (a). In precharge stage, when Clk is low, PMOS M_1 gets ON and the dynamic node charges through V_{DD}, but at that time the NMOS M_2 is OFF. This results the discharging path to be in OFF state.

In the evaluation phase, when Clk is high, NMOS M_2 gets ON and the dynamic node discharges through GND, if the PDN is ON as shown in Fig. 3.9 (b). This state results discharge path to conduct from dynamic node to GND. On the other hand as the as the Clk is high PMOS M1 is OFF, by which no static current path can be established between V_{DD} to GND. At the evaluation phase when the PDN is ON, there is neither charging path nor discharging path present in the circuit.

This proves that in domino logic circuit family there is no static power consumption in the circuit. It only consumes dynamic power. In ideal condition, no static current path ever exists between V_{DD} and GND.

To find power consumption of the ideal basic domino logic circuit, we can neglect the static power consumption in the circuit i.e. power consumption at T_{ON} and T_{OFF}. As a result only we have to find out the switching power consumption i.e. dynamic power of the circuit.

Domino logic has two stages of operation. First is the dynamic stage and the second is the buffer stage.

The average power consumption of first stage can be found out by

$$P_{avg1} = K.{V_{DD}}^2.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{dyn} \quad (3.1)$$

In which, r = T_{on}/ (T_{on}+T_{off});

K is the probability of the state that the input logic change in a unit time. Note that K carries the unit of frequency.

T_{off} is the time when input logic is OFF

T_{on} is the time when input logic is ON.

V_{noise} is the pulse voltage in output node of basic domino logic

C_{dyn} is the capacitance at node N_DYN

Power consumption of the second stage in conventional domino logic can be calculated by,

$$P_{avg2}=K.V_{DD}{}^2.\left(C_{load}+C_{buffer}\right)+r.f.V_{DD}.V_{noise}.\left(C_{load}+C_{buffer}\right) \quad (3.2)$$

C_{buffer} is the buffer's internal parasitic capacitor.

C_{load} is the load capacitor in the output of the buffer.

Assuming $C_{load} \gg C_{buffer}$, we can simplify equation (3.2)

$$P_{avg2}=K.V_{DD}{}^2.C_{load}+r.f.V_{DD}.V_{noise}.C_{load} \quad (3.3)$$

And the total power consumption of the conventional case is

$$P_{avg}=K.V_{DD}{}^2.\left(C_{load}+C_{dyn}\right)+r.f.V_{DD}.V_{noise}.\left(C_{load}+C_{dyn}\right) \quad (3.4)$$

In contrast, in the proposed logic style, when PDN turns from OFF to ON, output node gets pulled up to the 'High' logic level. This pulling up will consumes a large amount of current. In the precharge period, when the pull-down network is on, the node 'a' and 'b' will nearly be the same for, and

$$V_{GS} = V_G - V_S = V_a - V_b = 0.$$

As per theory, when V_{GS} is having lower voltage than V_{TH}, then the MOS transistor will be OFF and there is very small current go through it, which can be overlooked in most cases.

Now, we can find the power saving, if we will find the power consumption of the proposed structure. Since the first stage is same as conventional stage, the power consumption of the stage 1 is not changed as equation (3.1). The consumption of second stage of proposed logic is given in equation (3.5).

In the proposed logic power is given by

$$P_{prop} = K.V_{DD}{}^2.C_{load} + r.f.V_{DD}.V_{noise\_p}.C_{load} \quad (3.5)$$

Where V_{noise_p} is the pulse voltage in the output node of the proposed logic

So the finally the amount of power which the proposed circuit saves is then observed from equation (3.1), (3.4) and (3.5) is

$$\mathrm{P_{avg}} - \mathrm{P_{prop}} = \mathrm{K}.V_{DD}{}^2.\left(C_{load} + C_{dyn}\right) + r.f.V_{DD}.V_{noise}.\left(C_{load} + C_{dyn}\right) - \mathrm{K}.V_{DD}{}^2.C_{load} - r.f.V_{DD}.V_{noise\_p}.C_{load}$$

Power saved due to semidynamic logic is

$$P_{saved} = \mathrm{K}.V_{DD}{}^2.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{load} - r.f.V_{DD}.V_{noise\_p}.C_{load}$$

We can take $V_{noise} \gg V_{noise\_p}$, as noise in the proposed logic is very less as compared to noise in the basic domino logic. So, the above equaton becomes,

$$P_{saved} = \mathrm{K}.V_{DD}{}^2.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{dyn} + r.f.V_{DD}.V_{noise}.C_{load} \quad (3.6)$$

The ratio of power saved η can be calculated as,

$$\eta = \frac{\mathrm{P_{avg}} - \mathrm{P_{prop}}}{\mathrm{P_{avg}}}$$

$$\eta = \frac{\mathrm{K}.V_{DD}{}^2.\left(C_{load} + C_{dyn}\right) + r.f.V_{DD}.V_{noise}.\left(C_{load} + C_{dyn}\right) - \mathrm{K}.V_{DD}{}^2.\left(C_{load} + C_{dyn}\right) - r.f.V_{DD}.V_{noise_p}.C_{load}}{\mathrm{K}.V_{DD}{}^2.\left(C_{load} + C_{dyn}\right) + r.f.V_{DD}.V_{noise}.\left(C_{load} + C_{dyn}\right)}$$

The dynamic capacitance is very less as compared to the load capacitance

i.e. $C_{dyn} << C_{load}$

So in the above derivation we have neglected the C_{dyn}

$$C_{load} + C_{dyn} = C_{load}$$

The ratio of power saved η *becomes,*

$$\eta = \frac{\begin{matrix} r.f.V_{DD}.V_{noise}.C_{load} \\ - r.f.V_{DD}.V_{noise_p}.C_{load} \end{matrix}}{\mathrm{K}.{V_{DD}}^2.C_{load} + r.f.V_{DD}.V_{noise}.C_{load}}$$

According to equation (3.6), assuming the frequency of Clk is very large (in this simulation we have simulated with f = 500 MHz), then the above equation becomes,

$$\eta = \frac{r.f.V_{DD}.(V_{noise} - V_{noise_p}).C_{load}}{r.f.V_{DD}.V_{noise}.\left(C_{load} + C_{dyn}\right)}$$

$$\eta = \frac{(V_{noise} - V_{noise_p}).C_{load}}{V_{noise}.\left(C_{load} + C_{dyn}\right)} \quad (3.7)$$

If we will ignore the output noise of the proposed buffer, than the power saving is:

$$\boxed{\eta \simeq \frac{C_{load}}{C_{load} + C_{dyn}}} \quad (3.8)$$

(Note: the concusion is on the condition that $C_{dyn} << C_{load}$)

As this thesis progresses; we will show the amount of power saving with this circuit technique.

3.4.5 CHARGE SHARING ANALYSIS

In spite of a lot of advantages, domino circuits need special care to eliminate the charge-sharing problem. This problem results in an unexpected value of output. Let's consider a domino k-input AND gate in Fig. 3.11. In the evaluation period, supposing all

inputs In_i, are at high excepting input In_k which is situated next to the clock transistor M_n is low. As kth input In_k is at 'low', ideally, the value of the dynamic node V_X should remain at 'high'; but, the capacitor at the dynamic node C_O is charged in the precharge phase is distributed to the internal nodes of those turned-on transistors. Let C_i is the equivalent capacitance of the internal node, as shown in Fig. 3.11. The output voltage V_x, becomes V_{DD} * C_0 (C_0+C_i) in the evaluation phase. When C_i is very large, V_x may become too 'low' to determine the succeeding stage. As a result, under certain input conditions, re-distribution of charge among junction capacitance at internal nodes can cause error or glitch at outputs [108] [109] [110].

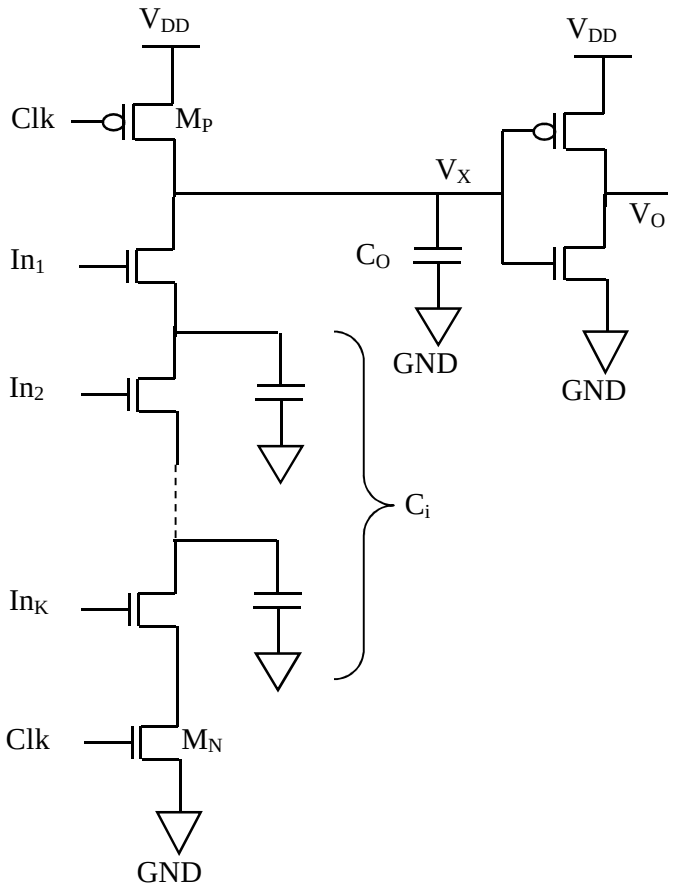


Fig. 3.11 Charge sharing Problem in Domino gate

This proposed logic also suffers from charge sharing problem in the precharge period. Charge sharing is introduced at the parasitic capacitance at node N_FOOT when the logic input is high. The voltage drop at the dynamic node should be less than noise margin. If there is a voltage drop at this dynamic node then there will be a variation in the output node. However, this variation can propagate to the next stage leading to serious charge sharing

problem and also leading to an incorrect output. Fig.3.12 shows the charge sharing problem in the proposed work.

This charge sharing problem can be assuaged by making some changes in the circuit.

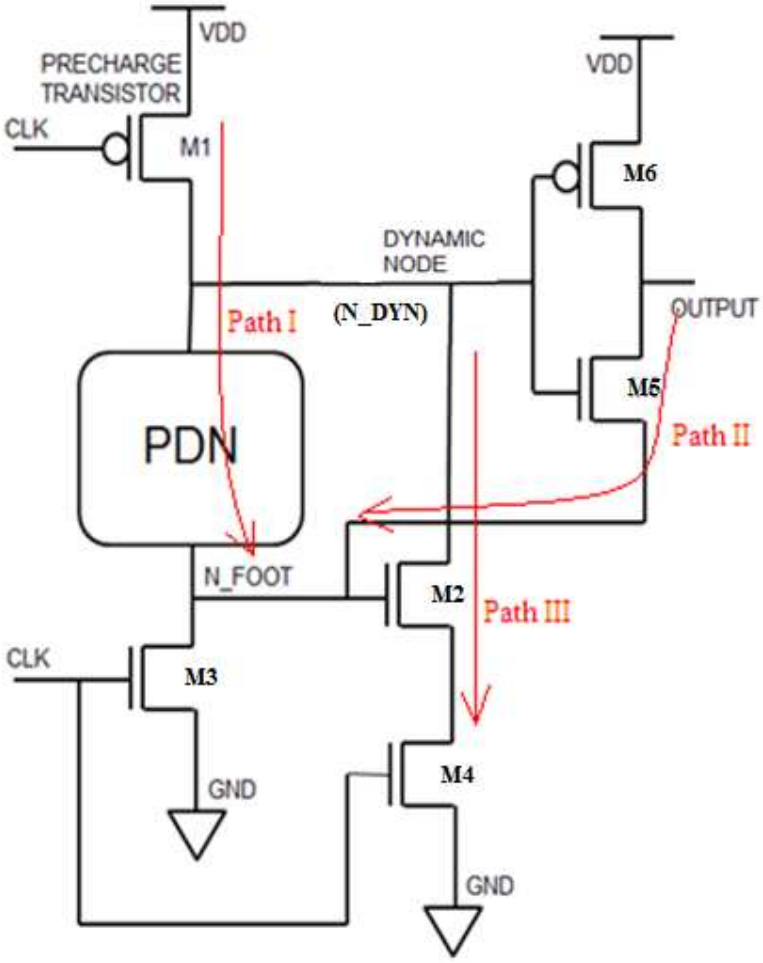


Fig.3.12 Charge sharing problem in the proposed work

Solution I – Dual voltage technique as shown in Fig.3.13 (a) - An extra higher voltage can be used as V_{DD2} for making the dynamic buffer to work at a higher voltage. We have to make V_{DD1} will be lower than V_{DD2}. This technique will compensate the voltage drop at the output node due to charge sharing. Fig.3.13 (a) shows the case of dual V_{DD}.

Result – It uses the dual power for voltage compensation at the output node. This process does not use any parasitic load capacitance and the charge sharing can be eliminated. But in this circuit technique we have to turn off the PMOS of the buffer. This dual voltage solution in this circuit technique will prohibit the switching off of PMOS, as V_{gsp} will be greater than the difference in V_{DD1} and V_{DD2}.

$$|V_{gsp}| > V_{DD2} - V_{DD1} > 0$$

This leads to a large leakage current which leads to the biggest drawback of submicron technologies.

Solution II – Channel length modification as shown in Fig.3.13 (b) – Increasing the channel length of M_5 can decrease the current flowing through path II and increase the current flowing through path I. It will also keep the transistor M_2 in off state to close the path III. So the voltage drop at output node will decrease. Fig.3.13 (b) shows this solution.

Result – By increasing the channel length a larger amount of charge will be shared through the PDN instead of M_5. This moderates the charge sharing at the output node. This process can lead to increase in delay of the circuit and also cannot solve the charge sharing solution completely.

Solution III – Increasing load capacitance as shown in Fig.3.13 (c) – By increasing the load capacitance of the output node C_o will be more than C_f. Making this we can reduce the charge sharing effect.

Result – when output load capacitance increased a lot of extra power was used by the circuit. Also it cannot reduce the charge sharing problem completely.

Solution IV – Increasing the width of M_2 we can reduce the current flowing through path III resulting in more current flow through path I as shown in Fig.3.13 (d).

Result – This increase the delay of the circuit and the circuit gets slow. Also it cannot completely eliminate the problem in cost of a large delay in the circuit.

Solution V – Implementing keeper- A keeper can be implemented parallel to the PMOS transistor as shown in Fig.3.14(a).

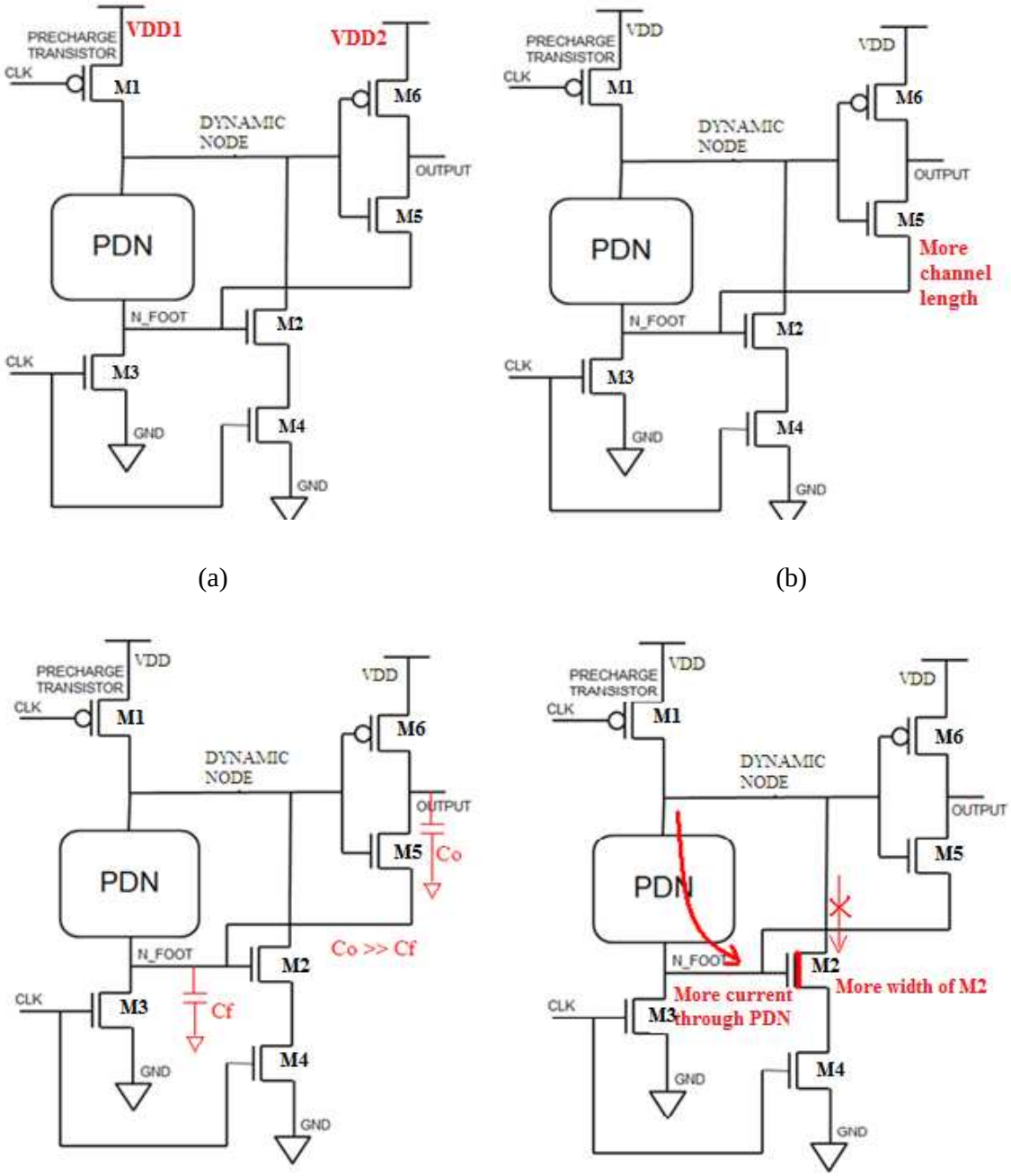


Fig.3.13 (a) Dual V_{DD} implementation (b) Increasing the channel length (c) Increasing load capacitance (d) Increasing the width of M_3

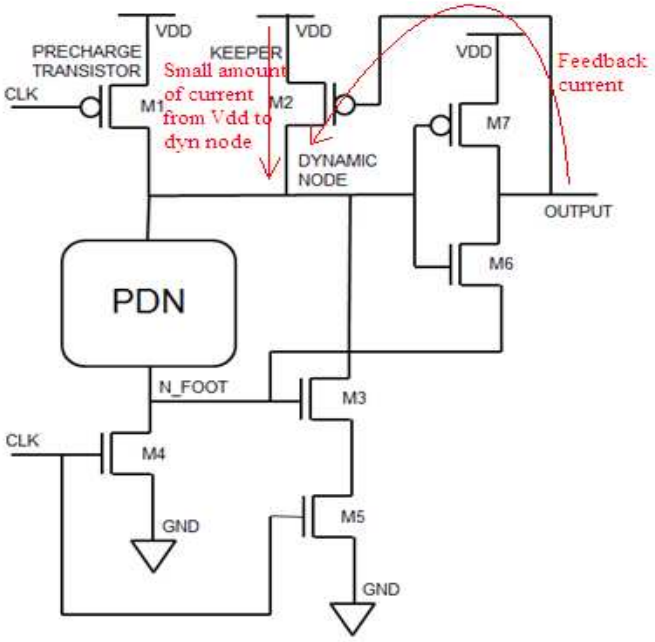
Result – Keeper is generally solves the charge sharing issue in dynamic logics. This is a very good solution because there is no static power consumption in the circuit with a keeper. It is a very good solution as compared to the solution I, II, III, IV. In this case voltage drop at the output node can be entirely eliminated. It also has less delay effect as compared to other solutions as less parasitic capacitance are involved.

The keeper transistor is generally a weak transistor. Keeper transistor supplies a slight amount of current from the V_{DD} to the dynamic node to recover the charge loss and to improve the noise robustness of the circuit. When the output node is at 0, it supplies 0 to the keeper transistor M_2. M_2 then gets ON. V_{DD} is then supplied to the dynamic node by which the charge loss at the dynamic node gets compensated to make the dynamic node at strong 1.

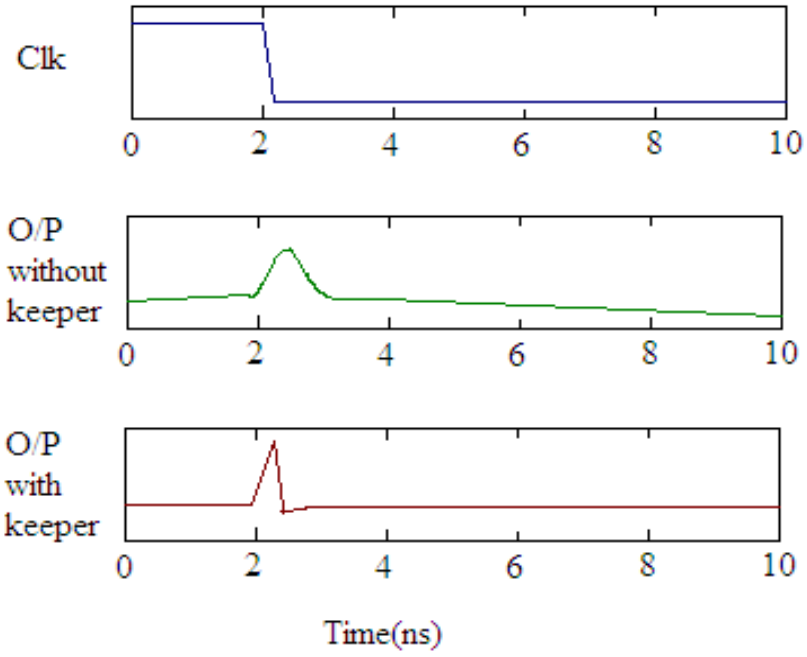
Fig.3.14(b) shows the simulation results of the charge sharing without and with keeper. The output waveform shows that the circuit with keeper keeps the output voltage at strong 1. This assures a good stability of the circuit. Using 180 nm technology when it was simulated with V_{DD}=1.8 V with and without keeper and compared then it can be seen that we can get a power saving of 45 % to 65 %. This can guarantee a stable circuit. Table 3.1 shows the comparison of power consumption of proposed circuit with and without keeper.

Table 3.1 Power consumption of the proposed circuit with and without keeper

Fan-in	Power consumption with keeper	Power consumption without keeper	Power consumption overhead
2-bit	1.80E-08	3.32E-08	45%
4-bit	2.56E-08	5.82E-08	62%
8-bit	3.11E-08	6.15E-08	49%
16-bit	3.42E-08	7.35E-08	63%
32-bit	4.23E-08	9.53E-08	55%



(a)



(b)

Fig.3.14 Keeper implementation

3.5 OR GATE IN PROPOSED LOGIC

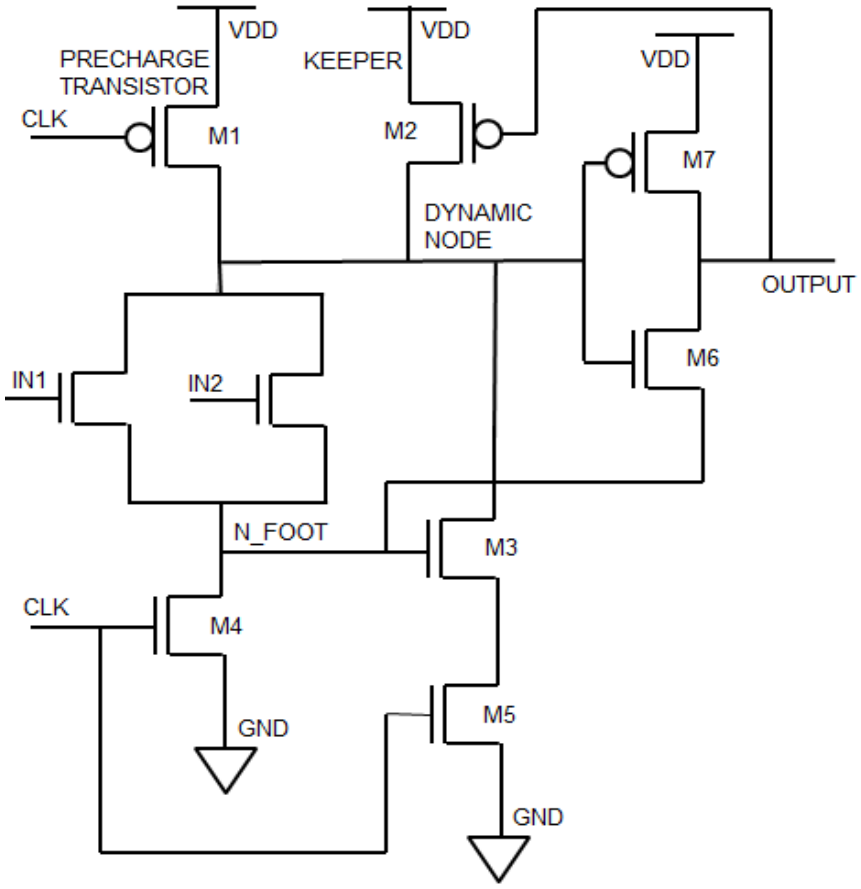


Fig. 3.15 Proposed 2-input OR gate

3.5.1 CIRCUIT DESCRIPTION AND OPERATION

In the domino logic worst case arises with OR gate, as there is no stacking transistor in the PDN designed with basic domino logic. Hereby, the novel OR gate is designed using the proposed logic as shown in Fig. 3.15. The PDN of basic OR gate is replaced by the two NMOS transistors supplied with the inputs IN_1 and IN_2 respectively. This circuit consists of a precharge transistor, an evaluation network evaluating two input OR, a keeper transistor, footer transistors and semi-dynamic inverter. In the precharge period, when the clock is 'LOW', the precharge PMOS gets ON and dynamic node gets connected to the V_{DD} and gets precharge to V_{DD}.When clock goes 'high', the evaluation period starts and output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic 1. At the evaluation period when all the inputs are at logic 0, the dynamic node becomes at logic 1. But the NMOS PDN leaks the charge stored in the capacitance at

the dynamic node due to the subthreshold leakage. This is again compensated by the PMOS keeper M_2, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at gate input, the keeper may not be able to restore the voltage level of the dynamic node. To stop that the footers M_3, M_4 and M_5 are connected. M_4 acts as stack transistor. At the evaluation phase when the PDN is at logic 1, at that time M_4 stops the free discharge of dynamic node voltage to evaluate logic 0 at the dynamic node. To compansate that M_3 makes a charge discharge path. Here M_5 again acts as a stack for the 2^{nd} path to maintain the dynamic node.

Domino logic always followed by an inverter. Trasistors M_7 and PMOS transistor M6 make a static NOT gate. This circuit expliots the principle of static logic, where, in static inverter, the source of NMOS is connected to ground. In this logic design the source of NMOS M_6 is connected to the foot of the PDN i.e the N_FOOT of the dynamic logic.

When the PDN is OFF and the N_DYN is at high voltage and the N_FOOT is at low voltage. The high level of dynamic node makes the gate of the NMOS M6 of the buffer V_{DD} and the low level of N_FOOT makes the source of the M_6 to 0. This makes M_6 ON and the voltage of buffer output will be same as the voltage of N_FOOT. It can be easily verified that if the NMOS of the buffer can permanently be turned off, pulses propagating to the output can be avoided.

In the evaluation period, when the NMOS clock transistor M_4 gets ON, N_FOOT gets discharged to 0. When the PDN is ON the N_DYN also gets discharged to ground. This makes the V_{GS} of buffer NMOS M_6 to 0 as $V_{GS} = V_G - V_S = 0$. This makes the NMOS OFF and the buffer output gets completely charged through PMOS M_7.

In precharge period, the dynamic node will get charged to ‘high’, when the PDN is ON the voltage of the N_FOOT is nearly same as N_DYN, as the NMOS M_4 is OFF. The V_{GS} of the buffer NMOS will be $V_G - V_S < V_{TH}$ which keeps the NMOS of the buffer at turned OFF stage. The PMOS of the buffer is also OFF due to the high level of N_DYN node. This makes the output of buffer LOW.

In the evaluation period, when the NMOS clock transistor M_4 is ON, N_FOOT gets discharged to 0. When the PDN is ON the N_DYN also gets discharged to ground. This makes the V_{GS} of buffer NMOS M_6 to 0 as $V_{GS}=V_G-V_S=0$. This makes the NMOS OFF and the buffer output gets completely charged through PMOS M_7.

In precharge period, the dynamic node will get charged to high, when PDN is ON the voltage of the N_FOOT is nearly same as N_DYN, as the NMOS M_4 is OFF. The V_{GS} of the buffer NMOS will be $V_G - V_S < V_{TH}$ which keeps the NMOS of the buffer at turned OFF stage. The PMOS of the buffer is also OFF due to the high level of N_DYN node. This makes the output of buffer LOW.

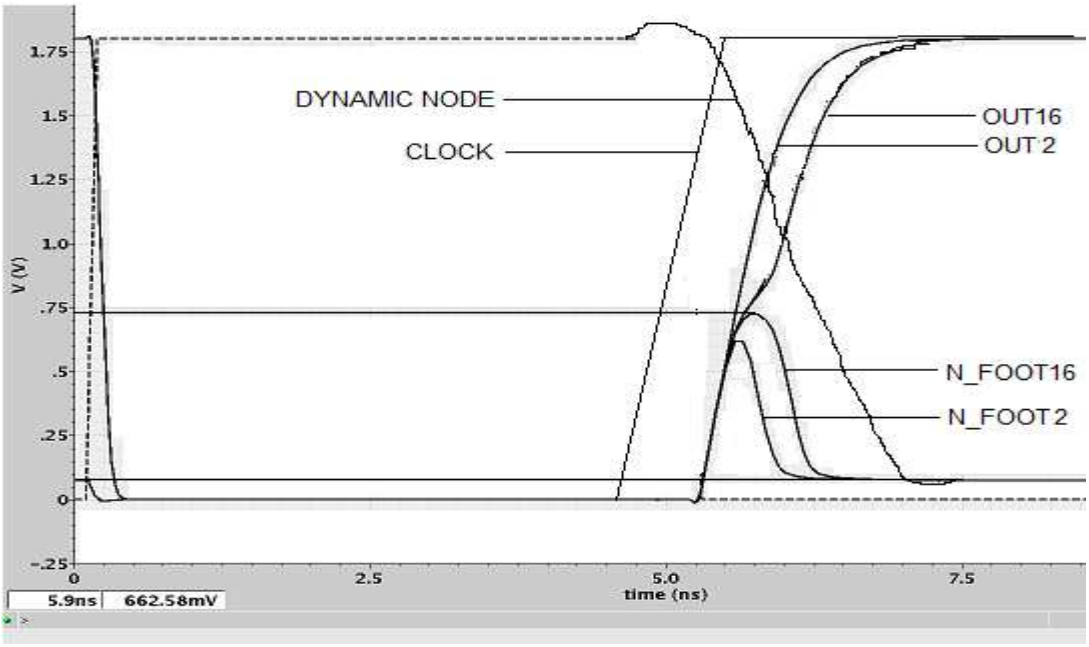


Fig.3.16 Simulated output voltages from 2-input to 16 input of OR gate

Fig.3.16 shows the simulated waveform of the proposed dynamic logic for OR gate. Here the number of inputs was varied from 2- inputs to 16-inputs. Fig.3.16 shows how the output waveform and the waveform of the N_FOOT shift towards the right with increasing the number of input.

3.6 COMPARISON OF THE PROPOSED OR GATE WITH DOMINO OR GATE

The circuits were simulated with Cadence Spectre using UMC 180 nm technologies and 1.8 V. The proposed circuit was being compared with the OR gate designed with previousproposed techniques. The OR gate was implemented and used as a vehicle for circuit observation because it is a typical example of wide pull-down network.

3.6.1 COMPARISON WITH NUMBER OF DEVICES USED

The proposed circuit was implemented and compared with the OR gate of other reference circuits and also investigated with different values of fan-in. It was found that the proposed circuit performs better than the previous proposed circuits due to its less switching activity at the output. Table 3.2 shows the comparison of the proposed scheme with the previous proposed schemes according to the number of transistor used and the use of inverting input. This comparison is useful because, the number of transistor effect the size of the circuit and the inverting input uses an extra inverter in the circuit. The presence of inverting input also create problem with the synchronization of the circuit.

Table 3.2 Comparasion of the proposed domino with previous proposed domino logic styles by number of transistors used for implementing 2-input OR gate

Circuit type	Scheme on Paper [95]	Scheme on paper [90]	Proposed Scheme
Number of transistor used transistor used	12	11	09
Use of Inverting clock	Yes	Yes	No

3.6.2 AREA PERFORMANCES

While, the performance of a circuit comes into consideration, area performs a vital role. Therefore, in this section we have designed OR gates with all types of logic styles. Except the basic logic styles, the OR gate with proposed logic has the lowest area as compared to the other reference domino logic styles, as some extra number of transistors are used in this circuit which gives benefit in form of power, delay and noise reduction. Fig.3.17 shows the chart presenting the comparison of area for all the logic styles, simulated with 2-input OR gate.

Fig.3.18 shows delay vs area for OR gate designed with the proposed logic and other reference circuits described in [95] and [90]. In Fig.3.18 the lowest point refers the proposed logic, higher and middle points refer scheme on [95] and [90] respectively. This graph has

been plotted for 2-inpur OR gate designed with different logic. The previous proposed reference circuits require more number of transistors to implement a given logic. On the other hand, the number of transistor required is lesser in the proposed logic circuit to design the same given logic. Fig.3.19 shows the PDP (logarithmic scale) vs area graph where the lowest point refers the proposed logic, higher and middle points refer scheme proposed on reference [95] and [90].

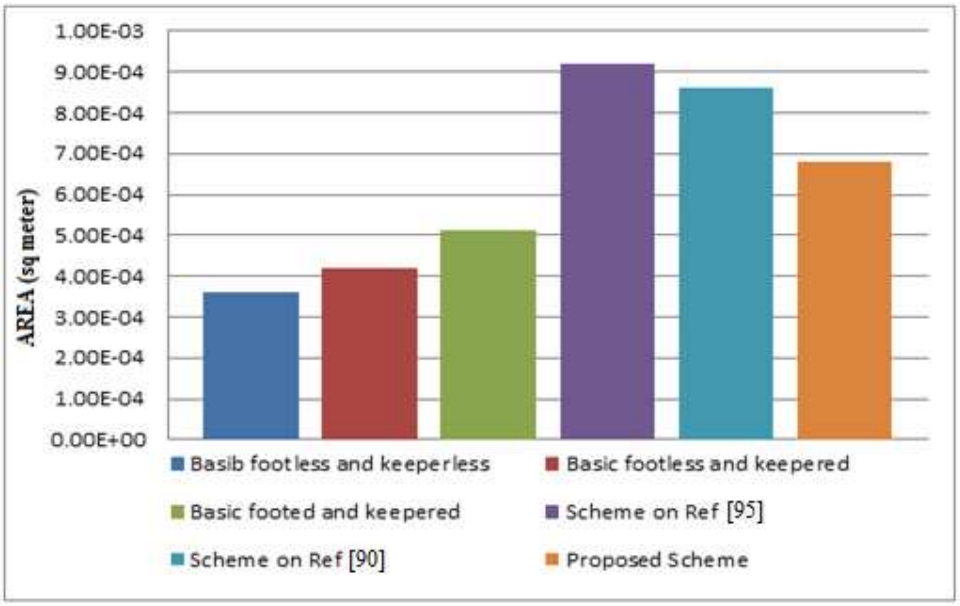


Fig.3.17 Chart showing area comparison of all the logic styles with proposed logic (Simulated with 2-input OR- gate)

[Note: - In Fig.3.18 the leftmost and the lowermost point represents high performance circuit as low area and less delay is desired in a circuit. Also, in Fig.3.19 the leftmost and the lowermost point represents high performance circuit as low area and less PDP is desired in a circuit.]

All the simulations were done using cadence spectre 180 nm technology, using 1.8 V V_{DD}, 500 MHz Clk frequency and at 27^0 C temperature. For comparison, all these circuits have been simulated in same environmental condition with 2-input OR gate.

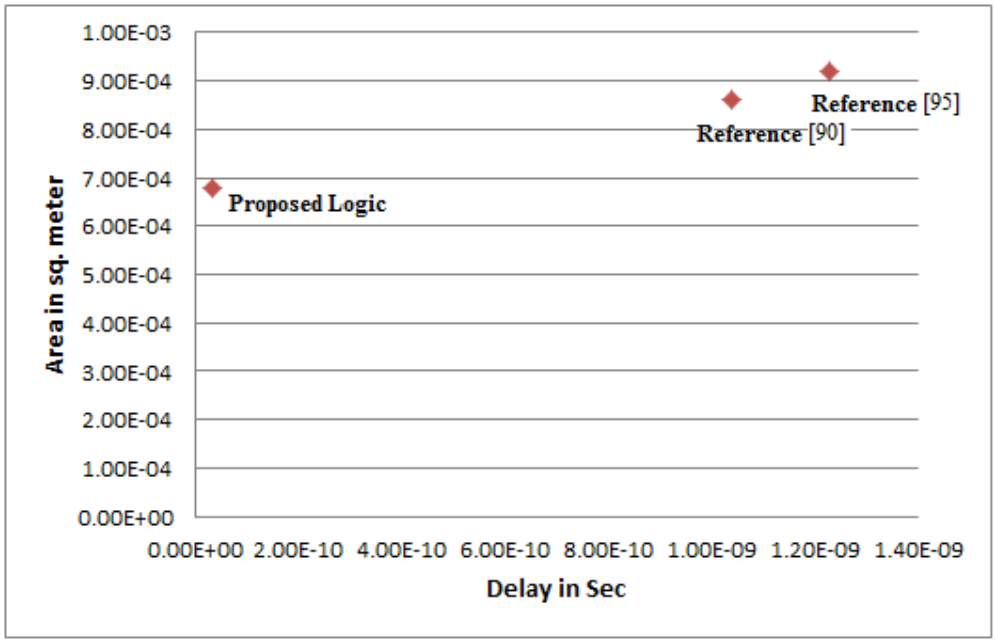


Fig.3.18 Delay vs area where the lowest point refers the proposed logic, higher and middle points refer scheme on [95] and [90]

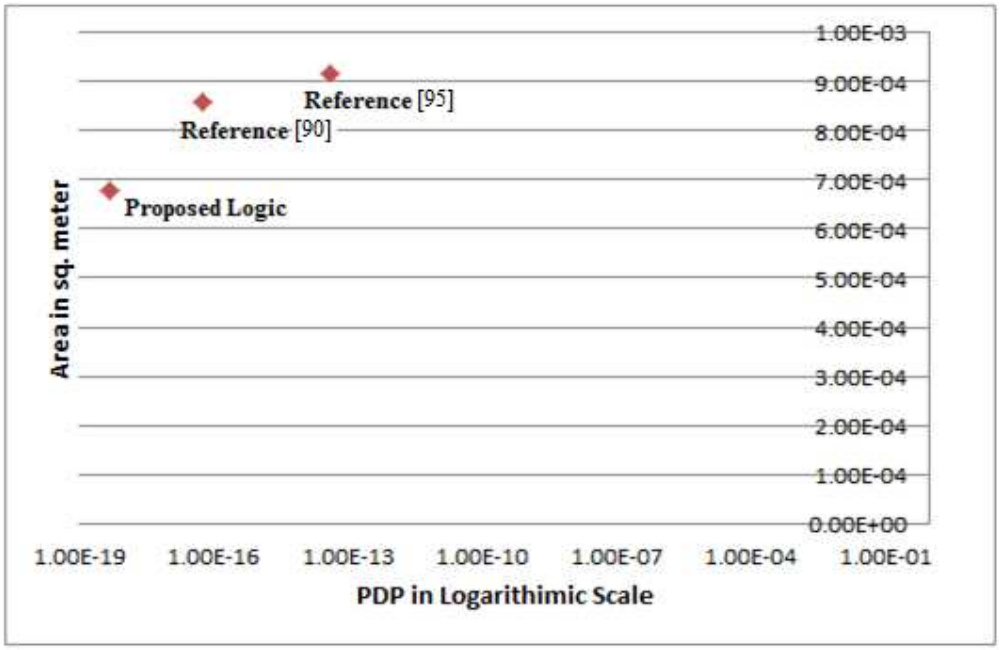


Fig.3.19 PDP (logarithmic scale) vs area where the lowest point refers the proposed logic, higher and middle points refer scheme on [95] and [90]

3.6.3 PDP PERFORMANCE

Table 3.3 Comparison of power and delay for OR gate designed with proposed domino logic with OR gate designed with Basic circuit and other reference circuits (Varying the supply voltage)

Supply Voltage in Volt	Parameters	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [95]	Scheme on paper [90]	Proposed Scheme
1.8	**Delay**	1.57 E-11	2.40 E-11	4.10 E-11	1.23 E-9	1.04 E-9	3.3 E-11
	Power	3.33 E-5	3.32 E-5	5.60 E-6	4.58 E-5	5.6 E-8	1.42 E-8
1.6	**Delay**	1.78 E-11	2.69 E-11	4.10 E-11	1.28 E-9	1.05 E-9	3.86 E-11
	Power	2.39 E-5	2.39 E-5	9.60 E-6	3.20 E-5	8.58 E-8	1.56 E-8
1.4	**Delay**	2.08 E-11	3.13 E-11	4.11 E-11	1.32 E-9	1.06 E-9	4.64 E-11
	Power	1.62 E-5	1.62 E-5	2.80 E-5	2.20 E-5	1.49 E-8	4.80 E-8
1.2	**Delay**	2.52 E-11	3.82 E-11	4.00 E-11	1.35 E-9	1.09 E-9	5.89 E-11
	Power	1.01 E-5	1.01 E-5	1.14 E-5	1.39 E-5	1.39 E-8	3.10 E-8
1.0	**Delay**	3.29 E-11	5.04 E-11	4.01 E-11	1.42 E-9	1.15 E-9	6.10 E-11
	Power	5.56 E-6	5.56 E-5	1.40 E-5	7.81 E-5	1.44 E-8	2.37 E-8
0.8	**Delay**	4.90 E-11	7.73 E-11	4.16 E-11	1.58 E-9	1.31 E-9	1.28 E-10
	Power	2.44 E-6	2.46 E-5	1.40 E-5	3.50 E-5	3.1 E-8	5.55 E-8

Table 3.4 Comparison of PDP for OR gate designed with proposed domino logic with OR gate designed with Basic circuit and other reference circuits (Varying the supply voltage)

Supply Voltage in Volt	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [95]	Scheme on paper [90]	Proposed Scheme
1.8	5.23E-16	7.97E-16	2.30E-17	3.94E-14	5.82E-17	4.69E-19
1.6	4.25E-16	6.43E-16	3.94E-17	4.10E-14	9.01E-17	6.02E-19
1.4	3.37E-16	5.07E-16	1.15E-16	2.90E-14	1.58E-17	2.23E-18
1.2	2.55E-16	3.86E-16	4.56E-17	1.88E-14	1.52E-17	1.83E-18
1.0	1.83E-16	2.80E-15	5.61E-17	1.11E-13	1.66E-17	1.45E-18
0.8	1.20E-16	1.90E-15	5.82E-17	5.53E-14	4.06E-17	7.10E-18

The PDP (Power-Delay Product) was calculated, simulated and plotted using cadence spectre. We constructed the 2 to 32 bit OR gate using the basic techniques, reference techniques and our proposed technique.

Table 3.5 Comparison of power and delay for OR gate designed with proposed domino logic with OR gate designed with Basic circuit and other reference circuits (Varying the number of fan-in)

OR-gate fan-in	Parameters	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [95]	Scheme on paper [90]	Proposed Scheme
2-Bit	**Delay**	3.96E-11	6.86E-11	5.10E-11	1.98E-09	1.95E-09	4.86 E-11
	Power	2.29E-05	3.29E-05	7.80E-06	5.30E-05	7.32E-08	3.32 E-08
4-Bit	**Delay**	4.58E-11	6.99E-11	7.45E-11	3.12E-09	2.56E-09	5.44 E-11
	Power	3.92E-05	3.92E-05	7.98E-06	5.25E-05	1.29E-07	5.82 E-08
8-Bit	**Delay**	5.59E-11	7.79E-11	8.70E-11	5.46E-09	4.09E-09	6.99 E-11
	Power	5.84E-05	5.84E-05	9.12E-06	7.42E-05	1.59E-07	6.15 E-08
16-Bit	**Delay**	6.53E-11	8.23E-11	9.51E-11	7.52E-09	7.15E-09	8.04 E-11
	Power	6.85E-05	6.83E-05	1.40E-05	8.81E-05	3.44E-07	7.35 E-08
32-Bit	**Delay**	9.95E-11	1.95E-10	1.35E-11	1.58E-08	1.56E-08	1.07 E-10
	Power	7.44E-05	7.43E-05	4.42E-05	9.72E-05	7.10E-07	9.53 E-08

Table 3.6 Comparison of PDP for OR gate designed with proposed domino logic with OR gate designed with Basic circuit and other reference circuits (Varying the number of fan-in)

OR-gate fan-in	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [95]	Scheme on paper [90]	Proposed Scheme
2	9.07E-16	1.57E-15	3.98E-17	1.05E-13	1.43E-16	1.61E-18
4	1.8E-15	2.74E-15	5.95E-17	1.64E-13	3.3E-16	3.17E-18
6	3.26E-15	4.55E-15	7.93E-17	4.05E-13	6.5E-16	4.3E-18
16	4.47E-15	5.62E-15	1.33E-16	6.63E-13	2.46E-15	5.91E-18
32	7.4E-15	1.45E-14	5.97E-17	1.54E-12	1.11E-14	1.02E-17

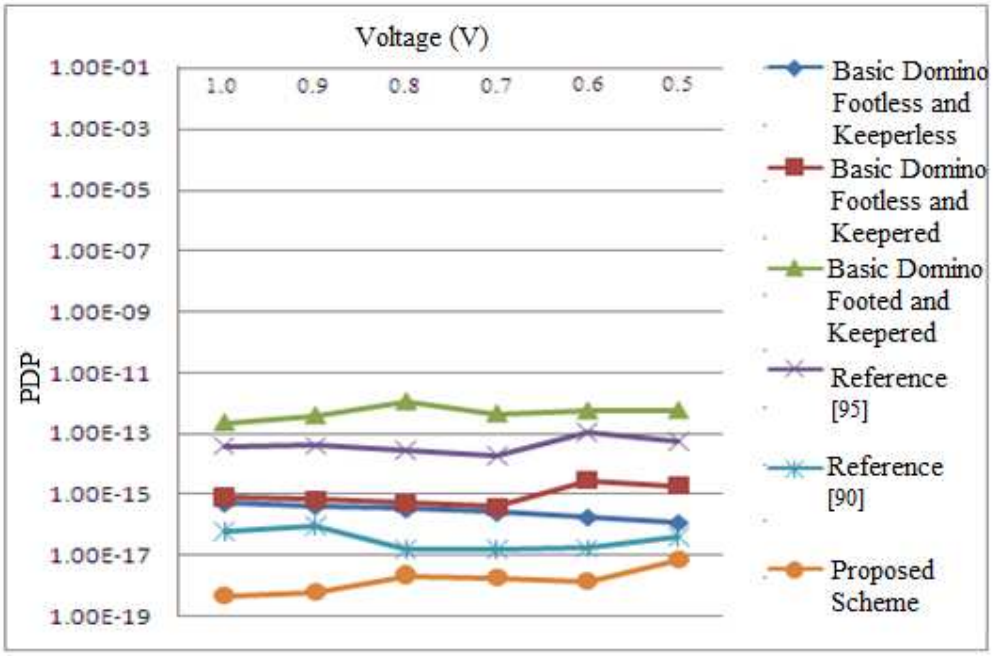


Fig.3.20 PDP Plot for the proposed scheme with the other schemes by reducing V_{DD} from 1.0 V to 0.5V

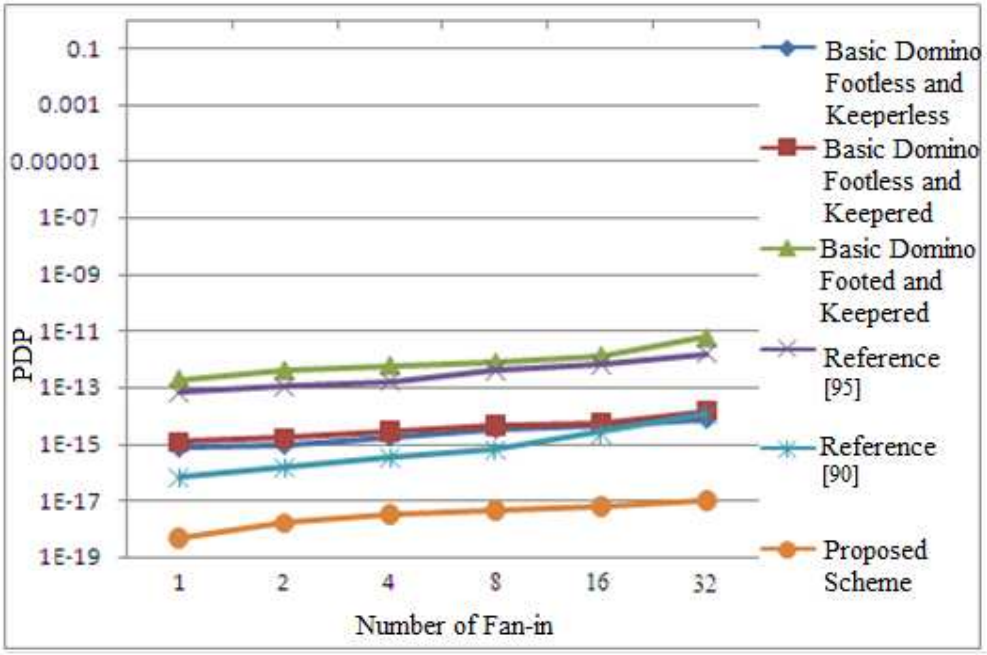


Fig.3.21 Simulation of OR-gate PDP Plot comparision for the proposed scheme with the other schemes by increasing the fan-in upto 32 bit

Fig.3.20 shows the comparison of power delay product (PDP) of all the reference circuits, the basic circuits and the proposed circuit, varying the voltage from 0.8 V to 1.8 V. Fig.3.21 compares the power-delay product (PDP) of the circuits by increasing number of fan-in. When compared to the other circuits, it can be seen that, the PDP can be reduced nearly 80% in the proposed circuit. This results due to the less number of switching in the circuit, which leads to faster operation and less power dissipation of the circuit for evaluation of the logic. Table 3.3 figures out the individual power and delay of the circuits, whereas Table 3.4 gives the information of the PDP of the individual circuits for different input voltages. Table 3.5 figures out the individual power and delay of the circuits and Table 3.6 shows the PDP of the circuit with different fan-in. The proposed circuit shows advantage in having less number of transistors as compared to the previous. As compared to the basic domino the proposed circuit contains only 3 extra transistors, where the other circuits contain more number of extra transistors as compared to basic domino circuit with the disadvantage of having the inverting clock.

3.6.4 SIMULATION RESULTS USING 65 nm TECHNOLOGY

We checked the power delay product using 65 nm technology. Power dissipation of the circuit increased a little bit as compared to 180 nm technology because of the presence of small spikes in the output node. Speed of the circuit increased as compared to 180 nm technology and finally PDP decreased by 10%.

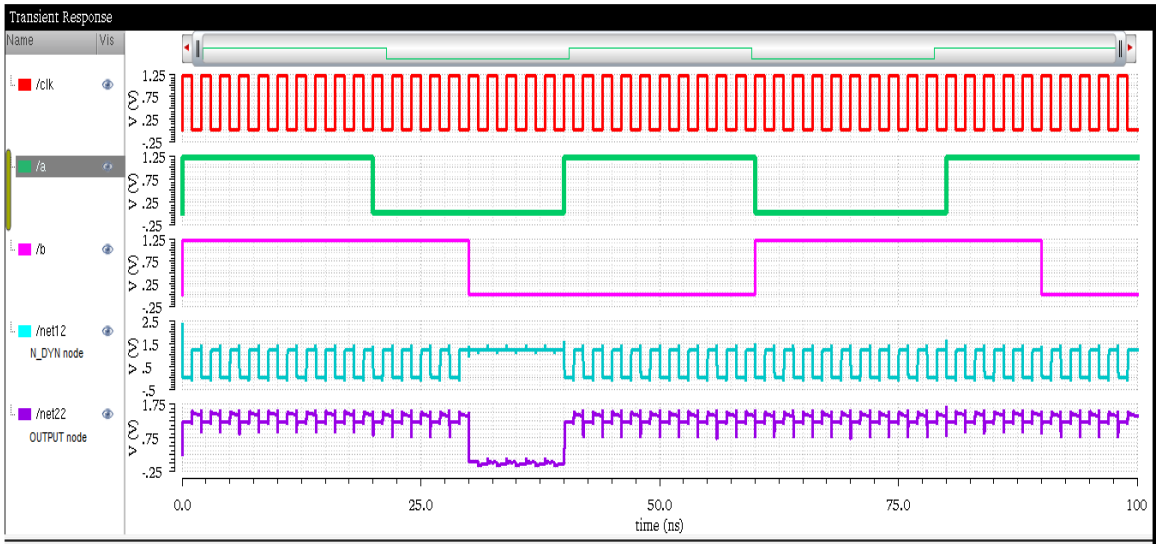


Fig. 3.22 Simulation output of 2-input OR gate using V_{DD}=1.2 V and in 65 nm technology

Table 3.7 Power and delay performance of 2-input OR gate using 180 and 65 nm technologies

Technologies	Power	Delay
180 nm	3.10 E-8	5.89 E-11
65 nm	4.20 E-8	3.90 E-11

Table 3.8 PDP performance of 2-input OR gate using 180 and 65 nm technologies

Technologies	PDP
180 nm	1.82 E-18
65 nm	1.63 E-18

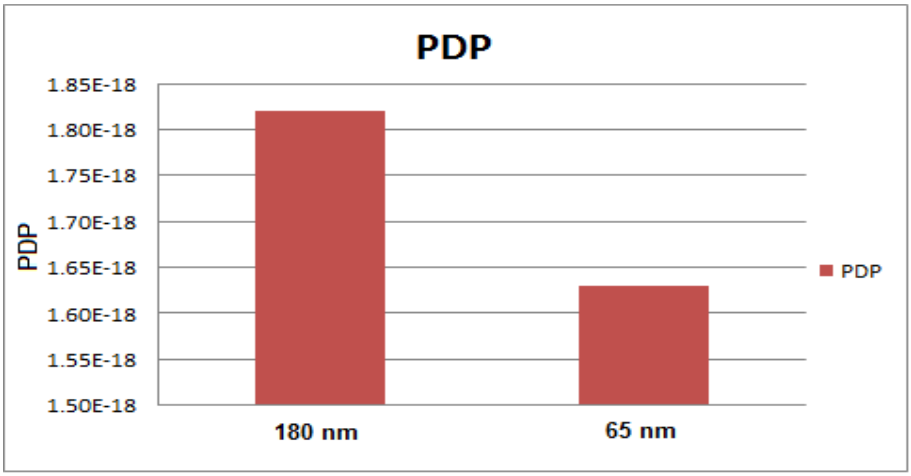


Fig. 3.23 PDP performance of 2-input OR gate using 180 and 65 nm technologies

Fig. 3.22 depicts the simulation output of 2-input OR gate using VDD = 1.2 V and in 65 nm technology. Table 3.7 shows power and delay performance of 2-input OR gate using 180 and 65 nm technologies and Table 3.8 and Fig. 3.23 compares PDP performance of 2-input OR gate using 180 and 65 nm technologies.

3.7 LEAKAGE CURRENT COMPARISON

All the noise tolerant circuit techniques are based on the principle of increasing the threshold voltage of transistors in the PDN. The increase in threshold voltage of NMOS transistors leads to reduction in sub-threshold leakage current [111]. Sub-threshold leakage current (I_{subth}) is the drain to source leakage current when transistor is OFF and is given by [111].

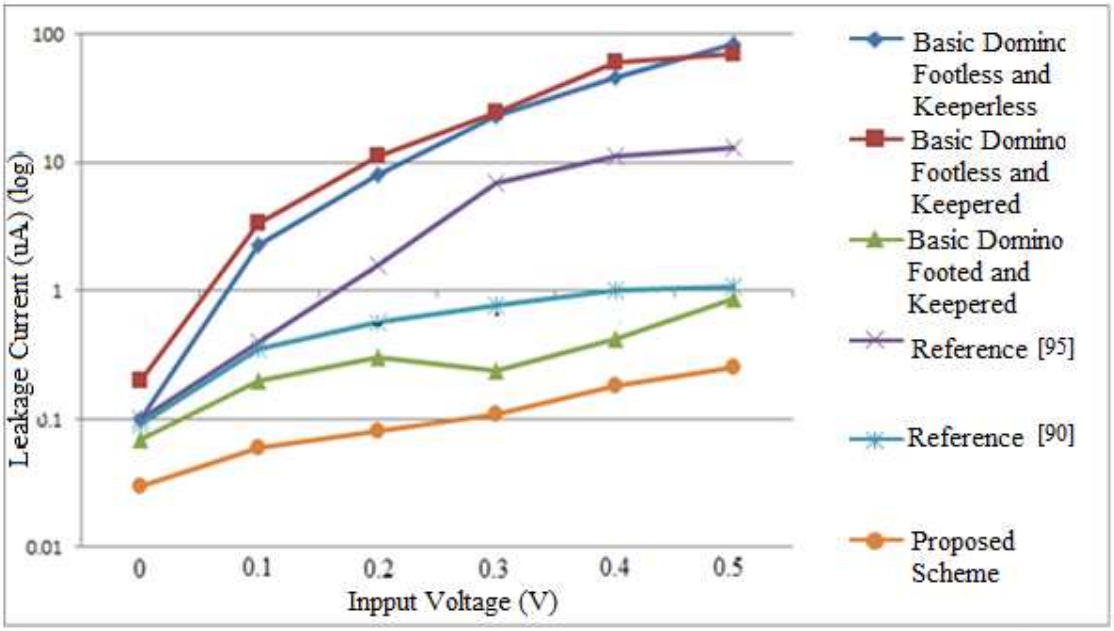


Fig.3.24 Leakage currents of the analyzed techniques as a function of input voltage for 16-input OR-gate

$$I_{subth} = Ae^{\frac{1}{mV_T}(V_{GS}-V_{th\,0}-\gamma V_S+\eta V_{DS})}[1-e^{\frac{V_{DS}}{V_T}}]$$

Where

$$A = \mu_0 C_{OX}^{'} \frac{W}{L_{eff}} (V_T)^2 e^{1.8} e^{\frac{-\Delta v_{dt}}{\eta V_T}}$$

Also

$V_{th\,0}$ = Zero bias Threshold Voltage

V_T = KT/q is the thermal Voltage

η = DIBL coefficient

Cox = Gate oxide Thickness

μ0 = Zero bias mobility

m = subthreshold swing coefficient

Fig.3.24 depicts a semi-log graph where the leakage currents at the critical node (I_{LEAK} for the techniques [95] [90] and [112] [113] [114] [115] [116] [117] I_{VDN} for the proposed one) are plotted as a function of the gate input voltage. The graph relates to a 16-input OR gate and the variable parameters of each technique have been set in order to ensure the same PDP value. It is worth noting that the difference between I_{LEAK} of the schemes [112] [113] [114] [115] [116] [117] and I_{VDN} of the proposed technique is larger than one order of magnitude. The stacking transistor and the extra path from the dynamic node to the ground help in reducing the leakage current.

3.8 KEEPER OPTIMIZATION

We first optimized the feedback keepers such that the keeper strength for speed is minimized, when the keeper strength for noise tolerance (that is, the gate noise-tolerant requirement) is given. Fig.3.1 shows a dynamic logic gate with the conventional feedback keeper.

I-V characteristic of the keeper circuit is very sensitive to the parameters of the transistors. The I-V characteristic of this simple keeper is very suitable for the high-performance keeper application because:

1) The I-V curves do have the folded-back property

2) When proper beta ratio and transistor threshold voltage values are chosen, the folded-back phenomenon can occur in the left half of the plot. This simulation has been studied with SPICE simulation.

The impacts of V_{DD} voltage and transistor sizing on the I-V characteristic of the circuit are shown in Fig.3.25 and Fig.3.26. It is observed that the current peak moves down when the absolute value of the V_{DD} voltage is reduced. When the relative size of the transistors is changed, it is also observed that even though the magnitude of the current changes, the shape of the I–V characteristic remains largely unchanged. Obviously, a large W/L ratio and a low V_{DD} are preferred in this application.

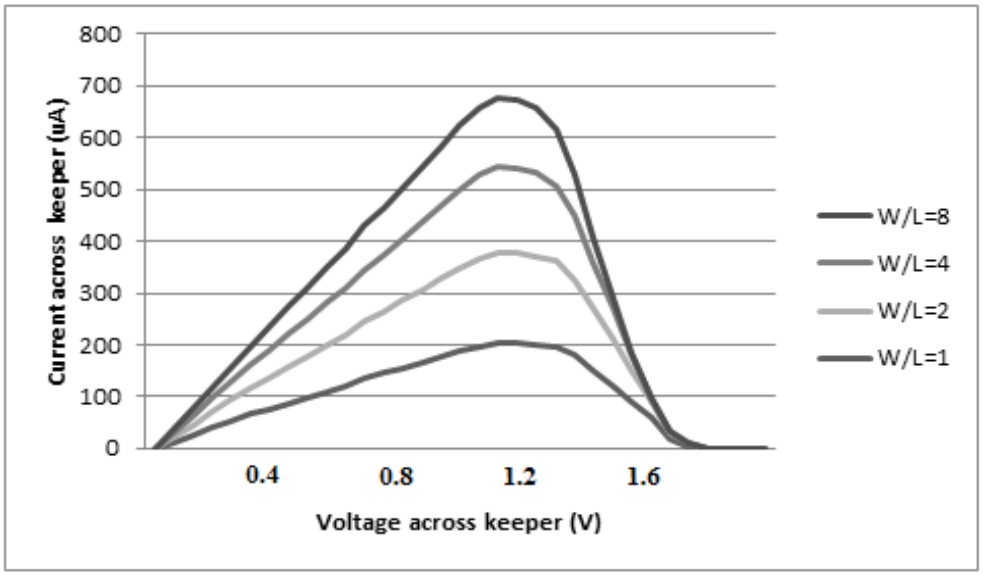


Fig.3.25 I-V characteristics of feedback keeper with different W/L ratio

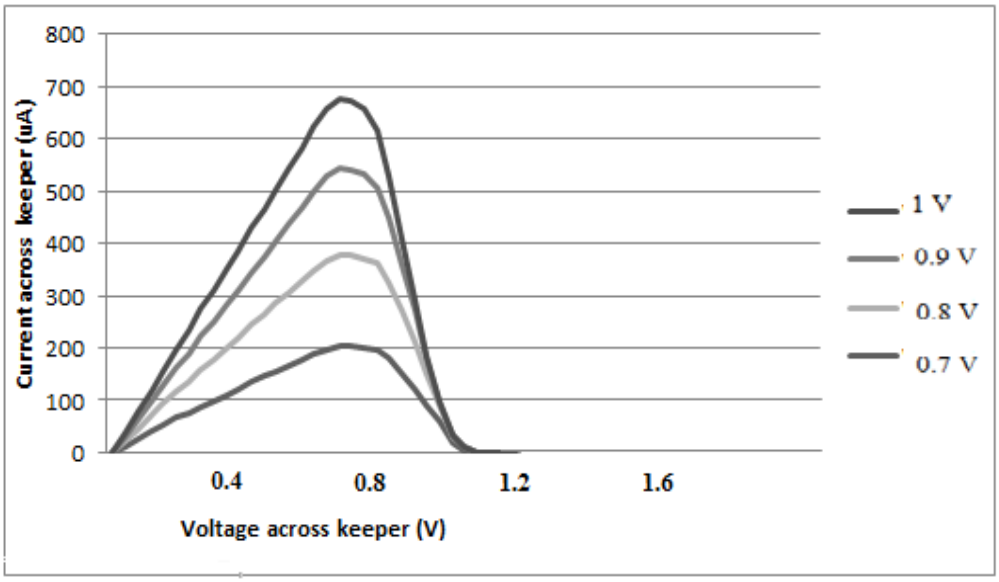


Fig.3.26 I-V characteristics of feedback keeper with different value of V_{DD}

3.9 IMPLEMENTATION OF PROPOSED LOGIC IN DIFFERENT LOGIC FUNCTIONS

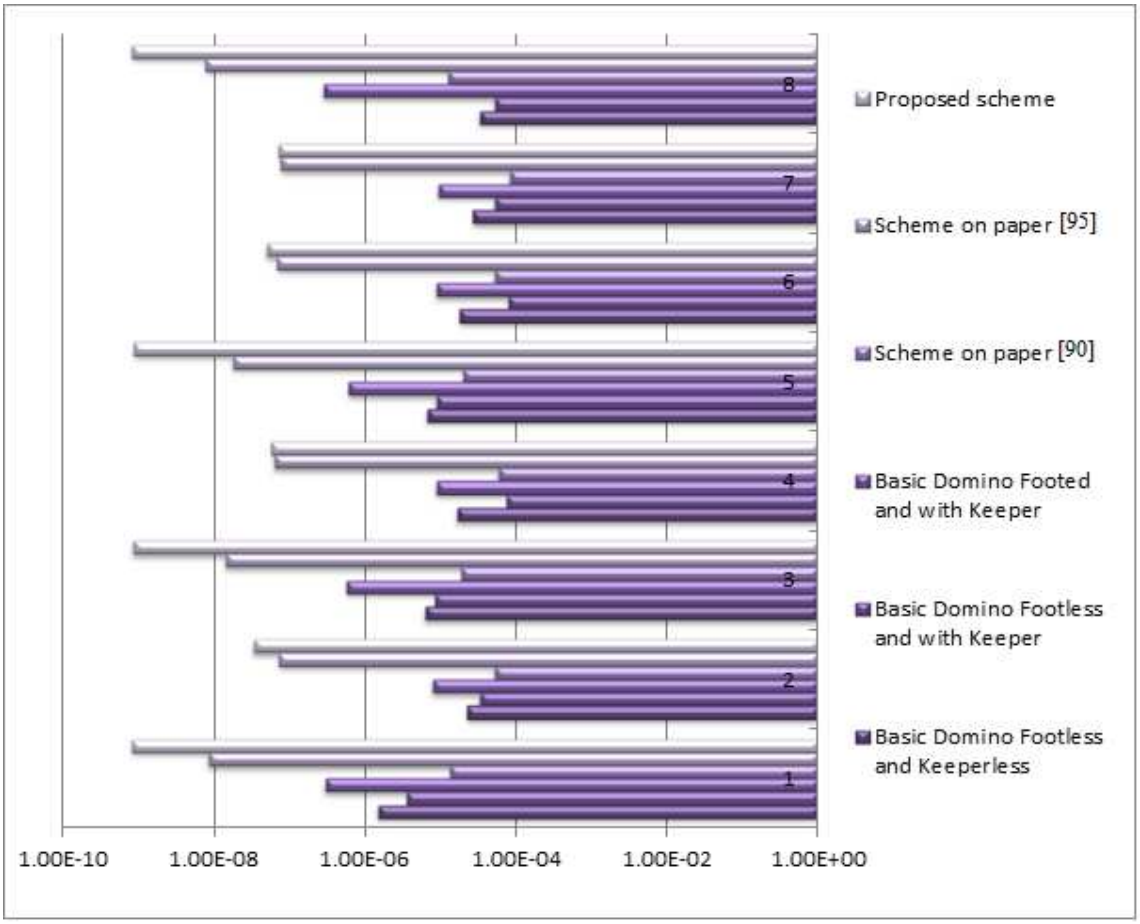


Fig.3.27 Graphical representation of power dissipation comparison with different logic function and proposed scheme

1. X = A B2. X = A + B3. X = A B C4. X = A + B + C5. X = A B C D6. X = A + B + C + D7. X = A B C + D8. X = A B + C D

With 1:1 duty ratio of the clock signal, we have calculated the power dissipated for our proposed logic. In order to validate the claimed power saving and faster circuit operation extensive simulations were performed using a set of logic as illustrated in Table 3.9 and Table 3.10. In this comparison the supply voltage was 1.8 V, clock frequency was 500MHz, load capacitance was 10pf. The results are shown in the graphical form for easy comparison in the Fig.3.27 and Fig.3.28. The X-axis of Fig.3.27 shows the power consumption and has been taken in logarithmic value. As the power consumption of the proposed scheme is least,

the power consumption bar extends more in the negative direction. Similarly in Fig.3.28 the X-axis shows the delay in logarithmic scale. The least delay of the proposed circuit spreads more in the negative direction. This experimental analysis validates that the proposed logic is more power saving and fast for other logic functions.

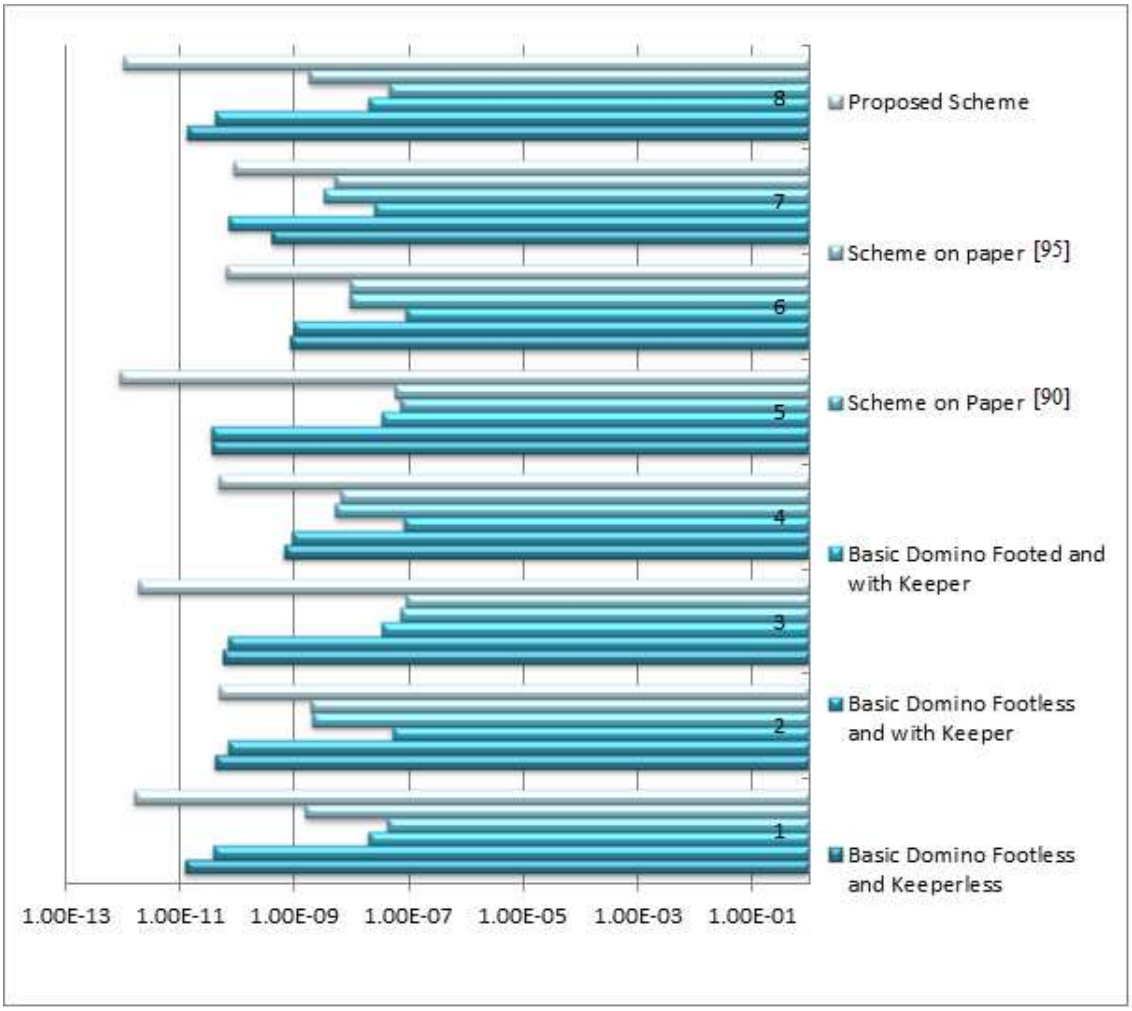


Fig.3.28 Graphical representation of circuit delay comparison with different logic functions and the proposed scheme

1. X = A B 2. X = A + B 3. X = A B C 4. X = A + B + C 5. X = A B C D 6. X = A + B + C + D 7. X = A B C + D 8. X = A B + C D

Table 3.9 Power saving comparison with different logic functions and the proposed scheme

Logic functions	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [95]	Scheme on Paper [90]	Proposed Scheme
X=AB	1.50E-06	3.67E-06	2.98E-07	1.35E-05	8.59E-09	8.41E-10
X=A+B	2.29E-05	3.29E-05	7.80E-06	5.30E-05	7.32E-08	3.32E-08
X=ABC	6.31E-06	8.53E-06	5.79E-07	1.93E-05	1.42E-08	8.49E-10
X=A+B+C	1.68E-05	7.56E-05	8.89E-06	5.83E-05	6.37E-08	5.87E-08
X=ABCD	6.56E-06	8.73E-06	6.09E-07	2.04E-05	1.79E-08	8.76E-10
X=A+B+C+D	1.79E-05	8.03E-05	8.74E-06	5.24E-05	6.86E-08	5.07E-08
X=ABC+D	2.72E-05	5.29E-05	9.30E-06	8.30E-05	7.81E-08	7.32E-08
X=AB+CD	3.29E-05	5.19E-05	2.80E-07	1.30E-05	7.82E-09	8.32E-10

Table 3.10 Circuit delay with different logic functions and the proposed scheme

Logic functions	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [95]	Scheme on Paper [90]	Proposed Scheme
X=AB	1.21E-11	3.73E-11	1.94E-08	4.28E-08	1.55E-09	1.59E-12
X=A+B	3.96E-11	6.86E-11	5.10E-08	1.98E-09	1.95E-09	4.86E-11
X=ABC	5.54E-11	6.79E-11	3.33E-08	7.27E-08	8.92E-08	1.86E-12
X=A+B+C	6.56E-10	9.26E-10	8.11E-08	5.22E-09	6.43E-09	4.70E-11
X=ABCD	3.55E-11	3.52E-11	3.39E-08	7.09E-08	5.72E-08	0.86E-12
X=A+B+C+D	8.59E-10	9.85E-10	8.81E-08	8.91E-09	9.30E-09	6.21E-11
X=ABC+D	5 96E-11	7.16E-11	2.50E-08	3.28E-09	5.05E-09	8.66E-11
X=AB+CD	1.31E-11	3.99E-11	1.93E-08	4.35E-08	1.81E-09	1.01E-12

3.10 COMPARISON IN DIFFERENT CORNER PROCESSES

3.10.1 CORNERS

Corners define differences due to process inaccuracies, temperature and other parameter variations. It is clear that simulations that take these differences into consideration will differ one from another. Corners that describe differences due to process inaccuracies (such as doping variations) are supplied with the process kit and usually are located in model library. For example the kit can include corners for: Fast NMOS Fast PMOS, Slow NMOS Slow PMOS, Fast NMOS Slow PMOS, Slow NMOS Fast PMOS and Typical NMOS Typical PMOS. There is also possibility that corners will describe IC's behavior in different temperatures and other parameter variations, such as V_{DD} variations (in this case V_{DD} has to be a variable in schematic). Each corner that will be simulated can contain one technology corner, one temperature value and one value for every other parameter. During corner simulation all available corners are simulated and thus influence of parameter variations on IC can be checked.

3.10.1.1 CORNERS ANALYSIS

In a theoretical manufacturing process, process variables can have exact values and these exact values can be used to calculate the yield for the process. However, in a real manufacturing process, process variables are subjected to a manufacturing tolerance. They fluctuate randomly around their ideal values. The combined random variation for all the components results in an uncertain yield for the circuit as a whole.

Corners analysis looks at the performance outcomes generated from the most extreme variations expected in the process, voltage and temperature values (the *corners*).

With this information, we can determine whether the circuit performance specifications can be met, even when the random process variations combine in their most unfavorable patterns.

In this corner analysis we have used our the foundry provided library files for Slow-Slow (SS), Slow-Fast (SF), Typical-Typical (TT), Fast-Slow (FS) and Fast-Fast (FF) processes.

3.10.2 PDP ANALYSIS OF THE PROPOSED CIRCUIT BY DIFFERENT CORNER PROCESSES

Fig.3.29 and Table 3.11 demonstrate that, the proposed circuit shows the best PDP performance under differences process inaccuracies, temperature and other parameter variations; this was done by corner analysis. The proposed circuit shows best result when it is compared with the different corner cases. The proposed logic shows nearly same PDP for all the corner processes. Due to less number of switching the deflection of the power and delay is less with the variation of processes like temperature, voltage and process.

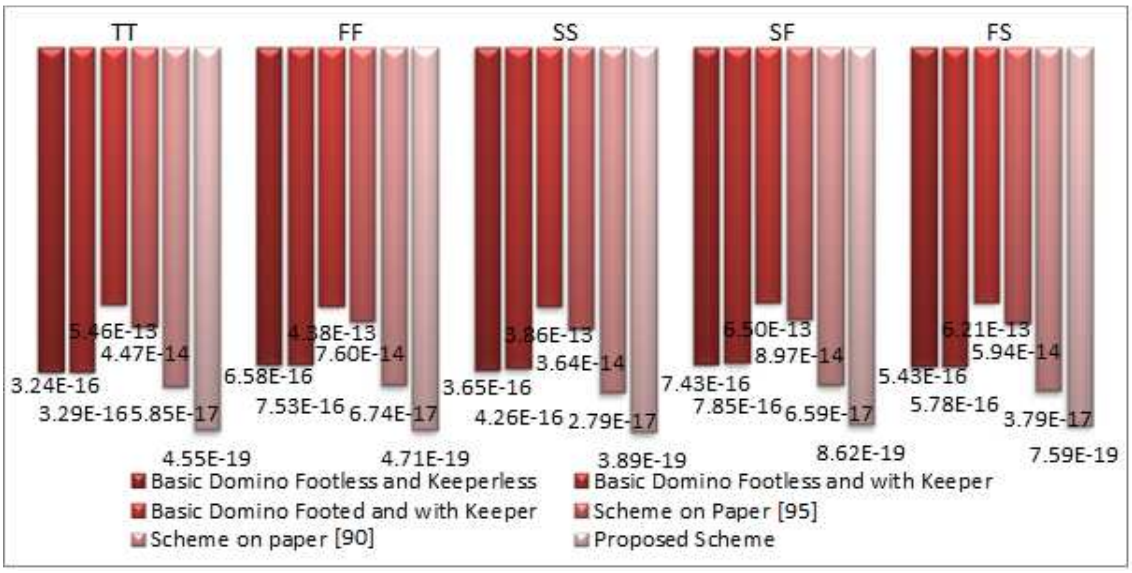


Fig.3.29 Simulated PDP output of different logic style compared with the proposed logic style in different corner Processes (Simulated with 2-input OR gate)

Table 3.11 PDP performance of different logic style compared with the proposed logic style in different corner processes (Simulated with 2-input OR gate)

P-D-P	TT	FF	SS	SF	FS
Basic Domino Footless and Keeperless	3.24E-16	6.58E-16	3.65E-16	7.43E-16	5.43E-16
Basic Domino Footless with Keeper	3.29E-16	7.53E-16	4.26E-16	7.85E-16	5.78E-16
Basic Domino Footed and Keepered	5.46E-17	4.38E-17	3.86E-17	6.50E-17	6.21E-17
Scheme on Paper [95]	4.47E-14	7.60E-14	3.64E-14	8.97E-14	5.94E-14
Scheme on Paper [90]	5.85E-17	6.74E-17	2.79E-17	6.59E-17	3.79E-17
Proposed Logic style	4.55E-19	4.71E-19	3.89E-19	8.62E-19	7.59E-19

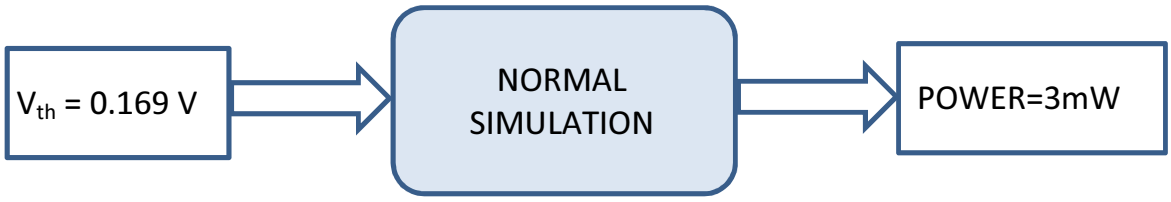
3.11 STATISTICAL ANALYSIS OF PROPOSED CIRCUIT

The manufacturing variations in components affect the production of any design that includes them. Statistical analysis permits us to study this relationship in detail. In general we can say that Monte-Carlo simulation is a technique used to understand the impact of risk in the system.

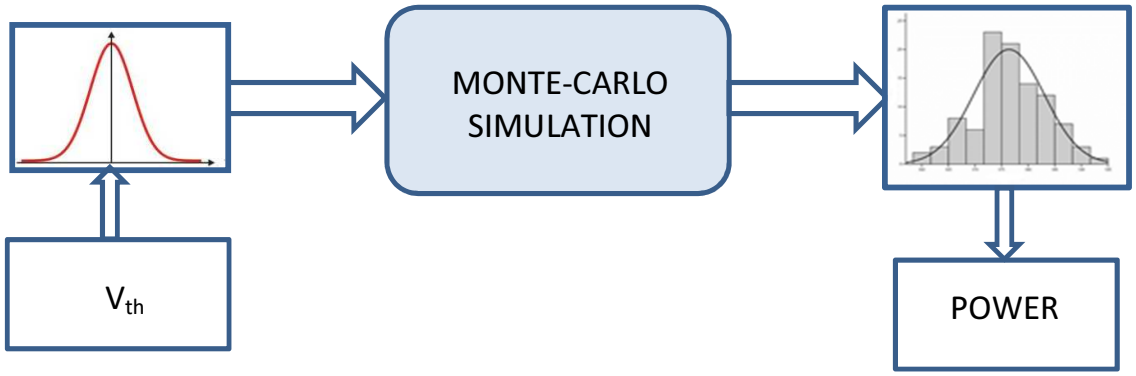
Fig.3.30 shows the difference between normal simulation and Monte-Carlo simulation means in normal simulation, we are giving fixed supply and we are getting fixed output or power but suppose supply voltage is changed because of some reason then what will be the output or power that we can analysis by Monte Carlo simulation where the shape of each statistical distribution represents the manufacturing tolerances on a device.

3.11.1 WORKING OF MONTE-CARLO SIMULATION

The manufacturing variations in components affect the production yield of any design that includes them. Statistical analysis allows you to study this relationship in detail. To prepare for a statistical analysis, we create a design that includes devices models that are assigned statistically varying parameter values. The shape of each statistical distribution shows the manufacturing tolerances on a device or devices. During the analysis, the statistical analysis option performs multiple simulations, with each simulation using different parameters values for the devices based upon the assigned statistical distributions. When the simulations finish, we may use the data analysis features of the statistical analysis option to examine how manufacturing tolerances affect the overall production yield of our design. If necessary then we may switch to different components or change the design to improve the yield [12] [13]. Fig.3.30 shows the difference between normal and Monte Carlo simulation.



(a) Normal simulation process



(b) Monte-Carlo simulation process

Fig.3.30 Difference between normal simulation and Monte-Carlo simulation

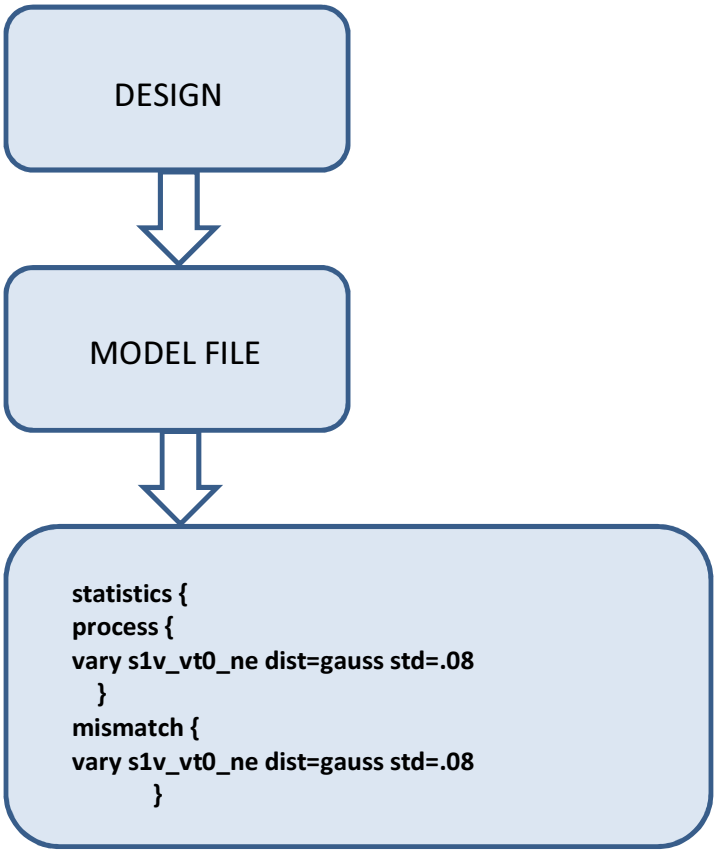


Fig. 3.31 Procedure of Monte Carlo on cadence

For Monte Carlo simulation we have to create a Design that includes devices or device models that are assigned statistically varying parameter values.

The statistics block defines how parameters vary during the analysis. In this case, each parameter has either a Gaussian or a log-normal distribution with a deviation specified by the

std. parameters. All the parameters vary when process variation is specified and four of them vary when mismatch is specified.

3.11.2 POWER DISSIPATION ANALYSIS BY MONTE-CARLO METHOD

We have simulated the histogram of the power dissipation of the proposed domino logic simulated with 2-input OR-gate and have compared it with the basic domino logic. The simulation has been done in cadence spectre using Monte-Carlo method. Fig.3.32 shows the result of power dissipation using Monte-Carlo simulation at V_{DD} = 1.8 V and N = 1000 for basic domino logic. This simulation is having mean at μ = 53 μW and standard deviation of 29.57 μW.

Fig.3.33 shows the result power dissipation using Monte-Carlo simulation process at V_{DD} = 1.8 V and N = 1000 for proposed domino logic. This simulation is having mean at μ = 55nW and standard deviation of 27.33 nW which is less than the basic domino.

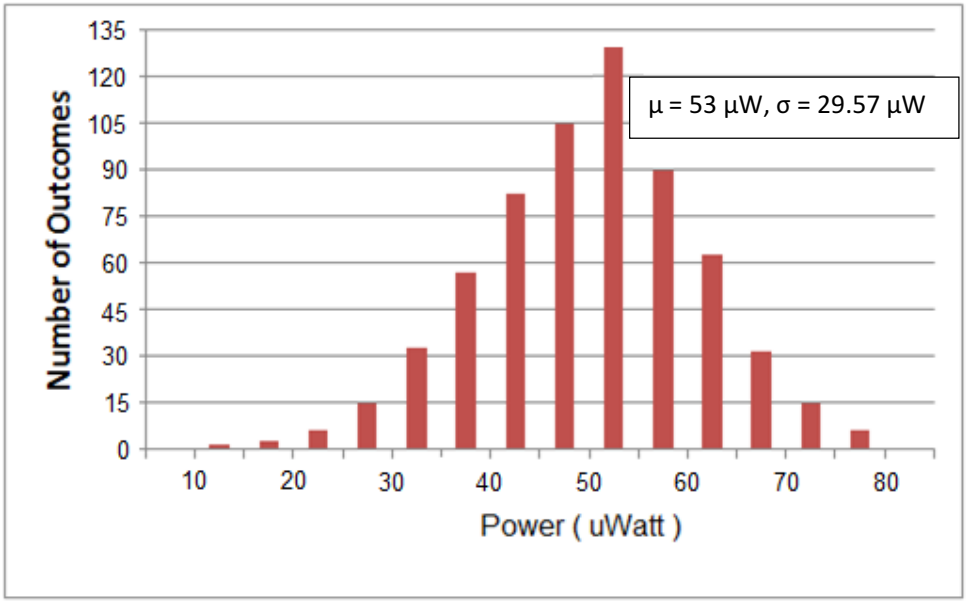


Fig.3.32 The histogram of power dissipation of basic domino logic simulated with 2-input OR-gate and 1.8 V for N = 1000

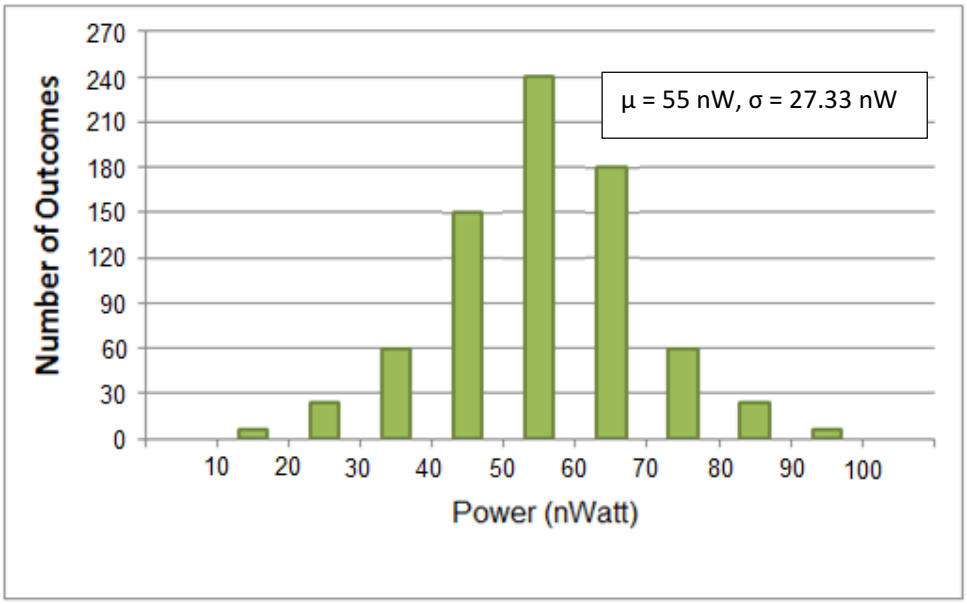


Fig.3.33 The histogram of power dissipation of proposed domino logic simulated with 2-input OR-gate and 1.8 V for N = 1000

The statistical distribution of histograms constructed for the basic domino shows a more spreaded output, whereas the statistical distribution of histograms constructed with the simulation of the proposed circuit gives a sharp waveform. This proves the stability of the circuit for a wide range of parameter values. This happened due to the reduction of noise in the circuit. This is because; the presence of noise disturbs the stability of the circuit with a small change in any parameter. For the basic domino the highest number of outcomes is 127 where in the proposed logic the highest number of outcome is 244, which is around double of the basic domino.

3.11.3 DELAY ANALYSIS BY MONTE-CARLO METHOD

We have simulated the histogram of the delay of the proposed domino logic simulated with 2-input OR-gate and compared it with the basic domino logic. The simulation has been done in cadence spectre using Monte-Carlo method. Fig.3.34 shows the result of power dissipation using Monte-Carlo simulation at V_{DD} = 1.8 V and N = 1000 for basic domino logic. Fig.3.35 shows the result power dissipation using Monte-Carlo simulation process at V_{DD} = 8 and N = 1000.

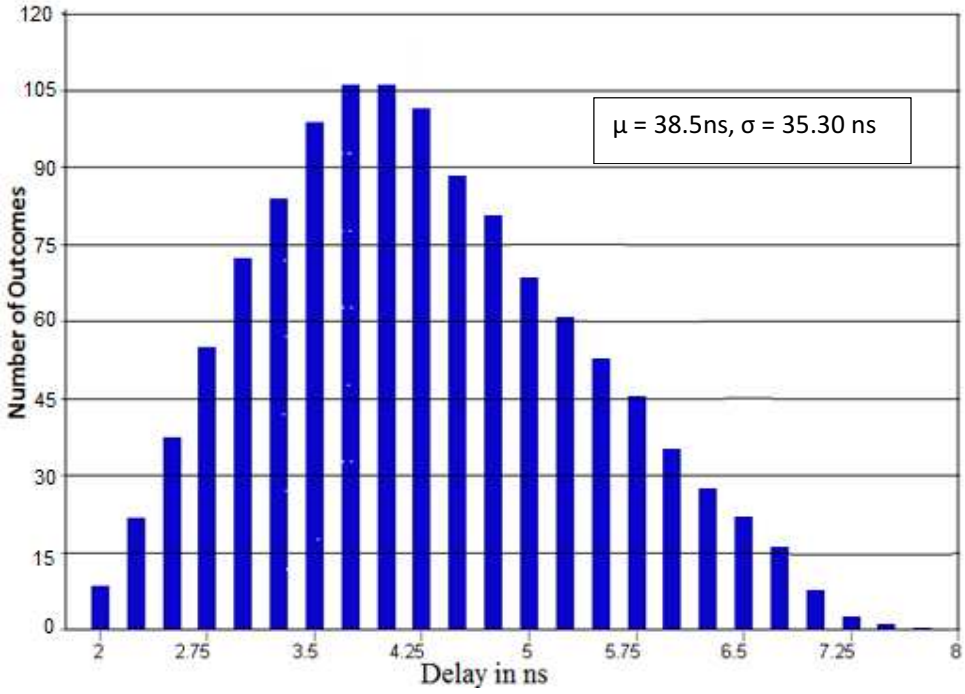


Fig.3.34 The histogram of delay of basic domino logic simulated with 2-input OR-gate and 1.8 V for N = 1000

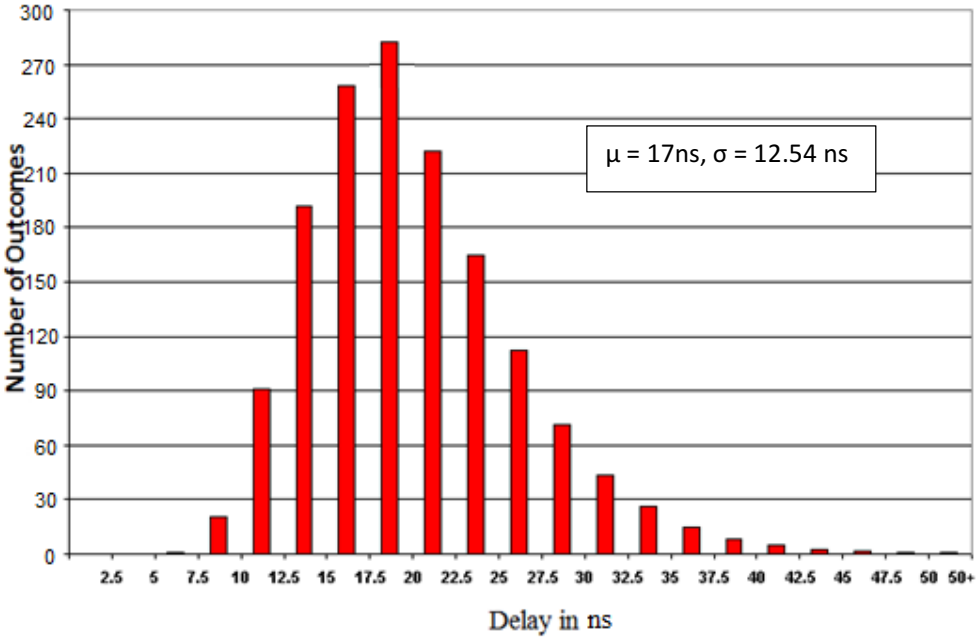


Fig.3.35 The histogram of delay of proposed domino logic simulated with 2-input OR-gate and 1.8 V for N = 1000

Like the power dissipation output, the statistical distribution of histograms constructed for the basic domino shows a spreaded output, whereas the statistical distribution of histograms constructed with the simulation of the proposed circuit gives a sharp waveform. This proves the stability of the circuit for a wide range of parameter values. This happened due to the reduction in switching of the circuit in the output node. Due to the minimization of switching the time of simulation decreases. Reduction in switching also decreases the noise of the proposed circuit. The highest number of outcomes for the basic domino is 107 where in the proposed logic the highest number of outcome is 280, which is 161% more from the basic domino. The output of basic domino is having mean at μ = 38.5 ns and standard deviation of 35.30 ns. The output of proposed domino is having mean at μ = 17 ns and standard deviation of 12.54 ns.

3.11.4 POWER DISSIPATION VS. DELAY WITH MONTE-CARLO SIMULATION

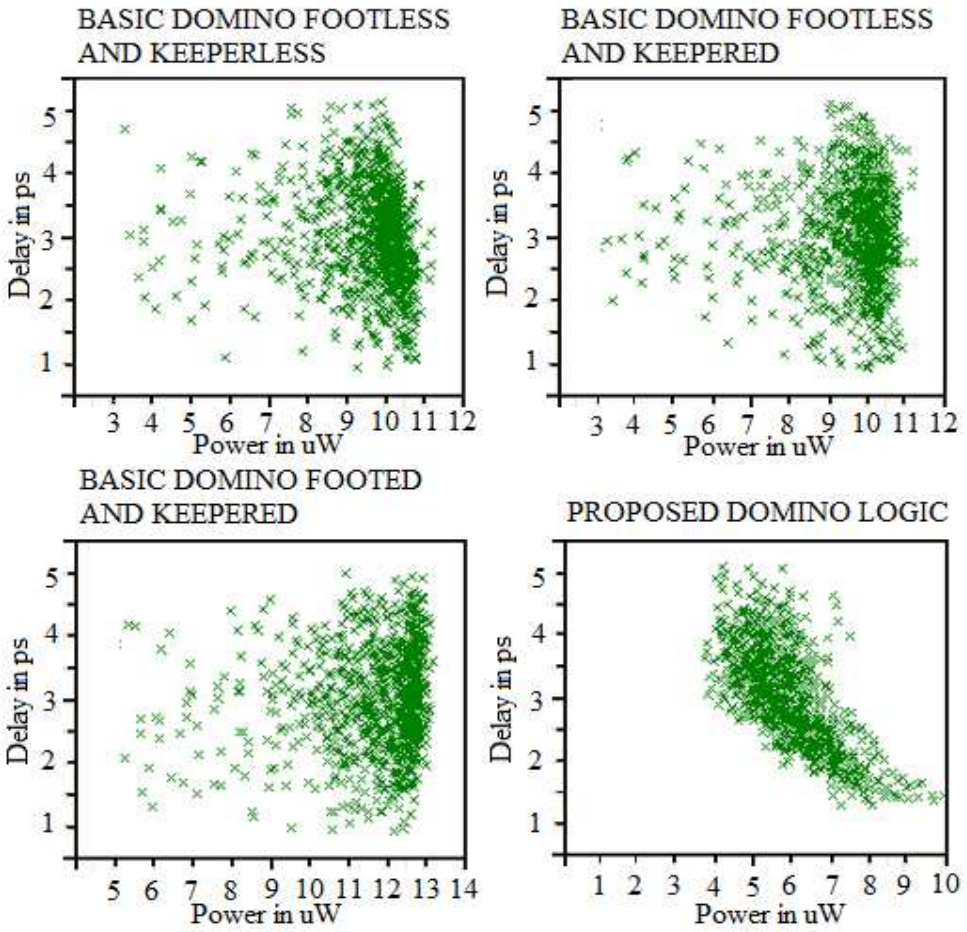


Fig.3.36 The scattered output of power dissipation Vs. Delay for basic domino logics and proposed domino logic simulated with 2- input OR - gate and 1.8 V for N = 10000

Fig.3.36 shows the scattered output of power dissipation vs delay for basic domino logics and proposed domino logic. This simulation was done using 2 – input OR gate as a vehicle. All these circuits were simulated in same environment at a temperature of 27^0 C, 1.8 V 500 MHz frequency and N = 10000.

The output has power in X – axis and delay in Y – axis with number of runs = 10000. It can be observed from the output that in proposed circuit the deviation of the output is less as for 10000 numbers of simulations. The output points of the proposed circuit are concentrated at a place, which results towards great performance of the circuit. On the other hand, the output of the basic circuits gives a scattered output.

3.12 SEQUENTIAL CIRCUIT IMPLEMENTATION USING PROPOSED LOGIC

3.12.1 BASIC CMOS FLIP-FLOP

The node X is precharged to V_{DD} when Clk = 0. The cascaded inverter generates a very narrow pulse at every rising edge of the Clk. If D = 1, then node X discharge through series connected of three transistors driving Q to 1. If D remains 1, node X will be discharged at every rising edge of the Clk. This leads to larger switching power. When D=0, node X remains at 1 driving Q to 0. Fig.3.37 depicts the basic CMOS flip-flip [118].

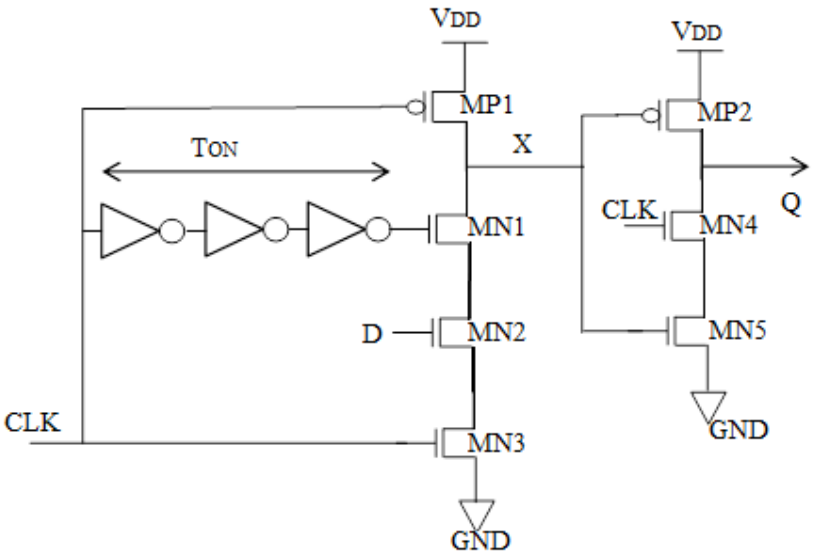


Fig.3.37 Basic dynamic FF [118]

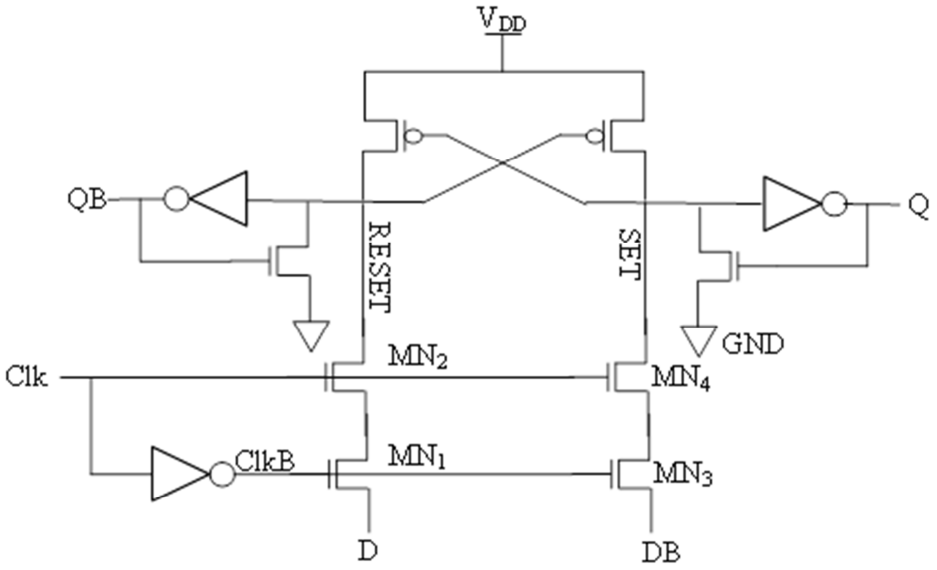


Fig.3.38 SDER FF [119]

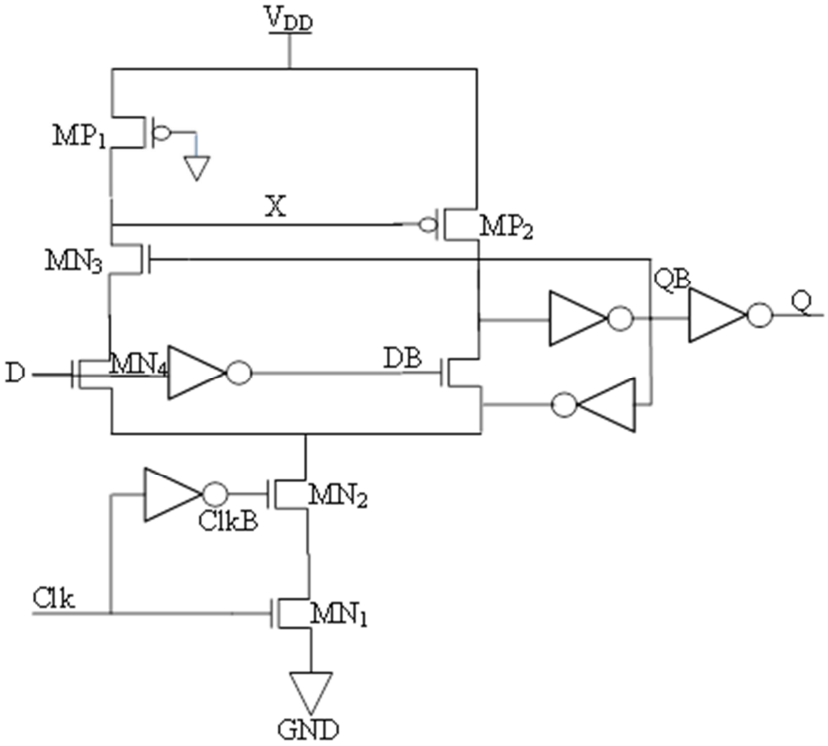


Fig.3.39 SCCER FF [119]

3.12.2 SDER FLIP-FLOP

The input data (D) and its inverted output (DB) applied to MN_1, MN_3 respectively. The clock signal (Clk) and its inverted output (ClkB) generates an implicit conducting pulse at every rising edge of Clk. Clk and ClkB applied to MN_2, MN_4 and MN_1, MN_3 respectively.

At rising edge of Clk all these transistor starts conducting for a short duration of time determined by delay of inverter and allows D & DB to reach at RESET & SET node. Q and QB retain the previous values till the next rising edge of Clk. This flip-flop is called as static because SET and RESET nodes retains the state of the flip-flop without being precharged. If the input data remains idle no internal switching occurs at SET and RESET node results in low power consumption at low data switching activity. Fig.3.38 depicts the SDER flip-flop [119].

3.12.3 SCCER FLIP-FLOP

A weak pull up transistor MP_1 is used to charge the node X to V_{DD}. The clock signals (Clk) and its inverted output (ClkB) generates an implicit conducting pulse at every rising edge of Clk allowing MN_1& MN_2 to conduct. MN_3 controlled by QB provides a conditional discharging path for node X. Since MN_3 controlled by QB, no discharge occurs at node X as long as D remains HIGH, results in low power consumption. The worst case, timing of this design occurs if D=1 and node X discharges through four transistors connected in series. This requires a wider MN_1& MN_2 for proper discharging of node X. Fig.3.39 shows the SCCER flip-flop [119].

3.12.4 PROPOSED FF

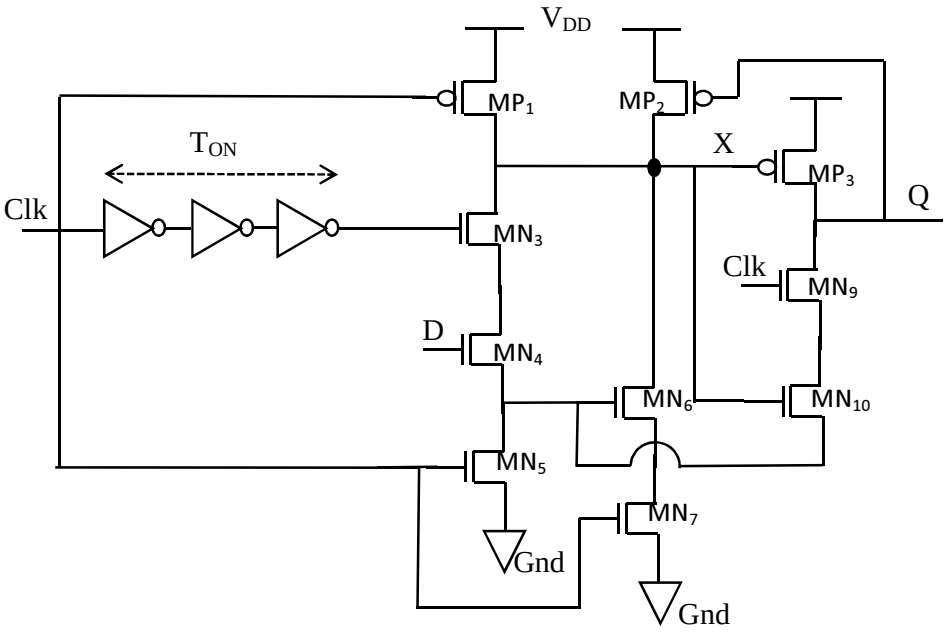


Fig.3.40 Proposed FF

The proposed FF uses the proposed logic of this thesis as depicted in Fig.3.40. It modifies the basic FF in the way that described in this thesis. The proposed FF has a precharge PMOS MP_1, a keeper PMOS MP_2. NMOS MN_3 inputs the delayed clock and NMOS MN_4 inputs D. MP_1 and MN_5 input the Clk, where MN_5 acts as the stack transistor. At the evaluation phase, when the PDN is conducting, at that time M_5 stops the free discharge of dynamic node voltage to evaluate logic 0 at the dynamic node. To compansate that MN_6 makes a charge discharge path. Here MN_7 again acts as a stack for the 2^{nd} path to maintain the dynamic node. Hence circuit becomes extra noise robust and reduces the leakage power consumption. This can be increased by widening the MP_2 (high W/L) to make it more conducting.

M_{10} should be grounded according to the basic circuit technique has connected to the N_FOOT in the proposed flip-flop. By doing this, the continuous switching activity of the N_FOOT does not pass to the output node. This reduces the power consumption and noise of the circuit. As the output does not switch many time, the circuit delay also becomes less and circuit gets fast.

When Clk=0, the node X or the dynamic node is gets precharged to V_{DD}. The cascaded inverter, which inputs to MN_3, generates a very narrow pulse at every rising edge of the Clk.

When D=1, then node X i.e. The dynamic node discharge through series connected of three transistors MN_3, MN_4 and MN_5 driving X to 0 and output node i.e. Q to 1. If D remains 1, node X will be discharged at every rising edge of the Clk. This leads to larger switching power.

When D=0, node X remains at 1 driving Q to 0. These conditions satisfy the conditions of D-FF.

3.12.5 SIMULATION RESULT FOR PROPOSED FF

All the flip-flops were designed using UMC 180 nm process technology using 1.8 V supply voltage. The designs were simulated at a temperature of 27^0 centigrade and clock frequency of 500 MHz. A load capacitance of 30 fF was used for all outputs. Fig.3.41 illustrates the timing definitions for the flip-flops. Delay was measured with 50% of the signal transitions. Setup time is defined as the time from when data becomes stable to the

rising transition of the clock. Hold time is defined as the time from the rising transition of the clock to the earliest time that data may change after being sample. Setup and hold times are measured with reference to the 50% of rising transition of the clock. Table 3.12 and Fig.3.42 compare the power, delay and PDP of all the FFs.

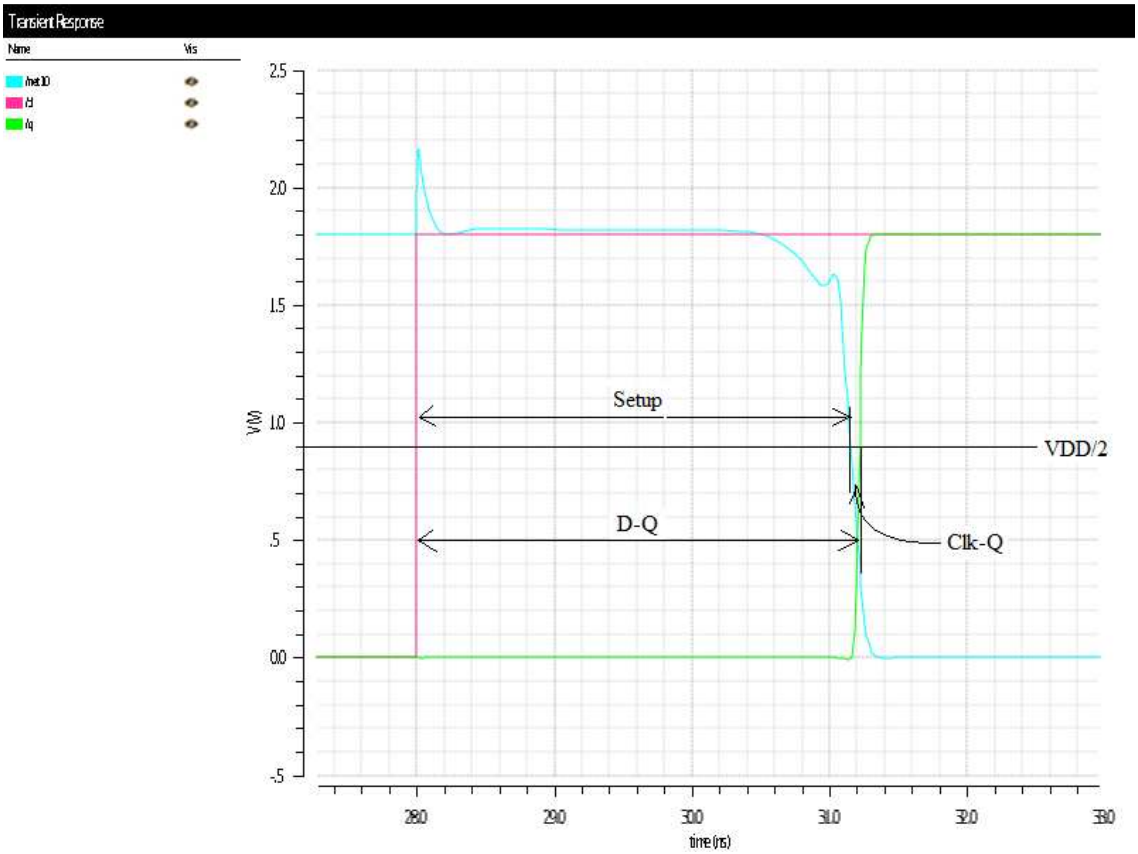
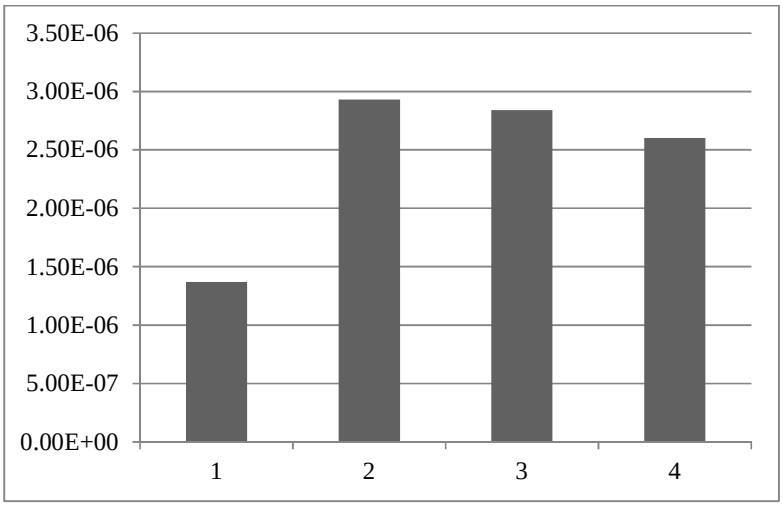


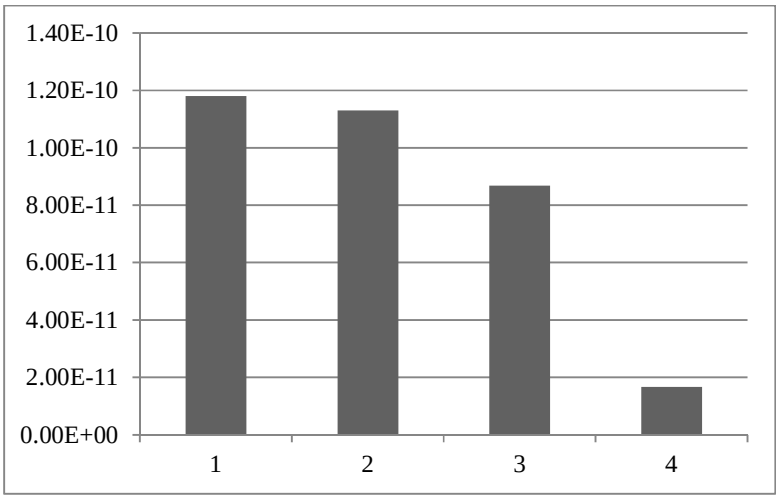
Fig.3.41 Proposed FF output illustrating timing definitions

3.12.6 SIMULATION RESULTS AND COMPARISON OF PROPOSED FF WITH OTHER FFS

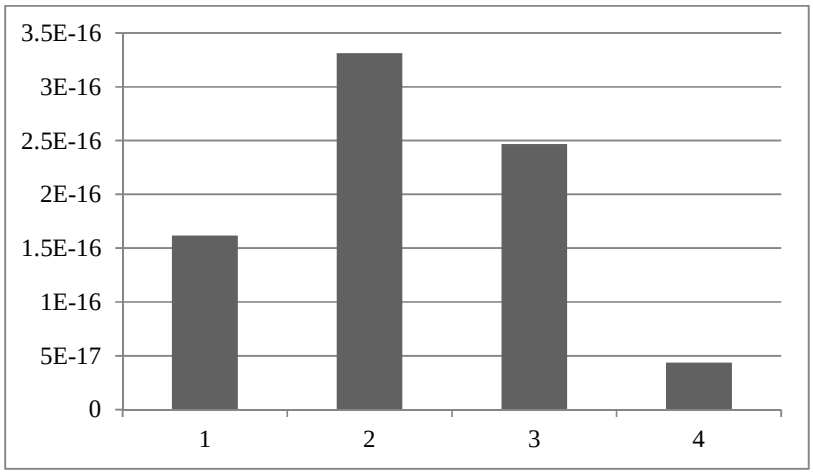
The proposed flip-flop was compared with the other flip-flops. An ideal clock was used for individual flip-flop simulations. Fig.3.43 depicts the Clk-Q (clock-to-output) delay versus setup time for all the flip-flops and Fig.3.44 shows D-Q (data-to-output) delay versus setup time for all the flip-flops. It can be clearly seen that the delay outputs of the previous proposed flip-flops were much more than that of the proposed flip-flop. These outputs give a clear illustration of the behavior of the proposed flip-flops in the minimum delay region.



Power Comparison



Delay Comparison



PDP Comparison

1. Basic FF 2. SDER FF 3.SCCER FF 4. Proposed FF

Fig.3.42 Power, delay and PDP comparison of all FFs

Table 3.12 Power, delay and PDP comparison of all the flip-flops

PARAMETERS	POWER (W)	DELAY (S)	POWER_DELAY PRODUCT
BASIC FF	1.37E-06	1.18E-10	1.6166E-16
SDER FF	2.93E-06	1.13E-10	3.3109E-16
SCCER FF	2.84E-06	8.69E-11	2.468E-16
PROPOSED FF	2.60E-06	1.67E-11	4.342E-17

For any flip-flop, there is a specific setup time which results in a minimum D-Q delay. This optimum setup time is used in this paper for the comparison of setup time. As shown in the graph of Fig.3.43 the Clk-Q delay becomes independent of setup time for more setup times. The proposed flip-flop has lowest Clk-Q delay and D-Q delay in comparison to all the previous proposed flip-flops. Among all other flip-flops SCCER FF has lowest D-Q delay and SDER has lowest Clk-Q delay.

Fig.3.45 shows the power as a function of data switching activity for all the flip-flops. Proposed FF has lowest power consumption for data switching activity less than 50%. For more than 50 % of data switching activity basic FF consumes lowest power. This is due to the fact that at higher switching activity there is a less opportunity of energy saving.

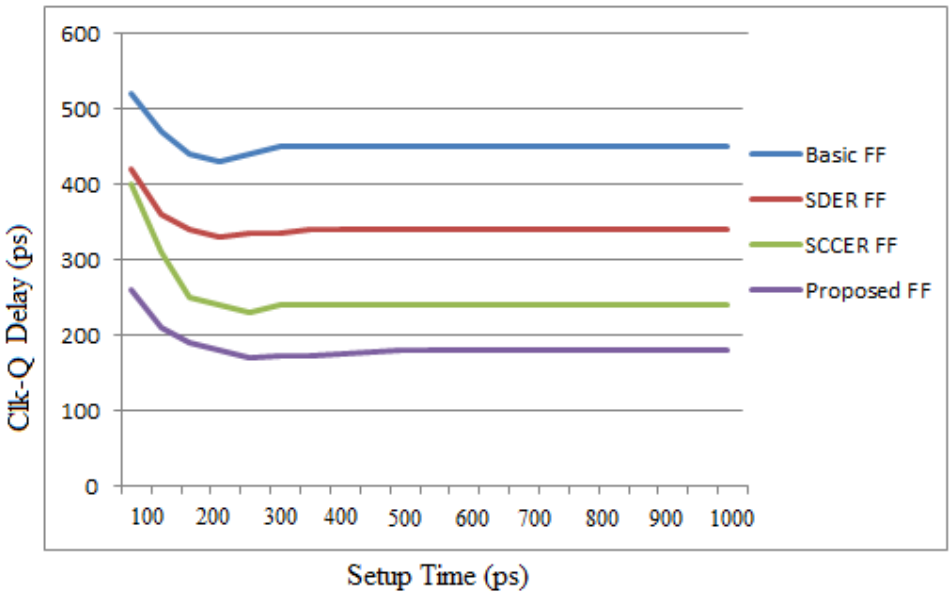


Fig.3.43 Clk-Q Delay Vs Setup Time

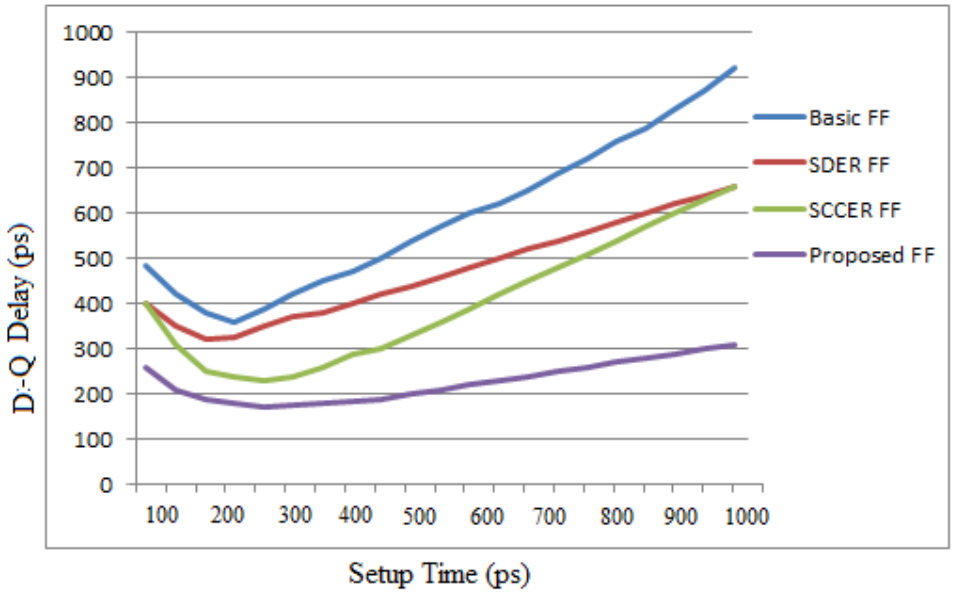


Fig.3.44 D-Q Delay Vs Setup Time

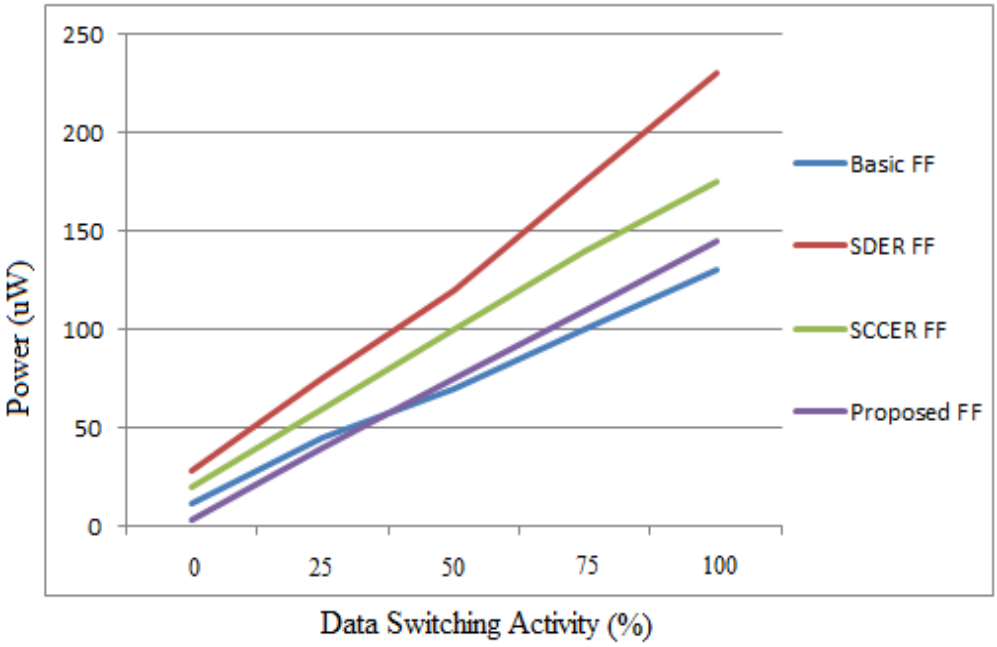


Fig.3.45 Power Vs Data Switching Activity at 50 MHz

3.13 CONCLUSION

In this chapter we have presented a new domino logic style and analysed this logic in various ways. This logic style is simulated and compared with the basic domino logic styles and also some previous proposed logic styles. All the logics were simulated and compared in the same environment and found that the performance of the proposed logic is very good as

compared to other logic styles. As previously discussed, it becomes harder to use dynamic logic as technology because of its noise. This proposed logic style increases the speed and reduces the power consumption of the circuit due to its less switching activity at the output. This virtual domino logic style also show advantages when implemented in different arithmetic circuits and also in sequential logic circuits. This proposed domino logic style is an ideal technology to reduce noise which has been discussed in the next chapter.

Chapter 4

NOISE ANALYSIS

4.1 INTRODUCTION

Noise is unwanted electrical or electromagnetic energy that degrades the quality of signals and data. Noise occurs in digital and analog systems, and can affect files and communications of all types, including text, programs, images, audio, and telemetry. [120]

Noise in a dynamic logic is defined as a pulse or glitch that appears at the inputs of dynamic gates. In CMOS dynamic logic the dynamic node gets charged at the precharge phase. Noise pulse discharges the dynamic node unwantedly [84]. Continuous scaling in CMOS technology and increase in circuit complexity now a days are making the role of noise in digital circuits more important [70] [121] [98] [84] [12] [122] [123] [112] [17]. The main reason for its importance is,

1. Scaling of threshold voltages
2. Increasing interconnect densities
3. High frequency of operation

Noise is used to describe a phenomenon that results voltage at non switching node to diverge from its nominal value [121]. Noise has always been a major issue for all analog circuits. The reason behind the popularity of digital systems as compared to analog system is the noise immunity in digital circuits. In the progress of advanced VLSI technology, noise tolerance in CMOS digital dynamic circuits is becoming a major issue. Additionally, with the continuous scaling of CMOS technologies, signal integrity and noise issues have become a metric of equivalent importance to power, performance and area. Static CMOS circuits can

achieve highest noise margin because at steady state output nodes are always connected to either V_{DD} or GND, but this is not possible in dynamic circuits due to possibilities of floating nodes, which makes dynamic circuit more susceptible to noise. If a dynamic node stores its value relatively for a long time, noise current can discharge the capacitor responsible for holding logic level at dynamic node leading to functional failure. Therefore, analysis of effect of noise in dynamic circuits is very important.

4.2 SOURCES OF NOISE IN DOMINO CMOS LOGIC CIRCUITS

In CMOS dynamic logic circuits sources of noise can be classified broadly into 2 basic categories:

4.2.1 INTERNAL GATE NOISES

Charge sharing noise - Charge sharing noise is produced by the redistribution of charge among the dynamic node and internal nodes of the pull-down network. Redistribution of charge causes the reduction of the voltage level. This reduction in voltage at the dynamic node causes change in output logic of the circuit**.**

Leakage noise – Charge loss due to subthreshold leakage current in the evaluation phase is referred as leakage noise. The exponentially of the circuit with respect to threshold voltage of transistor increases, which is constantly scaled-down as the V_{DD} decreases. Thus, leakage in transistors proves to be a very big source of noise in wide CMOS dynamic logic gates.

4.2.2 EXTERNAL NOISES

Input noise- Input noise is the noise, which is present at the inputs of a logic gate. These are produced by coupling effect of the logic gates. This noise is also known as crosstalk. This type of noise proved to be the vital source of failure for deep submicron VLSI circuits.

Power noise and ground noise- Parasitic resistance and inductance are present in the power and ground network of the chip package. This parasitic resistance and inductance are the cause of the power and ground noise. The chip package also contains chip pins. Presence of chip pins in the chip package increases the power and ground noise. This power and ground voltage mismatch between a driver gate and a receiver gate get translated to a dc noise at the input.

Substrate noise- The signal integrity of a logic gate through substrate coupling in a circuit can be affected by substrate noise. Also, noise in the substrate can lower the threshold voltage of the transistors in the PDN as threshold voltage of the transistor is a function of the substrate voltage.

Besides all these types of noises, alpha particle radiation can be dangerous for the correct functioning of very deep submicron CMOS domino logic circuits.

4.3 OR GATE IMPLEMENTATION IN PROPOSED DOMINO LOGIC

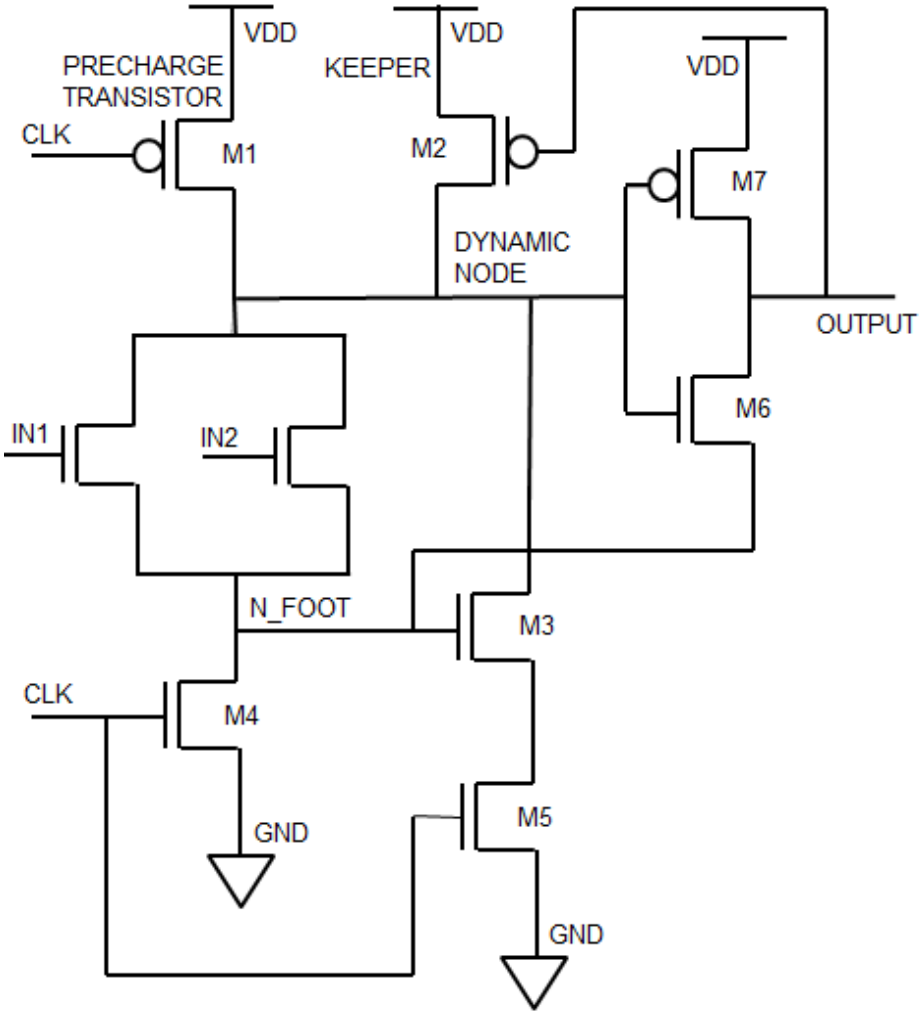


Fig.4.1 Novel 2-input OR gate designed with the proposed domino logic

4.3.1 DESCRIPTION

In the CMOS domino logic style, worst case scenario arises with OR gate, as there is no stacking transistor in the PDN designed with the conventional domino logic. Hereby, the novel OR gate is designed using the proposed logic in Fig.4.1. The PDN comprises of two NMOS transistors supplied with the inputs IN_1 and IN_2 respectively and are connected in parallel resulting in an OR gate. This circuit in a whole comprises of a precharge transistor M_1, an evaluation network connected in parallel evaluating two input OR, a keeper transistor M_2, footer transistors M_3, M_4 and M_5 and a inverter comprising M_6 and M_7.

In the precharge phase, when the clock is at LOW, at that time pre-charging PMOS M_1 gets ON (starts conducting) and the dynamic node is connected to the V_{DD} and gets precharged to V_{DD}. At the rising edge of clock i.e. in the evaluation phase, M_1 gets OFF (stops conducting) and the dynamic node gets evaluated with the pull-down network. While evaluating an OR gate, the dynamic node conditionally gets discharged ie. if any one of the input is at logic 1. At the evaluation period when all the inputs are at logic 0, the dynamic node becomes at logic 1. But due to the subthreshold leakage, NMOS pull-down network leaks the charge stored at the dynamic node capacitance. This leakage is again compensated by the PMOS keeper transistor M_2, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at gate input, the keeper may not be able to restore the voltage level of the dynamic node. To stop that the footers M_3, M_4 and M_5 are connected. M_4 acts as stack transistor. At the evaluation phase when the PDN is at logic 1, at that time M_4 stops the free discharge of dynamic node voltage to evaluate logic 0 at the dynamic node. To compansate that M_3 makes a charge discharge path. Here M_5 again acts as a stack for the 2^{nd} path to maintain the dynamic node.

To measure the robustness of the circuit, in the evaluation phase similar noise pulses were applied to every input and the noise amplitude at the output was measured as depicted in Fig.4.3. In this type of measurement, the amplitude of the output noise is observed for different amplitudes of the input noise keeping the duration of the input noise pulse constant. The noise pulse duration was kept at 30 ps (which is the typical gate delay of 180-nm technology). In this section, we have used two noise performance matrices UNG (Unity Noise Gain) and ANTE (Average Noise Threshold Energy). A pulse of noise have been used to simulate cross-talk noise at the input. The effective noise of a circuit depends on both the

duration and amplitude of the input noise. Here, we have changed the input noise level by changing the amplitude of the noise pulse.

4.4 NOISE TOLERANCE PERFORMANCE

Noise tolerance performance of the circuit can be measured in two ways for the proposed circuit.

1. UNG (Unity Noise Gain)
2. ANTE (Average Noise Threshold Energy)

For measuring UNG and ANTE for the proposed circuit, first we have to add a noise injection circuit (NIC) to the circuit to inject noise. This will let to find out the unity noise gain (UNG) and average noise threshold energy (ANTE) and compare the same with other circuits.

4.4.1 NOISE INJECTION CIRCUIT (NIC)

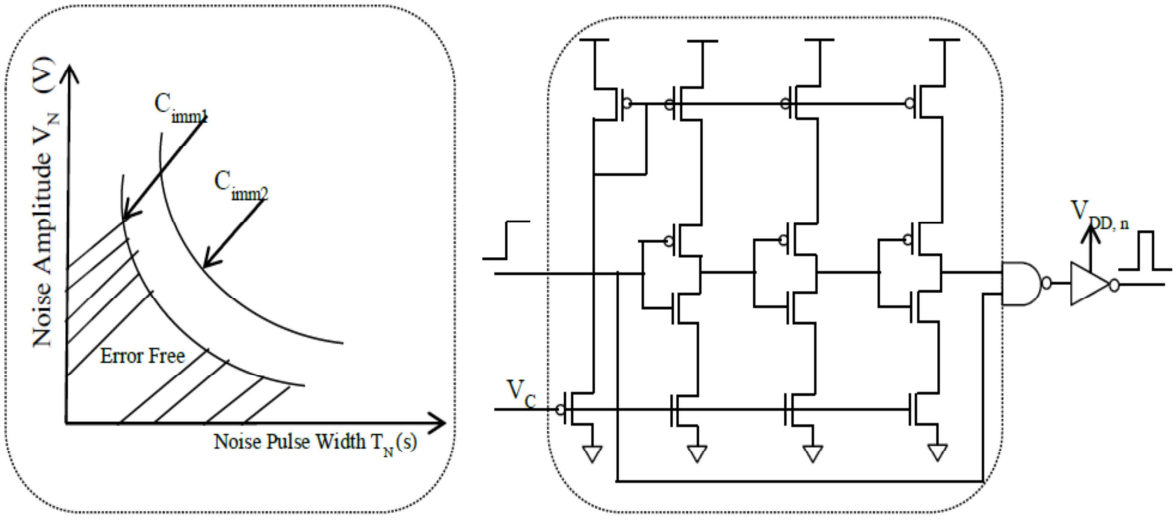


Fig.4.2 (a) Noise immunity curve [124] (b) NIC [87]

For finding the noise immunity of domino CMOS circuits noise pulses are inserted to the input of the circuits. Generally NIC circuit [125] is used to inject noise pulses of desired amplitude (V_N) and width (T_N) at the input of various logic gates as shown in Fig.4.2 (b). NIC are distributed throughout the chip to inject noise pulses. The NIC circuit is issued to create a glitch at the output of the given circuit by changing its inputs in time. The noise pulse of desired width (T_N) produced by NIC is controlled by V_C and the amplitude of noise pulse

(V_N) is controlled by the supply voltage of final inverter $V_{DD.n}$. so by varying V_C and $V_{DD.n}$ various amount of noise can be injected at the input of logic gates.

4.5 UNITY NOISE GAIN (UNG)

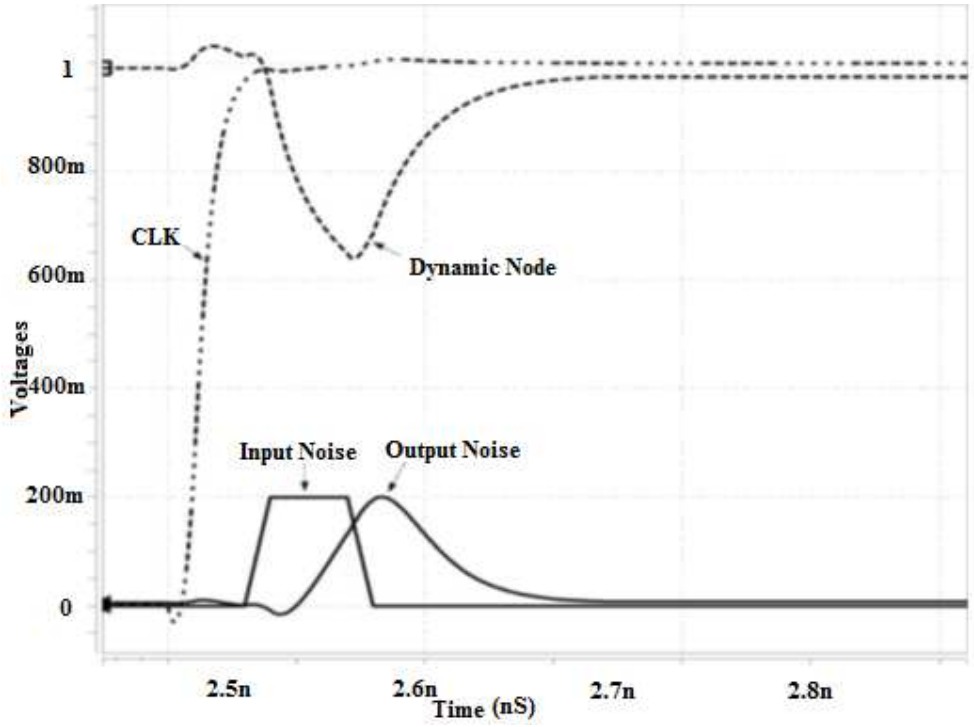


Fig.4.3 UNG-delay curves for domino 2-input OR gates

Unity noise gain is a method of leakage measurement of the circuit. To measure the robustness of the circuit, in the evaluation phase similar noise pulses were applied to every input of OR gate and amplitude of the noise at the output of the OR gates was measured as shown in Fig.4.3. Here, the amplitude of the output noise is detected for different amplitudes of the input noise keeping the width of the input noise pulse constant. The noise pulse duration was kept at 30 ps (which is the typical gate delay of 180-nm technology). Unity noise gain (UNG) is defined as the amplitude of the input noise which can cause the same amplitude of noise at the output [102]. A pulse noise have been used to simulate cross-talk noise at the input. The effective noise of a circuit depends on both the duration and amplitude of the input noise. Here, we have changed the input noise level by changing the amplitude of the noise pulse.

$$UNG = \{V_{noise}; V_{noise} = V_{out}\}$$

Fig.4.4 shows UNG histogram for all the dynamic OR gates, where the UNG of the OR gate designed with proposed logic was compared with the UNG of OR gate designed with the other basic styles simulated in the same environment. Table 4.1 figures out the same UNG comparison where UNG is normalizes to 1 V. The proposed logic shows considerably higher noise tolerance when compared with the basic domino logic, keepered and footed domino logic gates. In higher fan-in gates, there is a high UNG degradation. As the fan-in increases the UNG falls down. The proposed domino gives a better UNG performance because of its less number of switching at the output. The degradation slope of proposed circuit is very less as compared to other standard domino logic gate. This happens because there is a voltage drop through the footer transistors M_3, M_4 of the proposed circuit method as shown in Fig.4.1. Voltage drop in the footer transistor increases the gate switching voltage for this circuit. This gate switching voltage increases the noise immunity of the circuit. So, the circuit also possesses noise immunity in high fan-in.

Table 4.2 presents the UNG ratio for different fan-in of OR gates under the same Condition. In that table it can be seen that, the new technique beats all the previous proposed schemes. As compared to reference [90], which is the best competitor, the unity noise gain achieves at least 10% higher.

Table 4.1 UNG of the proposed domino logic compared to other basic domino logic styles under Same Delay (UNG Numbers Normalized to V = 1V)

Number of fan-in	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Proposed Scheme
2	390	436	567	856
4	372	409	530	851
8	347	376	493	849
16	310	332	448	842
32	285	301	426	840

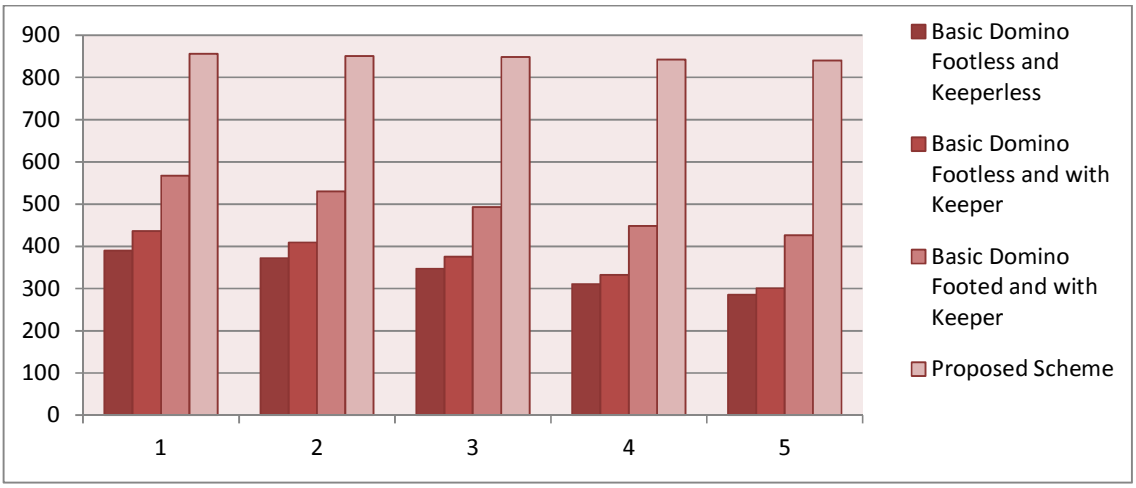


Fig.4.4 UNG comparison in case of different fan-in for wide dynamic OR gates

Table 4.2 UNG ratio for Different fan-in of OR gates under the same Condition

	UNG Comparison	**UNG Ratio**
Fan-in 2		
proposed/Basic Domino Footless and Keeperless	856/390	2.19/1
proposed/Basic Domino Footless and with Keeper	856/436	1.96/1
proposed/Basic Domino Footed and with Keeper	856/567	1.50/1
proposed/Scheme on Paper [95]	856/660	1.29/1
proposed/Scheme on Paper [90]	856/766	1.11/1

	UNG Comparison	**UNG Ratio**
Fan-in 4		
proposed/ Basic Domino Footless and Keeperless	851/372	2.28/1
proposed/Basic Domino Footless and with Keeper	851/409	2.08/1
proposed/Basic Domino Footed and with Keeper	851/530	1.60/1
proposed/Scheme on Paper [95]	851/667	1.27/1
proposed/Scheme on Paper [90]	851/771	1.10/1

	UNG Comparison	UNG Ratio
Fan-in 8		
proposed/ Basic Domino Footless and Keeperless	849/347	2.44/1
proposed/Basic Domino Footless and with Keeper	849/376	2.25/1
proposed/Basic Domino Footed and with Keeper	849/493	1.72/1
proposed/Scheme on Paper [95]	849/650	1.30/1
proposed/Scheme on Paper [90]	849/758	1.12/1

	UNG Comparison	UNG Ratio
Fan-in 16		
proposed/ Basic Domino Footless and Keeperless	842/310	2.71/1
proposed/Basic Domino Footless and with Keeper	842/321	2.62/1
proposed/Basic Domino Footed and with Keeper	842/448	1.87/1
proposed/Scheme on Paper [95]	842/640	1.31/1
proposed/Scheme on Paper [90]	842/741	1.13/1

	UNG Comparison	UNG Ratio
Fan-in 32		
proposed/ Basic Domino Footless and Keeperless	840/285	2.94/1
proposed/Basic Domino Footless and with Keeper	840/301	2.79/1
proposed/Basic Domino Footed and with Keeper	840/426	1.97/1
proposed/Scheme on Paper [95]	840/633	1.26/1
proposed/Scheme on Paper [90]	840/725	1.15/1

4.5.1 UNG COMPARISON UNDER DIFFERENT CORNER PROCESSES

Table 4.3 UNG ratio for Different fan-in of OR gates under the same Condition

	UNG Comparison	**UNG Ratio**
TT 250^0 C		
proposed/ Basic Domino Footless and Keeperless	850/392	2.16/1
proposed/Basic Domino Footless and with Keeper	850/432	1.96/1
proposed/Basic Domino Footed and with Keeper	850/565	1.50/1
proposed/Scheme on Paper [95]	850/664	1.28/1
proposed/Scheme on Paper [90]	850/763	1.11/1

	UNG Comparison	**UNG Ratio**
SS 125^0 C		
proposed/ Basic Domino Footless and Keeperless	841/370	2.27/1
proposed/Basic Domino Footless and with Keeper	841/403	2.08/1
proposed/Basic Domino Footed and with Keeper	841/525	1.60/1
proposed/Scheme on Paper [95]	841/655	1.28/1
proposed/Scheme on Paper [90]	841/738	1.13/1

	UNG Comparison	**UNG Ratio**
FF 55^0 C		
proposed/ Basic Domino Footless and Keeperless	830/333	2.49/1
proposed/Basic Domino Footless and with Keeper	830/356	2.33/1
proposed/Basic Domino Footed and with Keeper	830/478	1.73/1
proposed/Scheme on Paper [95]	830/643	1.29/1
proposed/Scheme on Paper [90]	830/736	1.12/1

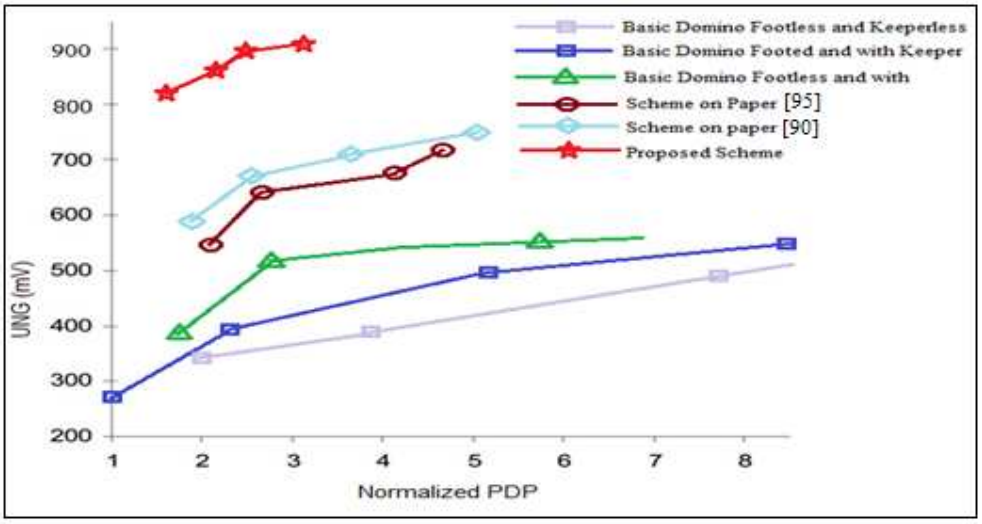
Table 4.3 shows the ratio of UNG for different corner cases under the same condition. Three cases have been shown in this table i.e. typical-typical (TT), slow-slow (SS), fast-fast (FF). This table shows that the proposed logic is having better noise tolerance than the basic circuit techniques and the scheme proposed in [95] and [90]. If we will compare it with reference [90], which is the best competitor, the unity noise gain achieves at least 10-13 % higher.

4.5.2 UNG COMPARISON AGAINST PDP

Fig.4.5 depicts the simulation results found for UNG against PDP for OR gates with different number of inputs. For all the techniques, the unity noise gain was measured in UMC 180 nm technology and a temperature of 27^0 C, by using the procedure explained above. All the inputs IN_1–IN_{15} were driven by noise pulses. These noise pulses given to the circuit were with the varying amplitude and same duration.

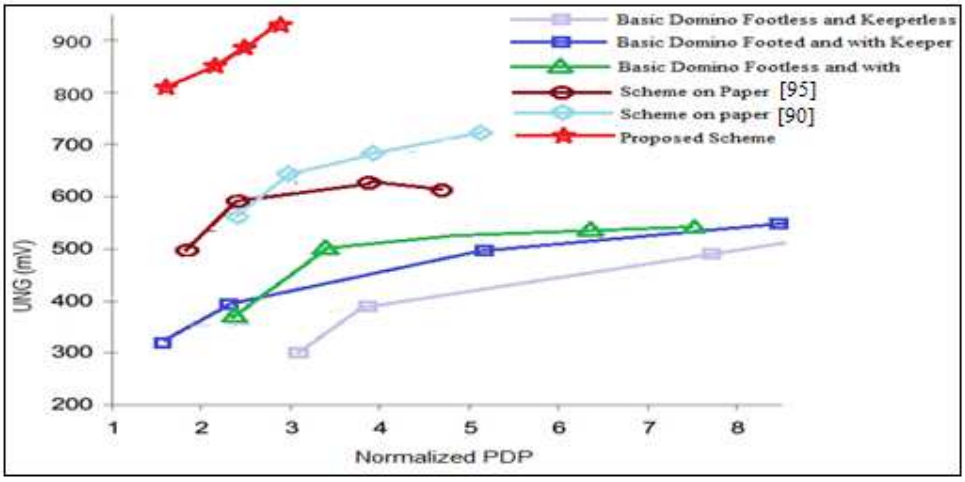
The amplitude of input noise pulse was gradually varied and watched, till a noise waveform with the same amplitude of the noise inputs found at the output. In the evaluation phase of CLK, when the CLK is high at that time, gate delay was measured, 0 to 1 transition of one of the input IN_1 and putting all the other inputs $IN_{2\text{-}N}$ low. Lastly, the PDP was measured in the worst-cases. Power delay product was measured after measuring the power dissipation and delay of the circuit. The UNG against the PDP for all the techniques and with different number fan-in were plotted as shown in Fig.4.5. As depicted in Fig.4.5, the proposed scheme reaches the highest values of the UNG, whereas the basic keeperless and footless domino techniques are at lowest place. With respect to basic keeperless and footless domino technique, the proposed domino circuit technique raises the UNG up to 45%.

The schemes of [90] and [95] achieve the best value of unity noise gain (UNG) after the proposed scheme. Still, the new scheme also achieves the lowest PDP with such a high UNG. With respect to the basic scheme, scheme [95] and [90] proposed scheme has higher UNG. In addition, the proposed scheme achieves PDPs 73, 64 and 53% lower respectively. In this section, the proposed circuit technique has been compared with all the other techniques. The simulations results confirm that, the proposed structures achieve the best UNG-PDP.



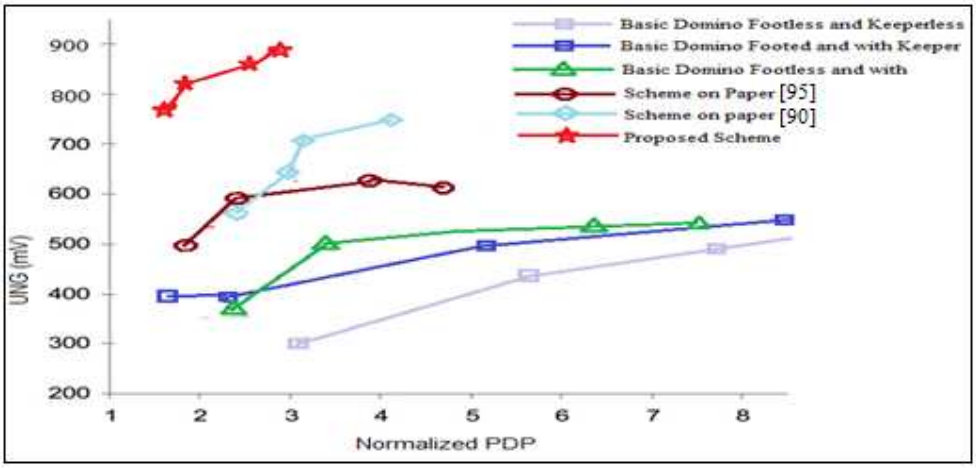
(a)

(a) UNG Vs. PDP (normalized PDP of 4 input OR gate)



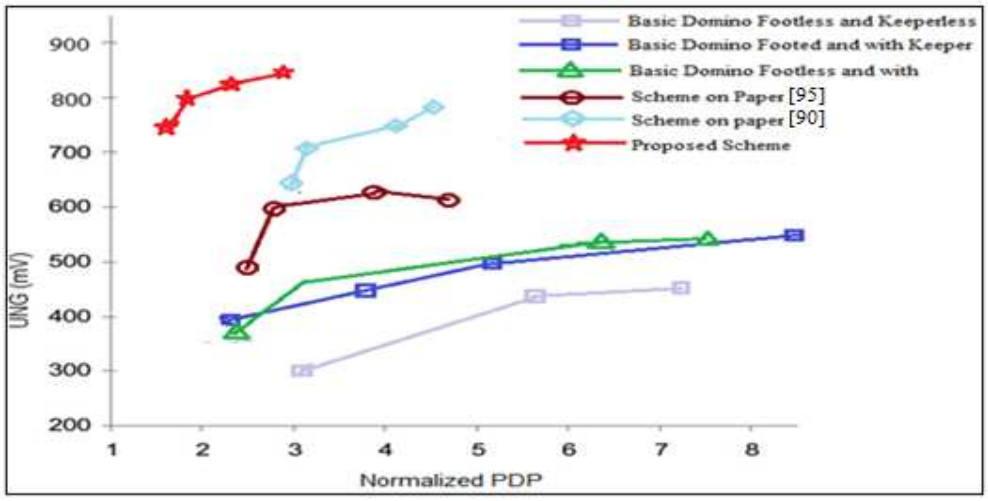
(b)

(b) UNG Vs. PDP (normalized PDP of 8 input OR gate)



(c)

(c) UNG Vs. PDP (normalized PDP of 16 input OR gate)



(d)

(d) UNG Vs PDP (normalized PDP of 32 input OR gate)

Fig.4.5 UNG Vs. PDP for all the techniques with different number of fan-in

4.6 AVERAGE NOISE THRESHOLD ENERGY (ANTE)

The ANTE metric is the Average Noise Threshold Energy. Average noise threshold energy is defined as the average input noise energy that the circuit can tolerate [84]. The energy of the pulse is defined as the energy equal to the energy dissipated in a 1 Ω resistor subjected to a voltage waveform with amplitude and width.

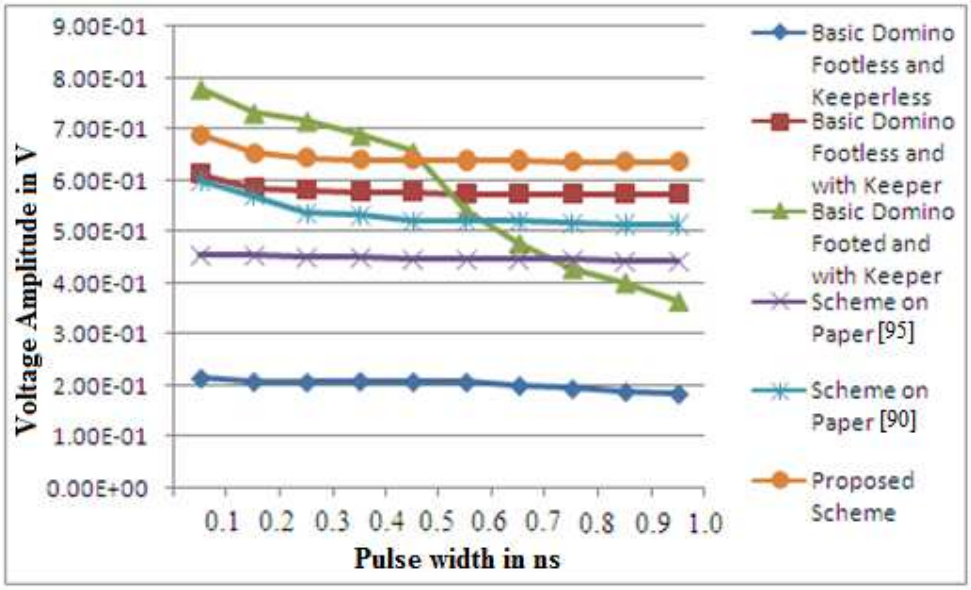


Fig.4.6 Plot for Noise Voltage Vs Noise Pulse Width for 2-input OR gate with V_{DD}=1 for different domino logic along with the proposed scheme

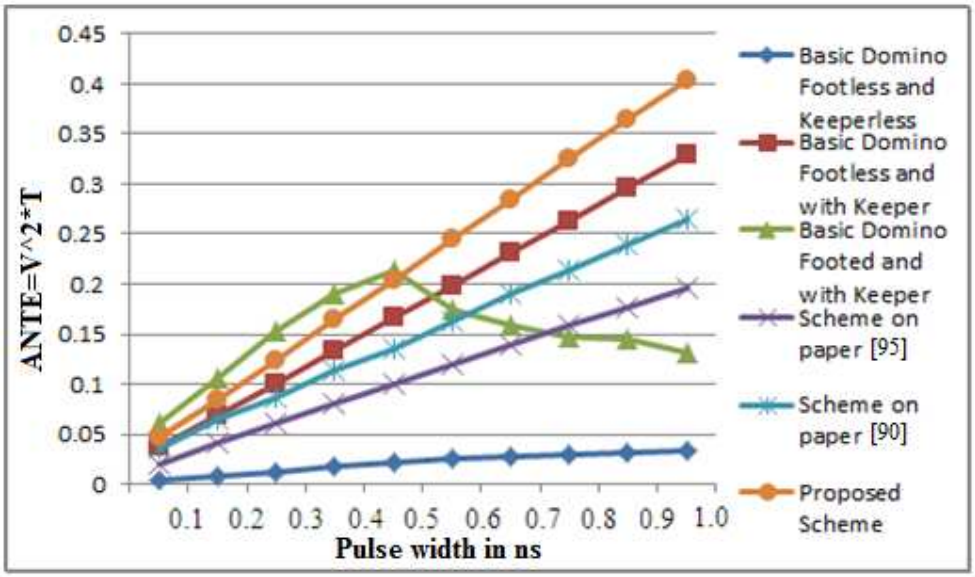


Fig.4.7 Plot for calculated ANTE Vs Noise Pulse Width for 2-input OR gate with V_{DD}=1 for different domino logic along with the proposed scheme

$$ANTE = (1/K) \sum V^2 \times T$$

Where K is number of observations

V is pulse amplitude

T is pulse width

Fig.4.6 and Fig.4.7 show the resulting noise immunity curve for the 2-input OR gate designed with the proposed domino logic circuit and compared with the 2-input OR gate of basic domino logic technique, keepered and footed domino techniques along with some recently proposed domino logic style. This was simulated in 500 MHz Clk frequency using UMC 180 nm technology at a room temperature of 27^0 centigrade using cadence specter. Fig.4.6 shows the plot for noise voltage against noise pulse width for 2-input OR gate with V_{DD}=1 for different domino logic along with the proposed scheme. Here, X-axis shows the pulse width of the noise input and Y-axis shows the amplitude of the noise pulse. To calculate the noise immunity of the circuit, any one of the inputs of the 2-input OR gate was given zero input value, while the other input was applied to a noise pulse. The pulse width of noise was kept fixed and the amplitude of noise was increased until output logic state changes. Therefore, we got the maximum noise amplitude, which the circuit can bear at a particular noise pulse width. Same procedure was repeated with different pulse widths till the noise immunity curve was constructed. Fig.4.7 Plot for calculated ANTE vs noise pulse width

for 2-input OR gate with V_{DD} = 1 for different domino logic along with the proposed scheme. The basic footed domino with keeper performs better than the proposed logic in this race upto 0.5 ns of input noise pulse width. However, it does performs good for input noise pulses over 0.5 ns. Over 0.5 ns of input noise pulse the proposed logic outperforms the basic footed domino logic in ANTE metric.

4.6.1 AVERAGE NOISE THRESHOLD ENERGY NOISE REJECTION CURVES

Domino CMOS Logic gates act as low pass filters. The dynamic noise rejection curve is defined as the locus of the combination of amplitude of noise input and duration of noise input, which can cause a gate to switch. If and only if the duration and amplitude combination of the noise lies above the dynamic noise rejection curve then the input noise causes failure of the circuit. In Fig.4.8, depicts the dynamic noise rejection curves of proposed circuit with different number of fan-in. This curve shows noise immunity. This curve when fan-in increases, noise margin decreases in this circuit.

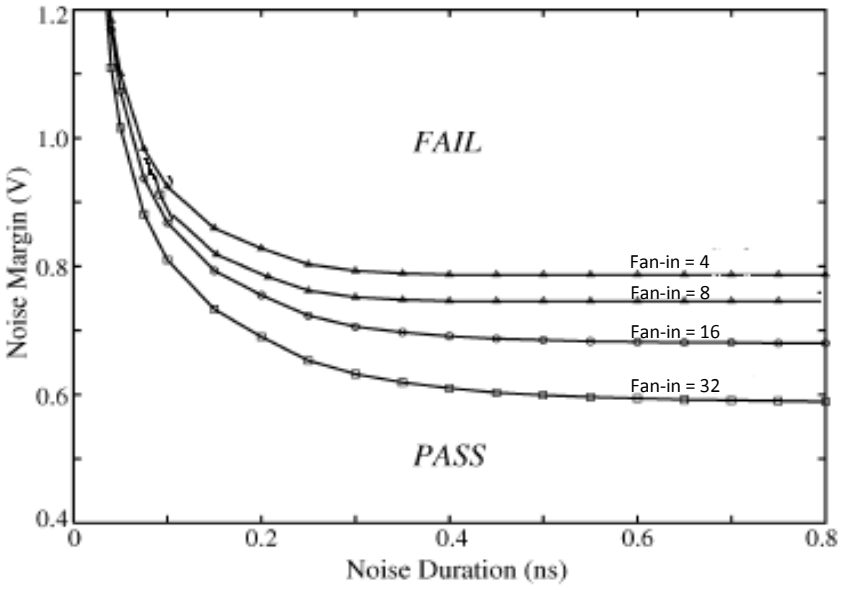


Fig.4.8 The dynamic noise rejection curves of proposed circuit with different fan-in

4.7 CONCLUSION

In this chapter, noise tolerance of the circuits was measured in two ways for the proposed circuit. 1. UNG (Unity Noise Gain) and 2. ANTE (Average Noise Threshold Energy). For measuring UNG and ANTE for the proposed circuit, first we have to add a noise injection circuit (NIC) to inject noise. This let us to find out the unity noise gain (UNG) and

average noise threshold energy (ANTE) and compare the same with other circuits. The noise tolerance of the proposed circuit when compared with the same of other proposed circuits was found to be 80 % to 90 % more noise tolerant than the other basic circuits and the two reference circuits simulated under same environment in UNG matric. When compared with reference [90], which is the best one, the UNG reaches at least 10-13 % higher. The proposed scheme reaches PDPs 53, 64 and 73% lower when compared with the basic scheme, scheme [95] and [90] respectively. When compared in the view of ANTE metric, ANTE metric also proved the proposed logic to be very much noise tolerant when compared to all other reference techniques. Simulation results of this chapter confirm that the proposed structure achieves a great level of performance on noise-tolerance. The new technique outperforms all the other schemes in noise tolerance performances. In order to demonstrate performance improvement of the proposed logic, few applications have been presented in the next chapter.

Chapter 5

APPLICATIONS OF PROPOSED DOMINO LOGIC

In this chapter, in order to prove the significance of proposed logic, several applications like adder and comparator are considered. These adder and comparator are simulated in UMC 180 nm technology and compared to their basic counterpart.

5.1 ADDERS

Full adders are the basic elements of complex arithmetic circuits such as adders, multipliers, dividers, exponent circuits, etc. [1] [126]. Thus, enhancement of the full adder circuit results to the performance upgrading of the entire system performances [95] [90]. Thus researchers from all over world are now working on full adder circuits to make it faster with smaller area and consuming lesser power [127] [128] [129].

A full adder circuit adds binary numbers and accounts for values carried in. A single bit full adder operates on single-bit numbers and adds them. This is generally written as A, B, and C_{in}. A and B are are operands of the addition operation. C_{in} bit is carried out in from consequent less significant stage. The circuit produces a double-bit output, carryout and sum typically represented by the signals C_{out} and S,

where,

$S = A \oplus B \oplus C_{in}$

$C_{out} = AB + AC_{in} + BC_{in}$

Complex arithmetic functions like multiplication, subtraction, addition, and division functions generally can be realized with multiple adders. Also all digital signal processing

units, microprocessors and encryption units have adder circuits in their core. Therefore, inefficient adder performance disturbs the arithmetic system entirely. Several CMOS adders have been proposed by researchers in the past years for improving either power, delay or noise performance [130] [122] [123]. In addition to that, numerous comparative studies have been done for analyzing which adder design provides us best performance when applied on an integrated circuits [9] [95] [131] [1] [132] [133] [134] [127] [128].

5.2 PREVIOUS PROPOSED ADDERS

The selection of a logic style is inclined to some factors specifically circuit speed, power dissipation, layout efficiency, noise tolerance, available supply voltage, area and process technology etc. Though dynamic circuits are often used for implementation of high speed logic circuits, yet there is fear of high leakage currents and a lot of power dissipation because of the presence of global clocking in a circuit. On the other hand, static logic style is voluminous and slow in operation. So in last some decades researchers have worked on adder circuits for improving either power, delay or noise performance. Here in this section, we are listing some of the past proposed adder structures.

5.2.1 CONVENTIONAL STATIC CMOS FULL ADDER CELL

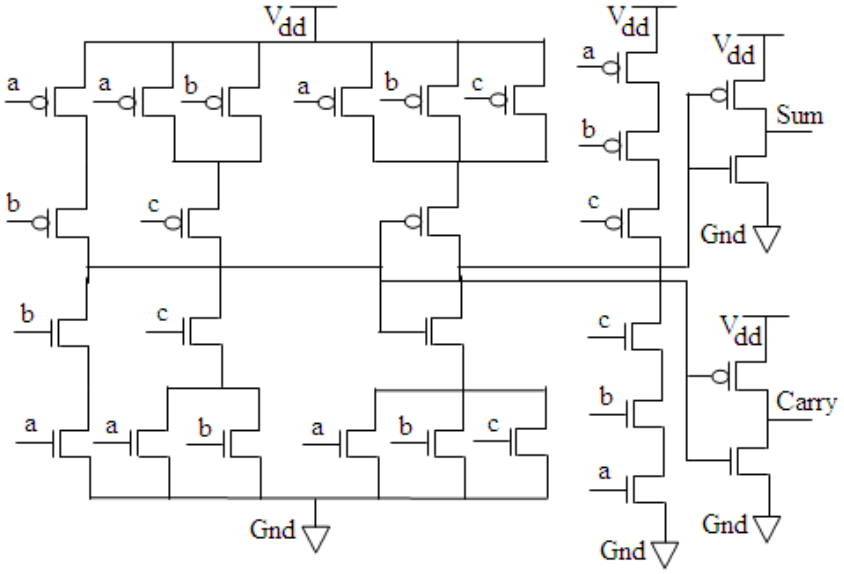


Fig.5.1 Conventional static logic full adder circuit (CSL) [134]

The conventional static CMOS full adder circuit [134] is depicted in Fig.5.1. Full adder designed with this logic style requires 28 transistors. This logic style is based on both

NMOS and PMOS logic style. Any logic gate designed in this method contains two complementary logic networks. One is combination of PMOS devices and the other combination of NMOS devices for creating pull up and pull down network. This design guarantees output node swings between V_{DD} and ground, so that static power dissipated in the circuit is negligible.

A schematic of conventional static logic is depicted in Fig.5.1. Static CMOS logic represents a traditional logic family well-known for simplicity in design style, robustness, low power, and good noise margins. An adder design with this logic uses 28 transistors, which represents the static CMOS design.

5.2.2 CONVENTIONAL DYNAMIC FULL ADDER CELL

The conventional dynamic full adder circuit is depicted in [29]. Full adder designed with this logic style requires 16 numbers of transistors, which is designed with CMOS logic style as depicted in Fig.5.2. Dynamic adder although having higher speed and small in size, yet performance of domino logic comes at the cost of power, robustness, and design effort. Domino logic consumes more power because of the increased number of transitions at the output node.

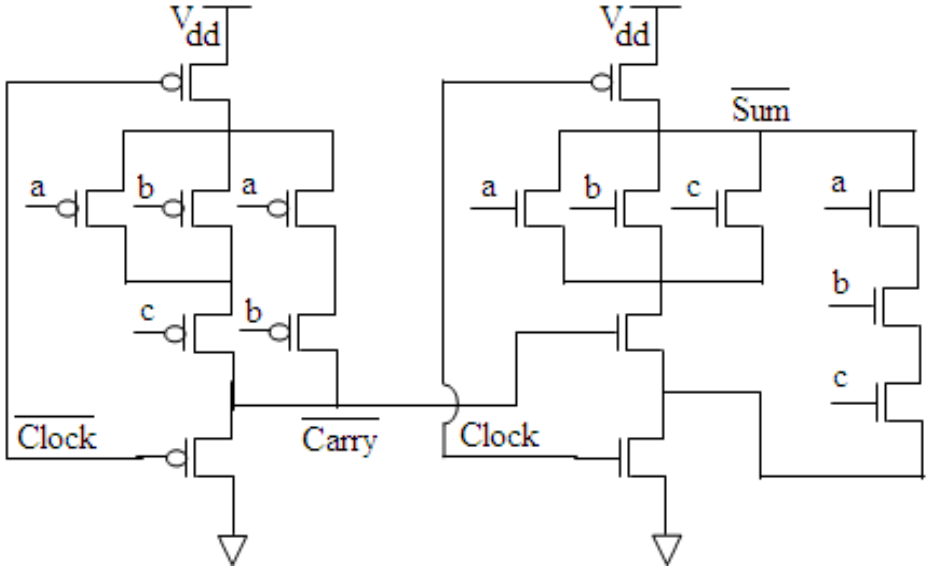


Fig.5.2 Conventional dynamic logic full adder circuit (CDL) [29]

5.2.3 COMPLEMENTARY PASS-TRANSISTOR LOGIC (CPL) FULL ADDER CELL

The complementary pass-transistor logic (CPL) full adder has been described in [1]. Full adder designed with this logic style requires 32 transistors. The design is based on the complementary pass-transistor logic as shown in Fig.5.3. CPL adder provides full swing of operation, high operational speed and best driving capabilities because of the presence of static inverters and a very fast differential stage of PMOS transistors. However, owing to the presence of static inverters and internal nodes, there is huge power dissipation.

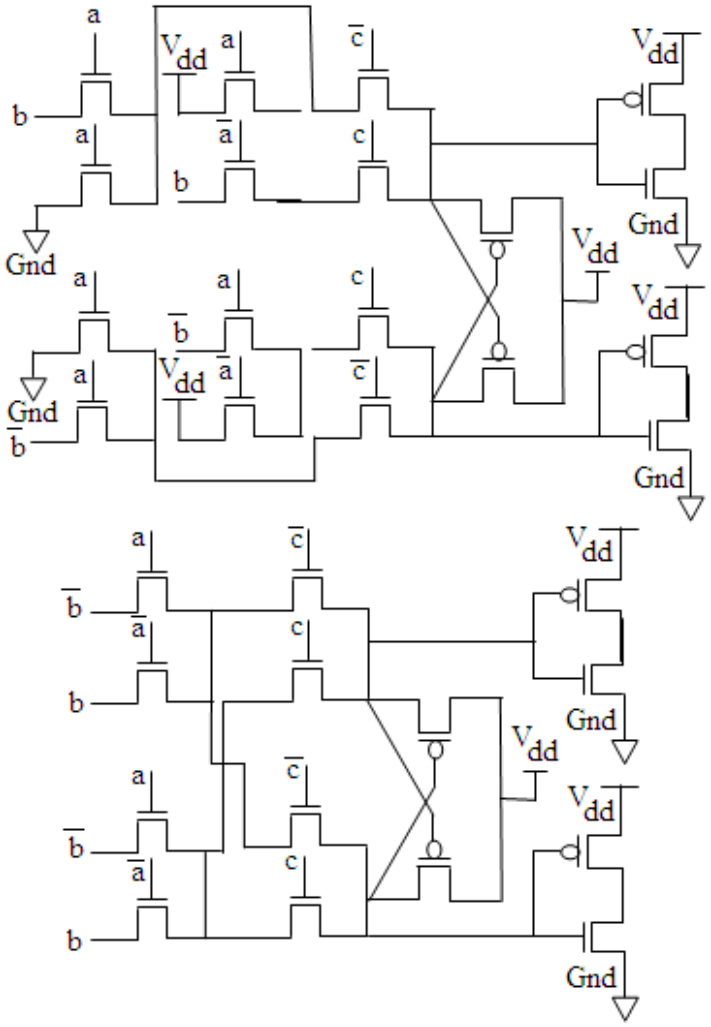


Fig.5.3 Complementary passtransistor logic (CPL) [1]

5.2.4 TRANSMISSION-GATES CMOS (TGCMOS) FULL ADDER CELL

Transmission-gates CMOS (TGCMOS) full adder circuit is described in [127]. Full adder designed with this logic style requires 20 transistors. The design contains transmission

gates as depicted in Fig.5.4. This circuit uses transmission gates in which PMOS and NMOS are in parallel and are controlled by complementary signals. Parallel PMOS and NMOS transistors are ON or OFF at the same time. The NMOS switch gives a good zero but a weak 1. The PMOS switch gives a good one but a weak 0. The main drawback of these TGCMOS is that their deficiency in driving capability. When transmission gate adders are cascaded, their performance reduces considerably.

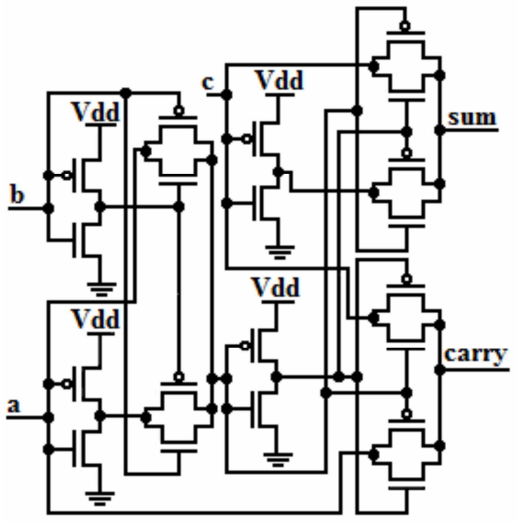


Fig.5.4 Transmission gate CMOS full adder circuit (TGCMOS) [127]

5.2.5 14 TRANSISTORS (14T) ADDER CELL

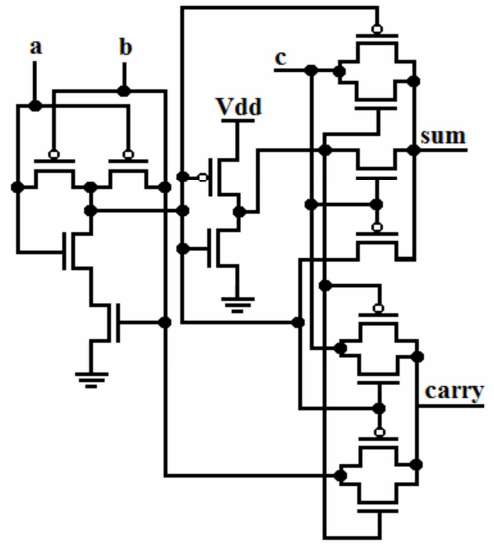


Fig.5.5 14 Transistor CMOS full adder circuit (14TCMOS) [128]

14T adder cell is a low power implementation of the full adder cell. Full adder designed with this logic style requires 14 transistors (14T) [128]. 14T full adder contains transmission gates and XOR gates designed for low power consumption as shown in Fig.5.5. 14T full adder cell is designed using transmission gates and low power XOR/XNOR gates. Limitation of 14T adder cell is its less driving capability and non-full swing output when V_{DD} becomes less than 1V.

5.2.6 TRANSMISSION FUNCTION FULL ADDER CELL (TFA)

The transmission function full adder cell (TFA) is described in [129]. Full adder designed with this logic style requires 16 transistors. This design contains transmission function as depicted in Fig.5.6. This transmission full adder, which is denoted as TFA, is less complex than the basic CMOS full adder circuit shown in Fig.5.1. Transmission function full-adder requires lesser number of transistors in comparison with conventional one. The transistor required for transmission function full-adder circuit is 16, while the number of transistors requires designing conventional static adder is 28. It provides buffered outputs of appropriate polarity for both sum and carry-out. TFA has a disadvantage of mediocre speed and higher power consumption.

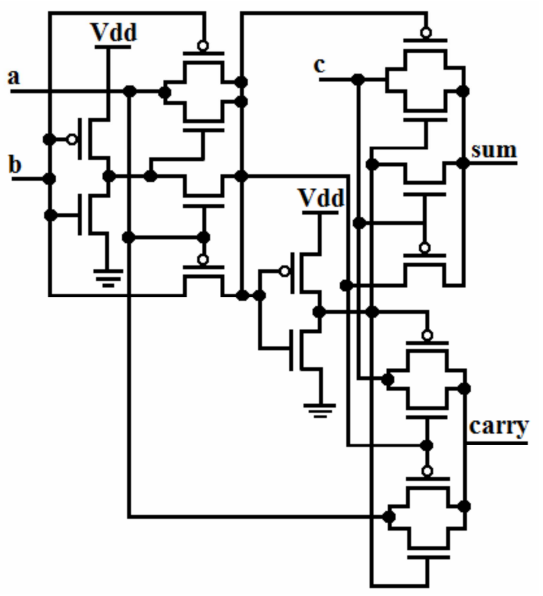


Fig.5.6 Transmission function full adder circuit (TFA) [129]

5.3 PROPOSED ADDER

In this section, a new full adder cell is presented, which is designed with the proposed circuit technique as depicted in Fig. 5.7. This circuit consists of two precharge transistors (M_1, M_8), evaluation networks to evaluate carry and sum (PDN Carry, PDN Sum), two keeper transistors (M_2, M_9), six footer transistors (M_3, M_4, M_5, M_{10}, M_{11}, M_{12}) and two pseudo-domino inverters. In the precharge phase, when Clk goes LOW, pre-charging PMOS transistor becomes ON and the dynamic node is connected to the V_{DD} and obtain precharge from V_{DD}. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input stays at logic 1. At the evaluation stage when all the inputs are at logic 0, the dynamic node becomes logic 1. But high fan-in NMOS PDN leaks the stored charge of the dynamic node due to subthreshold leakage. This leakage current is again compensated by PMOS keeper transistor, this targets to recover the voltage drop of the dynamic node. When an impulse of noise voltage occurs at input, keeper may not be able to recover the voltage level of the dynamic node. To stop that the footers M_3, M_4 and M_5 are connected to carry part and M_{10}, M_{11} and M_{12} are connected to the sum part. M_3 and M_{10} operate as stack transistors. At the evaluation phase when PDN of sum carry are at logic 1, at that time M_3 and M_{10} stops free discharge of dynamic node voltage to evaluate logic 0 at the dynamic node of carry and sum simultaneously. To compansate that M_5 and M_{12} make a charge discharge path for the carry part and the sum part simultaneously. Here M_4 and M_{11} again act as a stack for the 2nd path to maintain dynamic node.

It was previously discussed that, pulses at the N_FOOT always propagates due to the NMOS transistor of the buffer i.e. M_7 and M_{14} of this adder. These pulses are generated due to the precharge act of dynamic logic. So, by any means if we can switch off that NMOS transistors M_7 and M_{14} during precharge, the pulse propagating to the output can easily be avoided. Following this method, this novel circuit structure is proposed. This process makes the circuit become less power consuming and noise tolerant. This can be increased by widening M_2 and M_9 (high W/L) to make it more conducting.

The source of NMOS transistor of the buffer was connected to the foot of PDN i.e. drain of NMOS Clk transistor, instead of Gnd. By doing this, the circuit operates in Semi domino scheme.

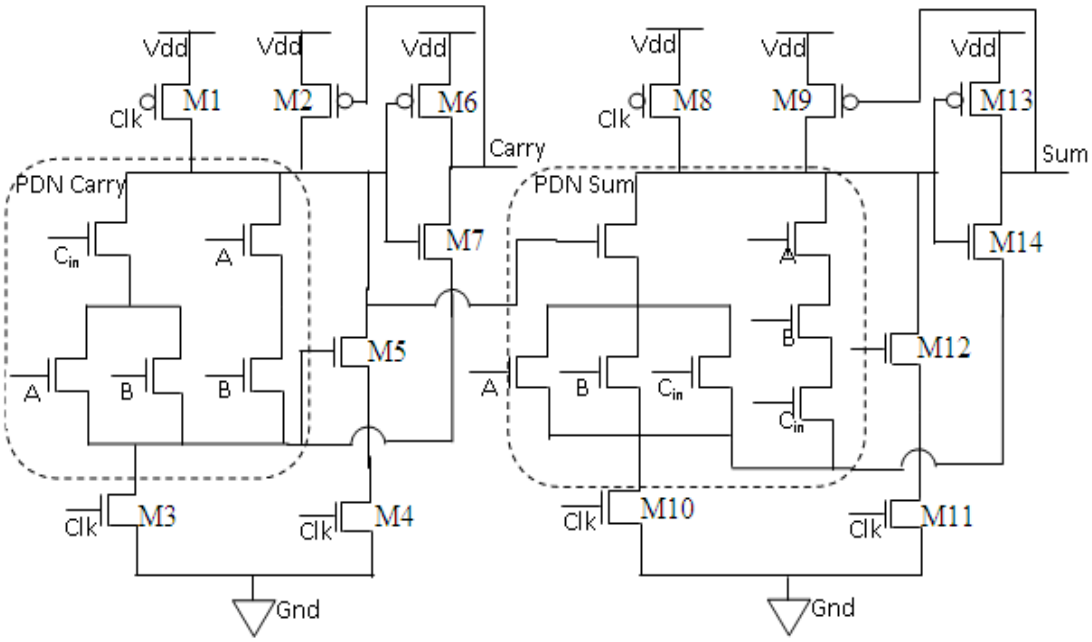


Fig. 5.7 Proposed full adder

Fig.5.8 and Fig.5.9 shows output waveform of the basic adder and the proposed adder circuits simultaneously. Among these output waveforms shown in Fig.5.8 and Fig.5.9, the first one shows the clock input, the second one shows the carry input (C_{in}), third waveform and the fourth waveform show the data inputs (A and B), the fifth waveform shows the carry output and the sixth one shows the sum output of the basic adder and the proposed adder simultaneously.

It can be seen that in Fig.5.8, sum and carry output waveforms of the basic adder contains a lot of noise. The output gets ON and OFF again and again with clock frequency when waveforms are at logic 1. This characteristic of the output waveform leads to more delay and more power consumption of the circuit. If input logic is on because of the pulse, the number of switching of the buffer in evaluation period will be as frequent as the clock signal. Therefore, heavy amount of current flows through the buffer; which results in increase in power consumption of the circuit. For each switching, Power Consumption = V_{DD}*I, where, V_{DD} denotes the supply voltage and I denotes the short circuit current flowing through the buffer from V_{DD} to GND. The power consumption of the circuit increases due to precharge phase of clock. Though we can't stop the precharge period, we have optimized the dynamic circuit in this thesis to reduce noise and power consumption. Fig.5.9 represents output waveform of proposed adder, which does not possess these pulses in the sum and carry waveform. This makes the circuit faster and the power consumption noticeably decreased.

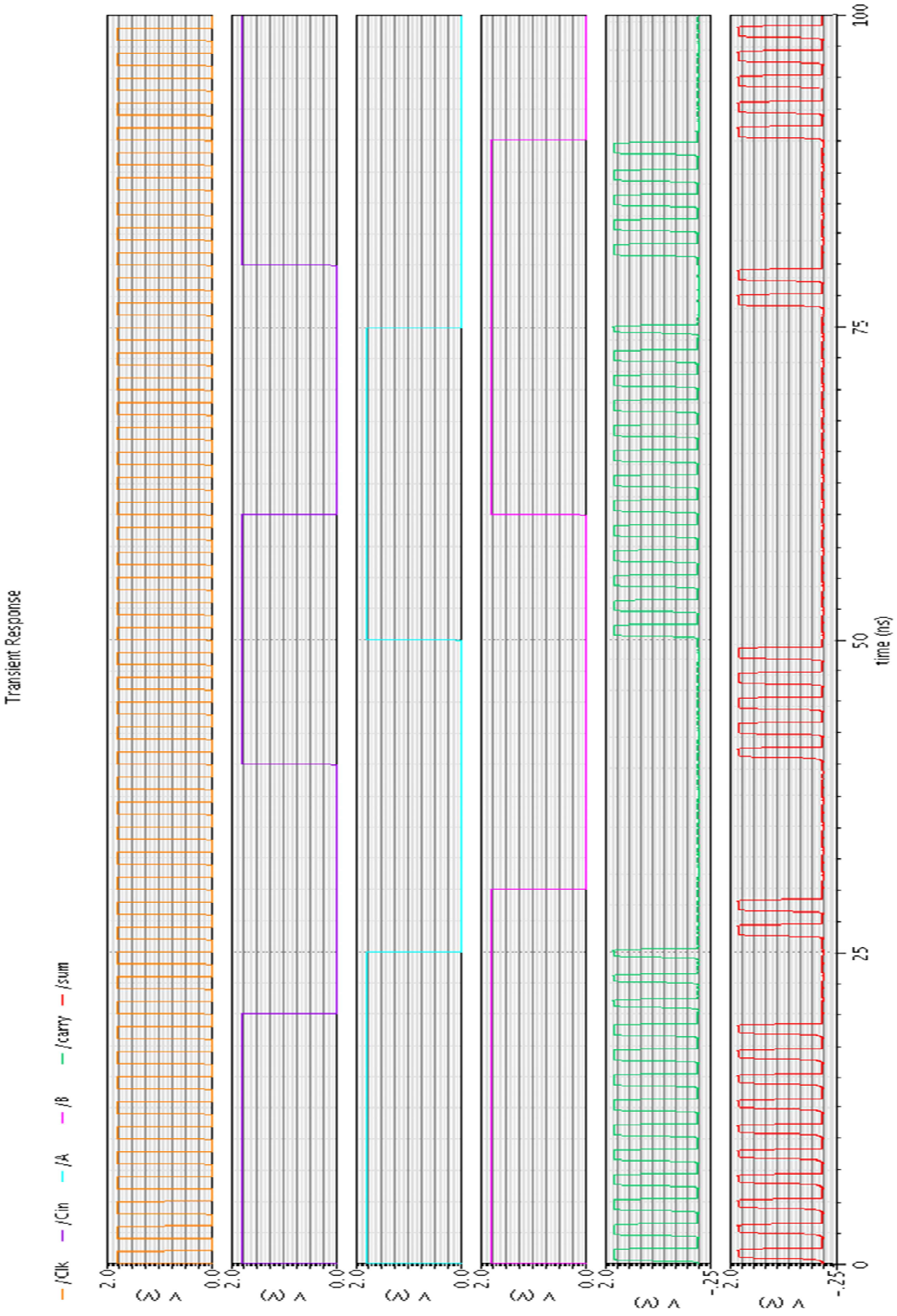


Fig.5.8 Output of the basic adder

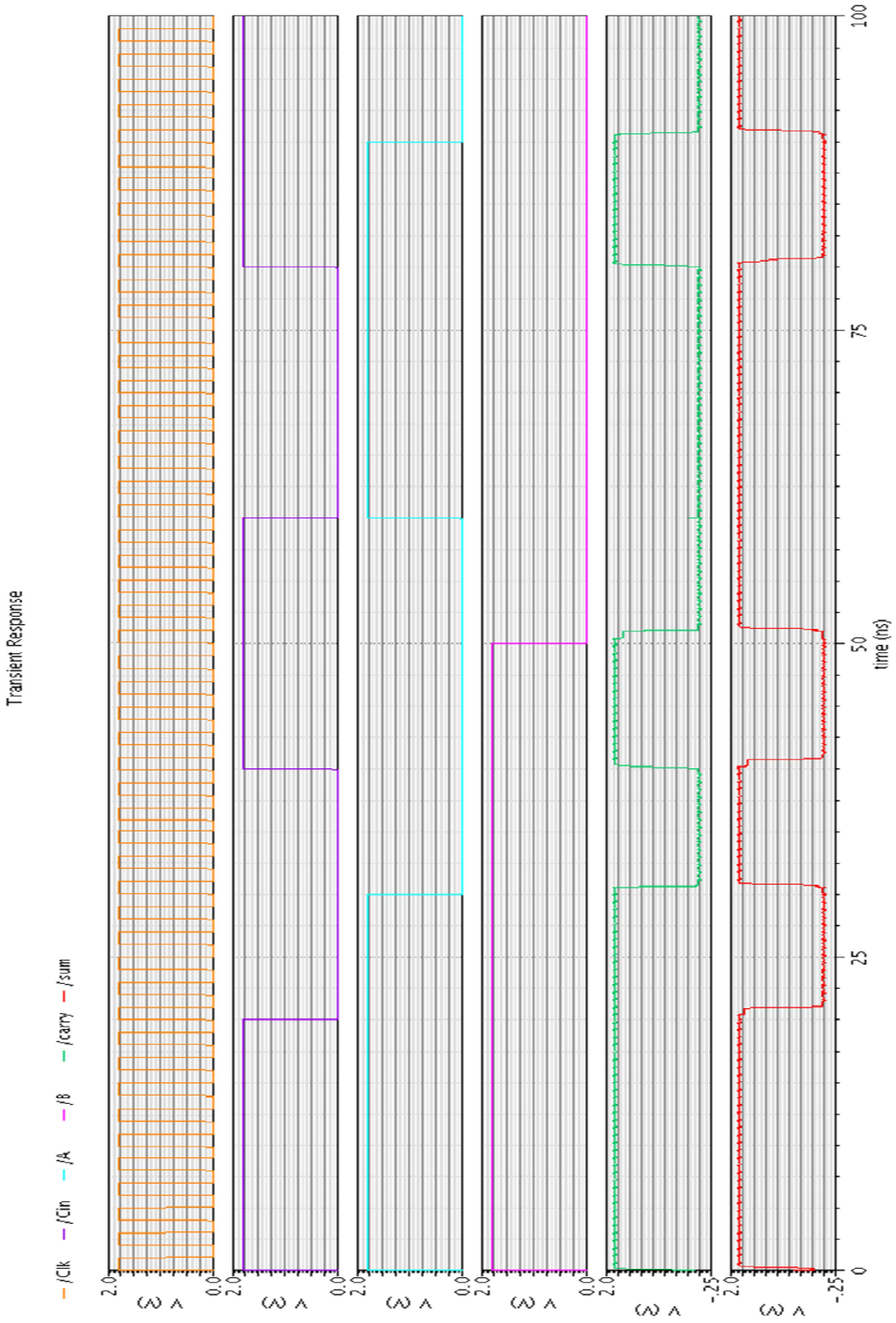


Fig.5.9 Output of the proposed adder

5.4 COMPARISON RESULTS

The adder circuits were simulated by using Cadence Specter using 180 nm technologies using 1.8 V. The circuit was being compared with the adders designed with previous techniques. It was found that the proposed circuit performs better than the previous proposed circuits. Hereby, in this section we will analyze the performance comparison with different simulation results.

5.4.1 POWER-DELAY PRODUCT (PDP) PERFORMANCE

Here, we have designed and compared the proposed full adder cells using the basic techniques, reference techniques and our proposed circuit technique. Fig.5.10 and Table 5.1 shows comparison of delay of all the reference circuits, the basic circuits and the proposed (PDL) circuit varying the voltage. Fig.5.11 and Table 5.2 compare power of the circuits by changing the supply voltage. When compared to the other circuits it can be seen that the power-delay-product (PDP) could reduce 65% to 85% times in the proposed adder circuit shown in Fig.5.12. As compared to basic domino the proposed circuit contains only 3 extra transistors whereas other circuits contain more number of extra transistors and also the inconvenience of having inverting clock. To estimate power, the power consumption estimated here is not only power consumption of the dynamic logic but also power which is dissipated through the clock buffer. Note that circuits having lower power-delay-product (PDP) are better performing.

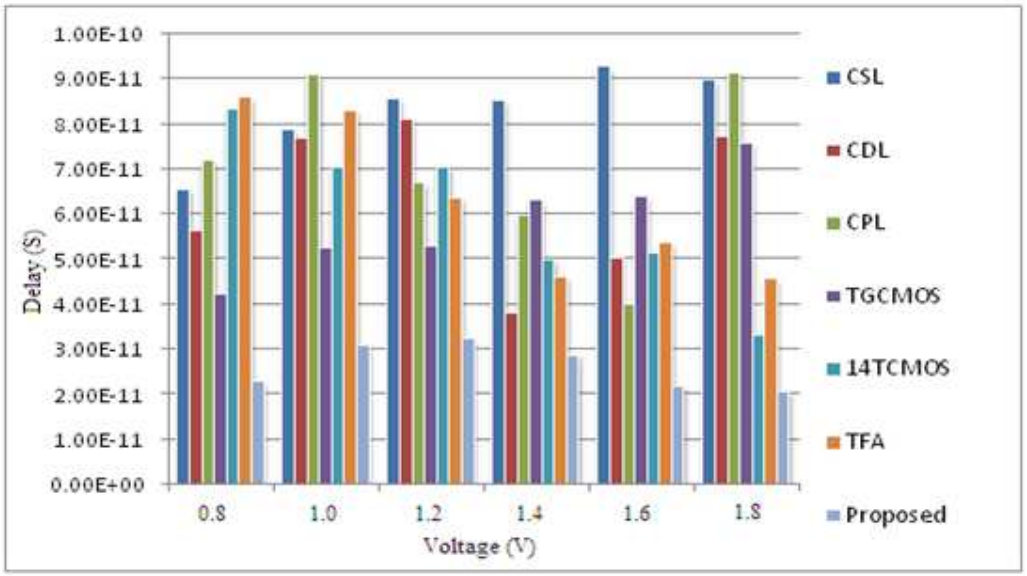


Fig.5.10 Delay comparison (Varying the supply voltage)

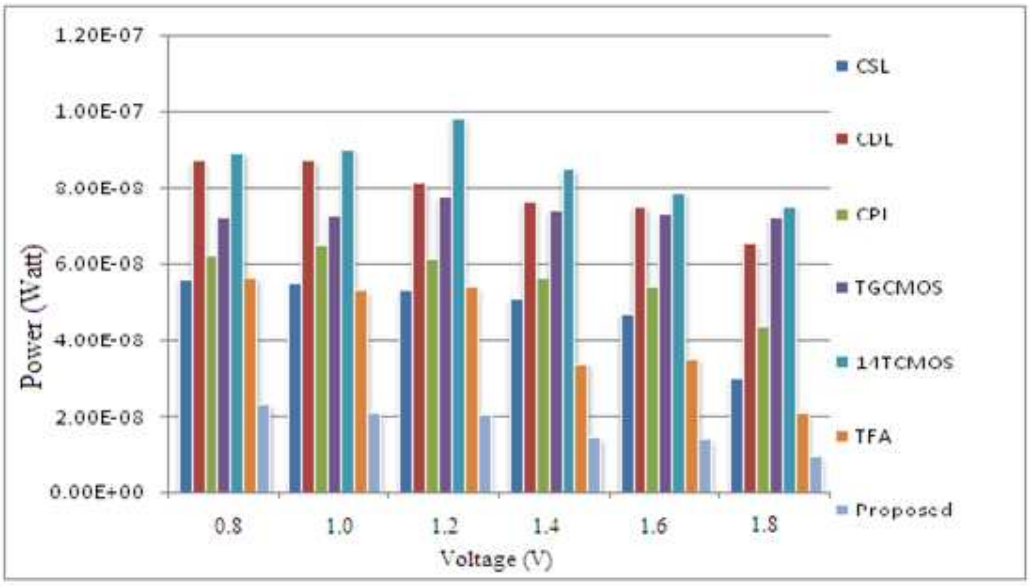


Fig.5.11 Power comparison (Varying the V_{DD})

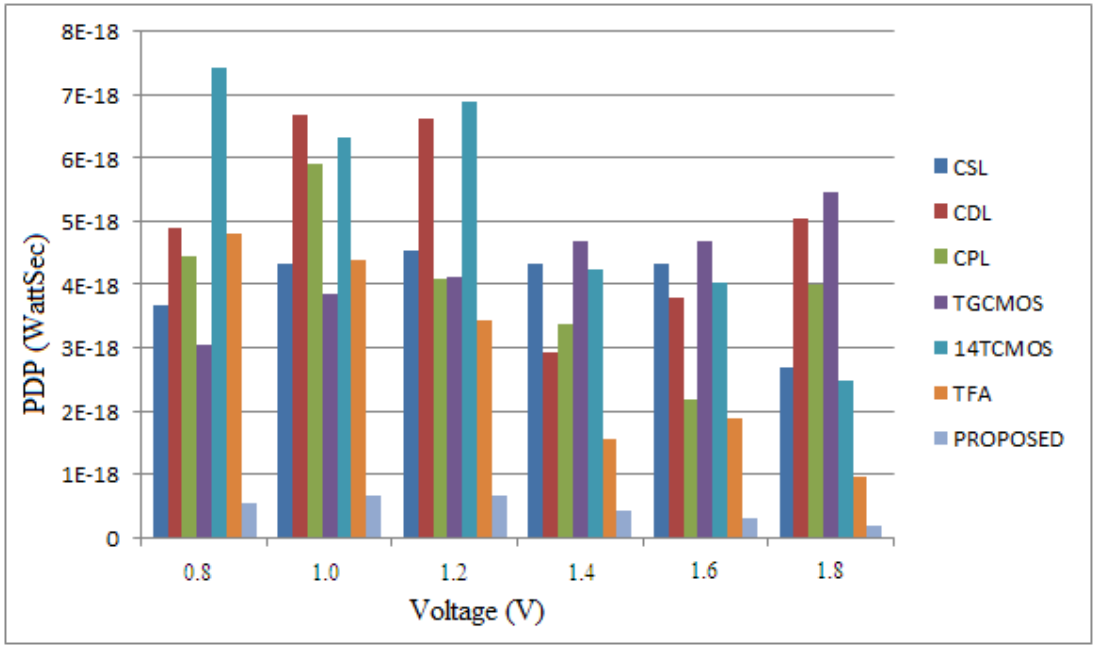


Fig.5.12 Power-delay product (PDP) comparison (Varying the supply voltage)

Table 5.1 Delay comparison (Varying the supply voltage)

LOGIC STYLES / SUPPLY VOLTAGES	CSL	CDL	CPL	TGCMOS	14TCMOS	TFA	Proposed Logic
1.8 V	6.57E-11	5.66E-11	7.19E-11	4.23E-11	8.34E-11	8.60E-11	2.30E-11
1.6 V	7.88E-11	7.69E-11	9.10E-11	5.28E-11	7.05E-11	8.30E-11	3.10E-11
1.4 V	8.58E-11	8.13E-11	6.70E-11	5.32E-11	7.06E-11	6.38E-11	3.24E-11
1.2 V	8.52E-11	3.82E-11	6.00E-11	6.35E-11	5.00E-11	4.62E-11	2.89E-11
1.0 V	9.29E-11	5.04E-11	4.01E-11	6.42E-11	5.15E-11	5.38E-11	2.20E-11
0.8 V	9.00E-11	7.73E-11	9.16E-11	7.58E-11	3.31E-11	4.57E-11	2.08E-11

Table 5.2 Power comparison (Varying the supply voltage)

LOGIC STYLES / SUPPLY VOLTAGES	CSL	CDL	CPL	TGCMOS	14TCMOS	TFA	Proposed Logic
1.8 V	5.57E-08	8.66E-08	6.19E-08	7.23E-08	8.90E-08	5.60E-08	2.30E-08
1.6 V	5.48E-08	8.69E-08	6.50E-08	7.28E-08	8.99E-08	5.30E-08	2.10E-08
1.4 V	5.28E-08	8.13E-08	6.10E-08	7.72E-08	9.78E-08	5.38E-08	2.04E-08
1.2 V	5.08E-08	7.63E-08	5.60E-08	7.40E-08	8.45E-08	3.38E-08	1.44E-08
1.0 V	4.67E-08	7.50E-08	5.40E-08	7.29E-08	7.83E-08	3.52E-08	1.38E-08
0.8 V	3.00E-08	6.53E-08	4.37E-08	7.21E-08	7.50E-08	2.08E-08	9.40E-09

5.4.2 UNITY NOISE GAIN (UNG)

Unity noise gain is a method of leakage measurement of the circuit. To measure robustness of the circuit, in the evaluation phase similar noise pulses were applied to every input of OR gate and noise amplitude at output of the OR gates was measured as shown in Fig.4.3. Here, noise amplitude at output is detected for different voltage of input noise keeping width of noise pulse constant. The noise pulse duration was kept at 30 ps (which is the typical gate delay of 180-nm technology). Unity noise gain(UNG) is defined as the input noise amplitude which can cause same amplitude of output noise [102]. A pulse noise have been used to simulate noise at the input. Actual noise of a circuit depends upon both duration and amplitude of input noise. So, the input noise level can be modified by modifying the pulse amplitude or duration. Here, the input noise level was changed by changing voltage of the input noise pulse. In our simulations, we have changed input noise of the circuit by changing the noise voltage. unity noise gain of the proposed circuit was 25 to 40 % more than that of the conventional circuits. Note that circuits having more UNG are more stable circuit.

Table 5.3 compares UNG of the proposed adder with other conventional style adders and Fig.5.13 shows it graphically. Note that more UNG implies more stable circuit.

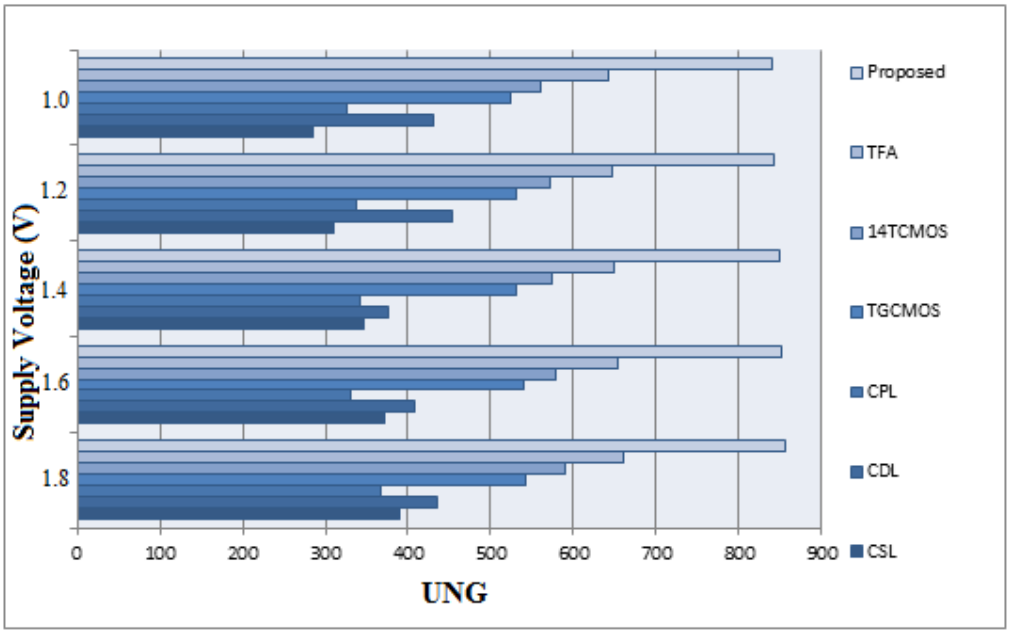


Fig.5.13 UNG comparison (Varying supply voltage)

Table 5.3 UNG comparison (Varying supply voltage)

Supply Voltages	CSL	CDL	CPL	TGCMOS	14TCMOS	TFA	Proposed Logic
1.8	390	436	367	542	589	661	856
1.6	372	409	331	541	578	654	851
1.4	347	376	343	532	574	650	849
1.2	310	453	338	530	571	647	842
1.0	285	431	326	524	560	642	840

5.4.3 LEAKAGE CURRENT COMPARISON

Leakage current of the proposed adder method has been simulated with UMC CMOS 180 nm technology and was compared with conventional adders simulated in the same environment. Fig.5.14 shows the comparison result. The footer transistors prevent a huge amount of leakage current from leaking.

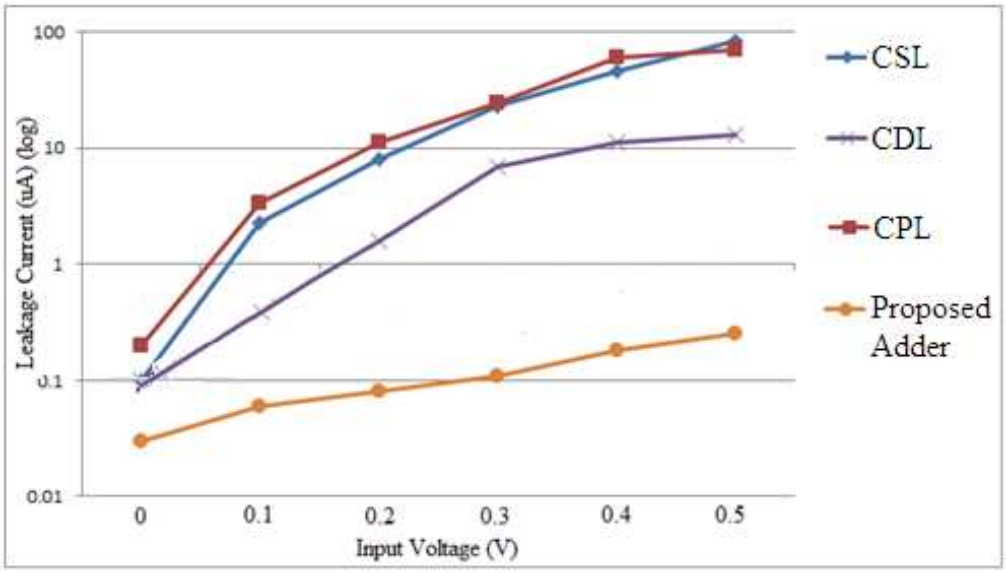


Fig.5.14 Leakage currents comparison of the analyzed techniques with conventional techniques for 1-bit adder

Fig.5.14 describes a semilog graph between I_{LEAK} i.e. leakage current for all the techniques and input voltage for the proposed one. Leakage currents at the critical node are plotted against input voltage of gate. The graph shows the comparison results of the analyzed technique with the conventional techniques simulated for 1 bit adder. The variable parameters of all the techniques were set with the intention of ensuring the same PDP value. It can be clearly seen that the leakage current I_{LEAK} of the proposed technique is larger than that of all other techniques when simulated in same environment.

5.5 DIGITAL COMPARATOR DESIGN BY PROPOSED LOGIC DESIGN

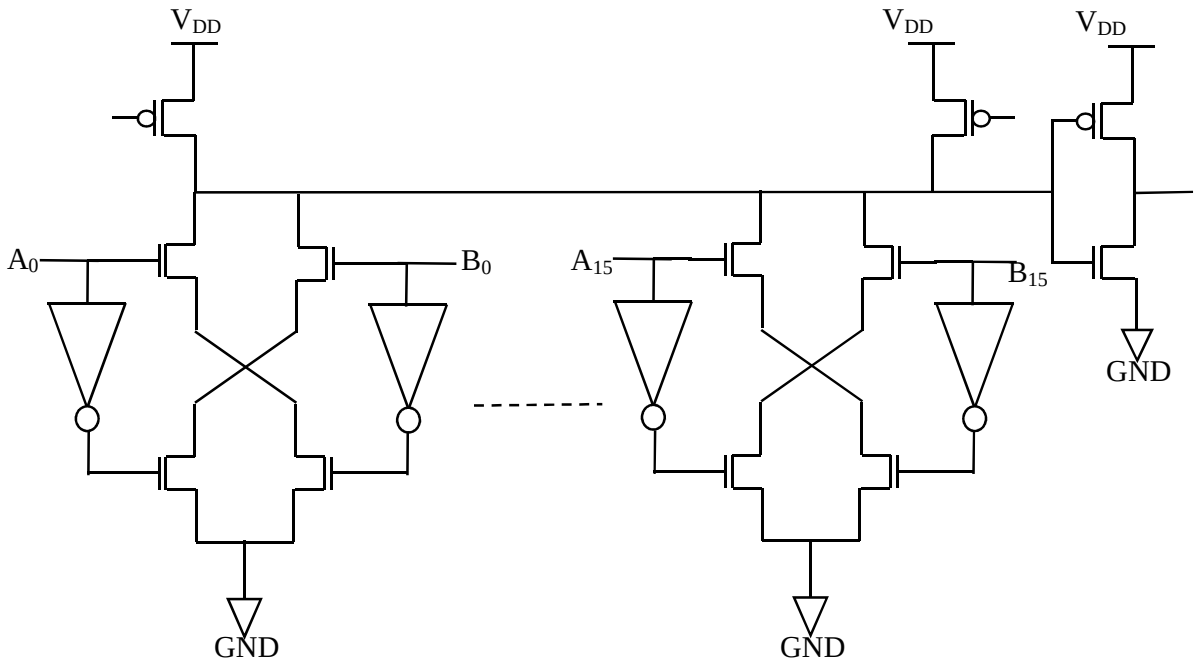


Fig.5.15 Basic 16-bit comparator design

To validate efficiency of the proposed CMOS domino logic technique Fig.5.16, we have employed this proposed design technique to design a large fan-in 16-bit comparator. This design has been defined and compared with its conventional equivalents in this section.

Fig.5.15 depicts the schematic design of a 16-bit input domino comparator designed with standard footless domino. In precharge phase clock (Clk) is '0', all inputs become zero. At that time, dynamic node gets precharged through the PMOS, as a result; the output becomes '0'. During the evaluation period when the clock goes high, PMOS becomes OFF and the pull down network conducts according to the logic levels of the inputs. If all

matching bits of A input and B input are equal, not any discharge path exits to discharge the dynamic node. But, if the logic level of A input and B input vary a single bit position, conducting path established from the dynamic node to GND, which discharges the dynamic node. This causes output node to become '1'.

In this circuit operation, the worst case situation with delay becomes, when the input A and input B differ in any single bit position. Here, only one of the two evaluation branches conducts, which discharges total voltage of dynamic node to ground. The worst case scenario for noise becomes, when every input bit becomes zero and they receive the same noise in the evaluation period. Considering typical case of a comparator, generally keeper transistor is upsized to achieve improved noise tolerance and delay performance. The keeper ratio actually described as ratio of current driving ability of the keeper to current driving ability of one of the evaluation branches. Comparator designed with basic domino logic fails to operate correctly for smaller size of keeper because of high leakage current. Here in proposed comparator, keeper was kept at minimum size and size of footer transistors are upsized to find better noise immunity and delay performance.

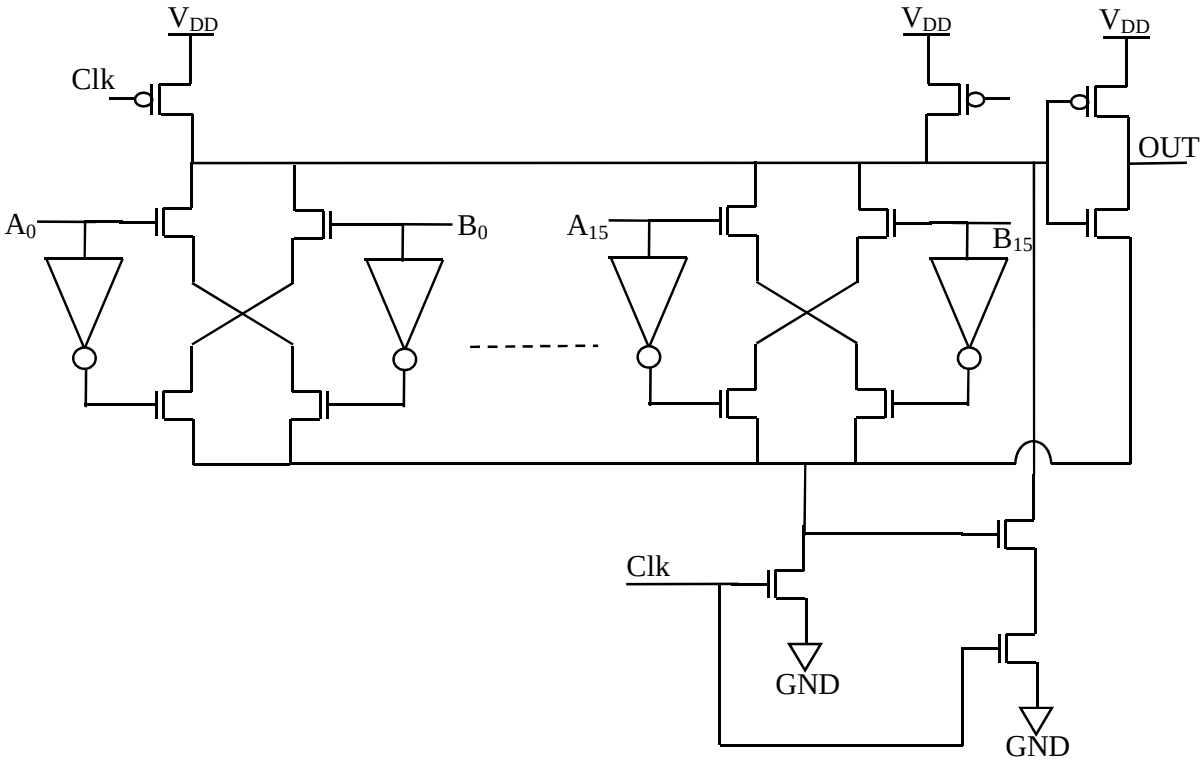


Fig.5.16 16-bit Comparator designed with the proposed logic

5.5.1 COMPARISON OF THE PROPOSED COMPARATOR WITH BASIC COMPARATOR

Fig.5.17, Fig.5.18, Fig.5.19 and Fig.5.20 show the results of this experiment in 180-nm process at 1.8 V and 27 ^{0}C. As detected from Fig.5.17 and Fig.5.18, the power consumption and delay of the comparator designed with the proposed logic is considerably lower than that of the basic logic. This implies that the power-delay product (PDP) of the proposed comparator is very less than that of the standard comparator. Fig.5.19 and Fig.5.20 show that the unity noise-gain of the proposed design is significantly more than the standard domino gate. In Fig.5.19 the UNG comparison is on the basis of varying the supply voltage and Fig.5.20 UNG comparison is on the basis of varying the fan-in of the circuit. Table 5.4, Table 5.5, Table 5.6 and Table 5.7 and also show the table where the observed data are presented in tabular form.

Table 5.4 Delay comparison (Varying the fan-in)

Fan-in of comparator	Basic Comparator	Proposed Comparator
4	5.81E-11	9.30E-12
8	6.11E-11	9.73E-12
12	6.15E-11	9.88E-12
16	6.54E-11	0.88E-11
24	6.86E-11	1.10E-11
32	7.00E-11	2.33E-11

Table 5.5 Power comparison (Varying the fan-in)

Fan-in of comparator	Basic Comparator	Proposed Comparator
4	7.50E-08	2.87E-08
8	7.83E-08	2.90E-08
12	7.98E-08	3.69E-08
16	8.17E-08	3.91E-08
24	8.27E-08	4.28E-08
32	8.92E-08	4.44E-08

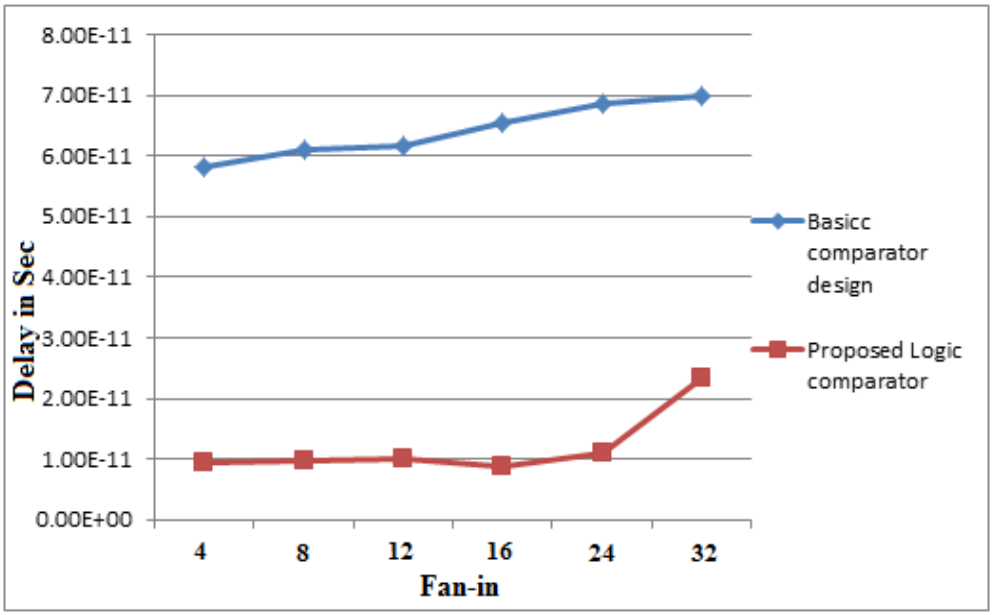


Fig.5.17 Delay comparison (Varying the fan-in)

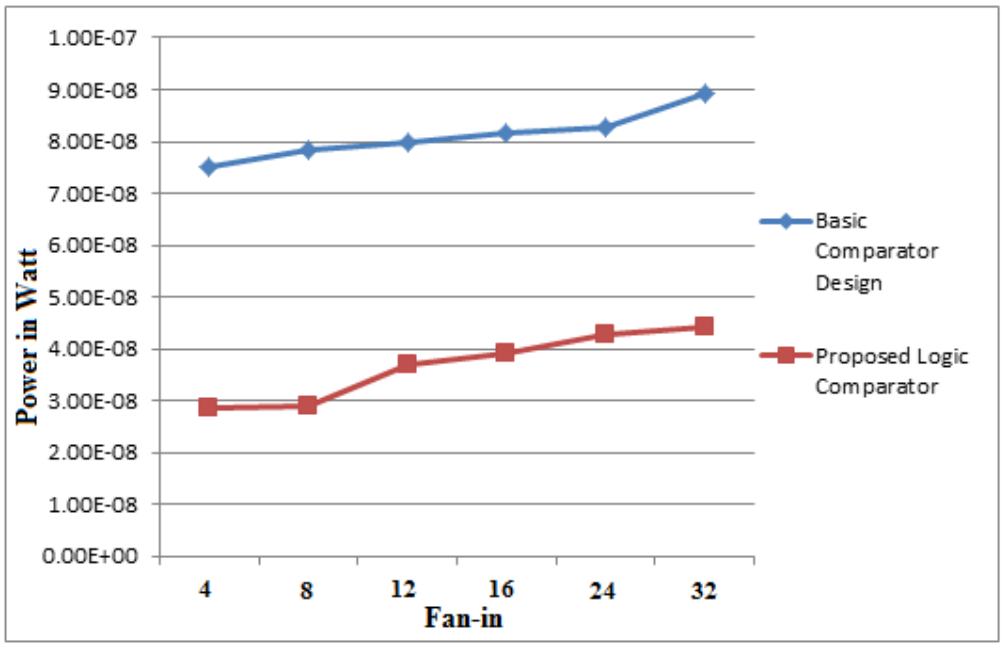


Fig.5.18 Power comparison (Varying fan-in)

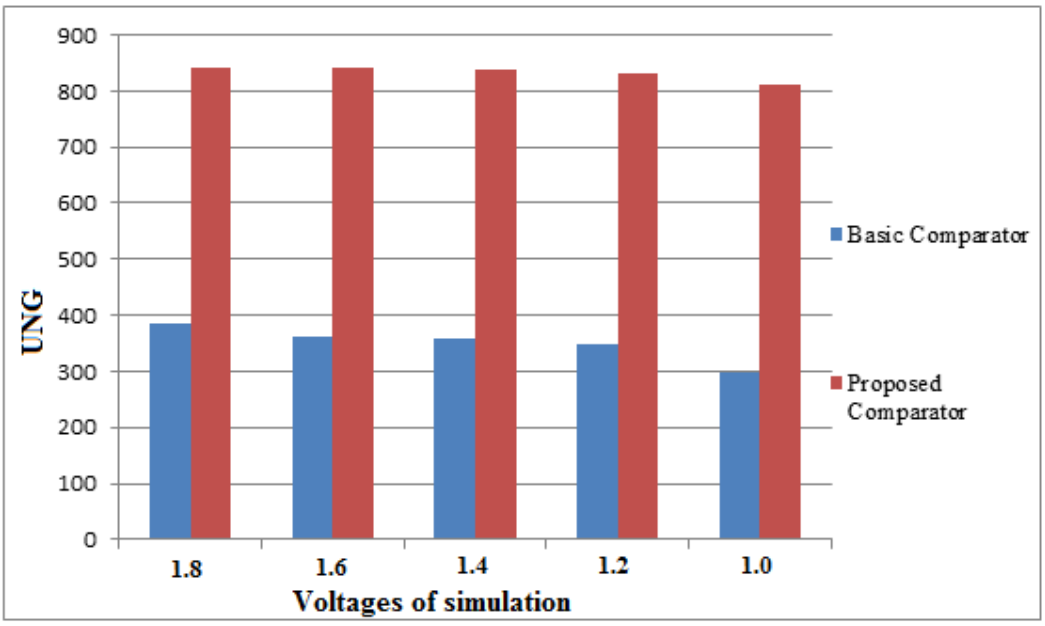


Fig.5.19 UNG comparison with fan-in of 16 bit (Varying the supply voltage)

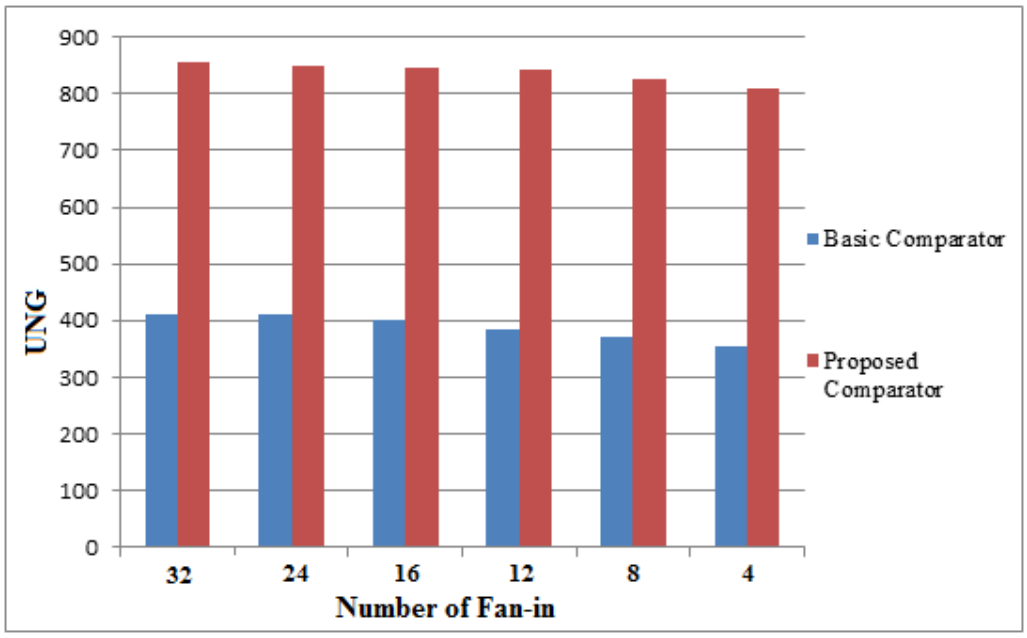


Fig.5.20 UNG comparison using supply voltage of 1.8 V (Varying the fan-in)

Table 5.6 UNG comparison with fan-in of 16 bit (Varying the supply voltage)

Supply Voltages	Basic comparator	Proposed Comparator
1.8	384	843
1.6	362	841
1.4	359	838
1.2	347	832
1.0	299	811

Table 5.7 UNG comparison with supply voltage of 1.8 V (Varying the fan-in)

Supply Voltages	Basic comparator	Proposed Comparator
4	411	856
8	410	850
12	400	846
16	384	843
24	372	825
32	356	811

Table 5.8 UNG comparison with fan in = 16 (Varying the supply voltage)

Supply Voltages	Basic comparator	Proposed Comparator
1.8	384	843
1.6	362	841
1.4	359	838
1.2	347	832
1.0	299	811

5.6 CONCLUSION

In this chapter, a full adder and a comparator were designed using the proposed logic. The proposed one after simulation was compared with the simulation results of the previous proposed logic, which were simulated in same environment as the proposed logic. The outputs were presented clearly in this chapter. In the next chapter we have designed an ALU testchip with proposed logic design style.

Chapter 6

LAYOUT OF TEST CHIP

6.1 INTRODUCTION

To demonstrate the advantages of proposed domino logic style in real hardware, we have built a custom test-chip in UMC 180 nm process with an ALU core, using the proposed domino logic style. In this chapter, we have designed the ALU chip. We have also presented initial power delay performance comparisons between the circuit level simulated ALU and real hardware implemented in the proposed domino logic style.

6.2 ANALOG IC DESIGN FLOW

The basic design flow of an analog IC design, together with Cadence tool is shown in Fig.6.1. A schematic view of the ALU circuit was designed first by using Cadence composer schematic editor. Then the circuit was simulated using cadence analog design environment. Then layout of schematic was designed by using Virtuoso Layout Editor [135] [136].

The resulting layout is then subjected to Design Rule Check (DRC), which is some geometric rules dependent on the technology. Electrical Rule Check (ERC) is then performed for electrical errors like short circuit. Then the layout of the ALU was compared with circuit schematic of the ALU by performing Layout Versus Schematic (LVS) check, to ensure that the required functionality is actually implemented.

Finally, a net list including parasitic resistance and capacitance was extracted. The simulation of this spice netlist is called as Post Layout Simulation. Once functionality of layout is verified than final layout was then converted to certain standard file formats like GDS-II depending upon foundry.

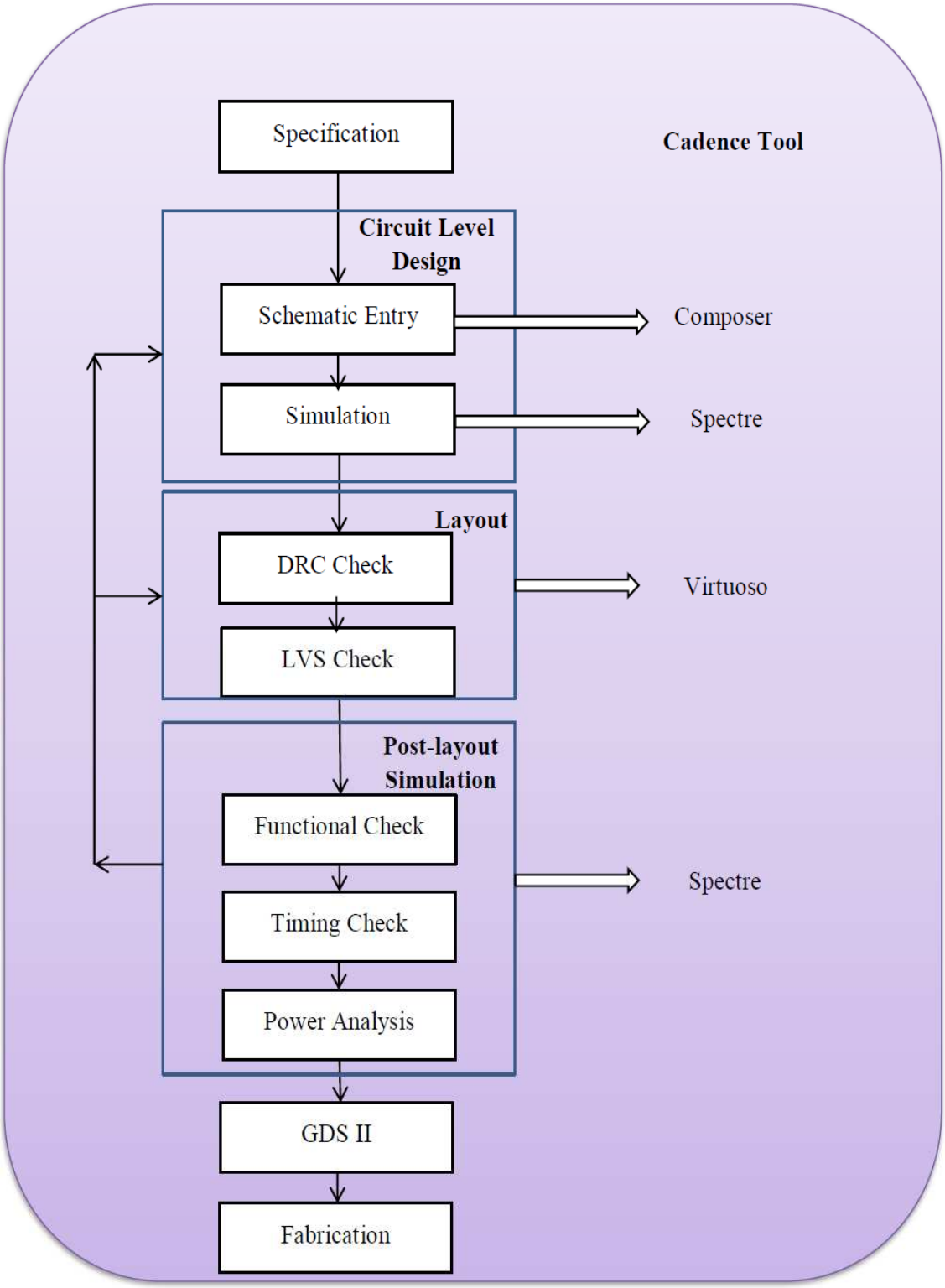


Fig.6.1 Analog IC design Flow

6.3 ALU ARCHITECTURE:

6.3.1 DESIGN SPECIFICATIONS:

Block diagram of ALU is shown in Fig.6.2. The ALU contains two units, one arithmetic unit and another logic unit. Arithmetic unit is built with adder/substractor, multiplier and shifter. Logic unit is built with NOT operator, OR/NOR operator, AND/NAND operator and OR/XOR operator. The operation mode is set by the control signal and the multiplexor unit. Here an approach was followed to design the test chip.

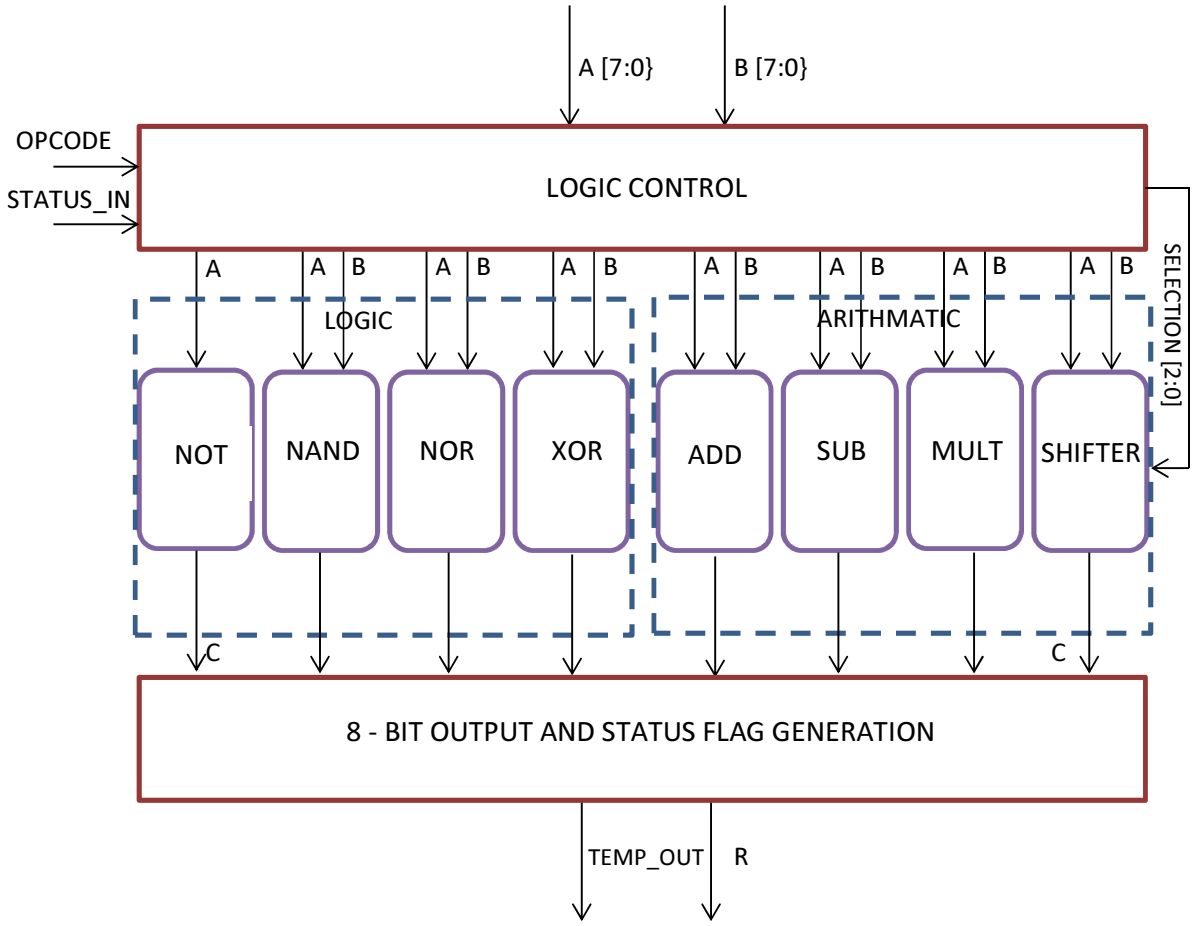


Fig.6.2 ALU block diagram

First top-down approach is followed to specify different blocks of ALU as shown in Fig.6.2. Then bottom-up approach is follows to design each individual block.

ALU cores consume a two 8-bit input vector and produce 8-bit output vector on every cycle, at up to roughly 1 GHz. The ALU contains two units, one arithmetic unit and another logic unit. Arithmetic unit is built with adder/substractor, multiplier and shifter. Logic unit is

built with NOT operator, OR/NOR operator, AND/NAND operator and OR/XOR operator. Operation mode is set by the control signal and the multiplexor unit.

Table 6.1 Functionality of ALU

Selection Line (S_2,S_1,S_0)	Functionality	Operation
000	NOT	A’
001	NAND	(AB)’
010	NOR	(A+B)’
011	XOR	A⊕B
100	ADD	A + B
101	SUB	A - B
110	MULT	A * B
111	SHFT	Right shift of A

The ALU has 8 operations implemented as defined by the Table 6.1. The operations are selected by the three select lines S_1, S_2 and S_3. The select lines are asserted by the corresponding ALU instructions as shown under operation column in the table.

6.3.2 SCHEMATIC & SIGNAL OF ALL THE INTERNAL BLOCKS

All the logical and arithmetic blocks were designed using the proposed domino logic technique using cadence spectre using 180 nm technologies. All circuits were designed using the proposed CMOS logic technique. In this section we have shown schematic diagrams of all the blocks used for the ALU.

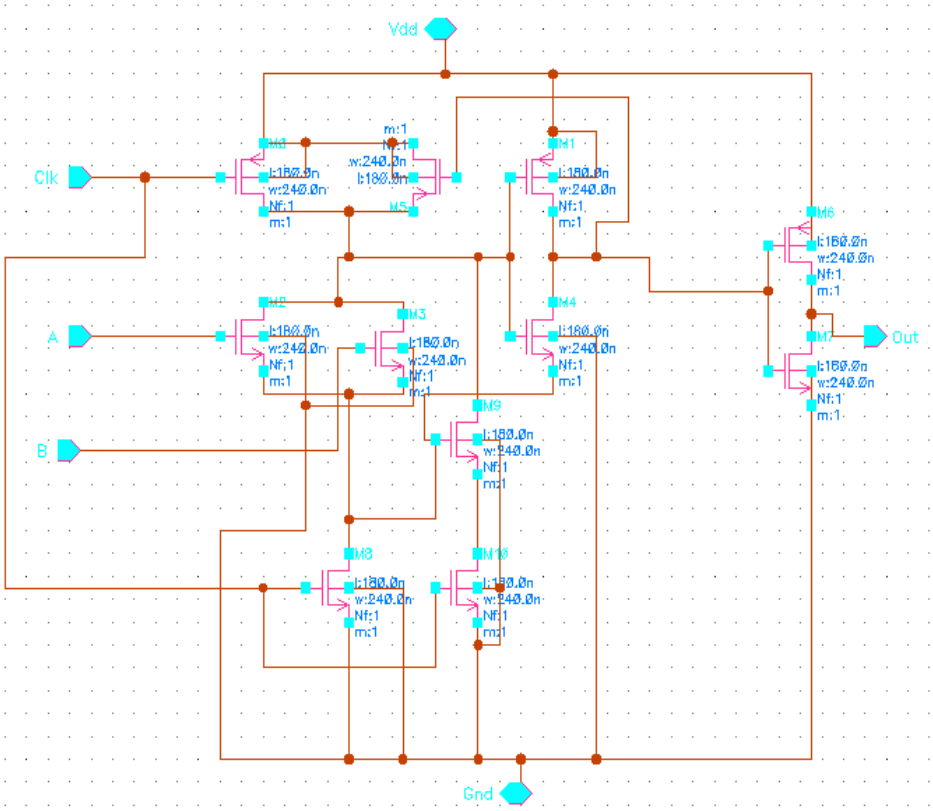


Fig.6.3 Proposed XOR2 gate schematic

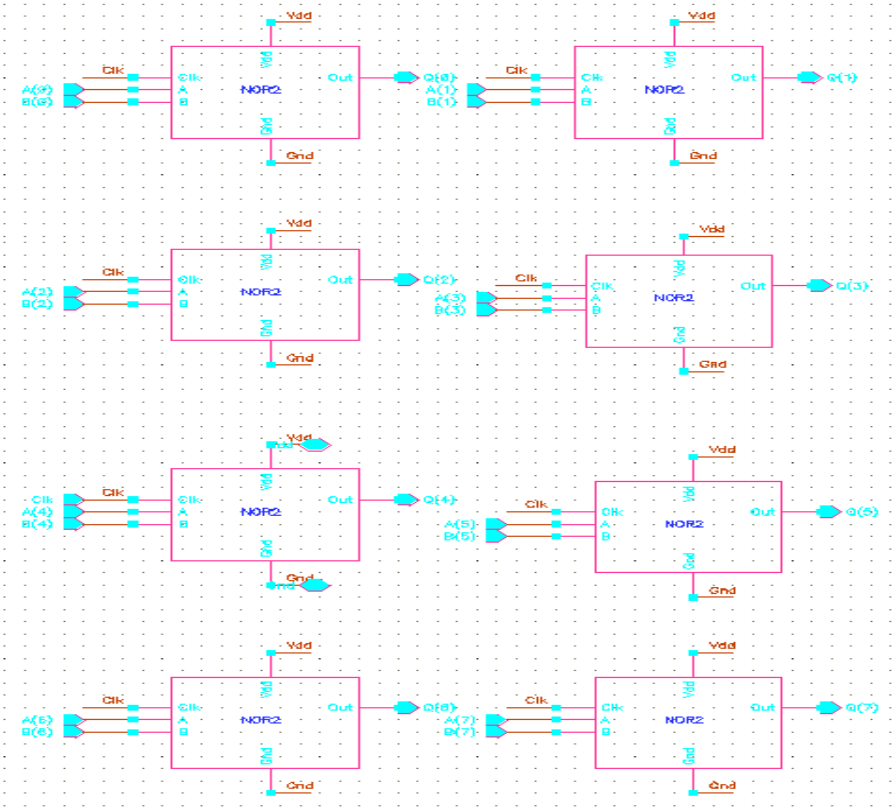


Fig.6.4 Proposed 8-bit XOR2 gate schematic

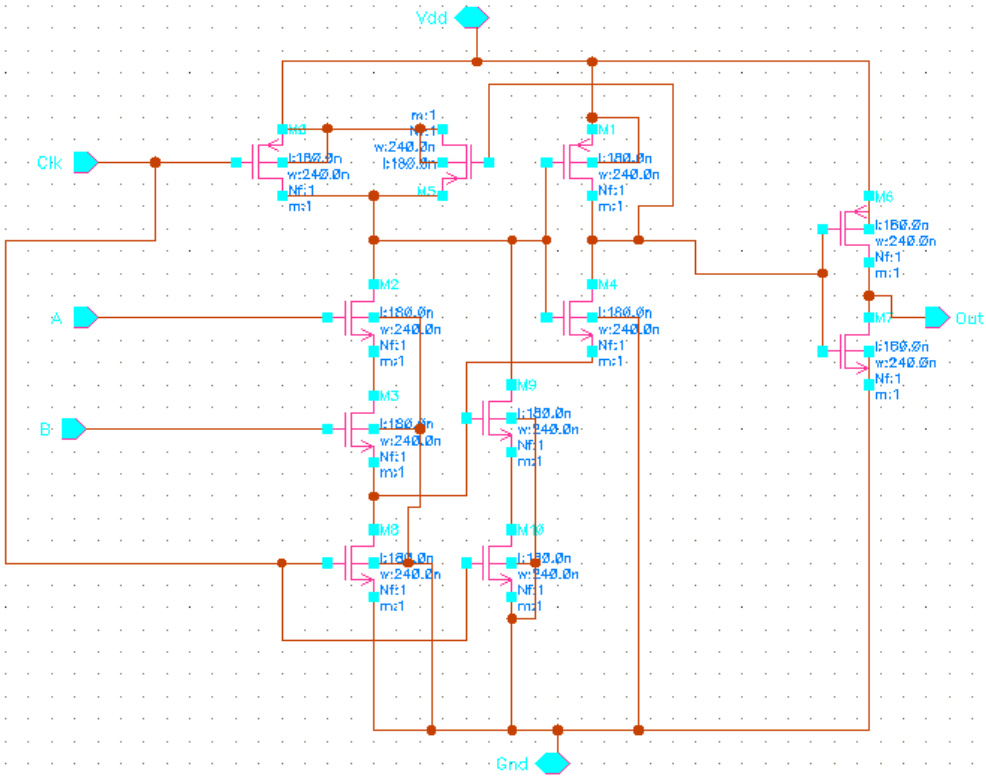


Fig.6.5 Proposed 2-input NAND gate schematic

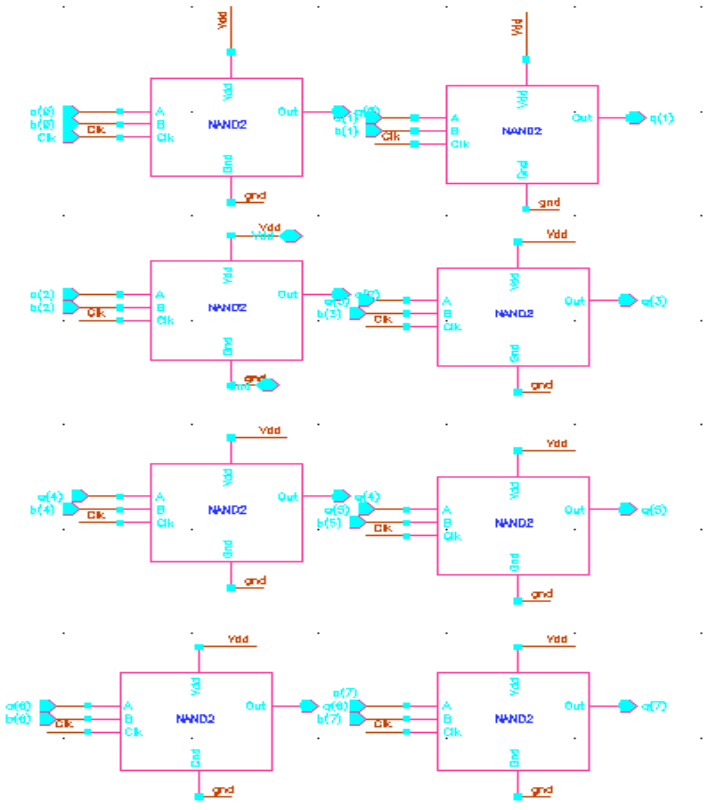


Fig.6.6 Proposed 8-input NAND gate schematic

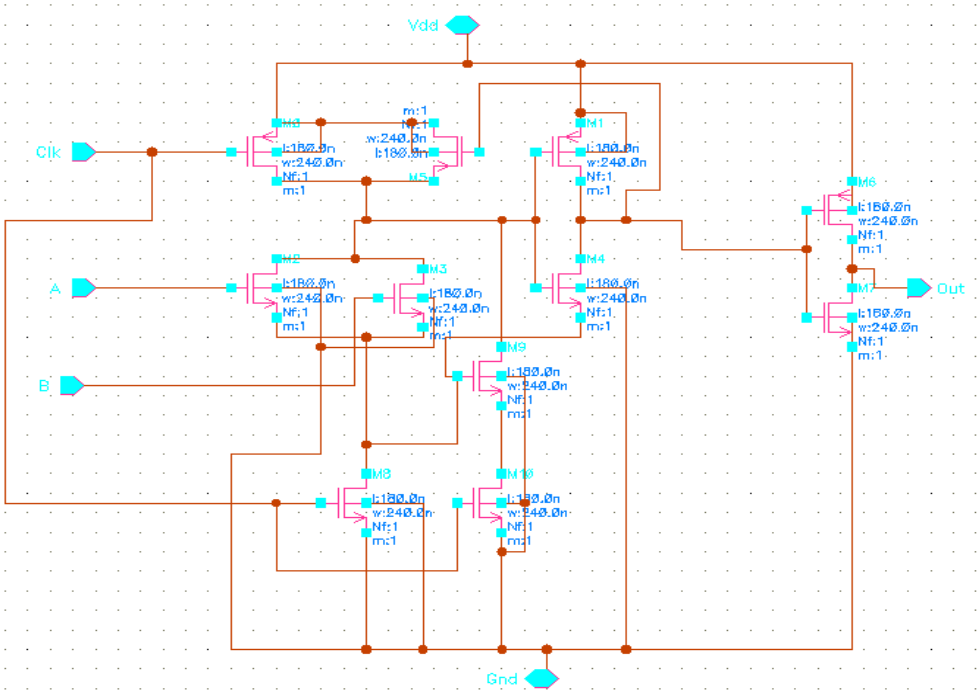


Fig.6.7 Proposed 2-input NOR gate schematic

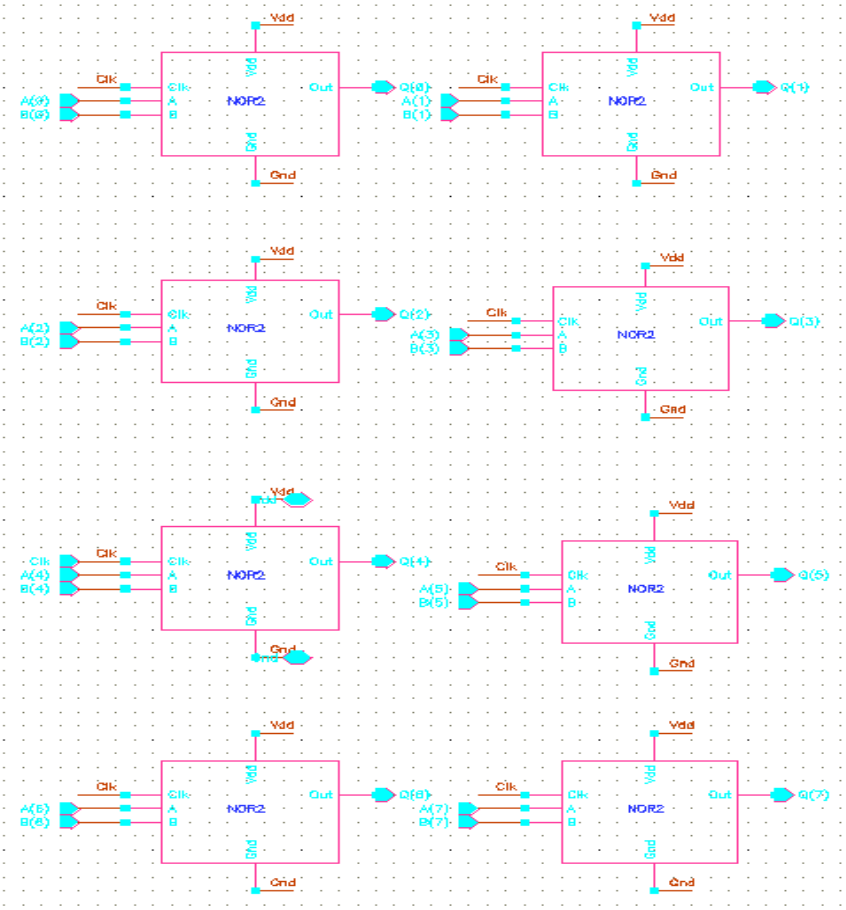


Fig.6.8 Proposed 8-input NOR gate schematic

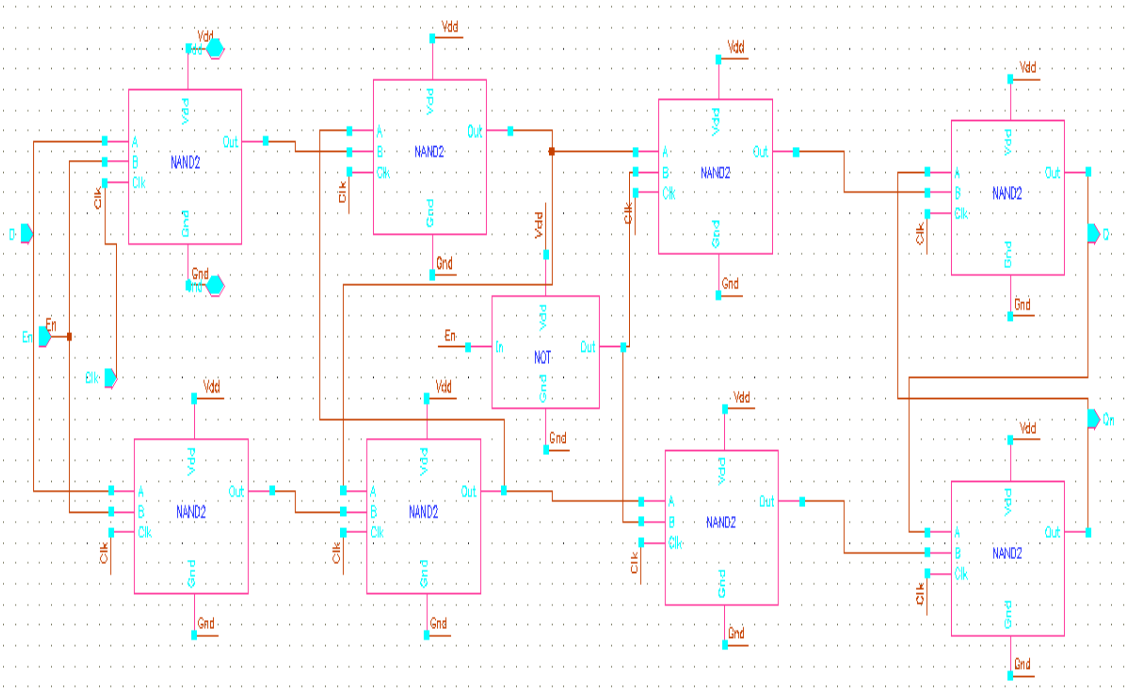


Fig.6.9 Proposed D-FF schematic

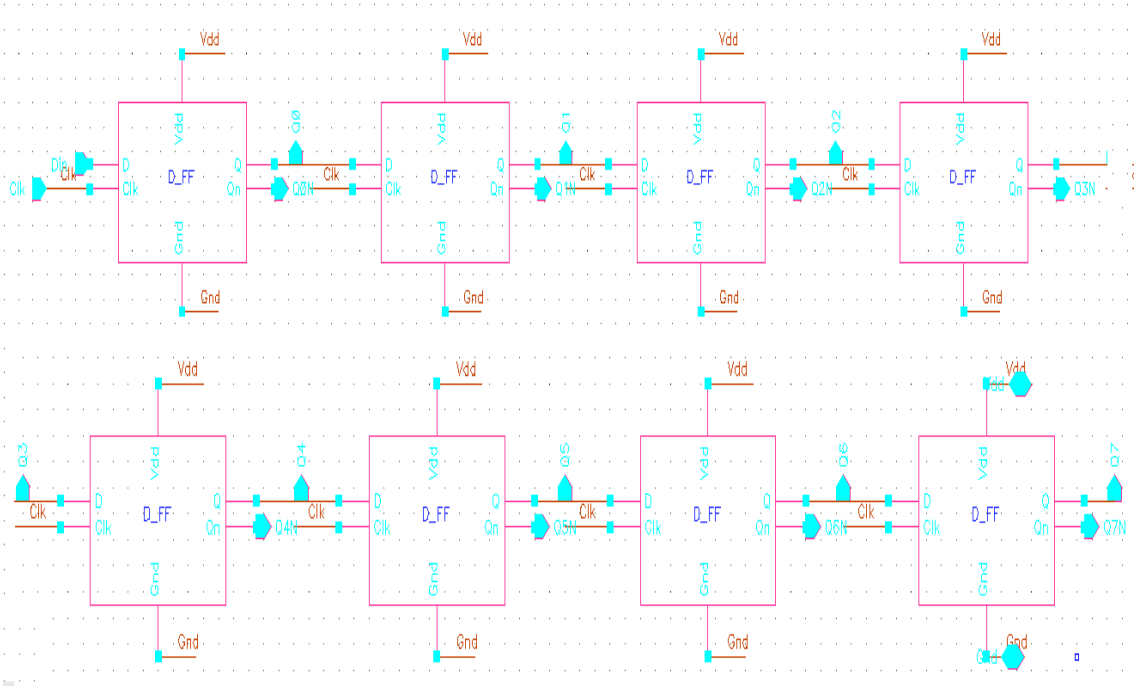


Fig.6.10 Proposed Shifter schematic

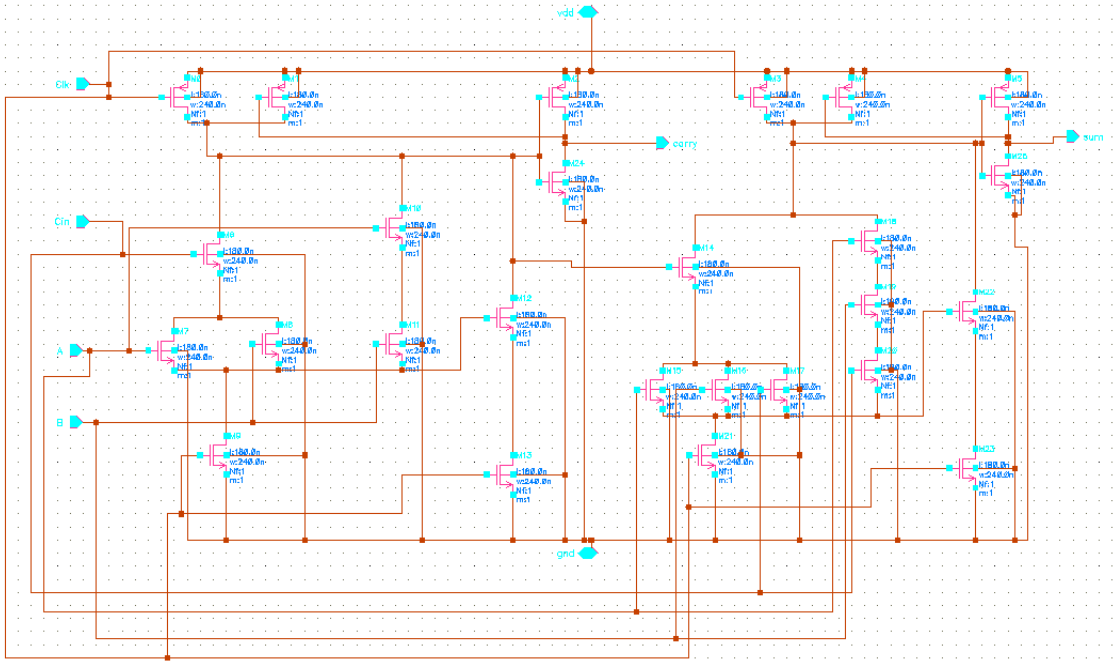


Fig.6.11 Proposed 1-bit adder schematic

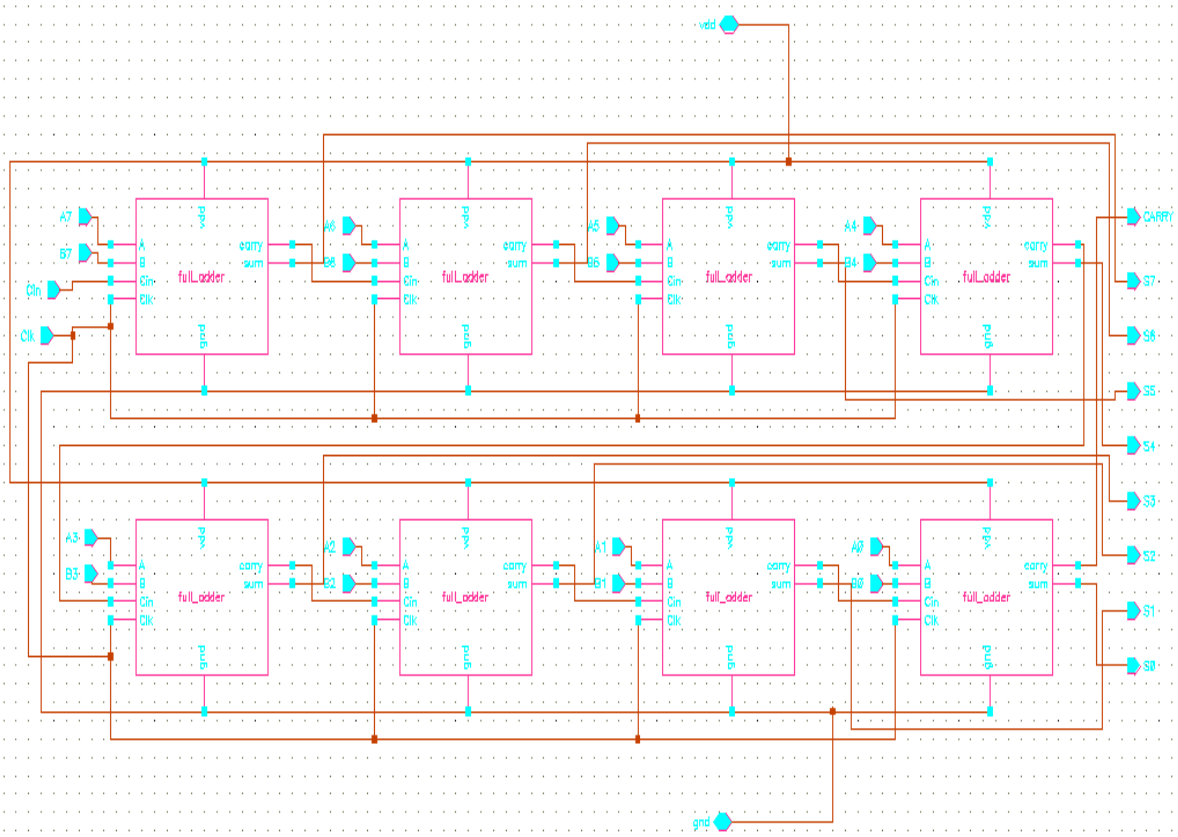


Fig.6.12 Proposed 8-bit adder schematic

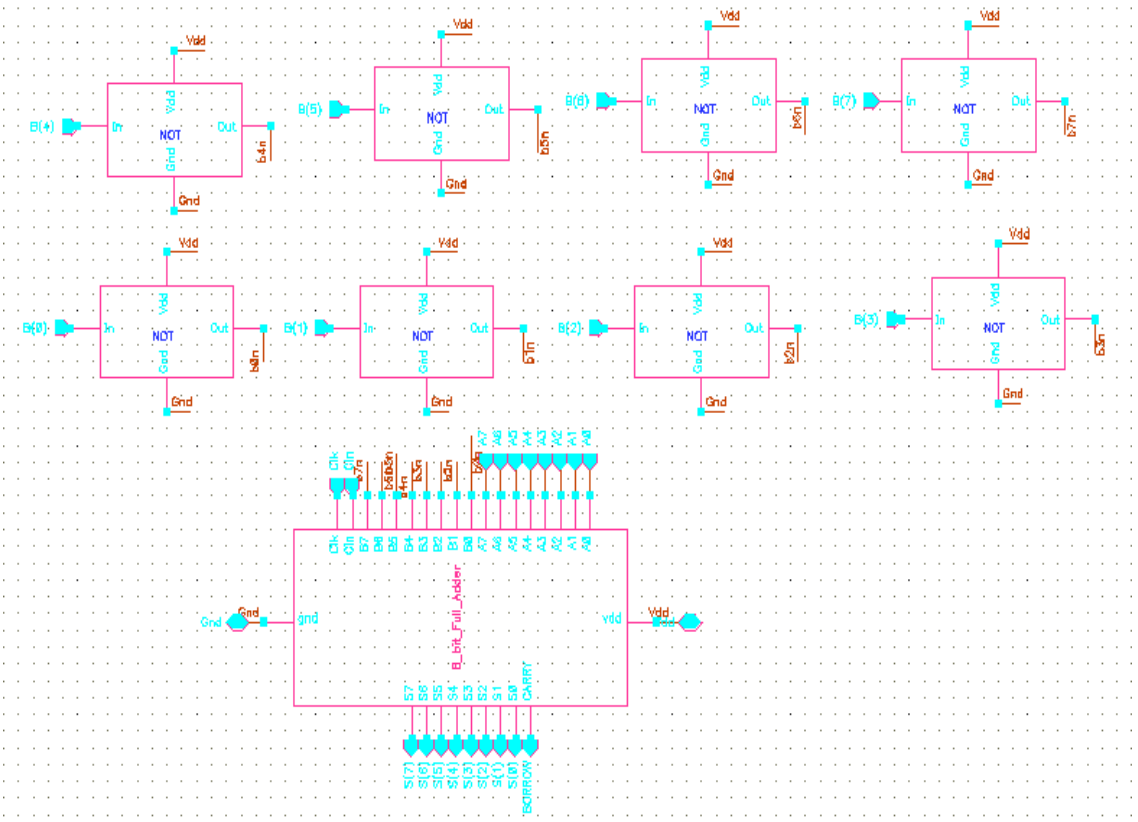


Fig.6.13 Proposed 8-bit substractor schematic

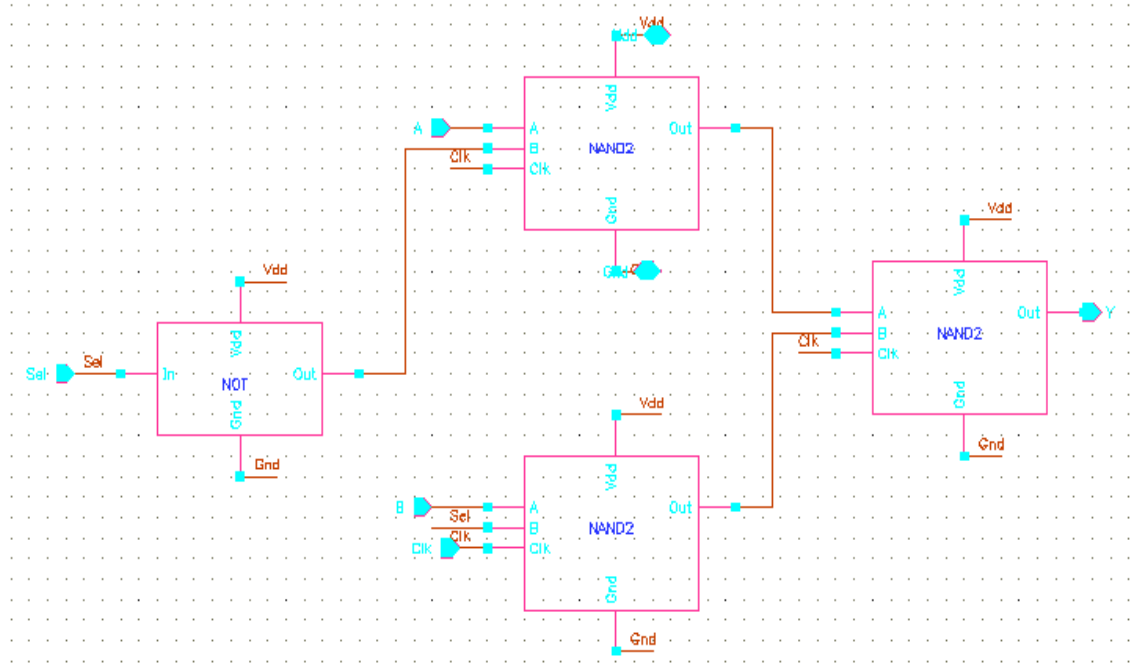


Fig.6.14 Proposed 2-bit mux schematic

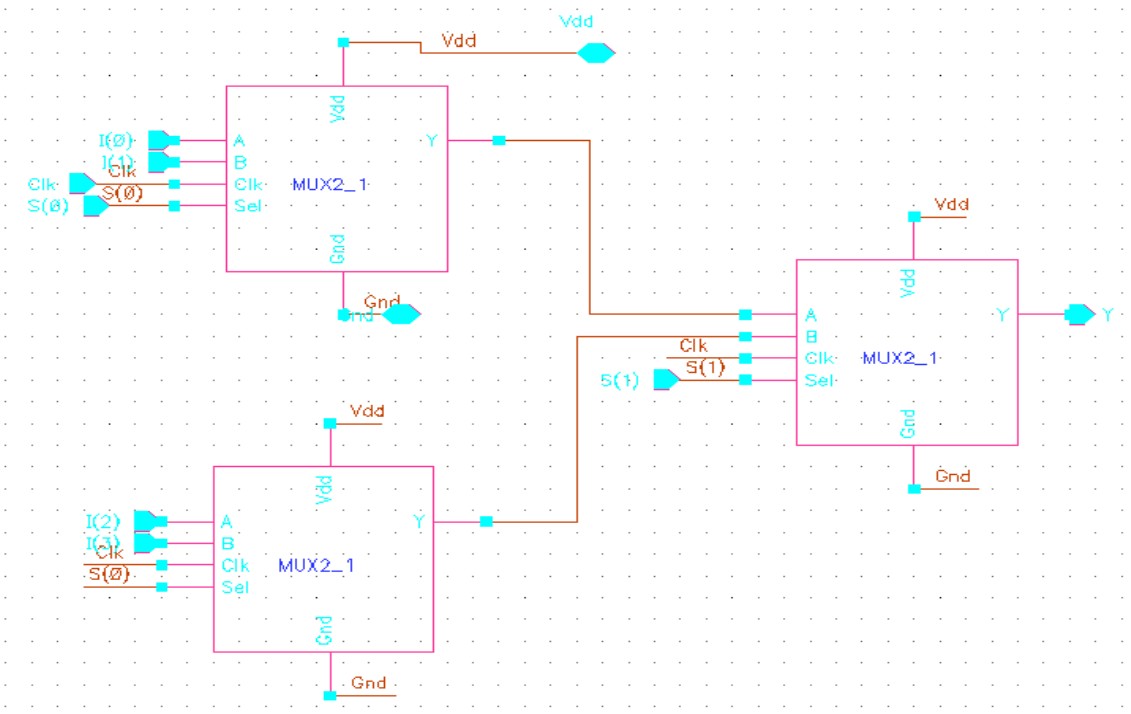


Fig.6.15 Proposed 4-bit mux schematic

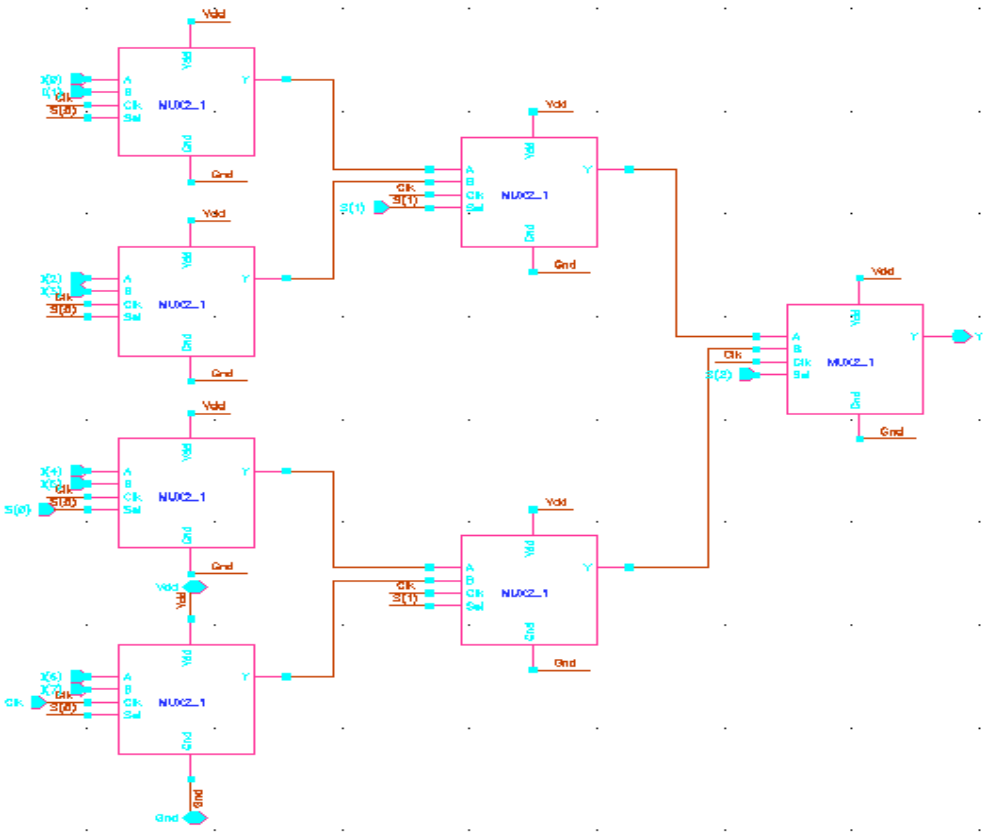


Fig.6.16 Proposed 8-bit mux schematic

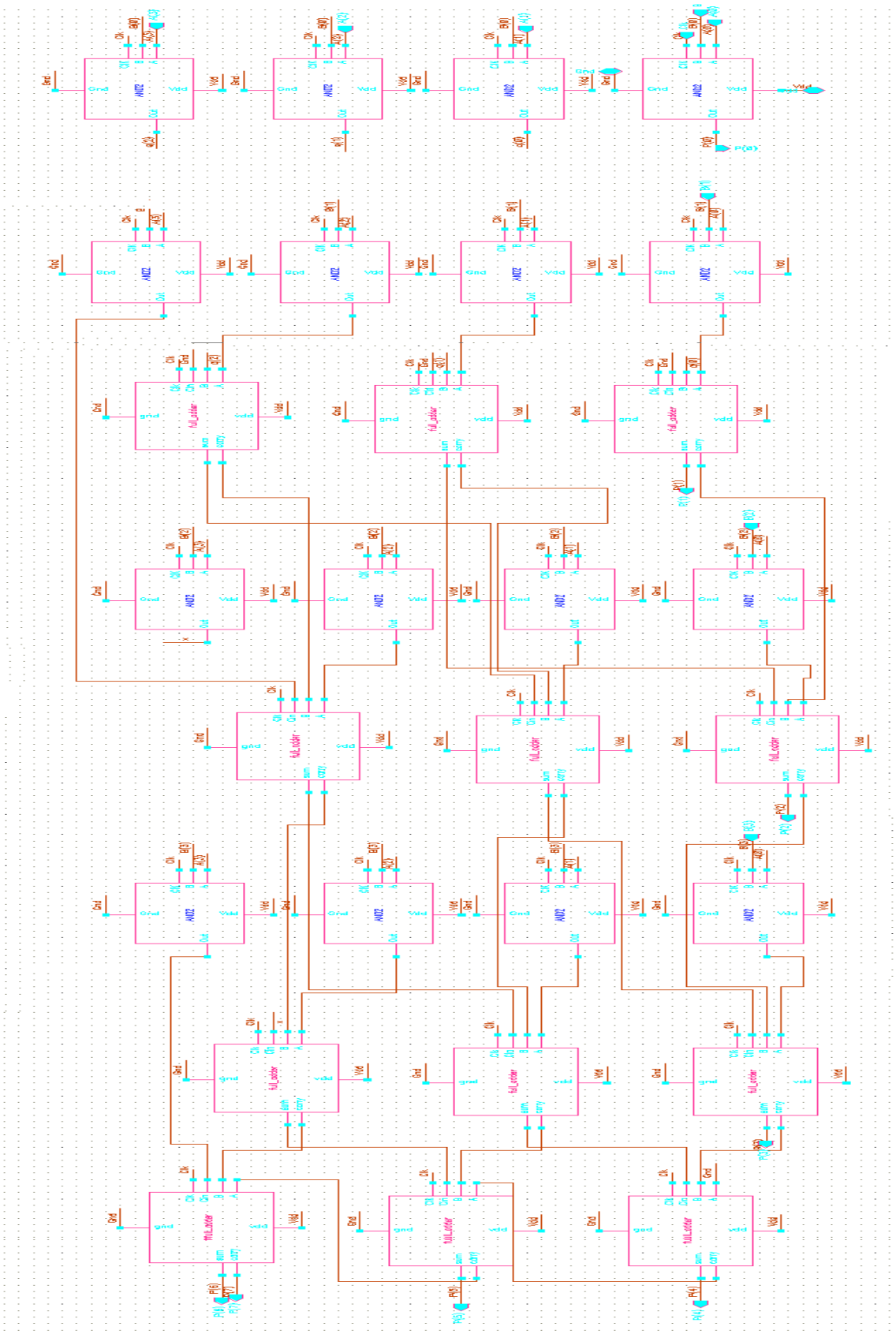


Fig.6.17 Proposed 4-bit multiplier schematic

Fig.6.3 depicts the proposed 2-input XOR gate which is used for the ALU design. Fig.6.4 shows the 8 bit XOR gate designed by cascading 8 numbers of 2-input XOR gates. This feeds as inputs A [0, 7] and B [0, 7] and gives XOR output Q [0, 7]. Fig.6.5 presents the proposed 2-input NAND gate which is used for the ALU design. The 8-bit NAND gate was designed by cascading 8 numbers of 2-input NAND gates as depicted in Fig.6.6. This feeds as inputs A [0, 7] and B [0, 7] and gives NAND output Q [0, 7]. Fig.6.7 presents the proposed 2-input NOR gate which is used for the ALU design. The 8-bit NOR gate was designed by cascading 8 numbers of 2-input NAND gates as depicted in Fig.6.8. This circuit feeds as inputs A [0, 7], B [0, 7] and result NOR output Q [0, 7]. All these circuits were designed using proposed CMOS domino logic design described in this thesis.

Fig.6.9 depicts the schematic of 1-bit D-FF designed in cadence spectre 180 nm technologies. This D-FF is designed using 8 NAND gates. 8 numbers of 1-bit D-FFs were cascaded to create one shifter as depicted in Fig.6.10. Fig.6.11 gives the schematic of 1-bit adder circuit designed with 28 transistors in cadence spectre. 8 numbers of 1-bit adders were cascaded to design one 8-bit adder circuit as depicted is Fig.6.12. One 8-bit adder circuit and 8 numbers of NOT gates were combined to form substractor circuit as depicted in Fig.6.13. Here all basic gates were designed using the proposed CMOS logic design using cadence spectre UMC 180 nm technologies and simulated using 500 MHz frequency at a temperature of 27^0 C.

Fig.6.13, Fig.6.14 and Fig.6.15 depicts the schematic of 2:1, 4:1 and 8:1 multiplexor. The 4:1 and 8:1 multiplexor were designed using 3 and 7 numbers of 2:1 multiplexor respectively. Fig.6.17 illustrates the multiplier designed with Braun multiplier style. Braun multiplier is a parallel multiplier, which is commonly called as Carry Save Array Multiplier. This multiplier can perform the multiplication of two unsigned numbers. It contains an array of adders and AND gates. This adders and AND gates are arranged in an iterative structure. This multiplier design does not require logic registers. The full adder and the AND blocks used to design this multiplier were designed using the proposed domino logic style as shown in Fig.6.17.

6.3.3 LAYOUT OF PROPOSED ALU

In full-custom (bottom-up) design flow, creation of layout is one of the most important steps. The designers describe the complete structures and relative placement of all the layers, which is to be used in fabrication. The layout is drawn by means of a Layout Editor. Physical layout design is very closely related to overall circuit performance (speed, area, power dissipation and noise performance), because the physical structure decides parasitic capacitances and resistances, and silicon area. Then a detailed layout of CMOS logic needs a very serious and time-consuming design effort.

A layout design of CMOS logic gates starts with circuit design and initial sizing of CMOS transistors. It is very vital that the layout design essentially should not violate any of the Layout Design Rules, so that a high probability of defect-free fabrication possessing all features of layout can be achieved.

Fig.6.18 to Fig.6.32 show the various internal modules and the layout of ALU.

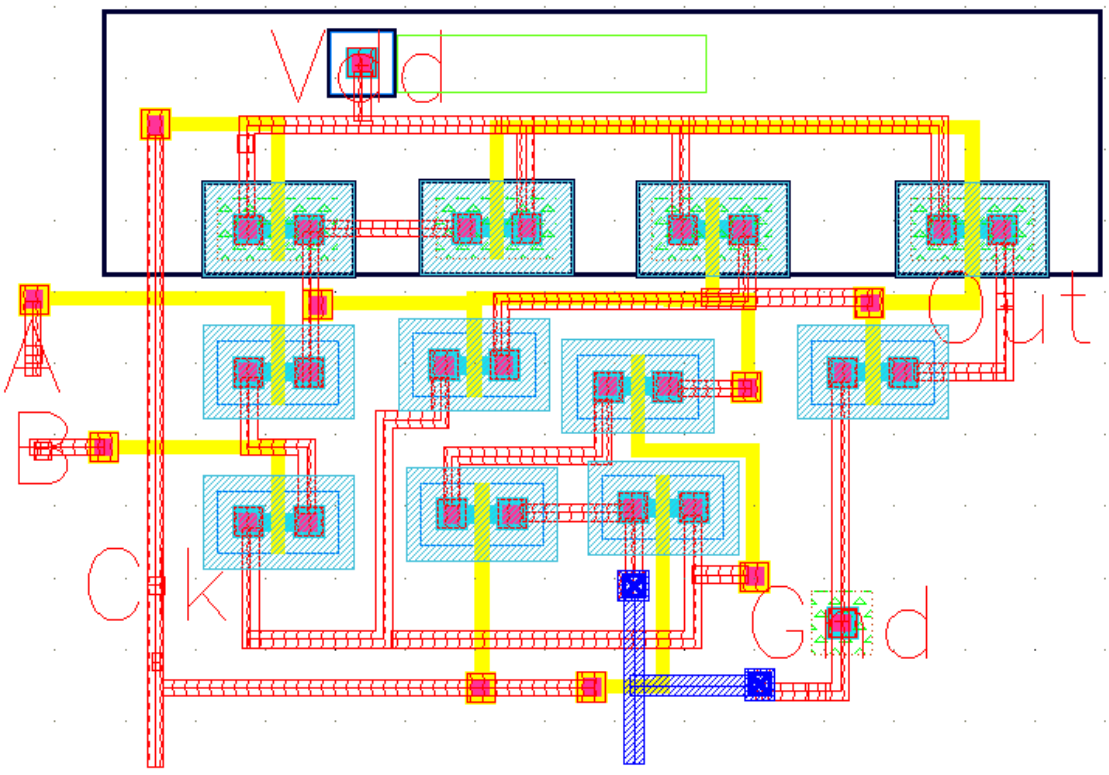


Fig.6.18 Proposed 2-input NAND layout

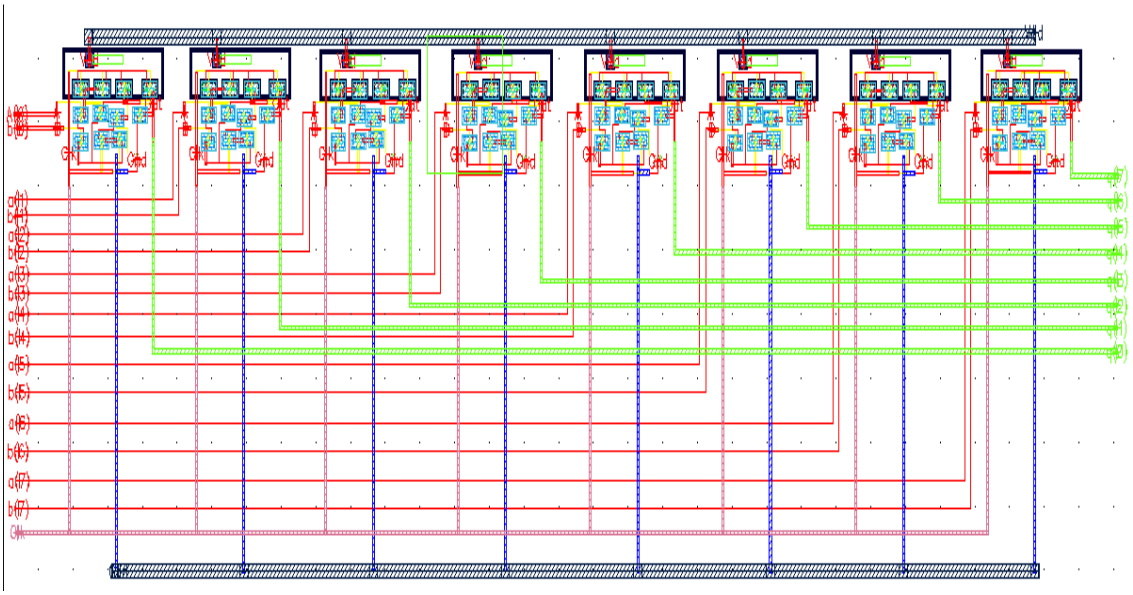


Fig.6.19 Proposed 8-input NAND layout

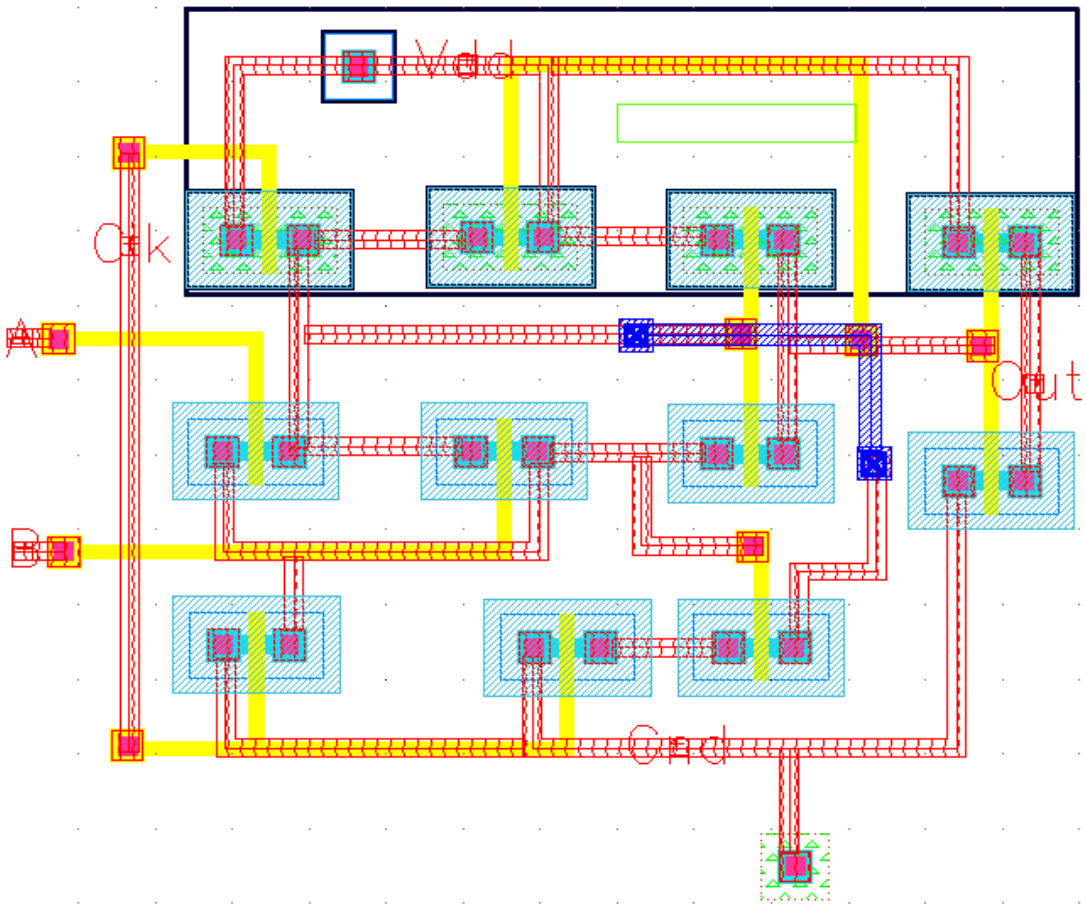


Fig.6.20 Proposed 2-input NOR layout

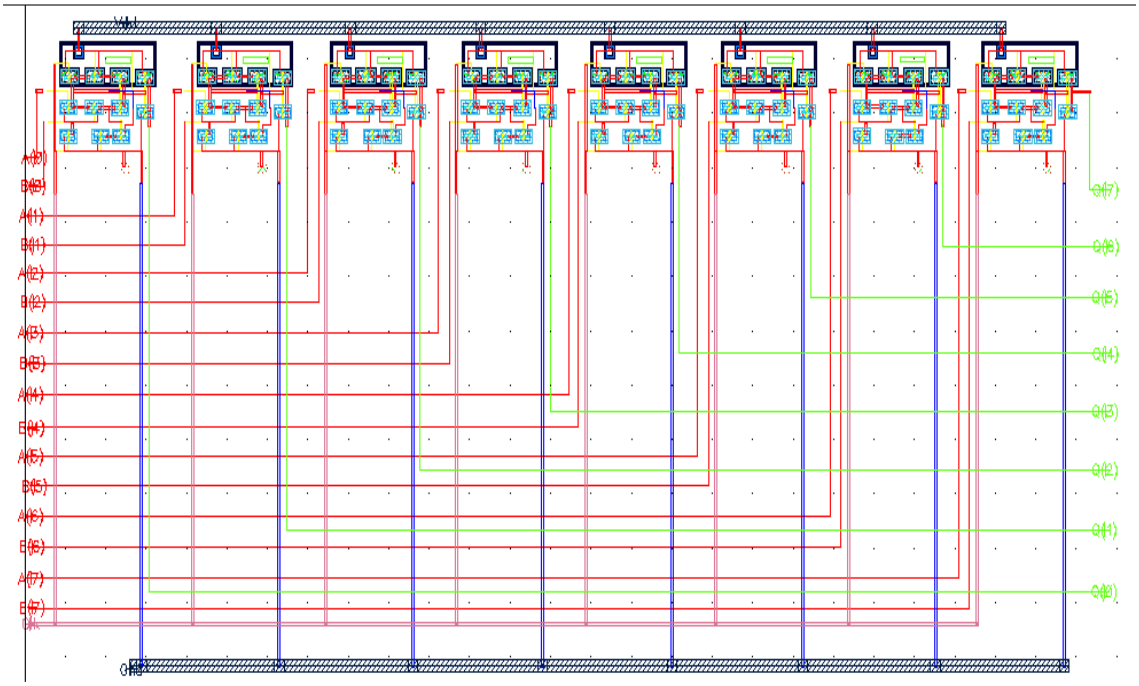


Fig.6.21 Proposed 8-input NOR layout

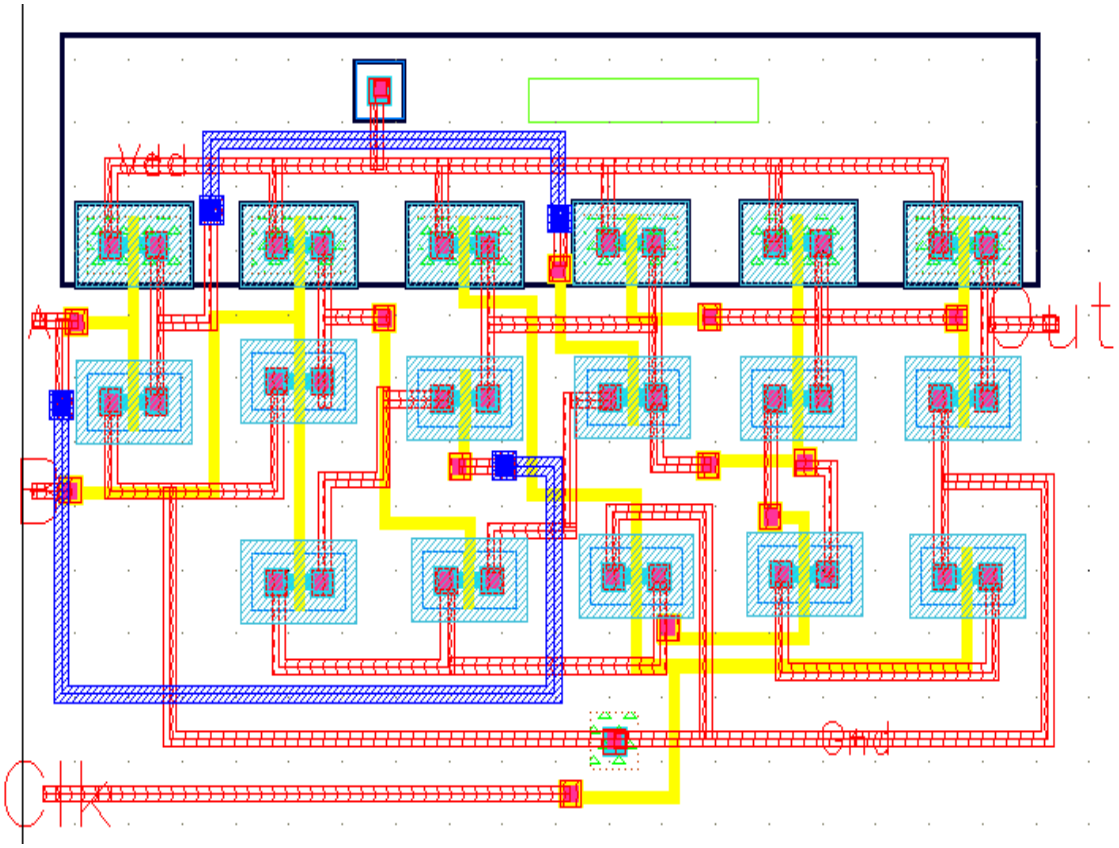


Fig.6.22 Proposed 2-input XOR layout

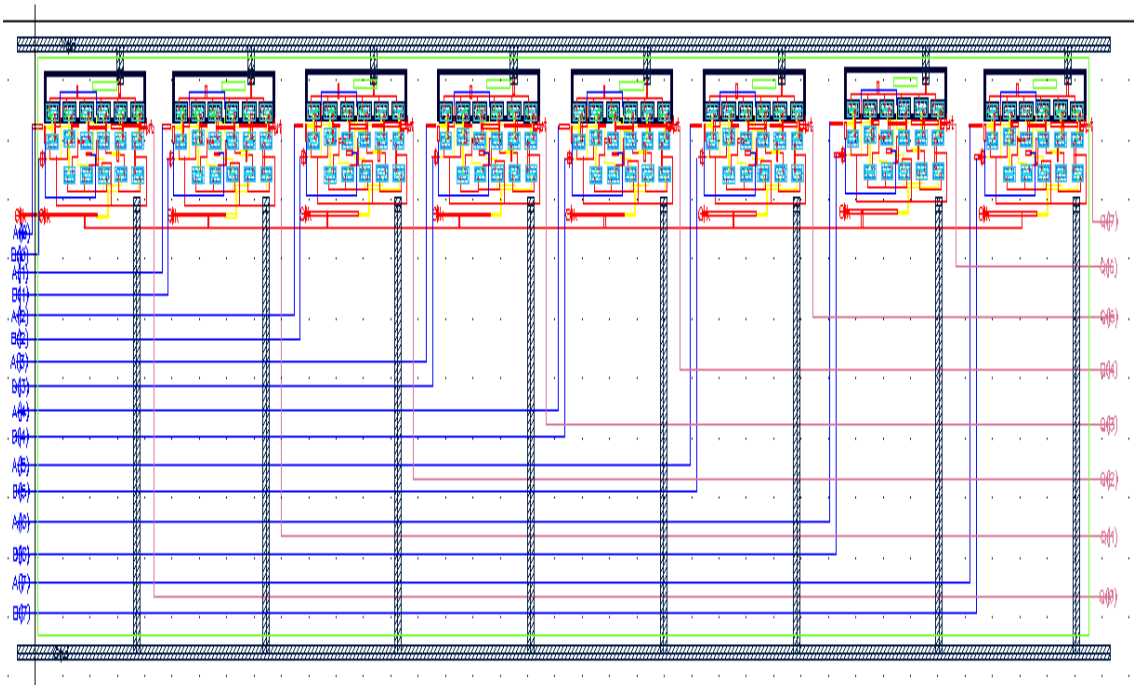


Fig.6.23 Proposed 8-input XOR layout

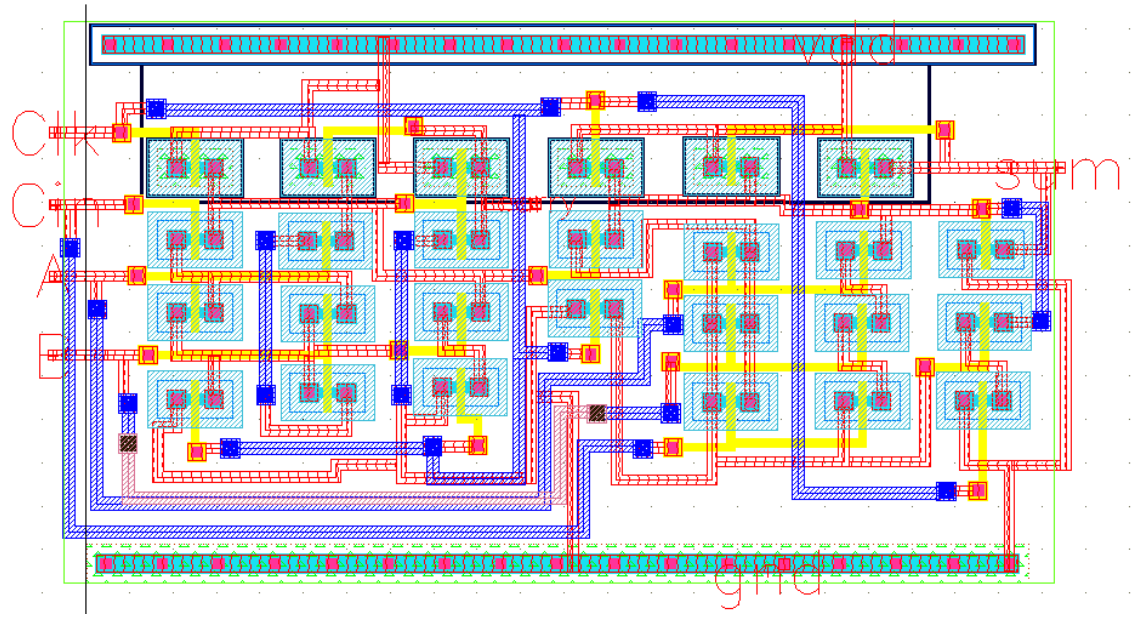


Fig.6.24 Proposed 2-bit adder layout

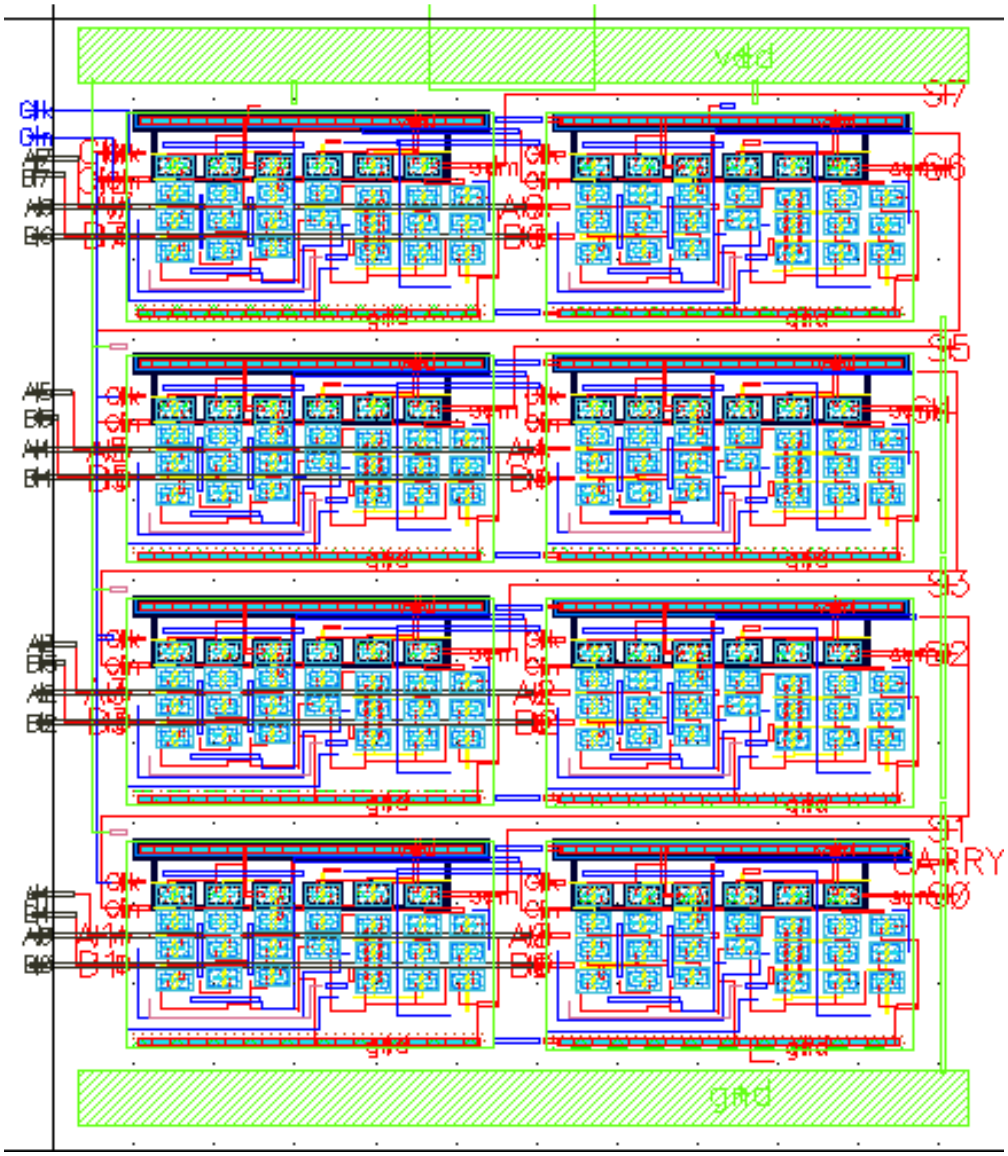


Fig.6.25 Proposed 8-bit adder layout

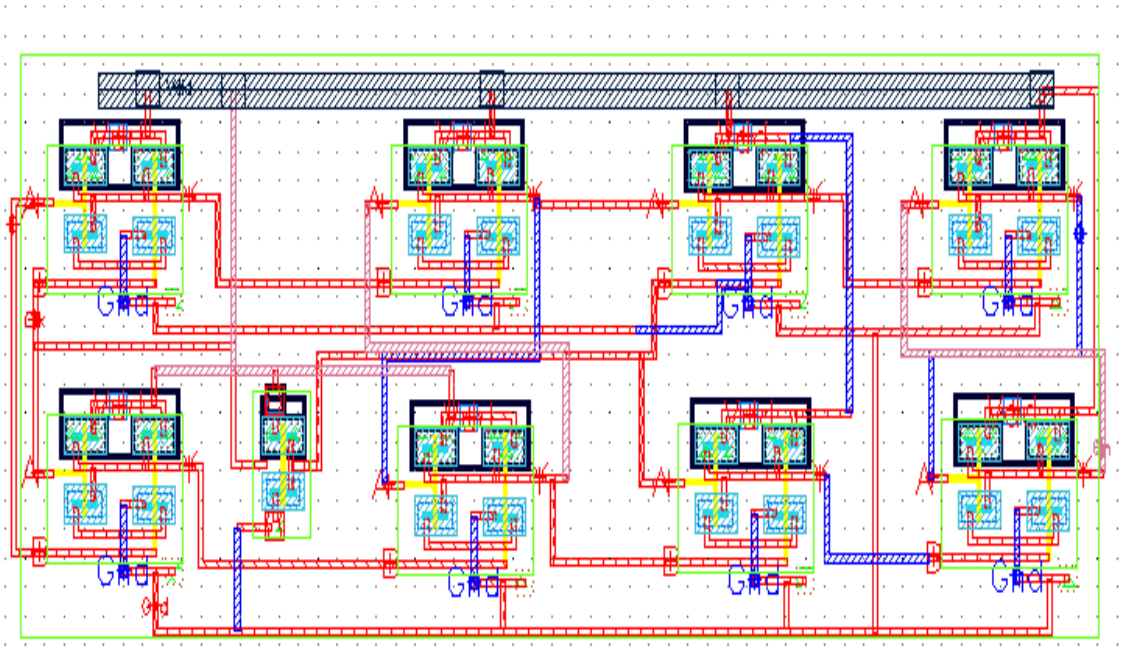


Fig.6.26 Proposed D-FF layout

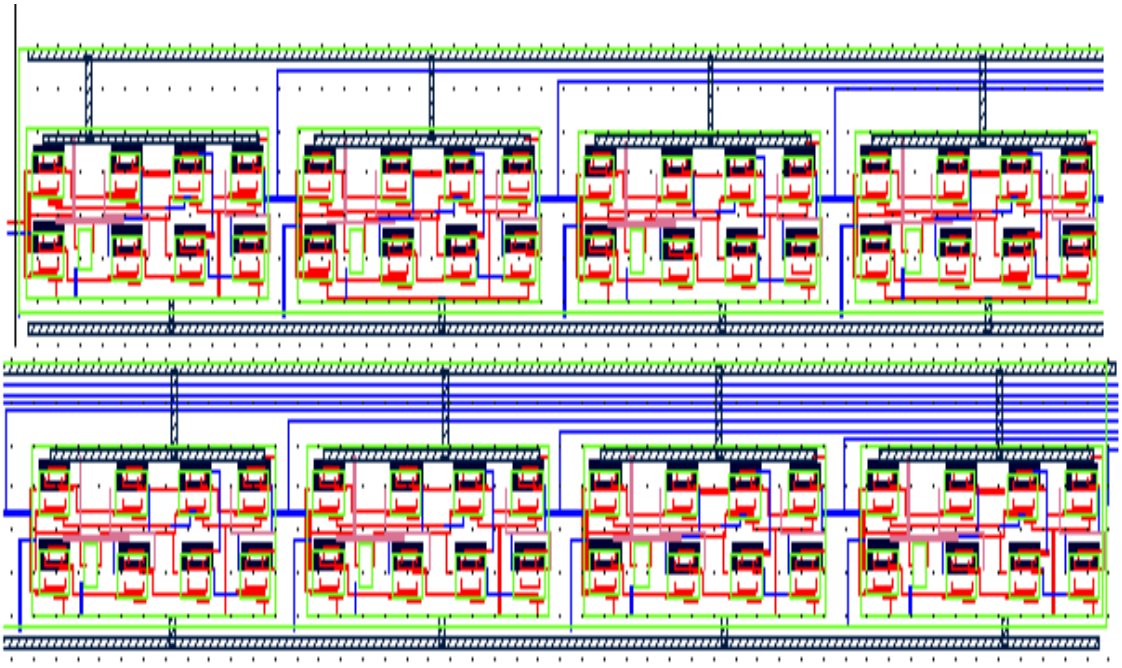


Fig.6.27 Proposed 8-bit shifter layout

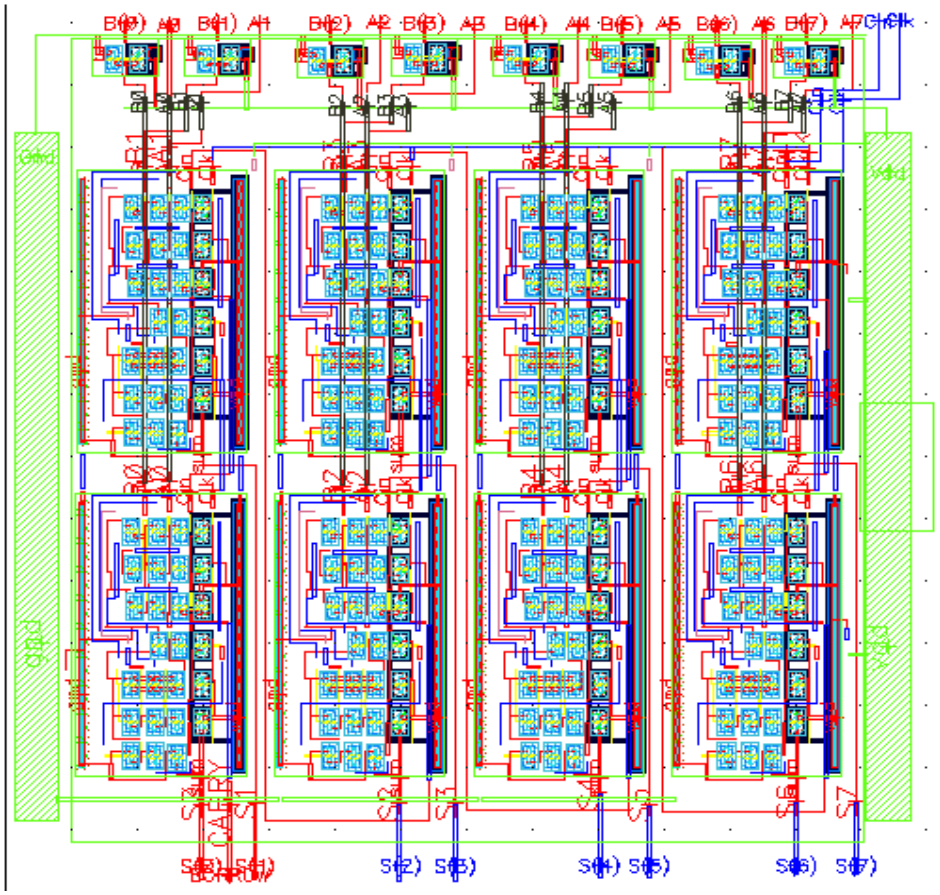


Fig.6.28 Proposed 8-bit Substractor layout

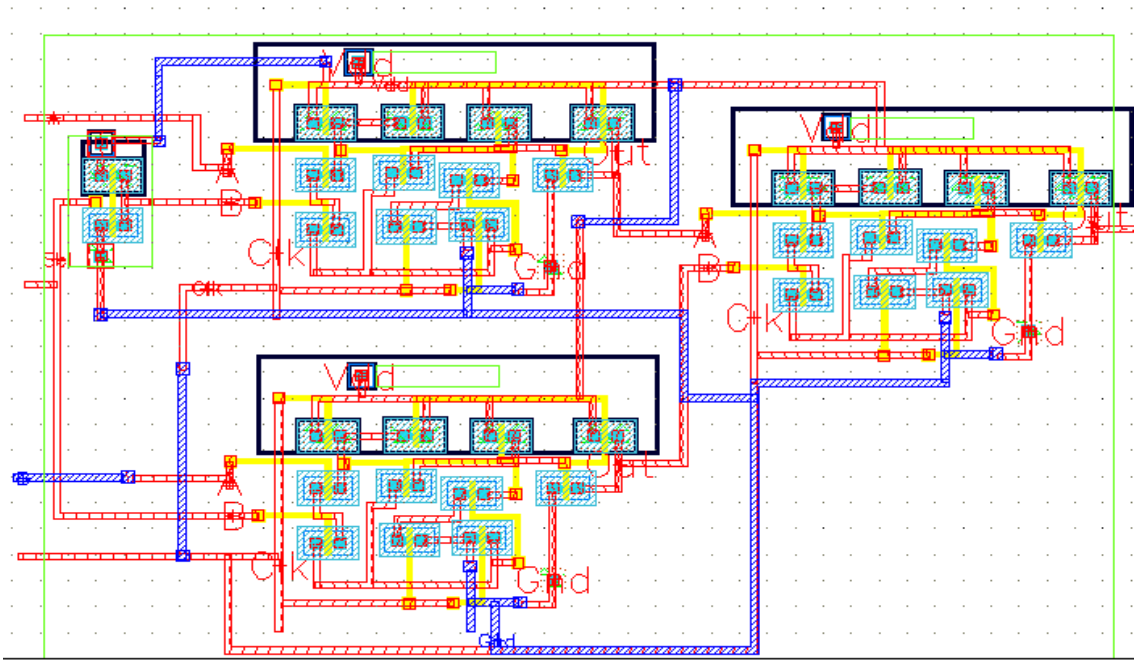


Fig.6.29 Proposed 2:1 mux layout

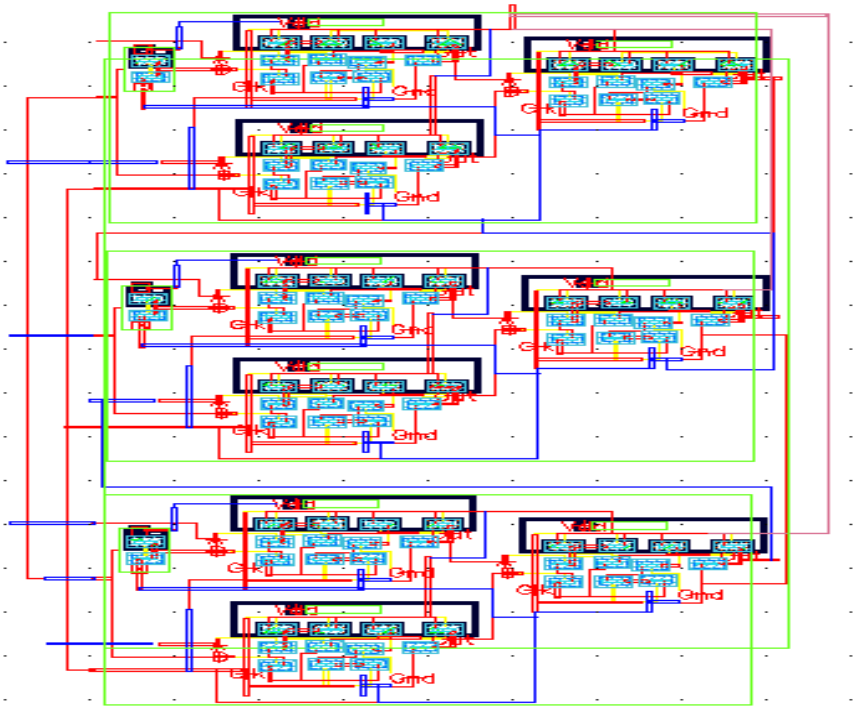


Fig.6.30 Proposed 4:1 mux layout

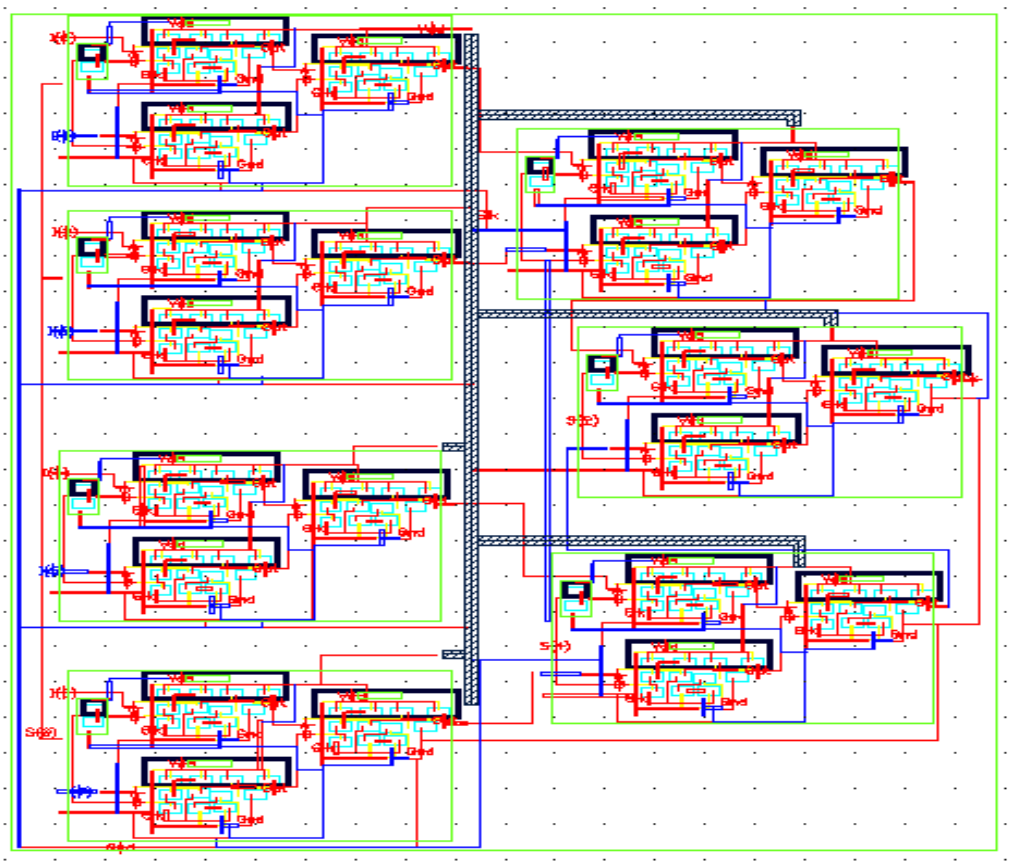


Fig.6.31 Proposed 8:1 mux layout

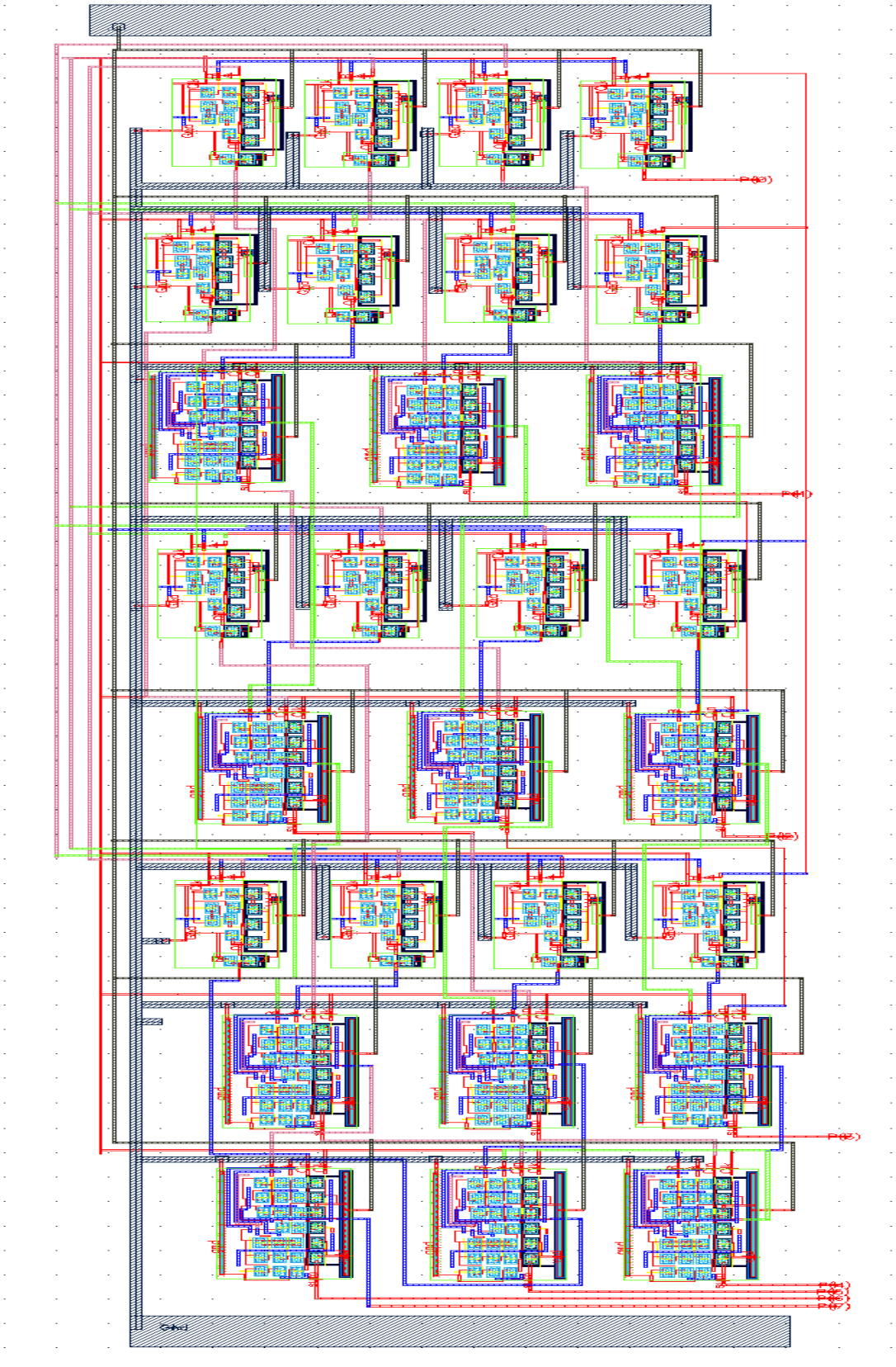


Fig.6.32 Proposed multiplier layout

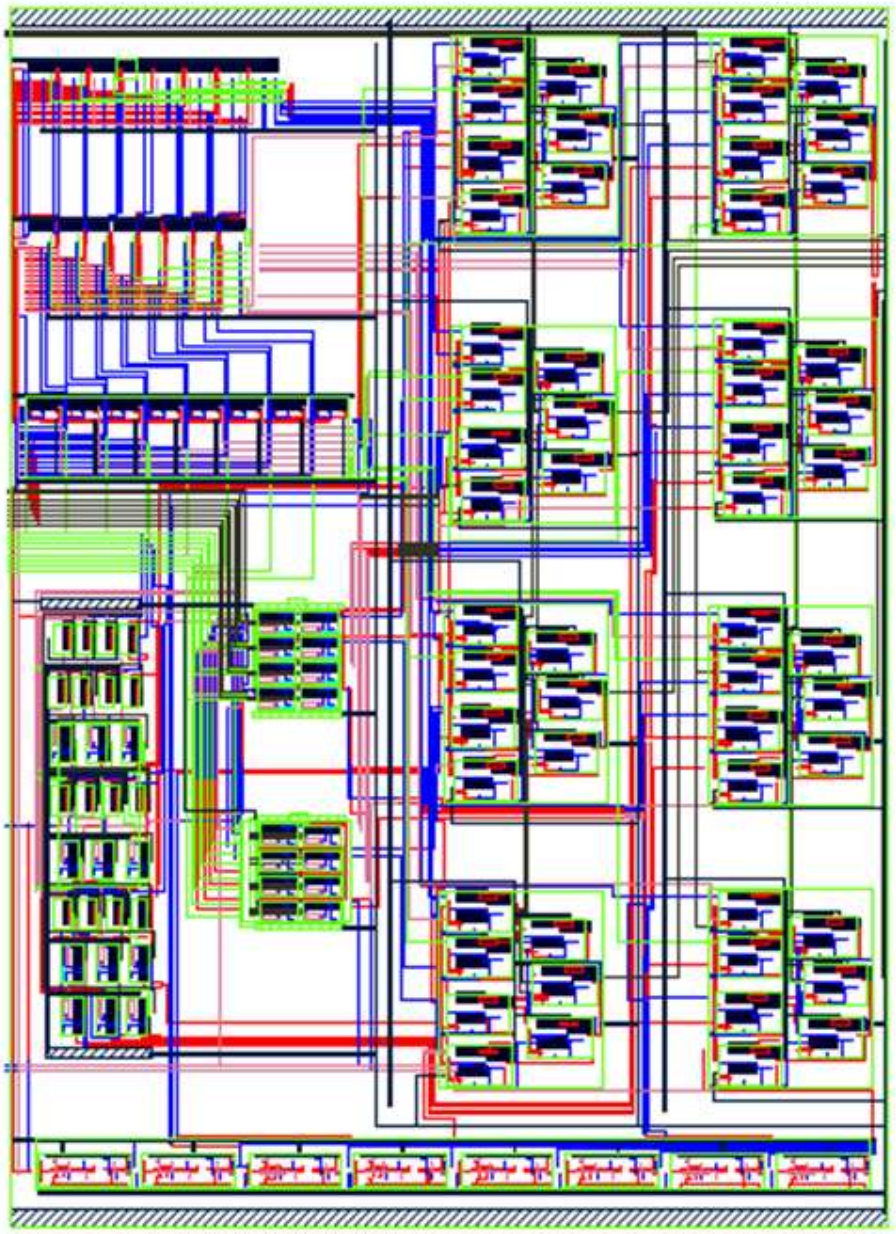


Fig.6.33 Layout of proposed ALU

6.3.4 CREATING I/O PINS

After completion of layout the input and output pins which are present in schematic are added to layout along with V_{DD} and GND.

6.3.5 DRC CHECK

The mask layout, which is created, has to conform to a complex set of design rules, with the purpose of guaranteeing least probability of defects in fabrication. A tool called as Design Rule Checker is built into the Layout Editor, which identifies any design rule violations during and after the mask layout design. DRC is used to check all process-specific design rules. There are technology specific design rules which describe how closely the layers can be placed together. These rules provide the minimum requirement to avoid failure of circuit due to fabrication fault. If the layout is done perfectly then it shows no DRC error as in the following Fig.6.34.

Fig.6.34 DRC error window

6.3.6 LVS CHECK

After the DRC is completed then the layout is checked compared to the schematic created earlier. This is called as "Layout versus Schematic" (LVS), to verify that layout is equivalent to schematic. If all the connections between components in schematic and layout are matched properly, then this LVS run shows that the schematic and layout matched, as shown in following Fig.6.35. A successful LVS does not guarantee that the extracted circuit will surely satisfy all the required performances.

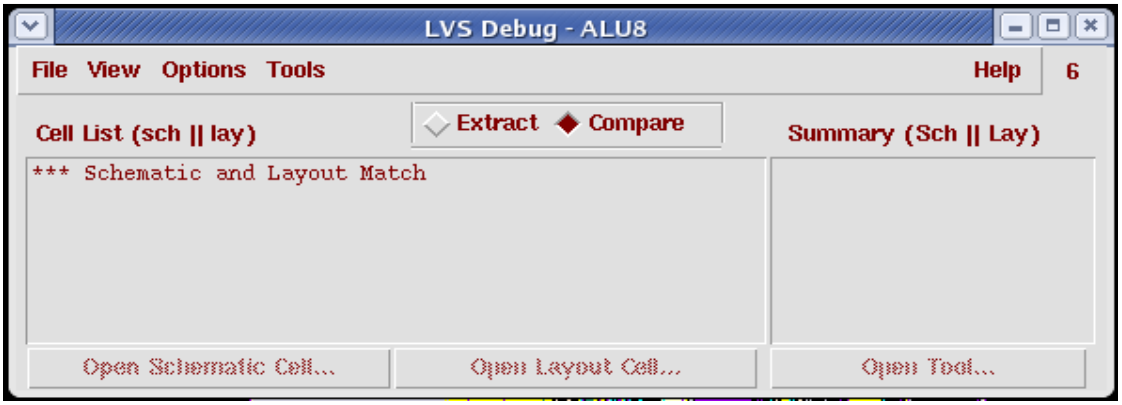


Fig.6.35 LVS run window

6.3.7 PARASITIC EXTRACTION

After completion of DRC & LVS the parasitic resistance and capacitance of layout is extracted by performing RCX extraction, which is called as av_extracted view. The av_extracted view of proposed ALU can be found out. After generation of av_extracted view post-layout simulation is performed. A configure window as shown in Fig.6.36 is generated to do post-layout simulation.

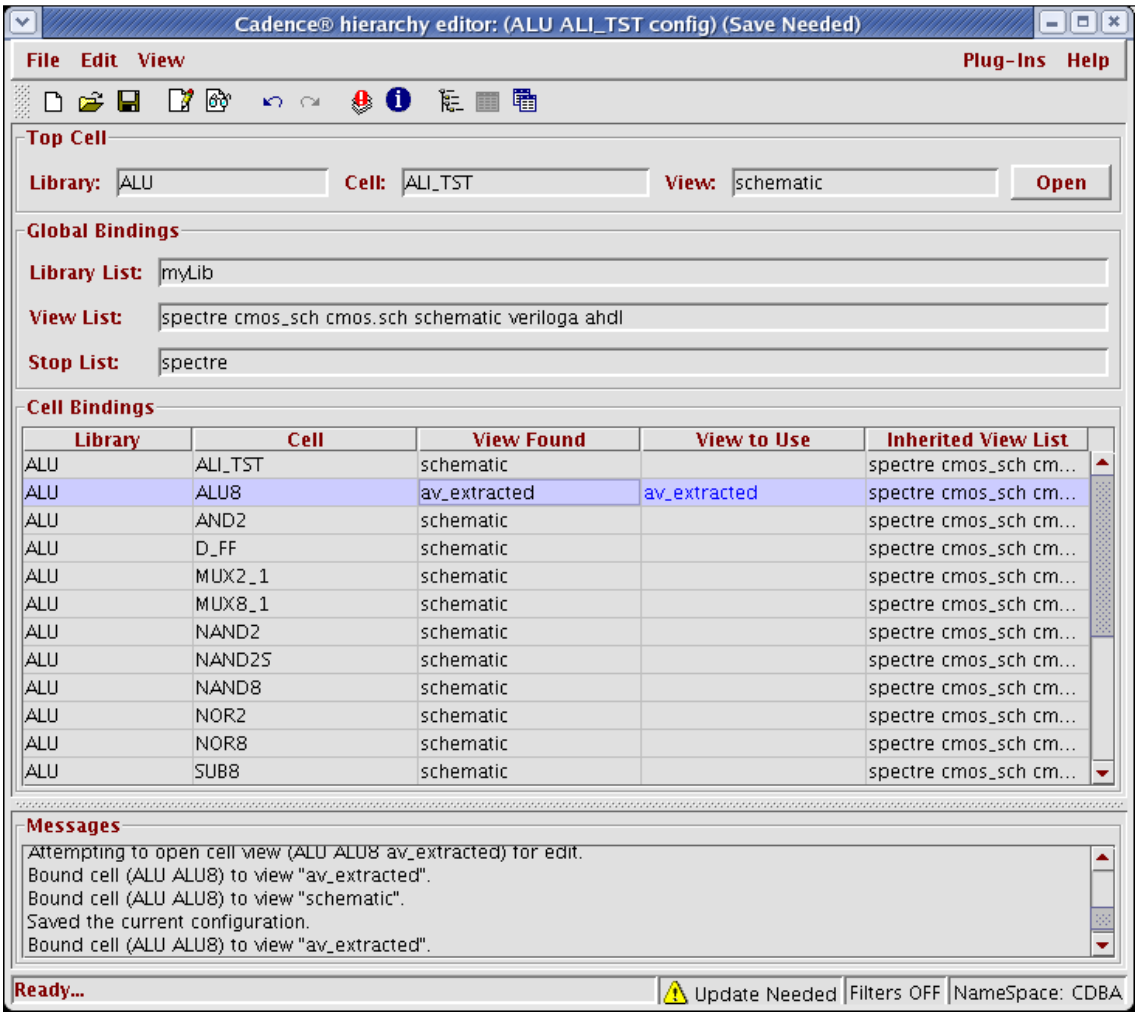


Fig.6.36 Configure window of 1-bit ALU for av_extracted view

6.3.8 POST LAYOUT SIMULATION & PERFORMANCE ANALYSIS

After parasitic extraction of ALU layout is over then we carried out post layout simulation. The post layout simulation results were compared with pre layout simulation. The post layout simulation result was done by using UMC 180 nm technology using the tool

cadence spectre. To demonstrate the proper operation of the proposed ALU we have taken some case studies.

CASE-I (Multiplication operation)

When selection = 110, A = 00001101, B = 00001010 then, A*B = 10000010.

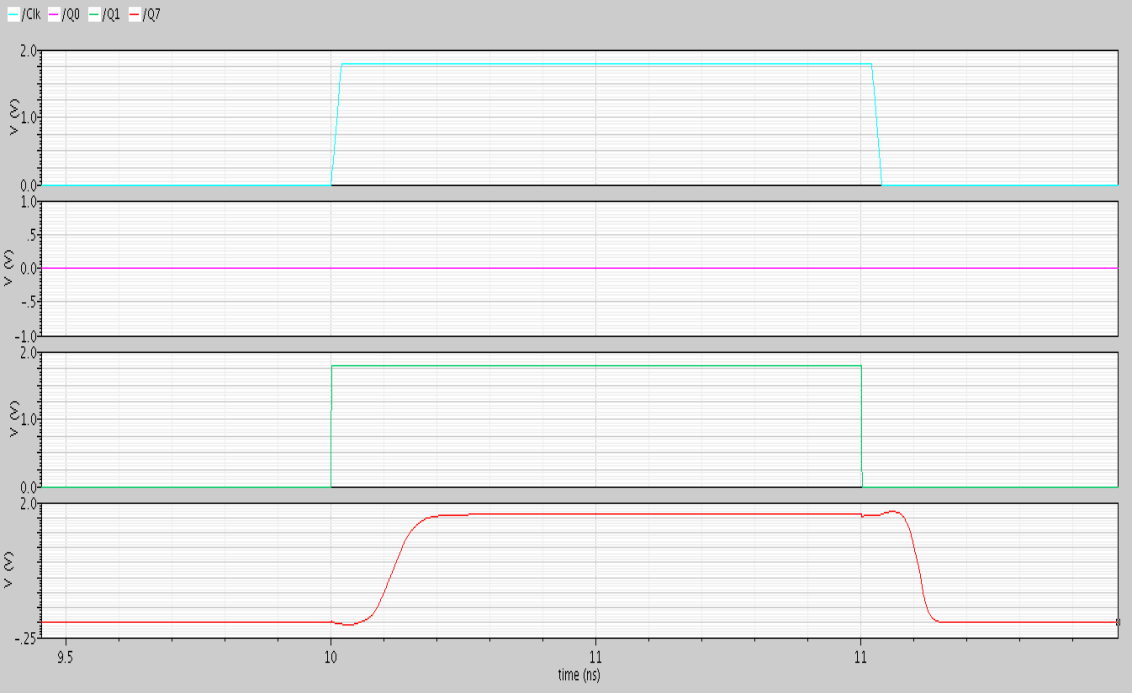


Fig. 6.37 Multiplication output of ALU

Fig. 6.37 depicts the output of the multiplication operation in the proposed ALU. To select the multiplication operation, selection line was set to '110' as shown in Table 6.1. Input A was set to '00001101' and input B was set to 00001010. The output was found out in the ALU was Q = 10000010. Here first waveform shows the clock input, second, third and fourth waveforms show the Q_0 , Q_1 and Q_7 bits. Fig. 6.38 shows the power consumption of the proposed ALU for multiplication operation and Fig. 6.39 shows the delay of the Q7 bit from the clock. Fig. 6.38 and Fig. 6.39 also compare the power and delay of the pre-layout and post-layout simulation when simulated for 8-bit multiplication operation in the proposed ALU.

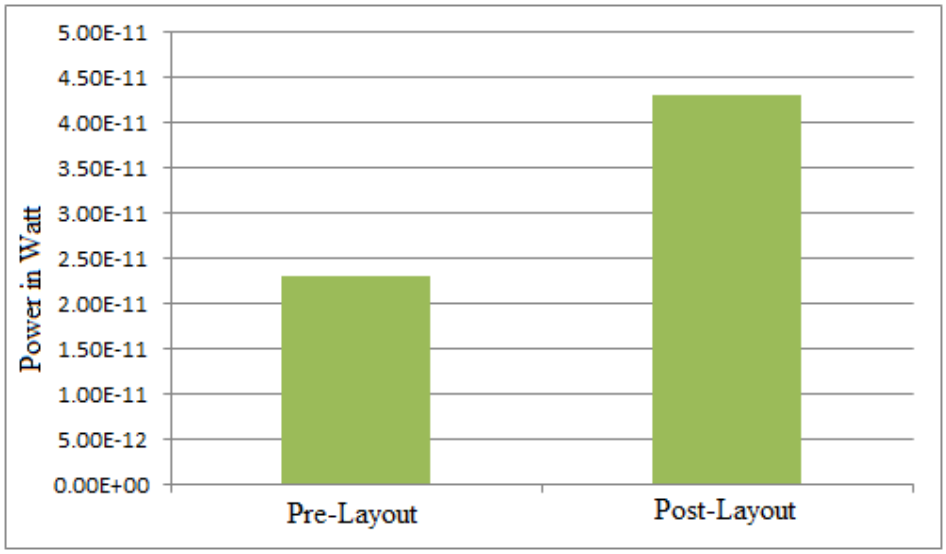


Fig. 6.38 Pre-layout and post-layout power comparison for multiplication operation

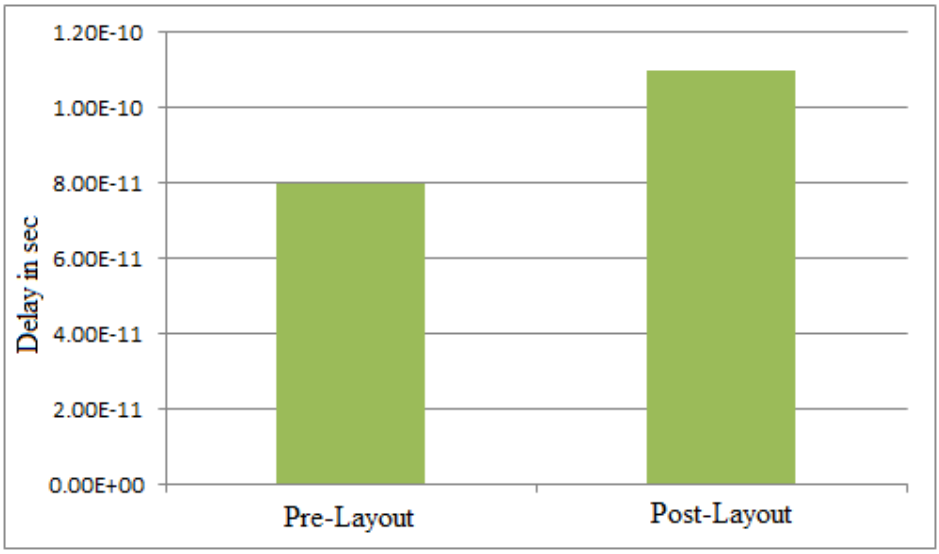


Fig. 6.39 Pre-layout and post-layout delay comparison for multiplication operation

CASE-I (Right Shift Operation)

When selection = 111, A = 10000001 then, after every positive edge trigger one bit right shift occurs as shown in Fig. 6.40.

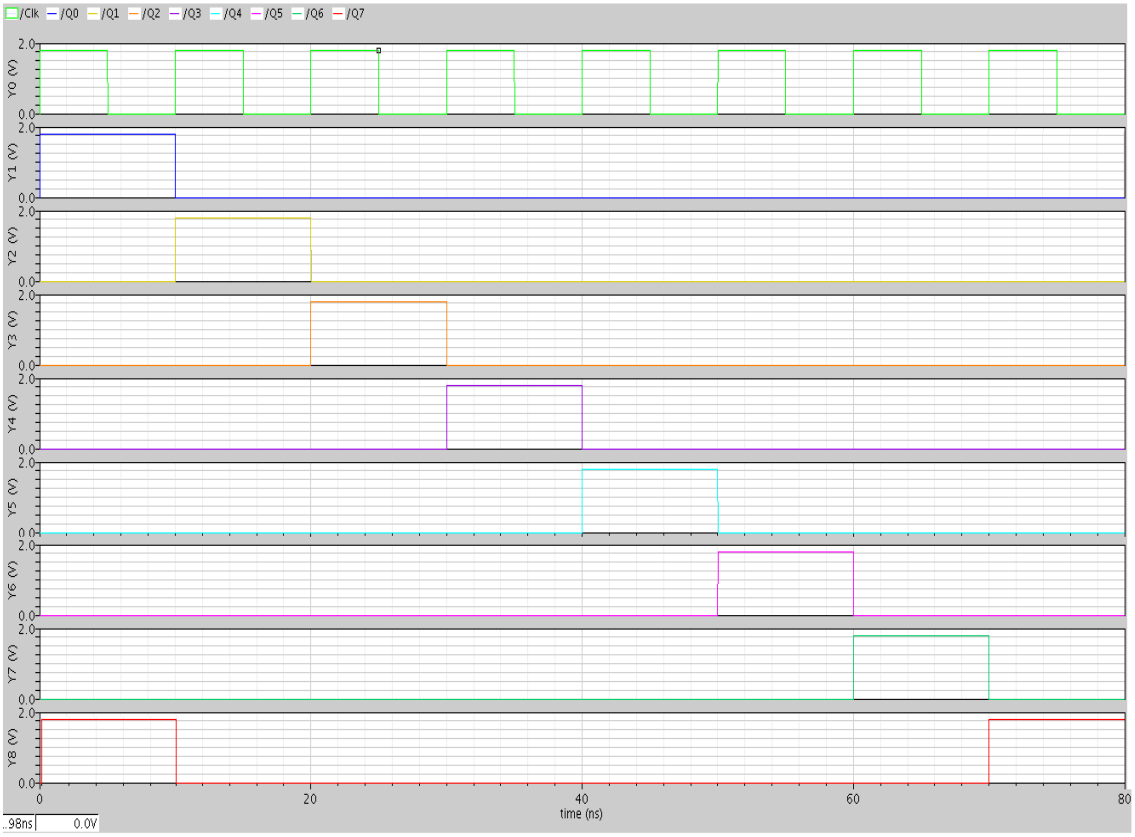


Fig. 6.40 Right shift operation of ALU

In case-II to select the right shift operation of ALU the select line was set to '111'. The input A was taken as '10000001' and right shift operation was done. Fig. 6.40 shows the output Q_0 to Q_7, where Q_0 was taken as the MSB. Fig. 6.41 shows the power dissipation of the ALU at the time of right shift operation and it also shows the difference in power consumption in case of pre and post-layout simulation. Fig. 6.42 compares the clock-Q_0 delay of pre-layout and post-layout simulations. In the post layout simulations the delay and power dissipation of circuit is getting more due to the presence of parasitic components present in the circuit.

The post layout simulation result was done by using UMC 180 nm technology using the tool cadence spectre. In Fig.6.43 post-layout delay comparison of the proposed ALU with ALU designed with basic dynamic logic is shown. Here delay of the ALU circuit was found out by changing the simulation voltages of both the ALUs. In this graph X-axis shows the different simulation voltages with which the ALU circuits were simulated and Y-axis shows delay of the ALU circuits. It can be found that ALU designed with the proposed logic

performs 50-60% faster than the ALU designed with the basic dynamic ALU. Proposed ALU is also 60-70 % less power consuming than the ALU designed with basic dynamic logic.

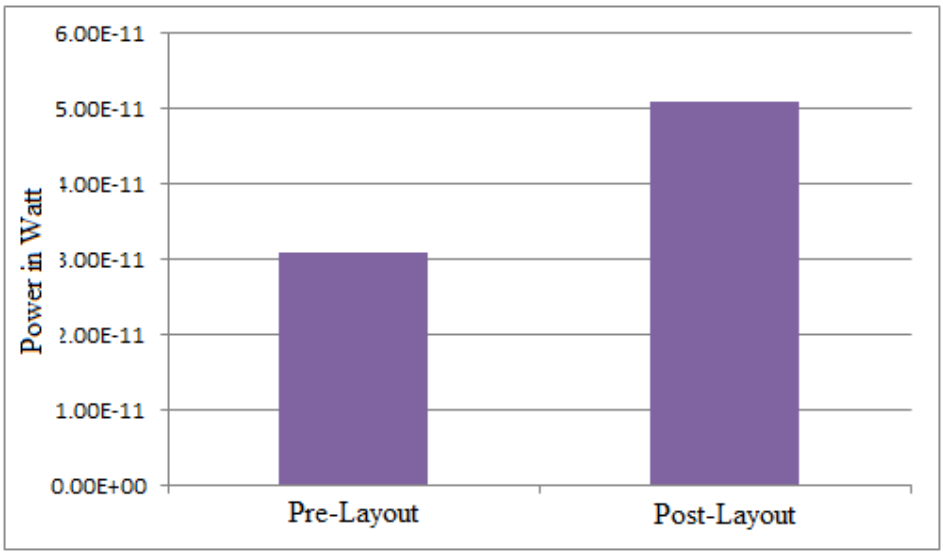


Fig. 6.41 Pre-layout and post-layout power comparison for right shift operation

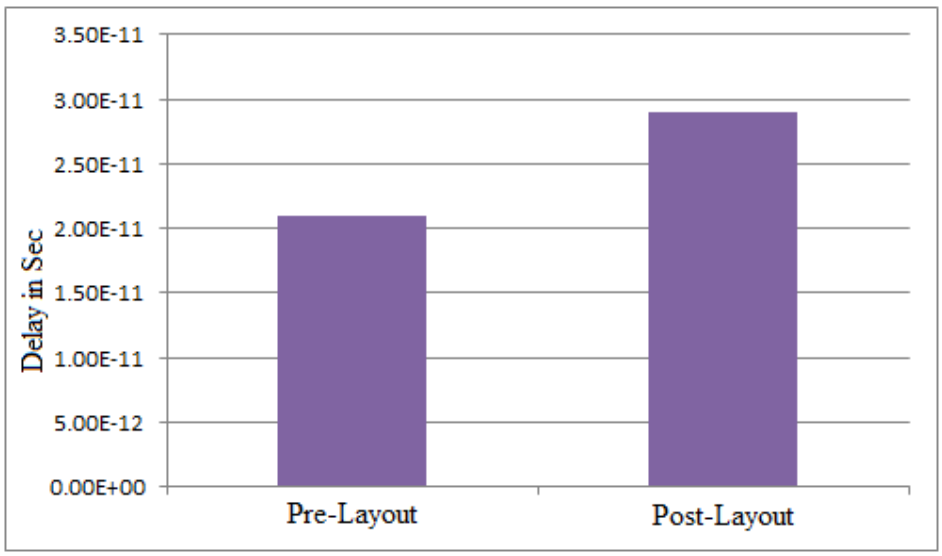


Fig. 6.42 Pre-layout and post-layout delay comparison for right shift operation

Here the proposed ALU gets the benefit on power consumption due to less switching activity of the output node as described in chapter 3. This analysis verifies the performance of the proposed ALU designed with UMC 180 nm technology. Both the figures Fig.6.43 and Fig.6.44 validate the enhanced performance of new ALU. The results of this section validate the performance of proposed adder circuit with a very small variation in post layout results.

The proposed ALU has much lower power consumption benefiting from the no pulse propagation to output node and footer transistors.

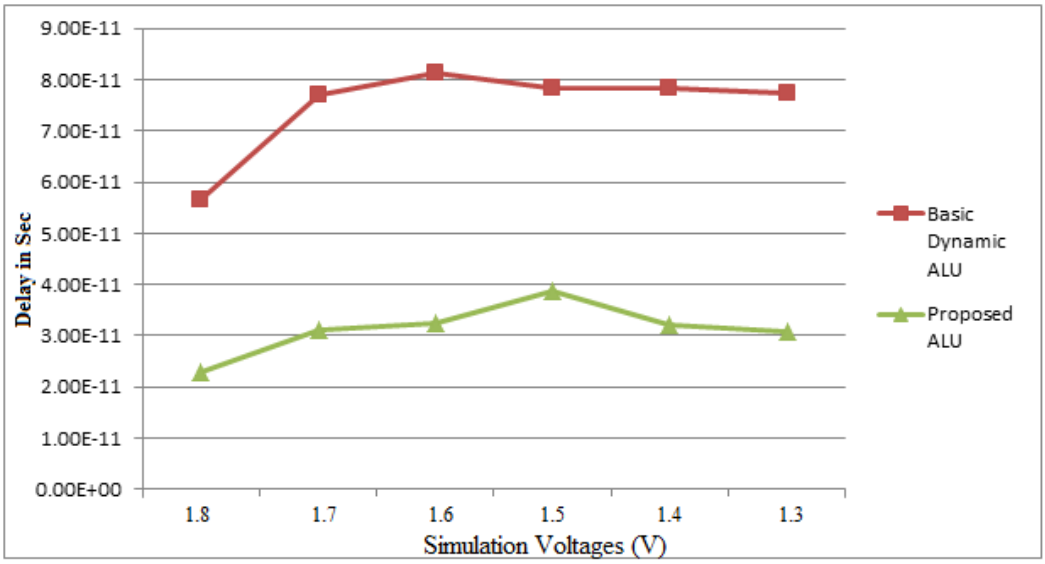


Fig.6.43 Post-layout delay comparison of proposed ALU with ALU designed with basic dynamic logic

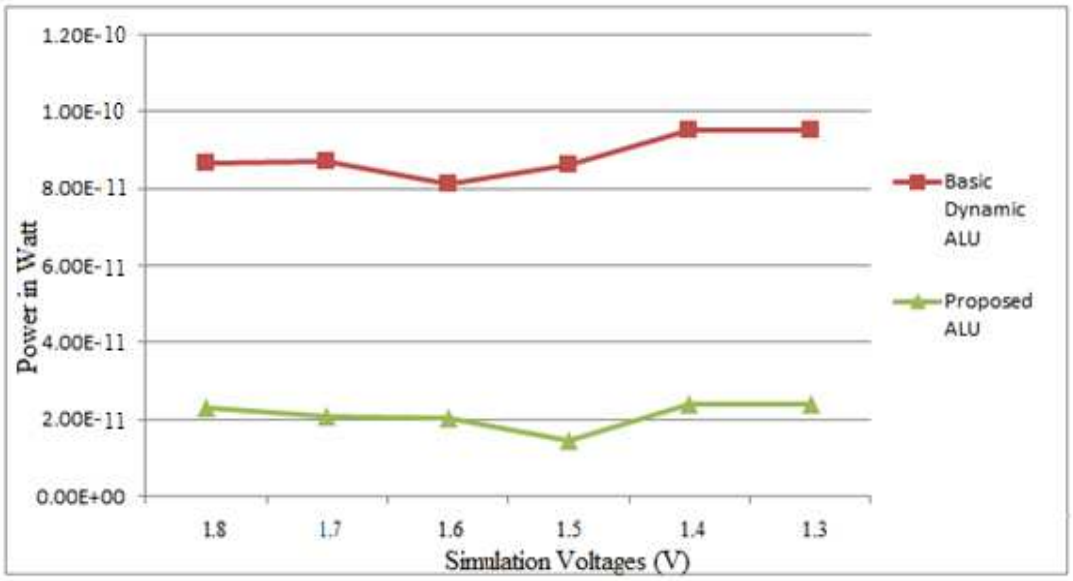


Fig.6.44 Post layout power comparison of proposed ALU with ALU designed with basic dynamic logic

6.3.9 PADDING AND CONNECTIONS

A pad consists of a bonding pad, ESD protection circuit. A bonding pad is an area where the bond wire is soldered. Wire goes from bonding pad to the chip. ESD circuit is electrostatic discharge circuit which is a protecting circuit consisting of a pair of big PMOS and NMOS transistors.

Electrostatic discharge occurs when the charge stored in the human body or other device is discharge to the gate of a MOS transistor on contact or by static induction. This can destroy the MOS transistor so ESD protection is required. The solution is to use clamping diodes implemented using MOS transistors with gate tied up to GND for NMOS and V_{DD} for PMOS.

The bonding pad consists of 3 superimposed squares in Metal 1, Metal 2 and Metal 3 joined together by respective vias (i.e. M_1-M_2 and M_2-M_3). The core of layout contains eight PMOS transistors connected parallel between V_{DD} and signal terminal. Metal 2 layer used to distribute V_{DD} where Metal 1 is used to distribute signal.

The designed test chip consists of 48 pads, 12 on each side. Among the 48 pads, 40 pads are normal I/O pads (10 on each side), 4 are V_{DD} pads (1 on each side) and 4 are GND pads (1 on each side). In between the bonding pads the filler cells are present. The filler cells prevent the contact of pads with each other. Wire goes from these bonding pads to the chip.

Fig.6.45 ALU Testchip shows the final ALU test chip designed with the proposed logic designed using UMC 180 nm technology.

6.4 CONCLUSION

We have designed and submitted for fabrication a testchip demonstrating functional proposed ALUs. Initial simulations indicate that the proposed ALU has lower energy consumption and delay than the equivalent domino logic ALU. We have also simulated and compared the pre-layout and post-layout simulations and demonstrated the small amount of deflection in results in the post-layout performances. This testchip is currently submitted for fabrication.

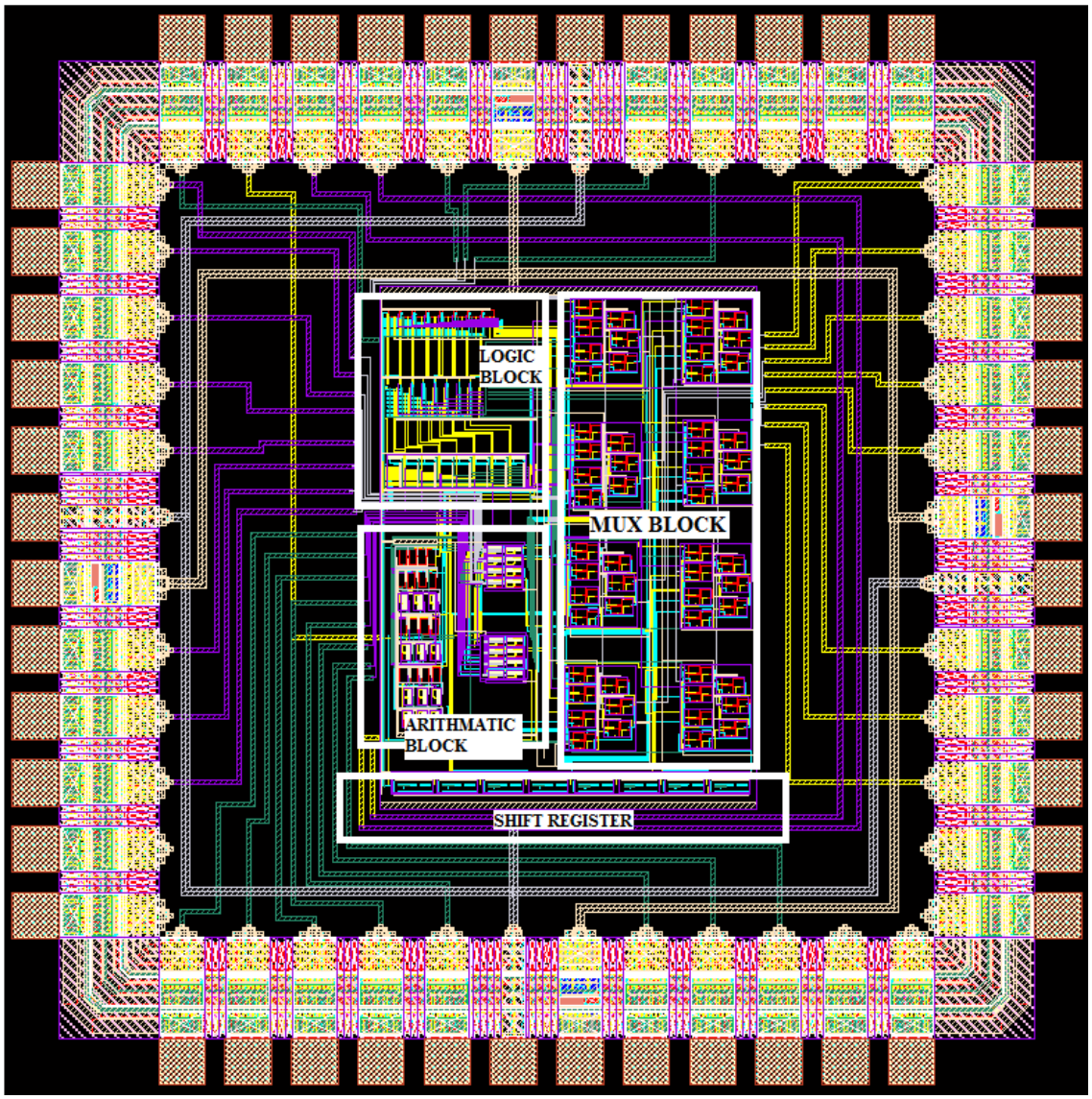


Fig.6.45 ALU Testchip

Chapter 7

CONCLUSIONS AND FUTURE WORK

In this dissertation, we have introduced and demonstrated a novel logic style. This logic consumes low power and is noise robust. This proposed logic is superior to domino and static CMOS logic in addition to some recent proposed logic styles in terms of energy and delay, and at the same time is more noise robust than any logic styles. In particular, we have shown 60 – 80 % power reduction vs. domino and 30 – 50 % speed improvement vs. static CMOS. In addition, we have presented that the logic also works efficiently with sequential circuits.

7.1 SUMMARY OF CONTRIBUTIONS

The main contributions presented in this thesis are:

- **The high performance logic design-**

  To enhance the performance of the domino logic style, we added three extra footer transistors and applied semi-domino logic style to come up with proposed logic style. This semi-domino logic style decreases switching at the output node; this facilitates reduction of power consumption of the circuit. Furthermore, the circuit becomes noise robust. The 3 extra footer transistors enhance the operational speed of the new domino logic which leads to decrease the delay of the circuit. Through extensive simulations the above ideas regarding speed, power and noise were validated. This proposed logic style has been compared with all basic domino logic styles and also some previous proposed logic styles in the same environment. It was found that the proposed logic is 20 – 30 % faster than the basic footed and keepered scheme and also 80 – 90 % faster than scheme [95] and [90]. Furthermore, the less switching activity of the output node

reduces the power consumption of the circuit by 70 % as compared to reference [90]**,** which is its best competitor.

- **Noise reduction-**

  To find the noise tolerance performance enhancement, UNG and ANTE of the proposed circuit and all other circuits were found out. The proposed circuit was found to be 70 – 90 % more noise tolerant than the other basic circuits and the two reference circuits simulated in same environment under UNG (Unity Noise Gain) metric. When compared with reference [90], which is the best competitor, the UNG reaches 10-13 % higher. When compared with basic scheme, scheme [95] and scheme [90] at the parity of UNG, the proposed scheme reaches PDPs 53, 64 and 73% lower respectively that clearly indicates superior feature of the proposed approach.

- **Proposed logic application-**

  Proposed domino logic was applied to design adder and comparator. These adder and comparator were then simulated and the simulation results were compared with the adder and comparator designed with other basic logic styles. The adder designed with proposed logic style has 60 – 70 % less PDP and 55 – 60 % higher UNG as compared to its basic counterpart. Whereas, the comparator designed with the proposed logic possesses 75 – 80 % lower PDP and 45 – 50 % higher UNG as compared to its basic counterpart.

- **Testchip-**

  We have implemented a testchip in UMC 180 nm technology containing an 8-bit ALU using the proposed logic style to demonstrate the feasibility of the proposed logic. Simulations indicate that the proposed ALU has lower power consumption and delay than the equivalent domino logic ALU. We have also simulated and compared the pre-layout and post-layout simulations and demonstrated a small amount of deviation in results in the post-layout performances. This testchip is currently submitted for fabrication.

7.2 FUTURE WORK

There is several research directions that can be pursued based on this work:

Robustness

Issues such as soft error, transient noise, and variability each present different failure modes and these effects can be analyzed.

Noise Reduction

Further noise reduction techniques can be explored. The noise reduction technique proposed in this work can form the basis.

Testing of test chip

The test chip after fabrication can be tested and it can be simulated with real hardware, where functionality of the test chip can be tested after fabrication.

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