MEMORY CHIP DESIGN USING CADENCE

A thesis submitted in the partial fulfilment of the requirements for the degree of

Bachelor of Technology

In

Electronics & Instrumentation Engineering

Submitted by:
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Roll No.:110EI0085
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING,
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

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CERTIFICATE

This is to certify that the thesis entitled "MEMORY CHIP DESIGN USING CADENCE" submitted by **DEBASISH SAHOO**, Final year student of Electronics &Instrumentation Engineering, Roll No: 110EI0085 in partial fulfilment of the requirements for the award of B.Tech degree at NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA is a project work carried out by them under my supervision. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any degree or diploma.

DATE:

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ACKNOWLEDGEMENT

First and foremost, we would like to express our gratitude and indebtedness to Prof. D.P. Acharya, Associate Professor, Department of Electronics & Communication Engineering, NIT Rourkela for his kindness in allowing us to work on the particular topic and for his inspiring guidance, constructive criticism and valuable suggestions throughout this project work. We are also sincerely thankful to Mr Arabinda Mishra (M. TECH) who always encouraged and helped us in the successful completion of our thesis work. Also I want to thank our lab assistants and departmental office staffs for their helping hands when ever required.

An assemblage of this nature could never have been attempted without reference to and inspiration from the works of others whose details are mentioned in the reference section. We acknowledge our indebtedness to all of them.

Last but not the least our sincere thanks to all our friends, who have patiently extended all sorts of help for accomplishing this undertaking.

ABSTRACT

In this paper an effort is made to design 16 bit SRAM memory array on 180nm technology. For high-speed memory applications such as cache, a SRAM is often used. Access time, speed, and power consumption are the three key parameters for an SRAM memory design (SRAM). The integrated SRAM is operated with analog input voltage of 0 to 1.8v. The 16 bit SRAM memory has been designed, implemented & analysed in standard UMC180nm technology library using Cadence tool. We also analyse the read and write operation of the designed memory cell.

Contents

INTRODUCTION

Now days with the growth the rapid growth of communication and signal processing the electronics became aware to the consumer. So the designer need substantial cost and form factor reduction system. So the designer brings SOC (system on chip) Designing system. In which the 70% of area of SOC is being covered by the SRAM cell. Which needs low power for the operation. And the speed of operation is also high which is so demand in the now days market. So we need

for the design of the SRAM kind memory cell in the market. Although there is some need of powerful design of the powerful operation for this. But it ensures a good kind knowledge to the market as well as to the designer.

Chapter1

What is SRAM ?

Importance of SRAM

Transistor sizing

Schematic of SRAM

Disadvantage

SRAM CELL

It is known as static random access memory. Its operation is very much important in the memory design work by the designer. The operation can be bit oriented manner or in word oriented manner. In bit oriented manner we access the data in single bit manner but in multiple bits in terms of powers of 2. So word oriented is little bit complex rather than bit oriented. The SRAM also now days more and more important electronics component in the day to day market. Now days peoples want minimize cost, how they can easily get and it should work in proper fascinated manner, so that a costumer can easily handle the data and properly utilize it for future aspects also. the main important thing in the design of SRAM cell is that it needs low power and low man force also for the designing. Its speed while working is so fast which is the important thing in now days market. Its products are also really good for the designer for working. With all these aspects the SRAM type memory is required. The main thing is that now days the designer needs system on chip design, by which the speed and accuracy can be increased,

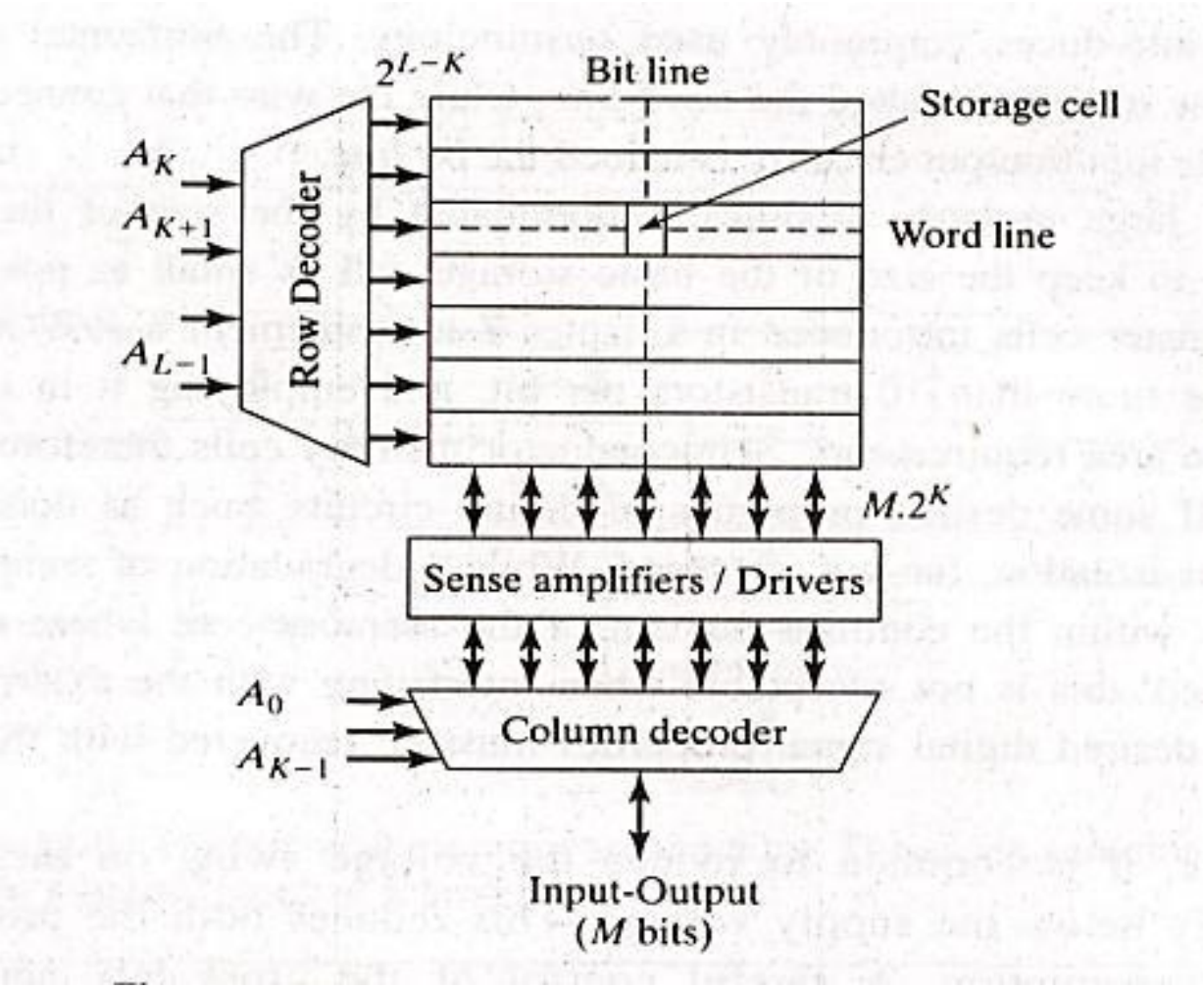
The major areas over the system on chip is being covered by the SRAM cell, which is major application of the SRAM cell.

Importance of SRAM

SRAM cell design are importance for so many reasons.

1. First of all, the design of a SRAM cell is key to guarantee stable and robust SRAM operation.
2. Second thing is that, owing to ceaseless drive to improve the on-chip stockpiling limit, the SRAM designers are propelled to expand the pressing thickness.
3. Therefore, a SRAM cell must be as little as could reasonably be expected while meeting the solidness, speed, power and yield stipulations.
4. An SRAM cell is the key SRAM segment putting away twofold data.
5. It has low power memory needed for the operation of the memory cell.
6. It does not require memory revive for the operation.
7. Speed of operation is quick. With the goal that we can work it in any way according to the prerequisite in the business.
8. Power loss is so less in the SRAM cell Design . So the different parts of the cell does not get Influenced any sort of impacts while performing the operation.

GENERAL SRAM ARRAY STRUCTURE



TRANSISTOR SIZING

Resistance of a transistor depends upon

Region of operation

Width to length(w/l) ratio of the transistor

nFET vs pFET-

>

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})} \qquad \beta_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)} \qquad \beta_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$$

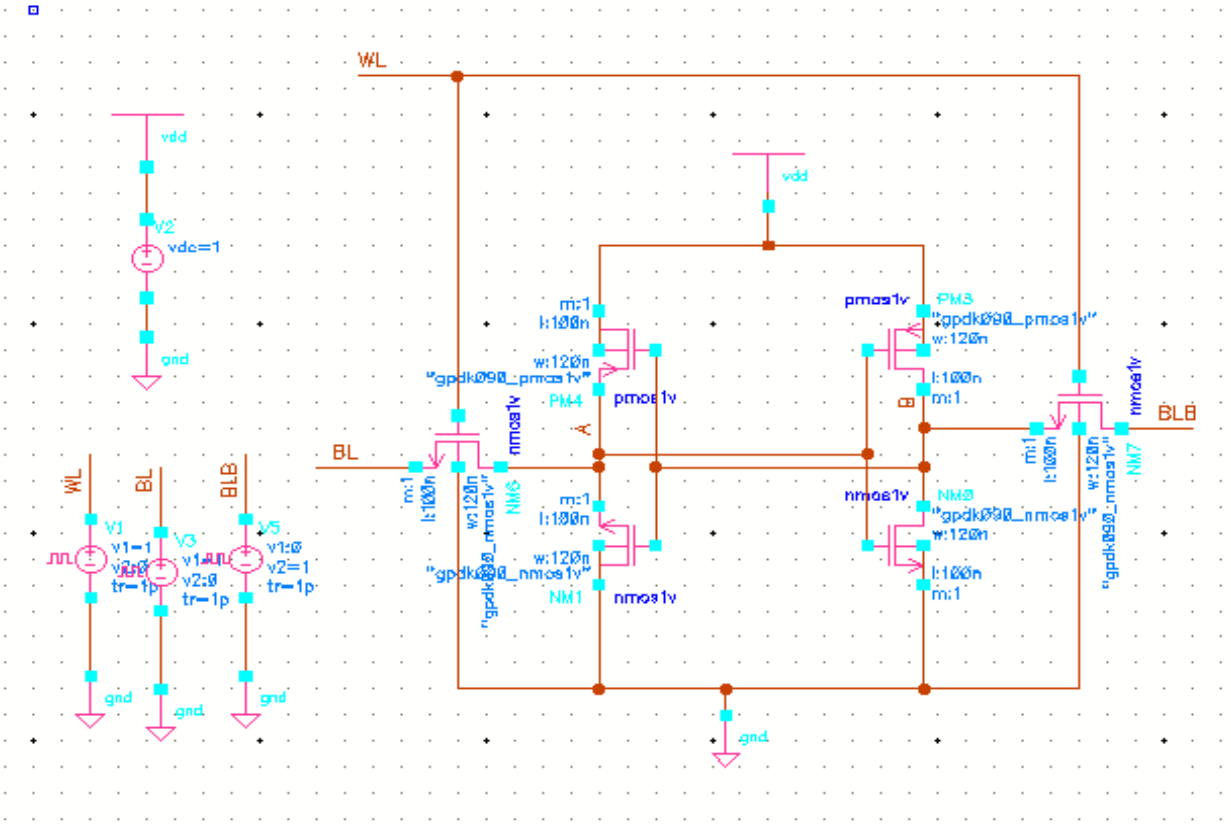
From the above expression we get that

Resistance of a transistor inversely proportional to the (w/l) ratio.

$$(w/l)_{pu} > (w/l)_p > (w/l)_{pd}$$

$$R_{pu} < R_p < R_{pd} \quad (W/L)_n = 3(W/L)_p$$

SCHEMATIC OF SRAM CELL IN CADENCE



Disadvantages of SRAM

1. SRAM need certain more transistor to store certain memory. As we know that if we increase the no of transistors, for calculating each and every transistors width to length ratio is an important factor in the designing.
2. Designing cost is more in SRAM. As the various components are being attached here so there more and more cost is being needed in the designing a memory cell. Sometimes also all the components are not easily available in the market. Due to which designer faces a lots of problem while design a memory cell.
3. It needs more space for the design. Due to which it needs large surface over the Designing criteria, along with some specifications for the designing.

Chapter2

DECODER BASICS

TRUTH TABLE

DECODER DESIGN

OUTPUT OF A DECODER

ADVANTAGES

DISADVANTAGES

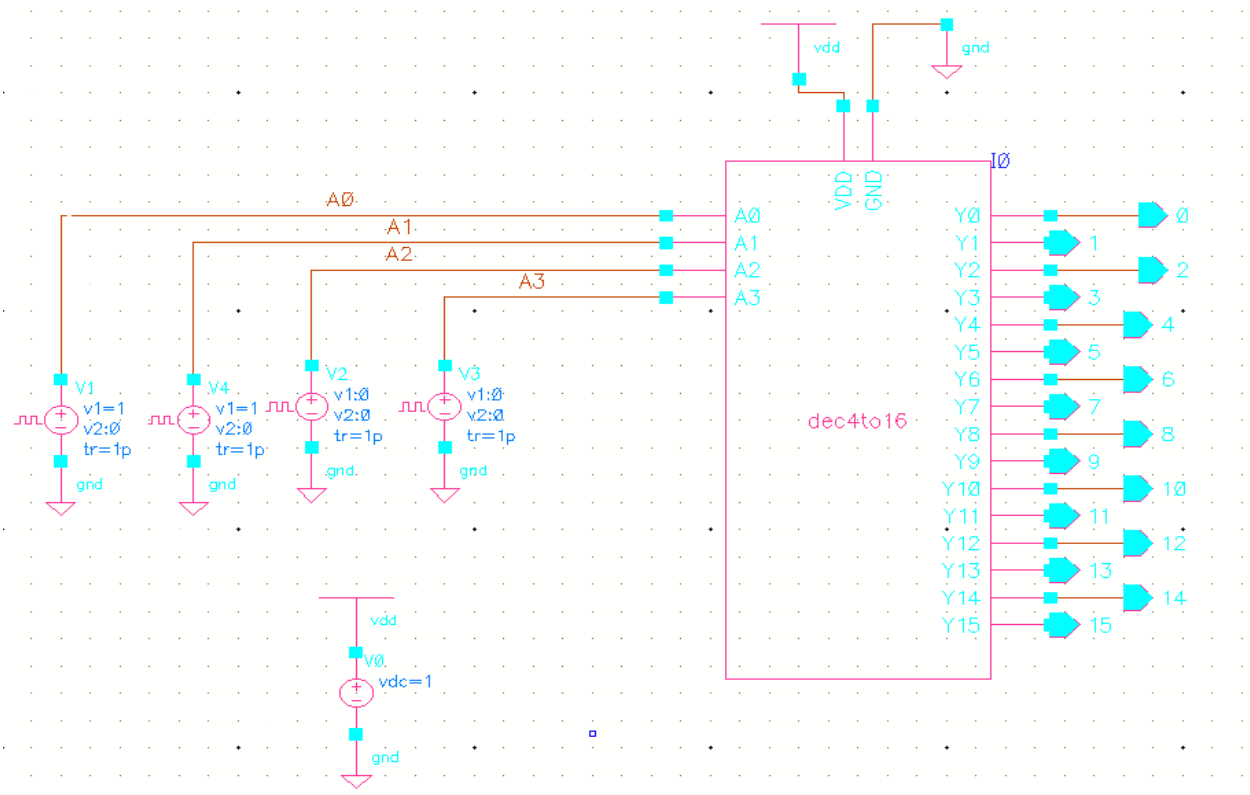
DECODER

It is just a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique outputs. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. With this the binary input conversion gets easier with the operation and we need for the desired output from this kind of combinational output by which we can use it for no of operations like data, word line selection for the memory cell. And also for the other digital information storage working.

A 2-to-4 decoder operates according to the following truth table.

S1	S0	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

SCHEMATIC OF DECODER CIRCUIT IN CADENCE

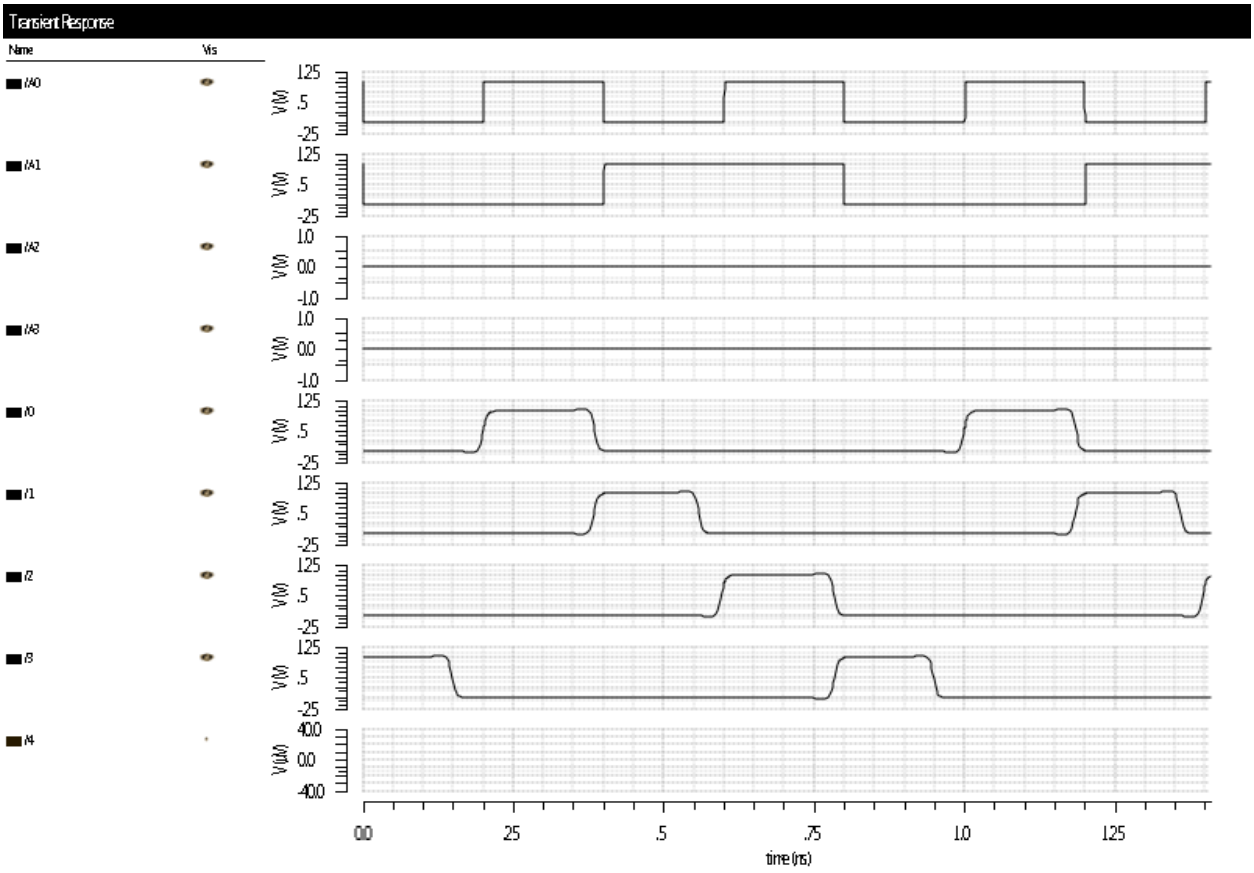


This is a 4 to 16 decoder which is designed in

cadence software. In which 4 inputs A0, A1, A2, A3

And the outputs are I0,I1, I2, I3, I4, I5, I6, I6, I7, I8, I9, I10, I11, I12, I13, I14, I15.

OUTPUT FROM AN DECODER



The output follows the input but after some interval of time. Because of the delay in the design i.e 270 ps. So we are getting the desired output after some intervals. We need to minimize these interval inorder to get some specification.

Data and word line selection

Data line selection	Word line selection
Datain 0	1
Datain 1	2
Datain 2	3
Datain 3	4
Datain 4	5
Datain 5	6
Datain 6	7
Datain 7	8
Datain 8	9
Datain 9	10
Datain 10	11
Datain 11	12
Datain 12	13
Datain 13	14
Datain 14	15
Datain 15	16

ADVANTAGES

1. It is more conventional way 2 convert n input to 2^n output. So that we can easily handle the inputs and output while carrying out the binary transformation.
2. Low power is needed for the operation. So that we can go for the easier things get accepted in a proper way.
3. Time response is so fast. As it is binary transformation time taking for the process is not so high.
4. Logical response is not get interfere by other responses. It means output does not altered by other factors.
5. Output follows properly to the input. The relation between output and input is like linear.

DISADVANTAGES

1. Designing of the circuit is little bit complicated. because of various NAND gates and NOT gates the circuit makes some complecated to the designer.
2. Error is in the circuit due to the delay in the circuit. The specified delay creates some problem to the designer. Here it is 270 ps.
3. Calculation of delay, power, volatge needs specified devices.

CHAPTER 3

PRECHARGE

BASICS

DESIGNED CIRCUIT

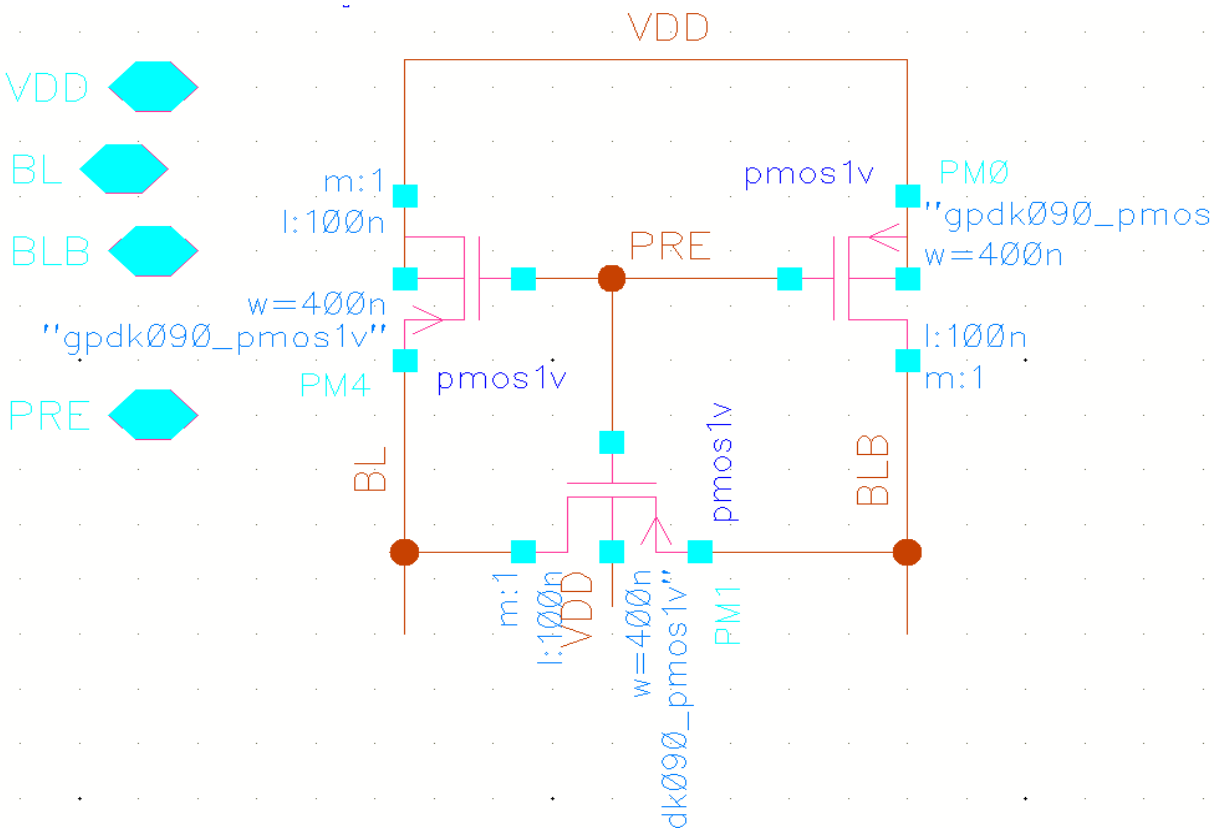
ADVANTAGES

DISADVANTAGES

PRECHARGE

The precharge circuit is one of the vital component that is constantly utilized within SRAM cell. The job of the precharge is to charge the bit and bitline bar to Vdd=1.8v. The precharge circuit empowers the bit lines to be charged high at all times aside from throughout read and write operation. The width needed for PMOS is least i.e 240 nm and length is fixed to 180 nm. For every section single precharge circuit is utilized. When a high-voltage framework is designed properly to handle the stream of greatest evaluated power through its circulation framework, the parts inside the framework can even now experience impressive stress upon the framework "power up". In a few requisitions, the event to actuate the framework is an uncommon event, for example, in business utility force dispersion which is ordinarily on practically constantly. Yet in different frameworks, for example, in vehicle requisitions, enactment will happen with each individual utilization of the framework. At the point when a long life of the parts and a high dependability of the high voltage framework is required, then a force-up strategy which decreases and limits the force-up stress is needed.

SCHEMATIC OF PRECHARGE CIRCUIT IN CADENCE



ADVANTAGES

1. It gives the potential to the bit line and bit line bar.it provides the voltage which is being so important for the bit line and bit line bar in the memory cell.
2. It provides voltage to the bit line and bit line bar all time except at the time of read and write operation.
3. It gives support up to maximum supply voltage vdd.
4. Due to which signal swing occurs. The output able vary in between some interval.
5. Power dissipated is also less. Loss of power due to the operation is less.

DISADVANTAGES

1. It is non linear in nature. The output does not follows to the inputs
2. In industrial setting cost down time will come.
3. The main disadvantage is that for each part we need extra power supply.
4. At the time of read and write operation we did not get any kind of supply voltage.

CHAPTER 4

DRIVER CIRCUIT

WHAT IS DRIVER CIRCUIT ?

DESIGNED DRIVER CIRCUIT

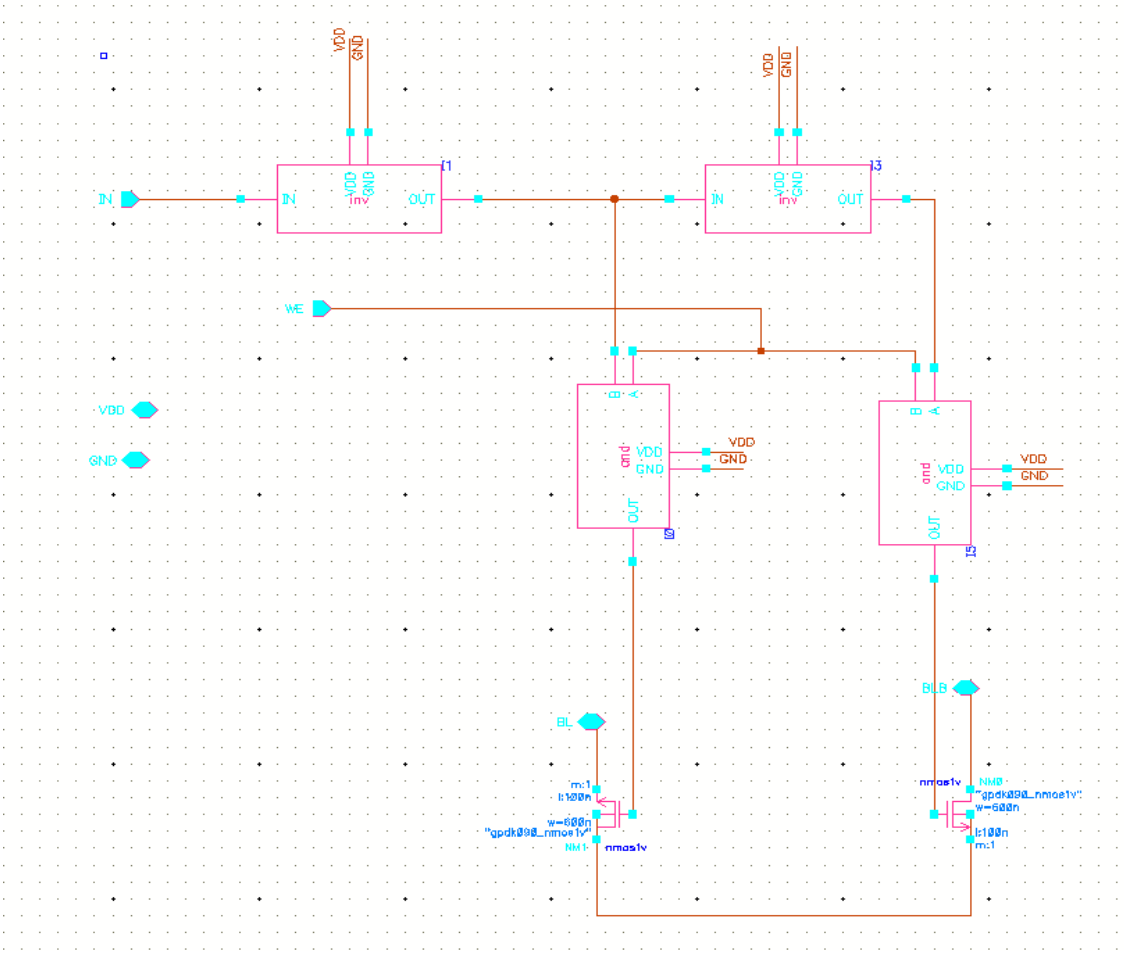
ADVANTAGES

DISADVANTAGES

DRIVER CIRCUIT

The driver circuit is one of the basic component in the memory design circuit. The job of the driver is to bring the bit line and bit line bar to ground potential for the further job. Before this the bit line and bit line are being charged maximum supply voltage Vdd. With precharge circuit it was get charged and after that it gets discharged. It is also known as write driver. The driver gets enabled by the word enable which is in the connected in the upper part. It is two nmos transistors are being connected back to back with fascinated manner. With also two inverters in the upper part. first of all two logics are given to the two points of the junction of the nmos. i.e 0 and 1. The bit line which is nearer to the 0 logic it gets discharged first after that its logic gets inverted. Like this way the bit line and bit line bar gets discharged to the ground. With this kind of operation the bit line and bit line bar gets discharged. Its main job is to provide low impedance path to the ground. So that the voltage difference between bit line and ground, bit line bar and ground is zero. So that another data can be easily retrieved by the memory cell when more no of data is to be accessed.

SCHEMATIC OF DRIVER CIRCUIT IN CADENCE



ADVANTAGES

1. With the driver circuit we able to bring the bit line and bit line bar to the ground potential.by adding a low voltage and a high voltage at two points of the cross coupled inverters.
2. From this we can get initaialiation conditions of the circuit.
3. We can get full description of the circuit.
4. Full modification is not needed by the designer.
5. Its description is easy.

DISADVANTAGES

1. The FETs (Field Effect Transistors) are being used have much higher on resistances, which difficult to get and higher cost also.

2. Switching speed of this circuit is also less.

3. Implementation of the circuit is also little bit complicated.

CHAPTER 5

SENSE AMPLIFIER

BASICS

DESIGNED CIRCUIT

ADVANTAGES

DISADVANTAGES

SENSE AMPLIFIER

Sense amplifier are the vital component in the memory design. The job of sense amplifier is to sense the bit line and bit line bar for proper monitoring action.It improves the read and write speed of the memory cell. Its another job is to reduce the power needed for the operation. The sense amplifiers primary job is to amplification of the voltage difference is being produced on the bit line and bit line bar at the time of operation. As it has the important job in the memory so it has different circuits for the operation.

As we know that in SRAM operation we don't need refresh of the memory for the further process, so the sense amplifiers non destructive at the time of operation. As the column multiplexers are connected in the memory cell at that time multiplexer should choose one sense amplifier for the single input. So that we can get proper use of the sense amplifier in the designing circuit.

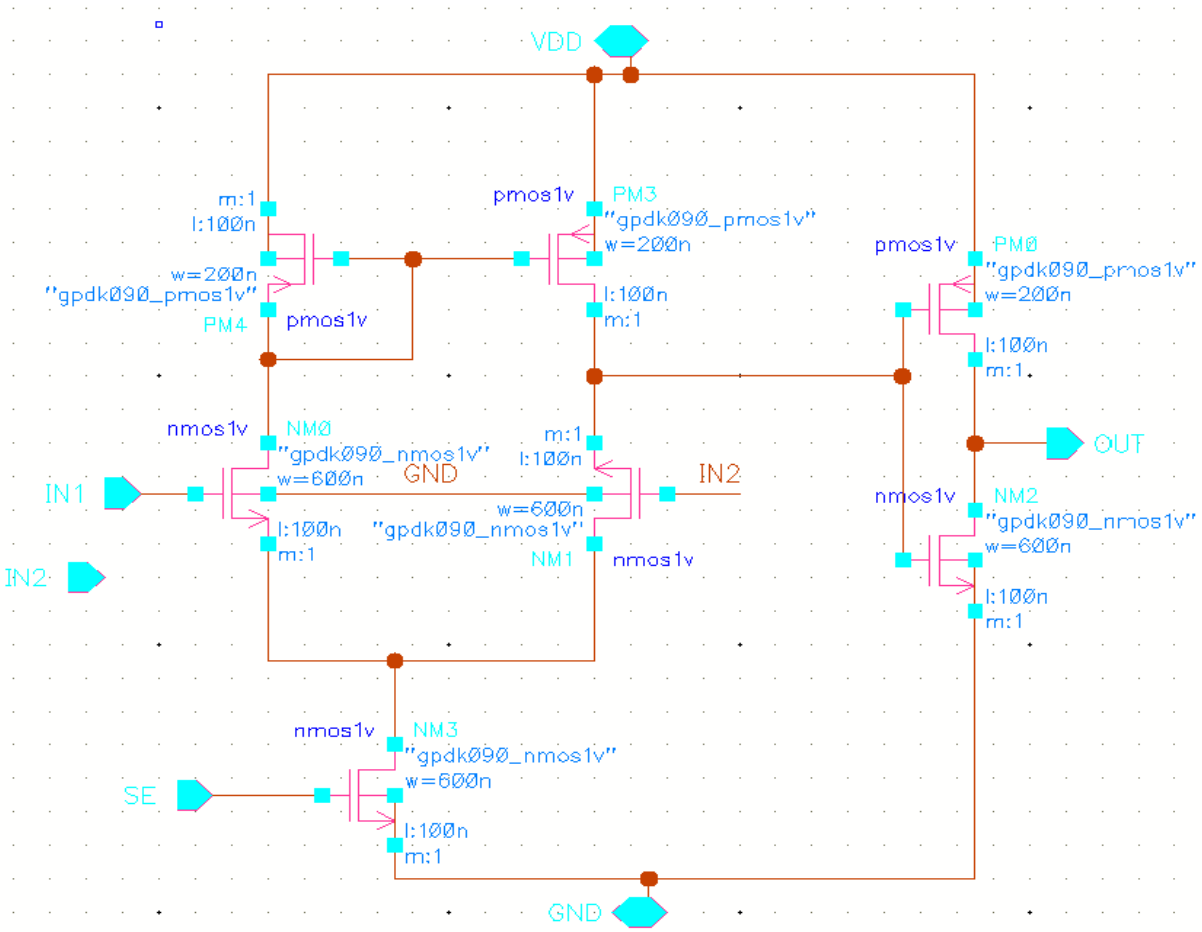
These are the various parameters of an sensing amplifier-

• Gain A =V_{out}/V_{in}.

• Sensitivity S =v_{in} min – least noticeable signal.

• Rise time t_{rise}, fall time t_{fall} – 10% to 90%

SCHEMATIC OF SENSE AMPLIFIER IN CADENCE


VDD
m:1
l:100n
w=200n
"gpdk090_pmos1v"
PM4
pmos1v
pmos1v
PM3
"gpdk090_pmos1v"
w=200n
l:100n
m:1
pmos1v
PM0
"gpdk090_pmos1v"
w=200n
l:100n
m:1
nmos1v
NM0
"gpdk090_nmos1v"
w=600n
GND
IN1
l:100n
m:1
IN2
m:1
l:100n
IN2
w=600n
"gpdk090_nmos1v"
NM1
nmos1v
OUT
nmos1v
NM2
"gpdk090_nmos1v"
w=600n
l:100n
m:1
nmos1v
NM3
"gpdk090_nmos1v"
w=600n
SE
l:100n
m:1
GND

ADVANTAGES

1. Although it can feet in the column pitch, s there is no need of column selection device in the circuit. It reduces propagation delay.
2. There exist a virtual short circuit across the bit line and bit line bar by which it is independent of current distribution in the circuit.
3. The delay in the circuit does not get affected by the bit line and bit line bar capacitance.
4. The bitline current i_c gets discharged through this capacitance.

DISADVANTAGES

1. It has negligible signal swing.
2. Bit line voltages decreases cross talk in between bitline and ground potential.
3. Power dissipation is also more.

CHAPTER6

DESIGNED MEMORY CELL

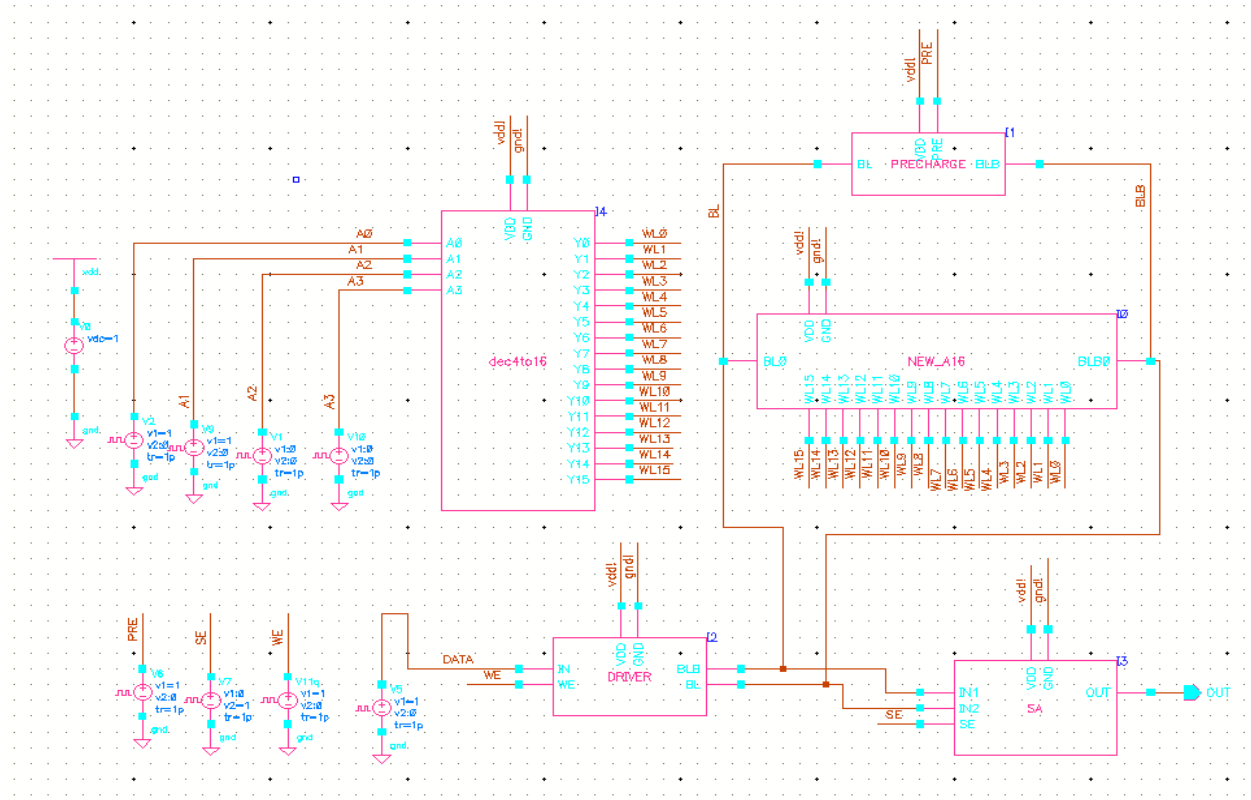
READ OPERATION

WRITE OPERATION

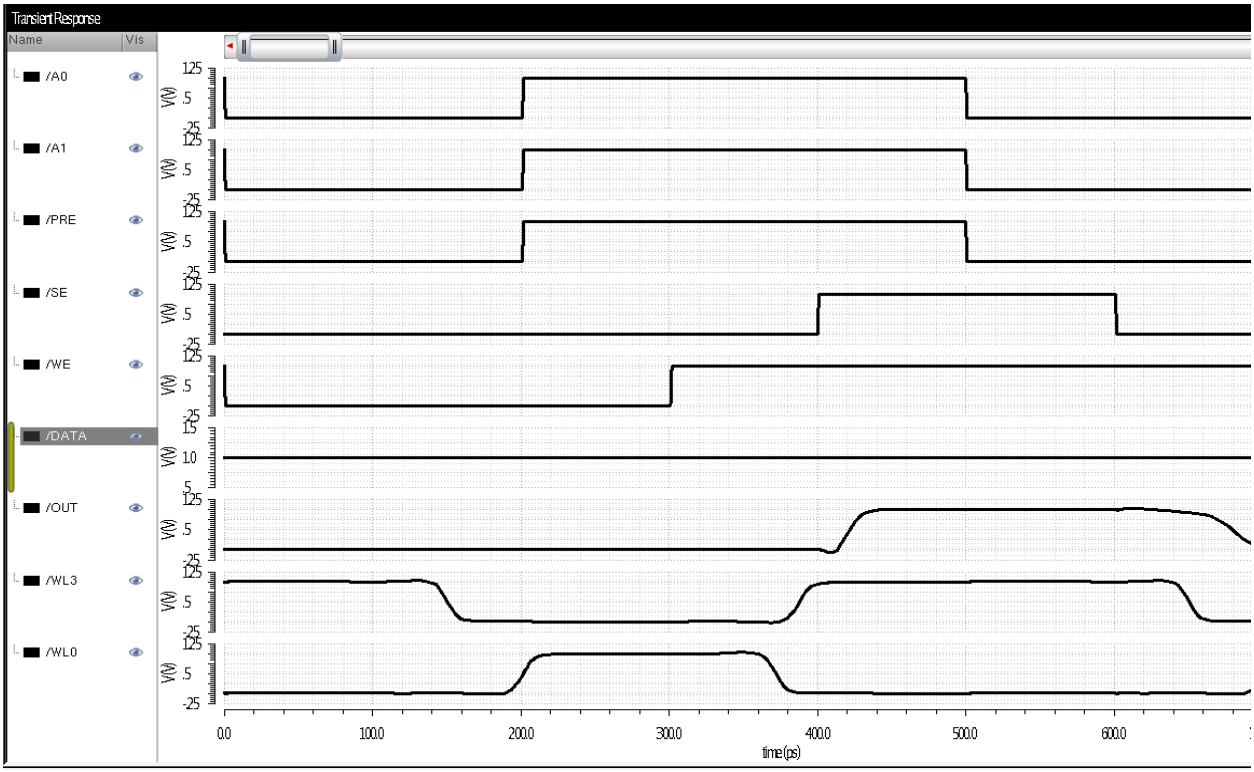
DISCUSSION

CONCLUSION

MEMORY CELL

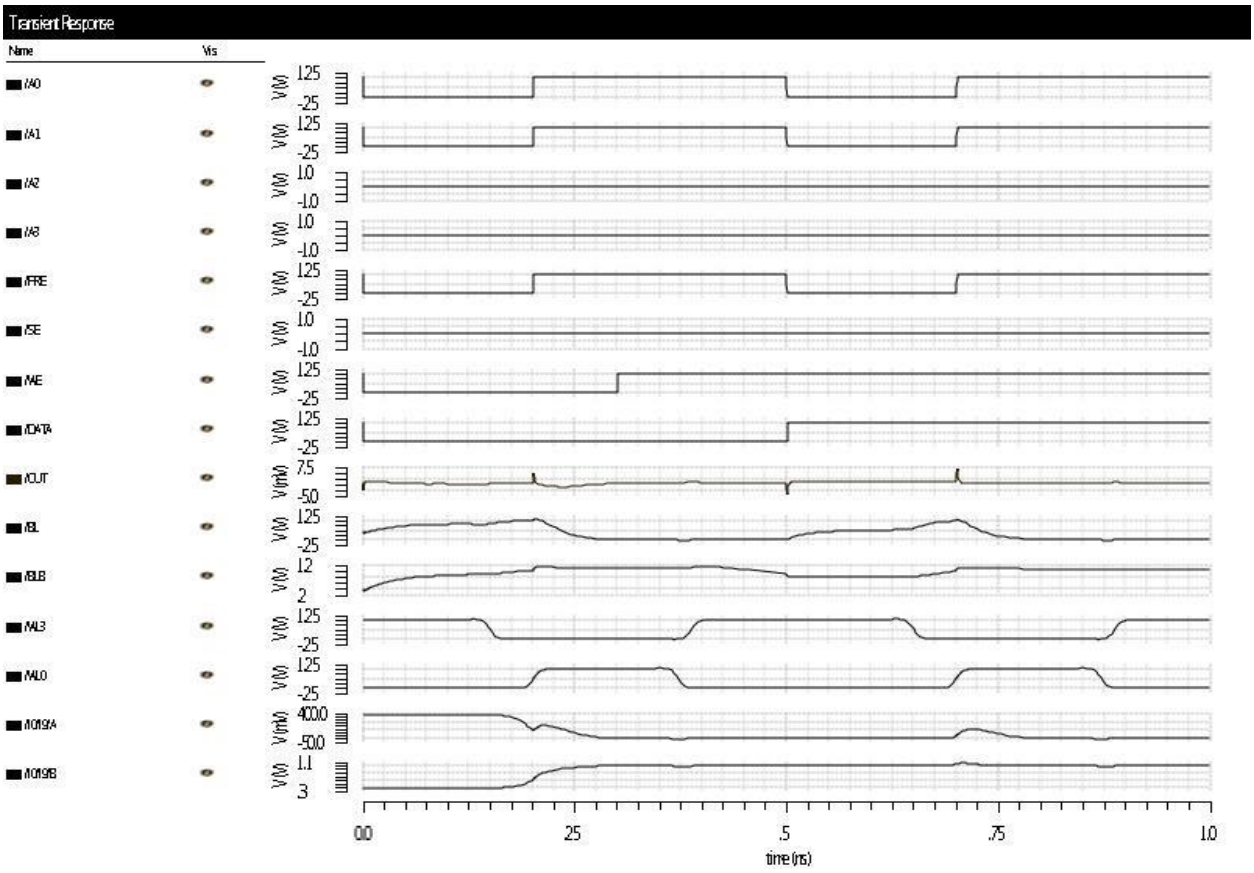


READ OPERATION OF THE MEMORY CELL



In read operation when both the inputs gets low at that time data is being kept at the constant value. When wl3 goes from high to low and wl0 goes from low to high with sense enable gets on we get confirmed for the read operation of the memory cell.

WRITE OPERATION OF THE MEMORY CELL



In write operation when the write enable gets on after that the data goes high from low to high after that remains constant, which shows that the data is being read by the memory cell.

EXPERIMENTAL RESULTS

In this we will discuss about the simulation result that is being done by the above memory cell. The work is being carried out with cadence virtuoso design software with read and write operation in the above layout. We have designed an 16 bit memory cell with this software. The stop time of the cell is 10ns. The duration of write enable and sense enable set to 5ns. The precharge level is Vdd/2. The delay in the decoder circuit is 270 ps. For which we are getting the output that follows to the inputs but after some interval of time. The read and write operation is being shown for the success of the designed memory cell.

DISCUSSION

This project discusses about the concept of memory chip design. There has been a brief summary about the different parts of memory chip is functions and applications. I have designed it in the cadence virtuoso software. The software was really used for the designing of the various things in VLSI. The designing of the cell gives brief idea of each and every individual parts of the designing system. We can also design many things from this software. So it should be logical information in the design and the need for the various circuits should be there. For the designer point of view it is a good technique.

CONCLUSION

The designed memory cell is capable of storing memory of 16 bit.

The complete array which includes pheripheral components such as memory bit cell, write driver circuit, pre-charge circuit, Sense amplifier are designed and integrated with the software.

The proposed work operated with 0 to 1.8 v, 1.8v supply voltage. And conjumes 49.94 mw power.

The SRAM is designed and implemented in standard UMC(united microelectronics limited) 180nm technology of version 5.14 using Cadence virtuoso tool for schematic.

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