NETWORK ON CHIP MODELLING USING CDMA CONCEPT

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NETWORK ON CHIP MODELLING USING CDMA CONCEPT

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May 2014

Dedicated to my beloved parents, my brothers and sister

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I, **Swetaleena Sahoo**, declare that this thesis titled, 'Network On Chip modelling based on CDMA concept' and the work presented in it are my own. I confirm that:

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ABSTRACT

The network on chip (NOC) is a widely discussed concept for handling the large on chip communication requirements of complex system on chip (SOC) design. The traditional bus based architecture does not communicate properly in very large SOCs. As a result the on chip communication uses the packet switching paradigm for routing information between the intellectual property (IP) blocks. The concept of code division multiple access (CDMA) is applied for on chip packet switch communication network. The technique of applying CDMA principle in NOC design is the point to be discussed in this project. A packet switched network on chip that applies the CDMA principle is realizable in a very common logic that is Register Transfer Logic (RTL) by using the VHDL coding technique. The globally asynchronous and locally synchronous (GALS) scheme is used for the realization of CDMA NOC by using both synchronous and asynchronous designing technology. Packet switched NOC is divided into two designing schemes which are named as CDMA NOC and POINT TO POINT NOC. The packet switch NOC which uses point to point design scheme, which is shown by the example of ring topology NOC, has a varying data transfer latency when the packets are transferred to different destination or to the same destination by different routes in the network. For the elimination of variation of data transfer logic CDMA NOC is used. The structure of the CDMA NOC is proposed and the process is coded and implemented by using ALTIUM software in this project. The model of CDMA NOC is described by the ALTIUM software. The comparative study of the characteristics of CDMA NOC and point to point NOC mainly ring topology are examined.

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Date:

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Abbreviations

SOC **S**ystem **O**n **C**hip

NOC **N**etwork **O**n **C**hip

CDMA **C**ode **D**ivision **M**ultiple **A**ccess

PTP **P**oint **T**o **P**oint

RTL **R**egister **T**ransfer **L**ogic

GALS **G**lobally **A**synchronous **l**ocally **S**ynchronous

FPGA **F**ield **P**rogrammable **G**ate **A**rray

VHDL **VHSIC H**ardware **D**escription **L**anguage

HDL **H**ardware **D**escription **L**anguage

PCB **P**rinted **C**ircuit **B**oard

DXP **D**esign **E**xplore

LED **L**ight **E**mitting **D**iode

TFT **T**hin **F**ilm **T**ransistor

CHAPTER 1

1.1 INTRODUCTION

1.2 OBJECTIVE

1.3 RESEARCH MOTIVATION

1.4 LITERATURE SURVERY

1.5 THESIS ORGANIZATION

CHAPTER- 1

1.1 INTRODUCTION

Code division multiple access (CDMA) is a technology which is used for radio communication and also used as tool for NOC design. Multiple access technique is a broad area for communication purpose, CDMA is an example of multiple access technology, through which several number of transmitter can send information in a single communication channel. In case of CDMA a particular bandwidth can shared between several numbers of users. To permit this technique to achieve without undue interference between users, spread spectrum technology and a special coding scheme are used by ***CDMA***.

In modern era every people want to use things which is smaller in size, can have more functionality and less cost. This can only possible if we can integrate more and more functionality into a single chip which helps achieving our objective and demand. To achieve this scientists have developed a new concept that is ***Nanotechnology***. Nano implies 10^(-9) which is very small. After Nano scale development, the scientists of the semiconductor had faced many challenges. The greater challenge was how to combine the Intellectual properties (IP) from various sources quickly and efficiently. These limitations have been overcome by introducing ***System on chip*** technology which is a grooming topic in modern technology. System on chip mostly called as SOC is a best solution of combining a number on functionality into a single chip. System on chip is called as bus architecture based technology. System on chip is an integrated circuit that integrates all the component of a system on electronics system into a single chip. The single chip can contain digital, analog and mixed signal and it can operate in any range of frequency. Basically it is very difficult to integrate the total system in a single chip but it can only possible due to the fast development in semiconductor devices. Instead of building an electronic product by assembling various component on a circuit board, the system on chip (SOC) technology helps all these parts to be fabricated in a single chip which can work as the required system. A system on chip architecture consists of processor, system bus, timer, interrupt controller and power management circuits. Day by day the components of the system on chip increases and to fulfil this the research scientists are trying to integrate more and more number of components into a single chip using the Intellectual

properties (IP). An example which helps to show the properties of system on chip is to integrate the audio system into a single chip. The system on chip has many advantages like low power consumption, less space consumption, faster circuit operation and low cost per gate etc. The implementation of the system on chip is reliable. Besides these advantages there were some causes for which now a day's system on chip architecture has been discarded. The drawbacks which faced by the system on chip were the complexity raised due to combining large number of components into a single chip and interconnection between them. Due to the system on chip bus architecture many problems raised for which a noiseless communication cannot be possible. To reduce this complexity a concept was introduced which is named as network on chip (NOC).

Network on chip technology is a "Front end solution to a back end problem". NOC is a technology of integrating a complex network system into a single chip. Company like 'Arteries' provides network on chip interconnect semiconductor intellectual property to system on chip (SOC) which can easily reduce cycle time, increase margin and can improve functionality on system on chip smoothly. As by increasing the market demand the researchers have added more number of traditional hierarchal buses or crossbar to SOC which becomes very complex for which the architecture and integration is affected. Due to large number of wires interconnection heat and power consumption is increased. These problems have one solution which is Network On Chip. Network on chip helps to reduce SOC manufacturing cost, increase performance of SOC, reduce SOC time consumption and also reduce the SOC design risk.

Efficient Communication is a medium through which data can transfer from transmitter to receiver with zero noise and any interruption in communication. Off chip communication uses physical links to connect transmitter and receiver established at different position .NOC is an on chip communication which integrates transmitter and receiver on a single chip, is better than the off chip communication.

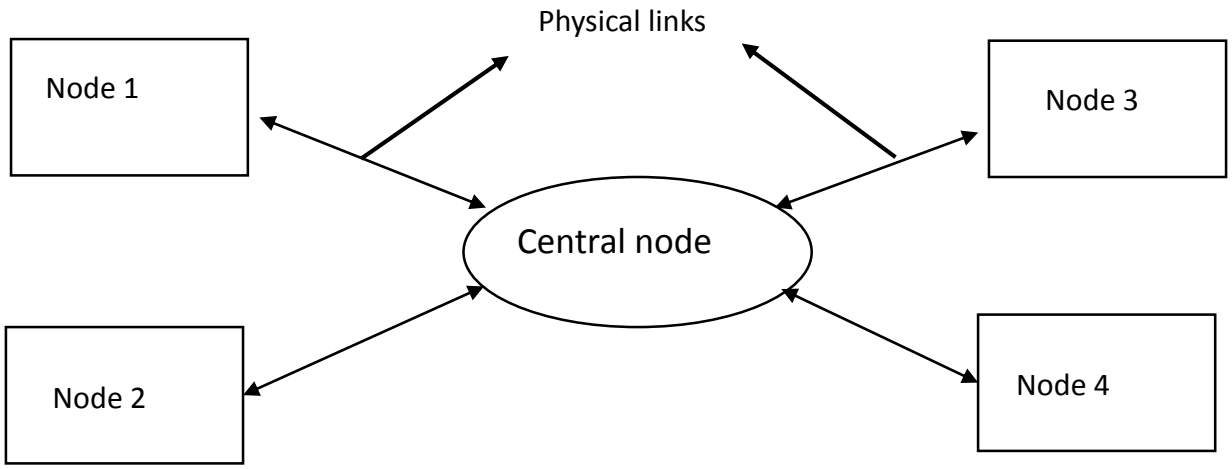

Fig 1.1.1:- **structure of circuit switch network on chip**

There many of type NOC can designed. The structure of NOC can classified into two categories-

i. Circuit Switched Network on chip
ii. Packet Switched Network on chip.

This type of categorization is based on the data switching nodes. The structure of circuit switch network is described in the above figure.

SOCBUS architecture [4], a mesh on chip network, is a good example of circuit switch network structure, the packet connected circuit scheme is used to allocate time or space slices on the switch links among the terminals in the network. In case of circuit switching network, a connection is established between two network nodes before beginning of data transfer between the two nodes. Bandwidth for the data communication remains same up to the termination of the transmitting data between the two nodes. While the nodes remain connected between the senders to the receiver, all the data follow the path which is to selected by the switches previously. The normal telephone line connection which works for voice communication is based on this concept of circuit switching. ISDN which means Integrated Services Digital Network is a best example of circuit switch

network. The works inside circuit switch network technique is divided into three steps which are circuit establishment, data transfer and circuit disconnection. Circuit establishment is a phase in which circuit must be established between one network node to another network node. This circuit can send information through signal before the receiving and sending end establishes their circuit. The next phase is data transfer phase in which information can be transmitted for one node to another node through the network. The data may be analog or digital signal that depends upon nature of the network protocol. The third and last phase is circuit disconnect phase in which after data transfer the circuit which is established between the nodes are disconnected.

AETHEREAL NOC [11] and PROTEO NOC [12] are two best examples of packet switch network. The combined guaranteed services and best effort router are applied in AETHEREAL NOC to transfer data packets in the network. The components in the PROTEO NOC system are connected through nodes and hubs. The network topology and data links in the PROTEO NOC can customized and optimized for a specific application. The packet switch network structure is described by the figure as follows.

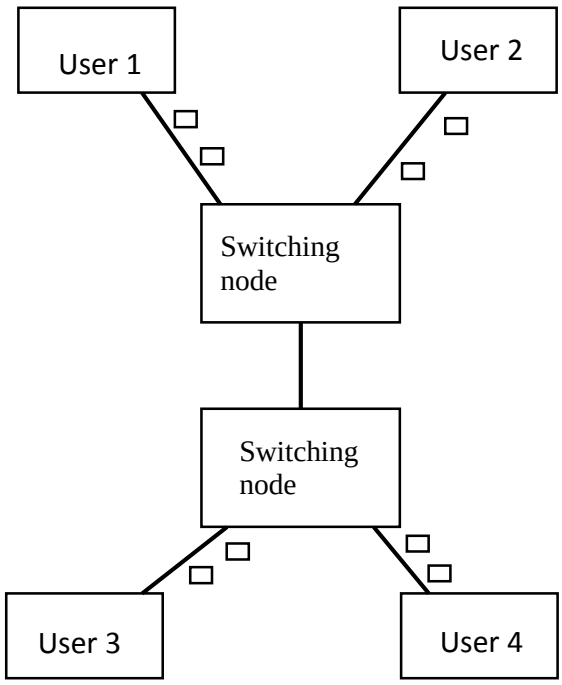

Fig 1.1.2:- **Structure of packet switch network on chip**

In previous paragraphs we have discussed circuit switch and packet switch network and their communication techniques and how data flows from sender to receiver by using these two techniques. But in case of circuit switch network there are many difficulties in the data flow which can be overcome easily by packet switch network structure or communication process. In telecommunication circuit switching network is one process in which a circuit or channel means a physical link is established between the sender node and the receiver node before the communication process starts. But the packet switch networking is a digital network communication method that combines all the transmitted data irrespective of the content type or structure into suitable sized blocks which called as packets. The network through which packet are transmitted is a shared network which helps to send each packet independently from other packets and allocated suitable path and transmission resources to each packet as they required. The ultimate goals of packet switched network for data communication are to optimize utilization of available link capacity, to minimize the response time for communication process and to increase the robustness of the communication technique. Packet switching network technique is safe as compared to circuit switch network. If we are comparing on the basis of efficiency packet switch network is better than circuit switch network communication. These are the advantages of packet switch network over circuit switch network. But in case of on chip communication where hundreds of intellectual properties(IP) are used , if the circuit switched network is used for data communication their then it will face problems of scalability and parallelism which problem can be easily overcome by using packet switched network technique in on chip communication. These shortcomings of circuit switched network can overcome by diving the full length data streams into small packets and sending the data packets to their destination node by node.

The packet switched network scheme is used first in multihop point to point (PTP) networking scheme. In this scheme of data transfer the packet transfer latency varies when data are transferred to same destination or different destination via different routes in the network. These variation in data transfer is the worst case scenario of the data transfer case. To reduce these data transfer variation and complexity occurred in the multihop point to point network on chip code division multiple access technique which is based in network on chip comes into picture. The

code division multiple access is a common mechanism is case of communication process. This CDMA technique is used in on chip platform is called as CDMA NOC. As described above network on chip is a technique which integrates the total communication system in a single chip. CDMA is widely used in wireless communication system for its higher bandwidth and using spread spectrum technique for better performance. In CDMA technique a set of orthogonal codes are applied to encode the data which can be collected from different users before transmission of these data into different mediums in communication process. This is the way how code division multiple access technique is permitted number of multiple number of users for using a same communication medium to communicate by separating each user by their coding domain. So CDMA NOC is proposed to transfer data packets from same or different sources to their destination without any problem. CDMA NOC has better data transfer latency and has a better way to communicate in on chip platform.

The Code division multiple access communication technique is discussed in next chapter.

1.2 OBJECTIVE

The salient features of the thesis are:-

i. Development of CDMA NOC structure.
ii. Simulation of CDMA transmission and reception using ALTIUM software.
iii. NODE to NODE transmission and its propagation delay observation.
iv. Theoretical studies of latency between POINT TO POINT NOC and CDMA NOC.

1.3 MOTIVATION

In the modern era the development of Nano chip is a growing topic for fulfilling the human choice to use Nano products. To produce a best product with low cost and small in size is very difficult. Integration of more and more functionality into a single chip is a better option for reduction of the above difficulties. The integration of the functionality of the total system in a

single chip is called SYSTEM ON CHIP (SOC). The system on chip also helps to reduce the time consumption of the total system. Basic building blocks of SOC are one memory block, one processor, one timing source and power supply block. SOC designing fulfils the demand of the human being. SOC basically used for design of embedded system. It performs both hardware and software operation of an embedded system. The use of SOC increased day by day.

Day by day the size of the chip are reduced and more functional blocks are added from which the complexity of the chip is increased. The quality of the system on chip is reduced. The challenges like

(a) reduce wire routing congestion

(b) ease timing closure

(c) higher operating frequencies

are seen in the system on chip design structures. To reduce the challenges faced by system on chip a new concept is developed which is called as network on chip. The technique also required to combine communication system with the embedded structure design. Network on chip (NOC) is platform in which the communication processes are designed by using field programmable gate array (FPGA) which is a digital concept. NOC concept is based on the features like it has regular geometry which gives a good and highly regulated chip. It has predictable electrical and physical properties. The structure of NOC depends on the concept of GALS scheme which is globally asynchronous and locally synchronous wiring technique. The NOC has a predefined communication infrastructure with known properties. NOC concepts mainly used to integrate a communication system into a single chip. This synopsis is based on a well known and highly useful communication technique which is code division multiple access (CDMA) concept to be designed by using network on chip (NOC) concept. NOC concept is also divided into two categories which are packet switched and circuit switched network. But packet switched network on chip has better performance than circuit switched network for utilization of available link capacity, to reduce the time complexity and to reduce the robustness of the network. Although packet network on chip is safer than circuit switched network on chip, but it has some problems like scalability and parallism which are reduced by CDMA NOC.

1.4 LITERATURE REVIEW

Network on chip(NOC) is a technology which is a front end solution of the backend problem of system on chip(SOC). Mostly from the starting of 20th century the NOC concept have been worked for different purposes. Noc concept is developed from system on chip. System on chip is designed for integrating the function of a system into a single chip. This concept has reduced the size of the system. Based on SOC many structures are proposed.

The concept of microelectronics is used for the development of concept of system on chip and network on chip. For bus based communication system SOC designing technique is used. The challenges like system complexity, time required for the working of the system are overcome by using system on chip concept. But by increasing the functionality integrated into a single chip the operation period of the chip is increased. The system complexity is increased. For the reduction of the problems occurred in the system on chip, network on chip concept is developed.

Code division multiple access technique is developed for communication purpose between and receiver but it is also used for system designing. In 2003 a parallel bus system [5] is proposed by using this CDMA concept. But in case of parallel bus system the routing congestion problem has raised which reduces the efficiency of the system. Packet switched NOC concept has developed for reduction of the problem faced by parallel bus system. In packet switched NOC concept datas are transferred from sending end to receiving end through packets. But each packet has two part one is message and another is header part. In the header part the detailed from the receiving node is mentioned. But due to error occurred in the transmission of the packets from one node to other node packet switched concept is not used for effective NOC structure designing.

CDMA concept is based on the concept that transferring the datas from node to node in bit by bit format. So modelling of network on chip structure by using the principle of

CDMA is better way for data transferring in chip level. By using CDMA NOC concept the data transfer latency has increased in node to node communication process.

1.5 THESIS ORGANIZATION

The details of the thesis is divided into 5 chapters. The outline of the chapter details are described below. Each chapter is the description of each single part of the project.

- CHAPTER 1:-

  This chapter contains the basic concept of system on chip, How network on chip(NOC) is developed from system on chip. The code of the division multiple access technique is also a part of chapter 1. Purpose of development of code division multiple access based on network on chip concept is discussed in this part of the thesis.

- CHAPTER 2:-

  This chapter gives the descriptive details of the concept of CDMA technique applying in network on chip. what is CDMA NOC and how it has been worked in FPGA platform is described in this chapter.

- CHAPTER 3 :-

  This chapter describes about the software (ALTIUM) which is used for the designing of CDMA concept using network on chip architecture. ALTIUM software is a digital platform which is to be used for the embedded system design.

- CHAPTER 4: -

  This chapter is a detailed of the work which is done in this project. The output of the work done in the project is described in this c and output are basically based on FPGA implementation.

- CHAPTER 5 :-

  This chapter is the conclusion part of the project. The future work which can be done by using this software or this concept is described in this chapter.

CHAPTER -2

2.1 CDMA CONCEPT

2.2 DIGITAL ENCODING DECODING SCHEME

2.3 STRUCTURE OF NOC BASED ON CDMA CONCEPT

2.4 REALIZATION OF THE STRUCTURE

CHAPTER 2

2.1 CDMA CONCEPT

Code division multiple access (CDMA) is a channel access method. It depends upon spread spectrum technology. The spread spectrum technology is based on adding a external sequence code i.e. spreading code with the message signal. For each message signal the transmitter is assigned with unique code. The code is generated by using PN sequence generator. The codes are of different types such as Maximal length sequence, Gold code, Kasami code, Barker code. The PN sequence code supports only binary coding means the code contains only zeros and ones. The zeros and ones are not in a particular manner means irrespective of the position of the zeros and the ones are generated but in the generated code the number of zeros is equal with the number of ones[6].

The communication system has two termination point basically that are the sender node and the receiver node. These nodes are combined through channels. In case of CDMA technique more than one user sends data at a time. The data are from different frequencies. The encoding and decoding schemes are used before datas are sending through channel by transmitter and after receiving the datas at receiver side. The encoding process is done in the sending end. The datas collected from different sources are encoded by using an orthogonal spreading code. After encoding process is completed the datas generated are combined with each other. This combination process is done for the transmission of data without inferences and overlapping of message. The orthogonal property of the code indicated auto correlation and cross correlation of the spreading code. The result of the auto correlation and cross correlation are in terms of 1's and 0's.

The autocorrelation property of the spreading code means summation of the product term of a spreading code with the same code. The result of these sum is to normalized for getting output of the auto correlation. Like auto correlation cross correlation is another one property for the spreading code. The cross correlation indicates

summation of the product of two different spreading codes. These auto correlation and cross correlation property of the spreading code are combined called as orthogonal property of a spreading code. This orthogonal property helps the spreading code to encode and decode the data the sending and the receiving end.

The principle CDMA concept is described in the figure 2.1. The indicates that n number of data are collected from different sources. These datas are combined with the spreading code generated by PN sequence generator. All the outputs are combined together through addition operation. This total operation is called encoding operation is to described in details in below paragraphs. The result is known as encoding result which is given as input for decoding operation. The encoded output is again undergone some process for decoding operation. The decoded result is again in discrete form. These two operations are combined called as the principle of code division multiple access technique. The decoding process is based on two principle one is accumulation and another one is comparison.

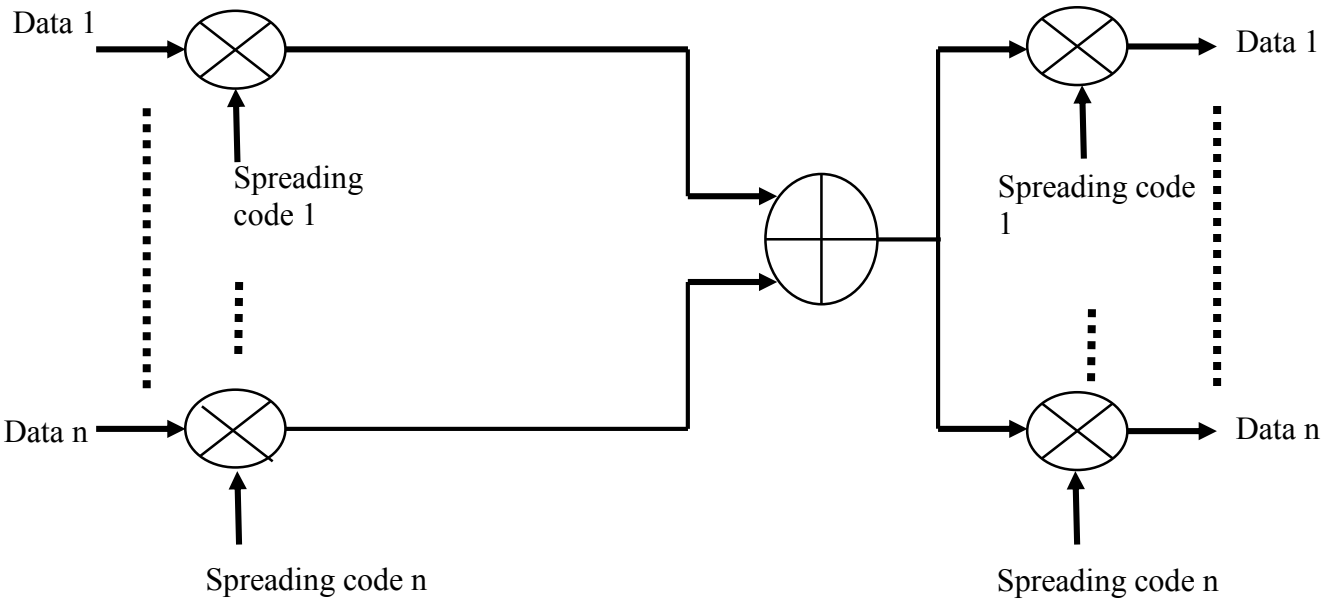

Fig 2.1.1:- Principle of CDMA techniques

The encoding process in CDMA technique is taken place before transmission operation. After encoding the data is sent to the transmitter for sending it to the receiver side through

communication channel. The data which is received at the receiver end is undergone decoding process. After decoding process the original is received by the receiver. This brief discussion of the CDMA technique. The total process is described below.

2.2 DIGITAL ENCODING AND DECODING SCHEME

DIGITAL ENCODING:-

CDMA is a analog communication system in which the analog signal are represented by continuous voltage signal or current signal. The output of encoder is represented in form of continuous voltage or the capacitance of the circuit. Due to this continuous signal output the transferring of data by continuous signal output gets obstructed due to my challenges faced by the continuous signal. The analog buses [1] are challenged due to coupling noise , clock skew, the variations of the capacitance of the circuit and the resistance which caused by the circuit implementation. To overcome the challenges faced by the data transferring through analog buses, the digital encoding and decoding scheme is developed for the code division multiple access communication technique. The principle of encoding scheme is described using the following figure 2.2.1.

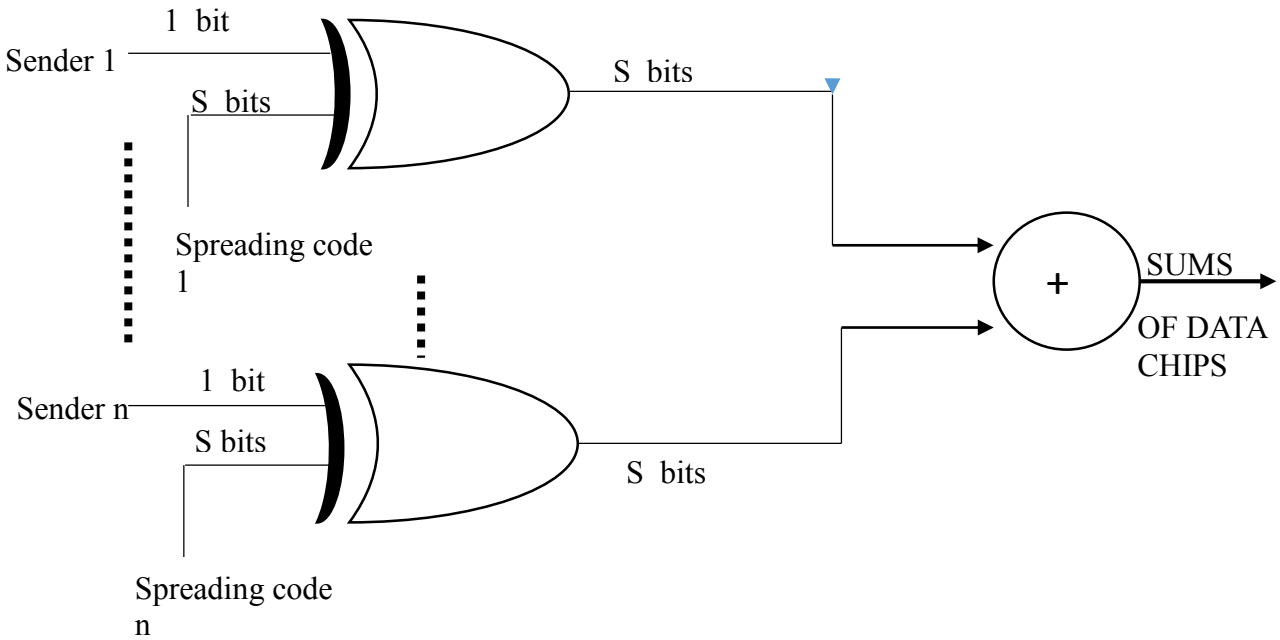

Fig 2.2.1: Digital encoding scheme

N number of signal are collected from n number of sources. These signals are given as input to the encoder in bit by bit manner. So it is a discrete form of signal processing. S bit of spreading code is generated by using PN sequence generator. For each message signal unique spreading code is used. The spreading code is S bit. The message signal is spreaded into S bits by EXOR operation of the message signal with S bit spreading code. The EXOR is based on the principle that "if all the inputs are equal the output must be zero, and if the inputs are different from each other than the output is one." For example A AND B are the 2 inputs of EXOR gate. The output is C.

A	B	C=AB'+A'B
0	0	0
0	1	1
1	0	1
1	1	0

Table 2.2.1 :- ex-or operation

The datas and the spreading codes are undergone this principle of EXOR gate. After each EXOR operation between each message signal and an unique spreading code the S bit datas are generated. Each S bit data is called as DATA CHIP. The data chips are combined with each other by addition. The resultant output is called as encoded output. The resultant output is converted into binary format. The binary form [3] of the result is taken the input of the decoder. In the encoding process after the summation operation the result is in the form of 0, 1, and 2. The result 0,1 and 2 can be coded by using binary code. So two bits are sufficient to represent the encoded result. For N input encoder N bit is required to represent the output.

The encoding process is required for conversion of different type of input data into a specialized format. By using this process transmission of data become efficient. Decoding is the opposite process of encoding. It is used to convert the special format of data into user friendly message signal at the receiving end.

This encoding operation can be easily understood by taking a small example. A 2 bit message is send into the encoder and two spreading codes are given. The

operation is described in the figure 2.2.2. The sender 1 sends a message that is 1 and the spreading code 00110011 is given. The 2nd message sender sends a signal which is represented by 0and the spreading given to it is 01011010. Then the message signals are spreaded by the EXOR operation with spreading code 1 and 2. The data chips formed are 11001100 and 01011010. They are added together. The of addition operation is 12012110. This result is encoded bit.

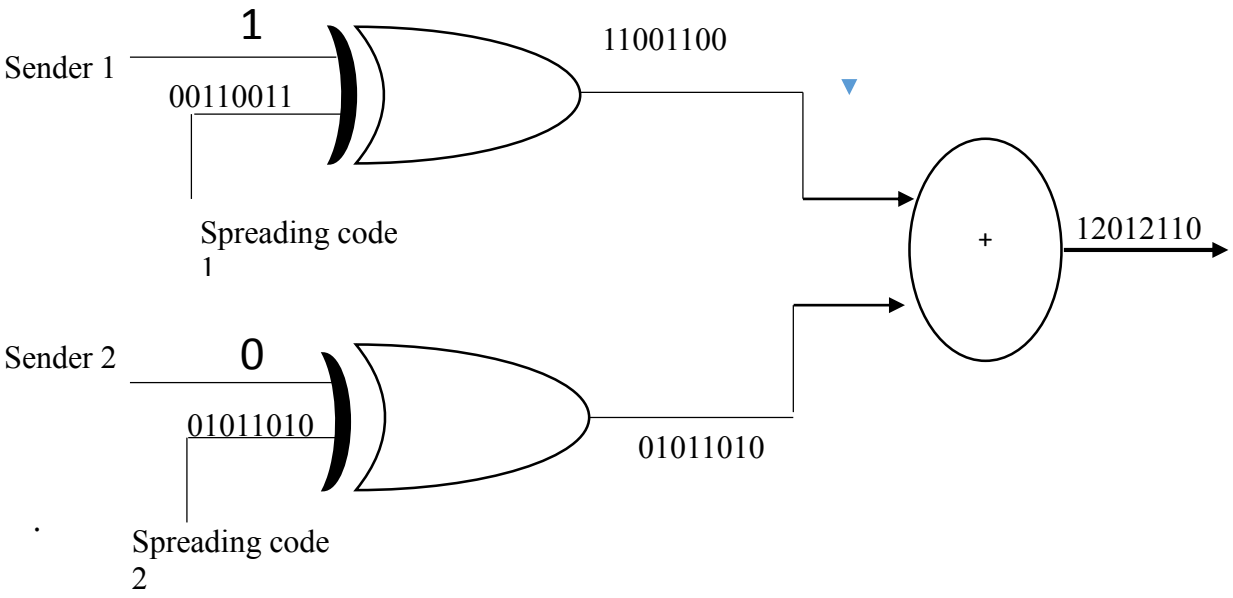

Fig 2.2.2:- Example of 2 bit encoder operation

DIGITAL DECODING:-

The digital decoding scheme is based two concepts which are

(a) Accumulation operation
(b) Comparison operation.

The encoded result is given as input to the decoder. The accumulator of the decoder is divided into two parts (a) Positive accumulator (b) Negative accumulator. The decoding operation is described by using the following figure.

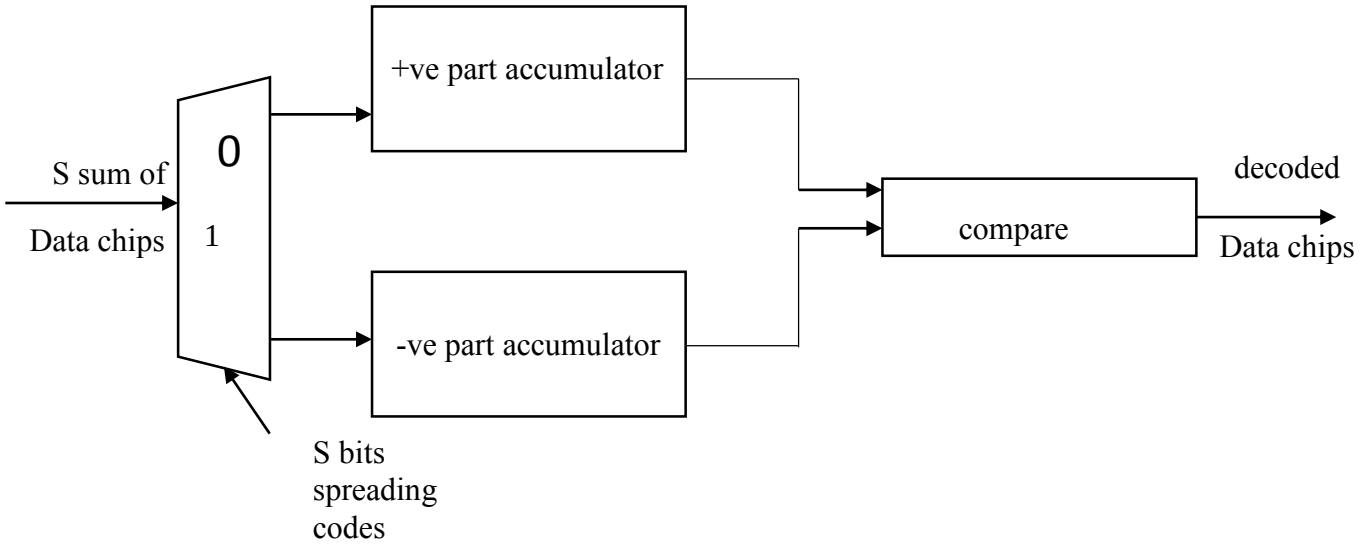

Fig 2.2.3:- Digital decoding operation

The data chips which are collected from encoder are divided into two categories by using accumulator. According to the function of accumulator it is divided into positive type and negative type of accumulator. According to the bit value of data chips spreading code are to be used for decoding operation. For decoding operation the spreading code which is used is same as the spreading code which is used for encoding scheme of that data bit. The data bit is either 0 or 1. The spreading code is playing very vital role in accumulator selection. The spreading code may be started from 0 or 1. According to the starting bit of the spreading code the positive or negative accumulator is selected. If the 1st bit of certain length spreading code is zero then the encoded output means the received data chip is moved to positive accumulator and if the 1st bit of spreading code is one then the data chip is moved to negative accumulator. This process continues upto the end of the spreading code. The principle of the decoding operation is described by one example in the below paragraph.

When the message signal send by sender is 1 and the value of the spreading code is 0 then after EXOR operation the value contributed by EXOR gate to the sum of data is always a nonzero value. The reverse operation also contribute a nonzero value to the sum of data

chip. Like this the decoding operation is also based upon the orthogonal property of the spreading code. After accumulation operation i.e positive accumulation and negative accumulation the results are compared by using comparator. According to the result of comparator the decoded bit is decided . the whole is based upon the orthogonal property of the spreading code. The value of any one of the accumulator is greater. If the value obtained by positive accumulator is greater than negative accumulator then the resultant decoded output is 1. If the value obtained by negative accumulator is greater than the positive accumulator then the resultant decoded output is 0. The encoding and decoding process are the basic rules of the CDMA communication technique. Encoder is used before transmission of data to the channel and decoder is used after the reception of the data at the receiving end. For efficient communication encoding and decoding is required.

The aim of using encoding and decoding scheme is to communicate data securely from sender node to the receiver node. The usage of large coding are avoided by using this techniques. By reducing the number bits in the coding the bandwidth required for transmission is also reduced. For encryption and error correction purpose also encoder and decoder are used. These two techniques are very useful in communication system.

2.3 STRUCTURE OF NOC BASED ON CDMA

Integration of a communication into a single chip is used to depict an architecture which is described as the solution of the face to face communication technique. A regular NOC structural engineering comprises of different sections of wires and switches. The architecture of network on chip is based on packet switching concept and circuit switching concept according to the data switching modes. But packet switched NOC is used for efficient communication system.

CDMA NOC is a packet switched concept. Between node to node transfer packet switching concept is better than circuit switched concept. The proposed CDMA NOC is described by the figure 2.3.1. This structure consists of Network Node, Transmitter and Network arbiter block.

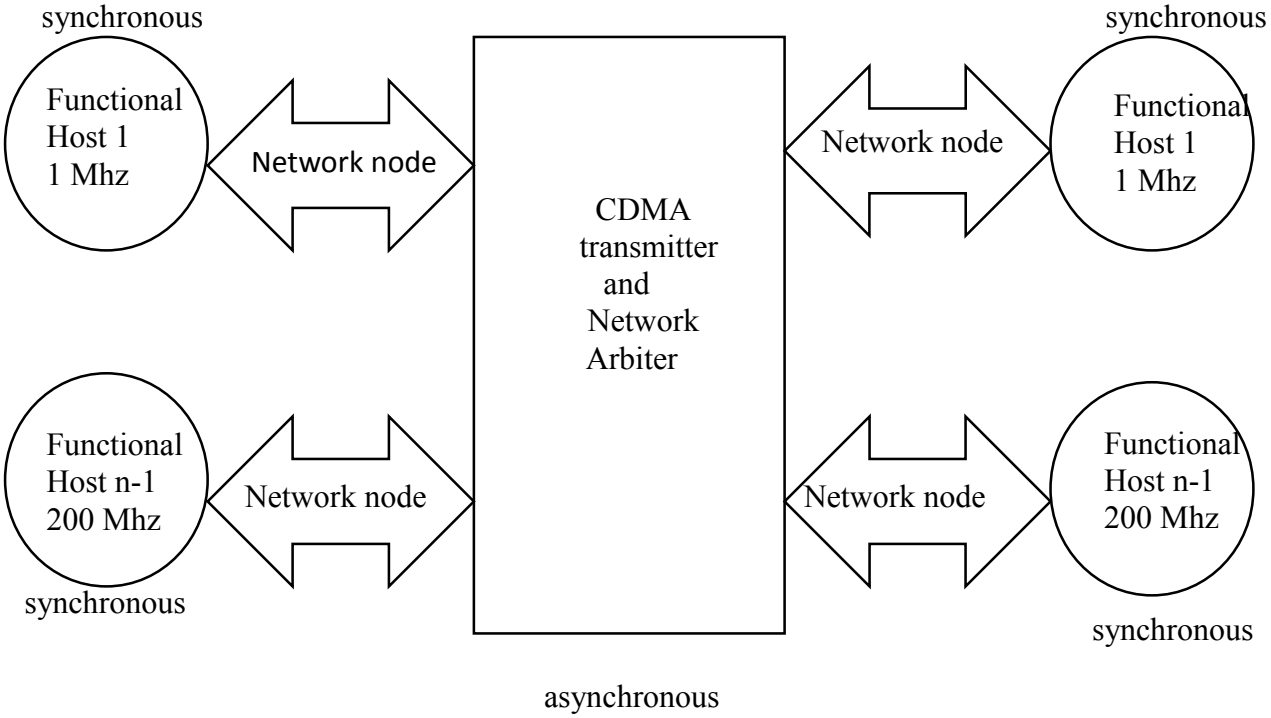

Fig 2.3.1:- CDMA NOC structure

The functional IP blocks are used as the input units to the system. These are connected to transmitter to transmit data through network nodes. The function each block is described in details in below paragraphs. Both synchronous and asynchronous data transfer can be done in this proposed structure. The communication between nodes are performed by CDMA transmitter.

The input are given in the form of functional host. Different host are sending data in frequencies. These different frequency data are combined together for transferring these data through transmitter. Due to coordinating the different frequency data problem arises. This problem can be overcome by using the globally asynchronous locally synchronous clocking scheme (GALS).

GALS scheme [14] is basically used for filling the gap between a synchronous domain or an asynchronous domain. In case of communication system for reducing the limitation raised due to data transfer at different frequencies GALS scheme is utilized. The clock given to the circuit is of different range which indicates asynchronous type of input is given

but using the asynchronous input the system cannot operate effectively so a synchronous clock is given for operation. For asynchronous data transfer a number synchronous modules are generated through which the data communication become easier and effective.

In this CDMA NOC structure both synchronous and asynchronous circuit are used. From the figure it is clear that here three type of components are used. The components are

(i) Network Node
(ii) Network Arbiter
(iii)Transmitter which is based upon CDMA concept.

(i) **Network Node**:-

The schematic details of the "Network Node" in the CDMA NOC is represented in Fig 2.7 , where the arrow pointer indicates the direction hoe datas are moving from one node to other node by using data packets. The message is distributed through packets. Each packet contains equal amount of data. The packaging of data is used for secure transmission of message. The data is entering through functional host. The "Network IF" is a part of functional host. The Network IF block of functional host is helps to transfer the data to the network node. The functional host is the outer part of the communication system. Inside the system both synchronous and asynchronous operation is combined performed for better transmission of data packets. GALS scheme is implemented inside the network node block. The total operation of the communication system is performed inside the Network Node block. As described in the figure the operation of the network Node is performed by using sub blocks. The sub blocks are

(a) Node IF
(b) Transmitter packet buffer
(c) Receiver packet buffer
(d) Packet sender
(e) Packet receiver.

The operations of the sub blocks of Network Node are described briefly. The function of each sub block is unique and specific. The detailed description of the sub block is given below.

(a) Node IF:-

The Node IF block acts like a communicator between Functional Host and Network Node. By using this Node IF the data are collected from the Network IF of Functional Host and the collected datas are moved to the transmitter packet buffer of Network Node. This block helps to divide the total data into number of data packets. Each packets are significant ID to move from sender to the required receiver node. This node is also required to combine the data packets to form the full data. The Node IF sub block sends the data to the "transmitter packet buffer" and receives the data from the "receiver packet buffer".

(b) Transmitter packet buffer :-

This sub block is a buffer which operates on the principle of asynchronous first input first output basic. The data packets which are coming from Node IF are kept in the transmitter packet buffer. The stored data are moving to packet sender by the help of transmitter packet buffer block.

(c) Receiver packet buffer:-

This sub block is similar the transmitter packet buffer. That sub block is used for out going of data at the transmitter end and the receiver packet buffer is used for in coming of data at the receiving end. It is also used for storage of data packet. For delivering data packet from "Packet Receiver" to the "Node IF".

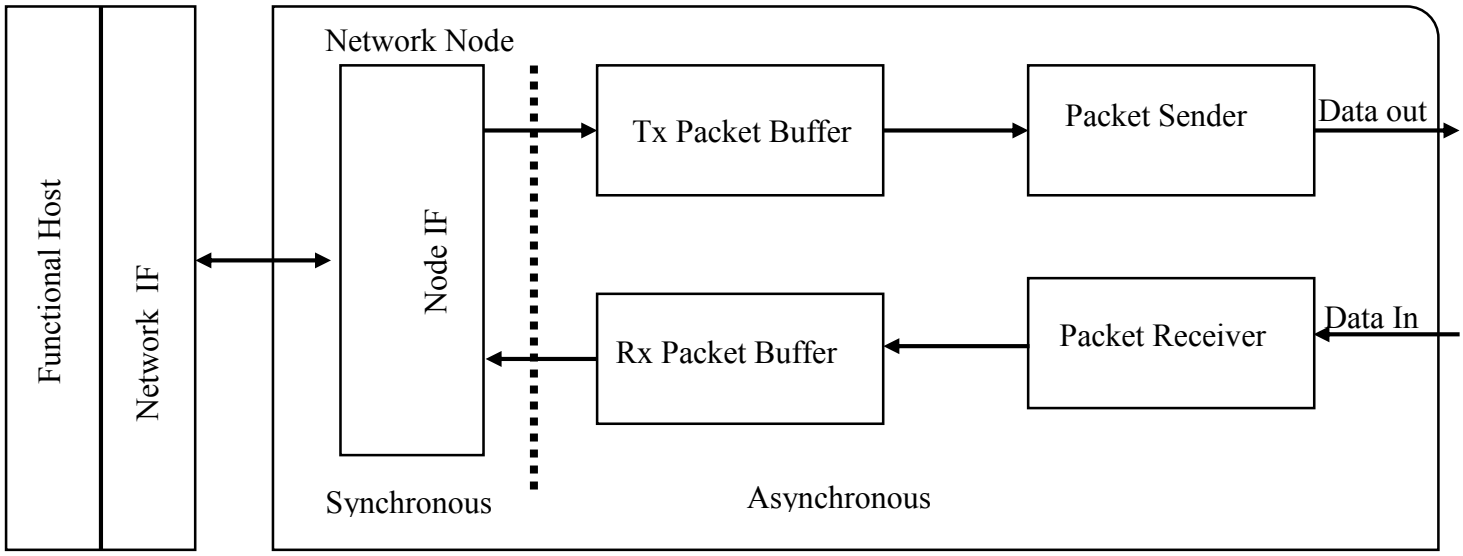

Fig 2.3.2:- Block diagram of Network Node

(d) Packet Sender:-

The data packets are stored in the "Transmitter packet buffer" sub block. When "transmitter packet buffer" is not empty , then a single packet of data is fetched by the "Packet Sender" sub block. This operation is performed on the principle of asynchronous protocol. The destination address written of the packet is extracted by using the "Packet Sender" sub block. Then the address of the destination is moved to the "Network Arbiter". When the "Network Arbiter" has given the permission to send the data packet then the "Packet Sender" sends the data packet to the transmitter block for transmission.

(e) Packet Receiver:-

The "Packet receiver" sub block is operated after the transmission and reception operation. The "Network Node" is to be reset after the function of "Packet Sender". The "Packet Receiver" sub block has been waited till the "Network Arbiter" has selected the proper spreading code and send it through sender. When the spreading code for the decoding of data is ready then the "Network Arbiter" has got a signal from receiver and that receiver is

waited to receive the data. Then the decoding operation is done. The decoded result is sent to the "Packet Receiver" to store the data properly.

The 1st part of the CDMA NOC structure that is Network Node and its functionality is described in detail in above paragraphs. Then the Network Arbiter is described below .

(ii) Network Arbiter:-

Spreading code plays a very vital role in the encoding and decoding process. The spreading which are used in the CDMA communication technique may with each other. If a single spreading code is used for number of users to encode their data packet and decode the packet into original data, then the data which are transferring through the spreading code may interfere with each other. This problem raised to the loss of the orthogonal property of the spreading code. This problem occurred due to the spreading code so it is called as spreading code conflict. This conflict can be overcome by using different protocol. The "Transmitter based protocol or T-protocol or A-T protocol" which is based on allocating a unique spreading code is applied to each user for data transfer operation. This transferring technique is a significant process for saving the orthogonal property of the spreading code. Other protocol are also used for reducing the conflict. They are as follows

(a) Common code protocol(C protocol)
(b) Receiver based protocol (R protocol)
(c) Common transmitter based protocol (C-T protocol)
(d) Transmitter – receiver based protocol(T-R protocol)
(e) Receiver –transmitter based protocol (R-T Protocol)

But the T-protocol is the best way to reduce the spreading code conflict. In T- protocol only for transmission purpose spreading is defined , but for decoding again conflict is raised. To reduce this in CDMA NOC Network Arbiter block is defined. The function of the network arbiter block is described below.

At the starting of the process when an user wants to send a data packet to another user then the sender user sends the destination address of the data packet which is to be

transferred , to the Network Arbiter block. After receiving the signal from the sender the Network Arbiter has to inform the receiver because the receiver is going to select a proper spreading code according to the sender to decode the data properly. Then after the selection of appropriate spreading code , the receiver sends an acknowledgement signal to the Network Arbiter. After getting the acknowledgement signal from the receiver the Network Arbiter block sends a signal back to sender. This signal indicates the permission for sending data packet is accepted by the Network arbiter. By this concept of sending and receiving signal before and after transmission the conflict can be overcome. At a time a number of user also wants to send the data packet to a particular receiver. Due to this the interference may arise. But the Network Arbiter block permits one user to send data to a single receiver. For selection of which user is to transmit data at what time is also a problem for Network Arbiter. This limitation can be reduced by applying "Round-Robin" arbitration scheme. This scheme is based on "First Come First Served" concept. The user which sends signal first to the Network Arbiter for sending data packet to the receiver that user get the permission first to send the data packet. But if different sender node want to send data packets to different receiver node then there is no problem. The Network Arbiter can be handled parallel operation in this type of situation.

The operation of arbiter in conventional bus based architecture is different from the Network Arbiter of CDMA NOC. For proper handling of spreading code in encoding and encoding is done by using the Network Arbiter which is used in CDMA NOC. The handling operation is done in parallel manner and it is based on time domain. According to required time for a particular transmission and reception the Network Arbiter sends the signal and receives the signal. The basic operation of Network Arbiter is the signal management for spreading code selection in time domain. But operation of arbiter which is used for conventional bus based architecture is based on time division principle. In this case the parallel of data can not be possible means at a particular time only one operation is done. In CDMA NOC structure the "Network Arbiter" block acts like a signal manger which gives a better communication with proper way of data transfer. So the CDMA NOC is better concept than the conventional bus based architecture in the basis of data transfer from node to node.

Besides "Network Node" and "Network Arbiter" , "Transmitter" also plays a vital role for the operation of CDMA NOC structure. The transmission process is based on CDMA principle. In

CDMA NOC data is transferred through packets. The principle of data packet transmission over transmitter is described below.

(iii) Transmitter based on CDMA concept :-

The function of "CDMA Transmitter" block is to receive data in the form of data packets from the "Network Node". The data packets are encoded using the encode by the unique spreading code defined for that data packet. Then the encoded signal is transmitted through transmitter. The total operation are supervised by the "CDMA Transmitter" block. Not only the reception of data but also all the operation up to the transmission of data packet through transmitted is taken care by the "CDMA Transmitter" block.

The structure of CDMA NOC is based on both synchronous and asynchronous circuit design criteria. In the figure 2.3.2 it is shown that the "CDMA Transmitter" block is under the asynchronous circuit design. Despite of realizing the asynchronous design technique the "CDMA Transmitter" block implements a new scheme for transferring information in form of data packets. The new scheme which is applied by "CDMA Transmitter" for data transfer is called as bit synchronous scheme. This scheme is based on bit by bit data transfer mechanism. This mechanism is independent upon the clock signal. In this scheme the data packets are encoded by using encoder and after encoding process the transmission is done. The data packets are transferred bit by bit manner. The encoded data is in the form of bits. So the transfer operation is easier.

The bit synchronous data transfer scheme is illustrated by one example. There are three data packets which are named as Packet A, Packet B, Packet C. At a time only one bit is to be transferred. At the starting of the transmission process, if the Network Node A and Network Node B are sending two data packet to the transmitter at a particular time. The two packets are Packet A and Packet B. Then the Network Node operates in parallel manner. The data of Packet A is encoded and transmitted through transmitter, the Packet B also encoded and transmitted in synchronous manner. The two packets are moving consecutively. After some time if the Network Node C wants to send another packet of data that is Packet C, then the "CDMA Transmitter" block has to send a waiting signal to the Network Node C. Then at the next timeslot the Network Node C sends the data packet C. In which time slot data Packet C is started to moving at that slot other two packets are also continuing their data transfer operation. The bit synchronous mechanism avoids the

interference in the data transfer process. This mechanism utilizes First come first serve principle. In this principle the data which has sent signal first to the Network Arbiter that signal is permitted to move in the first position. Due to this principle the data packets are transferred from "Network Node" to "CDMA transmitter" smoothly and effectively. So the for effective transmission process bit synchronous mechanism plays a vital role.

2.4 REALIZATION OF THE CDMA NOC STRUCTURE

For the understanding of realization of the CDMA NOC structure two issues are related. This two issues are discussed in this part of the chapter.

The two issues are

(a) Realization of Asynchronous design
(b) Data path required for CDMA NOC

(a) **Realization of Asynchronous design:-**

The CDMA NOC structure is based on two type of designing principle. In this CDMA NOC structure both synchronous and asynchronous blocks are present. The asynchronous blocks which are included in the CDMA NOC are "CDMA Transmitter", "Network Arbiter", "Transmitter Packet Buffer", "Receiver Packet Buffer", "Packet Sender" and "Packet Receiver". The synchronous and asynchronous blocks are illustrated in the figure 2.4.1.

The asynchronous design technique is based on the control logic concept. The blocks which are included in the asynchronous type are operated in this control logic principle. The "CDMA Transmitter" and "Network Arbiter" blocks are based on the path of data motion means these blocks are concentrated on data path so the control logic which is used for these asynchronous blocks is a straight forward C-element pipeline. The "Transmitter/Receiver buffer" , "Packet sender" and "Packet Receiver" are based on micro pipe line control logic which is based on the principle that "for utilizing the output which is formed in the present stage the input which is given in the past stage is enabled and disabled ".

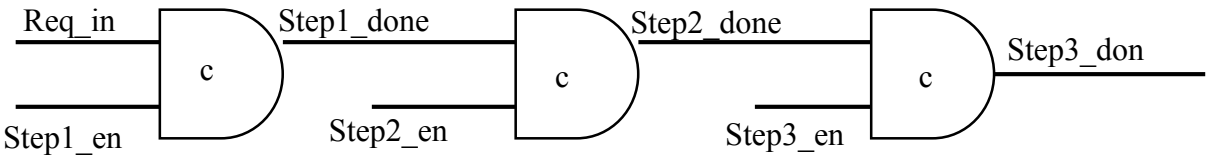

Fig 2.4.1:- C-element control pipe line

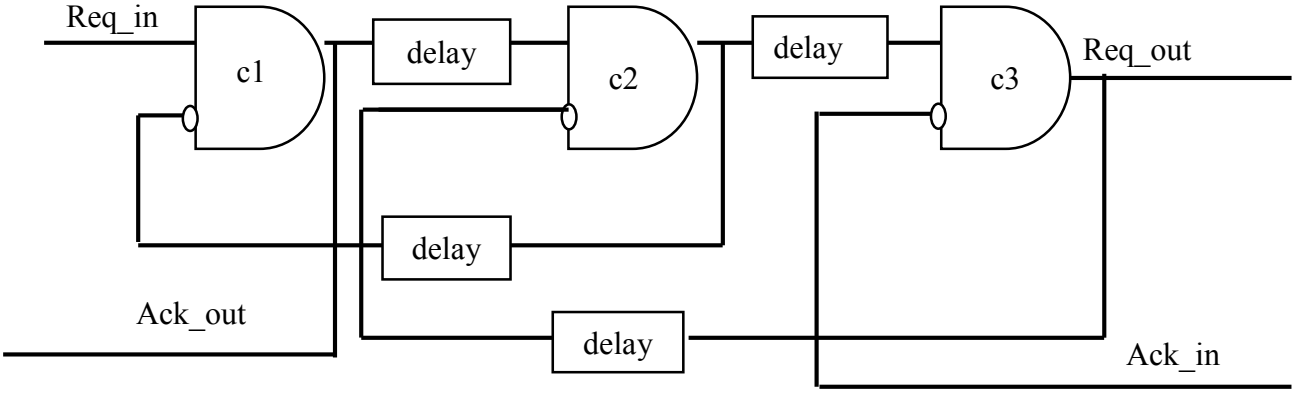

Fig 2.4.2:- Micro pipe line control logic

Fig 2.4.1 and 2.4.2 illustrates the control logic techniques. These control logic technique are based upon basic elements, C-elements, logic gates, latches, Register Transfer Logic (RTL), combinational logic gates etc. Based on these control logics the asynchronous blocks are operated. The control logic which is present in the micro pipeline control logic [9] can be realized by using logic gates.

The asynchronous blocks of the CDMA NOC structure are recognized with the register transfer logic (RTL) by using VHDL coding coordinating with the synchronous blocks for smoothly running with conventional design tool and the synchronous blocks used in the CDMA NOC structure.

(b) **Data path required for CDMA NOC :-**

The data path configuration for CDMA NOC consists of encoding and decoding process. The process of encoding is illustrated in the figure 2.2.1. The data obtained after encoding process is in the form S bits. The original single bit message signal is spreaded into S bits after the encoding operation. The data transfer latency varies largely due to the variation in the degree of data transfer between "CDMA Transmitter" and "Packet sender/Receiver" block. By increasing the number of encoded data bit and delivered by using the "CDMA Transmitter" at a particular period of time, the variation of data transfer latency is reduced. Due to this mechanism the area cost and parallism increase. To the reduce the parallism are area cost the different blocks like "CDMA Transmitter", "Packet Sender", "Packet Receiver" are realized using four different paths. The configuration of CDMA NOC is labeled in accordance with the number of data bit transferred from "Packet Sender" to "Packet Receiver " through "CDMA Transmitter".

CHAPTER-3

3.1 INTRODUCTION TO ALTIUM

3.2 DESCRPTION OF ALTIUM DESIGNER

CHAPTER - 3

3.1 INTRODUCTION TO ALTIUM

ALTIUM LIMITED is an Australian software company. This company provides a platform for designing of electronics system in personal computer. The hardware electronics systems are designed in software platform. Altium is developed in 1985 by Nicholas Martin who was working as an electronics designer at the University Of Tasmania. During his working period he has realized that availability of the tools required for printed circuit board designing were limited. These tools were collected manually which was very difficult or by using very costly software. For reducing these difficulties the Altium software is developed. Nicholas Martin has used this as designing of printed circuit board.

The first product is developed by using the software is called Dos based printed circuit board(PCB). The layout and design tools are developed by this. During starting period this software was used to fix individual component to a printed circuit board. In 1990 the field programmable gate array concept is developed for integrating the digital system in a chip. This concept is used in the Altium software for designing purpose. The tools which used for PCB design and which used for programmable logic system were different from each other, this difference became an obstacle in PCB design. For reducing these obstacles a unified system design platform was created in which a single data model is used for holding all design data required for the system design. A general project view and data model is created which helps to combine FPGA, PCB and embedded software.

By using different platform for layout designing, testing and analysis many limitation were shown. To reduce these limitation altium has designed its own software platform which is called as DESIGN EXPLORE(DXP). Altium designer is a product of altium which based on the DXP software platform. Altium Designer is an electronic outline computerization programming bundle for printed circuit board design, FPGA and implemented buy using embedded software. By increasing popularity, more and more number for features are

added in altium designer software. The version of the software varies according to functionality and speed of processing. The recent product of Altium Company is altium designer 14.2.

The Altium designer platform is used for both software and the hardware designing for a project. The platform of this is based on FPGA which is using hardware description language (HDL). Many other software languages like Java, C, verilog,VHDL etc.

The hardware used for Altium designer is called as Nano board. The microcontroller required for designing is inside the Nano board, this software has no need to access microcontroller externally.

The operation of altium is divided into number of specified type which are described as follows.

(a) schematic capture
(b) PCB design
(c) FPGA and embedded software tool
(d) Data management.

Altium Nano boards are interesting, reconfigurable equipment stages that bridle the force of reprogrammable gadgets to permit intuitive, seller free usage and organization of your hardware plans. The properties of the Nano board are

(i) Rapidly create, test, and show plan plans in genuine circumstances utilizing genuine fittings.
(ii) Get moment integration, Nano board and Altium Designer can actualize web network with a couple of mouse clicks.
(iii) Effortlessly and graphically build FPGA based installed frameworks with Altium Designer.

Altium designer combines many software in a single platform. For writing code VHDL or Verilog code in FPGA platform after execution of coding a simulator is to simulate to give the software based output. The multisim, XILLINX or Aldec simulator are used for simulating the codes written for the project. After the software part is over the schematic of the project can be designed by using the components present in the library. Once the designing is done, it goes for execution. In this process the software helps to verify the position and functionality of each

components. Then this is dumped into the Nano board. By varying the clock of input given to the circuit the result can be shown by using the Nano board.

3.2 DESCRPTION OF ALTIUM DESIGNER

Altium Designer is a product of Altium Company which is based on FPGA design platform. By using Altium Designer the embedded projects are designed using FPGA tools. Both software and hardware part of a project is done simultaneously by using Altium. Altium supports the tools of the XILLINX. The Xillinx or Multisim is required to know for doing project in Altium. It has two major parts for a project. One is software and another one is hardware. In the software the coding for the project is written. After writing the code the next step is to simulate it. The simulation operation is done by using Aldec Simulator or by Multisim. The simulation result is in the form of the waveforms. For FPGA projects the VHDL or Verilog coding technique is used. After completion of the coding part, the next step is to design a model for the required project. The designing of model is done by the tool called as schematic. For designing model for the project components are required which are placed in the library of the Altium Designer. This library contains different types of components on the basis of the hard ware required for design purpose. The library of Altium is a store of FPGA design tools. These tools include FPGA memory units, FPGA Peripheral blocks, Instruments used for FPGA design and FPGA input and outputs ports required for Nano board. These blocks contain many component. The components required for design the structure are dragged from the list of components from library and dropped in the schematic field. By using the wires and buses the components are connected with each other and form the actual structure.

According to the coding the structure is designed using above process. The input signal and output are connected to the schematic created due to coding through wires. The schematic is dumped into the Nano board. The result of the project is shown in the Nano board by using two indicators.

(a) One is in the form of LED glow
(b) Another one is TFT display.

According to the schematic the clock frequency or any type input is given to the Nano board manually by changing the frequency in the request frequency block which is present in the frequency generator block. Then the output of the schematic is shown in the Nano board. For displaying output in the from of LED glow, the output port of the schematic is connected to the LEDs present in the Nano board according to their numbers. For displaying the outputs in the TFT Display screen a specific coding is to be written for interconnecting the schematic block with the Nano board. These coding are mostly C language coding. After the coding part is over , that is to be dumped into the Nano board. This gives results in the TFT Display screen.

This part of chapter 4 describes about the how a user uses the Altium Design platform to design a project. This platform also helps to implement microcontroller application in the FPGA platform.

The Altium is complete packet of the design tools for Altera and XILLINX.

CHAPTER-4

4.1 SIMULATION RESULT

4.2 DESIGN OF CDMA NOC MODEL

4.3 REALIZATION OF PROPOSED STRUCTURE USING ALTIUM NANOBOARD

CHAPTER- 4

4.1 SIMULATION RESULT

The structure of Network on Chip is modelled by using the CDMA concept. The FPGA platform is used for modelling of NOC. The CDMA communication system is formed by combining the encoding, decoding, transmission and reception process. The CDMA transmission process is coded by using the VHDL coding technique. The Altium software is a FPGA platform in which both the coding and implantation of the coding can be done. The aldec simulator of the altium is used for simulation of the VHDL coding of transmission process. In the coding for transmission encoding of the input data and the transmission process is included. For encoding operation a sequence of spreading code is required. The spreading code is generated by using PN sequence generator. The coding of PN sequence generator to generate a series a spreading code is included in the transmission coding. The details of the coding part is described below.

Three bit data is given as input to the encoder. Three data indicates 0 to 7 or eight possible value is used as input. The message signal is the binary representation of value 0 to 7. For encoding these three bit data 3 PN sequences are required. For particular one input one PN sequence is generated. The PN sequence are generator by the EXOR operation of past output. The PN sequences are stored. When required these PN sequences are given inside the coding. After encoding operation of the individual message signal the encoded output formed is transferred from sender node to the receiver node. The encoding operation include EXOR and summation principle. The input data is spreaded by the EXOR of this data with the PN sequence generated by the PN sequence generator. Then all the outputs of the EXOR operation is added together. After both operation for each three bit data only one code is generated. The generated code is transferred from source to destination. By using 3bit the result of the encoding operation is shown. This process is based upon the input clock signal. According to the variation in the clock signal the speed of data transmission varies. After one 3 bit message signal transferred from source to destination the transmitter is reset. After reset operation the process again starts to generate PN sequence and encoding operation is performed. The resultant output is transferred from source to destination.

This process continuous till all the message signal are transferred from sender end to the receiver end. The output this coding process is in the form of transmission output. The output of this coding process is shown by the figure below.

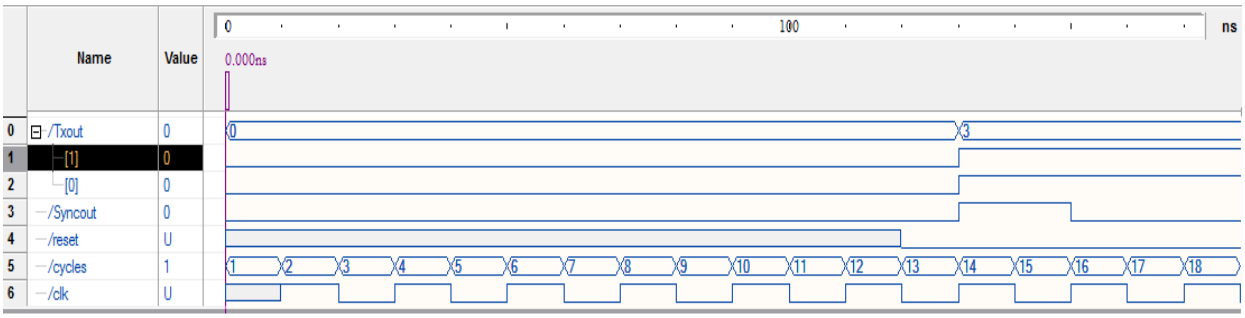

Fig 4.1.1:- Result of VHDL coding for CDMA (time duration from 0 to 100ns)

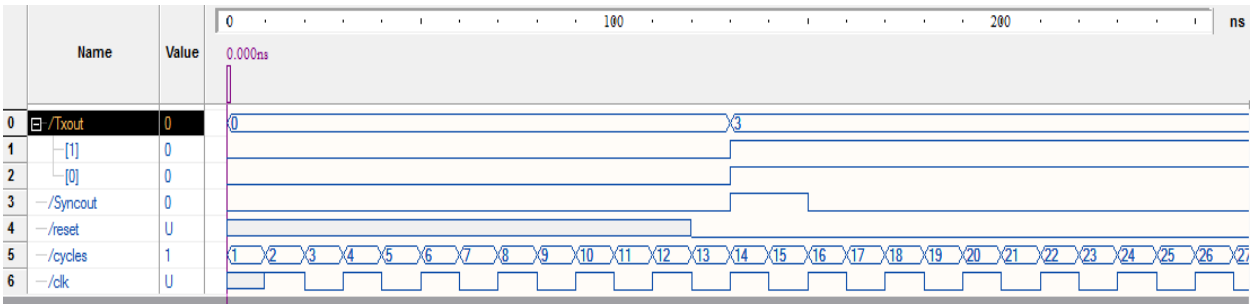

Fig 4.1.2:- Result of VHDL coding for CDMA (time duration from 0 to 200ns)

The input given for the transmission is in the form of clock signal. The clock signal value may be zero or one. When the clock signal is one then the operation of transmission is performed. The reset is another input given in the entity part. The output is shown in the above figure is in term of "Txout". The output of transmission operation is represented by binary representation. So only two bit is sufficient to show the result. So the output in the result shown is resented in two bits. Then the "cycle" which is shown in the results counts the number of cycles performed during the execution of the program. According to the time given for executing the program the no of cycle is decided. From 1 the cycles count starts up to the end of the execution. The cycle acts like a counter in executing the program. This also decides another output bit that is synchronous output. If the counter value is zero then the synchronous output is showing 1 and otherwise the result of the synchronous counter is 0. By using the above two simulation result, the transmission output

is known. This part is only shows the software part of the CDMA NOC structure. According to the coding the structure of the CDMA NOC is designed by using the schematic block of Altium software. The basic schematic block is created from the coding part by altium software.

4.2 DESIGN OF CDMA NOC STRUCTURE

The Altium Designer tool is based on both software coding and the hardware implementation of the software coding. For designing a structure this software consists of a number user friendly components according to the Nano board designed to implement the hardware. The components are stored in the library of Altium designer. To design a structure the Altium designer has a different platform that is schematic platform. For designing the schematic of a model the basic requirement is the VHDL or VERILOG coding. By the use coding the basic block containing the input output ports is generated and kept in the schematic block. After creating this block the input sources and output sources are connected to the basic schematic block. This sources are dragged from the library present in the Altium Designer platform. But this sources are dependent upon the Nano board specification. The Nano board of series 3000 is using in this project. The particular Nano board used for this project is NB 3000XN.05 which is based on Xillinx Spartan 3AN. The output of a structure can be shown in two forms one is in the form of LED glow and another one is in the form of TFT display.

The components selected from library for designing of the model of CDMA NOC are the components which are supporting for Nano board. The input sources are used for the structure of CDMA NOC clock signal and test buttons. The output are shown in form of LED. The glowing of LED shows the output of the structure in form of binary bits. As discussed in the section 4.1 the transmission output is in the form of binary bit representation. So only two LED is sufficient to show the output of the transmission. The synchronous output is a single bit output so only one bit is required to represent the synchronous output. According to the variation of frequency of the clock the speed of the transmission process varies. This shows how data transfer depends upon the clock signal. In input side the clock signal is connected to the clock part of the basic schematic created by the coding. The reset pin is connected to the test button. The test button is always in the inverting mode. So a logic inverter is connected between the test button and the reset pin. In the output side the transmitter port is connected to 2 bit LED because binary

bit is sufficient to show the transmitter output. The synchronous output connected to one LED because to display the Synchronous output only one bit is sufficient. The required model of the CDMA NOC structure is shown in the below figure. The result can be analyzed by the glow of LED. According to the change in frequency the LED glow also varies.

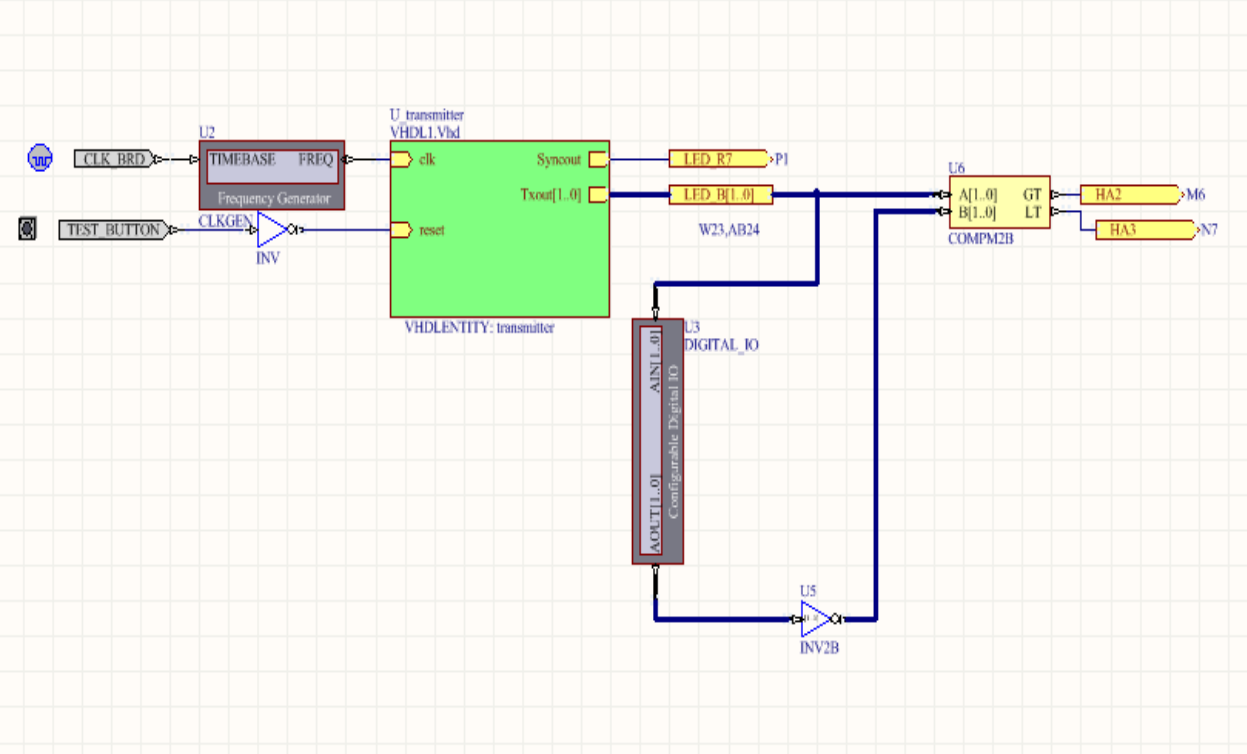

Fig 4.2.1:- Schematic model of CDMA NOC structure

The clock signal can be given in form of frequency. The frequency generator is connected to the clock signal block for giving different frequency to the basic schematic block.

Fig 4.2.2:- The frequency generator

The frequency can be changed in the request frequency section. In the above diagram is shows a frequency of 10 Hz. According to the requirement the frequency can be set.

4.3 RELIAZATION OF STRUCTURE USING NANOBOARD

The proposed structure is shown using Nano board. The structure created in altium designer schematic platform is dumped into the Nano board. Then clock signal is using that frequency generator. Then the output is displayed in the Nano board in the form of glowing the light. The Nano board result is shown in the below figure.

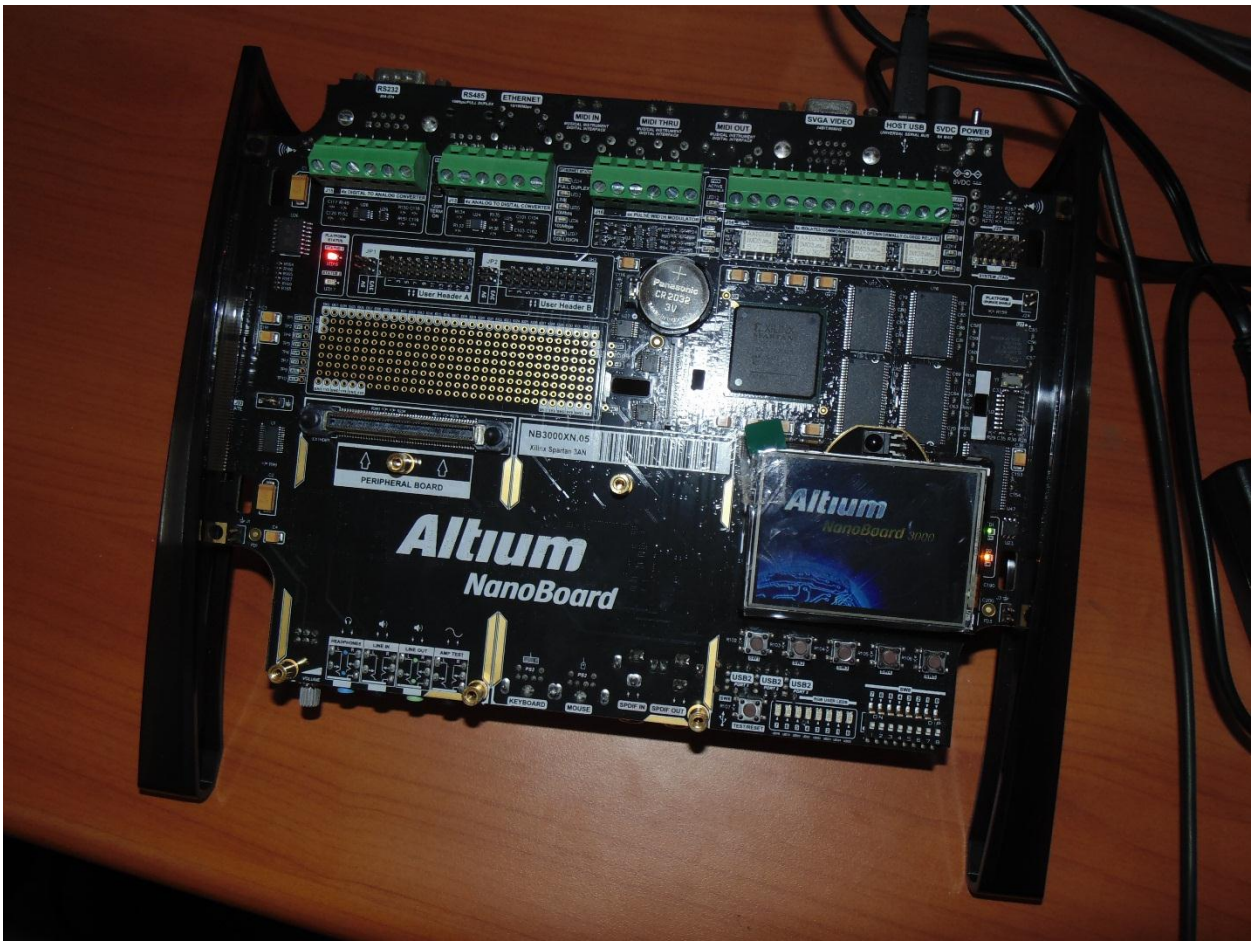

Fig 4.3.1:- Nano board representation of CDMA NOC structure

CHAPTER -5

5.1 COMPARISION OF CDMA NOC WITH PTP NOC

5.2 CONCLUSION

5.3 FUTURE WORK

REFERENCES

CHAPTER -5

5.1 COMPARISON OF CDMA NOC WITH PTP NOC

The Packet switched Network On Chip is divided into two categories.

(a) CDMA NOC (Code division multiple access network on chip)

(b) PTP NOC (Point to point network on chip)

The CDMA NOC and PTP NOC is compared on the basis of following properties.

(i) Resemblance of Data transfer principles

(ii) Comparative study of network node structure

(iii) Resemblance of data transfer latencies

(iv) Comparative study of area and power cost

(i) Resemblance of data transfer principle :-

In case of Point to Point NOC, the load applied in the PTP NOC due to data traffic is converted is converted into interconnection links between the network nodes. Due to distributed traffic scheme flexibility and scalability in data transfer occurs, these are the advantages of PTP NOC. But data transfer latency varies between Network Nodes, when data is transferred from network node to different destinations or to the same destination by using different route.

In the Point to Point NOC the data can be transferred in parallel manner if the process of data transfer is done between different links established in the network node. But in case of PTP scheme concurrent data transfer can not be possible in a single link because the sharing of link of the Network Nodes is done by using time division manner. The CDMA NOC structure supports the concurrency in the data transfer. By using concurrent data transfer scheme the CDMA NOC structure has a constant data transfer value by which it can give a valuable on chip communication system.

The multi cast data transfer scheme can be easily implement by using CDMA NOC. This scheme indicated that a same spreading code is used by multiple number of receiver for receiving the data packets. This mechanism can not be utilized in PTP NOC. This one very useful advantage of CDMA NOC.

Each packet which is to transferred from one Network Node to other that has two parts one is header part another one is message part. In case of PTP NOC the total packet is to transferred for data transmission to identify the receiver Node. But in case of CDMA NOC due to the operation of the "Network Arbiter" the receiver Node gets the information of the data packet which it is going to be receive, before reception of the data packet in form signal.

(ii) Comparative study of Network Node structure:-

Both in case of CDMA NOC and PTP NOC [7] the Network Node plays vital role communicating the datas from source to the destination. In case of PTP NOC the Network Node structure is based on layer approach of communication between the nodes. It is also uses the bidirectional ring topology which increases the system complexity. But in case of CDMA NOC the network nodes are managed properly due to which system complexity is reduced. Due to the proper message transfer by the signal based operation which indicates one – hop data transfer scheme the Network Node of CDMA NOC does not required to handle any type of bypass data packets for communication. CDMA NOC is based on a centralized traffic scheme. So it can overcome the limitation which is shown in the layered approach for communication utilized in PTP NOC. The network node structure of the PTP NOC is very complex in comparison with Network Node structure of CDMA NOC. In case of PTP NOC a communication controller is required to control the node to node communication process. So the Network Node of CDMA is better than the Network Node of PTP NOC.

(iii) Resemblance of Data transfer latencies:-

The CDMA NOC and PTP NOC both the packet switched data transfer scheme utilizes one common clock based concept that is globally asynchronous and locally synchronous scheme that is called as GALS scheme. So on the basis of this scheme the PTP NOC and CDMA NOC can not be compared with each other. So the data transfer latencies between these two models can be separated by using another one simulation based networks. These two parts of the networks are STL (synchronous transfer latency) and ATL (asynchronous transfer latency). These two parts describes how the data transfer latency of CDMA NOC is constant and performs better communication between nodes. Mostly the 32-bit CDMA NOC has better data transfer latency than other structures.

(iv) Comparative study of power costs and area :-

The comparative result of the CDMA NOC and the PTP NOC in the basis of power cost and area is described in a tabular format .

NOC TYPE	DATA PATH WIDTH	SIX – NODE SIMULATION NETWORK		
		AREA BITS(pJ)	DYNAMIC POWER	ENERGY COST 32-BIT DELIVERING 32
CDMA NOC	1-BIT	113.145	19.340	12.5168
	8-BIT	148.369	6.563	7.7428
	16-BIT	191.037	7.331	4.0868
	32-BIT	272. 806	7.332	4.0873
PTP NOC	32-BIT	177.007	7.324	4.7401

Table 5.1.1 :-Comparison of CDMA NOC with PTP NOC on the basis of power costs and area

5.2 CONCLUSION

The structure of Network On Chip in the principle of code division multiple access concept is proposed. The CDMA NOC supports GALS scheme to communicate data from the source to the destination node. For communicating data the encoding , decoding , transmission and reception process is required. The encoding and decoding process is described properly. On the basis of encoding and decoding data transmission operation is coded by using VHDL coding technique. From the results it can understood that transmission process is fully based on the frequency. The proposed CDMA NOC structure is designed by using the designing tool based on Altium software. This structure is to implemented in the Nano board successfully. The theoretical comparison between the Point To Point Network On Chip and Code division multiple access Network on chip is properly discussed. From the comparative study it is known that the performance of CDMA NOC structure is better than the structure of PTP NOC.

5.3 FUTURE SCOPE

1. NOC design can be investigated by using FHSS technique.

2.Futher enhancement of data transfer rate using packet switch network.

REFERENCES

[1] R. Yoshimura, T. B. Keat, T. Ogawa, S. Hatanaka, T. Matsuoka, and K. Taniguchi, "DS- CDMA wired bus with simple interconnection topology for parallel processing system LSIs," in Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf., 2000.

[2] T. B. Keat, R. Yoshimura, T. Matsuoka, and K. Taniguchi, "A novel dynamically programmable arithmetic array using code division multiple access bus," in Proc. 8th IEEE Int. Conf. Electron., Circuits Syst.,2001.

[3] R. H. Bell, Jr., K. Y. Chang, L. John, and E. E. Swartzlander, Jr.,"CDMA as a multiprocessor interconnect strategy," in Conf. Record 35th Asilomar Conf. Signals, Syst. Comput., 2001.

[4] D. Wiklund and D. Liu, "SoCBUS: Switched network on chip for hard real time systems," in Proc. Int. Parallel Distrib. Process. Symp. (IPDPS), 2003.

[5] S. Shimizu, T. Matsuoka, and K. Taniguchi, "Parallel bus systems using code-division multiple access technique," in Proc. Int. Symp. Circuits Syst., 2003.

[6] . M. Simon, J. Omura, R. Scholtz and B. Levitt, "Spread spectrum communications hand book", McGraw-Hill, 2002.

[7] X. Wang, D. Sigüenza-Tortosa, T. Ahonen, and J. Nurmi, "Asynchronous network node design for network-on-chip," in Proc. Int.Symp. Signal, Circuits, Syst., 2005.

[8] X. Wang, T. Ahonen, and J. Nurmi, "Prototyping a globally asynchronous locally synchronous network-on-chip on a conventional FPGA device using synchronous design tools," in Proc. Int. Conf. Field Program. Logic Appl., 2006.

[9] X. Wang and J. Nurmi, "A RTL asynchronous FIFO design using modified micropipeline," in Proc. 10th Biennial Baltic Electron. Conf.(BEC), 2006.

[10] E. S. Sousa and J. A. Silvester, "Spreading code protocols for distributed spread-spectrum packet radio networks," IEEE Trans. Commun., vol. 36, no. 3, Mar. 1988.

[11] K. Goossens, J. Dielissen, and A. Radulescu, "Æthereal network on chip: Concepts, architectures, and implementations," IEEE Des. Test Comput., vol. 22, no. 5, Sep./Oct. 2005.

[12] D. Sigüenza-Tortosa, T. Ahonen, and J. Nurmi, "Issues in the development of a practical NoC: The proteo concept," Integr., VLSI J., vol. 38, no. 1, 2004.

[13] A. J. Viterbi, CDMA: Principles of Spread Spectrum Communications. Reading, MA: Addison-Wesley, 1995.

[14] D. M. Chapiro, "Globally-asynchronous locally-synchronous systems,"Ph.D. dissertation, Dept. Comput. Sci., Stanford University,Stanford, CA, 1984.

[15] X. Wang, T. Ahonen, Jari Nurmi, "Applying CDMA technique to Network-on-Chip," IEEE Trans. VLSI. pp. 1091-1100. October 2007.

[16] D. Kim, M. Kim, G. E. Sobelman, "CDMA Based Network On Chip Architecture," IEEE Asia-Pacific Conference on Circuits and Systems, pp. 137-140. December, 2004.

[17] M. Kim, D. Kim, and G. Sobelman, "Design of a high-performance scalable CDMA router for on-chip switched networks," in Proc. Int. SoC Des. Conf., pp. 32-35. 2005.

[18] D. Kim, M. Kim, G. E. Sobelman, "FPGA based CDMA switch for Network-on-Chip", IEEE 13th Annual Symposium in Field-Programmable Custom Computing Machines. PP. 283-284. October 2005.

[19] L.Benini and G.D Micheli, "Network on Chips: A new SoC Paradigm,"IEEE computer ,Vol. 35, Issue 1, January 2002, pp. 70-78.

[20] Daewook Kim,Manho Kim and Gerald E.Sobelman "FPGA-based CDMA Switch for Networks-on-Chip" , (FCCM'05), IEEE computer SoCiety, 2005.