PERFORMANCE ANALYSIS OF DUAL MATERIAL GATE (DMG) SILICON ON INSULATOR (SOI) TUNNEL FETs

A dissertation submitted in partial fulfilment of the requirements for the degree of

MASTER OF TECHNOLOGY
IN
VLSI AND EMBEDDED SYSTEM

by

SHARA MATHEW
ROLL NO:212EC2138

to the

Department of Electronics and Communication Engineering

National Institute of Technology

Rourkela, Orissa, India

May 2014

PERFORMANCE ANALYSIS OF DUAL MATERIAL GATE (DMG) SILICON ON INSULATOR (SOI) TUNNEL FETs

A dissertation submitted in partial fulfillment of the requirements for the degree of

MASTER OF TECHNOLOGY
IN
VLSI AND EMBEDDED SYSTEM

by

SHARA MATHEW
ROLL NO:212EC2138

Under the Supervision of
Prof.(Dr.) P.K.TIWARI

to the

Department of Electronics and Communication Engineering

National Institute of Technology

Rourkela, Orissa, India

May 2014

DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ODISHA, INDIA-769008

CERTIFICATE

This is to certify that the thesis report entitled "**Performance Analysis of Dual Material Gate(DMG) Silicon On Insulator(SOI) Tunnel FETs**", submitted by **SHARA MATHEW** , bearing **roll no. 212EC2138** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded Systems**" during session 2012-2014 at National Institute of Technology, Rourkela is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Place: Rourkela

Date: 20th May, 2014

Prof. (Dr.) P. K. TIWARI
Dept. of E.C.E
National Institute of Technology
Rourkela – 769008

Dedicated to my family

ACKNOWLEDGEMENT

With solemn respect and deepest gratitude, I would like to thank my project supervisor Prof.(Dr.) P.K.Tiwari who has always been the motivating force of this project work. His complete commitment to research work as well as tireless effort to gain knowledge and share it with his students had made him a true academician, who has become a source of inspiration for me. I am indebted to him for his valuable guidance, support throughout my project work as well as the good amount of time he had given to me to clarify my doubts and discuss about my work. I express my sincere gratitude to Prof.(Dr) K.K.Mahapatra, Prof.(Dr.) D.P Acharya, Prof.(Dr.) Nurul Islam, Prof.Ayas Kanta Swain, Prof.(Dr.) Poonam Singh who had introduced the world of VLSI and Embedded System and helped me in grabbing knowledge in various domains of my specialization. I would also like to thank Prof.(Dr.) Sukhdev Meher and all other faculties and staff of ECE Department, NIT Rourkela for their help and support to complete my project work.

I am truly thankful to all research scholars of ECE Department, NIT Rourkela, especially Mr. Gopi Krishna S, Mr. Visweswara Rao , Mr. George Tom ,Mr Sudeendra Kumar, Mr Jaganath Mohanty and Mr Venkataratnam, who were always ready to share their knowledge throughout our course . I express my heartfelt gratitude to my colleague and friend Ms. Silpeeka Medhi with whom I always shared a peaceful and friendly working environment. I also extend my gratitude to Mr.Anand Mukhopadhyay, Mr.Raju Gorla and Mr.Ajit Kumar for the worthy ideas we had shared on our respective research areas. I am really thankful to all my classmates and other friends who had made my stay in NIT a pleasant experience.

Lastly I thank my family whose constant support and encouragement, always help me move forward in life even during hard times.

Finally, I bow myself to Almighty God whose blessings guard and guide me throughout my life.

Shara Mathew

ABSTRACT

As modern day computing systems are designed to perform innumerable number of functions with tremendous speed, the number of circuits to be accommodated in a chip keeps increasing day by day. Hence electronics industry constantly faces the challenge of miniaturization of transistors to increase the package density and thus linear scaling of CMOS technology has become a necessity in the present day microelectronic and nano-electronic regime. This leads to a major crisis of static power consumption and hence conventional MOSFETs fail to be a suitable candidate to handle the situation. Also Short Channel Effects(SCEs) come into picture. So non-conventional devices started gaining its significance to meet the ITRS requirements.

A promising candidate that attracted attention was Tunnel FETs which are gated reverse biased p-i-n diodes where ON current would be due to band-to-band tunneling and they exhibit very low OFF current of 10^{-17} A/μm which makes them a potential solution for power crisis. Also they prove to be an energy efficient electronic switch with a subthreshold swing not limited to 60mV/decade. Negligible Short Channel Effects of these devices gives them an added advantage over conventional MOSFETs .All these features raise up Tunnel FET as superior candidate for future CMOS era.

In the presented work, an analysis into the performance of a Dual Material Gate Single Dielectric SOI Tunnel FET has been done. Numerous simulations were done to determine the influence of work functions of both the gate materials on the electrical characteristics of the device. Comparative study was done between Dual Material Gate device and Single Material Gate device with regards to their electrical characteristics as well as SCEs like Drain Induced Barrier Lowering(DIBL) and threshold voltage roll-off. Parameters like intrinsic capacitances as well as transconductances were also determined.

The same analytic approach was extended to Dual Material Gate Hetero Dielectric SOI Tunnel FET to analyze the improved performance of the device compared to its Single Dielectric Dual Material Gate counterpart .Thus the work presented had all together analyzed attributes of incorporating Dual Material Gate as well as Hetero Dielectric in SOI Tunnel FET structures. Extensive simulations for the presented work were performed by using two dimensional device simulator (ATLAS™ SILVACO Int.)

TABLE OF CONTENTS

ABSTRACT.....VI

1. INTRODUCTION.....1
    1.1. SEMICONDUCTOR TECHNOLOGY SCALING : A HISTORICAL OVERVIEW.....3
    1.2. TYPES OF SCALING.....3
        1.2.1. Full Scaling (Constant Field Scaling).....3
        1.2.2. Constant-Voltage Scaling.....3
        1.2.3. General Scaling.....3

    1.3. POWER SHORTAGE IN THE ELECTRONIC INDUSTRY.....4

    1.4. LIMITATIONS DUE TO SCALING OF CONVENTIONAL MOSFETs.....6
        1.4.1. Channel Length Modulation.....6
        1.4.2. Short Channel Effects (SCEs).....6
            1.4.2.1. Velocity Saturation of Carriers.....6
            1.4.2.2. Drain Induced Barrier Lowering (DIBL) and Punch Through.....6
            1.4.2.3. Surface Scattering.....7
            1.4.2.4. Impact Ionization.....7
            1.4.2.5. Hot-Carrier Injection.....7

        1.4.3. Narrow Channel Effect.....7
        1.4.4. Subthreshold Conduction.....8

    1.5. REQUIREMENTS FOR FUTURE GENERATION TRANSISTORS.....8
        1.5.1. NEMFETs (Nano Electro Mechanical FETs).....9
        1.5.2. Ferroelectric gate dielectric FET.....9
        1.5.3. IMOS (Impact Ionization FETs).....9
        1.5.4. Feedback FETs (FBFETs).....10
        1.5.5. Tunnel FETs (TFETs).....10

    1.6. INTRODUCTION TO TUNNEL FETS.....10
        1.6.1. Structure And Operation.....11
        1.6.2. Ambipolar Nature Of Tunnel FETs.....13
        1.6.3. Band To Band Tunneling Mechanism.....14
        1.6.4. Features And Merits Of Tunnel FETs.....16

    1.7. THESIS ORGANISATION.....17

2. LITERATURE REVIEW.....18
    2.1 DOUBLE GATE TUNNEL FET.....19
    2.2 JUNCTIONLESS TUNNEL FIELD EFFECT TRANSISTOR.....20
    2.3 DUAL MATERIAL GATE TUNNEL FIELD EFFECT TRANSISTORS.....20
    2.4 PAST WORK.....20

3. SIMULATION METHODOLOGY.....23

    3.1 INTRODUCTION.....23
    3.2 STEPS TO DEFINE A STRUCTURE.....24
        3.2.1. Load a structure from Athena.....24
        3.2.2. Load a structure from DevEdit.....25
        3.2.3. Using ATLAS Commands to define a structure.....25
    3.3 SPECIFYING MODELS TO BE USED.....27
    3.4 COMMON MODELS USED IN BRIEF.....27
        3.4.1 Concentration-Dependent Low-Field Mobility Model.....27
        3.4.2 Analytic Low Field Mobility Model.....27
        3.4.3 Lombardi CVT Model.....27

3.4.4 Shockley-Read-Hall Recombination Model……………………………………………………..........................28
3.4.5 Auger Recombination Model………………………………………………………………..........................28
3.4.6 Boltzmann Model……………………………………………………………………………........................28
3.4.7 Fermi-Dirac Model…………………………………………………………………………..........................28

3.5 TUNNELING MODELS OF SIGNIFICANCE…………………………………………………......................28
3.5.1 Standard Band To Band Tunneling Model…………………………………………………......................28
3.5.2 Schenk Band to Band Tunneling Model……………………………………………………......................29
3.5.3 Kane Band-To-Band Tunneling Model……………………………………………………........................29
3.5.4 Non-local Band-to-Band Tunneling Model……………………………………….……………….....29

3.6 NUMERICAL METHODS…………………………………………………………………………..........................31

3.7 OBTAINING SOLUTIONS……………………………………………………………………….........................31
3.7.1 DC Solution………………………………………………………………………………...............................31
3.7.2 AC SOLUTION……………………………………………………………………………..............................32

3.8 INTERPRETING THE RESULTS……………………………………………………………...........................32
3.8.1 Run-Time Output………………………………………………………………………...............................32
3.8.2 Log Files……………………………………………………………………………….............................32
3.8.3 Parameter Extraction In DeckBuild……………………………………………………….........................33

3.9 MODELS USED IN SIMULATIONS OF DEVICES UNDER STUDY………………………….........................33

3.10 SIMULATED STRUCTURE OF SINGLE DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FET………………………………………………………………….……...........................33

4. ANALYSIS OF SINGLE DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FET…………………………….......36

4.1 INTRODUCTION…………………………………………………………………………….………………...36
4.2 DEVICE STRUCTURE IN DETAIL……………………………………………………….........................36
4.3 OPERATION………………………………………………………………………………….........................38
4.4 SIMULATION RESULTS……………………………………………………………………………………...38
4.5 CONCLUSION……………………………………………………………………………………………….......47

5 ANALYSIS OF HETERO DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FETS…………………………......48

5.1 INTRODUCTION…………………………………………………………………………………………….48
5.2 DEVICE STRUCTURE IN DETAIL………………………………………………………..........................48
5.3 OPERATION…………………………………………………………………………..............................50
5.4 SIMULATION RESULTS………………………………………………………………............................50
5.5 MERITS OF HD-DMG SOI TFET OVER SD-DMG SOI TFET…………………………….............................59
5.5.1 Reduction Of Threshold Voltage And Improvement In On Current…………………….............................59
5.5.2 Improvement in Output Characteristics…………………………………………………………..........60
5.5.3 Improvement In DIBL……………………………………………………………...............................60
5.5.4 Reduction In Threshold Voltage And Threshold Voltage Roll Off……………………….............................61
5.5.5 Improvement in Intrinsic Capacitances…………………………………………..................................61
5.5.6 Higher Transconductance…………………………………………………………………..........62
5.6 CONCLUSION………………………………………………………………………...…………………..63

6 CONCLUSION……………………………………………………………………………...............................64
6.1 PERFORMANCE ANALYSIS……………………………………………………………...............................64
6.2 SCOPE OF FUTURE WORK……………………………………………………………...............................65

LIST OF FIGURES

Fig.No Page No.

Fig. 1.1 First IC developed by Jack Kilby at Texas Instruments…………………………………………………...1
Fig. 1.2 First commercial IC developed by Robert Noyce at Fairchild semiconductor corp…………………………1
Fig.1.3 Transistor integration on chip displaying Moore's Law……………………………………………………2
Fig.1.4 Reduction in size of technology over the years……………………………………………………………..3
Fig.1.5 Device structure of simple SOI Tunnel FET………………………………………………………………11
Fig.1.6 energy band diagram along a horizontal cut on the n-type tunnel FET in OFF state and ON state………..12
Fig.1.7 Transfer characteristics of Double Gate(DG) Tunnel FET ………………………………………………13
Fig.1.8 Band diagram of a p-n junction with electron undergoing (a) direct band to band tunneling
(b) indirect band to band tunneling………………………………………………………………………………14

Fig.2.1: the structure of double gate tunnel fet with an intrinsic length of 59nm, dielectric thickness of 3nm……..18
Fig 2.2 : Schematical representation of the JL-TFET. The width of device equals to 1 µm.
Work function (CG) = 4.3 eV, Work function (PG) = 5.93 eV……………………………………………………19
Fig.2.3. Schematic diagram of a SD-DMG TFET…………………………………………………………………20

Fig.3.1 Inputs and Outputs of Atlas device simulator……………………………………………………………...24
Fig..3.2 Schematic of non-local band to band tunneling…………………………………………………………..30
Fig.3.3 Tonyplot structure file of SD-DMG SOITFET……………………………………………………………...33
Fig.3.4 Tonyplot structure file of SD-DMG SOITFET with meshes………………………………………………..34
Fig.3.5 Tonyplot structure file of HD-DMG SOITFET……………………………………………………………...34
Fig.3.6 Tonyplot structure file of HD-DMG SOITFET with meshes………………………………………………..35

Fig 4.1 cross sectional view of SD-DMG SOI TFET……………………………………………………………...37
Fig..4.2 Band diagram along horizontal cutline for SD-DMG-SOI TFET
(φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{aux}………………....38
Fig 4.3 Band diagram along horizontal cutline for SD-DMG SOI TFET
(φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{aux}………………...39
Fig.4.4 transfer characteristics for SD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm)
with V_{DS}=1V for different φ_{aux}………………………………………………………………………………..39
Fig.4.5 Band diagram along horizontal cutline for SD-DMG SOI TFET
(φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{tunn}………………...40
Fig.4.6 Band diagram along horizontal cutline for SD-DMG SOI TFET
(φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{tunn}………………..41
Fig.4.7 transfer characteristics for SD-DMG SOI TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm)
with V_{DS}=1V for different φ_{tunn}……………………………………………………………………………......41
Fig.4.8 transfer characteristics for SD- DMG SOI TFET (φ_{aux}=4.4eV, φ_{tunn}=4.0eV) with V_{DS}=1V
for different L_{tunn}……………………………………………………………………………………………......42
Fig.4.9 Transfer characteristics of the SD-DMG-SOITFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV,
L_{tunn} = 20 nm, L_{aux} = 30 nm and V_{DS} = 1.0 V) and SMG-SOITFET
(φ_m = 4.0 eV, φ_m = 4.4 eV, L_g = 50 nm, and V_{DS} = 1.0 V)………………………………………………………….43
Fig.4.10 Output characteristics of the SD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV,
L_{tunn} = 20 nm, L_{aux} = 30 nm, and V_{GS} = 1.8 V) and SD-SMG SOI TFET
(φ_m = 4.0 eV, φ_m = 4.4 eV, L_g = 50 nm, and V_{DS} = 1.8 V)………………………………………………………...43
Fig.4.11. V_T at different channel length for SD- DMG SOI TFET
(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV) and SMG-SOITFET(φ_m =4.0 eV,4.4eV)……………………………………...…45
Fig.4.12. Parasitic capacitances C_{gs} and C_{gd} as a function of V_{GS} in
SD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm)……………………….......46
Fig 4.13. Transconductance as a function of V_{GS} in SD-DMG SOI TFET

(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm)……46

Fig.5.1.Cross sectional view of HD-DMG SOI TFET……49
Fig.5.2 Band diagram along horizontal cutline for HD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{aux}……50
Fig.5.3 Band diagram along horizontal cutline for HD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{aux}……51
Fig.5.4 transfer characteristics for HD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) with V_{DS}=1V for different φ_{aux}……51
Fig.5.5 Band diagram along horizontal cutline for HD-DMG SOI TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{tunn}……52
Fig.5.6 Band diagram along horizontal cutline for HD-DMG-SOITFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{aux}……52
Fig.5.7 transfer characteristics for HD-DMG-TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) with V_{DS}=1V for different φ_{tunn}……53
Fig.5.8 transfer characteristics for HD-DMG-SOITFET (φ_{aux}=4.4eV, φ_{tunn}=4.0eV) with V_{DS}=1V for different L_{tunn}……54
Fig 5.9 Transfer characteristics of the HD-DMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and V_{DS} = 1.0 V) and HD-SMG-TFET (φ_m = 4.0 eV, φ_m = 4.4 eV, L_g = 50 nm and V_{DS} = 1.0 V)……54
Fig 5.10 Output characteristics of the HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and V_{GS} = 1.8 V) and HD-SMG-TFET (φ_m = 4.0 eV, φ_m = 4.3 eV, L_g = 50 nm and V_{DS} = 1.8 V)……55
Fig. 5.11. V_T at different channel length for HD- DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV) and HD-SMG-SOI TFET(φ_m =4.0 eV,4.4eV)……57
Fig5.12. Parasitic capacitances C_{gs} and C_{gd} as a function of V_{GS} in HD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm)……58
Fig 5.13. Transconductance as a function of V_{GS} in HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm)……58
Fig 5.14. Transfer characteristics of HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9) , SD-DMG SOI TFET (φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9) at V_{DS} =1V……59
Fig 5.15 Output characteristics of HDDMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SD-DMG-TFET(φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9) at V_{GS}=1.8V……60
Fig 5.16 DIBL for HD-DMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SD-DMG-TFET(φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9) V_{DS}=0.1V and 1V……60
Fig 5.17. V_T at different channel length for HD-DMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SD-DMG-TFET (φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9)……61
Fig 5.18. Cgs and Cgd for HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SD-DMG-TFET(φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9)……61
Fig 5.19. Tranconductance against varying gate-to-source voltage in for HD-DMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SD-DMG-TFET (φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9)……62

LIST OF TABLES

Table No Page No

4.1 DEVICE PARAMETERS TAKEN FOR SIMULATION (SD-DMG SOITFET)…………37

4.2 DIBL for 3 types of Single Dielectric Tunnel FET………………………………………....44

5.1 DIBL for 3 types of Hetero Dielectric Tunnel FET…………………………………………...56

LIST OF ACRONYMS

BOX:	Buried Oxide
CMOS:	Complementary Metal Oxide Semiconductor
DIBL:	Drain Induced Barrier Lowering
HCE:	Hot Carrier Effect
ITRS:	International Technology Roadmap for Semiconductor
MOSFET:	Metal Oxide Semiconductor Field Effect Transistor
NWFET:	Nano Wire Field Effect Transistor
SCE:	Short Channel Effect
SOI:	Silicon-on-Insulator
TCAD:	Technology Computer-Aided-Design
SD-DMG:	Single Dielectric Dual Material Gate
SD-SMG:	Single Dielectric Single Material Gate
HD-DMG:	Hetero Dielectric Dual Material Gate
HD-SMG:	Hetero Dielectric Single Material Gate
TFET:	Tunnel Field Effect Transistor
VLSI :	Very Large Scale Integration

Chapter 1

INTRODUCTION

1.1 SEMICONDUCTOR TECHNOLOGY SCALING : A HISTORICAL OVERVIEW

Semiconductor electronics have revolutionized our life by creating a world where billions of people connect to each other in each and every second of a day. Electronics have conquered our life to an extent in which everything around us is influenced and enhanced by the semiconductor technology. In the present day scenario, each and every moment of human life is engulfed by outcomes of advancements in semiconductor technology like social media, digital music, photography ,computing systems which process information with the speed of light.

Microchip revolution started by the invention of Germanium point contact transistor by John Bardeen, Walter Brattain and William Schockley at Bell Laboratories in 1947. But the basic principle of field effect transistor was put forth by Julius Edgar Lilienfeld in the year 1925 though it came into commercial existence many years later[1]. The first silicon transistor which was commercially produced was developed by Texas Instruments in the beginning of 1950s. 1958 saw the invention of first IC by Jack Kilby[2]. But the first commercial IC which was a flipflop was developed by Robert Noyce in late 1950s[3]

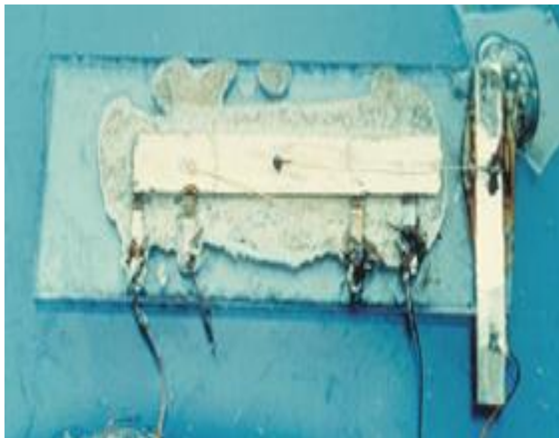

Fig. 1.1 First IC developed by Jack Kilby at Texas Instruments[2]

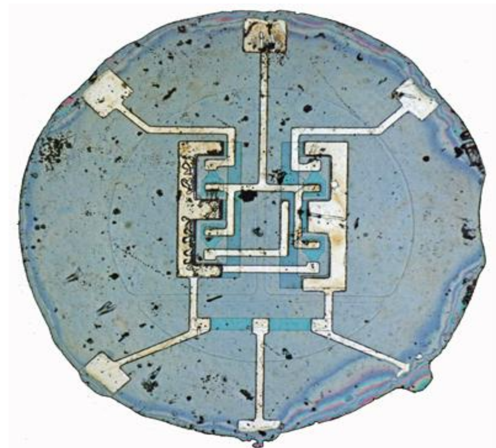

Fig. 1.2 First commercial IC developed by Robert Noyce at Fairchild semiconductor corp[3]

In 1962 first NPN transistor came into existence and then happened the invention of first microprocessor by Intel, INTEL 4004. During the following years as technology got scaled down, more complex processors like INTEL 8080, 8086, 8088, Motorola 68000 came out in the industry. Intel Pentium series got introduced in 1999-2000 which uses VLSI and ULSI technologies. In the present day , the technology had scaled down to 14nm technology and thereby the packing density is approaching to its saturation limit.

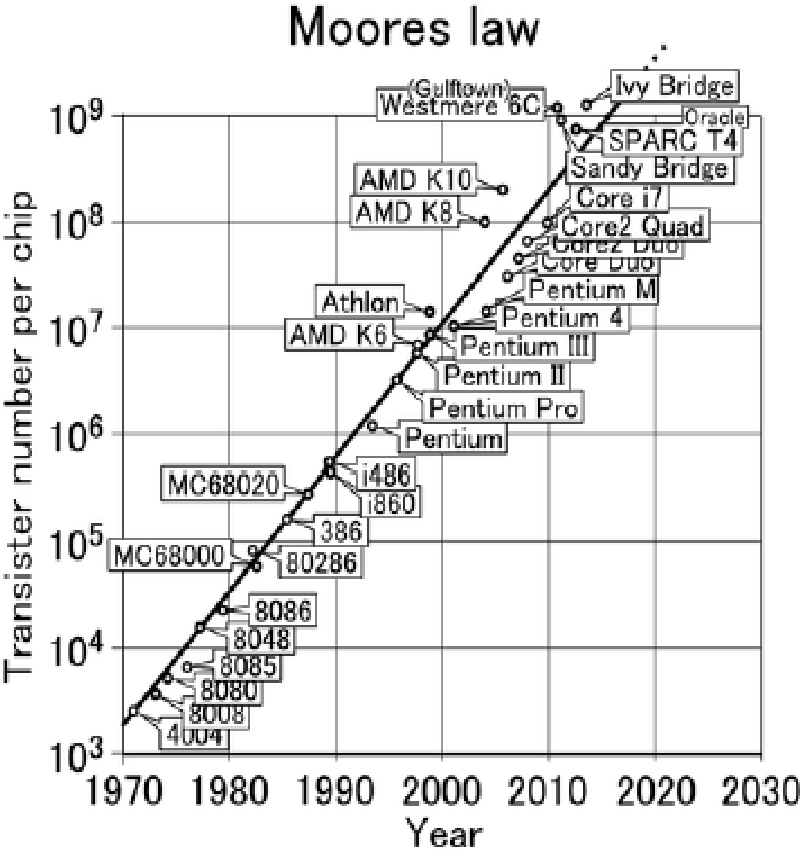

Fig.1.3 Transistor integration on chip displaying Moore’s Law[4]

Hence over the last six decades, scaling down of MOSFETs in size is continually been done so as to accommodate more devices in a given area of the chip. According to Moore’s law “the number of transistors on integrated circuits doubles approximately every 2 years”, whose prediction proves to be true and helps to set targets for research and development of semiconductor devices[4].

The International Technology Roadmap for Semiconductors (ITRS) is used to identify the obstacles and shortcomings so that industries and research communities can work effectively to overcome these shortfalls and helps in building semiconductors of future generation. Key findings as well as predictions of ITRS(2013) include , (i) combination of 3D architecture of the device as well as devices with low power would dominate in the new world of scaling which is coined in short as "3D Power Scaling." by stacking transistors in multiple layers ,increasing number of transistors per unit area can be accomplished.(ii) Emergence of carbon nanotubes, graphene combinations which offer ballistic conductors may be witnessed in the next decade. (iii) CMOS platform with extended functionality by heterogeneous integration of novel technologies and inventing devices with new processing paradigms can give new opportunities to semiconductor products of future era[5]

14 nm technology node according to ITRS is projected to have been dominating semiconductor companies by 2014. Significant advantages with regards to performance is being delivered by the 22nm Intel microarchitecture. The latest Intel® Core™ i7 processor uses 22nm technology, has around 1.4 billion transistors in a chip area of 160mm^2 which attains a clock speed of 3.4GHz

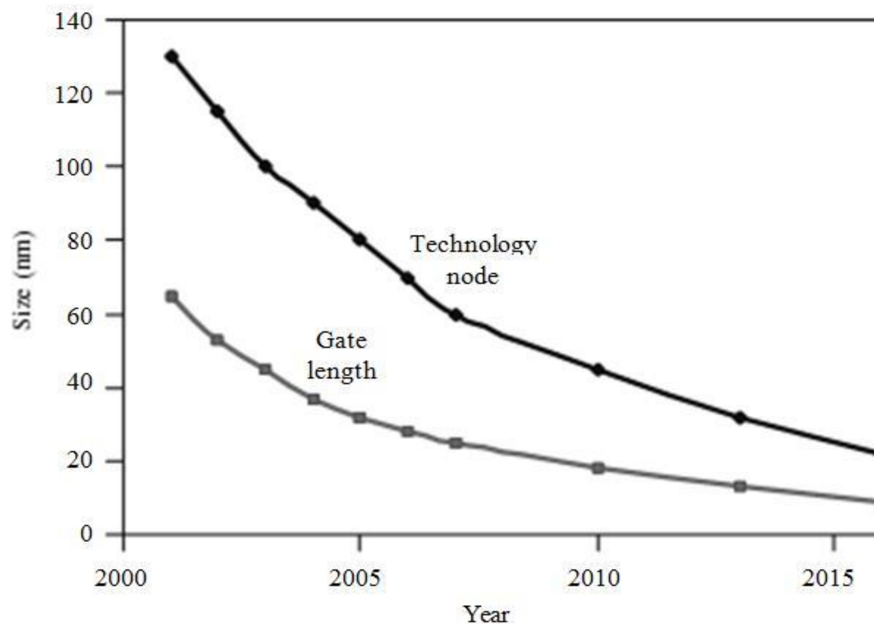

Fig. 1.4 Reduction in size of the technology over the years (Courtesy:ITRS 2005)

1.2 TYPES OF SCALING

1.2.1 Full Scaling (Constant Field Scaling)

In this type of scaling, both the horizontal and vertical dimensions are scaled down by 1/S where S is scaling factor. As the electric field which is the ratio between voltage and distance need to be constant, all the voltages also need to be scaled down by 1/S .In this type of scaling the threshold voltage is also scaled down by 1/S. Hence this scaling results in reduction of current which in turn reduce power. But power density remains constant as there is an increase in the number of transistors per unit area.

1.2.2 Constant-Voltage Scaling

In this method both horizontal and vertical device dimensions are scaled by S, but all the operating voltages are constant and thus their would be an increase in the electric fields in the device Here threshold voltages would be constant and the power per transistor increases by S. So power density per unit area will increase by S^3. Hence constant-voltage-scaling (CVS) becomes highly impractical. Also increased level of doping required for preventing channel punch through makes this type of scaling mostly impractical.

1.2.3 General Scaling

In general scaling, device dimensions will be scaled by a factor of S and the voltages will be scaled by another factor of U. The speed of the circuit can be improved by general scaling technique These type of devices would be energy efficient as well as reliable.

Hence constant advances in manufacturing techniques (especially lithography) had caused a constant reduction in the size of the transistor. Logic scaling had changed from a mostly lithography-based transistor shrink (easy scaling), to a performance enhanced era where novel materials and device structures need to be developed at a rapid pace. So the upcoming candidates in the future years which are under focus are FinFETs and high mobility FinFETs(14nm -10nm),next generation FinFETs with high mobility(10nm-7nm), gate all around FinFETs(10nm-7nm), tunnel FET(beyond 7nm), graphene FET(beyond 5nm)[6].

So the technology advancements witnessed by todays world have resulted in efficient monolithic ICs with novel transistors as switching elements and this had resulted in ICs that are considerably faster and highly complex to handle multiple functions.

1.3 POWER SHORTAGE IN THE ELECTRONIC INDUSTRY

Over the past four decades, there has been an increasing trend in the power consumption of lead microprocessors. In 1974, NMOS was preferred to PMOS due to its advantages like speed and area. But due to lower noise margins and static power consumption(DC) of NMOS technology, it was no longer used in the industry from 1980s. CMOS technology exhibits low intrinsic power dissipation and superior scaling characteristics and hence dominated IC industry in 1980s. But the rate at which chip area grows is much smaller as compared to the rate at which the number of transistors as well as power density grows. Hence the temperature of microprocessors increases as a result of increased power consumption. These temperature may even exceed 120^0C these days. As the temperature increases to higher levels, there would be an increase in leakage power which in turn increases the total power consumption. This can even cause thermal runaway in extreme situations

$$\text{Static power consumption} = I_{LEAK} * \text{Supply Voltage} \quad (1.1)$$

where I_{LEAK} is the sum of the leakage currents of MOSFET in OFF state.

$$\text{Dynamic power consumption} = f * C_L * (\text{Supply Voltage})^2 \quad (1.2)$$

where f is the frequency, C_L is the load capacitance.

It is seen that if supply voltage is not scaled down, there will be an increase in power density. Increase in power thus results in reduced battery life, more heat production and proves to be economically and environmentally less friendly[7]. So there is a significant challenge posed due to power consumption in designing IC systems.

1.4 LIMITATIONS DUE TO SCALING OF CONVENTIONAL MOSFETs

Various setbacks posed by scaling conventional MOSFETs are

1.4.1 Channel Length Modulation

When the MOSFET is scaled down to lower dimensions, inverted channel shortens as drain bias is increased thus giving rise to channel length modulation which in effect increases drain current for a MOSFET which operates in saturation as well as reduces output resistance of MOSFETs. The shortening of channel region happens due to extension of the non-inverted region towards source as drain voltage is made high. Hence reduction of output resistance happens due to decrease in length thus causing an increased drain current.

1.4.2 Short Channel Effects (SCEs)

A semiconductor device is said to be a short channel device when its channel length becomes comparable to drain depth and source depth as well as depletion width. Major SCEs are

1.4.2.1 Velocity Saturation of Carriers

When the MOSFETs are scaled down to very low dimensions, the charge carriers experience very strong electric fields due to which their velocity reaches a maximum and saturates thereby, there would be no longer increase in carrier velocity when applied electric field is increased further. This phenomenon provides limitation for carrier movement in semiconductor and is hence called velocity saturation effect which is one of the major SCE.

1.4.2.2 Drain Induced Barrier Lowering (DIBL) and Punch Through

In small channel MOSFETs, at comparatively high drain voltages, threshold voltages reduces unlike long channel devices where threshold voltage is independent of drain voltage.

This phenomenon happens in short channel MOSFETs as drain voltage is increased, the depletion region of the drain-body junction extends under gate and barrier lowering of electrons in channel takes place and threshold voltages reduces. Hence named the effect as Drain Induced Barrier Lowering(DIBL). When the drain as well as source depletion regions combine together, the gate voltage will not be able to control the current flow and this condition is coined as punchthrough.

1.4.2.3 Surface Scattering

In small channel dimensions, vertical component of electric field accelerate electrons towards the surface which undergo collision and faces difficulty as they move through the channel. This limits the mobility of electrons and the phenomenon thus named surface scattering.

1.4.2.4 Impact Ionization

Due to the presence of very longitudinal electric field in short channel MOSFETs, electrons have higher velocity, which impacts silicon atoms and ionize them and can create electron hole pair. This phenomenon worsens when electrons due to high fields, travel to substrate while trying to escape from the drain region and hence can affect the adjacent devices on the chip.

1.4.2.5 Hot-Carrier Injection

A mechanism that can change the switching characteristics permanently for a transistor, where an electron as well as a hole can gain high kinetic energy and enter into the dielectric of the MOSFET.. This makes semiconductor devices less reliable.

1.4.3 Narrow Channel Effect

In small channel width devices, depletion region in the channel region is larger compared to what is assumed. This takes place due to fringing fields. Hence due to narrow channel, threshold voltage of the device increases.

1.4.4 Subthreshold Conduction

Subthreshold conduction is the drain current between source and drain in the subthreshold region of MOSFET. As MOSFETs are scaled down to nanometer ranges, voltages also gets scaled down and subthreshold leakage increases and may led to 50% of total power consumed.

Hence conventional MOSFETs cannot be looked upon as the device of future semiconductor world as it can be optimized to a certain limit only. The subthreshold swing of conventional MOSFETs have a minimum limit of 60mV/decade. MOSFETs have I_{ON} to I_{OFF} ratio in the order of 10^3 to 10^4 .So device engineers go forward with nonconventional devices with subthreshold swing less than 60mV/decade and higher I_{ON} with very negligible I_{OFF} trying to make them behave as ideal switch.

1.5 REQUIREMENTS FOR FUTURE GENERATION TRANSISTORS

Nanoelectronics have set foot to develop environment friendly FET in which power consumption is very negligible. For this to be materialized we focus on lowering supply voltage and having better thermal management leading to reduced power IC performance. The ability of transistors to switch between ON and OFF states is quantified by the term subthreshold slope which is the amount of gate voltage to increase drain current by one decade.

Subthreshold Swing(S.S) can be formulated as below:

$$S,S = \ln(10) * \left(k * \frac{T}{q}\right) * \left(1 + \left(\frac{C_d}{C_{ox}}\right)\right) \tag{1.3}$$

where $'k'$ is the Boltzmann's constant, $'T'$ is temperature, $'q'$ is elementary charge ,C_d is capacitance of depletion layer and C_{ox} is the capacitance of gate oxide.

In the future CMOS era, transistors with the feature of steeper subthreshold swing becomes a necessity. These devices need to overcome 'kT/q' limit so as to have very steep subthreshold

slope and hence would have different manner of operation compared to normal MOSFET. Hence these devices need to give higher ON current, very low leakage currents(in nA of fA ranges) and thus reduce leakage power devices which were researched.

1.5.1 NEMFETs (Nano Electro Mechanical FETs)

These type of transistors have gate electrode which is a mechanical beam moving up and down such that it is in contact with the gate oxide during OFF state and away from gate oxide during ON state. They are accumulation mode devices exhibiting subthreshold swing less than 60mV per decade and hence having an enhanced I_{ON} to I_{OFF} ratio. Speed along with integration density and manufacturability is a concern in case of NEMFETs[8].

1.5.2 Ferroelectric gate dielectric FET

These are devices where ferroelectric (materials having electrical polarization internally) gate dielectric gives rise to negative gate capacitance for the structure. Due to the negative gate oxide capacitance, the resultant expression of subthreshold swing (1.1) will give a value less than 60 mV/decade and hence results in a steeper subthreshold slope. But studies conducted on these type of MOSFETs revealed their impractical nature when it comes to scaling[9]

1.5.3 IMOS (Impact Ionization FETs)

This novel device is based on control of impact ionization by field effect of the transistor. To switch between ON and OFF states, IMOS makes use of modulation of the break down voltage of a p-i-n diode by using its gate voltage. IMOS has a structure which is a reverse biased p-i-n diode with gate electrode spanning over a part of the intrinsic region. The electric fields of these IMOS FETs influence the coefficients of impact ionization and produce steeper suthreshold slope of about 5mV per decade. But these devices cannot be looked upon as the device of future CMOS era due to its intense hot carrier effect and the high voltages needed for their operation compared to present day MOSFETs[10].

1.5.4 Feedback FETs (FBFETs)

A type of transistor which uses positive feedback mechanism to obtain very less subthreshold swing of the order of 2mV per decade and higher I_{ON} to I_{OFF} ratio. This device is a forward biased p-i-n diode with gate over a partial area of intrinsic region. The positive feedback mechanism associated with this device causes lowering of threshold voltage and the device switches abruptly between two states. These type of FETs requires conditioning for the charges to be stored in gate-sidewall spacers for the formation of built in barrier potentials.

1.5.5 Tunnel FETs (TFETs)

The most popular among all other steep slope devices, TFETs operates with the principle of band to band tunneling. The structure is a gated p-i-n diode which is reverse biased with gate spanning over whole intrinsic region. The overlap of valence band with conduction band as well as the barrier with at the tunnel junction decides ON as well as OFF states in tunnel FETs. These devices have very low leakage current during OFF state and gives very steep subthreshold slope as well as high I_{ON} to I_{OFF} ratio. Also they have the added advantage of very negligible SCEs.

1.6 INTRODUCTION TO TUNNEL FETS

The tunnel field-effect transistor or tunnel FET is a device which is based on band to band tunneling of electrons and in principle, switch between on as well as off states at low voltages than the operating voltage of metal oxide semiconductor field effect transistor (MOSFET). It is therefore expected to reduce the consumption of power by electronic devices. This device with a new architecture poses an interesting phenomenon of quantum barrier tunneling of electrons at the tunnel junction which provides the transport mechanism of carriers[11]. But the lesser amount of current through tunnel FET as compared to MOSFET demands more research to improve on current to make it suitable for practical applications. This type of FET is capable of providing steeper subthreshold slope than conventional MOSFET (which is limited to 60mV per decade) thus making it a promising candidate of future semiconductor era.

1.6.1 Structure And Operation

Tunnel FET consists of p-i-n diode which is reverse biased by applying suitable voltage at the drain. When considerable voltage is applied at the gate terminal, device switches on as tunneling starts at the source-intrinsic body junction which is thus the cause for on current. Tunnel FET can be of two types namely n-type where source-channel-drain follows p+-i-n+ doping profile and p-type where source-channel-drain follows n+-i-p+ doping profile respectively. Though 'i' represents intrinsic region for channel, usually lightly p or n doped (around 10^{15} /cm^{-3}) channel region is considered. Fig1.6 below shows an n-type SOI Tunnel FET where source, drain and channel lies over buried oxide(SiO_2) present on top of silicon substrate. For n-type devices operation, both gate and drain are supplied with positive potential as compared to source and for p-type tunnel FETs, negative voltages are supplied at the gate and drain terminals.

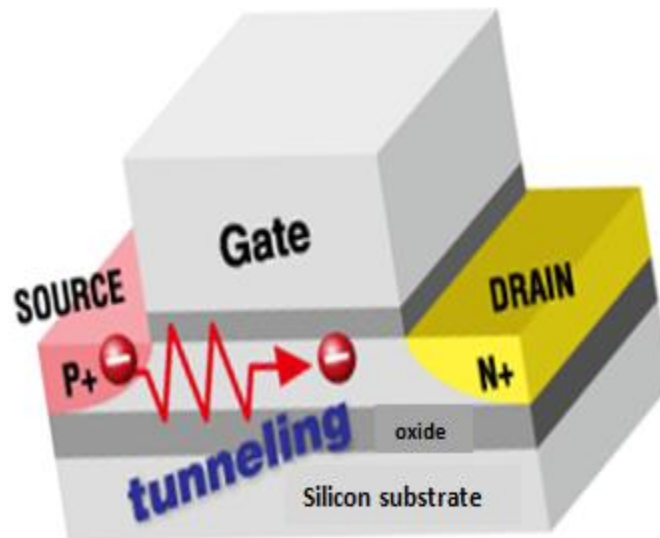

Fig.1.5 Device structure of simple SOI Tunnel FET(Courtesy:green nanoelectronics centre).

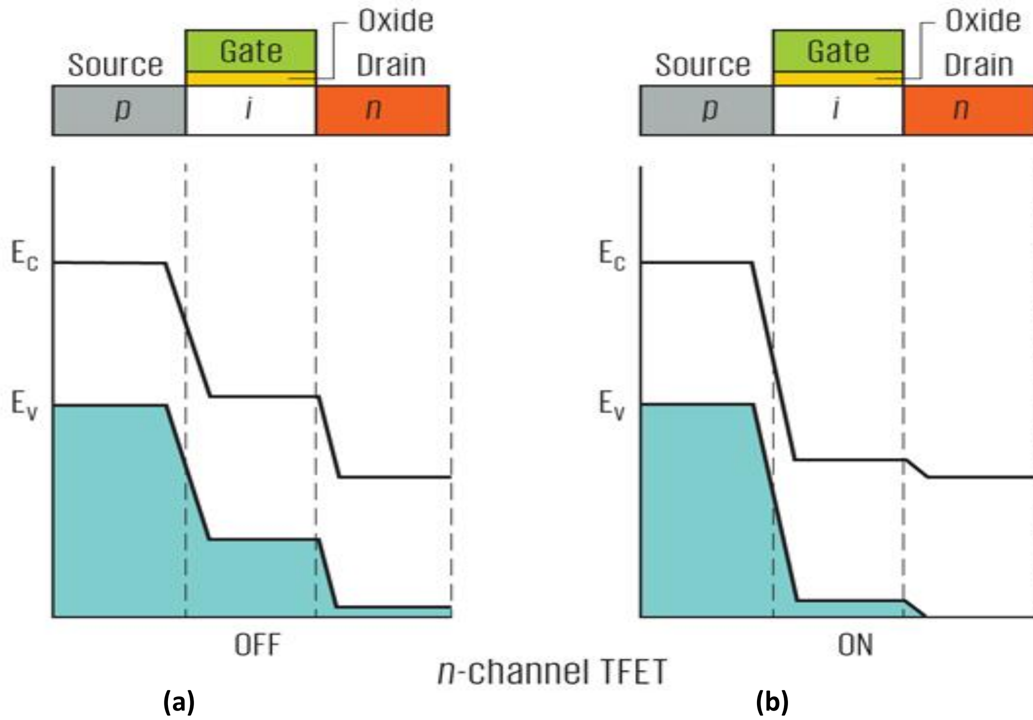

Fig.1.6 energy band diagram along a horizontal cut on the n-type tunnel FET in OFF state and ON state[12].

The tunnel FET is said to be in OFF state when the reverse biased p-i-n diode is supplied with gate voltage lesser than the corresponding threshold voltage where there will be no overlap of energy bands and energy barrier width in the tunnel junction is higher as shown in above fig1.6. Hence there will be no tunneling of electrons across the tunnel junction and the current which arises in this condition would be just leakage current of the order of about 10^{-17} A/µm.But as the gate voltage level is increased to a suitably high value, both the conduction band as well as valence band of the intrinsic region moves down and aligns almost with that of drain region. Hence overlap of valence band of source region with the conduction band of intrinsic region happens and tunnel barrier width narrows as shown in Fig1.7. This leads to electrons tunneling from source region to intrinsic region which in turn becomes the transport mechanism involved[12]. The tunneling gives rise to on current of the order of about 10^{-6} A/ µm to 10^{-4} A/ µm.

1.6.2 Ambipolar Nature Of Tunnel FETs

The term 'ambipolar' means that conduction happens as gate voltage increases in the positive direction(positive values) as well as negative direction(negative values). Tunnel FETs exhibit ambipolar nature which is a dominant phenomenon of symmetric structures where source as well as drain is doped to similar levels as well as the gate dielectric consists of the single material[13] For an n-type Tunnel FET, as gate voltage increases to more positive values, tunneling happens at the source channel junction and as gate voltage increases to more negative values, tunneling happens at the drain channel junction thus causing current to flow in both the cases. Fig.1.8 shows this phenomenon where significant drain current flows during higher positive and negative values of gate voltages.

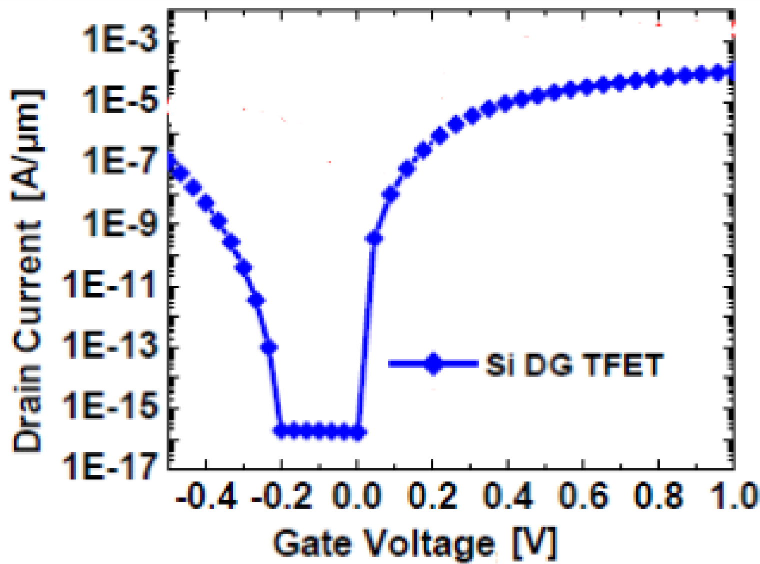

Fig.1.7 Transfer characteristics of Double Gate(DG) Tunnel FET [14]

Ambipolar characteristics can be reduced in tunnel FETs by introducing asymmetric architectures with unequal source and drain doping, including intrinsic region near the drain which is operated under different gate voltage and having different dielectrics (high k dielectrics like HfO_2 near tunnel junction and low k dielectric like SiO_2 near drain-channel junction).

1.6.3 Band To Band Tunneling Mechanism

In this mechanism, electrons travel from the valence band of the semiconductor to the conduction by tunneling across a potential barrier. This band to band tunneling is of two types: direct band to band tunneling and indirect band to band tunneling. In direct band to band tunneling, electrons travel across valence band and conduction band without absorbing or emitting phonon. Hence there is no change in momentum for the particle undergoing tunneling. This type of tunneling takes place in semiconductors like GaAs, InAs etc. Whereas in indirect band to band tunneling, electrons undergo a change in momentum as they travel from valence band to conduction band due to the absorption or emission of phonon. Indirect band to band tunneling takes place in semiconductors like silicon, germanium etc.

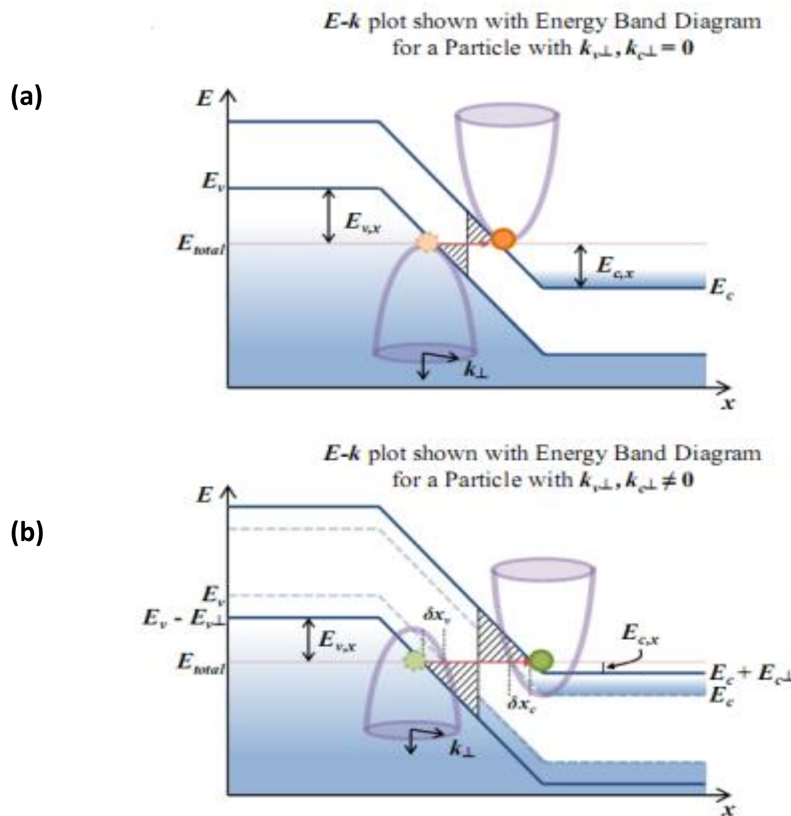

Fig.1.8 Band diagram of a p-n junction with electron undergoing (a) direct band to band tunneling (b) indirect band to band tunneling(Courtesy: wikipedia).

The involvement of phonon in indirect band to band tunneling causes change in perpendicular momentum, hence after tunneling,total energy and perpendicular momentum should be conserved. It can be seen in fig1.9 that non zero perpendicular momentum can cause an increase in tunneling path.

Wentzel–Kramers–Brillouin(WKB) approximation which is a method used for finding the approximate solutions for linear partial differential equations having spatially varying coefficients, is used to calculate band to band transmission coefficient which is given by

$$T_t \approx \exp(-2 \int_{-x1}^{x2} |k(x)|\, dx) \quad (1.4)$$

Here $k(x)$ represents the quantum wave vector of the tunneling electron inside the triangular potential barrier which spans from $-x1$ to $x2$. Here tunneling is assumed to take place in x direction. The potential energy at $-x1$ is E_g(energy band gap) and that at $x2$ is zero. The wave vector inside the triangular tunneling barrier is given by

$$k(x) = \sqrt{\frac{2*m^*}{\left(\frac{\mathrm{h}}{2\pi}\right)^2}(\mathrm{P.E-E})} \quad (1.5)$$

where P.E is the potential energy,h is the Planck's constant, E is the energy of incoming electron and m^* is its tunneling mass. P.E can be equated as Eg/2−qFx,

$$P.E = \left(\frac{E_g}{2}\right) - (q * F * x) \quad (1.6)$$

where F represents electric field.

Using (1.3) and (1.4) in (1.2), a general expression for band to band transmission is obtained, given by

$$T_t \approx \exp\left(\frac{-4*\sqrt{2*m^*}\ E_g^{\frac{3}{2}}}{3*q*\left(\frac{h}{2\pi}\right)*F}\right) \quad (1.7)$$

Considering triangular energy barrier having a height of $E_g + \Delta\emptyset$ and width λ ,(1.5) gives band to band current,

$$I_{BTB} \propto T_t \approx \exp(-\frac{4*\lambda*\sqrt{2*m^*}E_g^{\frac{3}{2}}}{(3*(\frac{h}{2\pi})*(E_g+\Delta\emptyset))}) \quad (1.8)$$

Hence the equation(1.6) gives a quantitative idea of band to band tunneling current flowing through tunnel FET.

1.6.4 Features And Merits Of Tunnel FETs

Tunnel FETs have many features which makes them a better transistor for future. The main difference of tunnel FETs as compared to conventional MOSFETs is the transport mechanism of charge carriers in the two devices. As band to band tunneling is the inherent mechanism of former device, drift and diffusion of charge carriers is the transport mechanism of latter device. So tunnel FETs have weaker temperature dependence as tunneling doesn't depend on temperature. Hence, it has the potential for a subthreshold swing lesser to kT/q limit(60mV/decade) at temperature of 300K. In tunnel FETs ,gate controls the tunnel barrier width and hence leakage current is very negligible because there is only feeble current when tunnel barrier width is high. This adds to its advantages as the static power dissipation would very less as compared to conventional MOSFETs.

Due to the steeper subthreshold slope of tunnel FET, supply voltage needed can be lower which in turn reduces static as well as dynamic power dissipation. Also tunnel FETs have very high on current to off current ratio. This property along with steeper subthreshold slope makes them perform close to ideal switch which can switch between ON and OFF states with small variation of gate voltage at the threshold potential.

Short channel effects are not dominant in tunnel FETs unlike MOSFETs and hence scaling of tunnel FETs doesn't pose serious challenges. Thus tunnel FETs pose to be a promising candidate for ultra low power era.

1.7 THESIS ORGANISATION

Chapter 2 briefs about the various architectures of tunnel FETs and various works done in the past pertaining to tunnel FETs

Chapter 3.summarizes the Atlas device simulator and its various features. It also briefs about relevant models used in current simulation work.

Chapter 4 explains the performance analysis of Single Dielectric Dual Material Gate SOI Tunnel FET.

Chapter 5 explains the performance analysis of Hetero Dielectric Dual Material Gate SOI Tunnel FET and draws out comparison of single dielectric structure with hetero dielectric structure.

Chapter 6. concludes the thesis and mentions the scope of future work.

Chapter 2

LITERATURE REVIEW

Tunnel FETs (TFET) ,a new transistor design has been gaining momentum in the last few years. TFETs are a promising device which is based on Band-to-Band Tunneling (BTBT) offering very low leakage current and obtaining a subthreshold slope much lesser than that of conventional MOSFET. Studies have been focused to obtain superior characteristics by employing Double Gate Technology as well as high K dielectric gate oxide in tunnel FETs[15]. Common configurations of Tunnel FETs studied in the past are discussed below

2.1 DOUBLE GATE TUNNEL FET

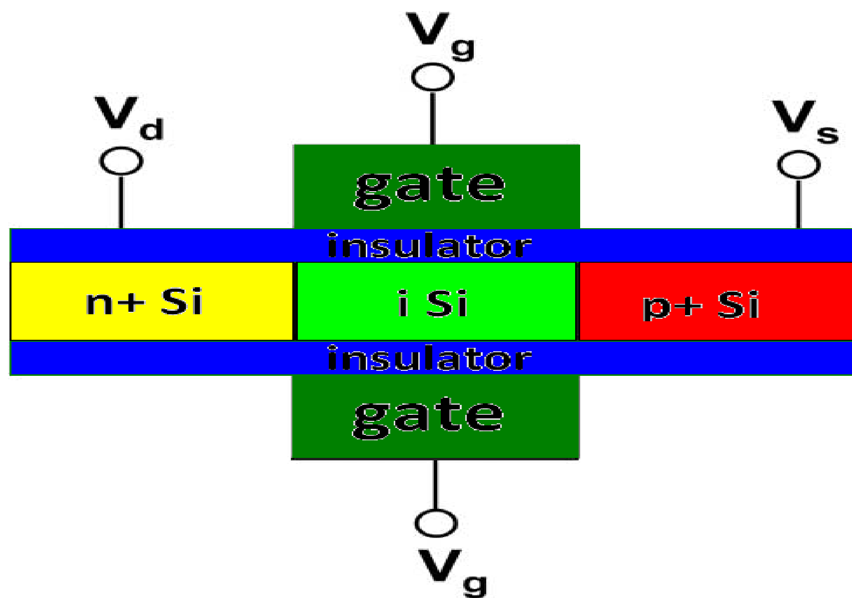

Fig2.1: Cross Sectional view of Double Gate Tunnel FET[16]

Double Gate Tunnel FETs are one of the most widely researched device due to the potential advantages it provides like very high I_{ON} to I_{OFF} ratio and extremely low subthreshold swing. These devices have two gates as shown in fig.2.1 which influences the energy bands at the tunnel junction thereby initiating band to band tunneling. Double Gate Tunnel FETs are highly stable in RF range-off and has high cut-off as well as maimum oscillating frequency. By using High K

dielectric as the gate oxide, further improvement in on current can be obtained and optimizing this device with most suitable device dimensions, work functions of the gate electrodes and doping profiles of silicon region, leads to superior characteristics which makes capable enough for replacing MOSFET technology.

2.2 JUNCTIONLESS TUNNEL FIELD EFFECT TRANSISTOR

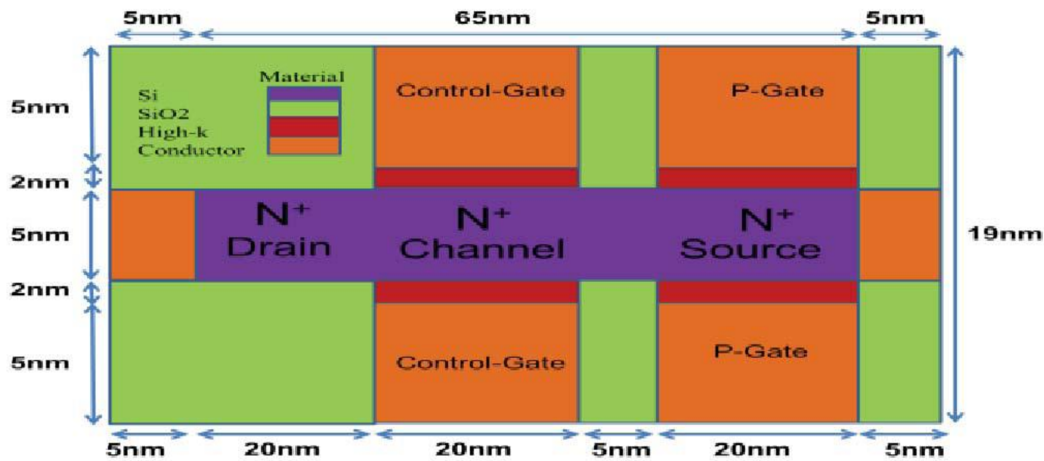

Fig 2.2 : Schematic view of the JL-TFET.[30]

These devices are peculiar due to the lack of steep doping profile unlike other types of Tunnel FETs. Different types of JL-TFETs are under study such as SOI JL-TFET, bulk planar JLTFET and Nanowire junctionless TFETs. Though it doesn't have any doping gradient in the silicon body, it has very high uniform doping profile. These devices have very negligible short channel effects[30]. This type of TFET has higher I_{ON} compared to other type of conventional TFET. In these TFETs there are two gate of which one is only the controlling gate and other is fixed gate. By suitable work function being set for fixed gate, source behaves as p type and then variation of voltage on controlling gate is done so as to switch the device ON and OFF. Hence these type of devices also prove to be a potential candidate to replace conventional MOSFETs.

2.3 DUAL MATERIAL GATE TUNNEL FIELD EFFECT TRANSISTORS

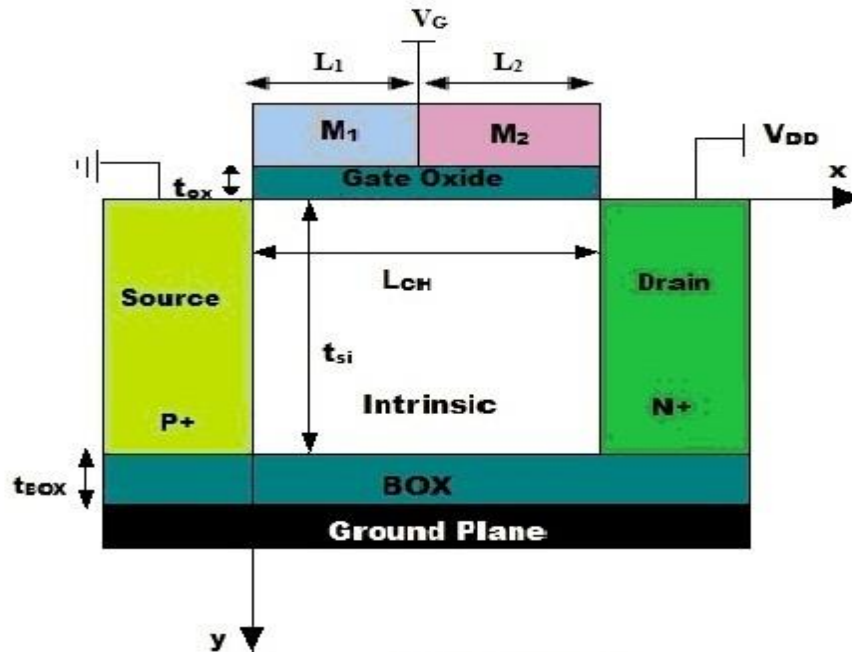

Fig.2.3. Schematic structure of a DMG TFET[22]

Fig.2.3 gives the structure of Dual Material Gate Tunnel FET which has the structure same as conventional Tunnel FET except for gate electrode consisting of material with two different work functions. Varying the work functions of these materials shows variation of electrical parameters and optimization could be done. These type of SOI Tunnel FETs have the advantage of easier fabrication compared to DGTFET due to easier fabrication because of the usage of SOI substrate. DMG Tunnel FET with double gate structure have also been widely studied. These type of Tunnel FETs are also capable of producing very high I_{ON}-I_{OFF} ratio and lower subthreshold slope.

2.4 PAST WORK

Various researches have been done in obtaining superior characteristics for these type of device by using high K dielectric with a double gate structure. Kathy Boucart *et al*, in the work" Double-Gate Tunnel FET With High-K Gate Dielectric", had presented an elaborate discussion on the features of DGTFET as well had optimized its performance by choosing suitable device parameters along with high K dielectric[16]. J. Wan *et al*, had researched the significance in

introducing various architectures for tunnel FETs by using high K dielectric along with low K dielectric so as to suppress ambipolar leakage, in his work “Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling” in 2011[17].

A recently published work by Sneh Saurabh and M. Jagadesh Kumar,named “Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor”, have demonstrated the attributes of Dua Material Gate Double Gate Tunnel FET (DMGDGTFET) and the change in its transfer characteristics due to variations of work functions of the gate materials. Also this work had revealed the superiority of Dual Material Gate device over Single Material Gate device.[18]. Similar works have been published demonstrating the comparisons on Single Material Gate, Dual Material Gate, Triple Material Gate Tunnal FETs by Ning Cui *et al* [19].

Characteristics of Hetero Dielectric Dual Gate Material Tunnel FET using Double Gate Technology has been researched in a work published where they have drawn comparisons among Dual Material Gate Single Dielectric structure, Dual Material Gate Hetero Dielectric structure and Single Material Gate Hetero Dielectric structure[20]. Threshold voltage extraction techniques for tunnel FETs have been done in a recent work[21]. Current to Tranconductance ratio method described in [21] have been a novel method to calculate threshold voltage of Tunnel FETs only. T.S.Arun Samuel *et al* in the work “Analytical Modeling and Simulation of Dual Material Gate Tunnel Field Effect Transistors”, have demonstrated as model for DMG SOI TFET which has shown to be appropriate as it was matching with the simulation results obtained[22].

Studies have been conducted on using Tunnel FETs in analog circuits as it is expected to give lesser power dissipation as well as lower operating voltage. This assumption was proved to be true by the work published by Ravindhiran Mukundrajan *et al* where simpler circuits like 2 input nand gate,2 input nor gate and complex circuits like Manchester carry chain circuits made of tunnel FETs exhibited much higher energy efficiency and lesser delay[23]. Also Radio Frequency Performance of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors was studied by In Man Kang *et al* and his work had revealed the superior RF characteristics of Hetero Dielectric structure compared to Single Dielectric structure[24]. [25],[26] gives an insight of the RF and Stability Performance of Double Gate Tunnel FET as well as linearity and analog

performance analysis of Double Gate Tunnel FET with effect of temperature and gate stack. An investigation into the performance of fully-depleted silicon-on-insulator (SOI), double-gate (DG) and cylindrical nanowire (CNW) FETs, with the aim of establishing optimization procedures and appropriate scaling rules towards their extreme miniaturization limits had been done in the paper by E. Gnani *et al* with the title “Design Considerations and Comparative Investigation of Ultra-Thin SOI, Double-Gate and Cylindrical Nanowire FETs”[27]. This work had concluded that CN FETs shows better short channel performance compared to other two structures. Also the performance improvement exhibited by Tunnel FETs with raised box at source,channel and drain was studied by B.Bhowmick *et al* in the year 2013.

Hence it is concluded from literature survey that Tunnel FET is a upcoming candidate for research and is looked upon as the efficient transistor of future

CHAPTER 3

SIMULATION METHODOLOGY

3.1 INTRODUCTION

Atlas provides general capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. Atlas is designed to be used with the VWF Interactive Tools. The VWF (Virtual Wafer Fabrication) Interactive Tools are DeckBuild, TonyPlot, DevEdit, MaskViews, and Optimizer. DeckBuild provides the environment for running Atlas command language. Various electrical characteristics which are produced as outputs as well as structure files created for the device can be visualized by TonyPlot. To create device structure and specify meshes used, interactive environment is provided by DevEdit. IC layout can be edited by using MaskViews. Optimization across various simulators can be provided by Optimizer. Athena is a process simulator which produces structures made by various processing steps. These structures can be used as inputs to Atlas. Atlas ultimately predicts various electrical characteristics pertaining to the device. These electrical characteristics can be used as input by by the Utmost device characterization and SPICE modeling software. These VWF Tools makes simulation closely linked to technology advancements and reflects the research happening experimentally. Hence these tools are very beneficial with regards to the upcoming semiconductor technology and in predicting all the features and characteristics of novel technology processes and devices.

Atlas is called a physically-based simulator for device as it can predict all the characteristics associated with a particular device with specified structure and voltage biases at the electrodes. These simulators divide whole of the device area with grids called 'meshes' with mesh points called 'nodes'. By applying differential equations which are derived from Maxwell's laws, current conduction and electrical parameters at each location through the structure is determined. Advantages of this type of physically based simulation are ,they provide a deep insight of the attributes of a device without experimentally creating the device, they

calculate very complex parameters with quickly, they helps us in estimating the trends in variation of the properties of the device according to varying bias conditions.

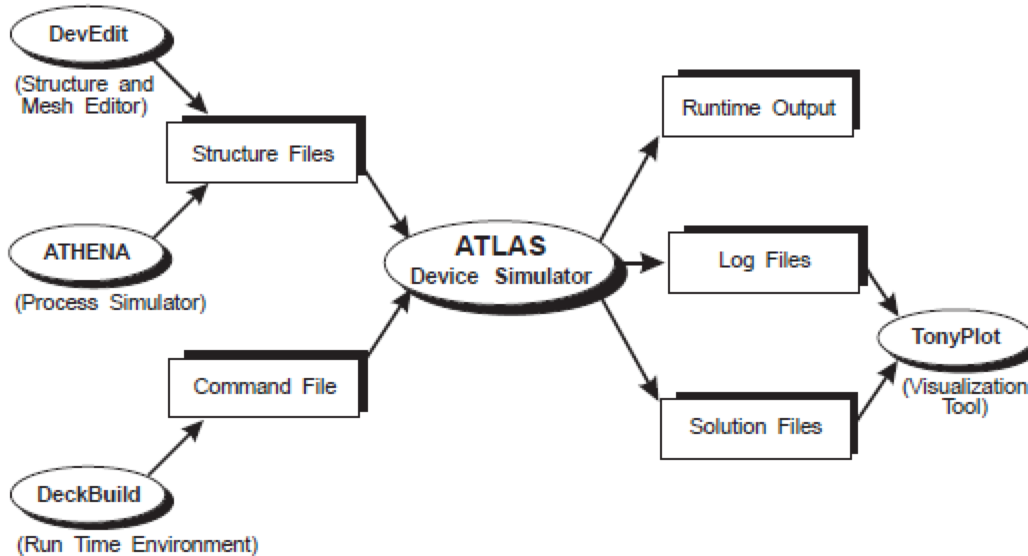

Fig3.1 Inputs and Outputs of Atlas device simulator[31].

Fig3.1. shows the information flowing through Atlas device simulator. The text file, which contains Atlas command language and structure file, which has the structure on which simulations has to be performed are the two input files to Atlas device simulator. Atlas has three types of output files: runtime output which gives the information being processed at every instant of execution of Atlas commands and simultaneously show the errors and warnings, log files which gives all the electrical characteristics which is specified in the Atlas command language and solution files which has the 2D or 3D data of the device parameters at each and every point in the device.

3.2 STEPS TO DEFINE A STRUCTURE

3.2.1. Load a structure from Athena

Atlas can be interfaced with Athena to load a structure defined and created by Athena. For this, a structure needs to be created in Athena and saved while Athena is active. For this , below command can be used.

`STRUCTURE OUTF= <structure name.str>` where *structure name* is the file which stores the device structure.

Then in Atlas simulator, above saved structure can be loaded by the following statement

```
MESH INF=<structure name.str>
```

3.2.2. Load a structure from DevEdit

A device structure created by DevEdit can be loaded into Atlas by interfacing Atlas with DevEdit. The syntax for this operation is as below.

```
MESH INF=<structure name.str>
```

Above command loads meshes, electrode locations, device dopings etc from DevEdit for the device loaded.

3.2.3. Using ATLAS Commands to define a structure.

To define a structure using ATLAS command language, a set of commands have to be used in a specified order which is as listed below.

The command language starts with initial mesh specification.

Mesh specification starts with a mesh mult statement which multiplies the spacing between the meshes by a factor (specified along with mesh.mult command) so that meshes can be finer or coarser according to the need.

Syntax:

```
MESH SPACE.MULT=<value>
```

This is followed by x.mesh and y.mesh statements

Syntax:

```
X.MESH LOC=<value1> SPAC =<value2>
Y.MESH LOC=<value3> spac =<value4>
```

where '*value1*' specifies in microns ,the location of vertical meshline and '*value2*' specifies the spacing between these vertical meshlines. Similarly '*value3*' specifies the location of horizontal meshlines and '*value4*', the spacing between them.

Subsequently the device structure is divided into various regions where each region is made of a particular material with a specific doping profile. The region can be specified as below,

Syntax:

`REGION NUMBER=<*value*> X.MIN=<*value1*> X.MAX=<*value2*> Y.MIN<*value3*> Y.MAX=<*value4*> MATERIAL=<*material1*>`

where '*value*' specifies the region number and '*material1*' is the material which forms the region (like SiO_2 ,Silicon etc).The region spans from '*value1*' to '*value2*' on the x-axis and '*value3*' to '*value4*' on y-axis of the 2D plane.

Then electrode is specified by the electrode statements with the syntax given below,

Syntax:

ELECTRODE NAME<*electrode1*> NUMBER=<*value*> X.MIN=<*value1*> X.MAX=<*value2*> Y.MIN<*value3*> Y.MAX=<*value4*>

where the electrode is named as '*electrode1*' which spans from x.min to x.max and y.min to y.max.

Doping statements have the syntax as

Syntax:

DOPING<*doping profile*> CONC =<*value*> <*doping type*> REGION=<*number*>

Doping profile can be uniform, gaussian etc with concentration and type of doping specified by '*value*' and '*doping type* ' respectively.

Contacts are specified by contact statements given by,

CONTACT NAME<*contact name*> WORKFUNCTION=<*value*> where '*value*' gives the work function of the contact with name '*contact name'*.

Work function of commonly used contacts like Aluminium, Tungsten, N.Polysilicon, P.Polysilicon etc can be specified by their name in the contact statement instead of specifying work function value. For example, the statement:

CONTACT NAME<f.gate> N.Polysilicon.

External inductors, capacitors and resistors can be specified by the following syntax.

CONTACT NAME=<*contact name*> RESISTANCE=<value1> CAPACITANCE=<value2> INDUCTANCE=<value3>

where ‘`value1`’,’ `value2`’and ‘`value3`’ are resistance value in ohms, capacitance value in farads and inductor value in henry respectively.

3.3 SPECIFYING MODELS TO BE USED

Generally MODELS statements are used to specify the physical models used in simulations with the exception of impact ionization which is specified in IMPACT statements. The MODELS are selected according to the physical phenomenon taking place inside the device under consideration. All the physical models used can be classified under 5 categories namely:

1. Carrier Statistics Models
2. Mobility Models
3. Recombination Models
4. Impact Ionization Models
5. Tunneling and Carrier Injection Models.

3.4 COMMON MODELS USED IN BRIEF

3.4.1 **Concentration-Dependent Low-Field Mobility Model**

This model is activated by specifying CONMOB in the MODELS statement. This model provides the data for low field mobilities of electrons and holes at 300K for silicon and gallium arsenide only.

3.4.2 **Analytic Low Field Mobility Model**

This model is activated by specifying ANALYTIC in the MODELS statement. This model can be used to specify doping and temperature dependent low field mobilities. This model also by default is specified for silicon at 300K.

3.4.3 **Lombardi CVT Model**

CVT in the models statement activates this model which has higher priority compared to all other mobility models. In this model, Matthiessen’s rule combines the components associated with mobility dependent on temperature, doping and transverse field. Activation of CVT model by default leads into activation of Parallel Electric Field Mobility Model.

3.4.4 **Shockley-Read-Hall Recombination Model**

By using the SRH parameter in the MODELS statement activates this model. The electron and hole lifetime parameters, TAUN0 and TAUP0, are user-definable parameters used in the MATERIAL statement .This model signifies the Shockley-Read-Hall recombination happening within the device.

3.4.5 **Auger Recombination Model**

This is activated by specifying AUGER in the MODELS statement. The auger coefficients for electrons and holes namely augn and augp are user definable parameters which are incorporated in the MATERIAL statement.

3.4.6 **Boltzmann Model**

It is the default carrier statistics model used which is activated by specifying BOLTZMANN in the MODELS statement. This model as the name indicates follows Boltzmann statistics.

3.4.7 **Fermi-Dirac Model**

The specification FERMI in the MODELS statement activates this model. This model follows Fermi-Dirac statistics and is used in heavily doped regions with reduced carrier concentrations.

3.5 TUNNELING MODELS OF SIGNIFICANCE

3.5.1 **Standard Band To Band Tunneling Model**

If high electric field is present in the device, localized electric field would be sufficient to cause tunneling of electrons due when there is sufficient bending of energy bands at the tunnel junction. Hence in this scenario standard band to band tunneling model is used. BBT.STD in the MODELS statement would activate this model. The tunneling rate is given by,

$$G_{BBT} = D\ \mathrm{BB.A}\ E^{\mathrm{BB.GAMMA}} exp\left(-\frac{\mathrm{BB.B}}{E}\right) \tag{3.1}$$

where E represents electric field, D is the statistical factor, and BB.A, BB.B, and BB.GAMMA are user-definable parameters with default value as given below.

BB.A = 9.6615e^{18} cm^{-1} V^{-2} s^{-1} , BB.B= 3.0e^{7} V/cm and BB.GAMMA= 2.0
Transforming this model to Klaassen model is possible by using BBT.KL in MODELS statement instead of BBT.STD. The default values of user definable parameters used in this model are BB.A = 4.00e^{14} cm$^{-1/2}$ V$^{-5/2}$ s^{-1} , BB.B = 1.9e^{7} V/cm and BB.GAMMA= 2.5.

3.5.2 **Schenk Band to Band Tunneling Model**

In this type of model ,phonon assisted band to band tunneling is considered. This model considers constant electric field throughout the tunneling length.This is also a local model and its generation recombination rate is given by

$$G_{BBT}^{\mathrm{SCHENK}} = \mathrm{A.BBT.SCHENK} F^{7/2} S \left(\frac{(A^{\mp})^{-3/2} exp\left(\frac{A^{\mp}}{F}\right)}{exp\frac{(\mathrm{HW.BBT.SCHENK})}{kT} - 1} + \frac{(A^{\pm})^{-3/2} exp\left(\frac{A^{\pm}}{F}\right)}{1 - exp\frac{(-\mathrm{HW.BBT.SCHENK})}{kT}} \right) \tag{3.2}$$

where ,

$A^{\pm} = \mathrm{B.BBT.SCHENK}(\hbar\omega \pm \mathrm{HW.BBT.SCHENK})^{3/2}$,

S is dependent on carrier concentrations, and $\hbar\omega$ is the energy of phonon.

3.5.3 Kane Band-To-Band Tunneling Model

A local band to band model proposed by Kane with tunneling rate given by

$$G_{BBT} = \frac{D\ \mathrm{BBT.A_KANE}}{\sqrt{E_g}} F^{\mathrm{BBT.GAMMA}} \exp\left(-\mathrm{BBT.B_KANE} \frac{E_g^{\frac{3}{2}}}{F}\right) \tag{3.3}$$

where *E*g is the band gap and *F* is the electric field. It is similar to the standard models but includes influence on tunneling due to band gap.

3.5.4 **Non-local Band-to-Band Tunneling Model**.

This model takes into consideration the spatial variation of energy bands and considers the fact that generation-recombination rate at each point depends not only on the electric field local to the point. Hence this model is nonlocal in nature unlike previous models. BBT.NONLOCAL considers that the tunneling happens through 1D slices, at the tunnel junction, where each slice is perpendicular to the tunnel junction . These slices would be parallel to themselves These tunnel slices can be specified in two ways (i) creating rectangular area surrounding tunnel junction using QTX.MESH and QTY.MESH statements and (ii) creating a region around tunnel junction using QTREGION statements. The first method can be used only for planar junctions while second method is applicable for both planar as well as non-planar junctions.

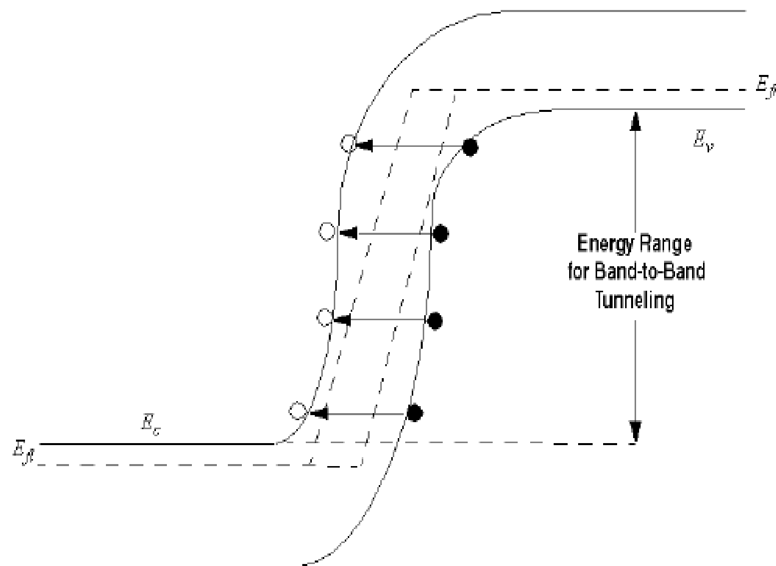

Fig.3.2 Schematic of non-local band to band tunneling[31].

Fig shows the tunneling of electrons from valence band to conduction band. Tunneling can be also considered to be with respect to holes. The tunneling probability is given by WKB approximation

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} k(x)dx\right) \tag{3.4}$$

where $\boldsymbol{k}(\boldsymbol{x})$ is evanescent wave vector between starting point(x_{start}) and ending point(x_{end}) of tunneling path.

3.6 NUMERICAL METHODS

Numerical methods are specified in the METHODS statement. Three types of techniques are used to find solution:1.Gummel

2.Newton

3.Block

Gummel method finds solution for one unknown variable keeping all other variables constant ,the process continues still a stable solution is obtained while newton method solve all the unknowns together. Block method is in between newton and gummel methods where it solves some unknowns together. For tunnel FET which is the device under consideration in this thesis, gummel is generally used.

3.7 OBTAINING SOLUTIONS

Voltages are supplied on the electrodes on the device and then current as well as other parameters such as electric fields and carrier concentrations are calculated . Initially electrodes are given zero voltages and then the bias applied is varied in small steps. These are specified in SOLVE statements.

3.7.1 DC Solution

To apply a fixed DC bias on electrode, DC solve statements are used.

Syntax:

```
SOLVE <v.electrode name>=<value>.
```

This statement implies that the particular electrode ,' *electrode name*' is supplied with DC voltage '*value*'.

To sweep the bias at a particular electrode from '*value1*' to '*value2*' in steps of '*step1*', following syntax can be used.

Syntax:

```
SOLVE <v.electrode name>=<value1> VSTEP=<step1> VFINAL=<step2>
NAME=<electrode name>.
```

To obtain convergence for the equations used, supply a good initial guess for the variables to be evaluated at each bias point. Initial solution is performed by the statement, SOLVE INIT.

3.7.2 AC SOLUTION

Specifying AC simulations is a simple extension of the DC solution syntax. AC small signal analysis is performed as a post-processing operation to a DC solution. The results of AC simulations are the conductance and capacitance between each pair of electrodes.

Syntax:

SOLVE VBASE=<value1> AC FREQ=<value2> FSTEP=<value3> NFSTEPS=<value4>

3.8 INTERPRETING THE RESULTS

Atlas produces three different types of output files.

3.8.1 Run-Time Output

Run-time output is provided at the bottom of the DeckBuild Window. Errors occurring in the run-time output will be displayed in the run-time window.

3.8.2 Log Files

Log files store the terminal characteristics calculated by Atlas. These are current and voltages

for each electrode in DC simulations. In transient simulations, the time is stored. In AC simulations, the small signal frequency and the conductances and capacitances are saved.

3.8.3 Parameter Extraction In DeckBuild

The EXTRACT command is provided within the DeckBuild environment. It allows you to extract device parameters. The command has a flexible syntax that allows you to construct specific EXTRACT routines. EXTRACT operates on the previous solved curve or structure file.

3.9 MODELS USED IN SIMULATIONS OF DEVICES UNDER STUDY

As tunneling FET is considered in this thesis, non local band-to-band tunneling model was of main interest[29].Also mobility models like concentration field mobility model, recombination models like auger recombination and SRH models were incorporated. Also Fermi model was the carrier statistics model used in the simulation[30].

3.10 SIMULATED STRUCTURE OF SINGLE DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FET.

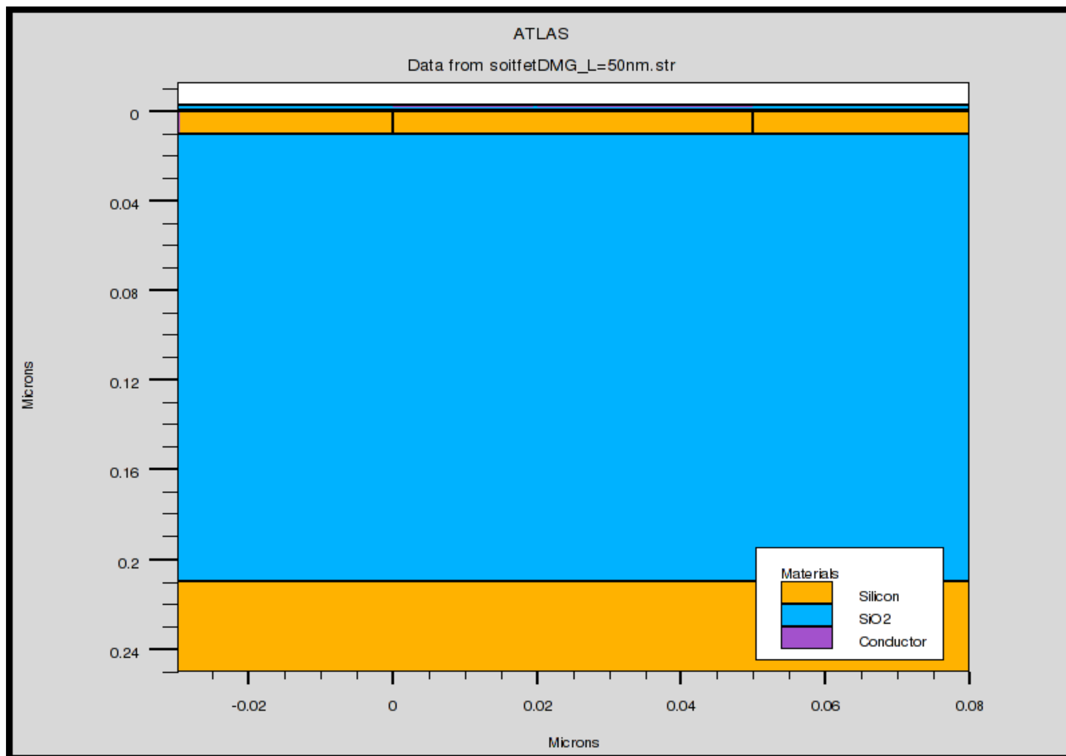

Fig. 3.3 Tonyplot structure file of SD-DMG SOITFET

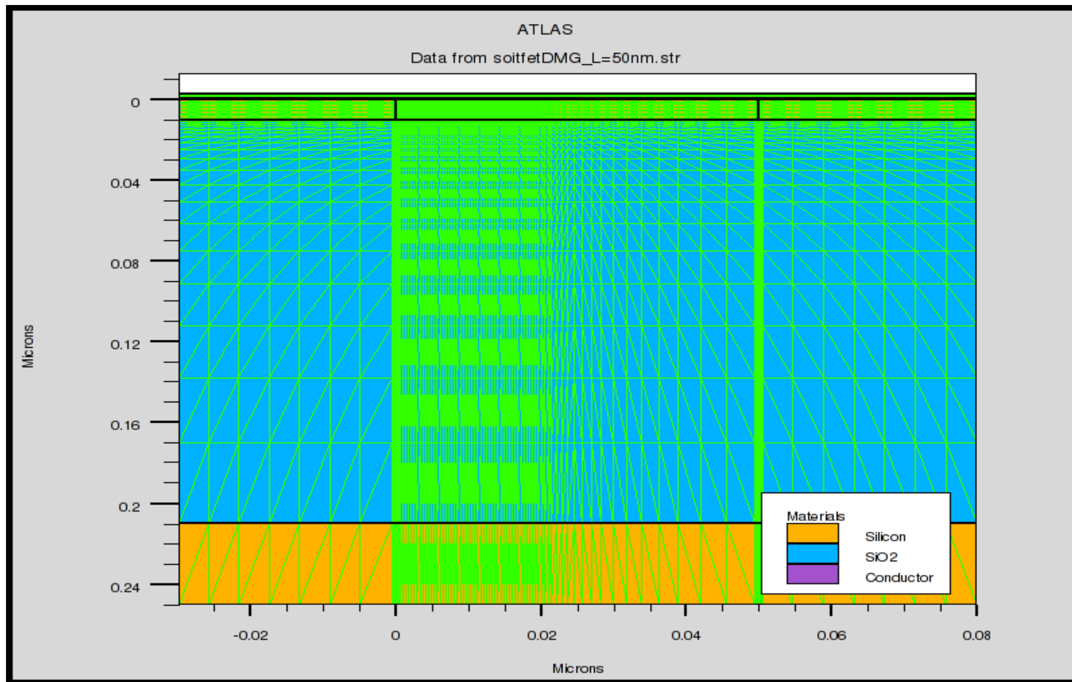

Fig.3.4 Tonyplot structure file of SD-DMG SOITFET with meshes

3.11 SIMULATED STRUCTURE OF SINGLE DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FET.

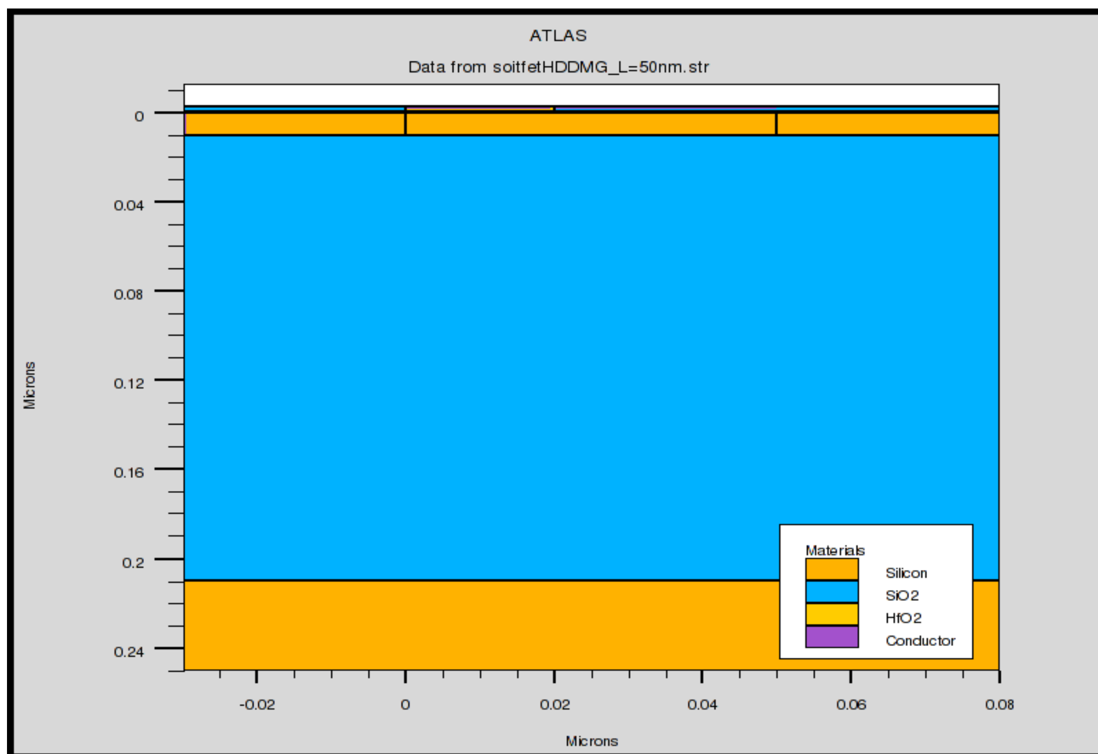

Fig.3.5 Tonyplot structure file of HD-DMG SOITFET

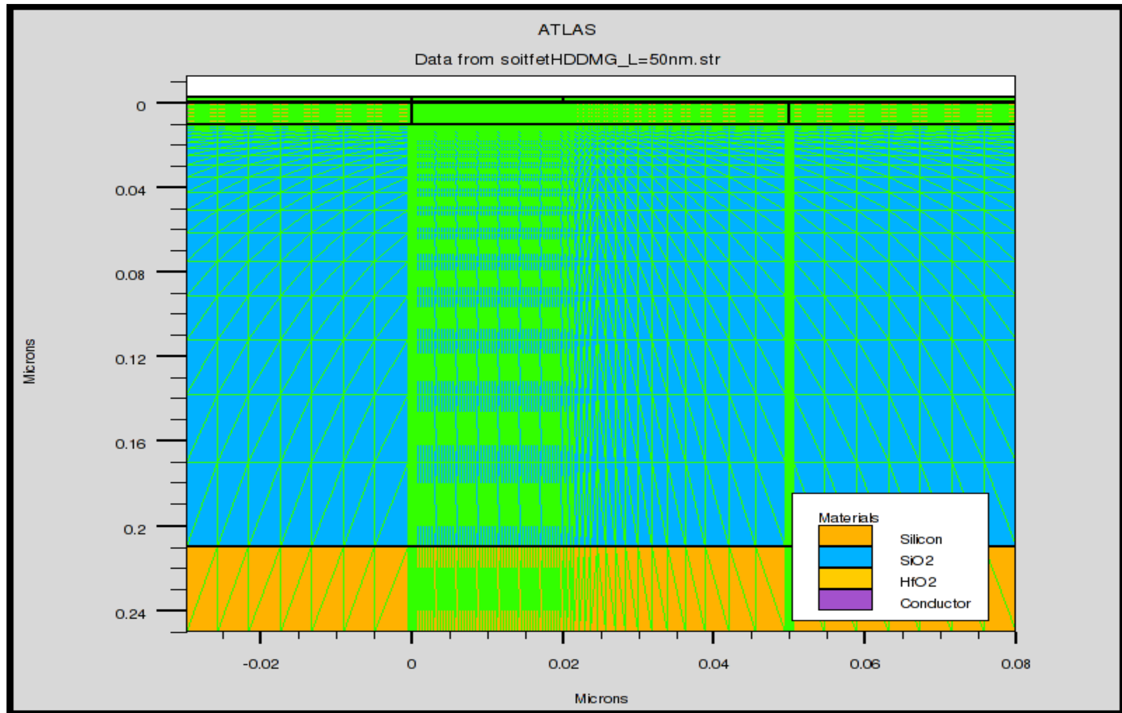

Fig.3.6 Tonyplot structure file of HD-DMG SOITFET with meshes

Fig.3.3,3.4 and 3.5,3.6 are the structures visualized in tonyplot for SD-DMG SOITFET(unmeshed,meshed) and HD-DMG SOITFET(unmeshed,meshed). It is visible in the mesh plot that,meshing is finer near the tunnel junction, so that accurate value of current due to tunneling phenomenon at the tunnel junction can be predicted.

CHAPTER 4

ANALYSIS OF SINGLE DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FET

4.1 INTRODUCTION

This chapter presents an investigation into the performance of Single Dielectric Dual Material Gate Silicon On Insulator Tunnel FET (SD-DMG SOI TFET) and compare its attributes with that of Single Dielectric Single Material Gate Silicon On Insulator Tunnel FET (SD-SMG SOI TFET).Analysis had been carried out to understand the influence of work function of the gate material on the source side(near tunnel junction) and the drain side ,on the threshold voltage of the device as well as its leakage current. Threshold voltages for the devices under study were determined. Short channel effects like Drain Induced Barrier Lowering and threshold voltage roll-off is determined for SD- DMG SOI TFET and compared to that of SD- SMG SOI TFET. RF analysis was also done to determine parameters like transconductance and intrinsic capacitances.

4.2 DEVICE STRUCTURE IN DETAIL

The cross section of SD-DMG SOI TFET, investigated in our work is shown in fig 4.1. The structure of n type SD-DMG SOI TFET described in this thesis consists of thin silicon layer (silicon body) of thickness t_{si} ,sandwiched between a very thin layer of gate oxide (SiO_2) of thickness t_{ox} and buried oxide (SiO_2) of thickness t_{box} . The buried oxide is mounted on a silicon substrate of thickness t_{sub} .The silicon body consists of a uniformly p+ doped source, uniformly p doped channel and a uniformly n+ doped drain. The silicon substrate is p doped uniformly. The gate spans over a length L_g with gate electrode made of two different metals with different work functions, φ_{tunn} and φ_{aux} spanning over a distance of L_{tunn} and L_{aux} respectively as shown in fig.1. The source as well as substrate is grounded (V_S=V_{sub}= 0V) and a voltage of V_{GS} is given to gate terminal and V_{DS} given to drain terminal. Source-channel junction and drain-channel junction are abrupt in nature and the two gate materials are connected.

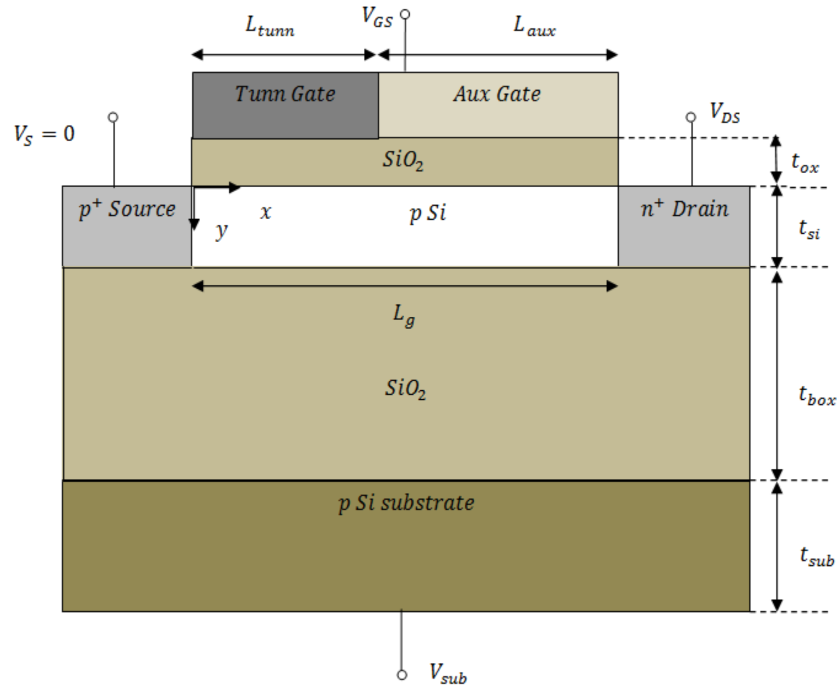

Fig 4.1 cross sectional view of SD-DMG SOI TFET.

TABLE 4.1 DEVICE PARAMETERS TAKEN FOR SIMULATION(SD-DMG)

Gate oxide thickness(t_{ox})	3nm
Silicon body thickness(t_{si})	10nm
Channel length(L_g)	50nm
Length of tunnel gate(L_{tunn})	20nm
Length of auxiliary gate(L_{aux})	30nm
Buried oxide thickness(t_{box})	200nm
Silicon substrate thickness(t_{sub})	40nm
Source doping	$1X10^{20}$ atoms/cm^3
Channel doping	$1X10^{16}$ atoms/cm^3
Drain doping	$5X10^{18}$atoms/cm^3
Substrate doping	$1X10^{17}$atoms/cm^3

4.3 OPERATION

SD-DMG SOI TFET is a p-i-n diode which is reverse biased by applying a suitably high positive drain voltage (as the tunnel FET described here is of n type). Increasing the gate voltage reduces the energy barrier width at tunnel junction and causes more of band overlap between valence band of the source side and conduction band of channel thus inducing tunneling, hence the device operates. By varying the work functions of both gate materials, modulation of band overlap as well as tunneling barrier width can be achieved, thereby having a control on the electrical characteristics of the device.

4.4 SIMULATION RESULTS

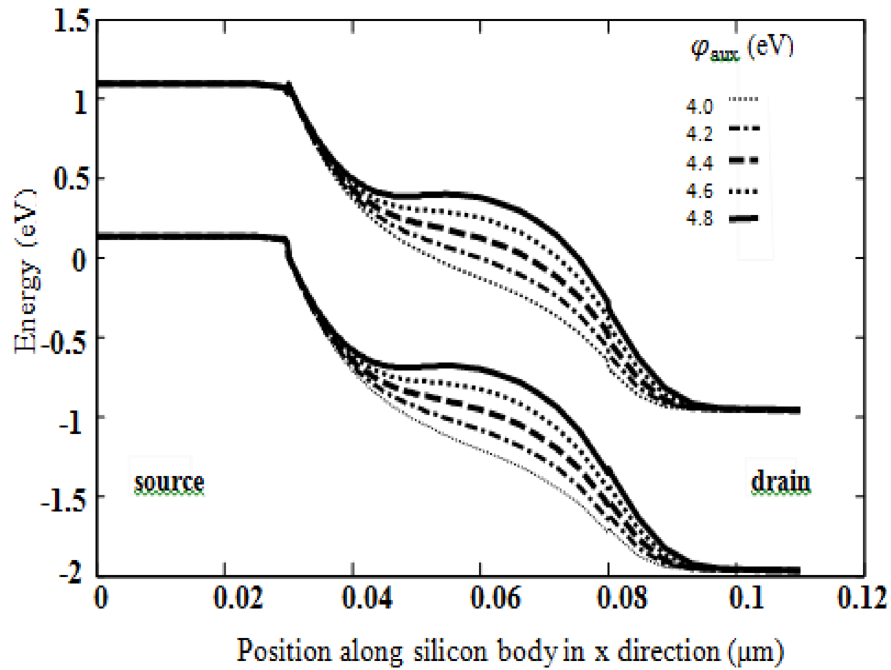

Fig.4.2 Band diagram along horizontal cutline for SD-DMG-SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{aux}

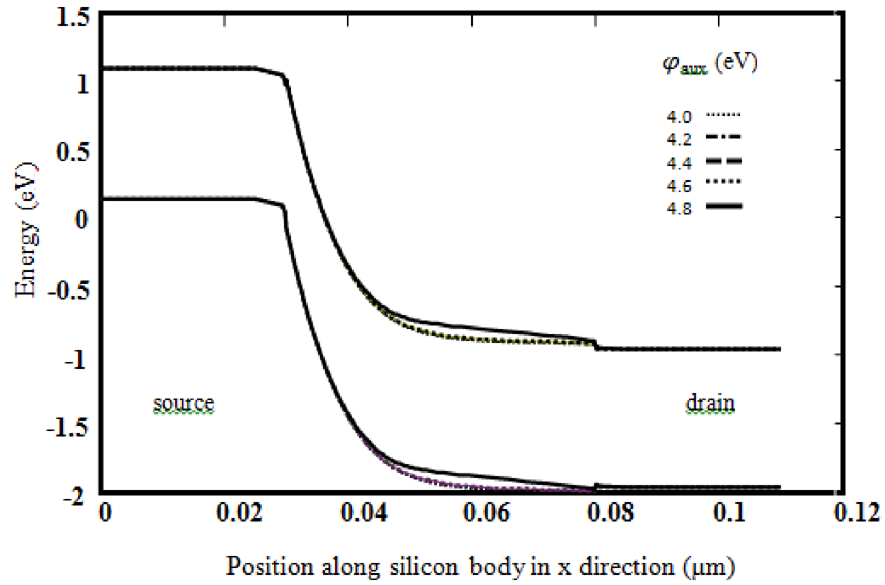

Fig 4.3 Band diagram along horizontal cutline for SD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{aux}

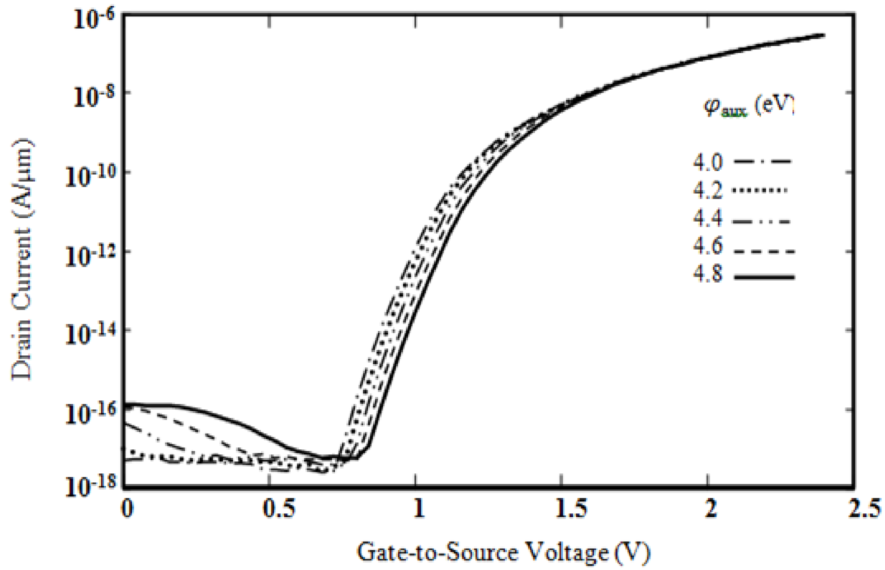

Fig.4.4 transfer characteristics for SD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) with V_{DS}=1V for different φ_{aux}

Initially work function of gate material near tunnel region(φ_{tunn}) has been fixed and work function of gate material near drain side(φ_{aux}) is varied and analyzed the energy band diagram of the structure in the OFF state (V_{GS}=0V) and ON state(V_{GS}=1.6V).This is demonstrated in fig 4.2 and fig 4.3. SD-DMG SOI TFET exhibits a very negligible leakage current of the order of 10^{-17}A/μm. As φ_{tunn} is fixed at 4.0 eV and φ_{aux} increased from 4.0eV to 4.8eV, a slight increase in leakage current is visible because at higher φ_{aux}, slightly more tunneling takes place near the intrinsic-drain junction due to lesser energy barrier near drain junction as shown in fig 4.2. In the ON state, there is a negligibly small decrease in I_{ON} as φ_{tunn} is fixed and φ_{aux} is increased, due to slight increase in tunnel width and decrease in band overlap near the source region as shown in fig4.3. The above mentioned phenomenon is visible in the transfer characteristics of the device (fig4.4), which shows that the impact on threshold voltage as well as I_{ON} for varying φ_{aux} is lesser though leakage current shows a variation from about10^{-17}A/μm to 10^{-16}A/μm. The leakage current increases more rapidly for φ_{aux}>4.4eV.

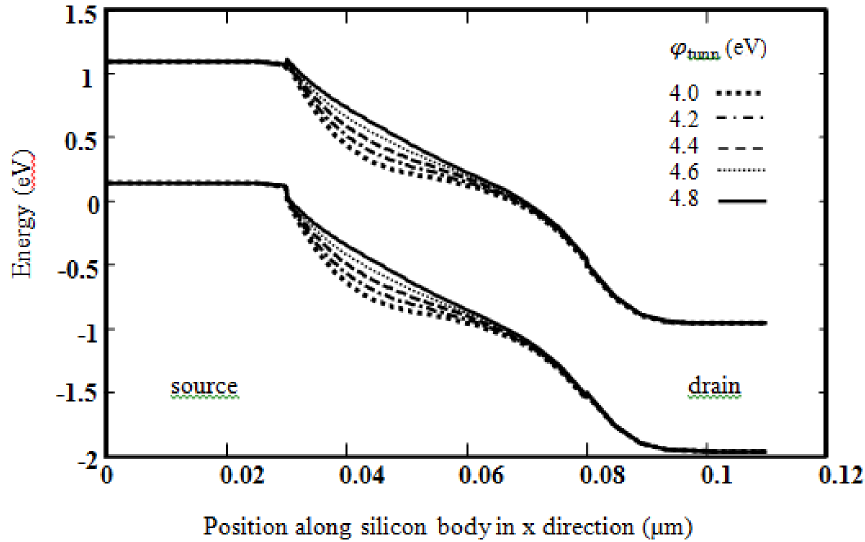

Fig4.5 Band diagram along horizontal cutline for SD-DMG SOI TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{tunn}

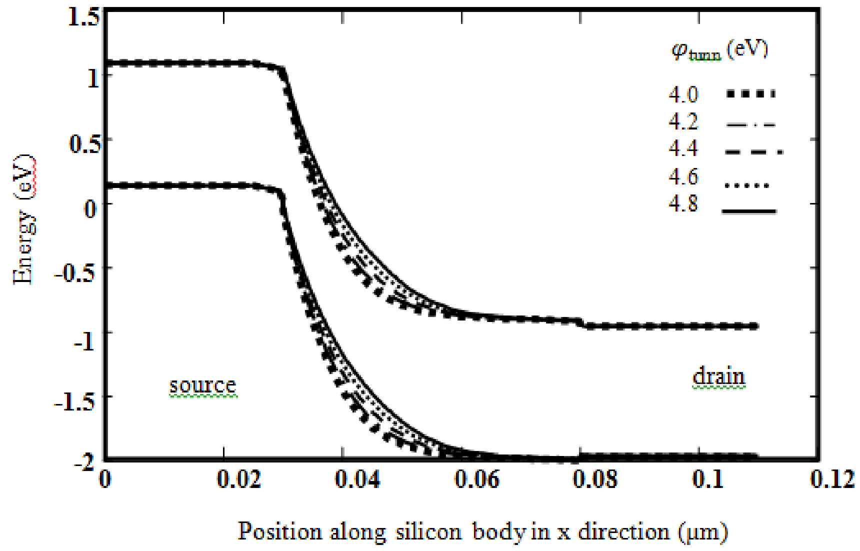

Fig 4.6 Band diagram along horizontal cutline for SD-DMG SOI TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{tunn}

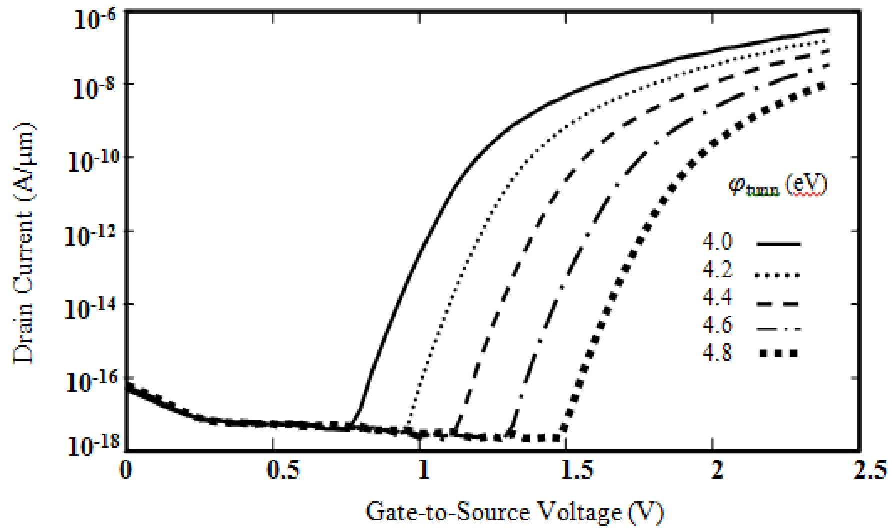

Fig 4.7 transfer characteristics for SD-DMG SOI TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) with V_{DS}=1V for different φ_{tunn}

Fig4 5 shows the variation in the band diagram of SD-DMG SOI TFET in the OFF state as φ_{tunn} is varied from 4.0eV to 4.8eV and φ_{aux} fixed at 4.4eV. As φ_{aux} is fixed and φ_{tunn} is increased, the tunnel width is considerably high in all cases. Hence very low leakage current (10^{-17}A/μm) flows in all cases. But when φ_{tunn} is lesser, gate voltage influences the tunnel junction more and induces tunneling at lesser gate voltage. Hence threshold voltage increases with increase in φ_{tunn}. Also fig 4.6 shows that in ON state, tunnel width is lesser and conduction band to valence band overlap is more when φ_{tunn} is lesser, hence causing higher I_{ON} when φ_{tunn}=4.0eV. Fig 4.7 shows the transfer characteristics in the above condition clearly depicting the greater impact caused by the variation of φ_{tunn} on the threshold voltage as well as I_{ON}. Therefore optimum φ_{tunn} is 4.0eV.So for further simulations we used optimum value of φ_{tunn}=4.0eV and φ_{aux}=4.4eV for SD-DMG SOI TFET.

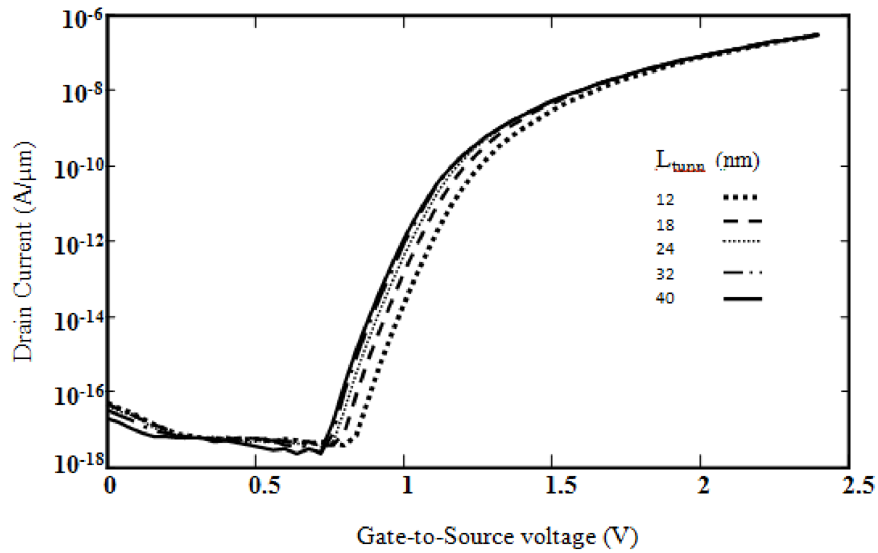

Fig4.8 transfer characteristics for SD- DMG SOI TFET (φ_{aux}=4.4eV, φ_{tunn}=4.0eV) with V_{DS}=1V for different L_{tunn}

An analysis into the dependence of transfer characteristics of SD-DMG SOI TFET on varying tunnel gate length (L_{tunn}) is done. Fig 4.8 shows variation of transfer characteristics when L_{tunn} is varied from 12nm to 40nm. It is seen that threshold voltage shows a reduction tendency on increase of L_{tunn}. When 20nm<L_{tunn}<40nm, the transfer characteristics is almost same. When L_{tunn} < 20nm, threshold voltage is comparatively higher .So we choose L_{tunn}=20nm for better I_{ON}

and lower threshold voltage. Subsequently we compare our optimized SD-DMG SOI TFET with SMG-SOITFET (work function of metal gate (φ_m)=4.0eV,4.4eV).

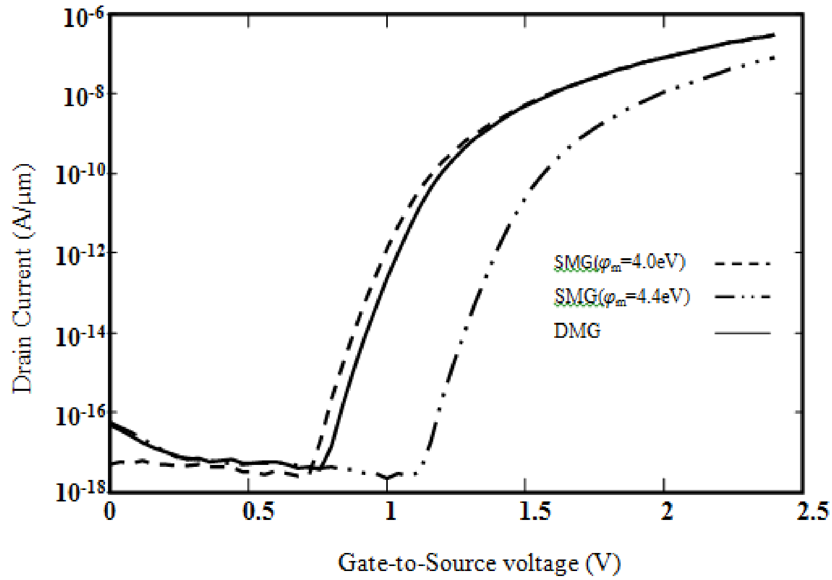

Fig 4.9 Transfer characteristics of the SD-DMG SOITFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and V_{DS} = 1.0 V) and SD-SMG SOI TFET (φ_m = 4.0 eV, φ_m = 4.4 eV, L_g = 50 nm, and V_{DS} = 1.0 V).

It is seen in fig 4.9 that SD-DMG SOI TFET has transfer characteristics similar to SD-SMG SOI TFET (φ_m=4.0eV) where the threshold voltage is lesser and I_{ON} greater than SD-SMG SOI TFET (φ_m=4.4eV).

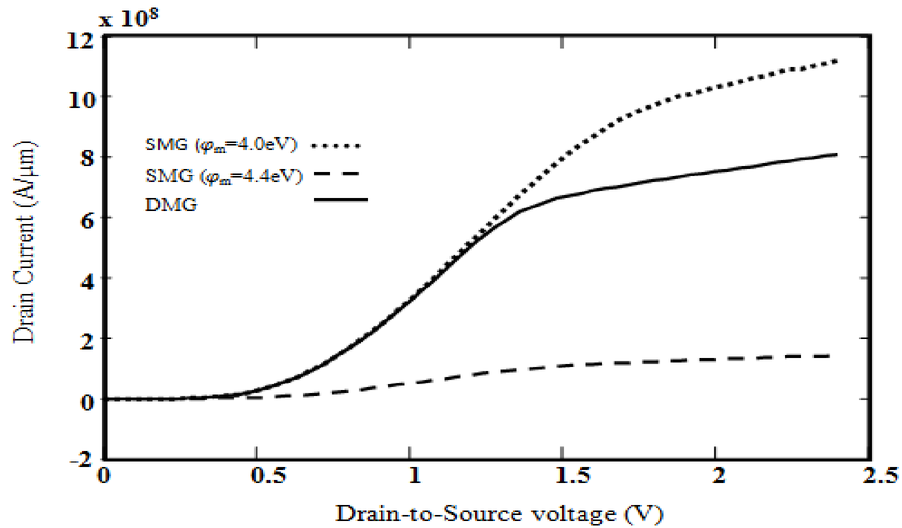

Fig 4.10 Output characteristics of the SD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, and V_{GS} = 1.8 V) and SD-SMG SOI TFET (φ_m = 4.0 eV, φ_m = 4.4 eV, L_g = 50 nm, and V_{DS} = 1.8 V).

Examining the output characteristics in fig 4.10, we see that, SD-SMG SOI TFET (φ_m=4.0eV) gives higher drain current as compared to SD-DMG SOI TFET as well as SD-SMG SOI TFET(φ_m=4.4eV), but SD-DMG SOI TFET has the added advantage over SD-SMG SOI TFET(φ_m=4.0eV), that onset of saturation happens at a lower drain voltage. Hence comparing electrical characteristics of three devices in fig 4.9 and fig 4.10, SD-DMG SOI TFET is more suitable because of its lesser saturation drain voltage and moderately high drain current thus making it more suitable for CMOS applications.

Table 4.2 DIBL for 3 types of Single Dielectric Tunnel FET

Type of TUNNEL FET	Gate Oxide used	Work functions of gate materials used (eV)	Measured DIBL(mV/V)
Single Dielectric Single Material Gate (SD-SMG)	SiO_2	4.0 only	270
Single Dielectric Single Material Gate (SD-SMG)	SiO_2	4.4 only	230
Single Dielectric Dual Material Gate (SD-DMG)	SiO_2	4.0 and 4.4	198.5

Table4.2 shows the measured value of DIBL for both single material as well as dual material tunnel FETs with SiO_2 gate oxide. It is seen from the measured values that using dual material for the gate electrode reduces threshold voltage reduction on increasing applied drain to

source voltage as compared to single material structure with work function of gate electrode either 4.0eV or 4.4eV. Hence lesser DIBL of dual material gate SOI TFET makes it a more promising candidate compared to single gate material structure.

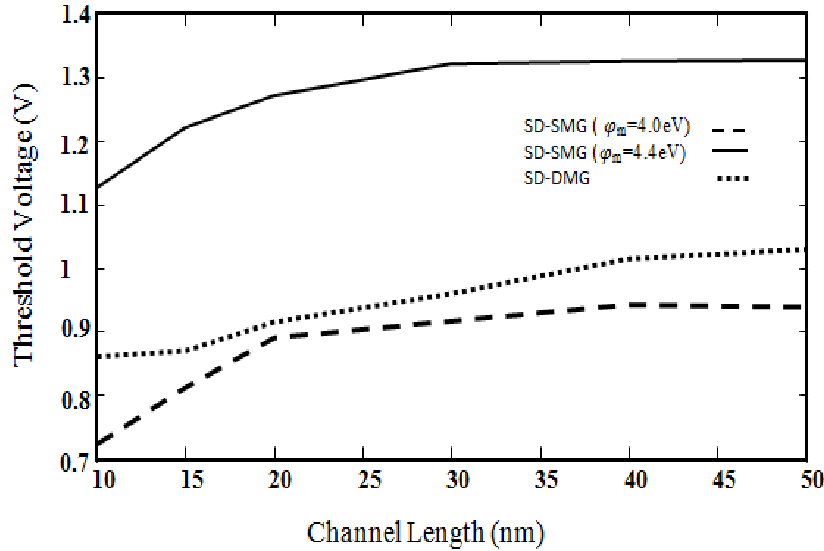

Fig.4.11. V_T at different channel length for SD- DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV) and SD-SMG SOI TFET(φ_m =4.0 eV,4.4eV)

Fig4.11 shows the comparison of threshold voltages in SD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV) and SD-SMG SOI TFET(φ_m=4.0 eV and 4.4eV) with varying channel length. It can be seen that threshold voltage (V_T) is slightly lower in Single Material Gate device with work function 4.0eV as compared to Dual Material Gate counterpart but it is the highest for Single Material Gate tunnel FET with work function, 4.4eV. Though Dual Material Gate exhibits slightly higher threshold voltage for all channel length compared to SD-SMG SOI TFET(φ_m=4.0eV) ,it is preferred here due to its lesser threshold roll off as shown in fig 4.11 . Also V_T remains almost constant when channel length is decreased further from 20nm and then there is a tremendous decrease in the case of SD-SMG SOI TFET but in SD-DMG SOI TFET the amount of decrease in threshold voltage is lesser as channel length is decreased.

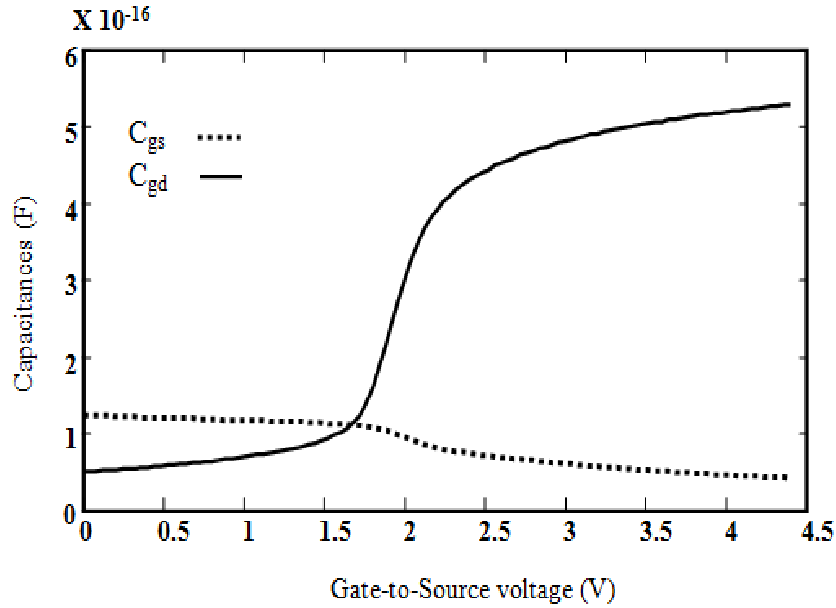

Fig4.12. Parasitic capacitances C_{gs} and C_{gd} as a function of V_{GS} in SD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm).

Intrinsic capacitance in SD-DMG SOI TFET has been determined so as to model its RF behavior. Gate-to-source capacitance (Cgs) and gate-to-drain capacitance (Cgd) as a function of V_{GS} is shown in fig.4.12. It can be seen that Cgd is the main factor influencing total gate capacitance (Cgg). Cgs decrease as V_{GS} is increased. Cgd shows a tremendous increase as V_{GS} is increased due to reduction of potential barrier at the drain side.

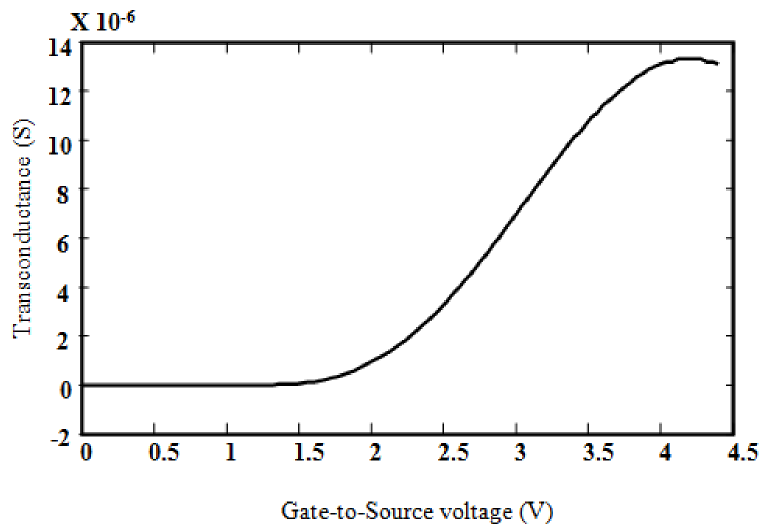

Fig 4.13. Transconductance as a function of V_{GS} in SD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm).

Fig4.13 shows the variation of transconductance (gm) with varying V_{GS} for SD-DMG SOI TFET. gm is in the order of μS comparatively lesser than conventional MOSFET.

4.5 CONCLUSION

As shown, with suitable combination of work functions of the gate materials in SD-DMG SOI TFET, optimized electrical characteristics can be obtained. Also the influence of work functions of the gate materials on the tunnel side as well as drain side on the transfer characteristics has been studied. Comparison of the transfer characteristics as well as output characteristics had shown that SD-DMG SOI TFET as a better candidate compared to SD-SMG SOI TFET.SDDMG-TFET has the added advantage as DIBL as well as threshold voltage roll-off was found to be lesser .Also transconductance and intrinsic capacitances were obtained through simulation and lesser value of drain current leads to a reduced transconductance compared to conventional MOSFET

CHAPTER 5

ANALYSIS OF HETERO DIELECTRIC DUAL MATERIAL GATE SOI TUNNEL FETS.

5.1 INTRODUCTION

In this chapter an investigation into the performance of Hetero Dielectric Dual Material Gate SOI Tunnel FET (HD-DMG SOI TFET) has been done and its characteristics with that of Hetero Dielectric Single Material Gate SOI Tunnel FET (HD-SMG SOI TFET) is compared. By suitable combination of work functions of both the gate materials, steep I_d-V_g variations and higher I_{ON} to I_{OFF} ratio of 1.6 X 10^{11} had been achieved. Also using a high K dielectric near the tunnel junction and low K dielectric near the drain junction enhancement in the tunneling ON current as well as suppression in the ambipolar nature of Tunnel FET is visible. Advantages in using a Dual Material Gate compared to Single Material Gate such as lesser threshold voltage and lower DIBL have also been studied. The chapter winds up by provides an insight into the merits provided by employing hetero dielectric structure with dual material gate on SOI tunnel FET as compared to its single dielectric counterpart.

5.2 DEVICE STRUCTURE IN DETAIL

The cross section of HD-DMG SOI TFET, investigated in our work is shown in fig 5.1. The structure of n type HD-DMG SOI TFET consists of thin silicon layer (silicon body) of thickness t_{si}, sandwiched between a very thin layer of gate oxide (HfO_2 and SiO_2) of thickness t_{ox} and buried oxide (SiO_2) of thickness t_{box} . The high K gate oxide (HfO_2) is present near the tunneling junction spanning over a distance L_{tunn} and low K gate oxide (SiO_2) present adjacent to HfO_2, towards the drain side, spreading over a length L_{aux} as shown in fig 5.1 The buried oxide is mounted on a silicon substrate of thickness t_{sub} .The silicon body consists of a uniformly p+ doped source, uniformly p doped channel and uniformly n+ doped drain. The silicon substrate is p doped uniformly. The gate spans over a length L_g with gate electrode made of two different metals with different work functions, φ_{tunn} and φ_{aux} spanning over a distance

of L_{tunn} and L_{aux} respectively as shown in fig.5.1. The gate electrode with work function φ_{tunn} is exactly above HfO_2 and that with work function φ_{aux}, exactly above SiO_2. The source as well as substrate is grounded (V_S=V_{sub}= 0V) and a voltage of V_{GS} is given to gate terminal and V_{DS} given to drain terminal. Source-channel junction and drain-channel junction are abrupt in nature and the two gate materials are connected and so is the two gate dielectrics.

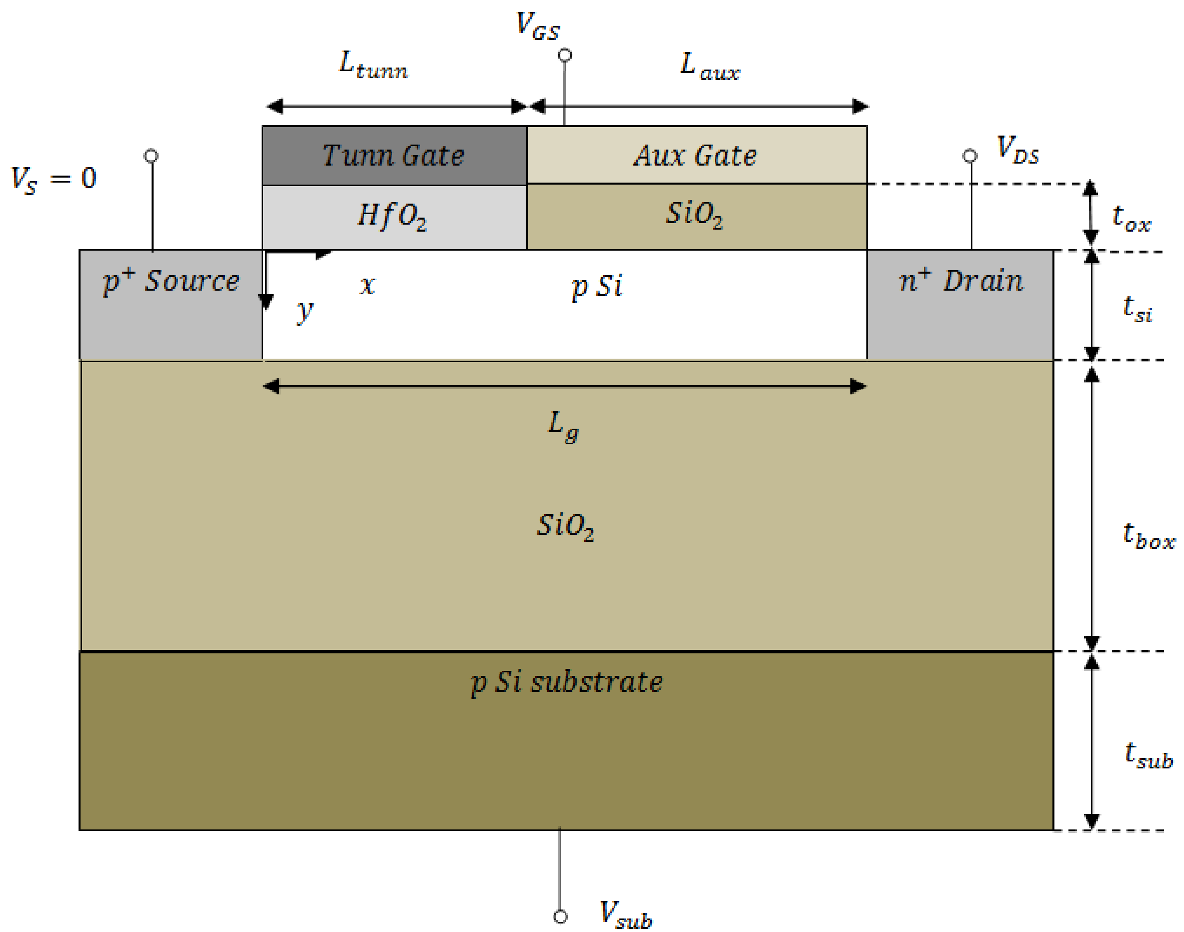

Fig.5.1.Cross sectional view of HD-DMG SOI TFET

5.3 OPERATION

HD-DMG SOI TFET is a p-i-n diode which is reverse biased by applying a suitably high positive drain voltage (as the tunnel FET described here is of n type). Increasing the gate voltage reduces the energy barrier width at tunnel junction and causes more of band overlap between valence band of the source side and conduction band of channel thus inducing tunneling, hence the device operates. For better tunneling rates we use a high K dielectric near the tunnel junction as this results in more coupling of gate voltage at the source side near the tunnel junction. By varying the work functions of both gate materials, modulation of band overlap as well as tunneling barrier width can be achieved, thereby having a control on the electrical characteristics of the device.

5.4 SIMULATION RESULTS

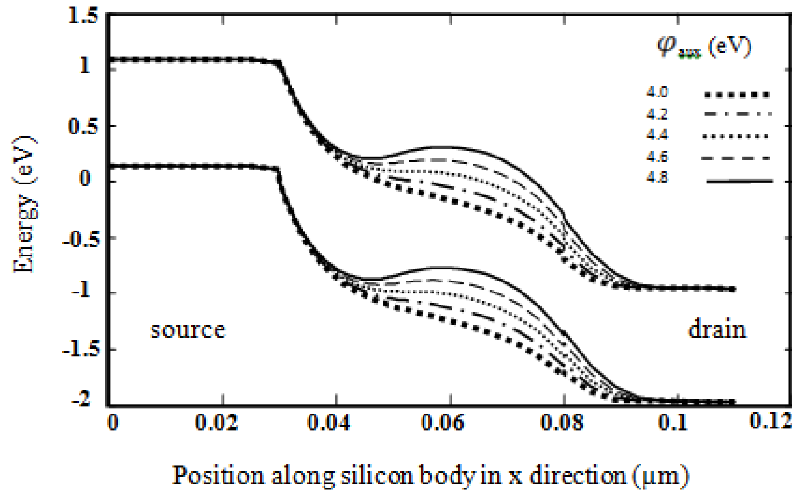

Fig 5.2 Band diagram along horizontal cutline for HD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{aux}

Work function of gate material near tunnel region(φ_{tunn}) is fixed and work function of gate material near drain side(φ_{aux}) is varied and thus analyzed the energy band diagram of the structure in the OFF state (V_{GS} =0V) and ON state(V_{GS}=1.6V). This is demonstrated in fig 5.2 and fig 5.3

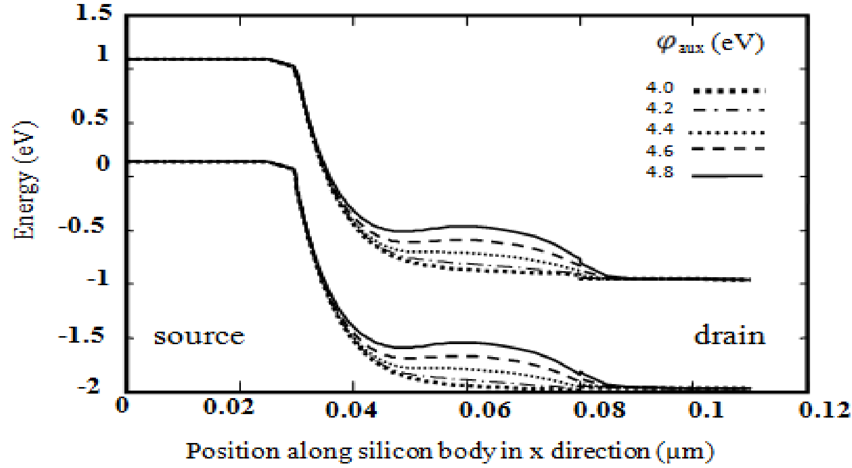

Fig 5.3 Band diagram along horizontal cutline for HD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{aux}

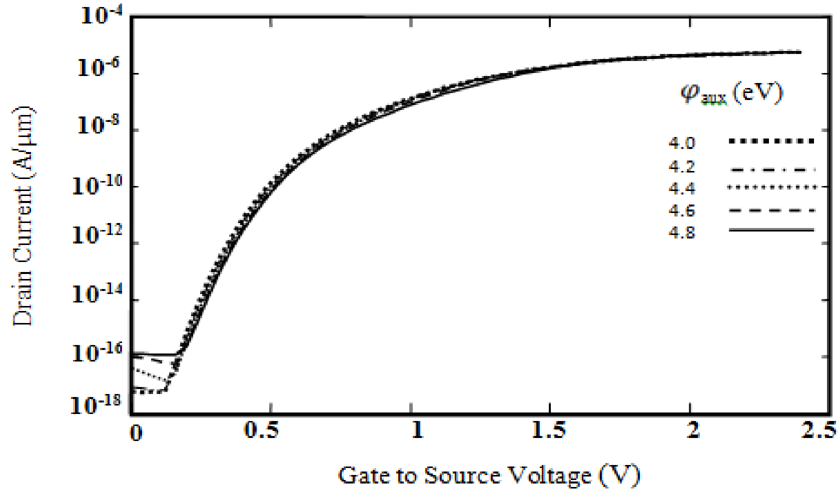

Fig 5.4 transfer characteristics for HD-DMG SOI TFET (φ_{tunn}=4.0eV,L_{tunn}=20nm,L_{aux}=30nm) with V_{DS}=1V for different φ_{aux}

HD-DMG SOI TFET has a very negligible leakage current of the order of 10^{-17}A/µm. As φ_{tunn} is fixed at 4.0 eV and φ_{aux} increased from 4.0eV to 4.8eV, we can see a slight increase in leakage current because at higher φ_{aux}, slightly more tunneling takes place near the intrinsic-drain junction due to lesser energy barrier near drain junction as shown in fig 5.2. In the ON state, there is negligible variation in I_{ON} as φ_{tunn} is fixed and φ_{aux} is increased, the band diagram in this condition is as shown in fig 5.3. The above mentioned phenomenon is visible in the transfer characteristics of the device (fig5.4), which shows that the impact on threshold voltage

as well as I_{ON} for varying φ_{aux} is lesser though leakage current shows a variation from about 10^{-17}A/µm to 10^{-16}A/µm.The leakage current increases more rapidly for φ_{aux}>4.4eV.

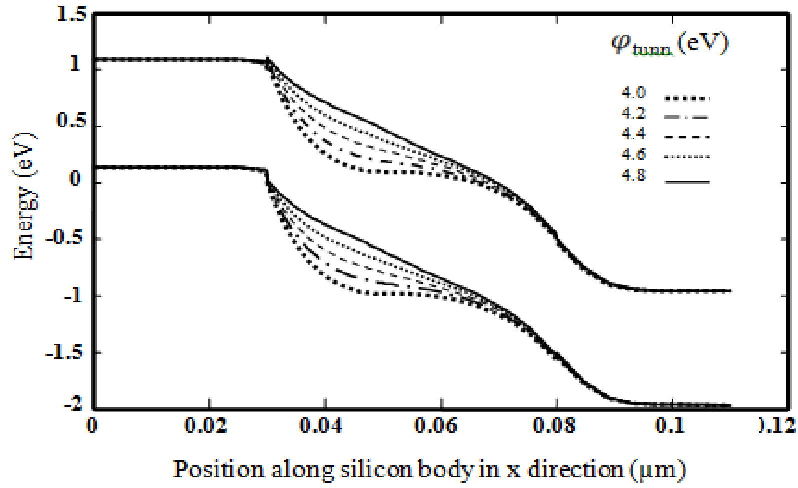

Fig 5.5 Band diagram along horizontal cutline for HD-DMG SOI TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in OFF state with V_{DS}=1V and V_{GS}=0V for different φ_{tunn}

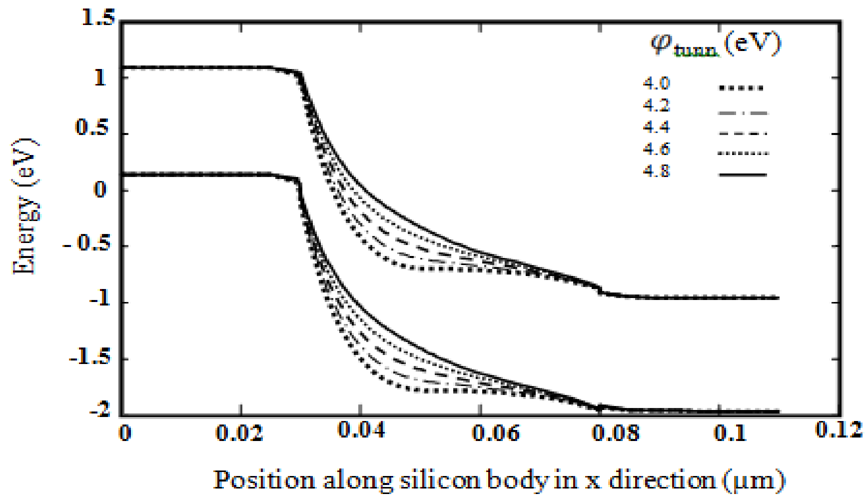

Fig 5.6 Band diagram along horizontal cutline for DMG-SOITFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) in ON state with V_{DS}=1V and V_{GS}=1.6V for different φ_{aux}

Fig5.5 shows the variation in the band diagram of HDDMG-TFET in the OFF state as φ_{tunn} is varied from 4.0eV to 4.8eV and φ_{aux} fixed at 4.4eV. As φ_{aux} is fixed and φ_{tunn} is increased, the tunnel width is considerably high in all cases. Hence very low leakage current (10^{-17}A/µm) flows in all cases. But when φ_{tunn} is lesser, gate voltage influences the tunnel junction more and induce tunneling at lesser gate voltage. Hence threshold voltage increases with increase in φ_{tunn}.

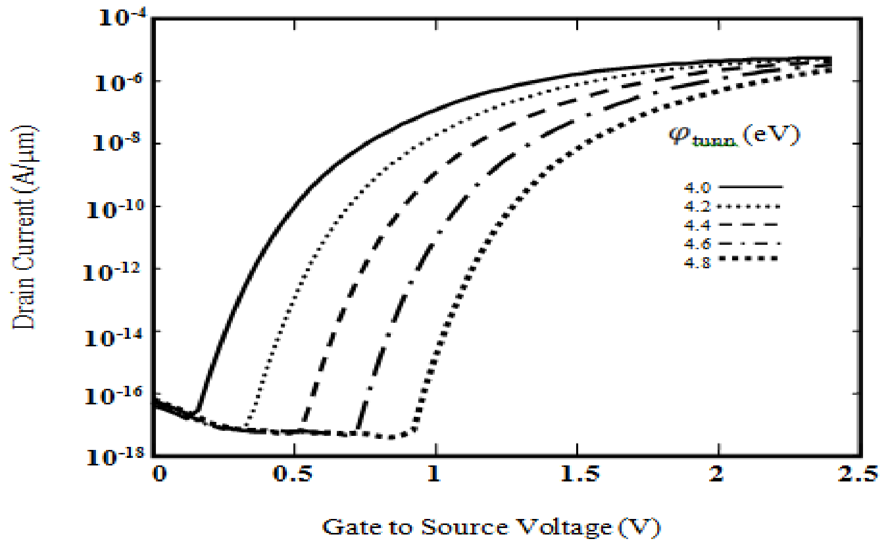

Fig 5.7 transfer characteristics for HDDMG-TFET (φ_{aux}=4.4eV,L_{tunn}=20nm,L_{aux}=30nm) with V_{DS}=1V for different φ_{tunn}

Also fig 5.6 shows that in ON state, tunnel width is lesser and band overlap is more at the source region when φ_{tunn} is lesser, hence causing higher I_{ON} when φ_{tunn}=4.0eV. Fig 5.7 shows the transfer characteristics in the above condition clearly depicting the greater impact caused by the variation of φ_{tunn} on the threshold voltage as well as $I_{ON.}$ Therefore optimum φ_{tunn} is 4.0eV. So for further simulations optimum value of φ_{tunn}=4.0eV and φ_{aux}=4.4eV has been used for HD-DMG SOI TFET.

Analysis on the dependence of transfer characteristics of HD-DMG SOI TFET on varying tunnel gate length (L_{tunn}) is done. Fig 5.8 shows variation of transfer characteristics when L_{tunn} is varied from 12nm to 40nm.It is seen that threshold voltage shows a slight reduction tendency on

increase of $L_{tunn.}$ When 20nm< L_{tunn}<40nm, the transfer characteristics is almost same. When L_{tunn} < 20nm, threshold voltage is slightly higher .So L_{tunn}=20nm had been chosen for better I_{ON} and lower threshold voltage. Subsequently comparison of optimized HDDMG-TFET with HDSMG-TFET(work function of metal gate(φ_m)=4.0eV,4.4eV) is done.

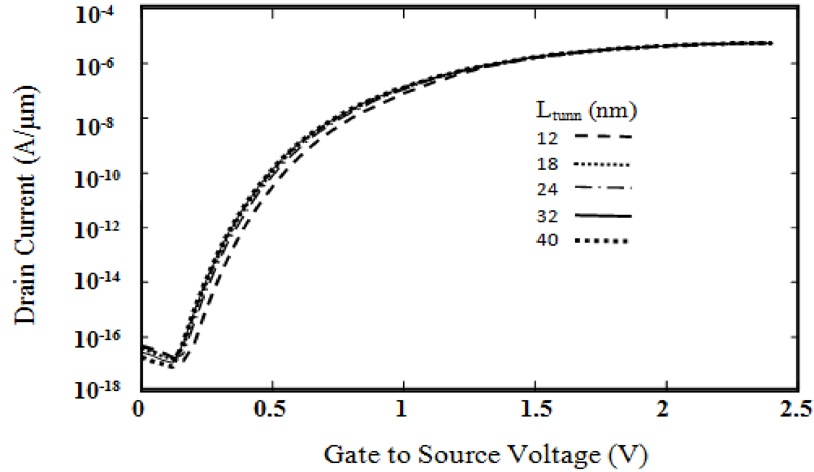

Fig 5.8 transfer characteristics for DMG-SOITFET (φ_{aux}=4.4eV, φ_{tunn}=4.0eV) with V_{DS}=1V for different L_{tunn}

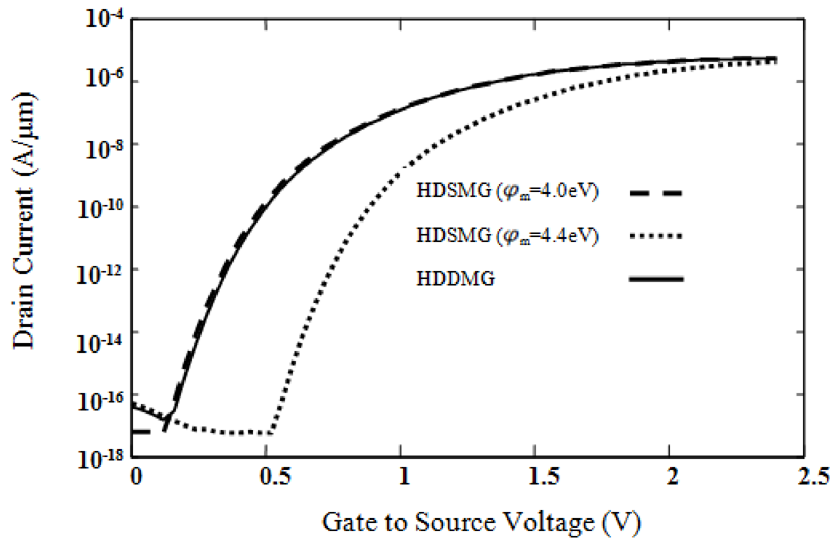

Fig 5.9 Transfer characteristics of the HDDMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and V_{DS} = 1.0 V) and HDSMG-TFET (φ_m = 4.0 eV, φ_m = 4.4 eV, L_g = 50 nm and V_{DS} = 1.0 V).

It is seen in fig 5.9 that HD-DMG SOI TFET has transfer characteristics similar to HD-SMG SOI TFET(φ_m=4.0eV) where the threshold voltage is lesser and I_{ON} greater than HD-SMG SOI TFET (φ_m=4.4eV).

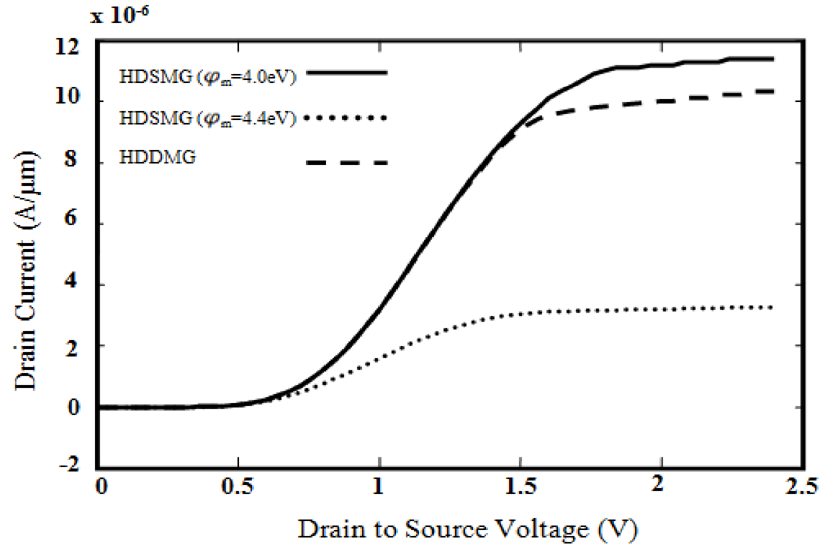

Fig 5.10 Output characteristics of the HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm and V_{GS} = 1.8 V) and HDSMG-TFET (φ_m = 4.0 eV, φ_m = 4.3 eV, L_g = 50 nm and V_{DS} = 1.8 V).

Output characteristics in fig 5.10, shows that HD-SMG SOI TFET (φ_m=4.0eV) gives slightly higher drain current as compared to HD-DMG SOI TFET as well as HD-SMG SOI TFET(φ_m=4.4eV), but HD-DMG SOI TFET has the added advantage over HD-SMG SOI TFET(φm=4.0eV) that onset of saturation happens at a lower drain voltage. Hence comparing, the transfer characteristics as well as output characteristics of three devices HD-DMG SOI TFET is more suitable because of its lesser saturation drain voltage and high drain current thus making it more suitable for CMOS applications.

Table 5.1 DIBL for 3 types of Hetero Dielectric Tunnel FET

Type of TUNNEL FET	Gate Oxide used	Work functions of gate materials used (eV)	Measured DIBL(mV/V)
Hetero Dielectric Single Material Gate (HD-SMG)	HfO_2 and SiO_2	4.0 only	120
Hetero Dielectric Single Material Gate (HD-SMG)	HfO_2 and SiO_2	4.4 only	80
Hetero Dielectric Dual Material Gate (HD-DMG)	HfO_2 and SiO_2	4.0 and 4.4	44.8

Table5.1 shows the measured value of DIBL for both single material as well as dual material tunnel FETs with hetero dielectric gate oxide. It is seen from the measured values that using dual material for the gate electrode reduces threshold voltage reduction on increasing applied drain to source voltage as compared to single material structure with work function of gate electrode either 4.0eV or 4.4eV. Hence lesser DIBL of dual material gate hetero dielectric SOI TFET makes it a more promising candidate compared to single material gate hetero dielectric structure.

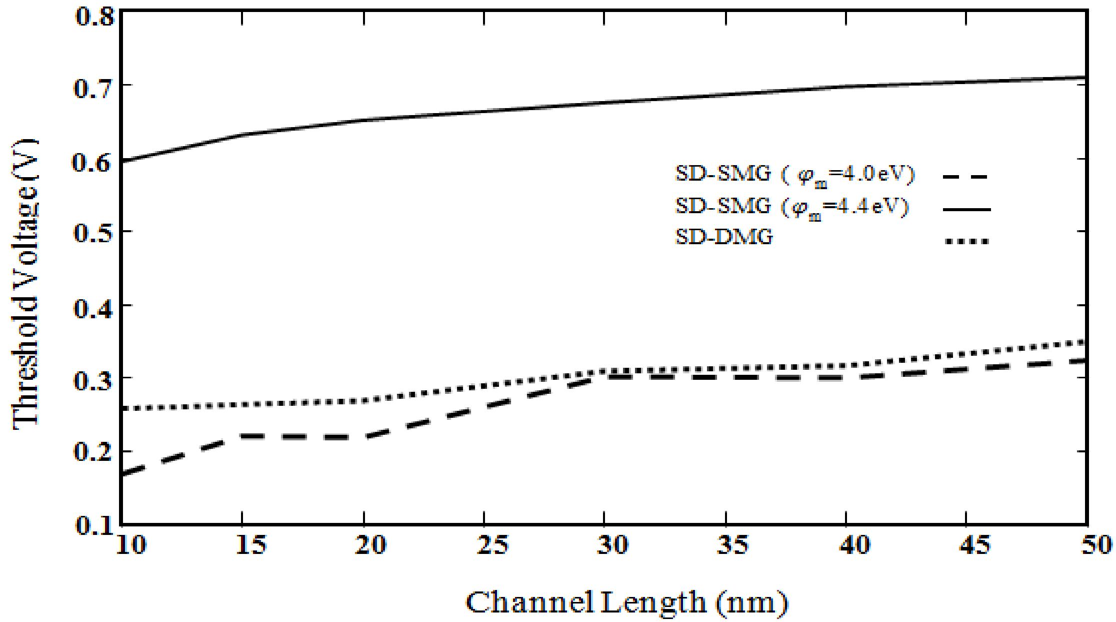

Fig. 5.11. V_T at different channel length for HD- DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV) and HD-SMG-SOI TFET(φ_m =4.0 eV,4.4eV)

Fig 5.11 shows the comparison of threshold voltages in HD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV) and HD-SMG SOI TFET(φ_m=4.0 eV,4.4eV) with varying channel length. It can be seen that threshold voltage (V_T) is slightly lower in Single Material Gate device with work function 4.0eV as compared to Dual Material Gate counterpart but it is the highest for Single Material Gate tunnel FET with work function, 4.4eV. Though Dual Material Gate exhibits slightly higher threshold voltage for all channel length compared to HD-SMG SOI TFET(φ_m=4.0eV) ,it is preferred here due to its lesser threshold roll off as shown in fig 5.11 . Also V_T remains almost constant when channel length is varied in case of Dual Material Gate but shows a staggered variation in case of Single Material Gate (φ_m=4.0eV). Hence HD-DMG SOI TFET proves to be a better transistor than other TFETs discussed here.

Fig 5.12 shows the intrinsic capacitances in HD-DMG SOI TFET so as to model RF behavior. Gate-to-source capacitance (Cgs) and gate-to-drain capacitance (Cgd) as a function of V_{GS} is shown in fig 5.12. It can be seen that Cgd is the main factor influencing total gate capacitance (Cgg). Cgs decrease as V_{GS} is increased. Cgd shows a tremendous increase as V_{GS} is increased due to reduction of potential barrier at the drain side

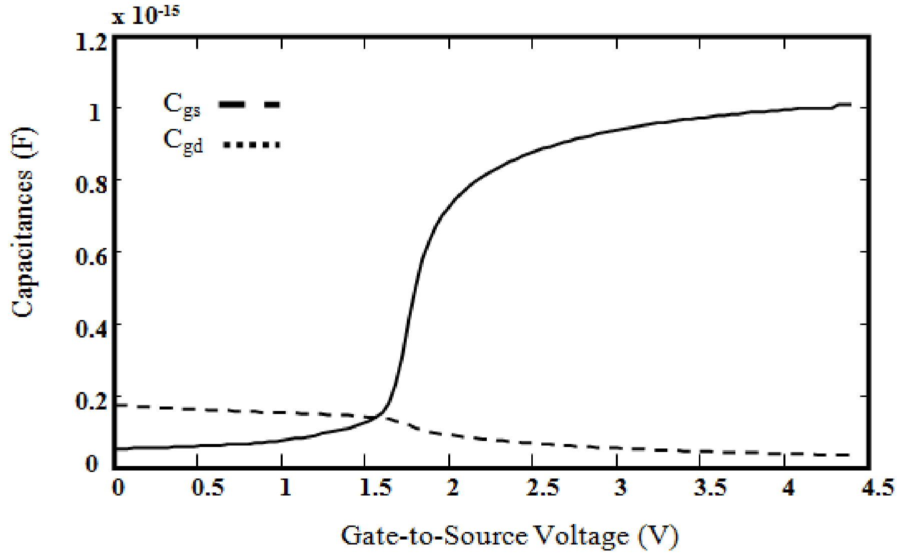

Fig 5.12. Parasitic capacitances C_{gs} and C_{gd} as a function of V_{GS} in HD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm).

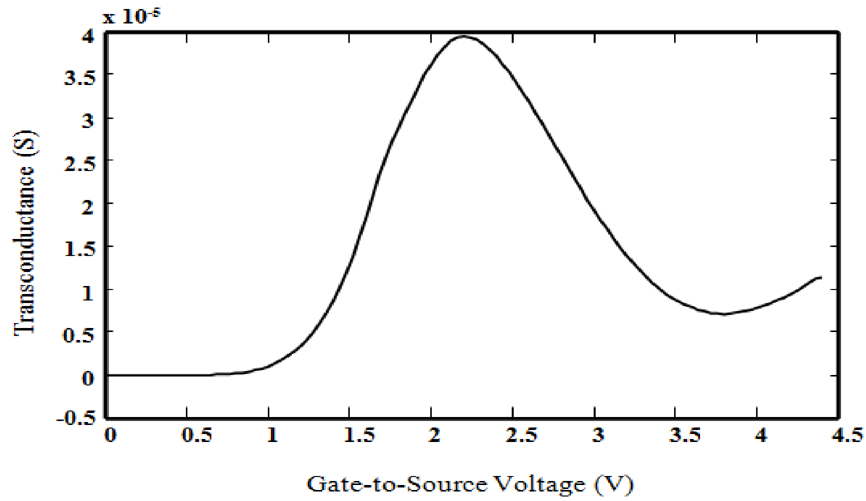

Fig 5.13. Transconductance as a function of V_{GS} in HD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, and L_{aux} = 30 nm).

Fig 5.13 shows the variation of transconductance (gm) with varying V_{GS} for HD-DMG SOI TFET. It is observed that gm reaches its maximum around 2V of gate voltage Hence the HD-DMG SOI TFET approaches to its fully ON state, when the potential at gate reaches to 2V

provided drain electrode is supplied with 1.5V. The lower ON current in the device under consideration, causes the transconductance to be of lower values as compared to conventional MOSFETs.

5.5 MERITS OF HD-DMG SOI TFET OVER SD-DMG SOI TFET

5.5.1 Reduction Of Threshold Voltage And Improvement In On Current

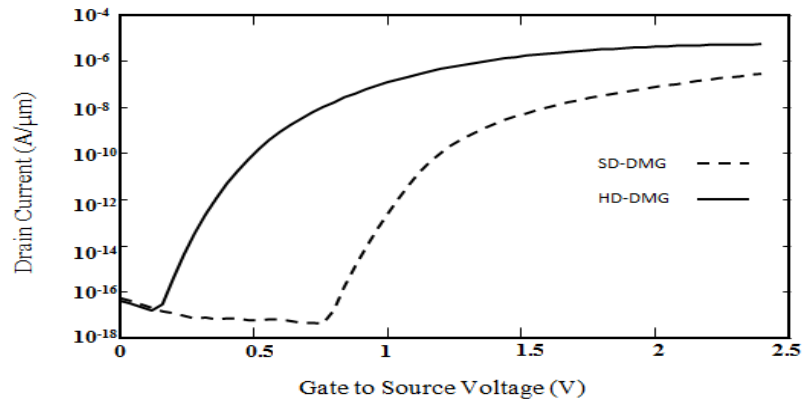

Fig 5.14. Transfer characteristics of HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, $\mathcal{E}ox_{tunn}$=25, $\mathcal{E}ox_{aux}$=3.9) , SD-DMG SOI TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, $\mathcal{E}ox$=3.9) at V_{DS} =1V

It is seen in fig 5.14 that HD-DMG SOI TFET has a better transfer characteristics with a higher I_{ON} and lesser threshold voltage as compared to SD-DMG SOI TFET as the presence of high K dielectric causes onset of band-to-band tunneling at a lesser gate voltage and a higher I_{ON} to flow in the ON state of the device

5.5.2 **Improvement in Output Characteristics**

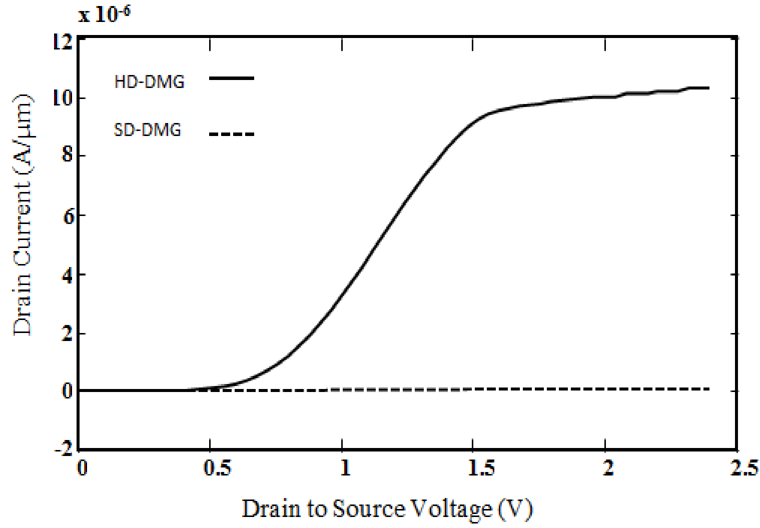

Fig 5.15 Output characteristics of HDDMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SDDMG-TFET(φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox=3.9) at V_{GS}=1.8V

Output characteristics in fig 5.15 show that HD-DMG SOI TFET gives much higher drain current as compared to SD-DMG SOI TFET (around 10^{-8}A/µm). The presence of high K dielectric near tunnel junction has caused increase in drain current by around 100 orders of magnitude.

5.5.3 **Improvement In DIBL**

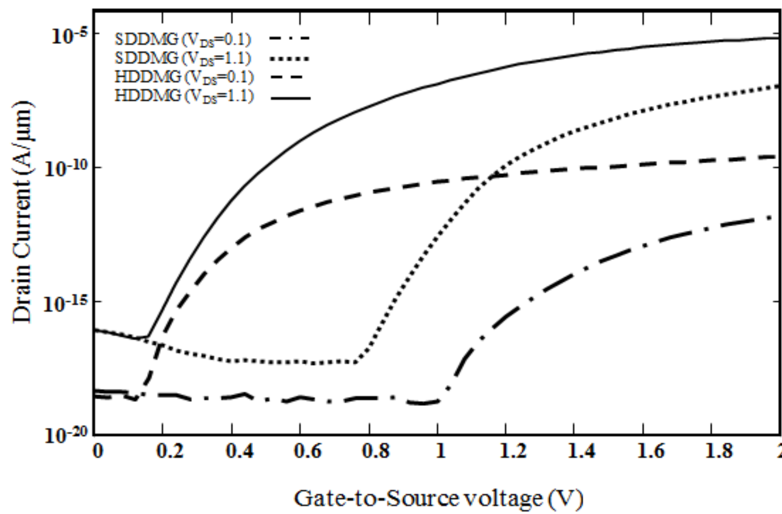

Fig 5.16 DIBL for HDDMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SDDMG-TFET(φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox=3.9) at V_{DS}=0.1V and 1V

Fig 5.16 had revealed that the DIBL reduces tremendously for Hetero Dielectric Structure compared to Single Dielectric Structure.

5.5.4 Reduction In Threshold Voltage And Threshold Voltage Roll Off

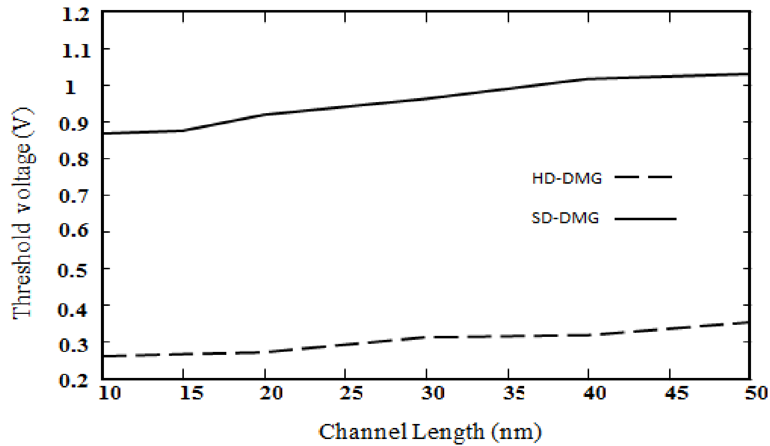

Fig 5.17. V_T at different channel length for HDDMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SDDMG-TFET (φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox=3.9)

It is seen that threshold voltage as well as threshold voltage roll off are lesser in the case of SD-DMG SOI TFET and SD-SMG SOI TFET and hence this is another advantage of dual material gate over single material gate.

5.5.5 Improvement in Intrinsic Capacitances

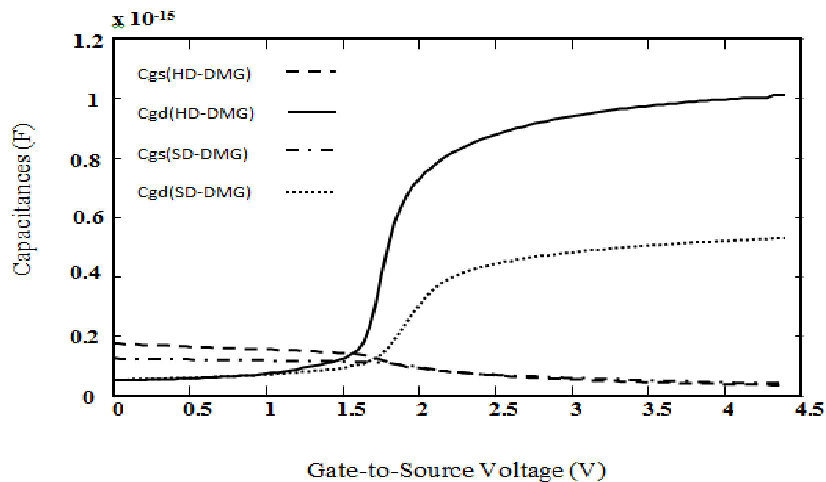

Fig 5.18. Cgs and Cgd for HD-DMG SOI TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SDDMG-TFET(φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9).

The variation of intrinsic capacitances (gate to source capacitance and gate to drain capacitance) with respect to variation in gate to source voltage is shown in Fig 5.18. It is seen that hetero dielectric structure has higher intrinsic capacitances than single dielectric structure which is due to the presence of high K gate oxide. High K dielectric due to its higher value of relative permittivity results in an increased value of intrinsic capacitance thereby causing a higher gate voltage coupling resulting in an enhanced tunneling rate.

5.5.6 Higher Transconductance

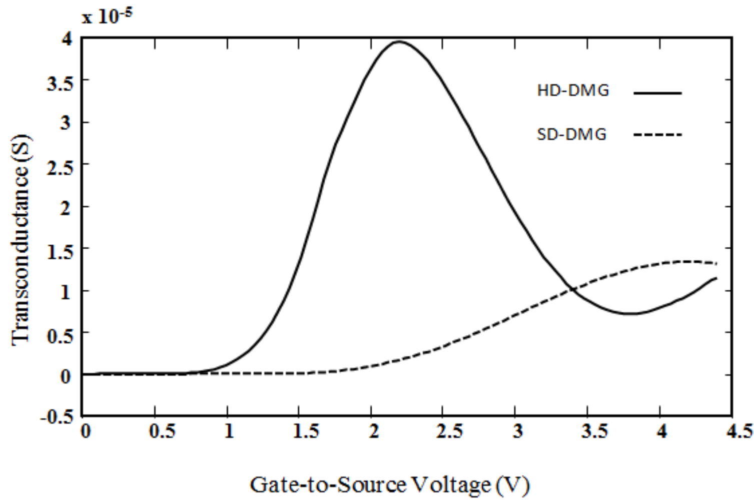

Fig 5.19. Tranconductance against varying gate-to-source voltage in for HDDMG-TFET (φ_{tunn} = 4.0 eV, φ_{aux} = 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, εox_{tunn}=25, εox_{aux}=3.9), SDDMG-TFET (φ_m = 4.0 eV, 4.4 eV, L_{tunn} = 20 nm, L_{aux} = 30 nm, Ɛox=3.9).

Fig 5.19 shows the variation of transconductance (gm) against gate to source voltage in HD-DMG SOI TFET as well as SD-DMG SOI TFET. An improvement in gm is visible in hetero dielectric structure compared to single dielectric structure hence former device gives improved RF characteristics.

5.6 CONCLUSION

As shown, with suitable combination of work functions of the gate materials in SD-DMG SOI TFET, optimized electrical characteristics can be obtained. Also the influence of work functions of the gate materials on the tunnel side as well as drain side on the transfer characteristics has been studied. Comparison of the transfer characteristics as well as output characteristics had shown that SD-DMG SOI TFET as a better candidate compared to SD-SMG SOI TFET.SDDMG-TFET has the added advantage as DIBL as well as threshold voltage roll-off was found to be lesser .Also transconductance and intrinsic capacitances were obtained through simulation and lesser value of drain current leads to a reduced transconductance compared to conventional MOSFET. Also comparisons of single dielectric and hetero dielectric DMG SOI TFETs were studied and analysis revealed that hetero dielectric structure a better candidate than single dielectric structure due to its improved I_{ON}, lesser threshold voltage, lesser threshold voltage roll off, lesser DIBL and improved transconductance.

CHAPTER 6

CONCLUSION

6.1 PERFORMANCE ANALYSIS

In the work presented here, performance based analysis of both SD-DMG SOI TFET and SD-DMG SOI TFET has been done. It was visible that varying the work functions of both tunnel gate and auxiliary gate ,influences the threshold voltage as well as on current of the device in both cases, but the effect was more when the work function of the tunnel gate is varied. In both the cases, tunnel gate work function of 4.0eV and auxiliary gate work function of 4.4eV was chosen along with tunnel gate length of 20nm which gave optimized electrical characteristics.

Also transfer characteristics as well as output characteristics of Single Gate material structure was compared with Dual Gate Material Structure. It is seen that short channel effects like threshold voltage roll off as well as DIBL are lesser for DMG structure compared to SMG structure. Also transconductance as well as intrinsic capacitances with respect to varying gate voltages were analyzed for each structure.

From the results obtained for both the structures, a comparative study was done which revealed the superiority of hetero dielectric structure as compared to single dielectric structure. It was observed that HD-DMG SOI TFET has lesser threshold voltage and higher on current compared to SD-DMG SOI TFET. Also there is a tremendous decrease in DIBL in Hetero TFET as compared to Single dielectric TFET. Threshold voltage roll off shows a slight decrease in the case of HD-DMG SOI TFET

On measuring the transconductance, it was found to be comparatively higher in hetero TFET which is due to the presence of high K dielectric near the tunnel junction. Also intrinsic capacitances (source to gate capacitance and drain to gate capacitance) were also higher in hetero dielectric TFET compared to single dielectric TFET. Hence HD-DMG SOI TFET proves to be a promising candidate for the upcoming semiconductor technology.

6.2 SCOPE OF FUTURE WORK

In the work outlined in this thesis ,performance analysis of SD-DMG SOI TFET and HD-DMG SOI TFET were done by simulations performed on both the devices. A deeper insight into the physics of operation of these devices can be obtained by mathematically modeling these devices and solving for various device parameters. Also an in depth RF analysis would characterize the device for high speed applications. It is also possible to fabricate the device, and measuring the accuracy between the experimental data and the simulation results.

BIBLIOGRAPHY

[1] http://www.computerhistory.org/semiconductor/timeline/1926-field.html.

[2] http://jackkilby.wikispaces.com/

[3] http://www.computerhistory.org/semiconductor/timeline/1959-Noyce.html

[4] http://ple.elg.ca/course/

[5] Dan Rosso, International Technology Roadmap for Semiconductors Explores Next 15 Years of Chip Technology, Semiconductor Industry Association , April 1, 2014

[6] B. A. Rainey et al, "Demonstration of FinFET CMOS Circuits", *DRC 2002*, pp. 47-48

[7] K Ranjith Kumar "Temperature Adaptive and Variation Tolerant CMOS Circuits" ,Ph.D thesis,University of Wisconsin-Madison, Wisconsin,May 2008

[8] Hei Kam "A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics", Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International

[9] A. Gerber, "Ferroelectric field effect transistors using very thin ferroelectric polyvinylidene fluoride copolymer films as gate dielectrics", Journal of Applied Physics, 107, 124119 (2010)

[10] Raymond Woo , "Band-to-band Tunneling Transistor Scaling and Design for Low Power Applications", Doctoral Thesis,Department of electrical engg,Stanford University,2009.

[11] James Towfik Teherani, "Band to Band Tunneling in Silicon Diodes and Tunnel Transistors",M.S Thesis,Massachussets Institute of Technology,June 2010

[12] Alan Seabaugh, The Tunneling Transistor,IEEE Spectrum, 30 Sep 2013

[13] J. Wan et al "Sharp-Switching CMOS-Compatible Devices with High Current Drive", Future Trends in Microelectronics: Frontiers and Innovations,2013

[14] Rakhi Narang et al, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling", JOURNAL OFSEMICONDUCTOR TECHNOLOGY ANDSCIENCE, VOL.12, NO.4, DECEMBER, 2012

[15] Peter Matheu, "Investigations of Tunneling for Field Effect Transistors",Doctoral Thesis, University of California, Berkeley, 2012

[16] Kathy Boucart and Adrian Mihai Ionescu, "Double-Gate Tunnel FET With High-K Gate Dielectric", IEEE Transactions on Electron Devices, VOL 54, NO 7, July 2007.

[17] J. Wan, C. Le Royer, et al, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling", Solid-State Electronics 65–66 (2011) 226–233

[18] Sneh Saurabh,"Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 2 FEBRUARY 2011

[19] Ning Cui, Renrong Liang,et al "Lateral energy band profile modulation in tunnel field effect transistors based on gate structure engineering", AIP Advances 022111 (2012)

[20] Upasana, Rakhi Narang, Mridula Gupta et al "Simulation Study for Dual Material Gate Hetero-Dielectric TFET: Static Performance Analysis for Analog Applications", 2013 Annual IEEE India Conference (INDICON).

[21] Adelmo Ortiz-Conde , Francisco J. García-Sánchez, et al, "Threshold voltage extraction in Tunnel FETs", Solid-State Electronics 93 (2014) 49–55.

[22] T.S.Arun Samuel, N.B.Balamurugan, S.Sibitha, R.Saranya and D.Vanisri ,"Analytical Modeling and Simulation of Dual Material Gate Tunnel Field Effect Transistors", J Electr Eng Technol Vol. 8, 2013

[23] Ravindhiran Mukundrajan, Matthew Cotter et al, "Ultra Low Power Circuit Design using Tunnel FETs", VLSI (ISVLSI), 2012 IEEE Computer Society Annual Symposium

[24] In Man Kang, Jung-Shik Jang, and Woo Young Choi, "Radio Frequency Performance of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors", Jpn. J. Appl. Phys. 50 (2011) 124301

[25] K.Sivasankaran ,P S Mallick ,et al "RF and Stability Performance of Double Gate Tunnel FET", Emerging Electronics (ICEE), 2012 International Conference on Date 15-17 Dec. 2012.

[26] Rakhi Narang, Manoj Saxena ,et al "Linearity And Analog Performance Analysis Of Double Gate Tunnel Fet: Effect Of Temperature And Gate Stack", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011

[27] Gnani, S. Reggiani, M. Rudan et al "Design Considerations and Comparative Investigation of Ultra-Thin SOI, Double-Gate and Cylindrical Nanowire FETs", Solid-State Device Research Conference, 2006. ESSDERC 2006

[28] B. Bhowmick, S. Baishya and J. Sen, "Optimisation and length scaling of raised drain buried oxide SOI tunnel FETs",ELECTRONICS LETTERS 1st August 2013 Vol. 49 No. 16

[29] Koichi Fukuda, Takahiro Mori, et al," On the nonlocal modeling of tunnel-FETs", SISPAD 2012, September 5-7, 2013

[30] M. W. Akram et al, "P-type double gate junctionless tunnel field effect transistor", Journal of Semiconductors, Vol. 35, No. 1, January 2014

[31] ATLAS Device Simulation Software User's Manual, Silvaco Int., Santa. Clara, CA, Version 5.18.3.R, 2012

PUBLICATIONS

1. **Shara Mathew**, Silpeeka Medhi, Pramod Kumar Tiwari ”A Perfoormance Analysis of Hetero Dielectric Dual-Material-Gate Silicon-on-Insulator Tunnel Field Effect Transistor (HD-DMG SOI TFET)”IEEE conference proceedings, **CCSN Micro-2014,** Kolkata(**accepted)**
2. **Shara Mathew,** Silpeeka Medhi, Pramod Kumar Tiwari “Comparative Study of Dual-Material-Gate Silicon-on-Insulator Tunnel FET (DMG-SOI TFET)“,**J.Solid State Electronics (submitted).**