POWER FACTOR CORRECTION (PFC) OF AC-DC SYSTEM USING BOOST-CONVERTER

A THESIS

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF TECHNOLOGY
IN
POWER ELECTRONICS AND DRIVES

By

PRATAP RANJAN MOHANTY

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Department of Electrical Engineering

National Institute of Technology, Rourkela-769008

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NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA

CERTIFICATE

This is to certify that the thesis entitled **"POWER FACTOR CORRECTION (PFC) OF AC-DC SYSTEM USING BOOST-CONVERTER"** submitted by **Pratap Ranjan Mohanty**, in partial fulfillment of the requirements for the award of Master of Technology in the Department of Electrical Engineering, with specialization in "**Power Electronics and Drives"** at National Institute of Technology, Rourkela is an authentic work carried out by his under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/Institute for the award of any Degree or Diploma.

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Pratap Ranjan Mohanty
M-Tech (Power Electronics & Drives)
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Specially Dedicated to PujyaGurudev……
……..My Bapuji

Dedicated to Pujya Mata-Pita, Sad-Gurudev and Prabhuji……

ABSTRACT

In the present situation, the evolution of growing in computers, laptops, uninterrupted power supplies, telecom and biomedical equipment has become overpowering. Hence, the utilization of such equipment results high power consumption and small power density which provided a large market to Distributed Power System (DPS). Power conditioning; typically rectification is essential usually for electronics equipment. Rectifier behaves as nonlinear load producing non-sinusoidal line current due to the nonlinear input characteristic. The steady growth of use of electronics equipment is become a significant problem as per the line current harmonic is concerned. Their adversative effects on the power system are acknowledged healthy. Hence fore, in three-phase systems, the neutral current magnitude increase and becomes the cause of overheating of transformers and induction motors, as well as the dreadful conditions of system voltage waveforms. There are numbers of international standards to limit the harmonic content, caused due to the line currents of equipment coupled to electricity distribution networks. Accordingly, a reduction in line current harmonics, or Power Factor Correction – PFC is vital. This idea is the inspiration to this research effort. The objective is to improve the power factor nearly unity with minimum Total Harmonic Distortion (THD).

There are two types of PFC's. 1) Passive PFC, 2) Active PFC. For this thesis work small EMI (LC) passive PFC and Boost Converter active PFC are presented with suitable switching control. Different conventional and nonlinear control schemes are analyzed for the switching of Boost PFC Converter, which is the key to obtain power factor nearly to unity with least percentage of THD. There are some major conventional control techniques that are implemented for the thesis work, which are; 1) Peak Current Control 2) Average Current Control 3) PI Control. Also for improved dynamic response and large stability range at high frequency the nonlinear controllers; 1) Dynamic Evolution Controller and 2) Sliding Mode Controller are applied. For each cases the input power factor is closed to unity and the line current waveform is observed as sinusoidal with THD percentage is in the tolerate limit.

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- ***Objective of this thesis work***

I. INTRODUCTION:

1. RESEARCH BACKGROUND:

[1]In the late 19th century the control troubles to the supply network was detected practically and it was first constructed. The British Lighting Clauses Act of 1899 was first among these to prevent uncontrolled arc-lamps from causing flicker on incandescent lamps. In the 1970's the evolution of electronic equipment claimed essential control to the disturbances produced due to the increase in electronic equipment.

[1]-[3]The day by day increase in electronics consumers and the rigid occurrence of mains rectification circuits inside the electronic devices dominants the cause of mains harmonic distortion. Some form of ac to dc power supply are used within the construction of most modern electrical and electronic apparatus and for each half cycle of the supply these supplies take pulses of current. Considering for single apparatus (a domestic television, for example) the amount of reactive power drawn may be small, but for bulk, may be 100 or more TVs the reactive power utilization from the same supply phase causing a flow of substantial amount of reactive current and hence harmonics generation. The advancement in power electronic converters reduces the weight and size and simultaneously the performance and function of such converters preferable for industrial, commercial and residential purposes.

[1]-[3]This reactive current can't be identified since the domestic tariff meter is concerned and it results loss of revenue due to the mismatch between the developed and that used power. Different streets are supplied from different phases creates 3-phase unbalance within a housing scheme. Through the neutral line of the star configuration unbalanced current flows and causes heating & burning of the conductor, in extreme cases. Also, the supply voltage waveform gets distorted because of the reactive current hence an EMC problem happens, for an apparatus, sensitive to such voltage distortion. Moreover, this cumulates supplementary losses and dielectric stresses in capacitors and cables due to the harmonic content and hence the increase in currents in windings of rotating machinery and transformers and noise in various products, and taking out of premature failure of fuses and safety modules.

[1]-[3]Since in the present situation, the rise and growth in utilization of equipment like computers, laptops, telecom, biomedical equipment, and uninterruptable power supplies is uncontrollable and also resulting to the high power draw and small power density. But

industry or market appeals the diminishment of power sources with greater power density at sensible value. Thus, it is compulsory to deliver additional power on a smaller cost and size for the telecom and computer applications. To settle these concerns, it is desired to endorse the distributed power system (DPS). Therefore, DPS has expanded from an ordinary access, utilizing isolated DC-DC converters to midway bus construction using non-isolated converters [4,5].

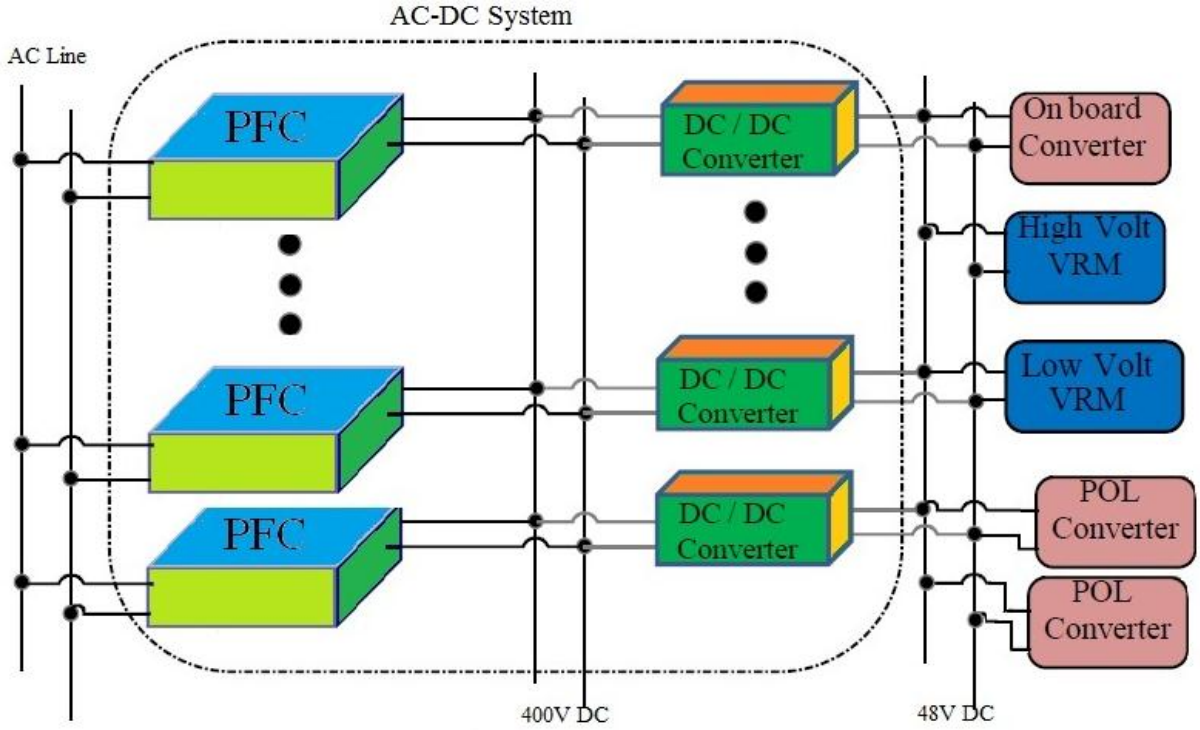


Fig. 1.1: Block Diagram of Basic Distributed Power System

2. NONLINEAR LOADS AND ITS EFFECTS:

The distortion normal electric current waveform due to the nonlinear loads creates harmonics in AC distribution systems. Nonlinear loads arise for variable resistance i.e. resistance varies for each sine wave of the applied voltage, causing in a series of positive and negative pulses, as in fig. 1.3. In AC-DC system, the connected equipment to the DPS desires some kind of power conditioning, rectification in general, which creates a non-sinusoidal line current because of the non-linear input characteristic.

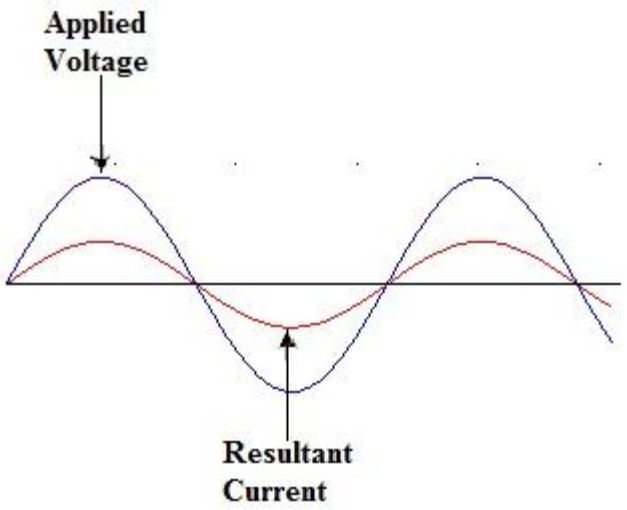


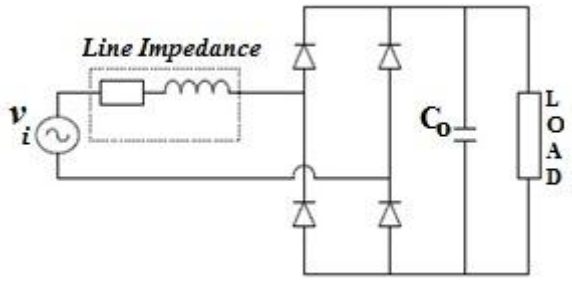
Fig 1.2: Linear Load Sine Wave

In addition to the original current

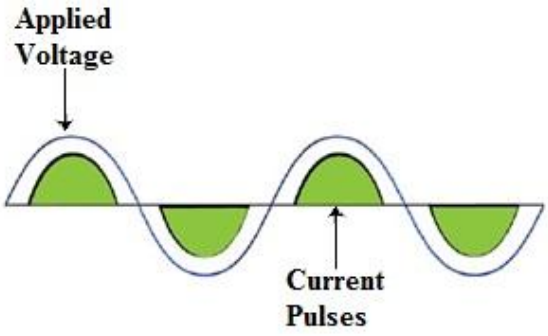
The sequence of pulses generates harmonic currents additionally to the original current. In sample, the third harmonic of 50Hz is 150Hz. For 3-phase systems, even harmonics are canceled out; hence concern is the odd harmonics only. In a balanced distribution network, at the common neutral conductor the current cancel each other out when adding together and return to the source, due to which the neutral current becomes zero. The presence of nonlinear loads, make all the third harmonic exactly in phase and add, rather than cancels in all the phases, therefore, current and heat is developed on the neutral conductor. The harmonic loads decrease the distribution capacity and effects to the quality of the power of public utility systems. Computer equipment with switched mode power supplies, battery chargers, UPSs, variable speed motors and drives, fax machines, laser printers, photocopiers, medical diagnostic equipment etc. work as nonlinear loads, invariably.

Harmonics Mitigation

Realistically, completely eliminating harmonics would be very challenging and overpriced. Understanding of the choices and their relevant costs for balancing the real harmonic load in contradiction of the cost of the solution is the vital factor. For the minimization of the actual harmonic loads there are numbers of selections offered, but should be studied deliberately because of the combined expenditure and usage of extra copper, is enhancing increase in deficient.



(a)



(b)

Fig. 1.3: Single Phase Diode Bridge Rectifier (a)Schematic (b) Typical line voltage and current waveforms (Non-linear Load Current Pulse)

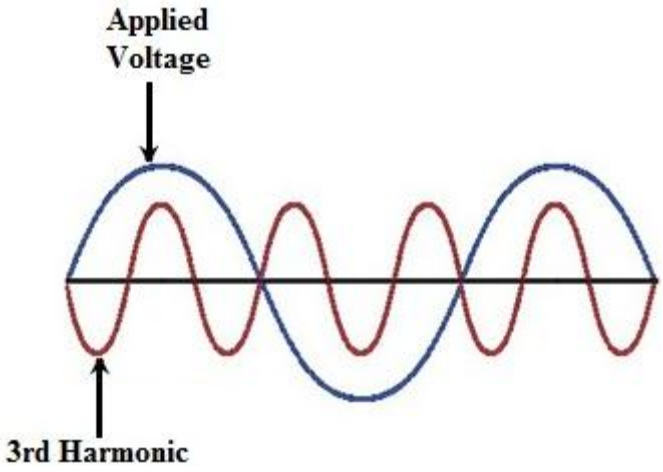


Fig. 1.4: Third Harmonic Current

STANDARDS REGULATING LINE CURRENT HARMONIC:

All the negative effects of line current distortion needs for a setting limits for the line current harmonics of joined equipment to the distribution network. Standardization activities have been carried out since long days. In 1982, the IEC-International Electro-technical Committee published standard IEC 555-2, was approved as EN 60555-2 European standard in 1987 by the European Committee for Electro-technical Standardization-CENELEC. In 1995 standard

IEC 1000-3-2 [6] [1] took position of standard IEC 555-2 and is further approved by CENELEC as European standard EN 61000-3-2.

Table 1.1: Representation of Standard IEEE 519-1992 and Odd harmonic limit

Maximum Harmonic Current Distortion in % of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits. TDD: Total Demand Distortion, based on average maximum demand current at the fundamental frequency, measured at PCC h: harmonic number						

3.1 IEC 1000-3-2 Standard:

1. To assure satisfying power quality, it enumerates the limit of load current harmonics which can be peaked from the utility.
2. It can be applied to the equipment up to 16A_{rms} per phase, with a rated current.
3. Harmonic content of the line current are set within specific limit for electrical equipment, since there are four (A, B, C and D) classes of electrical equipment, according to the IEC 1000-3-2. For rated power less than 75W these limits cannot be applied.

   CLASS A: The equipment, not described in one of the other three classes come under CLASS A. Under this class balanced three phase equipment, household appliances (shouldn't be specified under CLASS D) are present.

CLASS B: Under this class compact appliances and non-professional arc welding equipment are present.

CLASS C: Lightening (dimmer for incandescent lamp belongs to CLASS A) equipment are under this CLASS.

CLASS D: Personal Computers and monitors, television receivers etc. are the equipment with special shape of line current and with the active input power is lower than or same to 600W are under this CLASS.

3.2 IEEE 519-1992 Standard:

It explains a harmonic as, "A Sinusoidal component of a periodic wave in other words quantity including a frequency that is an integral multiple of the fundamental frequency" [7] [1]. For both utilities and individual consumers, it recommends the practices and also specifies the demand for harmonic control in power system network [7] [1]. At utility the line current harmonic limits are

given as the percentage of the maximum load current I_L (fundamental frequency component) demand at the common coupling-PCC (the electrically joined point/merge between the utility and customer distribution systems). For low ratio of I_{sc}/I_L, current distortion is reduced. In large the inductive impedance of the AC line controls the distortion level. IEEE 519-1992 limits are exceeded for the non-linear load, even when only 10%. Many time the harmonic current distortion is within IEEE 519-1992 limits, provided the non-linear loads under 20% of the total system load.

4. POWER FACTOR CORRECTION [1]-[3]

It is a measurement of the degree of the utilization of the power from grid. Mathematically it is the propertion of the real power to the apparent power and is in the range of 0 to 1.

$$PF = \frac{Real\ Power}{Apparent\ Power} \tag{1.1}$$

Real power is in watts and is the power necessary for real work done. Apparent power is in volt-amp. and is the vector summation of active and reactive power.

For pure sinusoidal voltage and current waveforms; $PF = \cos \emptyset$ (1.2)

Where "$\cos \emptyset$ " is the displacement factor of the voltage and current. In general PFC tends to the compensation of the displacement factor.

But for non-linear load i.e; for sinusoidal line voltage and non-sinusoidal line current waveform the *PF* can be expressed as;

$$PF = \frac{V_{rms}}{V_{rms}} \frac{I_{1rms}}{I_{rms}} \cos\phi \tag{1.3}$$

$$= \frac{I_{1rms}}{I_{rms}} \cos\phi$$

$$= \mathrm{K_p}\cos\phi \tag{1.4}$$

where, $K_p = \frac{I_{1rms}}{I_{rms}} = \frac{I_{1rms}}{\sqrt{I^2{}_{1rms} + I^2{}_{2rms} + \cdots + I^2{}_{nrms}}} \in [0,\ 1]$, Purity factor, represents the harmonic content of the current associated to the fundamental . Hence in practical *PF* is proportional to both harmonic content & displacement factor. Where *n* is the n^{th} order of the harmonic current.

The total harmonic distortion factor THD_i is defined as;

$$THD_i = \frac{\sqrt{I^2{}_{2,rms} + I^2{}_{3,rms} + \ldots + I^2{}_{n,rms}}}{I^2{}_{1,rms}} = \frac{\sqrt{\sum_{n=2}^{\infty} I^2{}_{n,\,rms}}}{I_{1,\,rms}} \tag{1.5}$$

Hence, $K_p = \frac{1}{\sqrt{1 + THD_i{}^2}}$ (1.6)

Therefor with a substantial harmonic content a achieving of high power factor can be possible. The power factor PF isn't much affected by harmonics, unless their amplitude is quite large (low K_p, very large THD_i). Also small harmonic content doesn't assure high power factor (*Kp* close to unity, but low *cosΦ*).

Hence in simple, the power factor correction is referred as the minimization of the line current harmonic. The main objective of the thesis is the power factor correction i.e.; maintaining a least phase angle between the input voltage and current with improved *THD* level i.e. keeping the harmonic content to a minimum level. The effect of harmonic and its problems on power system is observed as significant and hence Electricity regulatory commissions and utilities, all over the world is penalizing the users for harmonic dumping into the supply lines. Central Electricity Regulatory Commission of India has given guideline to Institute of Electrical and Electronics Engineers (IEEE) Standard 519-92 on permissible limits for harmonics in the electrical system [8] Both the utility and users should know and understand the standard and the essential of limits specified.

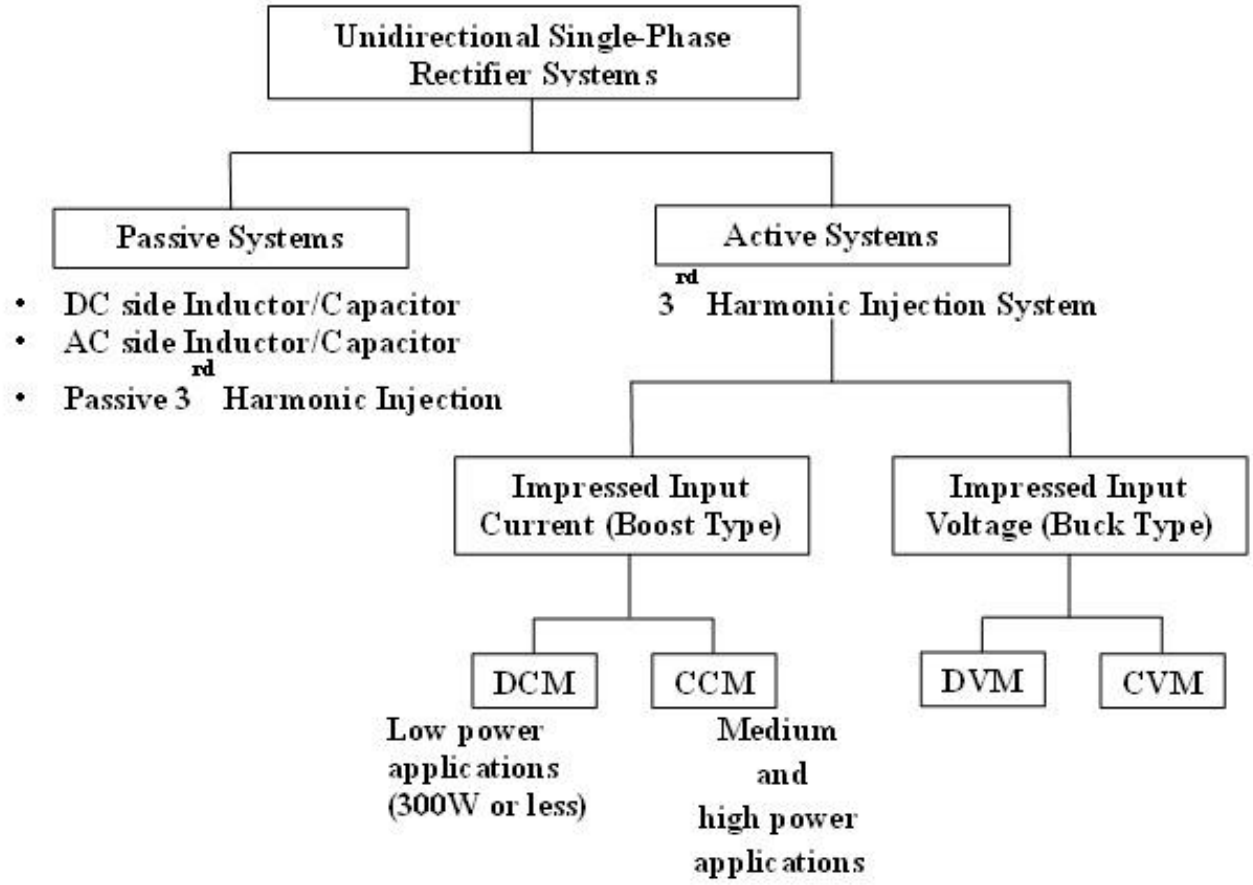
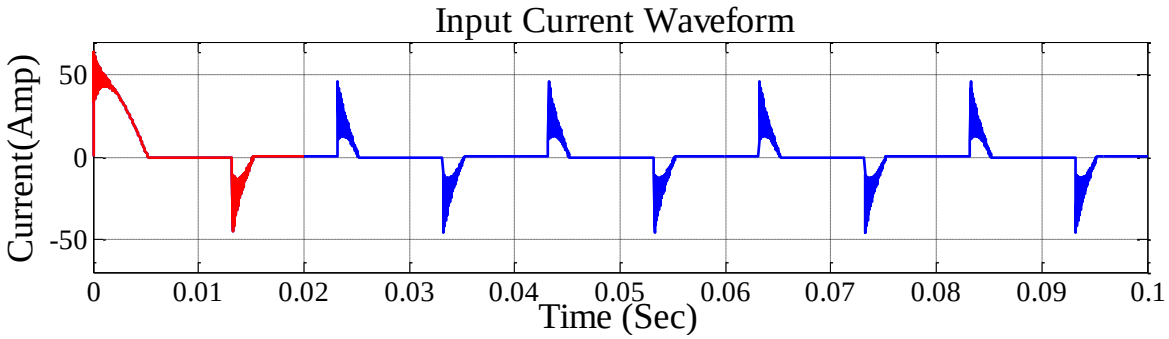
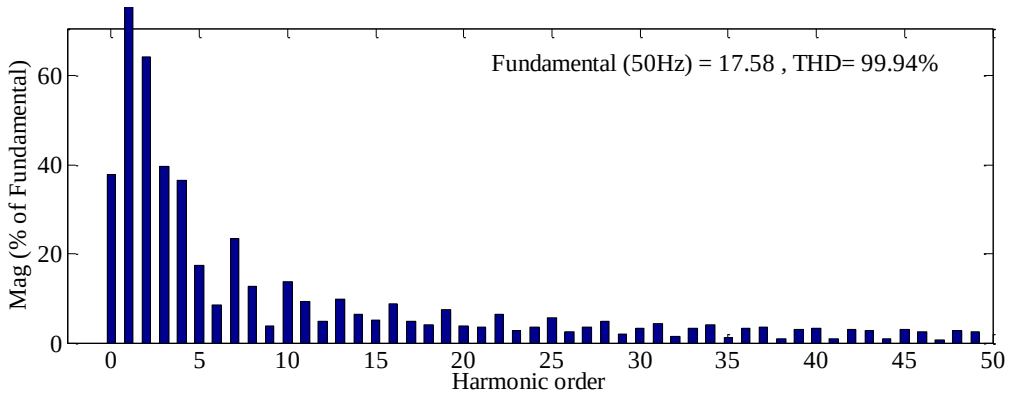


Fig. 1.5: Classification of PFC Method based on Mode of Switching



(a)



(b)

Fig. 1.6: Waveforms of AC-DC System without any PFC circuit (a)Input Current (b) THD for line voltage v_i=230Vrms R_L = 100Ω, C_o = 0.02μF, the line current has THD = 99.94% and pf=0.9396

As per earlier discussion, because of the non-linear loads in the distribution network, line current harmonics are introduced as in the fig. 1.6, which need to be minimized. There are numbers of procedures for the power factor correction [9]- [12]. But mainly, it categorized into methods as; *"Passive method"* and *"Active method"*. L-C filter is used in "P*assive PFC approach"*. L-C filter is introduced between the supply line and diode rectifier [13][14] to improve the shape of the line current as in fig. 1.6. It is simple and rugged technique but bulky in size and expensive. Moreover, in this technique power factor cannot be highly improved and output voltage is not controllable. Active switches are used in association with reactive element for "*Active PFC approach*" as in fig. 1.7 for the improvement of line current shape and to obtain controllable output voltage. For this DC-DC converter is in employment and is working at high frequency to make shape of the line current waveform as sinusoidal [9][13][14]. Boost, buck, buck-boost, flyback, cuk, or sepic topologies are the commonly used PFC DC-DC converter topologies [14-16]. Mainly Boost Converter topology is more suitable for PFC application and is widely used for PFC pre-regulation application [14],[17].

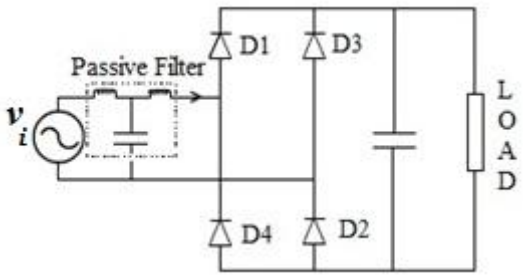


Fig. 1.7: Schematic diagram of Passive PFC Technique

Fig. 1.8 illustrates that the PFC technique improves the input current drawn from the mains supply and reduces the DC bus voltage ripple. The target of PFC is to make the input current waveform inphase to the voltage and in view of power supply like a simple resistor [9],[14]-[17]. This grants the Power Distribution System to run much efficiently, with minimum energy consumption.

This thesis work is focused in the area of active PFC approach and boost topology is employed for research on AC-DC PFC pre-regulator system for the improvement of quality of power.

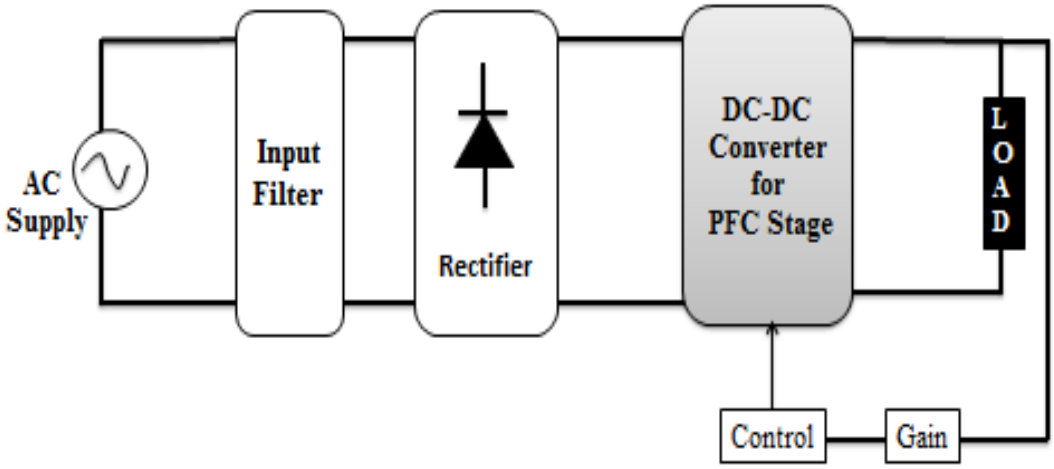


Fig. 1.8: Schematic diagram of Active PFC technique

Benefits of high power factor:

1. Voltage distortion is less.
2. All the power is active.
3. Small RMS current.
4. Higher number of loads can be fed.

Advantages of Circuits with PFC:

1. The cost saving factor like the electrical loads (SMPS, Electronic ballast unit or other electrical load) become much simpler.
2. Because of the smaller RMS current with PFC, it permits to use small, much cost-effective mains rectifiers to the manufacturer of electrical load.
3. The input voltage for the DC electrical load becomes stable and regulated. Indeed, the AC-DC system becomes operates on wide-range power supply because of PFC.

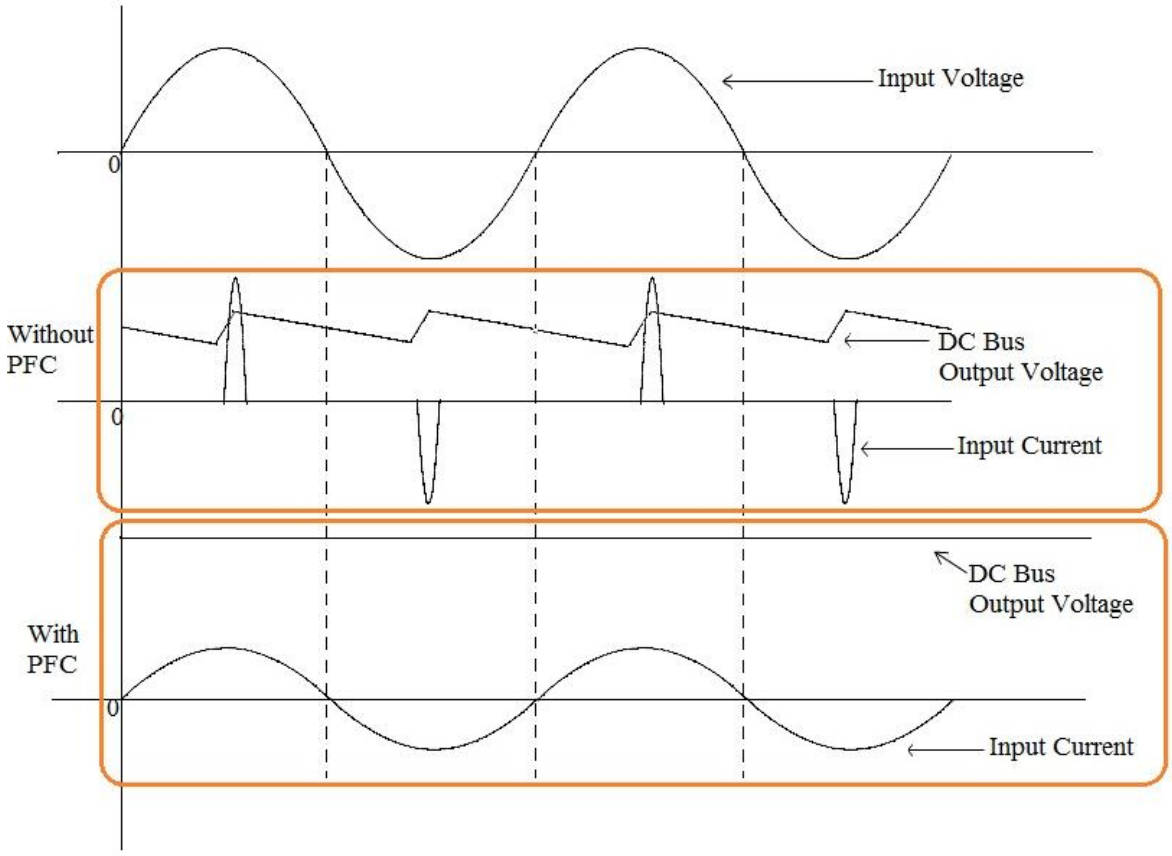


Fig. 1.9: Current Waveforms with and without PFC technique

5. BOOST VERSUS BUCK PFC CONVERTER [18][19]

Boost PFC Performance

Advantages:

- Attains very low THD, offering possibly the best power factor, PF
- Higher output voltage
- In size, efficient energy-storage capacitors
- Easy switch current sense and gate drive, because of low-side boost switch
- Relaxed surge management

Limitations:

- Output voltage must always be greater to the instantaneous AC input
- May require high-voltage regulation and isolation stage to come down the voltage to the required practical level.
- High bus voltage may cause higher levels of EMC noise.
- At start-up, since there is no inrush limitation, a costly inrush limiting mechanism with highly dissipative character is required.

- There is a significant drop in efficiency at low line, due to higher difference between the AC input voltage and the bus voltage.

Buck PFC Performance

Advantages:

- Easy functional safety spacing and isolation and regulation stage.
- Across the PFC choke there is small difference in input-to-output voltage hence merit to use a smaller value of inductor, comparatively.
- Easy control. No need of AC line-sense reference and multiplier to obtain good THD and PF.
- An auxiliary mechanism for inrush limiting is not required, because of inherent "free" inrush limitation at starting.

Limitations:

- The inherent AC line current "crossover" distortion restricts for achievable THD and PF.
- Based on the used configuration, it is required to use either a high-side bus-voltage sense or a high-side drive switch.
- Complicated surge management, since no direct link to the storage capacitor from AC input.
- Less efficient energy storage of the capacitor, due to lower output voltage. Hence, a large bulk capacitor is required with lower hold-up time.
- Requires voltage loops with lower bandwidths and with the slower transient response, due to the higher percentage of bus voltage ripple in comparison to that the case of Boost converter.

6. MOTIVATION

Almost every electronic equipment are of distinct power rating and the amazing demands of power sources for such equipment acts tense and great task to the power engineer. AC-DC active PFC converters system introduces the idea of regulated DC bus bar voltage. On power distribution and management this fulfills to the higher current desires and the dynamic characteristics of AC-DC system. For specific applications like power sources to telecom and computer servers, biomedical equipment and aeronautical engineering it is too humbling while considering high efficiency, high power density and fast dynamic response etc. But the

transfer of electrical power from power grid to the consumer-end is possible with low cost and high efficiency since Power Electronic Converter designed are leading with sophisticated appropriate control technique.

The magnetic components, are employed in converters is becoming reduced size because of the high switching operations. This reflects as advantages in cost, size and performances of power electronics and hence is popularized in commercial, industrial, military, residential and aerospace environments nowadays. In DPS implementation of galvanic isolation for protection and for the achievement of flexible system configuration is highly essential. By incorporating active PFC converters in DPS all the mentioned perfection can be achieved.

The research still in progress to accomplish better efficiency and fast dynamic response and high power inflation with stiff regulatory standards, that inspires to improve performance of the active PFC converters for DPS. With some control techniques and simple elongated PWM technique are interrogated in this thesis work. And for the improvement of power factor and THD during step change in load current and line voltage the research work is exploited in AC-DC PFC converter.

7. OBJECTIVES

To improve the power factor of the single phase AC-DC system and keeping the input current THD within a tolerable limit, irrespective of load behavior with a good dynamic response is the key objective. The above targets will be tested through;

i) Average current controlled method
ii) Peak Current controlled method
iii) PI Controlled method
iv) Dynamic Evaluation Controlled method
v) Sliding Mode Controlled method

Finally a comparative study of the above methods is to be presented.

II. Conventional Control Scheme for PFC Boost Converter

- ***Peak Current Control***
- ***Average Current Control***
- ***PI Control***

I. CONVENTIONAL CONTROL SCHEME:

There are variety of control methods, among which any one method can be used in PFC application. In general, for any control strategy for PFC, two basic feedback compensating loops are required [1-3],[20-21], [17] shown in fig. 2.1. A voltage feedback compensating loop is used as the outer loop to keep the bus voltage to a fixed DC (predefined reference) value [17][21]. An inner loop, known as current loop is to control the inductor current to a specific level and to shape the inductor current with the aim to be as alike as possible to the rectified input DC voltage keeping almost unity PF [1-3],[20-21]. The PFC power supplies with control loops implementation is employed to achieve a stable system with a tolerable dynamic behavior irrespective of the system loading conditions [21][17][1].

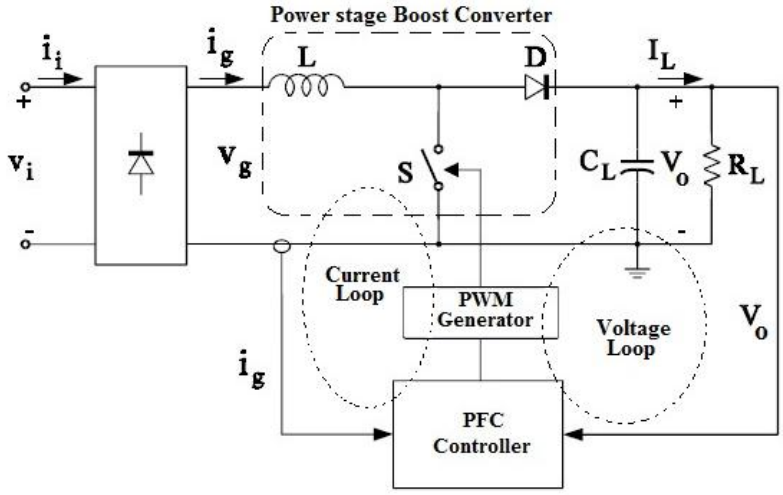


Fig. 2.1: Principle of Control Scheme of Boost PFC

In general, the PFC control strategy is categorized [2] [17] [21] as 1) Active Control Method 2) Automatic control of line current. For CCM, active control method is used, whereas, automatic control method is related to the DCM operation of the converter [2]. Several control methods are there under active control methods [1-3],[20-21],[17]. Some of them are;

1. Peak current control method
2. Average current control method
3. Charge control method
4. Hysteresis Mode Control
5. Borderline Control
6. Non-linear Carrier Control
7. Discontinuous Current PWM Control

1 PEAK CURRENT CONTROL METHOD

The switch turns on with a constant frequency and it can turn off uphill inductor current reaches a level set by the outer loop. Therefore, instant over-current switch protection is easier, but there is very noise sensitive control [1]. A compensating ramp is always required to add, when the duty cycle exceeds 0.5, otherwise the control is inherently unstable [1] [21-22].

[1][21] The switch is getting turned on with a fixed frequency by a clock signal as in fig. 2.2(a) and is turned off when the sum of the positive ramp of the inductor current (i.e. the switch current) and an external ramp (i.e. compensating ramp) touches the sinusoidal current reference as in fig. 2.2(b). Usually, this reference can be attained by multiplying a scaled replica of the rectified line voltage, V_o times the output of the voltage error amplifier, which sets the current reference amplitude. This is way for natural synchronization of the reference signal and hence reference is always proportional to line voltage, which is the condition to acquire unity power factor.

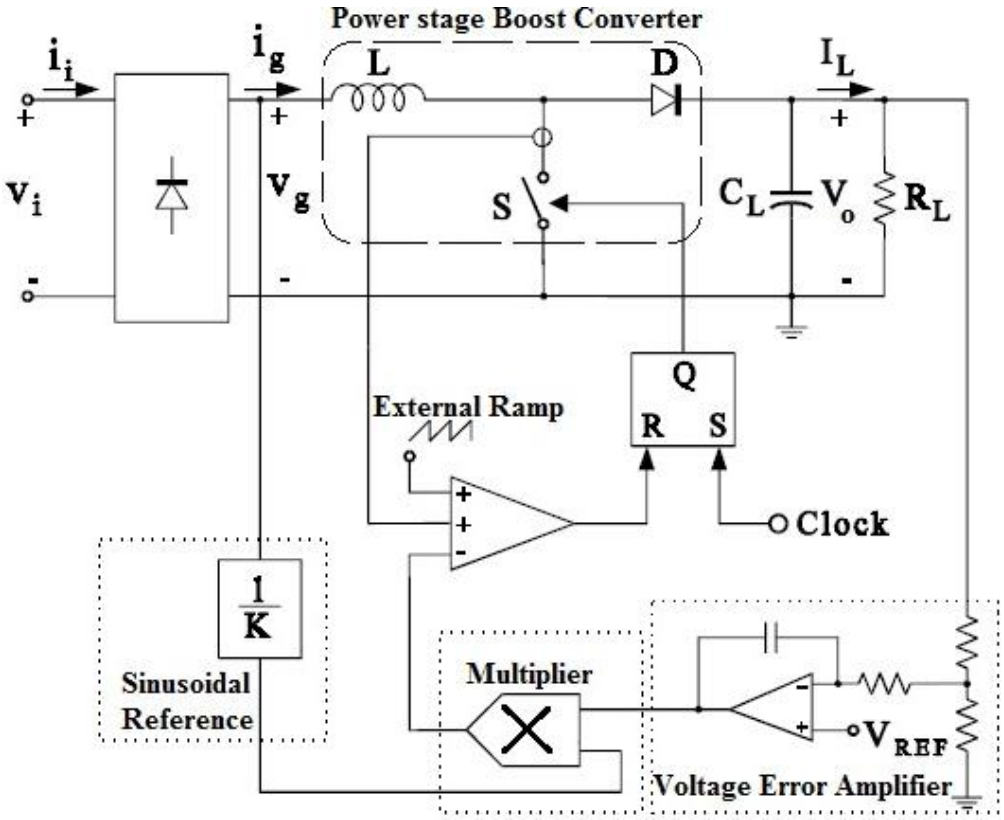
[1][21] Fig. 2.2 shows, the converter is in continuous inductor current mode operation, which implies that the devices current stress as well as reduction in input filter requirement. Furthermore, with continuous input current, the diode of the bridge can be slow devices (they operate at line frequency). On the contrary, the hard turn-off of the freewheeling diode increases losses and switching noise, calling for a faster device.

Advantages

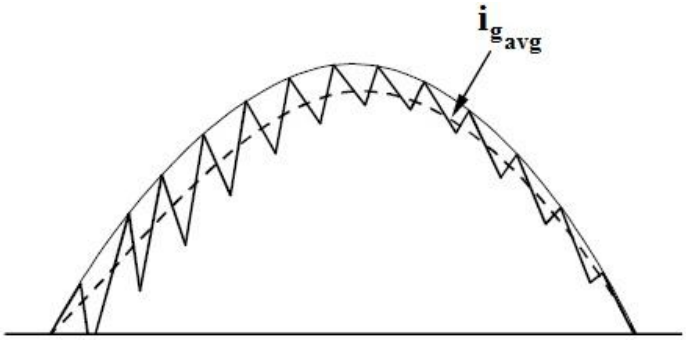
- Fixed switching frequency
- Only the switch current must be sensed, which can be accomplished by a current transformer, thus avoiding the losses due to sensing resistor.
- Current error amplifier and its compensation network are not required
- Improved reliability and increased speed response because of the instantaneous pulse-by-pulse current limit, i.e. the possibility of true switch current limiting

Disadvantages

- Presence of subharmonic oscillations, at duty cycle exceeding 0.5, so a compensating ramp is required.
- Input current distortion which increases at high line voltages and light load and is worsened by the presence of the compensation ramp [22-23].
- Control more sensitive to commutation noises.



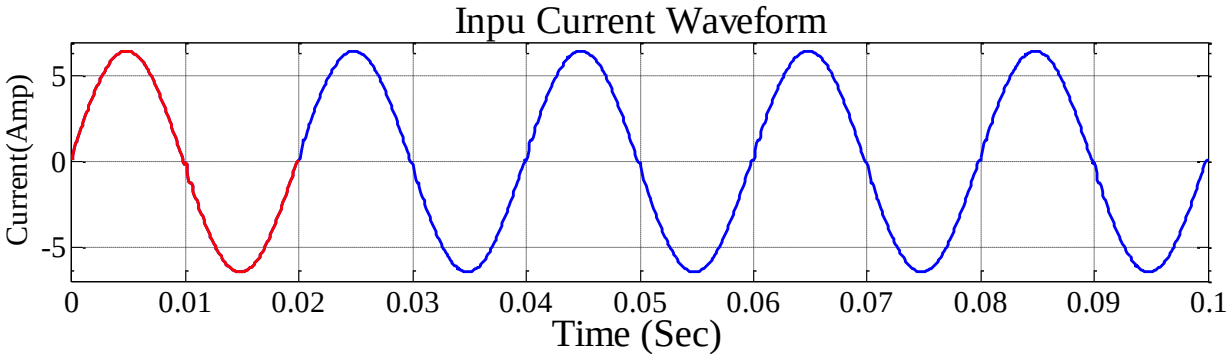
(a)



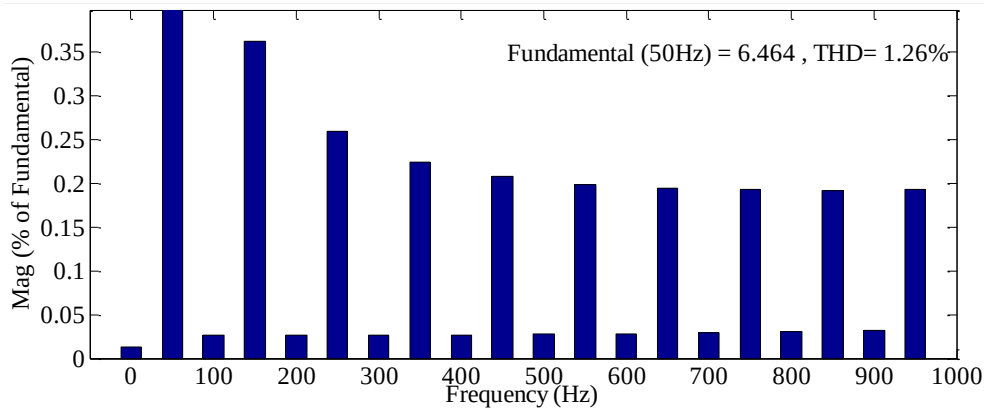
(b)

Fig. 2.2: Peak Current Control Scheme

Simulation Results



(a)



(b)

Fig. 2.3: Peak Current Controlled Boost PFC Converter: (a) Input current (b) THD for line voltage v_i=230Vrms, ,

, C_o = 0.02μF, L= 1mH operating at switching frequency 10KHz, the line current has THD=1.26% and pf=0.996

2 AVERAGE CURRENT CONTROL METHOD

Each control method has its own qualities and drawbacks based on the topology of the DC-DC converter employed in PFC converter. Now a day's average current control method is taken as a standard strategy in the industry for the boost AC-DC PFC converter, since it has merits of less THD with improved noise and easy to shape input current waveform [14] [21] [1-2].

This control method also allows a better improved input current waveform [23-25]. A current error amplifier is there as in the fig. 2.4, which filters the inductor current sensed. The output of the current error amplifier drives a PWM modulator. The inner current loop tends to reduce the error between the average input current, i_g and its reference. The latter is obtained

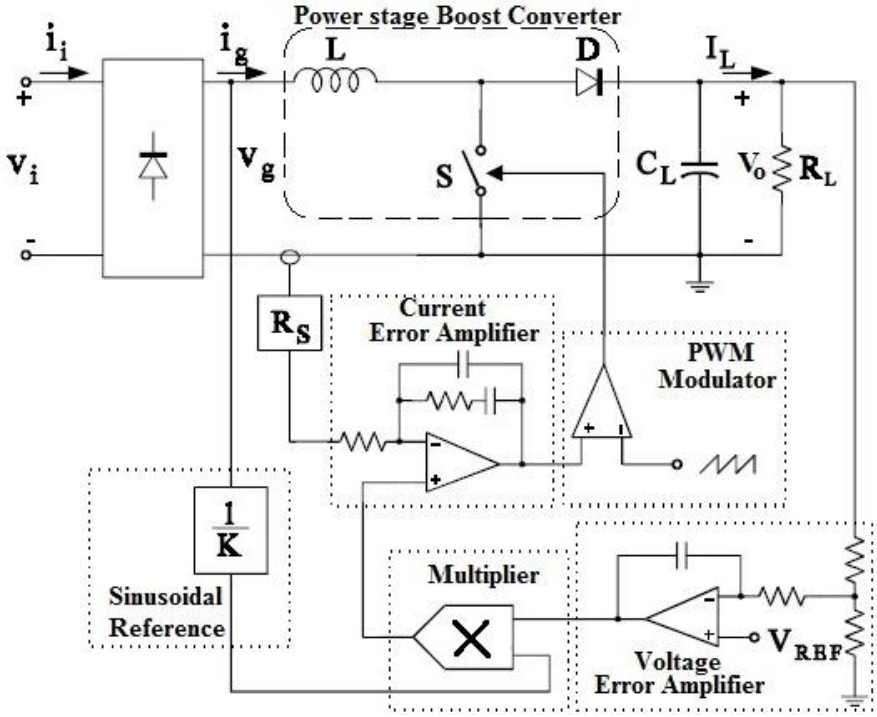
as the peak current control. Same considerations can be realized with respect to this control technique because the converter works in a continuous inductor current mode. This method overpowers the complications of the peak current control method by introducing a high gain integrating current error amplifier (CA) into the current loop [14] [21] [1-2].

Advantages

- Fixed switching frequency
- No need of external compensating ramp
- Less sensitive to communication noises, due to current filtering
- Better input current waveforms than the peak current control method because, near the zero crossing of the line voltage, the duty cycle is close to one [23].

Disadvantages

- Inductor current must be sensed.
- A current error amplifier is desirable and its compensation network design must take into account the different converter operating points during the line cycle.



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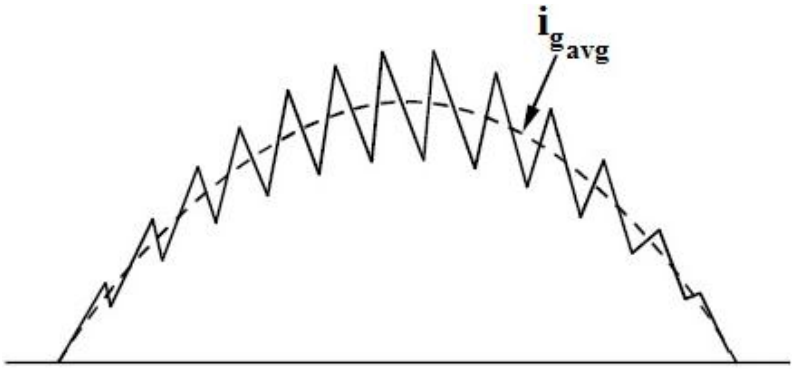
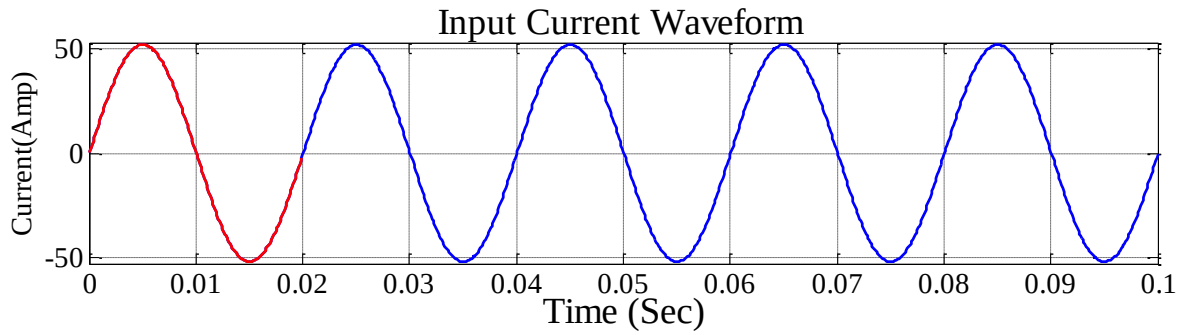


(b)

Fig. 2.4: Average Current Control Scheme

Simulation Results



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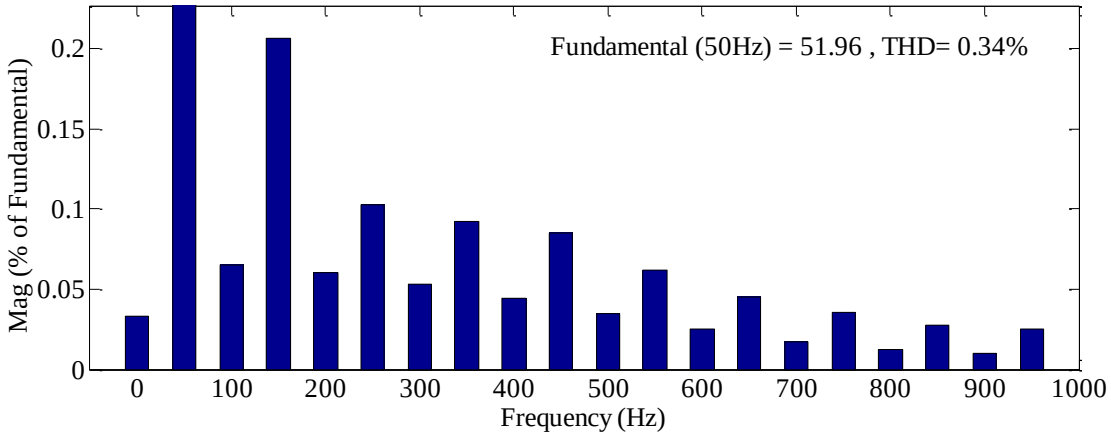


(b)

Fig. 2.5: Average Current Controlled Boost PFC Converter: (a) Input current (b) THD for line voltage v_i=230Vrms, , C_o = 0.02μF, L= 1mH operating at switching frequency 10KHz, the line current has THD=0.34% and pf=0.993

3 PI CONTROL METHOD [27-30]

For Boost PFC converter operating in PI control strategy the current loop and compensating current error amplifier are not required as for the cases of traditional linear control method for Boost PFC converter, referring to the fig. 2.1, fig. 2.2 and fig. 2.3.

[26-27] Since, the boost converter operates in two modes, for one cycle the steady state time integral of the inductor voltage can be;

$$V_g t_{on} + (V_g - V_o) t_{off} = 0 \tag{2.1}$$

$$\Rightarrow \frac{V_o}{V_g} = \frac{T_s}{t_{off}} = \frac{1}{1-D} \tag{2.2}$$

For on the state and by using Laplace transformation:

$$V_g(s) = L \times S \times I_s(s) \tag{2.3}$$

And also, Again $V_o(s) = I_s(s) \times R$ (2.4)

Therefore, basic output transfer function of the converter is;

$$\frac{V_g(s)}{V_o(s)} = \frac{L\,S}{R} \tag{2.5}$$

The use of loop feedback is essential to measure and maintain the output voltage.

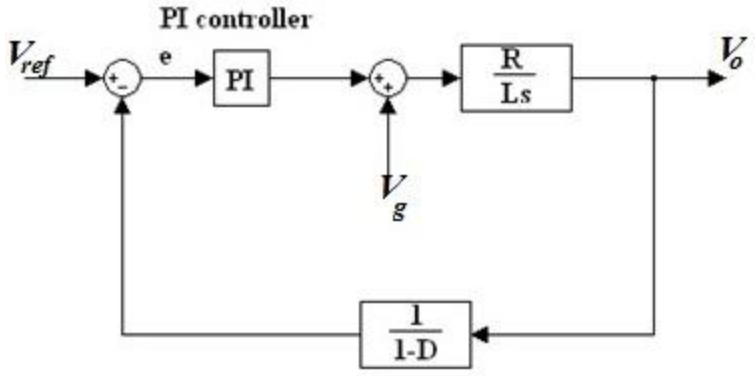


Fig.2.6: Closed Loop System Boost PFC Converter for PI Controller

[27-30] The output $V_o(s)$ is send to the PWM, the output of which is compared with V_{ref} and processed in the PI controller as in fig. 2.6, V_g is then added and given to the system.

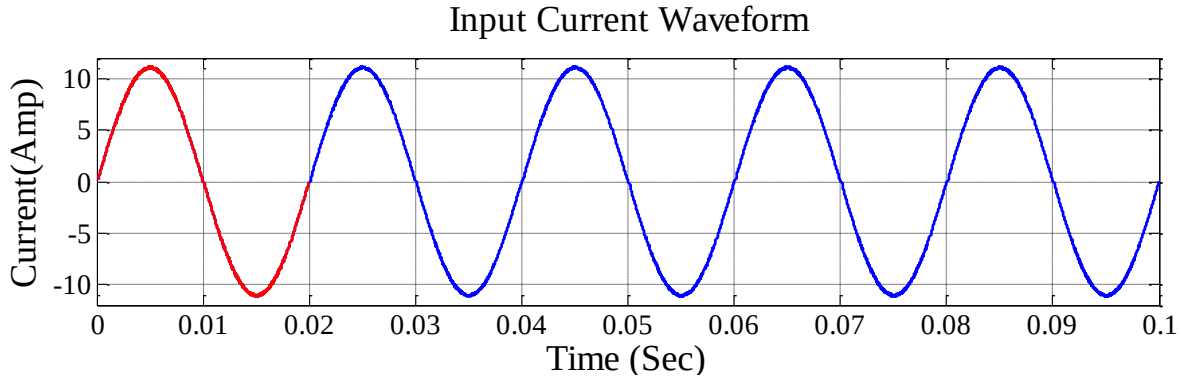
As per the fig. 2.6; $V_o = \frac{R}{Ls}\left[V_g + \left(K_p + \frac{K_i}{s}\right)e\right]$ (2.6)

$$\Rightarrow \frac{V_o(S)}{V_{in}(S)} = \frac{\frac{R}{LS}}{\left[1 + \left\{\left(\frac{R}{LS}\right)\left(K_p + \frac{K_i}{S}\right)\left(\frac{1}{1-D}\right)\right\}\right]} \quad (2.7)$$

Considering $V_{ref} = 0$;

$$V_o + \left[\frac{R}{Ls}\left(K_p + \frac{K_i}{s}\right)\left(\frac{1}{1-D}\right)V_o\right] = V_{in}\frac{R}{Ls} \quad (2.8)$$

Simulation Results



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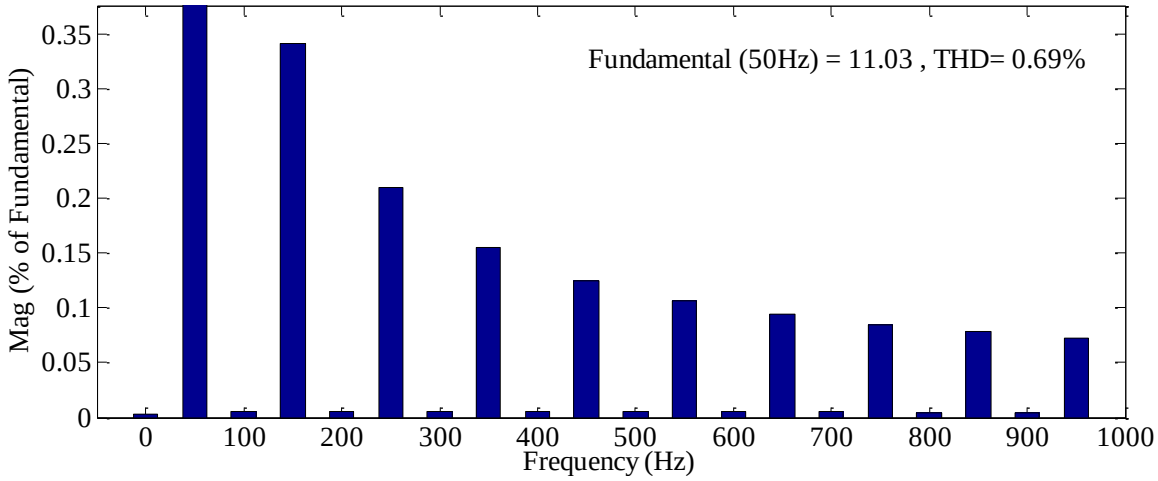
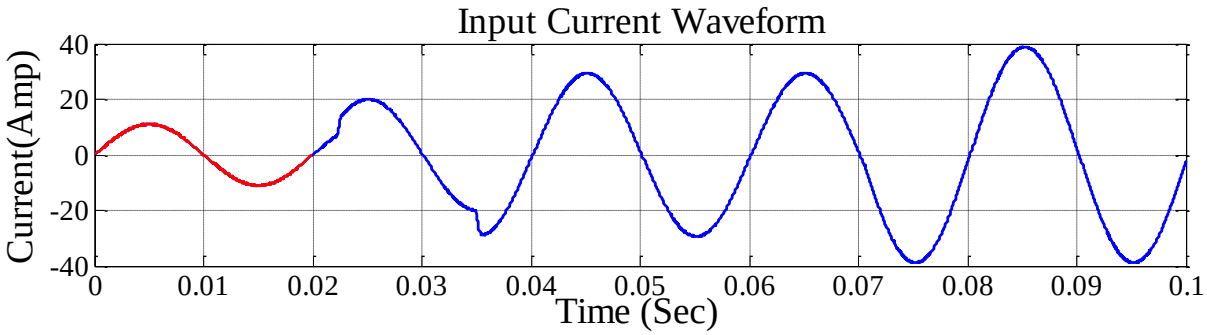
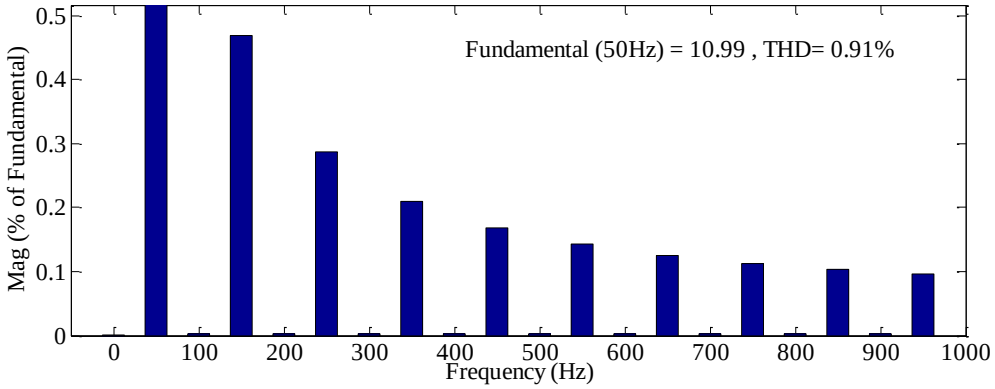


(b)

Fig. 2.7: PI Controlled Boost PFC Converter: (a) Input current (b) THD for line voltage v_i=230Vrms , C_o = 0.02μF, L= 1mH operating at switching frequency 10KHz, the line current has THD=0.69% and pf=0.9909 (K_p = 1.8 and K_i = 0.004 are taken)



(a)



(b)

Fig. 2.8: PI Controlled Boost PFC Converter: (a) Input current (b) THD for line voltage v_i=230Vrms, C_o = 0.02µF, L= 1mH operating at switching frequency 10KHz, the line current has THD=0.91% and pf=0.9909 (K_p = 1.8 and K_i = 0.004 are taken) (LOAD1, LOAD2, LOAD3 and LOAD4 are connected to the output terminals one after another at t= 0sec, 0.0223 sec, 0.035 sec and at 0.07 sec

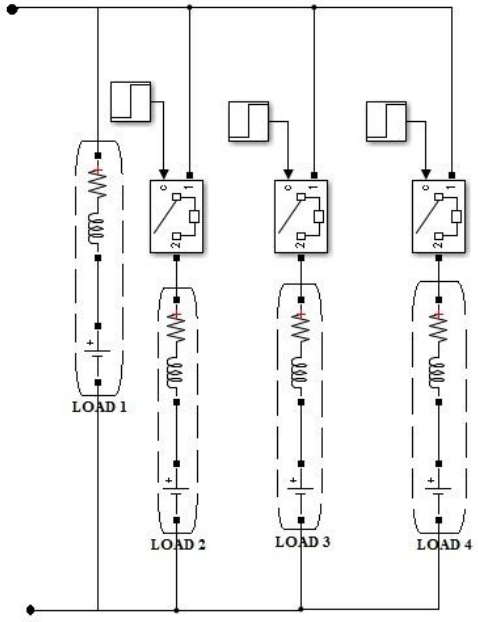


Fig. 2.9: Time Varying Load for Boost PFC Converter AC-DC System

III. Nonlinear Control Technique for PFC Boost Converter

- ***Dynamic Evolution Control***
- ***Sliding Mode Control***
- ***Summary***

III. NONLINEAR CONTROL SCHEME:

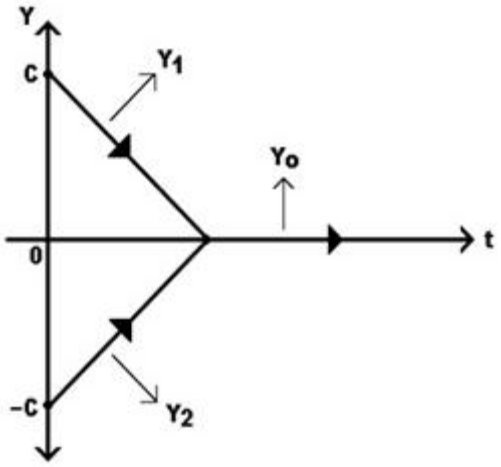
The Boost converter always needs extensive operating conditions and fast response, which is satisfactorily impossible by conventional PWM current mode controller. The nonlinear controllers offer control backing in this regards. In comparison to the conventional current mode controllers the nonlinear controller is able to provide:

- Comparable fast dynamic responses
- Inherent robust features with fixed operating frequency
- Stable for large operating range
- Least deviation of settling time over wide operating range
- Low overshoots voltage relatively over wide operating range

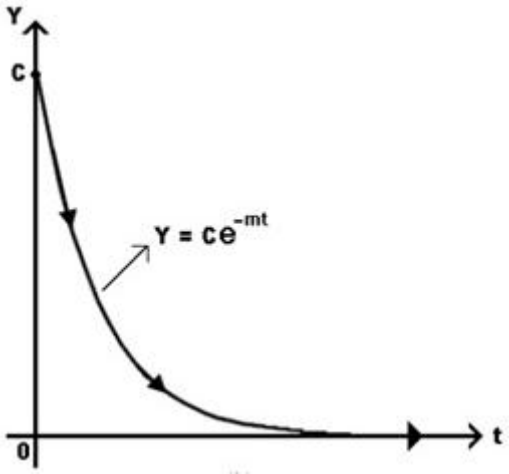
1 DYNAMIC EVOLUTION CONTROL METHOD [32-34]

This is a new approach for boost DC-DC converter controller implemented for Boost PFC technique. This control method adventures the non-linearity and time varying properties of the system and hence, a superior control method [31] -[34]. Some major limitations of linear control methods are overcome by this method, since it uses the dynamic equation model of the converter explicitly [31] -[34].

Feedback control needs an operation that, in the existence of disturbances, the difference between the output of the system and the reference must be tended to zero [35]. The key principle of the Dynamic Evolution Control technique is, "The *Error State*, i.e., the difference between the output system and the reference input must be reduced to zero", without loss of generality. The elementary idea is the minimization of *State Error* by driving the state error to follow the definite track, which ensure the Null condition of *Error State* in increase of time. The target of the controller is to monitor the dynamic characteristic of the system to work on the governing equation $Y=0$. The evolution track can be a function of a linear path or of an exponential path as in fig. 3.1. For the Boost PFC converter, the linear evolution path is chosen for the controller.



(a)



(b)

Fig.3.1: (a) Linear Evolution Path (b) Exponential Evolution Path

$$Y_1 = C - mt \tag{3.1}$$

$$Y_2 = -(C - mt) \tag{3.2}$$

$$Y_0 = 0 \tag{3.3}$$

where *C* is the initial value and *m* is the slope.

In fig.3.1 (a), the value of *Y* decreases linearly to zero as a function of time by following either path Y_1 or path Y_2 based on positive or negative initial value of *Y* respectively. Y_1 path is being followed, it the initial value is positive, whereas for negative initial value of *Y*, path Y_2 is being followed. The linear decrease speed of *Y* value is proportional to the reduction rate of slope *m*. The value of Y follows the Y_0 path after reaching zero position, i.e. Y = 0.

For fig.3.1 (a) and from equations 3.1, 3.2 and 3.3 the generalized equation is;

$$Y = (C - mt)u \tag{3.4}$$

Here *u* is considered as the specific coefficient of the *Y* and *u* is given as;

$$u = \frac{Y}{|Y|} = \begin{cases} -1, & for\ Y < 0 \\ 0, & for\ Y = 0 \\ +1, & for\ Y > 0 \end{cases} \tag{3.5}$$

Considering *Y* as the error state function of the converter and *C* is the initial value, the equation 3.4 represents the dynamic evolution of the state error function(*Y*), which is enforced to follow the evolution path as in the fig. 3.1 (a).

The state error function *Y* is driven decrease to zero linearly with decrease rate *m*, therefore, from equation 3.4, the derivative of *Y* can be written as;

$$\frac{dY}{dt} = -mu \tag{3.6}$$

$$or, \qquad \frac{dY}{dt} + mu = 0 \tag{3.7}$$

From equation 3.4 and 3.7, the dynamic evolution function can be written as;

$$|Y|\frac{dY}{dt} + mY = 0, \qquad m > 0 \tag{3.8}$$

Now, the leading aim is to formulate a control law, which ensures the zero position of state error function (*Y*) of Boost PFC converter as well as the control law should guarantee the follow up of state error function (*Y*) to the evolutionary path. For DC-DC converter, this control law signifies as the duty cycle equation $\alpha(V_o, V_g, i_L)$.

[32-34] Considering the average model of the PWM switch [36], the dynamic equation for Boost PFC converter is;

$$V_g = L\frac{di_L}{dt} + V_o(1 - \alpha), \qquad 0 < \alpha < 1 \tag{3.9}$$

$$\Longrightarrow V_o = V_g + V_o\alpha - L\frac{di_L}{dt} \tag{3.10}$$

[32-34] The dynamic evolution and synthesis of control expression starts by defining the error state function (*Y*) as;

$$Y = kV_{err} \tag{3.11}$$

where k is taken positive coefficient and V_{err} is the error voltage.

$$\Longrightarrow \frac{dY}{dt} = k\frac{dV_{err}}{dt} \tag{3.12}$$

Substitution of equations 3.12 and 3.11 in equation 3.8 gives;

$$|kV_{err}|k\frac{dV_{err}}{dt} + mkV_{err} = 0 \tag{3.13}$$

$$\Longrightarrow |kV_{err}|k\frac{dV_{err}}{dt} + (mk-1)V_{err} + V_{ref} = V_o \tag{3.14}$$

Substituting the equation 3.10 into 3.14, we get;

$$\Longrightarrow |kV_{err}|k\frac{dV_{err}}{dt} + (mk-1)V_{err} + V_{ref} = V_g + V_o\alpha - L\frac{di_L}{dt} \tag{3.15}$$

Resolving equation 3.15 for duty cycle, the control law can be obtained as;

$$\alpha = \frac{|kV_{err}|k\frac{dV_{err}}{dt} + (mk-1)V_{err} + L\frac{di_L}{dt} + V_{ref} - V_g}{V_o} \tag{3.16}$$

Rearranging the equation 3.16, we get the control law as;

$$\alpha(V_o, V_g, i_L) = \frac{V_{ref} - V_{in}}{V_o} + \frac{(mk-1)V_{err}}{V_o} + \frac{|kV_{err}|k\frac{dV_{err}}{dt}}{V_o} + \frac{L\frac{di_L}{dt}}{V_o} \tag{3.17}$$

The equation 3.17 represents the duty cycle of Boost PFC converter. The derived expression of duty cycle, $\alpha(V_o, V_g, i_L)$ works as the control action. This equation enforces the state error function (Y) to fulfill the dynamic evolution function 3.8. Subsequently, the state error function (Y) is compulsory to make evolution by ensuing equation 3.4 and reduce to zero ($Y = 0$) with a decrease rate m. So the state error function (Y) obeys the equation $Y = kV_{err} = 0$. Thus the error state reaches to zero,

$$V_{err} = 0 \tag{3.18}$$

Taking $V_{err} = V_{ref} - V_o$, we get $V_o = V_{ref}$ (3.19)

The equation 3.18 explains that the output of the converter converges to the steady state of the converter. As per the synthesis process is concerned, the dynamic evolution controller can be worked for complete non-linear system without any requirement of any simplification and linearization on system model, which is essential for natural control techniques.

All the four terms of the control law equation 3.17 have their own specialty. The first one is the feedforward term, second and third terms are represented as the proportional and derivative terms of the alarm in the output voltage and the last term is the derivative term of the inductor current.

By using the duty cycle equation the preferred value of the signal level control $V_{control}$ can be calculated, comparison of which with a repeating signal, V_{st} of constant peak creates PWM signal as in fig. 3.2. The dynamic evolution control operates at constant frequency since the frequency of V_{st} is kept constant.

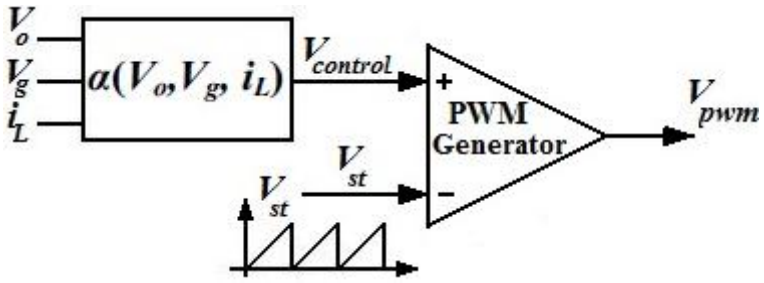
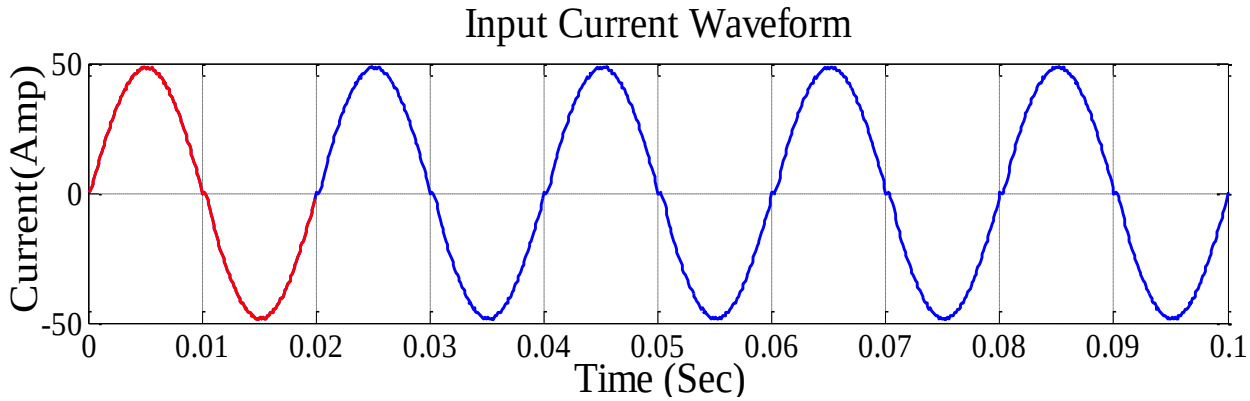


Fig. 3.2: PWM Signal Generator



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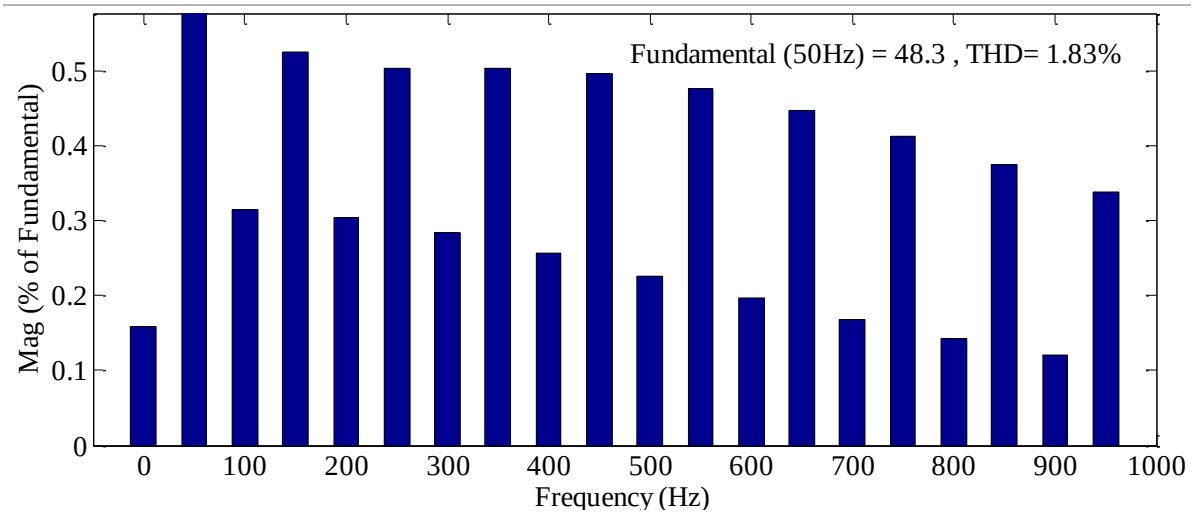


(b)

Fig. 3.3: Dynamic Evolution Controlled Boost PFC Converter: (a) Input current (b) THD for line voltage v_i=230Vrms, output voltage V_o = 350V DC, C_o = 0.02μF, L= 1mH operating at switching frequency 10KHz, the line current has THD=1.83% and pf=0.998

2 SLIDING-MODE CONTROL [37-42]

Technically, this controller has a time-varying state-feedback discontinuous control law due to which switching from one continuous structure to another according to the existing situation of the state variables in the state space is possible with high frequency. The objective is to enforce the dynamics of the system under control to follow the desired and pre-determined [37].

Sliding mode current controller technique is implemented for PFC boost converter. Fig. 3.4 represents the basic circuit diagram of PFC Boost converter governed by sliding mode controller. This control scheme for PFC boost converter begins with the selection of sliding surface [37-41]. The continuous increase in current makes the direct surface $v_o - V_{ref}$ nearly to zero [41]. By using two cascaded control loops to achieve it. From the voltage error the outer voltage loop produces the reference current. The stability criteria and existence of sliding mode can be achieved by controlling the output voltage of AC-DC converter. The inductor current is controlled by the inner current loop through sliding mode technique. For the regulation of current SMC is used, due to which voltage loop is highly sensitive to the

high frequency switching and to the uncertainties in the reference current [38][41]. Therefore, for improved performance the sliding surface is;

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 \tag{3.20}$$

where α_1, α_2 and α_3 are the control parameters, generally stated as sliding coefficients and x_1, x_2 and x_3 are called as the desired state feedback variables which are to be controlled.

$$\begin{cases} x_1 = i_{ref} - i_g' \\ x_2 = V_{ref} - \beta v_o \\ x_3 = \int (x_1 + x_2) dt \end{cases} \tag{3.21}$$

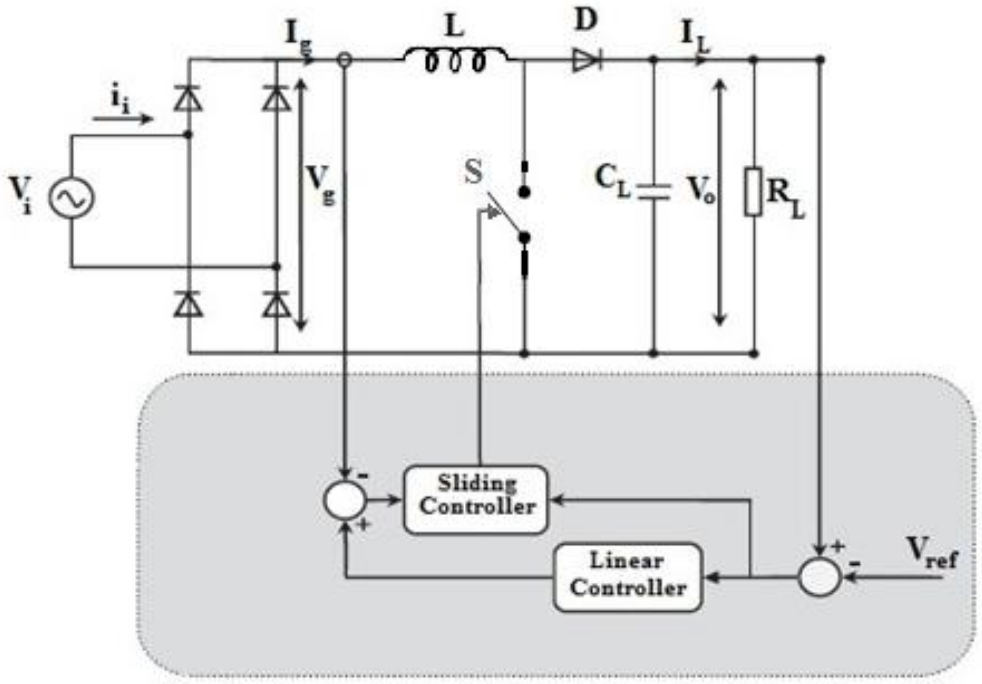


Fig. 3.4: Boost PFC Converter operated by Sliding Mode Controller

[37-39] In the SM current controller only the controlled variables x_1 (Current error) and x_2 (Voltage error) are essential for high frequency operation which ensures on regulation of both the output voltage and inductor current hence they follow their references precisely.

The switching function for logic state of power switch S is;

$$u = \frac{1}{2}\left(1 + sign\,(S)\right) \tag{3.22}$$

For SM operation, three necessary conditions are namely the hitting, existence, and stability conditions. Resulting control function for hitting condition;

$$u = \begin{cases} 1 =' ON' & when\ S > 0 \\ 0 =' OFF' & when\ S < 0 \\ unchanged & otherwise \end{cases} \tag{3.23}$$

Considering the continuous conduction of PFC boost converter and by time differentiation, from equation 3.21, the system dynamic model is;

$$\begin{cases} \dot{x_1} = \dfrac{d\left[i_{ref} - i_g{}'\right]}{dt} = \dfrac{\beta K}{C} i_C - \dfrac{v_g - \bar{u} v_o}{L} \\ \dot{x_2} = \dfrac{d\left[V_{ref} - \beta v_o\right]}{dt} = -\dfrac{\beta}{C} i_C \\ \dot{x_3} = x_1 + x_2 = (i_{ref} - i_g{}') + (V_{ref} - \beta v_o) \\ \quad = (K+1)\left[V_{ref} - \beta v_o\right] - i_g{}' \end{cases} \tag{3.24}$$

Where $\bar{u}$= 1 – *u*, is considered as inverse logic of *u*.

By solving the equation $\frac{dS}{dt} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} + \alpha_3 \dot{x_3} = 0$ the equivalent control signal would be;

$$u_{eq} = 1 - \frac{K_2}{v_o} i_C - \frac{v_g}{v_o} + \frac{K_1}{v_o}\left[V_{ref} - \beta v_o\right] - \frac{K_3}{v_o} i'_g \tag{3.25}$$

Where K_1, K_2 and K_3 are the fixed gain parameters.

$$\begin{cases} K_1 = \dfrac{\alpha_3}{\alpha_1} L(K+1) \\ K_2 = \dfrac{\beta L}{C}(K + \dfrac{\alpha_2}{\alpha_1}) \\ K_3 = \dfrac{\alpha_3}{\alpha_1} L \end{cases} \tag{3.26}$$

$u_{eq} = (0,1)$ and it can be represented in terms of the controlled state variable like as;

$$u_{eq} = 1 - \frac{K_2 \frac{v_o}{r_L} - v_i + K_3\left[V_{ref} - \beta v_o\right] - K_3\left(i_{ref} - i'_g\right)}{K_2 i'_g - v_o} \tag{3.27}$$

From the sliding surface 3.20, the controller is driven and is executed through a PWM, comparing $u_{eq} = d$ (duty ratio of the PWM controller). The control law equation is described as in fig.3.5, involving;

$$\begin{cases} \text{a control signal } v_C = G_S K_1\left[V_{ref} - \beta v_o\right] - G_S K_2 i_C - G_S K_3 i'_g + G_S[v_o - v_g] \\ \text{a ramp } v_{ramp} = G_S v_o \end{cases} \quad (3.28)$$

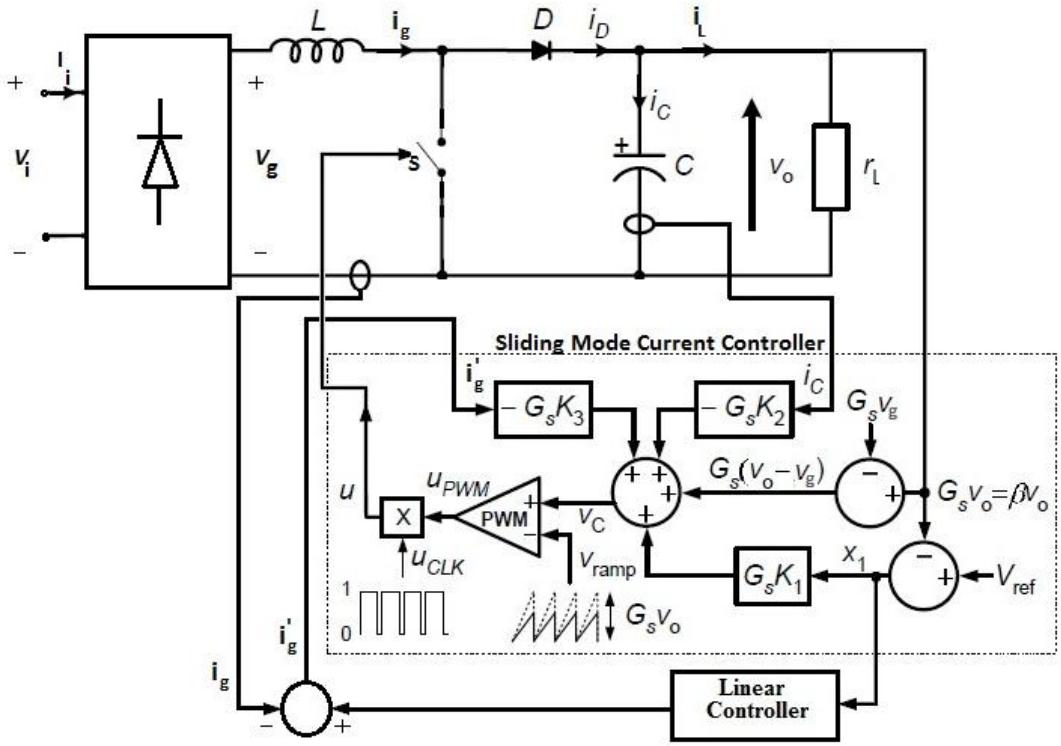


Fig.3.5: Boost PFC Converter describing Sliding Mode Control Law

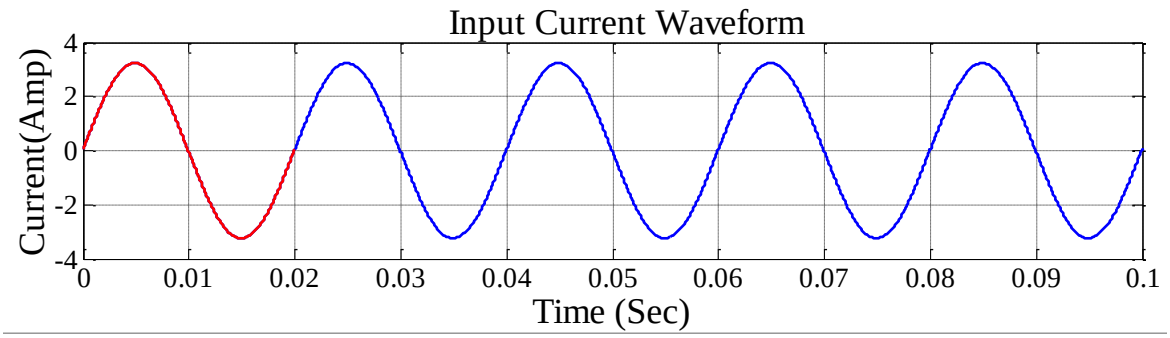
The factor $G_S = (0,1)$, is introduced purposefully to down scale the equation to a practical level of magnitude. To make the duty ratio of the output of the controller always below 1, a multiplier is incorporated for the multiplication of u_{PWM} and u_{CLK}. By a logic AND operator the impulse generator creates u_{CLK}. Based on equation 3.28, the controller is designed with assuming $\beta = G_S$.

The selection of appropriate switching function gives satisfied hitting condition. To attain existence condition $lim_{S\to 0}\, S.\dot{S} < 0$, which is essential. This can be obtained form the equation 3.20 and from its time derivative as below;

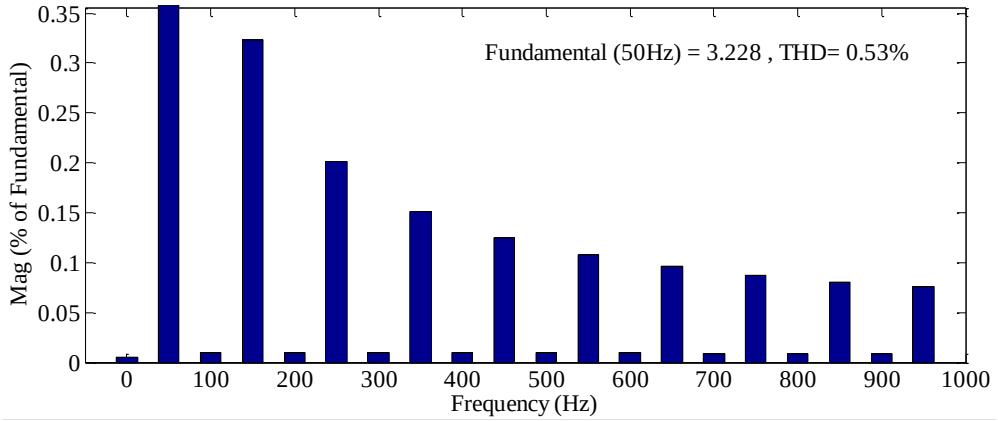
$$\begin{cases} \alpha_1\left[-\frac{\beta K}{C} i_C - \frac{v_g}{L}\right] - \alpha_2 \frac{\beta}{C} i_C + \alpha_3\left((K+1)\left[V_{ref} - \beta v_o\right] - i'_g\right) < 0 \\ \alpha_1\left[-\frac{\beta K}{C} i_C - \frac{v_g - v_o}{L}\right] - \alpha_2 \frac{\beta}{C} i_C + \alpha_3\left((K+1)\left[V_{ref} - \beta v_o\right] - i'_g\right) > 0 \end{cases} \quad (3.29)$$

[37-39] [42] The control law and the sliding gain coefficients should be designed in such to fulfill the stability condition. This is to make sure that the trajectory is directed by the desired sliding manifold and always towards a stable equilibrium point.

Simulation Result

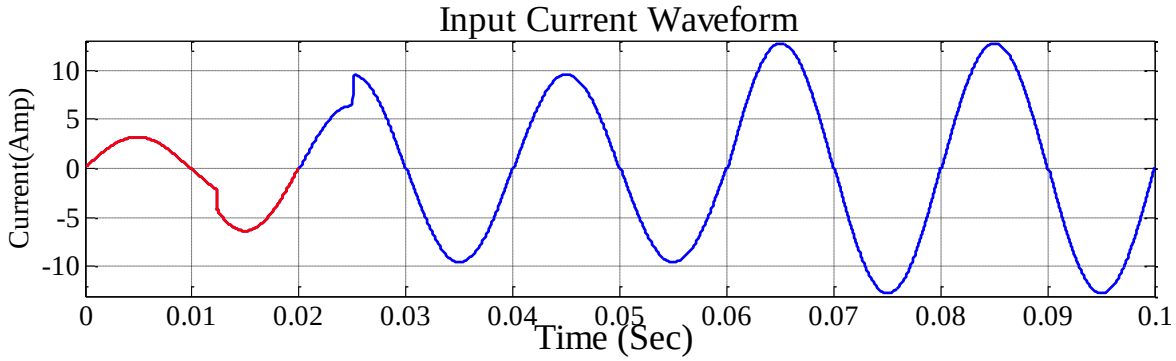


(a)

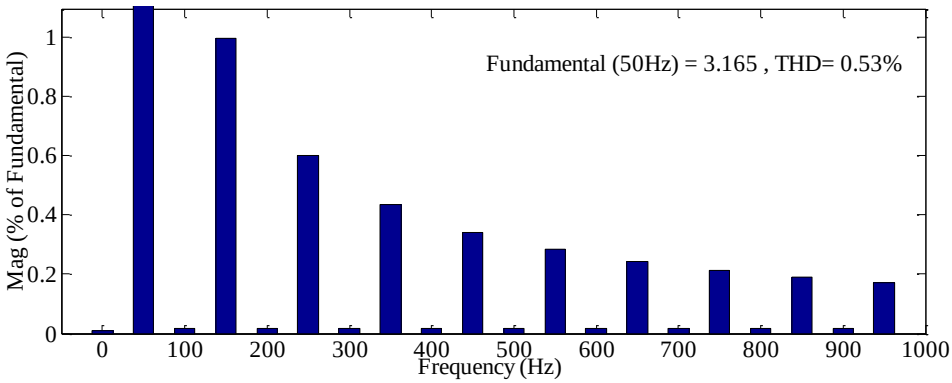


(b)

Fig.3.6: Sliding Mode Controlled Boost PFC Converter (a) Input Current (b) THD for line voltage v_i=230Vrms, C_o = 0.02μF, L= 1mH operating at switching frequency 10KHz, the line current has THD=0.53% and pf=0.9998



(a)



(b)

Fig.3.7: Sliding Mode Controlled Boost PFC Converter (a) Input Current (b) THD for line voltage v_i=230Vrms, C_o = 0.02μF, L= 1mH operating at switching frequency 10KHz, the line current has THD=0.53% and pf=0.9998 (LOAD1, LOAD2, LOAD3 and LOAD4 are connected to the output terminals one after another at t= 0sec, 0.0123 sec, 0.035 sec and at 0.07 sec

IV. Conclusion and Future Scope

- ***Conclusion***
- ***Future Scope***

IV. CONCLUSION AND FUTURE WORK:

1. CONCLUSION

The line current harmonics minimization is essential to comply with the standard resulting in increase in degree of utilization of the grid power. This is discussed as the Power Factor Correction-PFC, in general.

PFC is a technique of counteracting the undesirable effects of electric *loads* that create a power factor (PF) less than 1.

There are numbers of technique for PFC. Based on the selection electric element to filter out the harmonics and to get nearly unity input power factor, the PFC technique is categorized into "*active*" and "*passive*" PFC method.

The "*passive PFC"* circuit uses low-frequency filter components to reduce harmonics. Moreover, in this technique power factor cannot be highly improved and output voltage is not controllable. Active switches are used in association with reactive element for *"Active PFC approach"* for the improvement of line current shape and to obtain controllable output voltage. For this DC-DC converter is employed and is operated at high frequency to shape the line current waveform as sinusoidal as possible.

In *"Active PFC approach",* the Boost PFC converter is taken (since it has significant advantages as discussed in chapter-I) with suitable switching control strategy. There are variety of control methods, among which any one method can be used in PFC application. In general, for any control strategy for PFC, two basic feedback compensating loops are required. A voltage feedback compensating loop is used as the outer loop to keep the bus voltage to a fixed DC (predefined reference) value. An inner loop, known as current loop is to control the inductor current to a specific level and to shape the inductor current with the aim to be as alike as possible to the rectified input DC voltage keeping almost unity PF. The PFC power supplies with control loops implementation is employed to achieve a stable system with a tolerable dynamic behavior irrespective of the system loading conditions.

Using some conventional control methodologies and some nonlinear control techniques the non-sinusoidal input current is converted into sinusoidal with improved THD and their advantages and limitations based on constraints are discussed.

Some conventional control schemes are taken;

1. Peak current control
2. Average current control
3. PI control

Some nonlinear control schemes are taken;

1. Dynamic Evolution control
2. Sliding Mode control

Nearly unity power factor with tolerate percentage of THD of the input line current is observed for Boost PFC converter operating in above control methods. The Table 2 explains about the obtained power factor and THD for the Boost PFC converter with constant R-Load, operating with different control schemes. Whereas, for PI Controlled operating and Sliding Mode Controlled operating Boost PFC converter with time varying R-L-E-Load the obtained power factor and THD are analyzed.

Table 4.1: PF and THD of AC-DC System with R-Load Operating in Different Control Method

AC-DC System with Constant R- Load			
AC-DC System		**Pf**	**THD (%)**
Without filter & converter		0.9396	99.94
With Converter & with Filter	Peak Current Control Method	0.996	1.26
	Average Current Control Method	0.993	0.34
	PI Control	0.9909	0.73
	Dynamic Evolution Control	0.998	1.83
	Sliding Mode Control	0.9998	0.53

Table 4.2: PF and THD of AC-DC System with R-L-E-Load Operating with Different Controller

AC-DC System with Time Varying R-L-E Load		
Boost PFC Converter with	**Pf**	**THD (%)**
PI Control	0.9988	0.91
Sliding Mode Control	0.9998	0.53

Even though peak current control gives better characteristics, it has several drawbacks, such as: poor noise immunity, need of slope compensation, peak to average current error. These problems can be eliminated by average current control at the cost of increased circuit complexity.

For faster dynamic responses and large stable operating range any suitable nonlinear control scheme can be adopted for Boost PFC converter.

The dynamic evolution controller can be worked for complete non-linear system without any requirement of any simplification and linearization on system model, which is essential for natural control techniques, since the control law carries feedforward term, proportional and derivative terms of the alarm in the output voltage and another derivative term of the inductor current.

In sliding mode control method the trajectory is directed by the desired sliding manifold and always towards a stable equilibrium point, hence dynamically highly stable.

2. FUTURE SCOPE

For this work the Boost PFC Converter with different controllers are realized with the help of MATLAB/Simulation, which can be analyzed in real time simulator for the consideration of practical applications. Also, the hardware implementation can be realized practically with suitable control technique.

The switching losses can be considered and suitable soft switching technique can be introduced.

Some special suitable optimization technique can be employed to ensure the very high dynamic stability and very wide stable operating range.

REFERENCES

[1] Ms. Kurma Sai Mallika,"*Topological Issues in Single Phase Power Factor Correction*", Thesis, Degree of Master of technology In Power control and drives, Department of electrical engineering National institute of technology Rourkela-769008, 2007

[2] Matada Mahesh, "*Performance improvement of ac-dc power factor correction converters for distributed power system*", Thesis, Degree of Doctor of Philosophy Under the supervision of Prof. Anup Kumar Panda, NIT, Rourkela, Oct 2011

[3] Yiqing Zhao, "*single phase power factor correction circuit with wide output voltage range*", Thesis, Degree of Master of Science, Electrical Engineering, Fred C. Lee, Chairman, Dusan Borojevic, Dan Y. Chen, February 6, 1998, Blacksburg, Virginia

[4] M. Mankinkar, "Power supplies' energy business/ revenue models", *in Proc. IEEE Applied Power Electron., Conf. (APEC'06), pp. 3-5, 2006*

[5] F. C. Lee, P. Barbosa, Peng xu, J. Zhang, B. Yang and F. Canales, "*Topologies and design considerations for distributed power system applications", in Proc IEEE, vol. 89, no. 6, June 2001, pp. 939-950.*

[6] "*Limits for harmonic current emissions (equipment input current <16A per phase)." IEC 1000/3/2 International Standard. (1995).*

[7] "*IEEE 519 Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems." IEEE Industry Applications Society/ Power Engineering Society. (1993).*

[8] "*IEEE 519 Recommended Practices and Requirements for Harmonic Control in Electric Power Systems," Tech. Rep., IEEE Industry Applications Soc./Power Engineering Soc.,1993.*

[9] N. Mohan, et el. *Power Electronics: Converters, Applications, and Design*. New York: NY, USA, John Wiley & Sons, Inc., 1995.

[10] Kelley, Arthur W, et el. "*Rectifier Design for Minimum Line Current Harmonics and Maximum Power Factor", IEEE Trans. on Power Electronics. vol. 7, no. 2,(Apr 1992): pp. 332-341.*

[11] Redl, Richard, "*An Economical Single-phase Passive Power-Factor-Corrected Rectifier: Topology, Operation, Extensions, and Design for Compliance." Proc. of IEEE Applied Power Electronics Conference, APEC'98. (1998): pp. 454-460.*

[12] Basu, Supratim, et el. "*PFC Strategies in light of EN 61000-3-2*." Bose Research Pvt. Ltd., Bangalore, India. Paper identification number A123656. (2004): pp. 1-9.

[13] Sum, K. Kit, "*Improved valley-fill passive power factor correction current shaper approaches IEC specification limits*" PCIM Magazine. (Feb. 1998): pp. 42-51.

[14] Y. Zaohong, and P. C. Sen, "*Recent developments in high power factor switch-mode converters", in Proc. IEEE-Elect. & Computer Engg., Conf., vol. 2, 1998, pp. 477-480.*

[15] C. Qiao, and K. M. Smedley, "*A topology survey on single-stage power factor corrector with a boost type input-current-shaper," IEEE Trans. Power Electron., vol. 16, no. 3, pp.360-368, May 2011.*

[16] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "*Single phase power factor correction: A survey," IEEE Trans. Power electron., vol. 18, no. 3, pp. 749-755, May 2003.*

[17] K. Liu, and Y. Lin, "*Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters," in Proc. Power Electron. Spec. Conf. (PESC'89), 1989, pp. 533-540.*

[18] Ned Mohan, Tore M. Undeland, William P. Robbins, "*Power Electronics: Converters, Applications, and Design, 3rd Edition", September 2002, ©2003, Book, ISBN: 978-0-471- 22693-2, 824 pages*

[19] Bernard Keogh, "*Power Factor Correction Using the Buck Topology—Efficiency Benefits and Practical Design Considerations*", 2010 Texas Instruments Power Supply Design Seminar SEM1900, Topic 4 TI Literature Number: SLUP264

[20] A. El Aroudi, R. Haroun, Cid-Pastor, L.M. Salamero, "*Suppression of Line Frequency Instabilities in PFC AC-DC Power Supplies by Feedback Notch Filtering the Pre-Regulator Output Voltage," IEEE Trans. On Circuit and Systems-I: Regular Papers, Vol.60, No.3, March 2013*

[21] L. Rossetto, G. Spiazzi, and P. Tenti, "*Control techniques for power factor correction converters*" in *Proc. Intrl. Conf. on Power Electron., and Motion Control*, Warswaw, Sept. 1994, pp. 1310-1318.

[22] Redl, Richard, "*Reducing distortion in peak-current-controlled boost power factor correctors." Proc. of IEEE Applied Power Electronics Conference, APEC'94. (1994):p.576-583.*

[23] Zhou, C., et el. "*Design Trade-offs in Continuous Current-mode Controlled Boost Power-Factor Correction Circuits*" HFPC Conf. proc. (1992): pp. 209-220.

[24] C. Silva, "Power Factor Correction with the UC3854," Application Note, Unitrode Integrated Circuit.

[25] Andreycak, B., "*Optimizing Performance in UC3854 Power Factor Correction Applications*" Unitrode, Products & Applications Handbook. (1993/94.)

[26] http://en.wikipedia.org/wiki/Boost_converter

[27] Mohammed, B. M Hasaneen, and Adel A. Elbaset. "*Design and Simulation of DC-DC Boost Converter*", 2008

[28] Mitulkumar R. Dave, K.C.Dave, "*Analysis of Boost Converter Using PI Control Algorithms", International Journal of Engineering Trends and Technology- Volume3Issue2- 2012*

[29] Copeland, Brain R. "*The Design of PID Controllers using Ziegler Nichols Tuning*", 2008.

[30] D.P.Eckman, *Automatic Process Control.* New Delhi: Wiley Eastern,1992

[31] A. Kolesnikov, G. Veselov,A. Kolesnikov, A. Monti,F.Ponci,E.Santi and R. Dougal,"Synergetic Synthesis of DC-DC Boost Converter Controllers: Theory and Experimental Analysis", IEEE APEC 2002, pp.409-415,March 2002

[32] A.S. Samosir,A.H.M Yatim,"*Implementation of New Control Method based on Dynamic Evolution Control with Linear Evolution Path for Boost DC-DC Converter", 2nd IEEE International Conf. on Power and Energy (PECon 08), December 1-3, 2008, Johar Baharu, Malaysia*

[33] A.S. Samosir,A.H.M Yatim, "*A New Control Method Based on Dynamic Evolution Control for Power Converter*", TENCON, Nov. 2008

[34] A.S. Samosir,A.H.M Yatim, "*Dynamic Evolution Control of Bidirectional DC-DC Converter for Interfacing Ultracapacitor Energy Storage to Fuel Cell Electric Vehicle System*", AUPEC, Dec. 2008

[35] K. Ogata, "Modern Control Engineering", Prentice-Hall, inc. 1997

[36] V. Vorperian, "*Simplified Analysis of PWM Converters Using Model of PWM Switch", IEEE Transaction on Aerospace and Electronic System, pp. 490-496, May 1990.*

[37] Siew-Chong Tan, Yuk-Ming Lai, Chi Kong Tse, "*Sliding Mode Control of Switching Power Converters: Techniques and Implementation*", CRC Press, @2012 by Taylor & Francis Group

[38] Siew-Chong Tan, Yuk-Ming Lai, Chi Kong Tse, Luis Martínez-Salamero, Chi-Kin Wu ,"*A Fast-Response Sliding-Mode Controller for Boost-Type Converters With a Wide Range of Operating Conditions", IEEE Transactions on industrial electronics, vol. 54, no. 6, December 2007*

[39] Siew-Chong Tan, Yuk-Ming Lai, Chi Kong Tse,"*General Design Issues of Sliding-Mode Controllers in DC–DC Converters", IEEE Transactions on industrial electronics, vol. 55, no. 3, March 2008*

[40] Abdelhalim Kessal, Lazhar Rahmani, "*Analysis and design of sliding mode controller gains for boost power factor corrector*", ISA Transactions52(2013)638–643

[41] HeZhaolan, ZhangShuli,WuJunfeng."*Sliding mode control of switched linear systems based on common Lyapunov function*", 3rd international symposium on systems and control in aeronautics and astro- nautics (ISSCAA);2010.pp.300–4.

[42] Utkin VI. *Sliding modes and their applications on variable structure system.* Moscow Russia: MIR publisher; 1978.