An 8-bit Low Power Energy Recovery Full Adder Design

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Abstract

With the development of wireless communication and portable electronic products, circuit power consumption has become the critical bottleneck of the VLSI design. Among the low power VLSI designs, adiabatic circuit shows a promising future and has been studied by many researchers. As a newly emerged low power technique, adiabatic circuits can be implemented with different architectures such as PAL, 2N-2N2P, ECRL, and CAL, etc. They all lead to significant power saving. In this paper, we implemented true single-phase energy-recovering logic (TSEL) in PSPICE to build a 8-bit low power full adder. In order to verify the power saving of the adiabatic design, a traditional 8-bit static CMOS full adder is also designed in PSPICE for reference. PSPICE power simulation is used to simulate the power consumption of both full adder designs for the same given input pattern sequence. PSPICE power simulation result shows that TSEL full adder lead to effective power saving compared to conventional CMOS full adder. The adiabatic design also shows good potential to be used in high speed circuit design.

Introduction

VLSI (very large scale integration) technology has been growing at exponential rate for many decades since its invention. Nowadays a modern CPU (Central Processing Unit) circuit may contain billions of transistors. As device density in VLSI becomes extremely dense and the clock frequency of circuits keep increasing, the power density of modern VLSI also ramps up very quickly. The accumulated heat can quickly raise the temperature and burn out the circuit if the heat is not properly dissipated. This has become a serious bottleneck for further increase of circuit speed. Moreover, with the wide spreading of portable and wireless devices, there is pressing need to lower down the power consumption of VLSI circuits so that the battery life can be extended. Even though the power of single MOS transistor continues to decrease, the overall power consumption of personal computer is still growing at very fast rate. High power consumption leads to increased energy costs and shorter battery life for portable electronics. It also leads to overheating and downgrades system performance stability. As a result, low power VLSI becomes more and more important in modern VLSI design.

Various low power VLSI technique have been proposed. Among them, adiabatic computing is a newly-emerged innovative low power technique. Unlike the conventional static CMOS design, adiabatic circuits usually keep a small voltage drop between two ends of device resistance, thus only part of the energy is consumed on resistance components. The rest of the energy flow back to the power supply through cross-coupled transistor and can be reused in next process. In this way, the energy consumption of the circuits can be significantly reduced.

The basic structure of a TSEL PMOS gate is illustrated in Fig. 1 [1], which is a PMOS inverter. This inverter consists of a pair of cross-coupled transistors (MP1 and MP2), a pair of current control switches (MP3 and MP4), and two function blocks (MP5 and MP6). The port PC supplies the sinusoidal power-clock V_{PC}. The port RP supplies a constant reference voltage V_{RP} to the PMOS gate. Inputs and outputs are dual-rail encoded. The current control switches and the reference voltages are the structural characteristics that differentiate TSEL from other adiabatic logic families. The operation of a TSEL PMOS gate has two phases: discharge phase (DP) and evaluate phase (EP). Fig.2 shows these phases with respect to the power-clock V_{PC}. During DP, the energy stored in the capacitance of nodes “out” or “/out” is recovered. In the beginning of this phase, V_{PC} is high. As VOC starts ramping down toward low, it pulls both V_{out} and $V_{/out}$ down toward the PMOS threshold voltage |Vtp|. This event is adiabatic until VPC drops below VRP-|Vtp|. The output of the gate is evaluated during EP. Let us assume that Vin is high and V/in is low. Initially, VPC is low. As VPC starts rising, MP1 and MP2 turn on. While VPC<VRP-|Vtp|, MP3 and MP4 are conducting. Since VRP exceeds VPC, a pull-up path is created from RP to /out, and the voltage at /out starts rising toward VRP. The pair of cross-coupled transistors MP1 and MP2 function as a sense-amplifier and boost the voltage difference of the two output nodes. As soon as this difference exceeds |Vtp|, MP1 turns off and /out is charged adiabatically from that point on. When VPC≥VRP-|Vtp|, MP3 and MP4 are turned off and disconnect the function blocks from the outputs “out” and “/out”. Hence, any further change in the inputs do not propagate to the outputs. Voltage of node “out” stays at |Vtp| throughout EP, and “/out” is charged up to the peak of VPC at the end of EP. The output values are ready to be sampled near the peak of VPC [1].

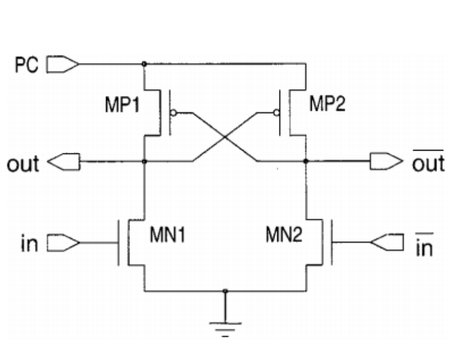


Fig.1. PMOS inverter in TSEL

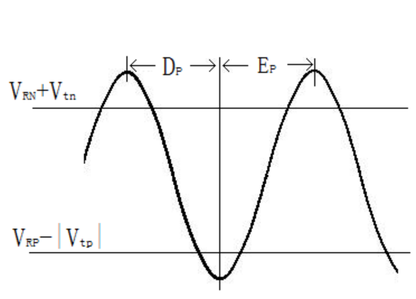
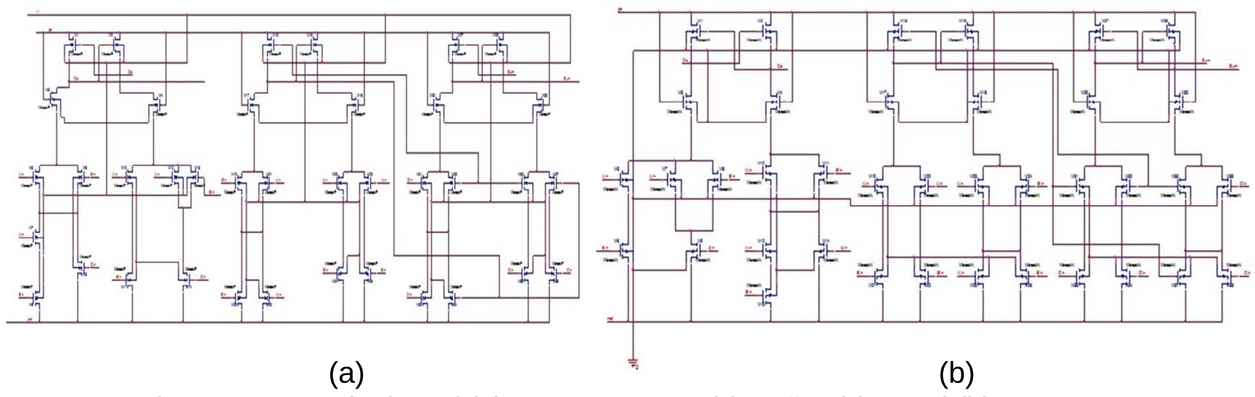


Fig.2. TSEL timing

Design Consideration

As Fig.3. shows, a TSEL 1-bit full-adder includes 38 transistors. We use XOR gates as much as possible to reduce the resistance of function blocks so that we can have stronger output signal. However the resistance can not be too small. Otherwise the reference voltage would not be able to pull up function block. All the inputs and outputs are dual-rail encoded, thus it is not necessary to put inverter between the blocks. Power clock, reference voltage and W/L ratio need to be selected carefully for the circuit to function properly. For comparison, a traditional 1-bit nMOS full-adder is also designed for pipeline cascading. Its structure is similar to pMOS technique. To improve the design efficiency, PSPICE hierarchical design is used to build 8-bit pipelined full adder. The schematic design is shown in Fig.4.



(a) (b)

Fig.3. PSPICE design of (a) TSEL pMOS 1-bit Full-Adder and (b) TSEL nMOS 1-bit Full-Adder

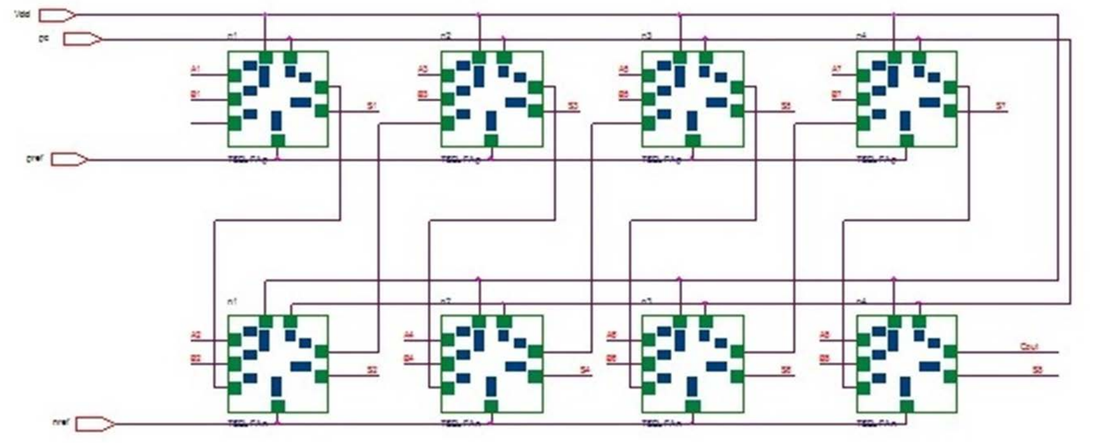
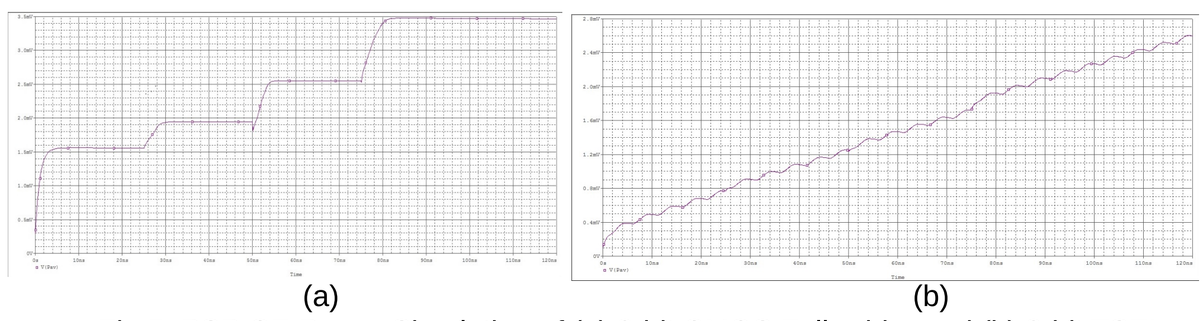


Fig.4. PSPICE schematic design of TSEL 8-bit Full-Adder

Simulation Result And Discussion



(a) (b)

Fig.5. PSPICE Power Simulation of (a) 8-bit CMOS Full-adder and (b) 8-bit TSEL Full-adder

For power comparison, PSPICE power simulation is performed on both static CMOS full adder and TSEL full adder for the same given input pattern sequence. Both full-adders are designed using 0.5µm CMOS technology. Simulation time is set as 100ns, with step of 5ns. Each gate has an output load capacitance of 60pF.

From Fig.5(a), we can see the average power consumption of 8-bit conventional static CMOS full-adder is:

Pav(CMOS) = 3.4724mW.

As we can see in the simulation result, power curves show step increase due to input pattern sequence. As we know, majority of power consumption in CMOS circuit is due to dynamic power, which is related to states switches. While output states remain unchanged, the power curve becomes flat. When new input pattern is applied and output nodes switch the states, power curve ramps up, indicating an increase in energy consumption. In the simulation, four input patterns are applied, hence leading to four ramping steps of the power curve.

From Fig.5.(b), we can see the average power consumption of TSEL 8-bit pipelined full-adder for the same given input pattern sequence is:

Pav(TSEL) = 2.3219mW.

The shape of TSEL full-adder power curve is different from the CMOS full adder. It shows more slow increase of power curve, instead of the steep step increase in power curve of CMOS full adder. That is because the output of TSEL logic is composed by sinusoidal wave which leads to slow gradual increase of power curve. Therefore TSEL circuit is more efficiency when working in high speed mode because it can reduce unnecessary switching power consumption.

From PSPICE power simulation, it shows that TSEL full adder consumes less power compared to CMOS full adder. However, TSEL full adder has more transistor count, hence leading to larger circuit area.

Transistors count increase of TSEL full adder: N_{diff} = 304 - 224 = 80

Circuit area increase of TSEL full adder: A= 80/224×100%= 35.7%

Energy saving of TSEL full adder: Psave = (3.4724 - 2.3219)/3.4724×100% = 33.1%

Based on above result, it shows TSEL 8-bit full-adder is much more energy efficient than conventional CMOS design. TSEL full-adder saves about one third of energy than static CMOS design. Due to the complexity of TSEL logic, its circuit area is inevitable larger than CMOS design. That is, we trade circuit area for power saving in TSEL design.

Conclusions and Future Work

In this project, an 8-bit TSEL pipelined full-adder is designed and simulated in PSPICE using 0.5µm process. For comparison, a static CMOS full adder is also designed in PSPICE. PSPICE power simulation is used to simulated the power consumption of both adders for the same given input pattern sequence. Simulation result shows TSEL full adder leads to ~33.1% power saving compared to CMOS design. While due too its complex structure, 8-bit TSEL full-adder uses 80 more transistors than CMOS design, which translates into ~35.7% area increase. The adiabatic computing demonstrates its attractive potential for future low power VLSI design.

References

[1] Suhwan Kim; M.C. Papaefthymiou "True single-phase adiabatic circuitry", IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 9, Issue: 1, Feb. 2001)