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Increasing the time resolution of a pulse width modulator in a class D power amplifier by using delay lines

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Abstract. In this paper, we present a method to increase the time resolution of a pulse width modulator by using delay lines. The modulator is part of an open loop class D power amplifier, which uses the ZePoC algorithm to code the audio signal which is amplified in the class D power stage. If the time resolution of the pulse width modulator is high enough, ZePoC could also be used to build an high accuracy AC power standard, because of its open loop property. With the presented method the time resolution theoretically could be increased by a factor of 16, which means here the time resolution will be enhanced from 5 ns to 312.5 ps.

Figure 1. Class D power stage.

1 Introduction

The mean advantages of a complete digital class D power amplifier based on the zero positon coding (ZePoC) are the low switching rate and the separated baseband. ZePoC was initially used and implemented for audio coding by the Institute for Theoretical Electrical Engineering in Hannover. Much research was done over years resulting in a number of publications. A good overview could found in the white paper from Texas Instruments (2005). The binary signal computed by the ZePoC algorithm implemented on a digital signal processor (DSP) is generated by a pulse width modulator (PWM) unit inside the DSP.

The DSP is an ADSP-21369 from Analog Devices, which PWM unit is clocked at 200 MHz (Analog Devices ADSP-21369 (2009)). At this time there are no DSPs on the market, which go far beyond this clock rate. To use ZePoC in an high accuracy AC power standard, the open loop structure of the ZePoC system must be preserved. The only way to increase the accuracy is to increase the time resolution of the PWM signal (Wellma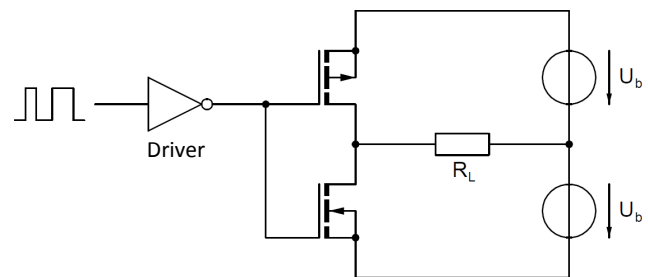nn et al., 2010). In this paper we present a way to increase the time resolution without increasing the clock rate of the PWM unit.

2 Basics

Figure 1 shows a class D power stage, which consists of an inverting driver, two complementary MOSFETs and a symmetric power supply. The driver switches the MOSFETs one at a time on and the other one off according to the input signal. This means that the theoretical efficiency of the power stage is 100 %, but in reality there are power losses because of the internal resistance of the MOSFETs and switching losses. Because of the low switching rate generated by the ZePoC algorithm, the efficiency of the power stage is > 90 %. Basically a class D power stage can only amplify binary signals. As a result, the power stage has an absolute nonlinear transmission behaviour. Therefore, a modulation and demodulation as shown in Fig. 2 of the signal is necessary to get an overall linear transmission behaviour.

In a class D amplifier, a passive low pass filter (LPF) is used for demodulation. The correctly reconstruction of the audio signal is only possible, if there is a gap in the spectrum
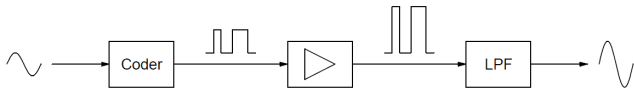
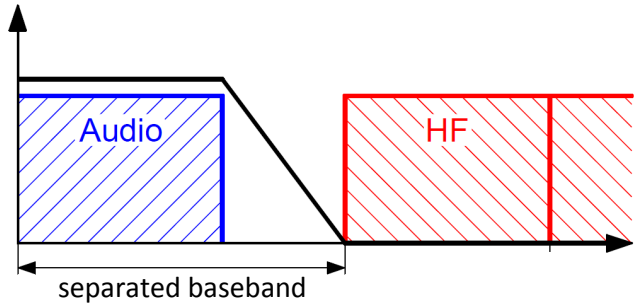**Figure 2.** Signal transmission in class D amplifier.

Figure 3. Spectrum of the ZePoC binary signal.

Figure 4. Pulse width modulated signal.

of the binary signal between the audio band and the high frequency distortions caused by the modulation process. ZePoC is a modulating algorithm with a separated baseband. This means that the spectrum of the generated binary signal is free of distortions below a specified frequency. The maximum of this frequency is half the switsching frequency.

Figure 3 shows the ZePoC spectrum with the audio band inside the sparated baseband. The black line illustrates the transfer function of the LPF used for signal reconstruction. Only the audio signal could pass the LPF, the high frequency (HF) distortions are blocked completely. The gap between the audio band and the HF part of the spectrum must be as wide as the transition band of the LPF. For that reason a switching frequency of 96 kHz is used.

The PWM signal shown in Fig. 4 demonstrates the need of increasing the time resolution of the PWM modulator. The PWM unit inside the DSP on which the ZePoC algorithm is implemented works with a clock speed of 200 MHz, so the value of the binary signal could only change every 5 ns. This means that the edges of the PWM signal are in a 5 ns time grid. With a switching rate of 96 kHz (T = 10.42 µs) the number of possible duty cycles of the PWM signal is limited to 2084. This equals to a resolution of approx. 11 bits. Compared to the resolution of an audio compact disc (CD) of 16 bits, the resolution of this class D amplifier must be increased by 5 bits to get the same resolution as a CD. 5 bits means a factor of $2^5 = 32$.

3 Approach

Figure 5 shows the entire signal chain of the class D amplifier. Out of a pulse code modulated (PCM) audio signal a PWM signal is generated by the DSP using the ZePoC algorithm. This binary signal is amplified by the class D power stage. A loadspeaker is connected to the output of the LPF
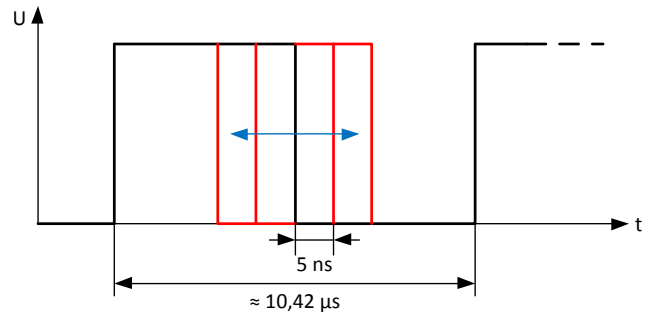
which reconstructs the audio signal. The amplitude of the signal (volume) could be controlled by the supply voltage of the class D power stage.

To increase the time resolution of the PWM modulator, an additional module will be inserted into the signal chain at the position of the red arrow. From the DSP board to the class D power stage the PWM signal is transferred via a low voltage differential signaling (LVDS) interface. For that reason the additional module must have a LVDS input and output.

The concept of the time resolution enhancement is displayed in Fig. 6. The PWM signal with the low time resolution at LVDS IN is received simultaneously by four LVDS receivers. Each output of the receivers drives a 75 Ω transmission line of an individual length. Every transmission line will delay the PWM signal by a specified time, this is why we call them delay lines. At the end the delay lines are terminated by 75 Ω resistors. The four trimmer capacitors are used to calibrate the delay times of the particular signal pathes.

Every delay line is connected to an input of an analogue multiplexer (Analog Devices ADG704, 1999) controlled by the DSP. Exactly one delay line will be routed through the multiplexer to the LVDS transmitter. The input of the class D power stage will be connected to the PWM signal with the higher time resolution at LVDS OUT. Thus, the modulated edge of the PWM-signal can be delayed for a defined time controlled by the DSP.

4 Implementation

The time resolution enhancement module (TREM) consists of two delay stages as shown in Fig. 6 connected in series. Figure 7 demonstrates how the time slot of 5 ns will be divided into 16 sections by the two stages. The blue marks show the delay times of the first stage and the red marks show the delay times of the second stage in combination with the first stage. So the first delay stage generates a 1.25 ns time grid and both together a grid of 0.3125 ns.

For the delay lines a coaxial cable of type RG179 is used. The velocity factor for this type of cable is 0.7. With this information, the length of the delay lines can be calculated. The coax cables must be a little bit shorter than calculated
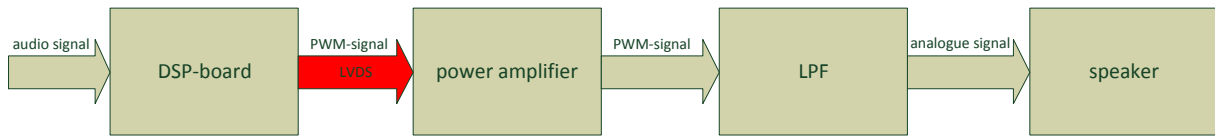
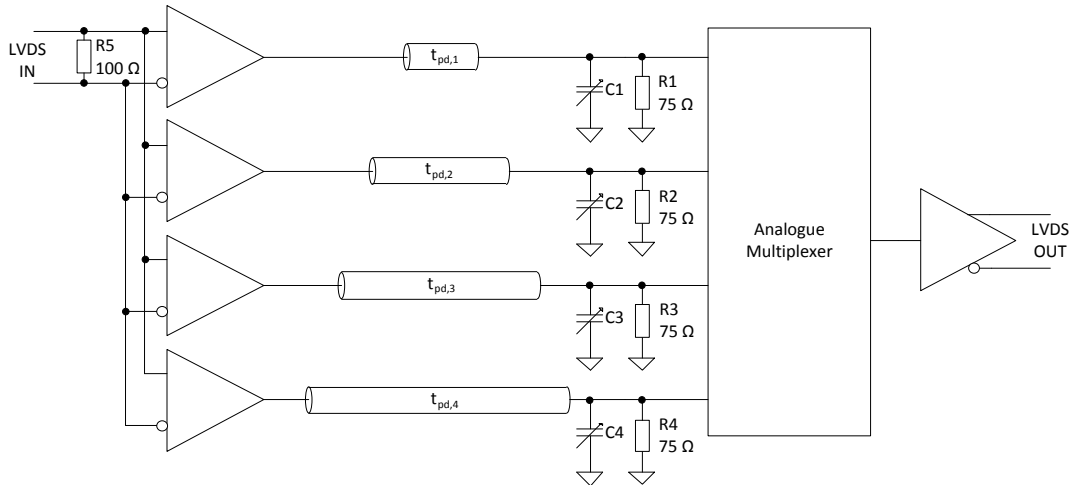**Figure 5.** Signal chain of the class D amplifier.
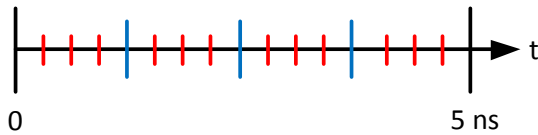

Figure 6. Concept with delay lines.

Figure 7. Time sections.

Table 1. Delay times and cable lengths of stage 1.

line	delay time	length
1	0 ns	0
2	1.25 ns	263 mm
3	2.5 ns	525 mm
4	3.75 ns	788 mm

Table 2. Delay times and cable lengths of stage 2.

line	delay time	length
1	0 ns	0
2	0.3125 ns	66 mm
3	0.625 ns	131 mm
4	0.9375 ns	197 mm

5 Measurement results

For each of the 16 possible signal paths the delay times were measured 1000 times and than averages were calculated. The blue line in Fig. 9 shows the measurement results. The red line shows the calculated delay times listed in Tables 1 and 2. There are some differences between the calculated and the measured delay times. The deviation between these two values are depicted in Fig. 10 for all 16 signal paths.

The highest deviation was measured for path 8. Its size is about 200 ps. In comparison to the shortest delay time of 312.5 ps, the time resolution could not reach the maximum value of 4 bits. It is not possible to reduce the deviation of path 8 without changing other deviations. The analysis of the standard deviation of the jitter for each path shows that all values are uniformly distributed and less than 50 ps. That means that the jitter has no problematic effect on the delay times.
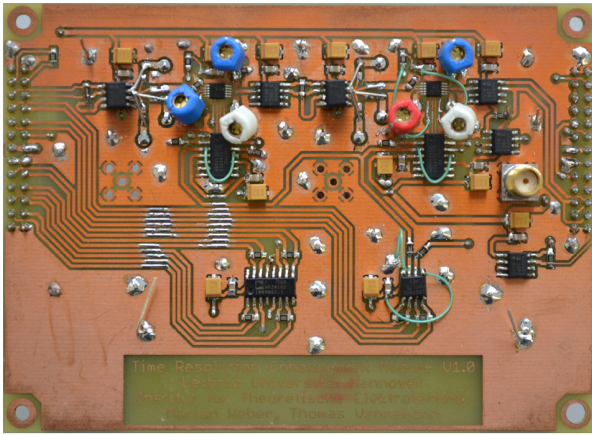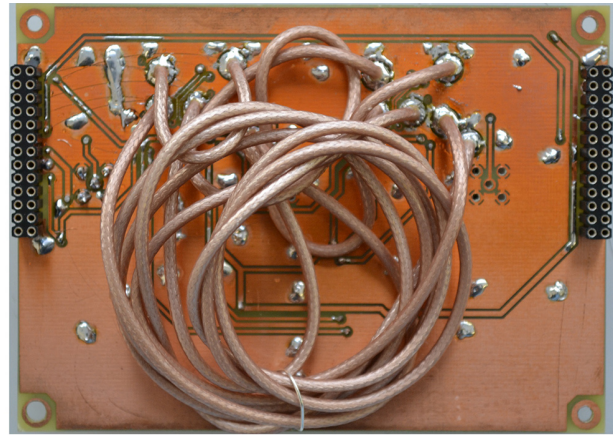
because of the trimming capacitors which add an capacitive load to each delay line. The delay times and the resulting lengths for each delay line of the two different stages are shown in Tables 1 and 2.

Figure 8 shows the prototype which includes the two delay stages. On the top side of the printed circuit board (PCB) are all surface mounted devices (SMD) and trimming capacitors. The connectors to the DSP board and the class D power stage are on the bottom side of the PCB. All delay lines are coaxial cables of type RG179 and are also mounted on the bottom side.

Top

Bottom

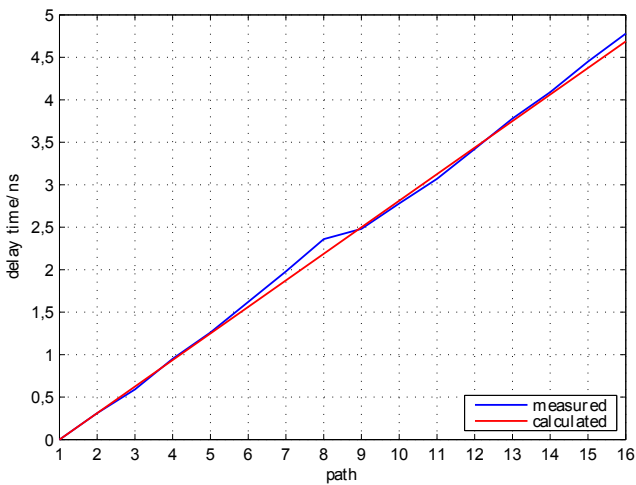**Figure 8.** Top and bottom side of the prototype board.

Figure 9. Averages of the delay times (over 1000 values).
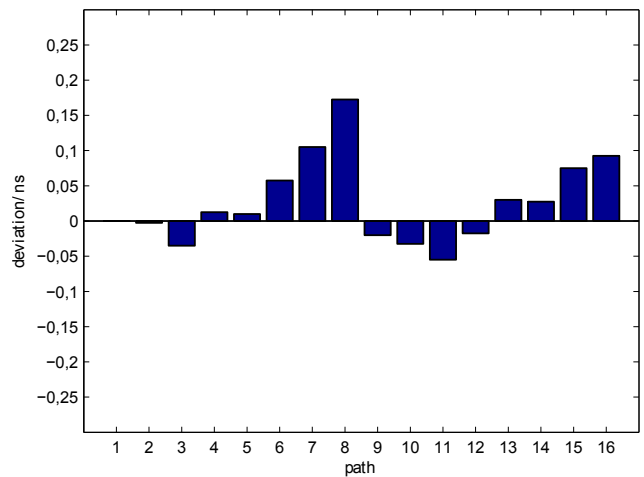

Figure 10. Averages of the deviations (over 1000 values).

6   Conclusions

In this paper, a method to increase the time resolution of a pulse width modulator that is used in a class D power amplifier was presented. The measurement results of the prototype shown that it is possible to increase the time resolution. However, the theoretical factor of 16 (4 bits) was not reached because the delay lines could not be tuned exactly. The exact time resolution improvement factor of the presented module can be determined by measurement of the signal to noise ratio (SNR) of the audio amplifier.

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