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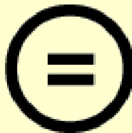

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ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Doctoral Thesis

Plasmonic Terahertz Detector Based on Asymmetric Silicon Field-Effect Transistor for Real-Time Terahertz Imaging System

Min Woo Ryu

Department of Electrical Engineering

Graduate School of UNIST

2017

ULSAN NATIONAL INSTITUTE OF
SCIENCE AND TECHNOLOGY

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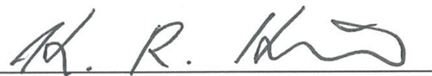
A thesis submitted
to the Graduate School of UNIST
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy

Min Woo Ryu

16. 12. 2016 of submission

Approved by



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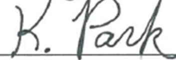

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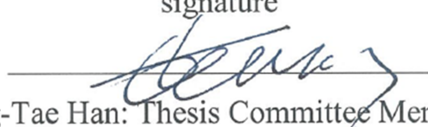

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Abstract

Terahertz (THz) technology has a great potential application owing to the unique properties of THz wave that has both permeability and feature of straight. Among the various technology in THz frequency range, THz imaging technology is very promising and attractive owing to harmlessness in human body by very low energy. In particular, for real-time THz imaging detectors, field-effect transistor (FET)-based THz detectors are now being intensively developed in multi-pixel array configuration by exploiting the silicon (Si) technology advantages of low-cost and high density integration.

FET-based plasmonic wave detection mechanism, which is not limited by cut-off frequency as in transit-mode, has attractive features such as enhanced responsivity (R_v) according to frequency increase in THz range and robustness to high THz input power. To analyze the operation principle of plasmonic THz detector, an analytical device model has been implemented in terms of device physics. The non-resonant and "overdamped" plasma-wave behaviors have been modeled by introducing a quasi-plasma electron charge box as a two-dimensional electron gas (2DEG) in the channel region only around the source side of Si FETs. Based on the coupled non-resonant plasma-wave physics and continuity equation on the technology computer-aided design (TCAD) platform, the alternate-current (ac) signal as an incoming THz wave radiation successfully induced a direct-current (dc) drain-to-source output voltage as a detection signal in a sub-THz frequency regime under the asymmetric boundary conditions between source and drain.

The significant effects of asymmetric source and drain structure, channel shape on the charge asymmetry and performance enhancement have been analytically investigated based on non-resonant plasmonic THz detection theory. By designing and fabricating an asymmetric transistor integrated with antenna, more enhanced channel charge asymmetry has been obtained for enhanced detection response. Through verification of the advanced non-quasi-static (NQS) compact model, the intrinsic FET delay and total detector delay in THz plasmonic detection are successfully characterized and are small enough to guarantee a real-time operating detector. These results can provide that the real-time THz imaging of moving objects has been experimentally demonstrated based on plasmonic 1x200 array scanner by using the high/fast detecting performance asymmetric FET and multiplexer/amplifier circuits.

The highly-enhanced R_v and reduced noise equivalent power (NEP) have been demonstrated by exploiting monolithic transistor-antenna device considering impedance matching between transistor and antenna. This record-high enhancement is due to antenna mismatching and feeding line loss reduction as well as the enhanced charge asymmetry in the proposed monolithic transistor-antenna device. Therefore, high-performance plasmonic THz detector based on asymmetric Si FET can compete as commercial THz detector by taking advantages of monolithic device technology for real-time THz imaging system.

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Nomenclature and Predicate

2DEG	Two-dimensional electron gas
ac	Alternating current
BSIM	Berkeley short-channel IGFET model
CW	Continuous-wave
CMOS	Complementary metal-oxide semiconductor
dc	Direct current
EOT	Effective-oxide thickness
FDTD	Finite-difference time domain
FET	Field-effect transistor
FPA	Focal plane array
GaAs	Gallium arsenide
GaN	Gallium nitride
HEMT	High-electron-mobility transistor
HSPICE	Hewlett simulation program with integrated circuit emphasis
IC	Integrated circuit
IGFET	Insulated-gate field-effect transistor
ILD	Inter-layer dielectric
MCB	Main control board
MUX	Multiplexer
NEP	Noise equivalent power
NQS	Non-quasi-static
MOS	Metal-oxide-semiconductor
NMOS	N-channel metal oxide semiconductor
OAP	Off-axis paraboloidal
PCB	Plastic chip board
PECVD	Plasma-enhanced chemical vapor deposition
QS	Quasi-static
R_v	Responsivity
RF	Radio Frequency
SBD	Schottky barrier diode
Si	Silicon
SRS	Surface roughness scattering
SSW	Subthreshold swing
STI	Shallow trench isolation

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TCAD	Technology computer-Aided Design
THz	Terahertz
VNA	Vector network analyzer
UCRF	UNIST central research facilities
UNIST	Ulsan National Institute of Science and Technology (Ulsan, Korea)

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Chapter I
Introduction

1.1 Terahertz technology

The terahertz (THz) frequency range (10^{11}~10^{13} Hz) in the electromagnetic wave spectrum is called THz wave, which forms the THz gap between the micro-wave band developed by electronics and light wave developed by photonics, which is depicted in Figure 1-1. When converted to a wavelength in the vacuum, it corresponds to a range of 3 mm to 0.03 mm. Because range of frequencies lie in between the ranges covered by the radio frequencies (RF) and microwave techniques, and the optical and photonic techniques, the THz technology in the electromagnetic wave spectrum has various potential applications for imaging and spectroscopy technology owing to its unique properties, which include permeability and feature of straight [1]. Then, it is possible to detect biopolymer, carbide and plastic unlike characteristics of other frequency bands.

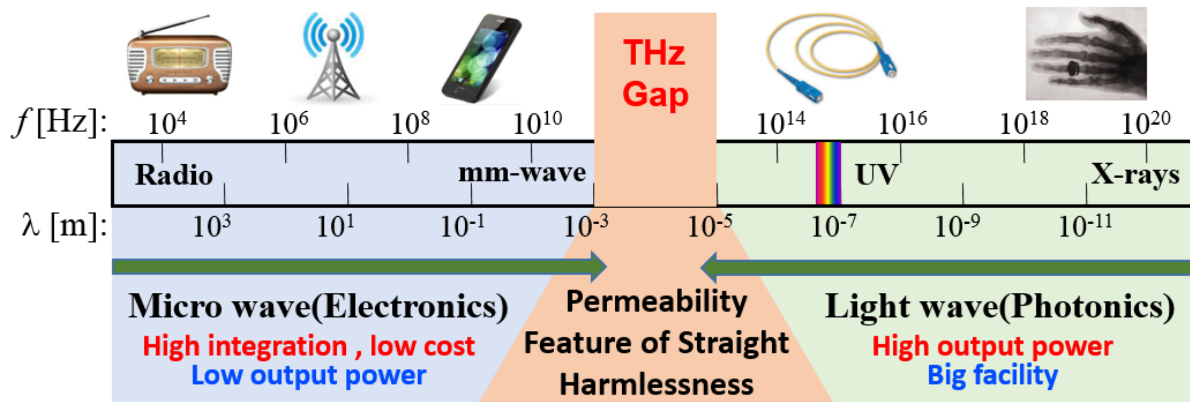

Figure 1-1. The electromagnetic wave spectrum.

Recently, a number of studies have been reported on THz imaging system, which is closer than spectroscopy to being commercialized in the near future. Moreover, owing to harmlessness in human body by very low energy in comparison with x-ray, THz imaging technology is very promising and attractive in near-future non-destructive human body inspection, security, and biomedical application as shown in Figure 1-2 [2-10]. Especially for the detector devices in THz imaging technology, electronic devices-based high performance detectors are now being intensively developed by exploiting their advantages of low-cost and high density integration for real-time THz imaging system [11-22].

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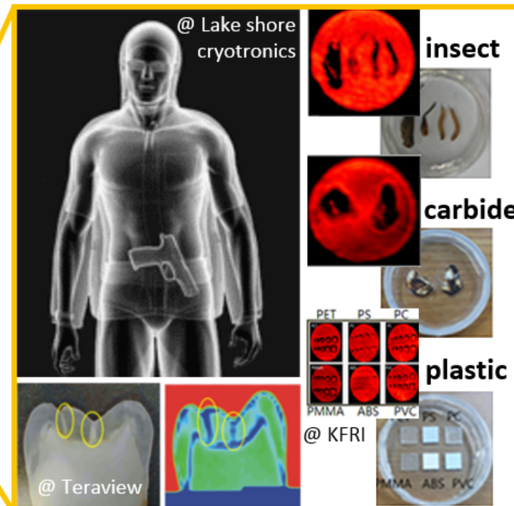

Figure 1-2. THz technology fields: Communication, imaging, and spectroscopy technology.

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1.2 Motivation

To address the specific technical issues related with performance limits, the performance metrics of THz detector based on field-effect transistor (FET) should be carefully investigated. Among key parameters indicative of detector performance are responsivity (R_v), sensitivity (or noise equivalent power) and response time. Responsivity relates the detector output signal to incident power, thus a more responsive detector would have a greater output signal for a given incident power. Sensitivity infers the minimum incident power which can be detected. Terahertz power arriving at the detector is diminished significantly by distance due to absorption in the atmosphere and in transmission through, or reflection from the imaged object. Additionally, ambient radiation and variations in the radiation emission process, described as radiometric fluctuation noise, place constraints upon detector sensitivity [23]. Noise equivalent power (NEP) is a widely-used measure inverse to sensitivity, and is frequently considered to be the minimum power detectable per square root of bandwidth, in units of W/Hz$^{0.5}$. Useful imaging relies on the ability to differentiate materials based upon differences in power arriving at the detector. These two typical performance metrics can be expressed as follows [24-25]:

$$R_v = \Delta u / P_a \tag{1.1}$$

$$NEP = \frac{\sqrt{4kTR_{ch}}}{R_v} \tag{1.2}$$

where Δu is output voltage (photoresponse), P_a is actual power estimated by incident THz total power, R_{ch} is channel resistance in transistor. From Eq. (1.1), the high R_v can be achieved by obtaining the Δu level of FET as high as possible under the same P_a from THz source. By definition of Eq. (1.2), the best NEP can be obtained by keeping total noise, thermally dominant, of detector as low as possible under the same R_v. The key factor is the Δu in FET stage for the highest R_v and the lowest NEP, which means that Δu of FET should be up to the breakthrough-level along with reducing the total noise of detector. In the conventional approach based on the THz detector configuration of Figure 1-3, however, there have been the following two technical issues limiting the detector performance:

- Only R_v enhancement approach (not photoresponse Δu in FET itself)

: Mainly focusing on circuitry design approach such as adding additional components (e.g. capacitors, FETs) and high-gain amplifier stage. It means that the total detector noise is increased by these additional components and no device-level research on FET itself for high performance THz detector.

- THz input power loss by impedance mismatching

: The typical THz detector should be integrated with antenna as shown in Figure 1-3, since THz

wavelength above the hundreds of micrometers is longer than FET size. However, the significant loss of THz input power originated from a lack of understanding on FET impedance in THz regime. It means the loss of output Δu in FET stage and no in-depth research on FET impedance matching in THz regime.

Therefore, the THz detector performance-breakthrough research should be focused on a device-level FET stage (Figure 1-3) for a feasible real-time THz imaging system.

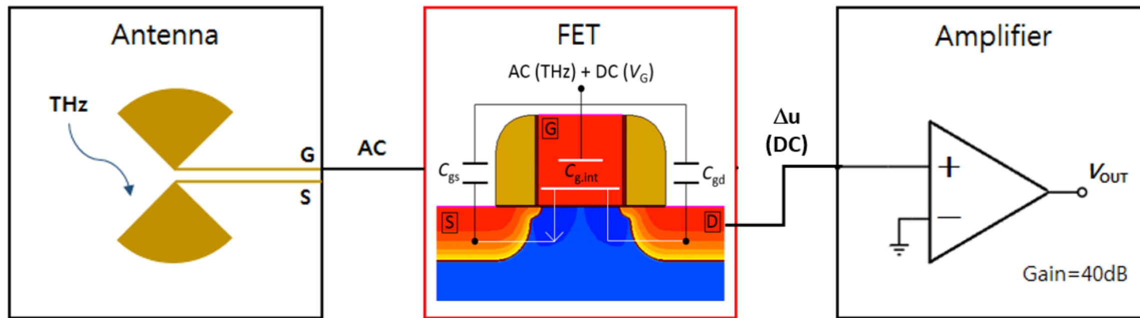

Figure 1-3. Typical stages of FET-based THz detector.

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1.3 Scope and organization

To develop high performance plasmonic THz detector, fundamental performance enhancement should be approached to investigation of from the analysis of device. This thesis focuses on FET-based plasmonic asymmetric THz detector. The main objective of this work is to demonstrate novel design based on asymmetric silicon FET structure for multi-pixel array detector. Furthermore, this includes the proposal and demonstration of monolithic transistor-antenna device for real-time THz imaging system.

This chapter, the thesis introduces THz technology focused on THz imaging technology and then, describes the development of FET-based plasmonic THz detector.

Chapter 2 is devoted to a theory of plasmonic THz detector through a background of plasma THz device and the operation principle of non-resonant THz detector.

Chapter 3 describes the structure and fabrication of plasmonic THz detector based on asymmetric transistor and then, shows the characteristics in terms of asymmetry ratio, detector delay, and detector performance metrics.

Chapter 4 describes the structure and fabrication of monolithic transistor-antenna device. This proposed novel device has perfect impedance matching between FET and antenna through gate metal functioned as THz antenna.

Finally, conclusion is given in Chapter 5.

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Chapter II

Theory of plasmonic terahertz detector

2.1 Plasma-mode

When THz wave is radiated in small size electronics, there are two modes, which are transit mode and plasma mode. Because the emission frequency of transit mode is strongly dependent on the cut-off frequency, which is determined by transit time of local electron, the experimental results show that the maximum emission frequency cannot exceed one terahertz [26]. On the contrary, Shur and Dyakonov predicted an instability of electron plasma waves in a short channel FET at THz frequencies in 1993 [27]. As gate lengths in high-electron-mobility transistors (HEMTs) [28-35] and silicon MOSFETs [36-38] are made increasingly smaller, charge transport becomes ballistic, and device channels behave as resonators. Terahertz response in these devices results from plasma waves being generated in the device channel due to modulation of the electron concentration. A localized decrease in electron concentration causes an excess of positive charge, attracting electrons in the vicinity. These electrons rush towards the positive charge, but because of their inertia, overshoot the charge location. Now attracted in the opposite direction, they again rush in and overshoot the charge location, hence, supporting oscillations of the electron density (i.e. plasma waves). Figure 2-1 compares plasma wave and transit mode performance for silicon (Si), gallium arsenide (GaAs) and gallium nitride (GaN) semiconductors, indicating an increase of roughly ten times in operating frequency, pushing device performance well into terahertz frequencies, even for silicon devices at contemporary gate lengths. The devices using plasma mode focus on propagation of collective electrons, which can be called plasma wave and it has faster velocity than electron drift velocity in resonant mode. FET-based plasmonic wave detection mechanism, which is not limited by cut-off frequency as in Schottky barrier diode (SBD) [39-42], has attractive features such as enhanced R_v according to frequency increase in THz range and robustness to high THz input power [43]. FETs are generally integrated with antennas considering THz wavelength for sub-micron Si FETs to detect sub-millimeter THz waves [44-46]. Therefore, because it is possible to make integrated circuit (IC) with low cost by using Si, the Si-based detector is competitive and offset these shortcomings in the imaging system [13,24,47].

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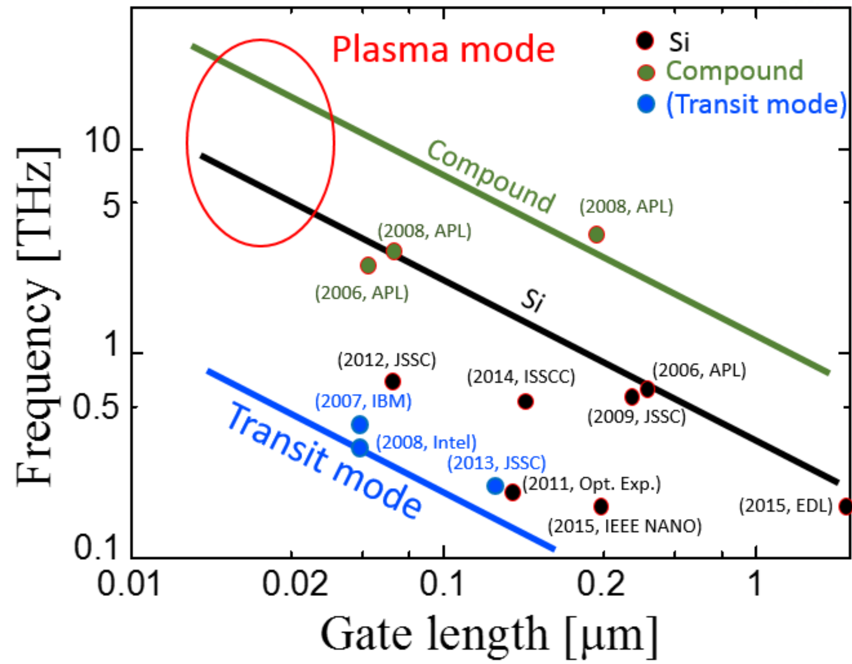

Figure 2-1. Comparison of plasmonic and transit mode operating frequency limits vs. gate length for several semiconductor materials.

2.2 Operation principle

In FET-based plasma wave detection theory [25,27], the resonance quality factor is $\omega\tau$ where ω is the incoming radiation angular frequency and τ is the plasmon decay time due to scattering in the FET channel, which is related with the carrier mobility $\mu = q\tau/m$ where m is the effective mass of electron, q is the electron elementary charge. As shown in Figure 2-2, in case of high frequency regime occurs when $\omega\tau >> 1$, the channel scattering frequency ($1/\tau$) is much smaller than the incoming THz radiation frequency, and then the channel plasma waves can be developed and the FET can act as a resonant [28-30] detector in the strong inversion condition if the channel length is shorter than the propagation distance of the plasma wave. On the other hand, in case of low frequency regime occurs when $\omega\tau << 1$, the typical situation in Si FETs with relatively and low channel mobility high scattering frequency ($1/\tau$). It means that the FET operates in a non-resonant regime [11-22,32-33], but the rectification mechanism is still available in the enables wideband THz detection and sub-threshold condition even though the plasma oscillation is overdamped and it cannot reach the drain side in the relatively long channel. THz detectors based on FET have been demonstrated by using Si metal-oxide-semiconductor FETs (MOSFETs) [11-19] and compound materials-based HEMTs [28-35] for sub-THz non-resonant mode at room temperature and resonant mode at low temperature, respectively.

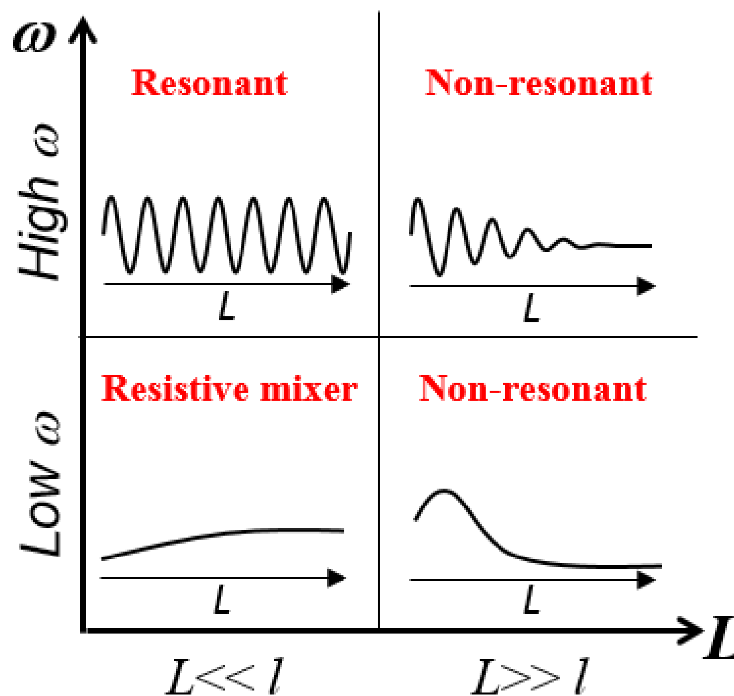

Figure 2-2. Modes and characteristic damping length according to the frequency and device length.

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For non-resonant operation regimes, the Δu appears as the form of dc voltage between drain and source which is proportional to the radiation THz power ([P]). To induce Δu from a given radiation THz power, some asymmetry between the drain and source is needed and there are typical three methods of asymmetry regime [48], such as the difference in the drain and source boundary conditions by using the asymmetry due to a dc current between source and drain [30], external capacitances [12], the asymmetry in feeding the incoming radiation with a special antenna [49]. Related works also have been reported with asymmetric effects of device parasitic in the circuit aspects of FET rectifiers by integrating patch antenna and a high-gain voltage amplifier, and a double-grating gate FET structure in asymmetric unit cell for strong coupling antenna. In case of non-resonant regime based on FET, Figure 2-3 show that THz detection as Δu is observed by voltage difference between the drain and source.

As explained in [25], the basic govern equations of the plasma-wave, which means the oscillations of a channel 2DEG density in time and space, can be summarized with the following three equations:

$$n = CU_g / q \tag{2.1}$$

$$\frac{\partial v}{\partial t} + v\frac{\partial v}{\partial x} + \frac{e}{m}\frac{\partial U_g}{\partial x} + \frac{v}{\tau} = 0 \tag{2.2}$$

$$\frac{\partial U_g}{\partial t} + \frac{\partial (U_g v)}{\partial x} = 0 \tag{2.3}$$

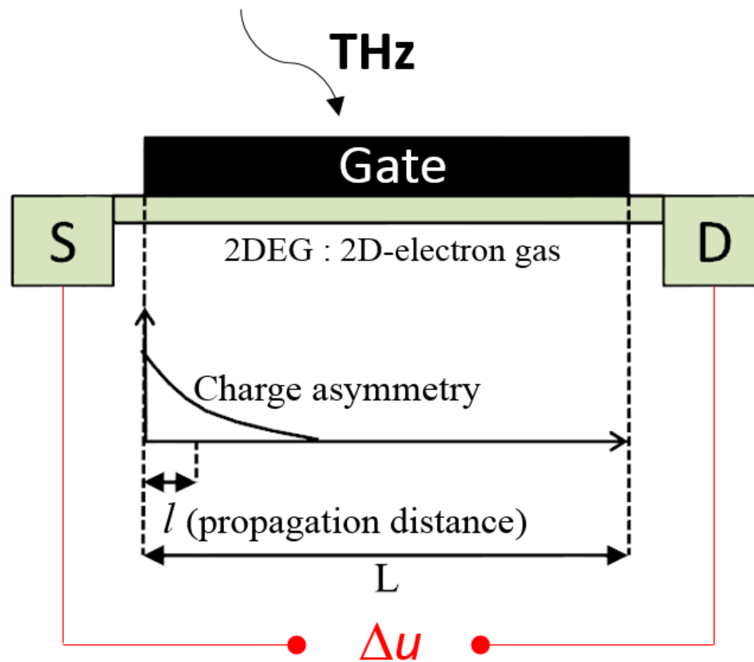

Figure 2-3. Schematic of THz detection based on FET in non-resonant regime.

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where n is the surface 2DEG concentration in the FET channel, U_g is the gate-to-channel voltage swing $U_g = V_{gc}(x) - V_{th}$ ($V_{gc}(x)$: the local gate-to-channel voltage, V_{th}: threshold voltage), C is the gate capacitance per unit area, q is the elementary charge, v is the electron drift velocity, m is the electron effective mass, and τ is the momentum relaxation time.

In the non-resonant regime of the plasmonic THz detectors, the plasma wave becomes overdamped and cannot exist since the electron drift velocity v is considerably small due to the scattering when $\omega\tau$ << 1. Then, the second term in the hydrodynamic Euler equation of Eq. (2.2) can be ignored and it becomes the Drude equation of motion as follows:

$$\frac{\partial v}{\partial t} = -\frac{e}{m}\frac{\partial U_g}{\partial x} - \frac{v}{\tau} \tag{2.4}$$

It should be noted that Drude Eq. (2.4) can be solved with continuity Eq. (2.3) in a self-consistent way on the TCAD platform. By using the following asymmetric boundary conditions for the detector operation,

$$U_g(0,t) = U_a \sin \omega t + V_g - V_{th} \tag{2.5}$$

$$U_g(L_g,t) = V_g - V_{th} \tag{2.6}$$

where U_a is the amplitude of the ac voltage, which is induced by the incoming THz radiation between the gate and source, and L_g is the channel (gate) length, the output signal of FET can be obtained as photoinduced drain-source voltage ΔU in the form of equation as follows [25, 43].

$$\Delta U = \frac{U_a^2}{4(V_g - V_{th})}\left[1 + \frac{2\omega\tau}{\sqrt{1+(\omega\tau)^2}}\right] \tag{2.7}$$

This Eq. (2.7) also can produce the consistent result with the position-dependent photoresponse,

$$\Delta U = \frac{U_a{}^2}{4(V_g - V_{th})}\left(1 - \exp(\frac{-2x}{l})\right) \tag{2.8}$$

where the distance from the source x is relatively much larger than the characteristic length (l) in the non-resonant regime of $\omega\tau$ << 1 [43].

Detector response time by occurrence of l is of great importance in sensing applications involving

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substantial imaging processing. Generally, the FET may be described by an equivalent circuit presented in Figure 2-4. The obvious elements are the distributed gate-to-channel capacitance and the channel resistance, which depends on the gate voltage through the electron concentration in the channel. In terms of low frequency regime ($\omega\tau << 1$), the plasma waves cannot exist because of an overdamping. At these low frequencies, FET become simply short-circuits which leads to an *RC* line as shown in Figure 2-4. Its properties further depend on the gate length, the relevant parameter being $\omega\tau_{RC}$, where τ_{RC} is the *RC* time constant of the whole transistor. Since the total channel resistance is $L\rho/W$, and the total capacitance is CWL (where W is the gate width and $\rho = 1/\sigma$ is the channel resistivity). In case of non-resonant plasmonic THz detector based on Si FET, $\omega\tau_{RC} >> 1$ by relatively long gate ($L >> \rho C\omega)^{-0.5}$. The induced ac current will leak to the gate at a small distance l form the source, such that the resistance $R(l)$ and the capacitance $C(l)$ of this piece of the transistor channel satisfy the condition:

$$\omega\tau_{RC}(l) = 1 \tag{2.9}$$

where,

$$\tau_{RC}(l) = R(l)C(l) = l^2\rho C \tag{2.10}$$

This condition gives the value of the ″leakage length″ l on the order of $(\rho C\omega)^{-0.5}$ (which can also be rewritten as $s(\tau/\omega)^{0.5}$). If l << L, then neither ac voltage, nor ac current will exist in the channel at distances beyond l from the source.

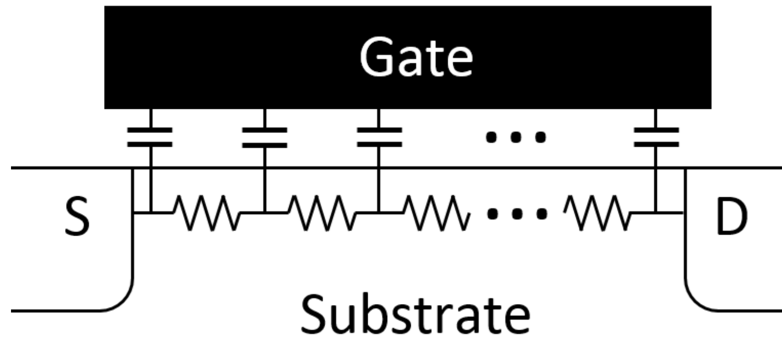

Figure 2-4. Schematic of a FET equivalent circuit.

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2.3 Summary

In this chapter, plasma-mode which is not limited by cut-off frequency, have been introduced in comparison with transit-mode. FET-based plasmonic wave detection mechanism in non-resonant regime has attractive features such as enhanced R_v according to frequency increase in THz range and robustness to high THz input power. rectification mechanism is observed in sub-threshold condition even though the plasma oscillation is overdamped and it cannot reach the drain side in the relatively long channel from a given radiation THz wave. the Δu appears as the form of dc voltage between drain and source which is proportional to the radiation THz power.

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Chapter III

Plasmonic THz detector based on asymmetric transistor

3.1 Introduction

Since the theoretical consideration of plasma waves as a fluidic behavior of two-dimensional electron gas (2DEG) in a FET channel was proposed by Shur and Dyakonov [27], THz emitters and detectors based on plasma-wave theory have been extensively developed. However, In terms of the technical difficulty in achieving a theoretical boundary condition, detector implementation is relatively easier than emitter implementation, where resonant plasma waves in the ballistic channel should be guaranteed. Meanwhile, FET can operate as a plasmonic detector even in non-resonant mode by the overdamped plasma wave ($\omega\tau < 1$) [25]. After the first realization of a plasmonic THz detector based on HEMT [31], Si MOSFETs-based plasmonic sub-THz detectors with relatively low channel mobility have also been demonstrated by showing comparable performance metrics with HEMT [24],[47]. These pioneering works enable the low-cost CMOS technology to be employed for plasmonic THz detector development, which lead to highly sensitive Si CMOS detectors for broadband THz imaging [13].

For CMOS technology-based THz detectors with different detection mechanisms from plasma mode, a Schottky barrier diode (SBD), which is a current-driven transit-mode device, has been scaled down for optimized design so as to increase its cutoff frequency over 1 THz. As a result, a 0.86 THz 4x4 array CMOS technology-based SBD imager was reported with raster scan measurement [22], while a 1x240 array compound InGaAs SBD imager was demonstrated as a real-time one-dimensional line scanner [42]. In terms of the circuit design approach, a resistive mixer-based THz detector has been proposed [11]. By utilizing distributed resistive self-mixing in the FET channel, a 0.65 THz focal plane array (FPA) detector integrated with differential amplifiers was reported [12] and recently, a 1 k pixel video camera has been demonstrated for a real-time high-resolution THz imaging by 65-nm CMOS bulk process technology [14].

The advantages of the plasmonic detection mechanism, which is not limited by cut-off frequency as in the transit mode, are that it can exhibit enhanced performance according to the THz frequency increase [25] and robustness to high-input THz power [43]. However, owing to the much longer wavelength of the THz range (0.3~3 mm) than the feature size of the electronic devices, THz detectors should be equipped with a relatively large size of antenna for input THz wave [7]-[20], which causes significant power loss during transmission, depending on the antenna design [44,46]. Furthermore, high-gain amplifiers, which are widely adopted due to their small output-signal by input power loss, can also increase the total detector noise by additional circuitry [17]. Thus, our previous works have enhanced the performance by focusing on asymmetric FET design itself in a non-self-aligned structure

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[45] and low-impedance FET design considering the impedance matching with the in-plane integrated antenna [46].

In this chapter, performance enhancement of the Si FET-based plasmonic THz detector is demonstrated by asymmetry ratio between source and drain in non-self-aligned process. In addition, high-performance plasmonic THz detector in a self-aligned 65-nm CMOS foundry technology by designing novel asymmetric channels with vertically integrated antenna on the top-metal layer.

3.2 Device structure and modeling

Plasmonic THz detectors based on Si FETs, which operate in non-resonant mode due to its relatively low mobility, can detect THz wave power by dc voltage difference between the source and drain in the sub-threshold conduction channel. As shown in Figure 3-1(a), when the channel inversion layer is not strongly formed in a weak-inversion regime by biasing dc gate voltage (V_{GS}) below threshold voltage (V_T), incoming THz wave, which can be modeled as the ac signal with a frequency (ω), induces the channel 2DEG oscillation with the propagation distance (l_{2DEG}). Under the asymmetric boundary conditions by the external gate-to-source ($Z_{gs,ext}$) and gate-to-drain impedance ($Z_{gd,ext}$), dc drain-to-source output voltage (Δu) can be obtained from the time-averaged asymmetric channel charge distribution [50].

Figure 3-1(b) and (c) show the device simulation results of channel 2DEG oscillation as a function of time and position for symmetric and asymmetric boundary condition, respectively. In the symmetric case of $Z_{gs,ext}= Z_{gd,ext}$ as shown in Figure 3-1(b), the overdamped plasma waves in both the source and drain side show the same l_{2DEG}. This symmetric 2DEG modulation would bring about the completely balanced internal diffusion current at the source ($I_{s,int}$) and drain ($-I_{d,int}$) in the opposite direction and thus there would be no response of Δv_{DS} by zero internal net current ($I_{net,int}$). In the case of $Z_{gs,ext} >> Z_{gd,ext}$ for the external gate-to-drain ac pass (short) condition, however, asymmetric $I_{s,int} >> I_{d,int}$ can be observed from the suppressed 2DEG modulation at the drain side and thus nonzero $I_{net,int}$ would be expected, as shown in Figure 3-1(c). In the open drain configuration (dc cut-off) by connecting the end-circuit stage with a high impedance such as a voltmeter, this nonzero $I_{net,int}$ should be canceled out by the internal cancellation current ($I_{c,int}$). Therefore, the output dc voltage of Δu would be generated at the drain node according to *Ohm's law* of $I_{c,int}= |I_{net,int}|= \Delta u/R$ where R corresponds to a channel resistance (R_{ch}) of FET in the subthreshold (weak-inversion) regime.

To achieve the external ac pass condition at drain side, the quantitative analysis of $Z_{gd,ext}$, which is typically related to an external gate-to-drain capacitance ($C_{gd,ext}$) in MOSFET, should be performed by the intrinsic gate-to-channel capacitance ($C_{g,i}$) for $C_{gd,ext}/C_{g,i} > 1$ from $Z_{gd,ext}= |1/j\omega C_{gd,ext}| < |1/j\omega C_{g,i}|$. Figure 3-2 shows the Synopsys™ *Sentaurus* mixed-mode technology computer-aided design (TCAD) simulation results of normalized Δv_{DS} as a function of $C_{gd,ext}/C_{g,i}$ by connection of the external lumped element $C_{gd,ext}$ with an exemplary MOSFET with a gate length of L_g= 300 nm, width of W= 1 μm, and oxide thickness of t_{ox}= 2 nm ($C_{g,i}$= 5.2 fF with ε_{SiO2}= 3.45x10^{-13} F/cm). At this point, the $C_{gd,ext}$ should be over 100 x $C_{g,i}$ to pass the ac signal completely for the saturated maximum Δu.

In terms of MOSFET design for the detection performance enhancement, it is more important to investigate the rapidly increasing Δu regime where $10^{-3} < C_{gd,ext}/C_{g,i} < 100$ by enhancing channel charge asymmetry rather than the saturated regime of $C_{gd,ext}/C_{g,i} > 100$. As reported in our previous work [45],

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the performance enhancement has been achieved in the range of $C_{gd,ext}/C_{g,i}$ from 2 to 20 by designing an asymmetric channel in a non-self-aligned structure where gate-overlapped source/drain region can be well controlled with layout design. Therefore, the MOSFET design itself without additional lumped circuit elements become significant for high performance in plasmonic power detection mechanism.

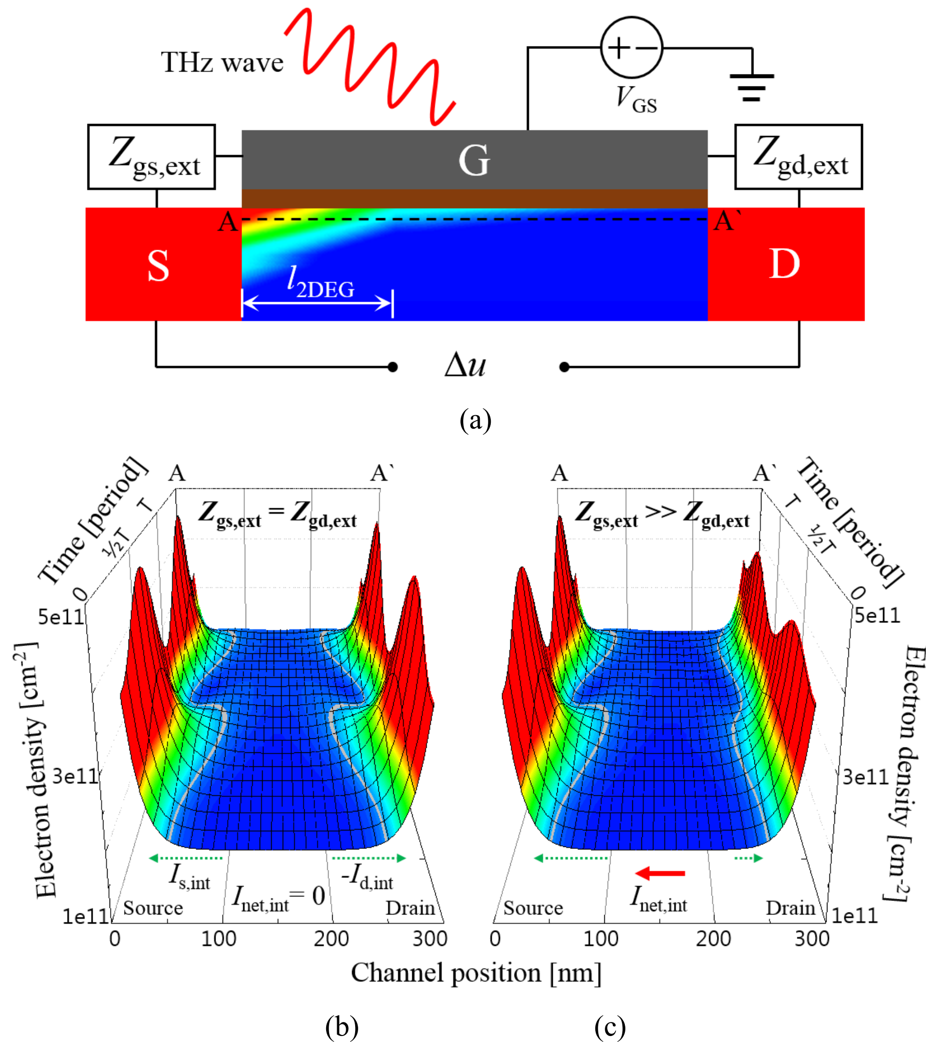

Figure 3-1. (a) Schematic of MOSFET-based plasmonic THz wave detection with two-dimensional electron gas (2DEG) having propagation distance (l_{2DEG}). The device simulation results of channel 2DEG oscillation as a function of time and position for (b) symmetric and (c) asymmetric boundary condition.

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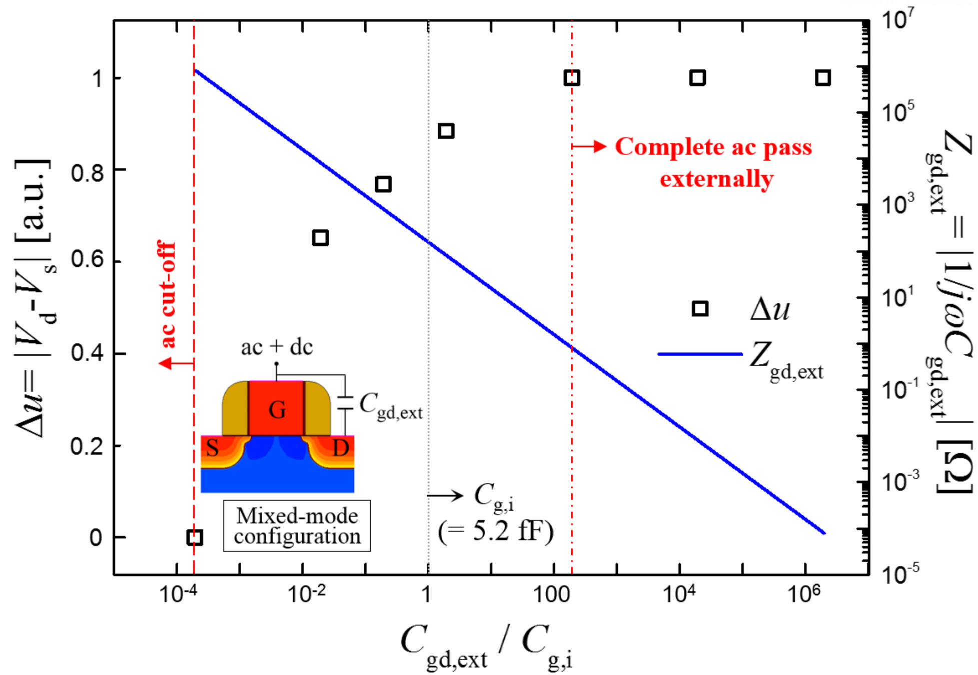

Figure 3-2. Mixed-mode TCAD device simulation results of normalized Δv_{DS} as a function of $C_{gd,ext}/C_{g,i}$ by a connection of the external lumped capacitance $C_{gd,ext}$ ($Z_{gd,ext}= |1/j\omega\, C_{gd,ext}|$ in right y-axis) to the drain node of an exemplary MOSFET.

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3.2.1 Asymmetric field-effect transistor structure

The effect of channel shape on the channel 2DEG density and its asymmetry has been investigated in comparison with a previous non-self-aligned structure, as shown in Figure 3-3. By using a 3-D TCAD device simulation framework, the non-self-aligned, trapezoidal, and self-aligned channel shape isolated by STI are modeled as illustrated in Figure 3-3(a), (b), and (c) with each contour plot of channel electron density showing the same l_{2DEG}, respectively, which indicate that the self-aligned channel in this work (Figure 3-3(c)) has more enhanced electron density near the source side than that of the non-self-aligned structure (Figure 3-3(a)). It can be noted that this result is due to a more confined channel around the source side by presenting the intermediate range of the channel 2DEG density profile at the source in case of the trapezoidal channel (Figure 3-3(b)).

In addition to channel 2DEG density enhancement (Figure 3-3), analysis of the channel shape effect on the charge asymmetry between drain and source has been performed by demonstrating the channel 2DEG density modulation as a function of channel position and time under a superimposed time-varying gate bias ($v_{GS}(t)= V_G + v_i \sin\omega t$) with dc $V_G= V_T$ and ac signal of THz wave with the amplitude of v_i= 20 mV. As shown in Figure 3-4(a), charge asymmetry between source and drain has been obtained under the equalized R_{ch} in each case, which confirms that the observed charge asymmetry only results from channel shape difference.

Figure 3-4(b) shows the normalized maximum and minimum N_{2DEG} by the minimum of each group at x= 25 nm, where N_{2DEG} is highly modulated (close to source), and x= 175 nm, where N_{2DEG} is almost invariable (close to drain). By taking a first-order diffusion approximation, the net current density ($J_{net,int}$) would be produced from these charge asymmetries and expressed as

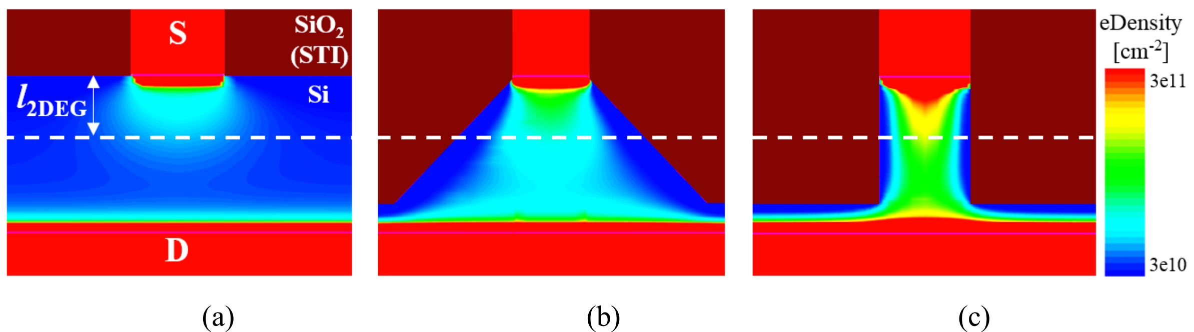

Figure 3-3. Channel electron density contour plots under THz wave radiation (ac signal) onto Si MOSFET with (a) non-self-aligned gate structure, (b) trapezoidal channel shape, and (c) self-aligned gate structure at equivalent channel resistance allowing the same l_{2DEG} for all the different channel shapes.

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$$J_{net,\text{int}} = qD_n\left[\frac{N_{2DEG}\,|_{x=175nm} - MAX(N_{2DEG}\,|_{x=25nm})}{\Delta x}\right] - qD_n\left[\frac{MIN(N_{2DEG}\,|_{x=25nm}) - N_{2DEG}\,|_{x=175nm}}{\Delta x}\right] \tag{3.1}$$

where q is the elementary electronic charge and D_{n} is the electron diffusivity. It can be expected from Figure 3-4(b) that self-aligned channel shape shows more enhanced $J_{\text{net,int}}$ because of the increased charge asymmetry. This $J_{\text{net,int}}$ is proportional to the dc offset voltage of Δu in the output voltage of $v_{\text{DS}}(t)$ as demonstrated in Figure 3-4(c), by following *Ohm's law* given by

$$\Delta u \propto J_{net,\text{int}} \times R_{ch}(V_{GS}) \tag{3.2}$$

where $R_{\text{ch}}(V_{\text{GS}})=\mu_{\text{n}}(W/L)C_{\text{ox}}(m\text{-}1)\exp\{q(V_{\text{GS}}\text{-}V_{\text{T}})/mk_{\text{B}}T\}$ and m is the body effect coefficient in the subthreshold MOS *I-V* equation [51]. Therefore, performance enhancement can be obtained in non-resonant plasmonic THz detector based on FET with a self-aligned gate structure since more enhanced channel charge asymmetry and higher $J_{\text{net,int}}$ have been confirmed.

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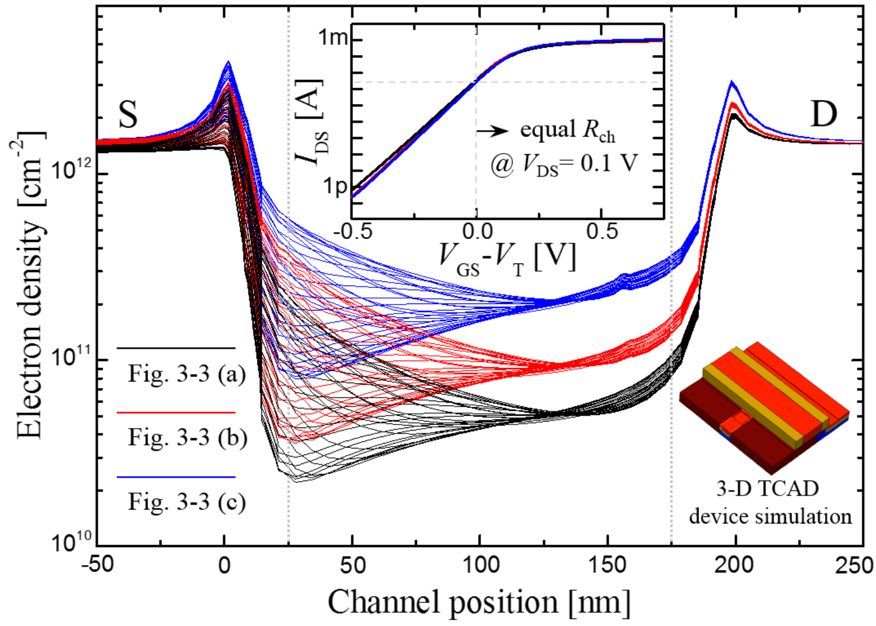
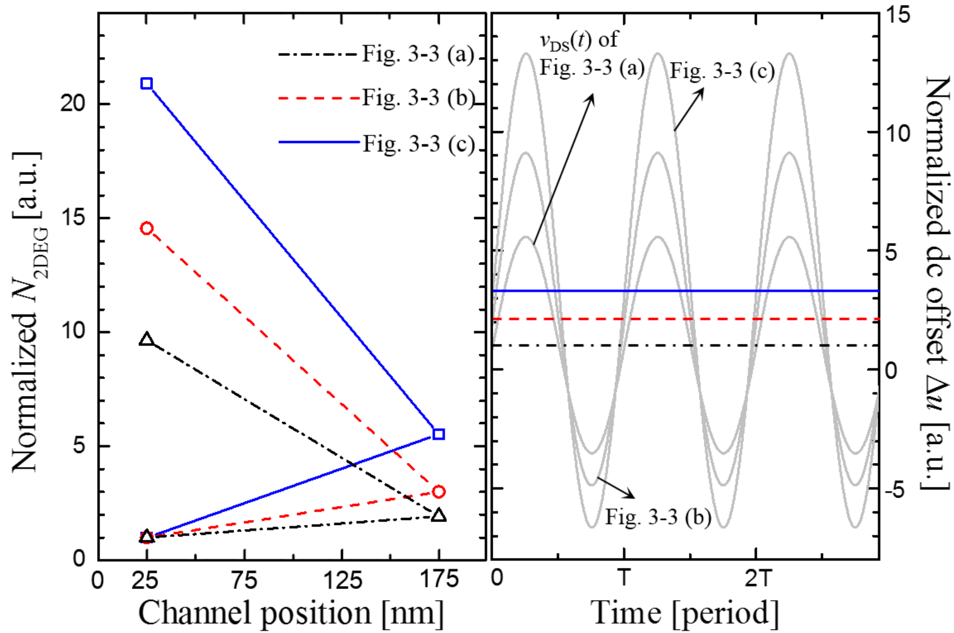


(a)



(b) (c)

Figure 3-4. (a) Electron density modulations as a function of channel position and time from 3-D TCAD device simulation in Figure 3-3 under the same R_{ch} (inset). (b) Normalized max and min N_{2DEG} by each min of Figure 3-4(a) at x= 25 nm (highly modulated) and x= 175 nm (almost invariable). (c) Simulation results of output $v_{DS}(t)$ with the normalized dc offset Δu by the lowest value of Figure 3-3(a) case.

3.2.2 Numerical device simulation

In the non-resonant mode ($\omega\tau < 1$), the 2DEG plasma waves cannot exist in the channel because of overdamping, which means a longer propagation length than the coherent distance, and thus, this eventually give rise to the asymmetric electron distribution along with the channel length direction. Therefore, as shown in Figure 3-5, the quasi-plasma electron box is modeled on the basis of the assumption of 'quasi-static' 2DEG density for the resultant channel electron distribution with asymmetry when THz wave is radiated. Although the resultant 2DEG behavior should be described by the hydrodynamic Euler equation with the convection component in the rigorous manner, the quasi-plasma 2DEG modeling has been performed on the basis of the Synopsys^{TM} *Sentaurus* TCAD platform, which does not include the hydrodynamic Euler formalism, for the efficient simulation of non-resonant wideband THz detectors by exploiting the advantage of well-established MOSFET models and the DC/AC analysis environment on TCAD. In our quasi-plasma 2DEG modeling under the given temperature (T= 300K) and with constant doping profiles. Quasi plasma 2DEG length is determined by, electron modulation simulation TCAD frame work and extract max length of the source side length. Because it is necessary to asymmetry environment between source and drain for extracting Δu in non-resonant THz detector based on Si MOSFET, the applied asymmetric boundary condition in the transient by adding varied external capacitance between gate and drain as shown in Figure 3-6. The gate-to-drain voltage (V_{gd}) can be saturated to DC output voltage as gate-to-drain capacitance (C_{gd}) increases since the gate-to-source voltage (V_{gs}) has been applied as $U_a \sin\omega t + V_g$. Thus, the C_{gd} in our device is satisfied with boundary condition for detecting THz wave.

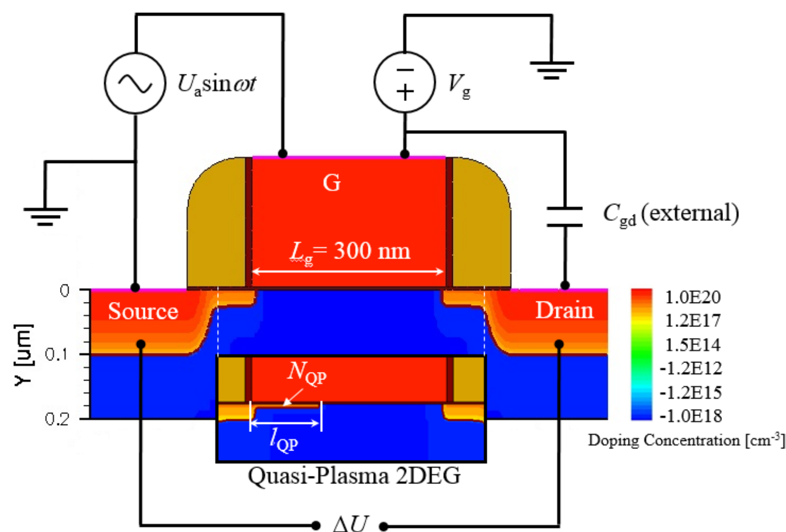


Figure 3-5. Schematic of THz detector with quasi-plasma 2DEG modeling.

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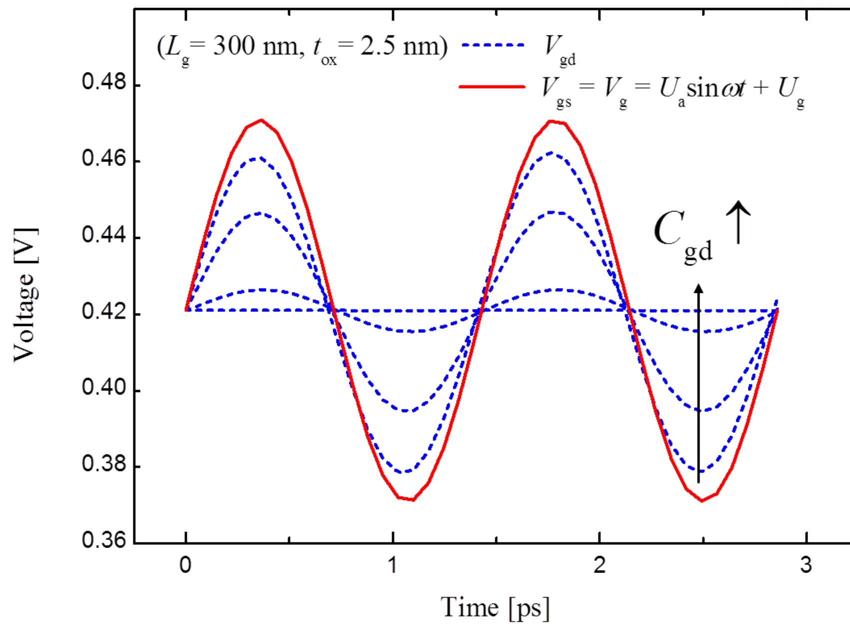

Figure 3-6. The transient simulation applied asymmetric boundary condition by the mixed-mode TCAD framework (Figure 3-5) according to the adding varied external capacitance between gate and drain.

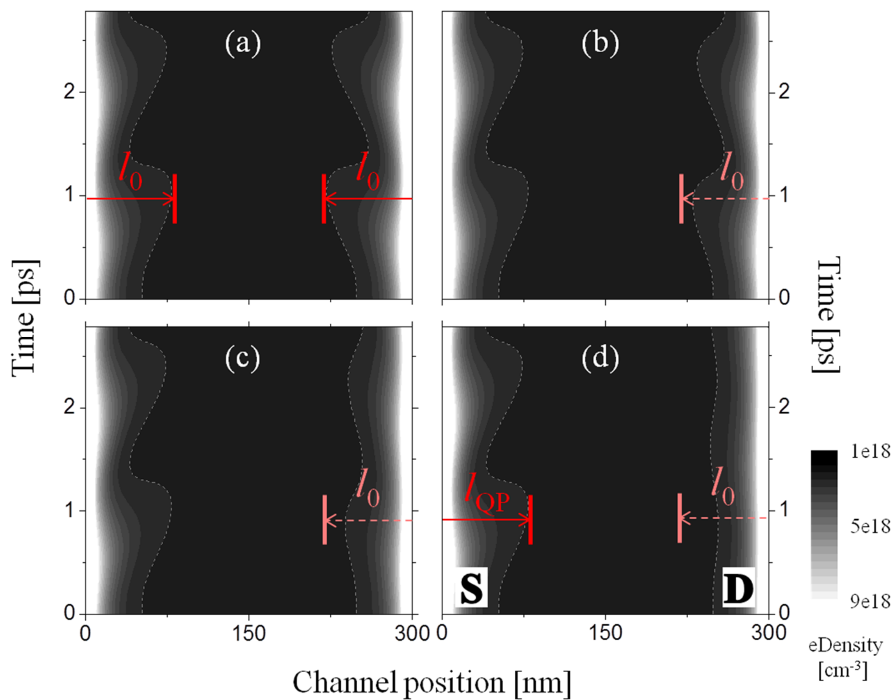

Figure 3-7. Contour plots of the channel electron density modulation according to the channel position at each time scale. (a) symmetry condition (b) C_{gd}= 1aF, (c) C_{gd}= 1fF, and (d) C_{gd}= 1pF.

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Figure 3-7(a) shows that the the channel 2DEG density modulation transient simulation at 0.7 THz has been demonstrated with TCAD framework based on the coupled continuity and Drude equation with normal electric field-dependent mobility model. These contour plots of the channel 2DEG density (at t_{ox}= 2.5 nm) modulation according to the channel position at each time scale depend on the symmetry. In terms of the symmetric condition, it is equal to propagation distance (l_0) at drain and source side. According to increasingly adding capacitance of 1 aF, 1 fF, and 1 pF as shown Figure 3-7(b), (c), and (d), respectively, their l at drain side are degraded as compared with l_0. If saturated asymmetric condition is satisfied with boundary condition at C_{gd} = 1 pF, the ac signal has been applied only at the source side (x= 0) as $V(0, t)$= 0.05sin(ωt) + V_g (=V_{th}; 0.42 V) and gate-to-drain voltage can be kept with DC gate voltage as $V(L_g, t)$= V_g= 0.42 V at x= L_g. From these contour plots of electron density by TCAD simulation, the l, which is the most important parameter as quasi-plasma 2DEG length (l_{QP}) in plasmonic THz detectors simulation, has been extracted as shown in Figure 3-7(d).

Figure 3-8 shows contour plots of the electron density for extracting the quasi-plasma 2DEG modeling by density (N_{QP}) and length (l_{QP}) according to t_{ox} variation. Electron density is sensitive as biased gate voltage in case of the ultra-thin gate dielectric. As thinner t_{ox}, electron density increases in 2DEG density modulation by improved subthreshold swing (SSW) of FET. N_{QP} is defined average of 2DEG density.

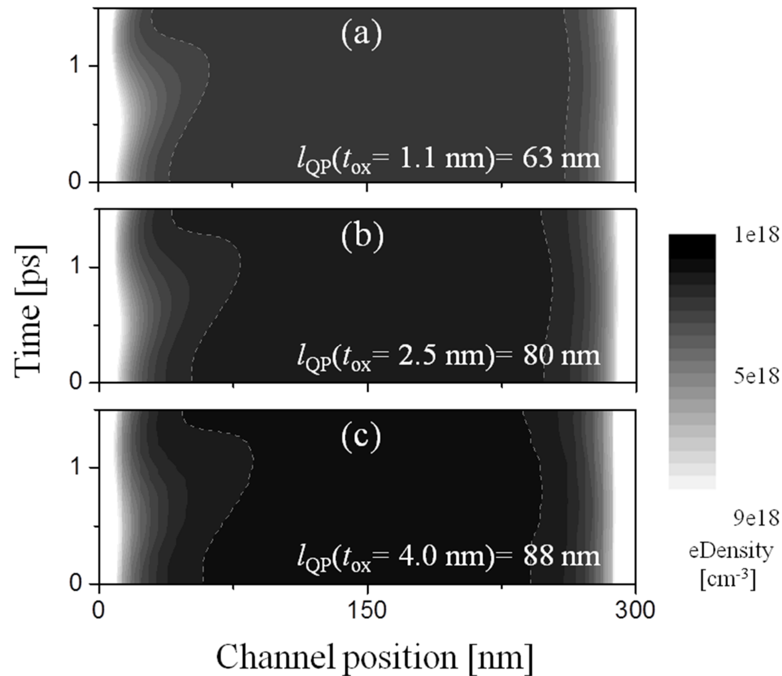

Figure 3-8. Contour plots of the channel electron density modulation according to the channel position at the same gate overdrive voltage V_g- V_{th}= 0. (a) N_{QP}= 6.5e18 cm^{-3} at t_{ox} = 1.1 nm, (b) N_{QP}= 6.1e18 cm^{-3} at t_{ox} = 2.5 nm, and (c) N_{QP}= 5.9e18 cm^{-3} at t_{ox} = 4.0 nm.

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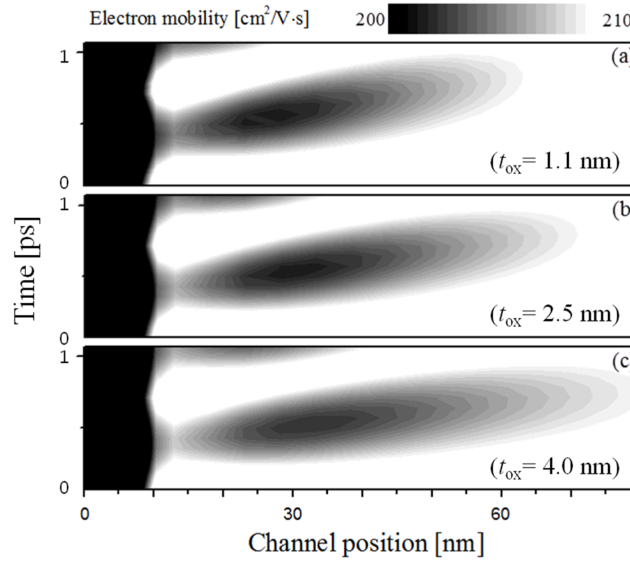

Figure 3-9. Contour plots of electron mobility in channel. (a) t_{ox} = 1.1 nm (b) t_{ox} = 2.5 nm, and (c) t_{ox} = 4 nm at the same gate overdrive voltage V_g- V_{th}= 0.

The propagation distance from the 2DEG density simulation results decreases by reducing t_{ox}. Since the modulation and propagation of a plasma-wave electron fluid ($l= s(\tau/\omega)^{0.5}$) definitely depend on the plasmon decay time $\tau= \mu m/e$ (where e is the electron charge), the parameter μ is the quality factor. These values of l can be varied by scattering, as plotted in Figure 3-9 which illustrates the electron mobility degradation according to the t_{ox} decrease because of the surface roughness scattering (SRS) by the enhanced normal electric field. Therefore, it can be expected that the value of l_{QP} decreases by more degraded electron mobility in thinner gate dielectric [46].

Figure 3-10 shows the simulation results of Δu, which has been normalized by maximum value near V_g= V_{th} with arbitrary unit, as a function of V_g at t_{ox}= 2.5 nm for investigating effects of key parameters about Δu by incorporating quasi-plasma 2DEG model with these physical parameters of l_{QP} and N_{QP} into channel region independently (Figure 3-5). The extracted Δu enhancement by N_{QP} as escalating is steeper effect than l_{QP} as diminishing. When l_{QP} is below 50 nm, it is same to the previous case because of l_{QP} equal to 2DEG length in drain side. Exceptionally, when N_{QP} is 1e18 cm^{-3}, device is induced with symmetry condition because of N_{QP}=N_{ch}. Figure 3-11 shows simulation results of the Δu as a function of V_g with various t_{ox}. In terms of N_{QP} as electron density of average (N_{QP}= 5e18 cm^{-3}) in channel surface, in accordance with the simplified theory of the non-resonant plasmonic wave THz detector, as t_{ox} scaled down from 4 to 1.1 nm, the higher Δu (about 21.6 percent) has been obtained in the sub-threshold region. When N_{QP} is electron density of average in propagation of a plasma-wave electron fluid, the more enhanced about 89.9 percent has been obtained. In order to enhance the performance throughout the device design such as t_{ox} scaling, increment of the density 2DEG modulation is primarily required for the high performance plasmonic THz detectors.

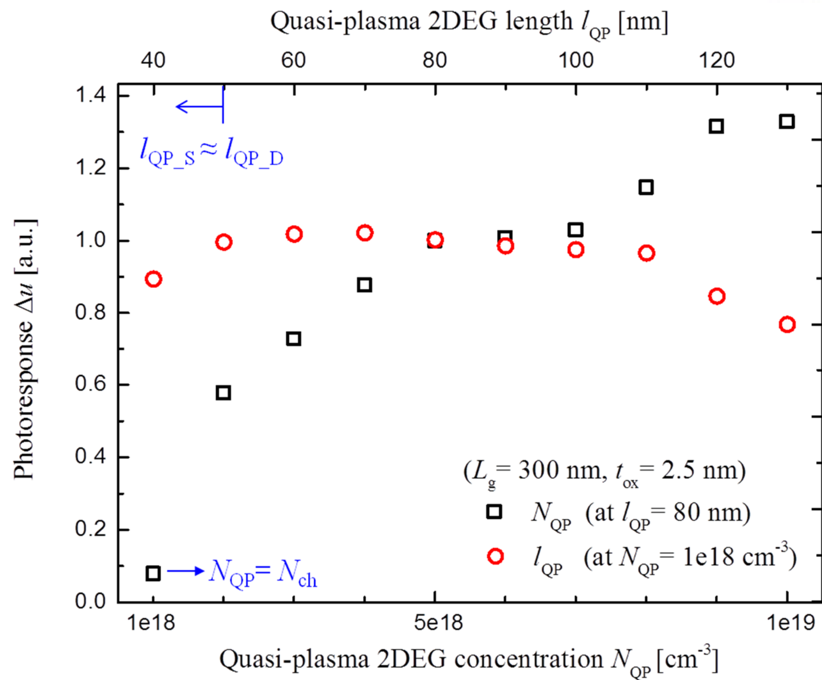

Figure 3-10. The simulation results of normalized Δu by the maximum point V_g with various N_{QP} (1e18~1e19 cm-3 at l_{QP}= 80 nm) and l_{QP} (40~130 nm at N_{QP} = 5e18 cm^{-3}) values based on a quasi-plasma 2DEG model at t_{ox}= 2.5 nm.

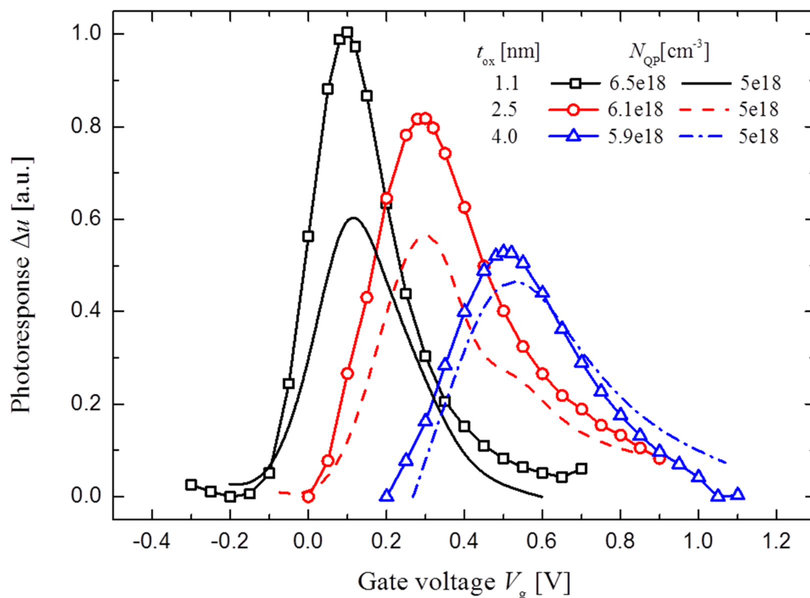

Figure 3-11. The simulation results of Δu as a function of V_g according to the variation t_{ox} (= 1.1, 2.5, and 4 nm) by incorporating the quasi-plasma 2DEG into channel region.

3.2.3 Non-quasi-static compact model

To characterize the transient delay components and detect speed performance, the equivalent circuit compact model of a MOSFET should be developed by including both the plasmonic power detection and the transit-mode non-quasi-static (NQS) has been modeled only by a distributed RC network [12,15] and numerical device simulation [52]; however, the reported NQS models with lumped elements fail to describe the plasmonic detection mechanism [53,54] and show the complexity for component analysis with segmented MOSFETs [55]. Moreover, even experimentally measured MOSFET delays during plasmonic power detecting operation have not been reported to date.

Figure 3-12 shows the equivalent circuit configuration of our advanced NQS model for plasmonic MOSFET operation. The background schematic is the calibrated TCAD device model with the experimental MOSFET fabricated by a non-self-aligned metal gate process [45]. The distinguished features of our proposed model in contrast with the Elmore model (dashed line box) [53] include the additional resistance of the gate (R_g), source (R_S), and drain (R_D) as well as the additional capacitance of the gate-to-drain ($C_{gd,ov}$) and source overlap capacitance ($C_{gs,ov}$) provided by the asymmetric overlap width of the source (W_S= 2 μm) and drain (W_D= 20 μm) under the same channel (L_g= 2 μm) and overlap lengths (L_{ov}= 4 μm), as shown in the inset of Figure 3-12.

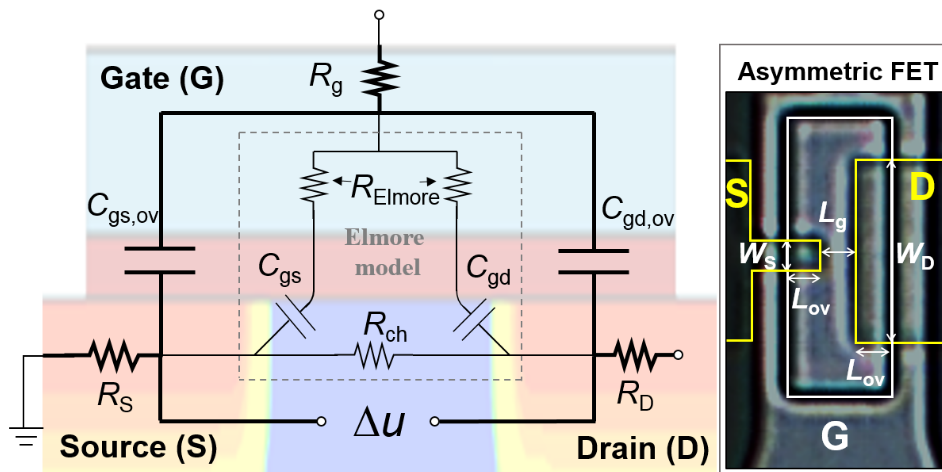

Figure 3-12. Equivalent circuit configuration of the advanced NQS model from an Elmore model (dashed box) for plasmonic MOSFET operation with a THz-wave detection output (Δu). Inset shows the top-view image of the fabricated asymmetric MOSFET from a non-self-aligned Al gate-lase process.

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To verify the model on the physical R_g effect in transit mode, large-signal DC transient gate delay characteristics according to Al (metal), NiSi (silicide), and poly-Si gate materials are compared with the numerical TCAD device simulation based on common material-dependent resistivity (ρ), ρ_{Al}= 2.7 μΩ-cm, ρ_{NiSi}= 21.5 μΩ-cm, and $\rho_{poly\text{-}Si}$= 135 μΩ-cm, as shown in Figure 3-13(a). Under the gate voltage (V_G) with increasing times of both 0.01 and 0.5 ns, the transient simulation results of the drain current (I_D) from our model are well-matched with the numerical 3D TCAD simulation results by describing the gate width (W= 20, 50 μm) effects on the I_D delay, while the Elmore model shows similar results with the quasi-static (QS) model that cannot describe the R_g effect on the transient delay characteristics. As shown in Figure 3-13(b), under the super-imposed small-signal ac voltage on the gate (v_{ac}= $v_a\sin 2\pi ft$, v_a= 20 mV, f=0.2 THz), the plasmonic THz power detection simulation capability of the proposed NQS model has also been verified by demonstrating the well-matched results of the DC output voltage (Δu) with calibrated TCAD and experimentally measured data [45]. The key model parameters of the asymmetric $C_{gd,ov}$= 56 fF(=10$C_{gs,ov}$) by the gate oxide thickness of t_{ox}= 50 nm under W_D= 20 μm(= 10W_S) with the same L_{ov}= 4 μm and R_g= 0.35 Ω for the Al gate are used based on the Hewlett simulation program with integrated circuit emphasis (HSPICE) BSIM3 model that is also calibrated for the fabricated Al-gate Si MOSFET.

Furthermore, the asymmetric $C_{gd,ov}$ effect on the peak Δu that is observed in the subthreshold region (V_G<V_T) as the non-resonant plasmonic detection theory [25] has also been verified with good agreement for the normalized peak Δu as a function of the ratio of $C_{gd,ov}$ and the intrinsic gate-to-channel capacitance ($C_{g,i}$) between the model and mixed-mode TCAD with external $C_{gd,ext}$= $C_{gd,ov}$, as shown in Figure 3-13(c). $C_{gd,ov}/C_{g,i} > 1$ is the key condition to enhance the performance (peak Δu) of the plasmonic THz detector [52]. In this work, the values of peak Δu from the experimental MOSFET with various asymmetry ratios (η_a= $C_{gd,ov}/C_{gs,ov}$= $C_{gd,ov}/2C_{g,i}$) from η_a= 1 (symmetry) to 10 have also been plotted exactly on the HSPICE simulation results from the proposed NQS compact model.

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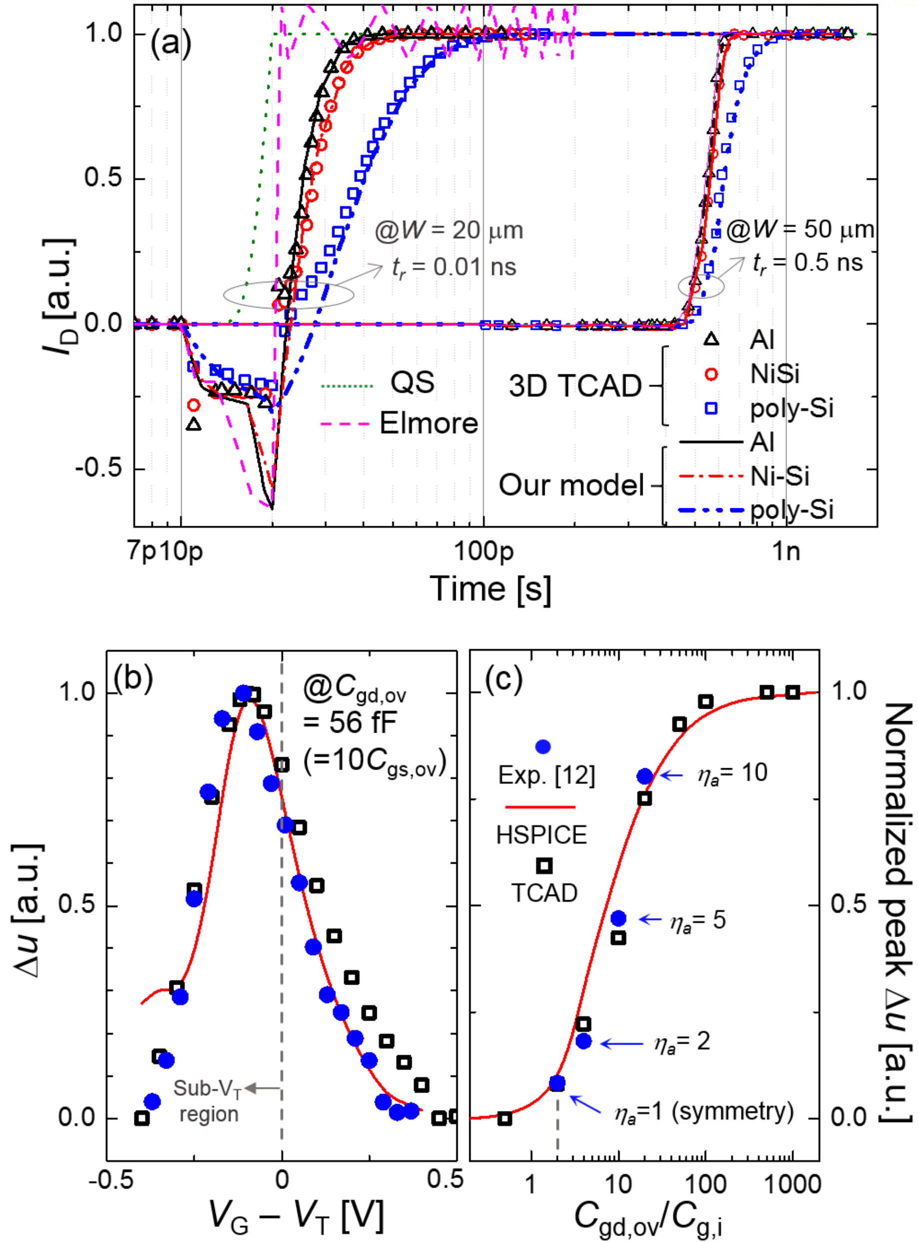

Figure 3-13. (a) Transient gate delay simulation results for Al, NiSi, and poly-Si gate materials from the proposed NQS model compared with 3D TCAD. (b) The well-matched HSPICE simulation results of Δu as a function of the gate overdrive voltage (V_G - V_T) at $C_{gd,ov}$(= 10$C_{gs,ov}$)= 56 fF and (c) the normalized peak Δu as a function of $C_{gd,ov}/C_{g,i}$ with experiment and mixed-mode TCAD.

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3.3 Device fabrication

First of all, to investigate detector performance of asymmetry ratio and delay, non-self-aligned process is adopted as relatively simple fabrication. Figure 3-14 shows that there are 4 mask layers: the first active layer for doping region of source and drain, the second gate open layer for gate-to-channel coupling region overlapped with source and drain, the third contact layer for via hole contact between metal and doping regions, the fourth metal layer for metallization of gate, source and drain electrodes, respectively. By using this layer sequence, the asymmetric source and drain doping region, which should be overlapped with gate electrodes, can be easily designed at the first layer step in non-self-aligned structure. The THz detector was fabricated in Ulsan National Institute of Science and Technology (UNIST) central research facilities (UCRF). The *p*-type boron-doped Si (100) wafer has doping concentration (N_a) of 1 x 10^{15} cm^{-3} and 200-μm-thick. After the native oxide was removed by wet cleaning, the thickness field oxide layer of 600 nm was thermally grown at 1100 °C for device isolation. By dry etching in CHF_3/CF_4 reactive-ion plasma, the field oxide was removed at the drain/source region.

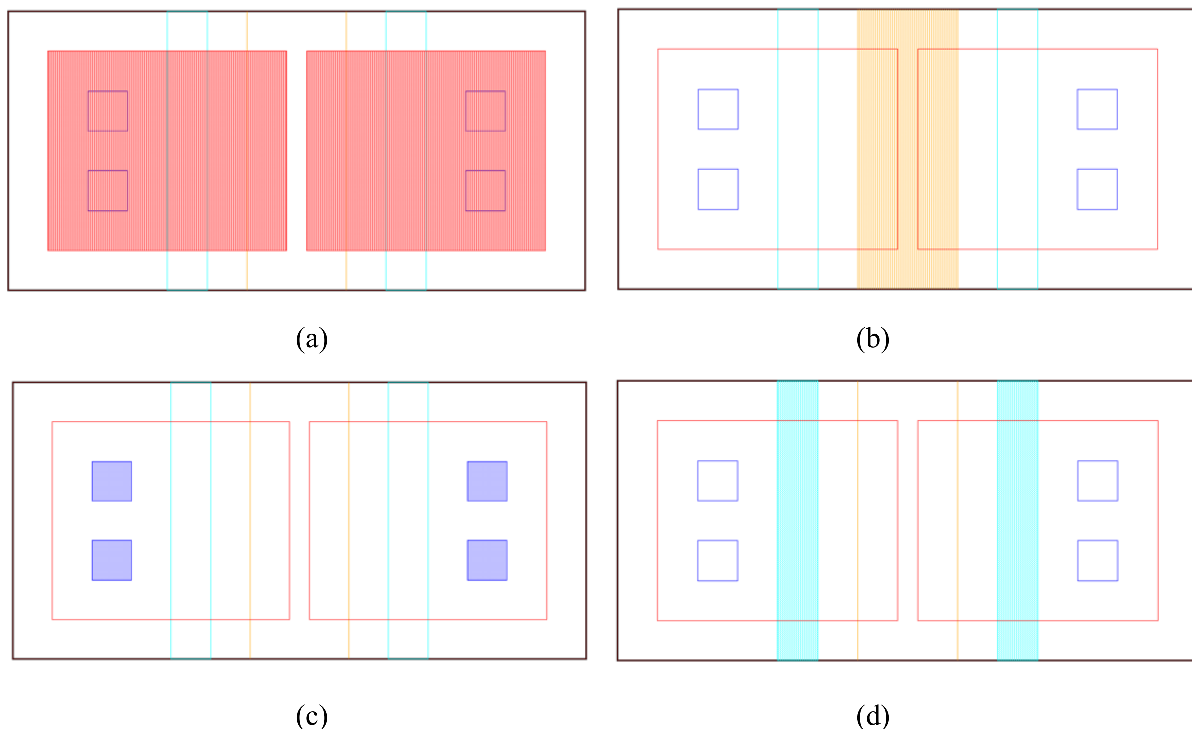

Figure 3-14. There are 4 mask layers: (a) the first active layer for doping region of source and drain, (b) the second gate open layer for gate-to-channel coupling region overlapped with source and drain, (c) the third contact layer for via hole contact between metal and doping regions, (d) the fourth metal layer for metallization of gate, source and drain electrodes, respectively.

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At this active layer as the first photolithography step, the drain/source region can be formed asymmetrically or symmetrically by varying the widths of the drain and source, and the L_g can be defined with the distance between the drain and the source at the same time (see Figure 3-15(a)). After the formation of the *n*-type source and drain region by the $POCl_3$ diffusion process with the surface concentration of 3×10^{19} cm^{-3} and a junction depth (X_j) of 250 nm, the 200-nm-thick inter-layer dielectric (ILD) oxide was deposited uisng plasma-enhanced chemical vapor deposition (PECVD). Subsequently, the gate open layer defines the gate-to-channel coupling region and a thermal oxide thickness of 50 nm was grown at 950 °C as the gate dielectric. Aluminum (including 1% Si) as the metal layer including an antenna pattern was deposited by dc sputtering and finally sintered at 450 °C, after opening the contact holes at the source and drain regions. The metallurgical channel length can be estimated to be 1.5 μm considering the diffused junction depth from L_g= 2 μm in the non-self-aligned structure. The V_{th} extracted from the I_d-V_g dc curves at V_d= 1 V was within the range of V_{th}= 0.4-0.5 V for all devices (Figure 3-15(b)).

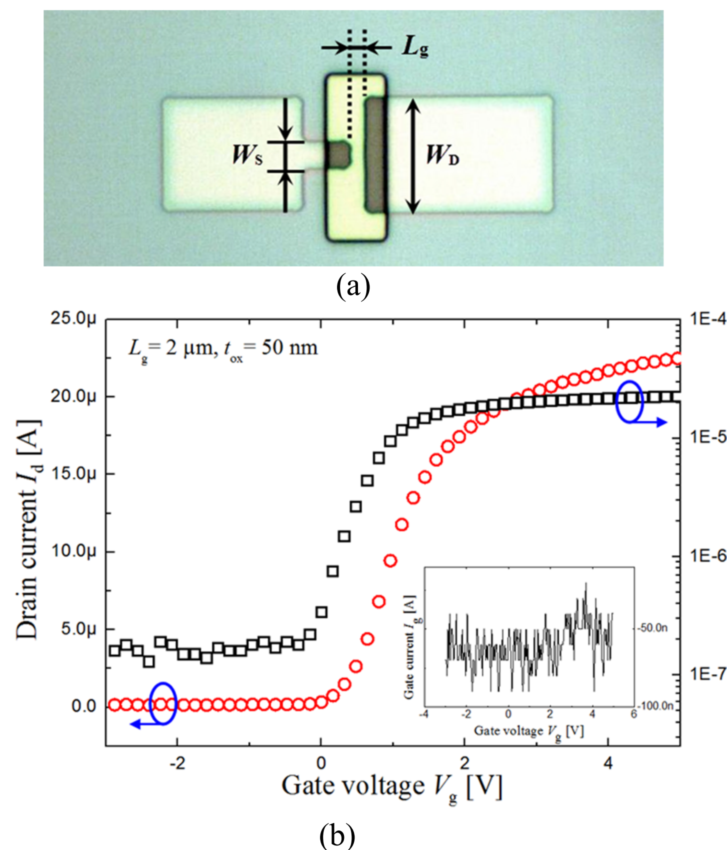

Figure 3-15. (a) Micrograph (top view) of the fabricated Si FET with asymmetric source and drain. W_D and W_S with corresponding asymmetry ratios (η_a= W_D / W_S) of 1, 2, 5, and 10. (b) DC transfer curves of the fabricated Si-FETs. The V_{th} is extracted from these curves at V_d= 1 V. Inset shows the negligible gate current for all gate voltages.

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Figure 3-16 shows a photograph of the fabricated THz detector based on FET integrated with a bow-tie antenna, which is connected between the gate and the source terminal. By finite-difference time domain (FDTD) antenna simulation, the architecture of the bow-tie antenna has been designed with the angle θ= 74° and radius r= 51 μm. At this point, it should be noted that the antenna design parameters are optimized since the radius of r= 51 μm has been selected by mainly targeting for 0.4 THz wavelength (λ/4= 187.5 μm) and the angle of θ= 74° is considered for bandwidth broadening for the 0.2-0.4 THz wideband detection, which is the advantage of the bow-tie antenna structure for the non-resonant plasmonic THz wave detection regime. The micrograph shows the fabricated Si FET-based THz detector with the asymmetric drain and source structure. The asymmetric structure is designed by the split of source width W_S as 20, 10, 4, and 2 μm with the fixed drain width W_D= 20 μm the corresponding the asymmetry ratio η_a (= W_D/W_S, where W_D and W_S are the gate-overlapped drain and source widths, respectively) would be 1, 2, 5, and 10, respectively.

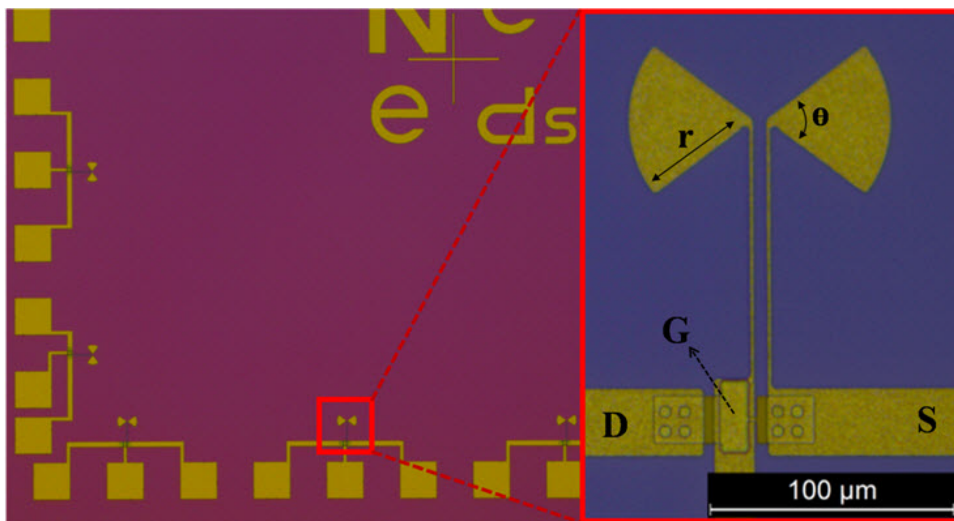

Figure 3-16. Photograph of the fabricated THz detector samples. The inset shows a micrograph (top view) of the fabricated Si FET with asymmetric structure. The bow-tie antenna with the r= 51 μm and θ = 74° has been integrated as the electrode metal layers of the gate and source.

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Secondly, self-aligned process by using 65-nm CMOS technology is performed for demonstrating multi-pixel array detector. Figure 3-17(a) and (b) shows the schematics of the layout and cross-sectional view of the fabricated asymmetric MOSFET for the plasmonic THz detector by using 65-nm CMOS technology, respectively. As shown in the plan-view of layout (Figure 3-17(a)), the asymmetric channel on the active layer has been newly designed with a different source (W_S) and drain width (W_D) surrounded by a shallow trench isolation (STI) process in a self-aligned poly-Si gate-first standard process, while the cross-sectional view of the asymmetric MOSFET is the same as the symmetric one (Figure 3-17(b)). The fabricated n-MOSFETs have a nominal L_g= 200 nm for asymmetric overlap capacitance with W_S= 200 nm and W_D= 2 μm on t_{ox}= 2 nm (effective-oxide thickness (EOT)= 1.9±0.15 nm). This is thinner than the t_{ox}= 10 nm used in our previous MOSFET [19], and can expect the more enhanced plasmonic channel electron density modulation induced by the thinner gate dielectric thickness [56].

As shown in the transfer I_D-V_G curve of Figure 3-18, successful dc characteristics have been obtained with a well-suppressed gate current (I_{GS}) below pico-ampere and a good subthrehold swing (SSW) of 72 mV/dec in the fabricated asymmetric MOSFET ($W_S << W_D$). From the linear region at low drain bias of V_{DS}= 0.1 V, the threshold voltage (V_T) has been extracted as V_T= 0.29 V, which is a key criterion for a non-resonant mode ($V_{GS} < V_T$) operation in the plasmonic power detection mechanism. The inset shows the linear and log-scale of transfer I-V curve in the saturation region at V_{DS}= 1 V, which indicates that an on-current (I_{ON}) of 0.64 mA/μm is relatively lower than the target value of 0.9 mA/μm provided by 65-nm CMOS foundry, owing to marginally increased L_g for asymmetric channel design with more reduced W_S than W_D.

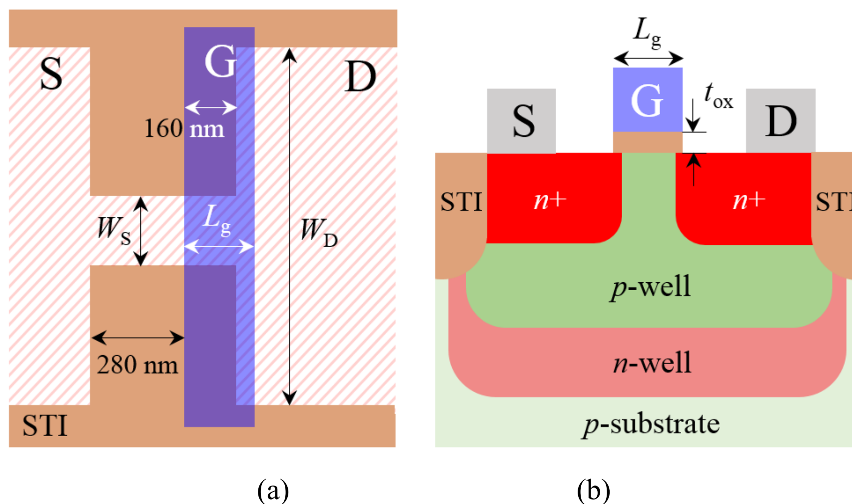

Figure 3-17. (a) Layout design of asymmetric channel with different source (W_S) and drain width (W_D) in self-aligned poly-Si gate process. (b) Cross-sectional view of the fabricated asymmetric MOSFET with L_g= 200 nm and t_{ox}= 2nm.

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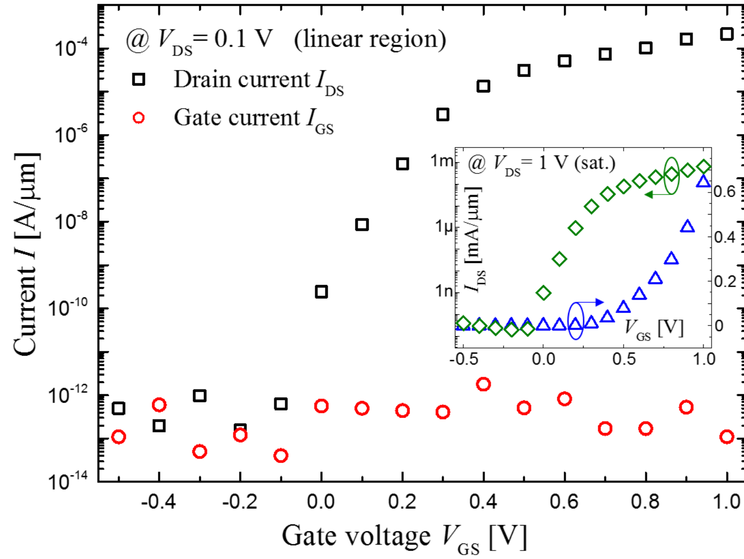

Figure 3-18. Measured transfer I_{DS}-V_{GS} curves of the fabricated n-channel asymmetric FET. The extracted V_T= 0.29 V and SSW= 72 mV/dec at V_{DS}= 0.1 V. Inset shows I_{DS}-V_{GS} curves in saturation region at V_{DS}= 1 V with I_{ON}= 0.64 mA/μm. All the measured I_{DS} are normalized by source width of W_S= 200 nm.

For absorbing THz wave with a sub-millimeter wavelength of 0.3~3 mm (0.1 ~ 1 THz), sub-micron or nanoscale asymmetric MOSFET should be integrated with the relatively large submillimeter dimension of antenna as a front part of the THz detector, as shown in Figure 3-19, which is the top-vie w micrograph image of the fabricated plasmonic THz detector. The integrated patch antenna on the top metal Cu layer, with a 2.4 μm-wide feeding line (EA), was designed at 0.2 THz resonance (i nset), which has the bandwidth of 11 GHz (S_{11} < -10 dB at 192~203 GHz) with a low characteristic impedance of Z_a= 50 Ω [57]. This is distinguished from a few kΩ-level high-impedance antenna design [44], to make the difference with a low input impedance (Z_{gs}) of the asymmetric MOSFET as small as possible. This power loss reduction by impedance matching has been confirmed by low-impedance antenna-coupled FET [46]. In this work, low-impedance MOSFET is also consistently designed with Re{Z_{gs}}= 50 Ω at 0.2 THz for the impedance matching as shown in the inset of Figure 3-19. Figure 3-20 illustrates the cross-sectional schematics of the patch antenna-coupled FET for THz wave power detection. By exploiting intermediate metal layers with low-κ inter-dielectric layer (ILD) in CMOS foundry process, the ground plane (B1) with a feeding line (EA) has been introduced below the patch antenna to minimize the loss of THz wave power through a radiation into a relatively high-κ Si substrate, as in our previous in-plane antenna structure [46]. This vertical integration of patch antenna has usually been adopted for high antenna efficiency in a CMOS-based plasmonic THz detector [12], [14]. Thus, fair comparison of detecting performance can be expected.

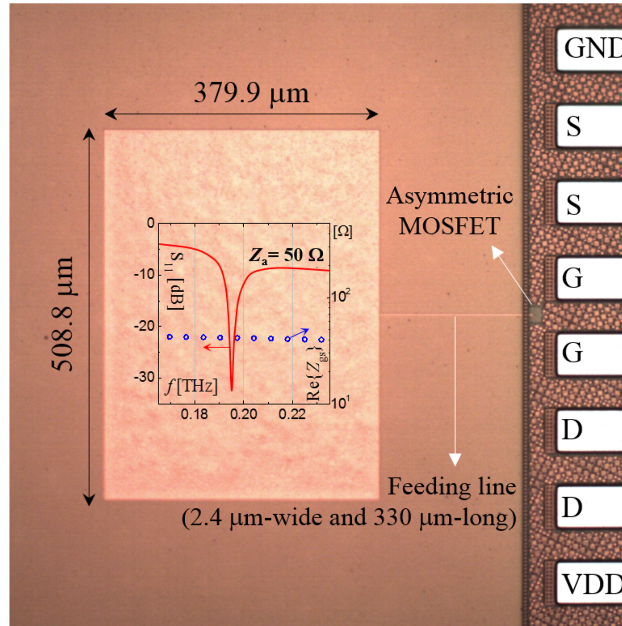

Figure 3-19. Top-view micrograph image of the fabricated asymmetric MOSFET integrated with patch antenna on top metal layer. Inset shows the simulation results of integrated patch antenna response (S_{11}) at Z_a= 50 Ω and FET impedance (Re{Z_{gs}}) as a function frequency around 0.2 THz.

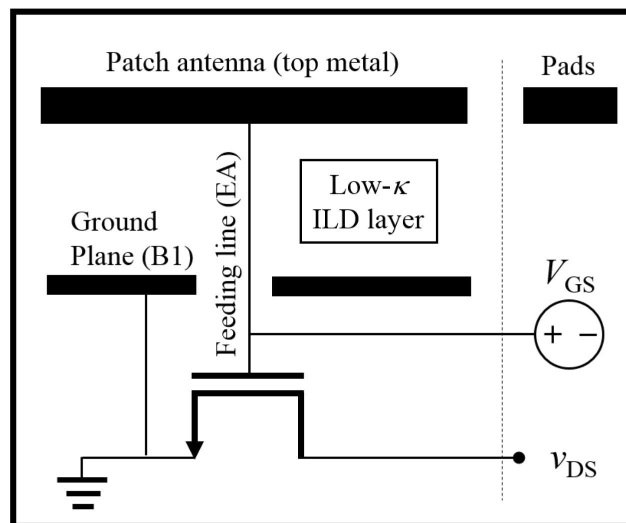

Figure 3-20. Cross-sectional schematic of a patch antenna-coupled FET with ground plane (B1) and feeding line (EA) on the intermediate metal layers having low-κ ILD layer.

3.4 Device characteristics

3.4.1 Plasmonic detection characteristics

Figure 3-21 shows the experimental setup for the Δu of the fabricated plasmonic THz detector. The THz radiation with f= 0.2 THz was generated by a gyrotron source as higher-order mode resonator, which enables real-time detection with the continuous-wave (CW) method since it is stable in the sub-THz frequency regime [58,59]. The THz wave was emitted through the waveguide, and reflected to off-axis paraboloidal (OAP) mirrors for collecting wave. The lock-in amplifier provides band-pass filtering approximately at a chopping frequency of 200 Hz, and thus, the post-detection background noise can be reduced significantly.

Figure 3-22 shows the Δu results of the fabricated THz detector with the asymmetric structure for 0.2 THz radiation. by the FET-based plasmonic detection theory [25,27], Δu appears in the form of dc voltage at the sub-threshold region ($V_g < V_{th}$), which indicates that the fabricated Si FET-based THz detector is successfully operated in the non-resonant broadband sub-THz detection regime at T= 300 K. Furthermore, reproducible Δu are obtained for various detectors with different asymmetry ratios (η_a= 10 and 2) and a much higher Δu for the detectors with η_a= 10 than η_a= 2. The Δu in the plot of Figure 3-22 has been normalized by the peak point with η_a= 10 to compare the relative Δu results clearly for each sample group with the different η_a values. In our proposed asymmetric structure, these asymmetric boundary conditions internally arise owing to the difference in the gate overlap capacitances between the drain and the source; thus, Δu starts to appear and increases as the structural asymmetry between the drain and the source areas under the gate increases.

As shown in Figure 3-23, the independent effects of the antenna and structural asymmetry on the signals of non-resonant plasmonic responses to 0.2 THz radiation from the gyrotron source have been successfully observed through the split experiments of the fabricated Si FET THz detectors with or without (w/o) the antenna structure. The R_v has been normalized by the peak value of the case w/o the antenna (red circle) with an arbitrary unit to demonstrate the quantitative effect of the antenna on R_V enhancement. In comparison with the symmetrical source and drain structure with the η_a= 1 as reference, the Δu of the w/o antenna structure with η_a= 10 has been enhanced by about 21.6 times, which is the structural asymmetry effect. In terms of the bow-tie antenna effect, the photoresponse of the antenna integrated structure with η_a= 10 has been enhanced by about 60 times compared with the case w/o the antenna structure.

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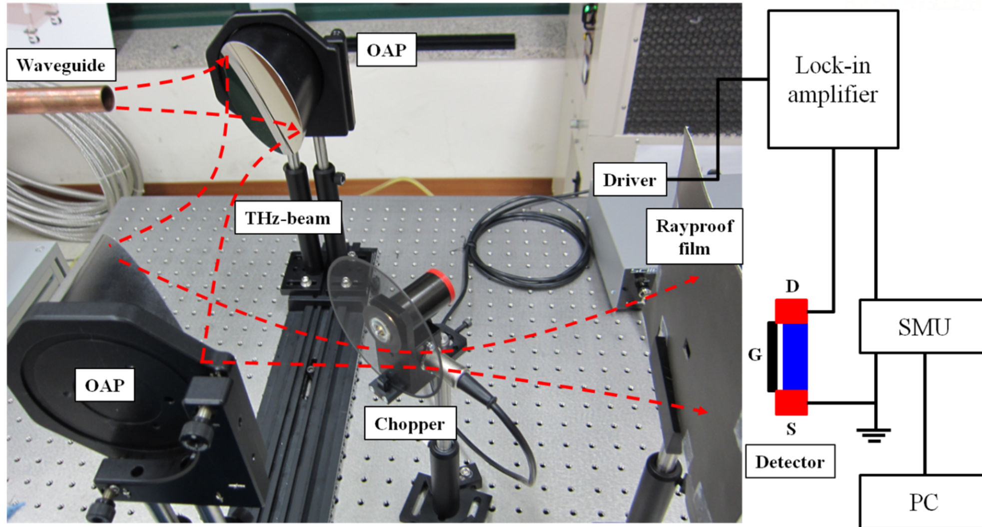

Figure 3-21. Experimental setup with optical transmission line system for the R_v of the fabricated plasmonic THz detector.

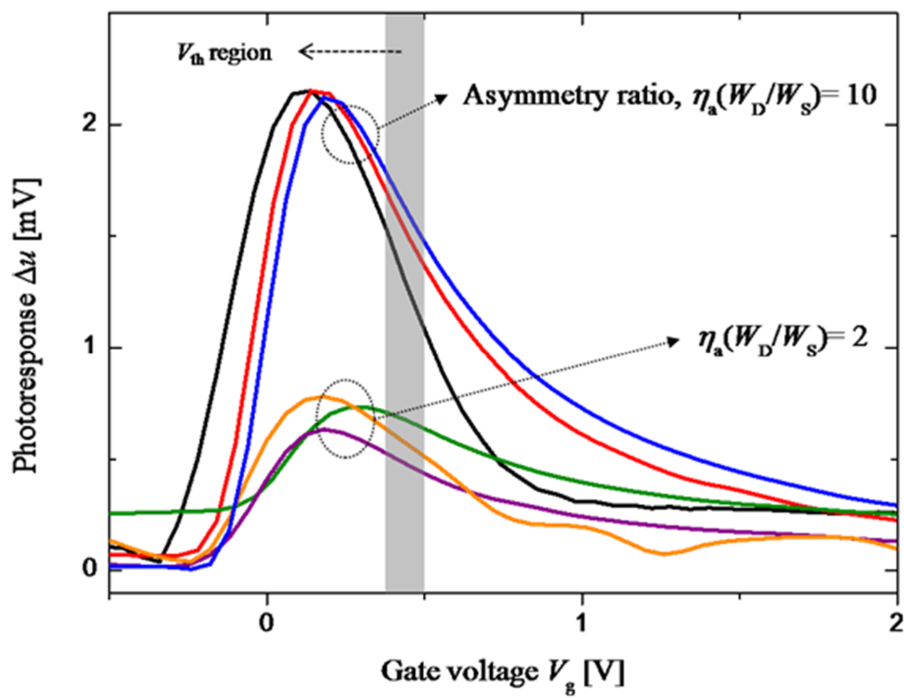

Figure 3-22. Experimental results of the Δu of Si FET response to 0.2 THz radiation. The Δu as a function of the V_g for various Si FETs with different asymmetry ratios: η_a= 10 and 2.

For this best photoresponse of Δu= 6 mV, the absolute value of R_v before normalization can be estimated by the following effective power estimation. Considering the actual radiated area of the detector (A_a) as 0.35 μm^2 with a beam size A_{beam}= 12.6 x 10^8 μm^2 (= πr_{beam}^2 where the beam radius r_{beam}= 2 cm), the actual consumed power P_a is P_{total} x A_a/A_{beam}= 0.027 mW (where P_{total}= 10 W) and then, R_v = Δu/ P_a= (6 mV)/ (0.027 mW)= 222 V/W. This estimated R_v is comparable to previously reported values (200-500 V/W) without on-chip amplification from Si FET-based plasmonic THz detectors [12,24].

Figure 3-24 shows the enhanced peak voltages of the photoresponse Δu (mV) as a function of the increase in η_a. The average (symbols) and value distribution (error bars) from 5-20 samples for each η_a indicate that the performance enhancement by the structural asymmetry is reproducible and controllable. Based on the same antenna effect on the performance, the enhancement of the Δu can be achieved by increasing η_a in a structural layout design. The Δu have been enhanced on average by about 6.1, 21.7, and 36.2 times linearly proportionally to the η_a increases of 2, 5, and 10 times from the symmetric structure (Δu of 0.71 mV), respectively.

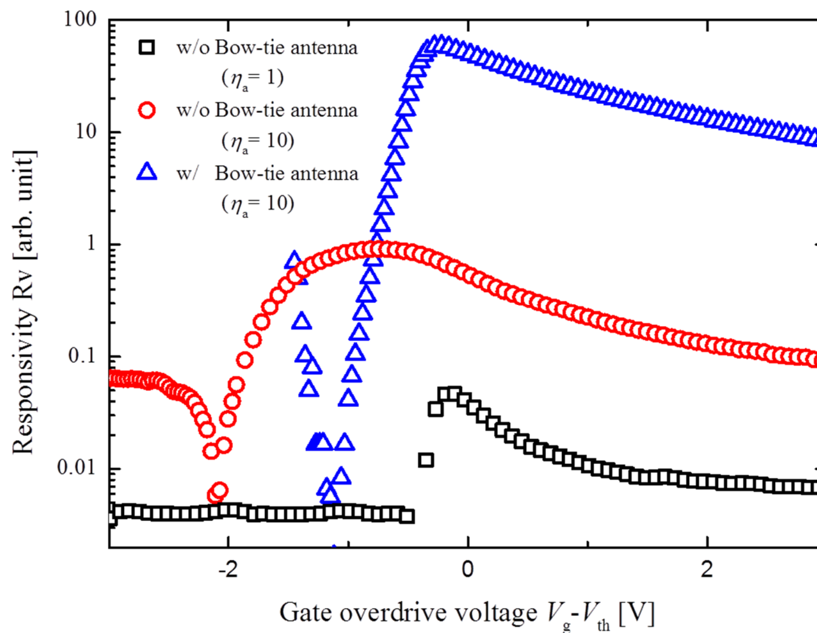

Figure 3-23. Experimental results of the THz detector response signal to 0.2 THz radiation.

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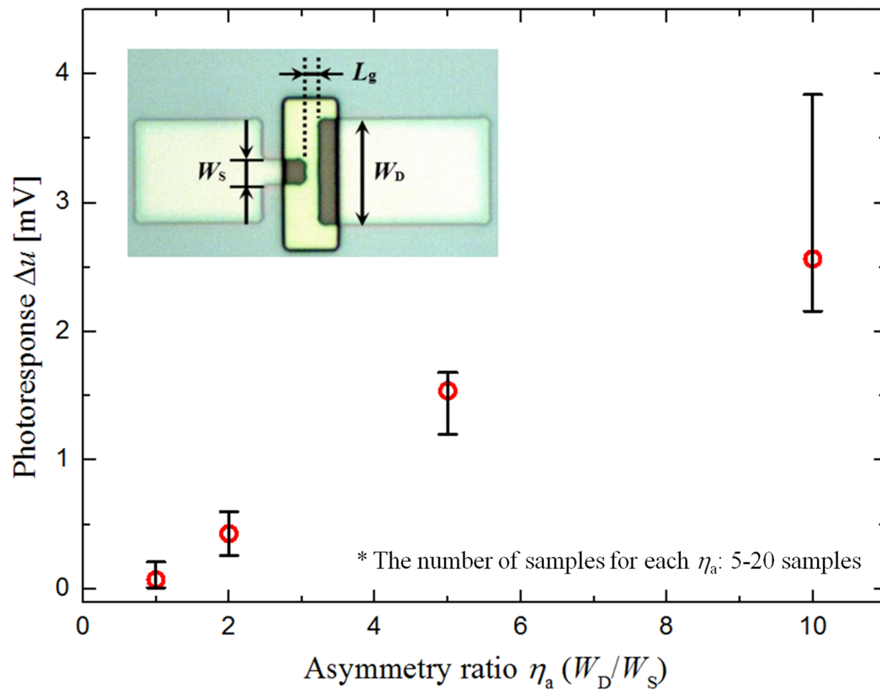

Figure 3-24. Experimental results of the Δ*u* for the different asymmetry ratios. W_D = 20 μm and W_S = 2 (20 samples), 4 (12 samples), 10 (7 samples), and 20 μm (5 samples) with corresponding asymmetry ratios ($\eta_a = W_D / W_S$) of 10, 5, 2, and 1 (symmetric), respectively.

3.4.2 Transient response of detector

Figure 3-25(a) shows the transient simulation results of $\Delta u(t)$ with the THz detection delay (t_d) and overshoot voltage (U_{os}) based on the established NQS compact model by modulating the DC $V_G(t)$ between turn-on V_G= -0.4 V and turn-off V_G= 0 V with a modulation frequency of f_m= 2 MHz and a rising time of t_f= 1 ns under the always-on v_{ac} with the THz incoming wave. The t_d can be defined as t_d= $t(\Delta u$= $0.1U_{os}) - t(\Delta u$= $0.9U_{os})$ with U_{os}= $\Delta u(t$= $t_f) - \Delta u$(saturated). In this simulation, $C_{gd,ov}$= 1 pF is used for clear observation of t_d and U_{os} by a strong asymmetric boundary condition of $C_{gd,ov}$ >> $C_{gs,ov}$= 5.6 fF under the duty period of 500 ns by f_m= 2 MHz.

The asymmetric $C_{gd,ov}$ effect on t_d and U_{os} in this transient $\Delta u(t)$ simulation has been investigated as shown in Figure 3-25(b). As expected, the t_d would increase (decrease) monotonically with an increase (decrease) in $C_{gd,ov}$, while U_{os} would be saturated up to the transition magnitude of V_G= 0.4 V at $C_{gd,ov}$> 1 pF and would then decrease because of the divided voltage reduction at the output drain node by decreasing the $C_{gd,ov}$ (upper capacitor) at the fixed drain junction capacitance (lower one); this is considered to be 1.5 fF << $C_{gd,ov}$ in our MOSFET design. As shown in the inset of Figure 3-25(b), it is newly found that the intrinsic detection delay of $t_{d,int}$ is obtained as 2.76 ns by only considering the MOSFET NQS compact model from Figure 3-12, with $C_{gd,ov}$= 56 fF.

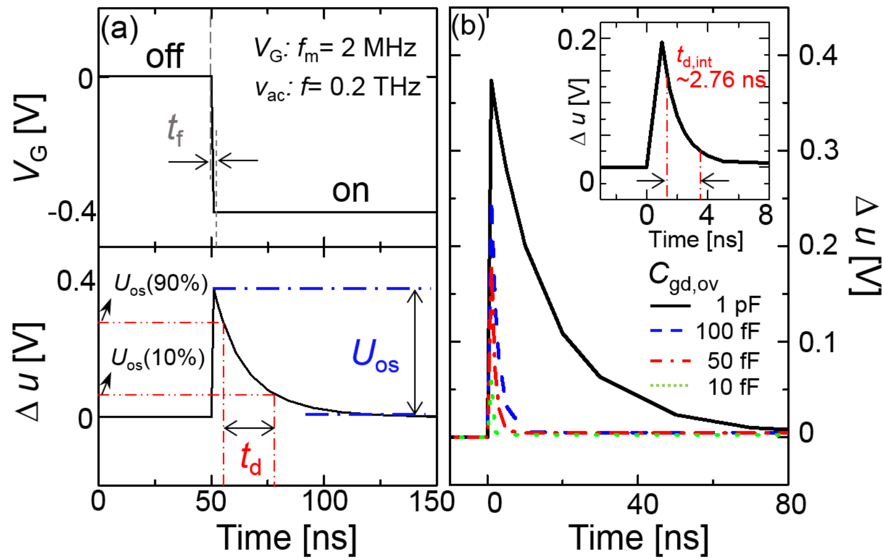

Figure 3-25. (a) Transient simulation results of $\Delta u(t)$ by $V_G(t)$ modulation with f_m= 2 MHz and t_f =1 ns. Delay (t_d) and overshoot (U_{os}) are defined. (b) Transient simulation results of Δu with varying $C_{gd,ov}$= 10, 50, 100 fF, and 1 pF. Inset shows the intrinsic THz detection delay of $t_{d,int}$= 1.14ns at $C_{gd,ov}$ = 56 fF.

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Figure 3-26(a) shows the measured delay results of a single pixel from the packaged multi-pixel detector with a multiplexer control circuit on a plastic chip board (PCB) with the same V_G on-off modulation with f_m= 2 MHz. It is noted that the measured delay of 76.3 ns is much longer than the intrinsic delay (~3 ns) by the model because of the parasitic components from bonding wires/pads and DC signal lines on the PCB. Since the THz radiation (v_{ac}) from a 0.2-THz gyrotron source is transferred onto the antenna separately from V_G [46], the parasitic gate capacitance ($C_{g,p}$) and gate-to-drain capacitance ($C_{gd,p}$) are modeled between the modulated V_G and v_{ac} in addition to the parasitic drain capacitance ($C_{d,p}$) from the physical PCB wires and pad signal lines, as shown in Figure 3-26(a) (inset). Then, these parasitic component effects on the t_d and U_{os} could be characterize by additionally connecting the external gate capacitance ($C_{g,ext}$) based on the equivalent circuit model in the inset of Figure 3-26(a). First, under the fixed $C_{g,ext}$= 0.5 nF with $C_{gd,p}$= 0.2 pF and $C_{d,p}$= 1.5 pF, as shown in Figure 3-26(b), the decrease of U_{os} with the increase of $C_{g,p}$ is simulated since the divided voltage at the input gate node decreases by increasing $C_{g,p}$ (lower capacitor) at the fixed $C_{g,ext}$ (upper one) as in the case of the intrinsic $C_{gd,ov}$ effect (Figure 3-25(b)). As shown in Figure 3-26(c), however, the increases of $C_{d,p}$ (0.75 - 3 pF) and $C_{gd,p}$ (0.1 - 0.4 pF) mainly increase the output t_d of $\Delta u(t)$ without an effect on U_{os} because the sum of $C_{d,p}$ and $C_{gd,p}$ determines the total capacitance at the drain output node.

Based on the effects of the parasitic component on t_d and U_{os}, the measured $\Delta u(t)$ results by experimentally connecting $C_{g,ext}$ (0.125 - 1 nF) on the gate signal line of the detector on the PCB have been well reproduced by simulation results (symbols) with parasitic components of $C_{g,p}$= 0.5 nF, $C_{gd,p}$= 0.2 pF, and $C_{d,p}$= 1.5 pF (Figure 3-26(a)). Finally, the measured total delay of a plasmonic detector pixel is confirmed to be below 100 ns; this delay is much smaller than the general display pixel delay of a few micro-seconds, and thus, it can guarantee a real-time multi-pixel THz imaging operation.

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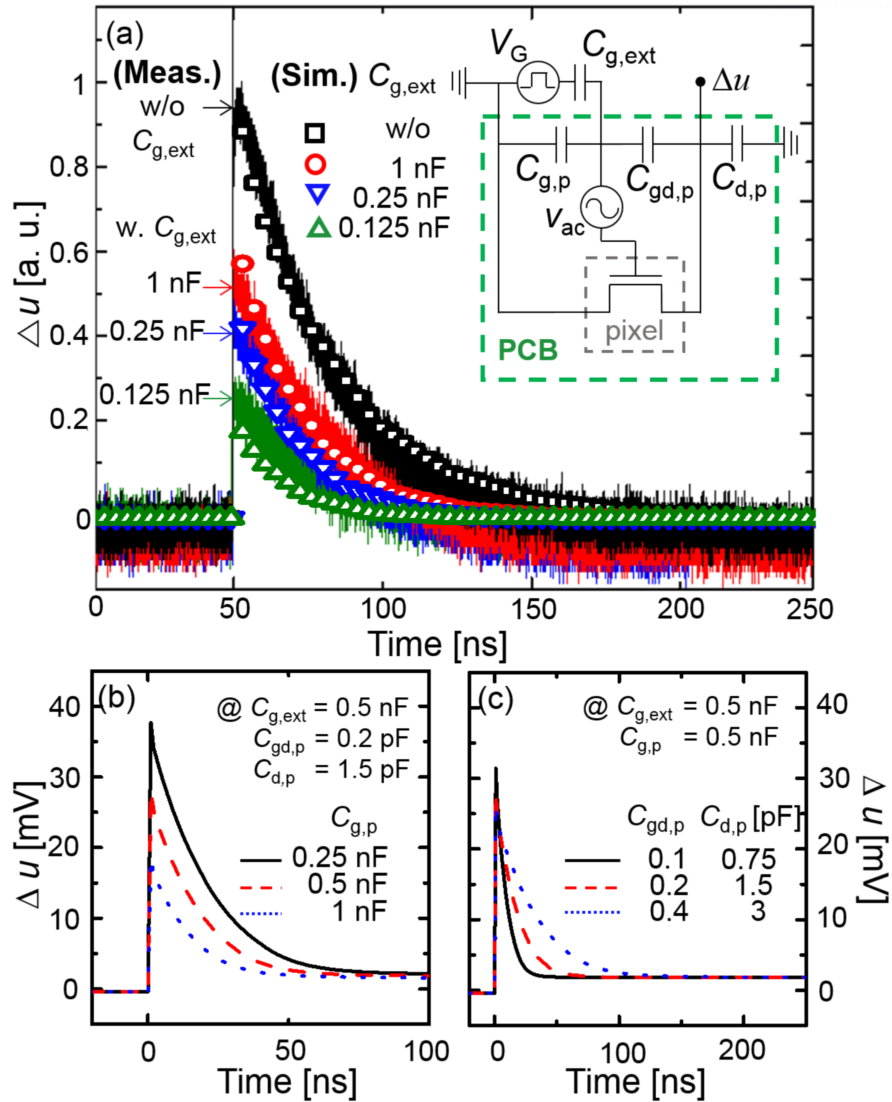

Figure 3-26. (a) Measured single-pixel transient delay results on the packaged multi-pixel detector by the external $C_{g,ext}$ connection and the well-matched HSPICE simulation with $C_{g,p}$= 0.5 nF, $C_{gd,p}$= 0.2 pF, and $C_{d,p}$= 1.5 pF based on the expected parasitic circuit model with $C_{g,ext}$ (inset) (b) Simulation results of Δu according to $C_{g,p}$ and (c) $C_{gd,p}$ and $C_{d,p}$ based on the model.

3.4.3 Responsivity and noise equivalent power

Figure 3-27 shows the measurement setup for a photoresponse (Δu) of the fabricated multipixel array plasmonic THz detector using a direct connection of an oscilloscope (LeCroy Wav-erunner 104Xi-A) to the drain node of the asymmetric MOSFET without a chopper and lock-in amplifier since directly measurable high Δu for real-time THz detection is expected. Radiation at f= 0.2 THz (fundamental mode) was generated by a high-power gyrotron source. Then, the THz beam, focused by OAP mirrors, is filtered through a grid polarizer for minimizing the interference according to the antenna polarity by changing an elliptic beam shape into a horizontal THz wave polarity [42]. Finally, a diverged THz beam with a beam diameter of d= 58 mm at the detector position is absorbed by the patch antenna, which leads to the output dc signal of Δu at the drain node connected by the oscilloscope.

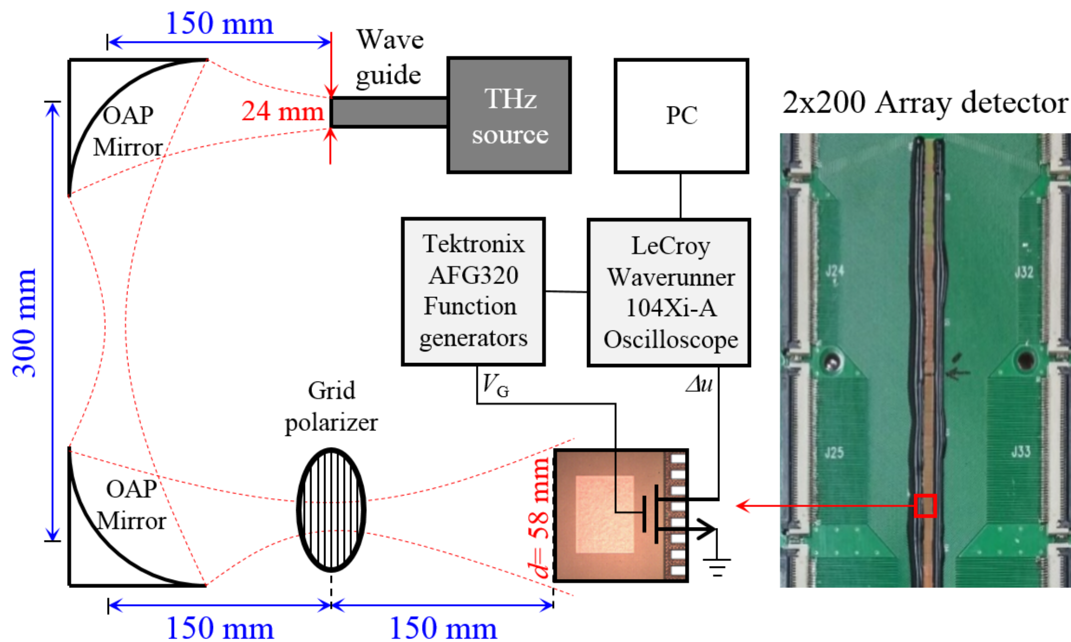

Figure 3-27. Photoresponse (Δu) measurement setup for the fabricated multi-pixel 2x200 array plasmonic detector using 0.2 THz gyrotron source with a direct connection of oscilloscope to the output drain node of asymmetric MOSFET.

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Figure 3-28(a) shows the measured results of Δu from the patch antenna-coupled asymmetric MOSFET at 0.2 THz radiation. The peak Δu appears at the subthreshold region (V_{GS}= 0.2 V < V_T= 0.29V) according to the non-resonant mode plasmonic THz detection theory, which is solely a THz wave detection result since there is no response when radiation from the THz source is off. The peak value of Δu = 110 mV is highly enhanced from the 32 mV of our previous non-self-aligned FET with the same asymmetry (η_a= W_D/W_S= 10) [46], owing to increased 2DEG density modulation by the self-aligned channel structure with a scaled-down EOT as well as a vertically integrated antenna.

Furthermore, as shown in the inset of Figure 3-28(a), Δu was immediately changed from 104 mV to 10 mV by modulating V_G from turn-on (V_{GS}= 0.2 V) to turn-off (V_{GS}= 0.8 V) through the function generator (Tektronix AFG320) with a 1 MHz modulation frequency, respectively. Therefore, the estimated detector delay (< 100 nsec) can be enough to guarantee real-time (e.g. 24 fps) THz detection by a multipixel array detector without a lock-in or electronic-circuit amplifier.

Based on the consistent actual power (P_a= 0.072 mW) estimation from the measured beam profile and THz source power at detector position [46], R_v (= $\Delta u/P_a$) has been plotted as a function of V_{GS} in the left y-axis of Figure 3-28(b). From the peak Δu= 110 mV at V_{GS} = 0.2 V, the highest value of R_v has been obtained as 1.5 kV/W, which is almost doubled from the previous result of 0.8 kV/W. NEP (= N/R_v, where N is the total noise of the detector), which is the most significant performance metric for imaging application, has also been plotted in right y-axis of Figure 3-28(b) by considering a thermal noise in FET channel as N= $(4kTR_{ch})^{0.5}$ at T= 300 K (inset of Figure 3-28(b)). This thermal noise assumption is commonly used in FET-based plasmonic THz detectors as a white noise [11,24], since there is no drain current by the dc open drain configuration in the case of non-resonant mode plasmonic detection; while transit-mode detectors like SBDs consider the current-driven noises such as shot noise or $1/f$ noise [60]. Then, from dc I-V characteristic of Figure 3-18 for R_{ch}, the lowest NEP has been estimated as 15 pW/Hz$^{0.5}$ near V_{GS}= V_T.

As summarized in Table 3-1, the results of R_v and NEP obtained in this work show the most enhanced performance in comparison with those of previously reported CMOS-based plasmonic THz detectors by excluding amplification stages. Therefore, high-performance multipixel plasmonic THz detector based on asymmetric Si MOSFET can compete with other commercial THz detectors by taking advantages of low-cost and high-integration density CMOS technology for real-time THz imaging applications.

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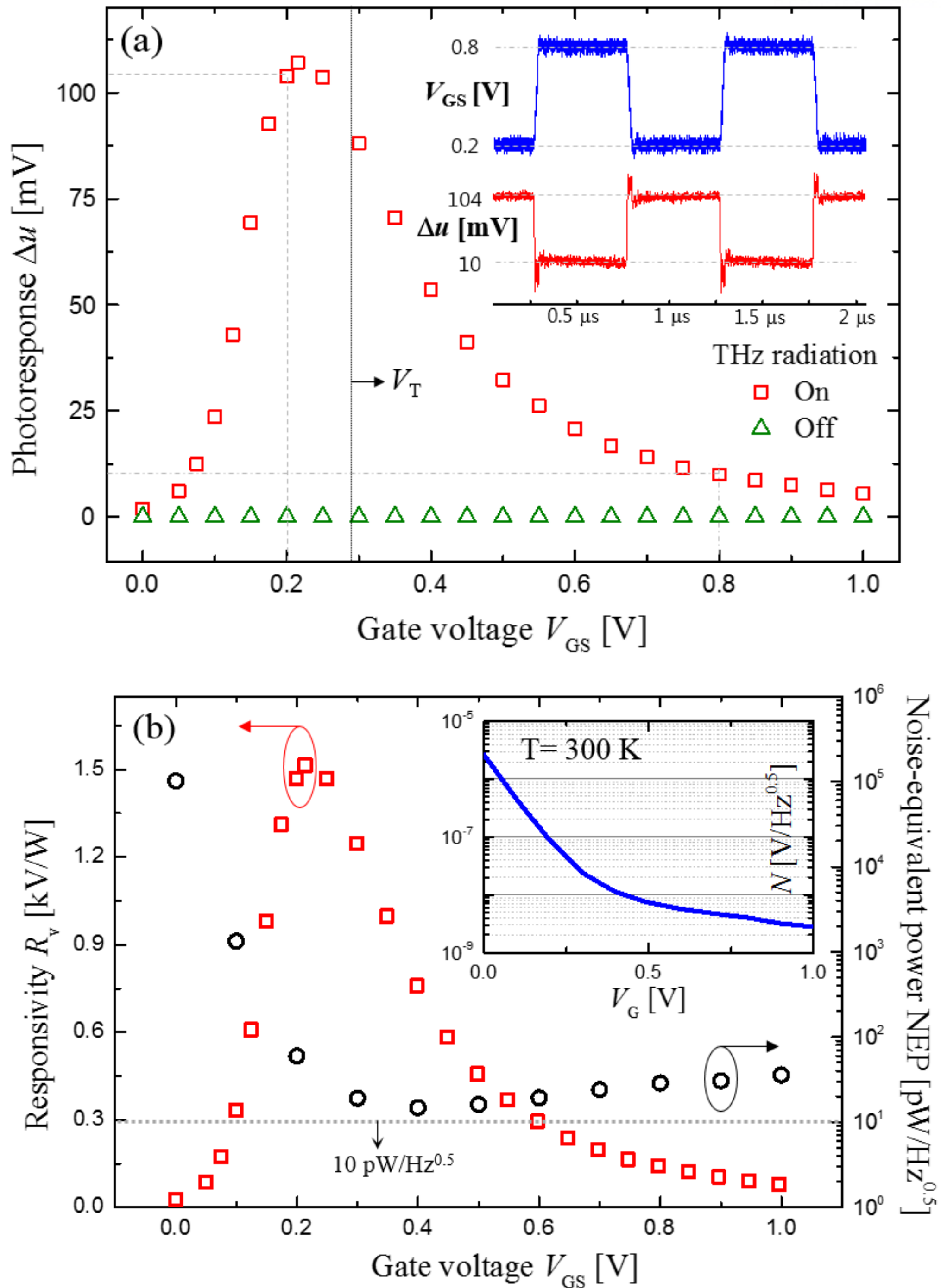

Figure 3-28. (a) Measured results of Δu as a function of V_{GS} of the patch antenna-coupled asymmetric MOSFET at 0.2 THz radiation. Inset shows the measured Δu as a function of time (t) according to V_{GS} modulation with f=1 MHz. (b) Responsivity (R_v) and noise-equivalent power (NEP) as a function of V_{GS}. Thermal noise N= $(4kTR_{ch}(V_G))^{0.5}$ has been estimated at T= 300 K (inset).

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Table 3-1. CMOS-based THz detector performances excluding amplifiers.

Tech.	f [THz]	R_v [V/W]	NEP [pW/Hz$^{0.5}$]	Ref.
300-nm	0.7	200	100	[6]
250-nm	0.645	566	300	[12]
65-nm	0.856	250	100	[13]
150-nm	0.595	350	20	[27]
2-μm	0.2	842	18	[19]
65-nm	0.2	1.5 k	15	This work

3.5 Demonstration of multi-pixel array detector

Figure 3-29 shows the photo images of main control board (MCB) with plasmonic 1x200 array detector for real-time THz imaging based on patch antenna-coupled asymmetric FET by using 65-nm CMOS technology. This array detector on MCB is implemented as line scanner under conveyor belt on real-time THz imaging system with a 0.2 THz gyrotron source and optical components of a high-density polyethylene cylindrical lens and OAP mirror for line beam profile, as shown in Figure 3-30. For a real-time detection of moving object on conveyor belt, high photoresponse (Δu) with small output delay of plasmonic detectors have been confirmed by showing a record-high peak value of Δu over 100 mV, which appears at sub-threshold region ($V_{GS} < V_T = 0.29$ V) according to the non-resonant plasmonic THz detection theory, by 65-nm CMOS asymmetric FET (Figure 3-31). The delay of Δu can be controlled by decreasing external gate capacitance $C_{g,ext}$ (Figure 3-26) . Based on calibrated dc I_{DS}-V_{GS} and I_{DS}-V_{DS} curves of the fabricated FET by TCAD simulation, new non-quasi static (NQS) compact model for plasmonic FET detector is developed by HSPICE. The transient simulation results from new model are well-matched with numerical TCAD as shown in Figure 3-13, which indicates that delay of FET itself (< 40 psec) in plasmonic detection is small enough to present real-time imaging.

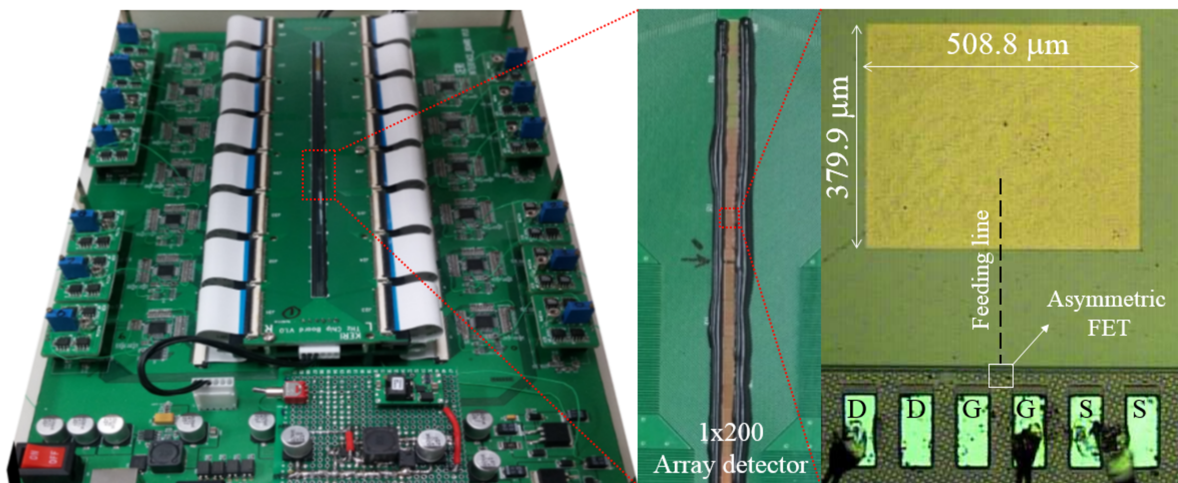

Figure 3-29. The photo images of main control board (MCB) with plasmonic 1x200 array detector based on antenna-coupled asymmetric FET.

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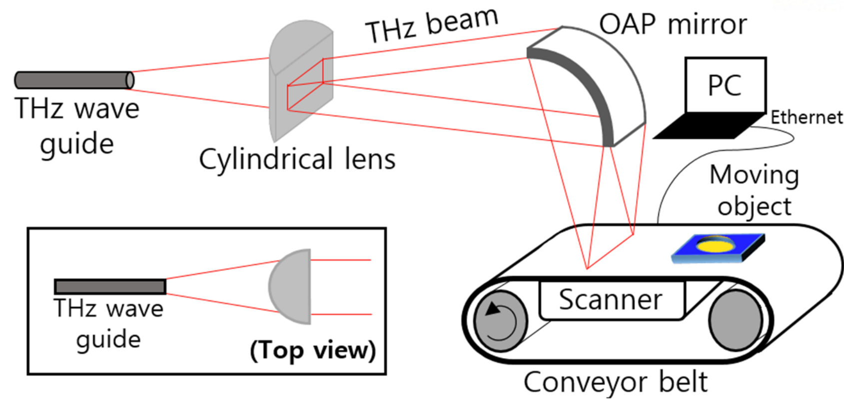

Figure 3-30. The experimental setup of a real-time THz imaging system with array scanner for moving object on conveyor belt.

Figure 3-31 shows the measured results of biased V_{GS} at peak Δu from duplicate two rows of 1x200 array (400 pixels) detector at 0.2 THz radiation, which confirms the yield and uniformity of 400 pixels with peak value of Δu results as shown in the inset. Furthermore, it can be easily controlled for real-time and large area detection by using THz imaging signal processing based on 13 x 32-channel multiplexer (MUX) 1 for biasing V_{GS} and 13 pairs of 32-channel multiplexer and amplifier for equalizing Δu in each pixel (Figure 3-32(a)). Detection results from THz radiation can be obtained through MUX 1 stage for V_{GS} biasing and MUX 2 stage, which have delay time of 10 µsec from the end of MUX 1 operation, for Δu amplifying as shown in timing diagram (Figure 3-32(b)). Therefore, detection is available in maximum 3.2 MHz (32 channels/10 µsec= $1/t_{pixel}$) because one cycle operation of 1x200 pixels can be achieved by simply 32 clock (=2^5, 5-bit).

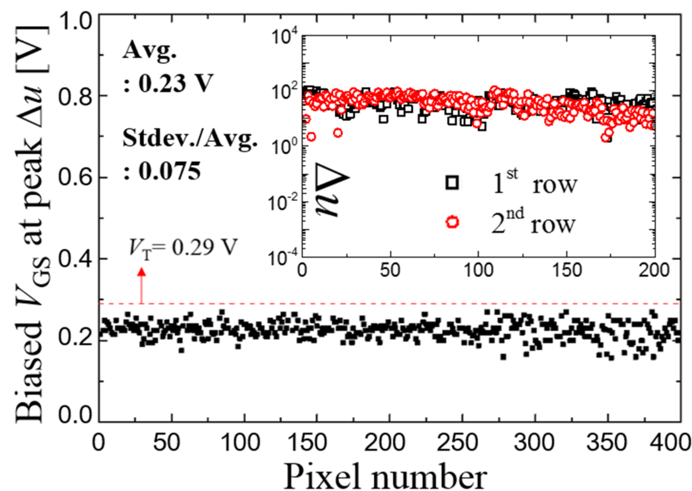

Figure 3-31. The measured results of biased V_{GS} at peak value of Δu from duplicate 1x200 array (400 pixels) detector during 0.2 THz radiation. (Avg. 0.23 V < V_T with Stdev./Avg= 0.075) Inset shows the peak value of Δu results of 400 pixels.

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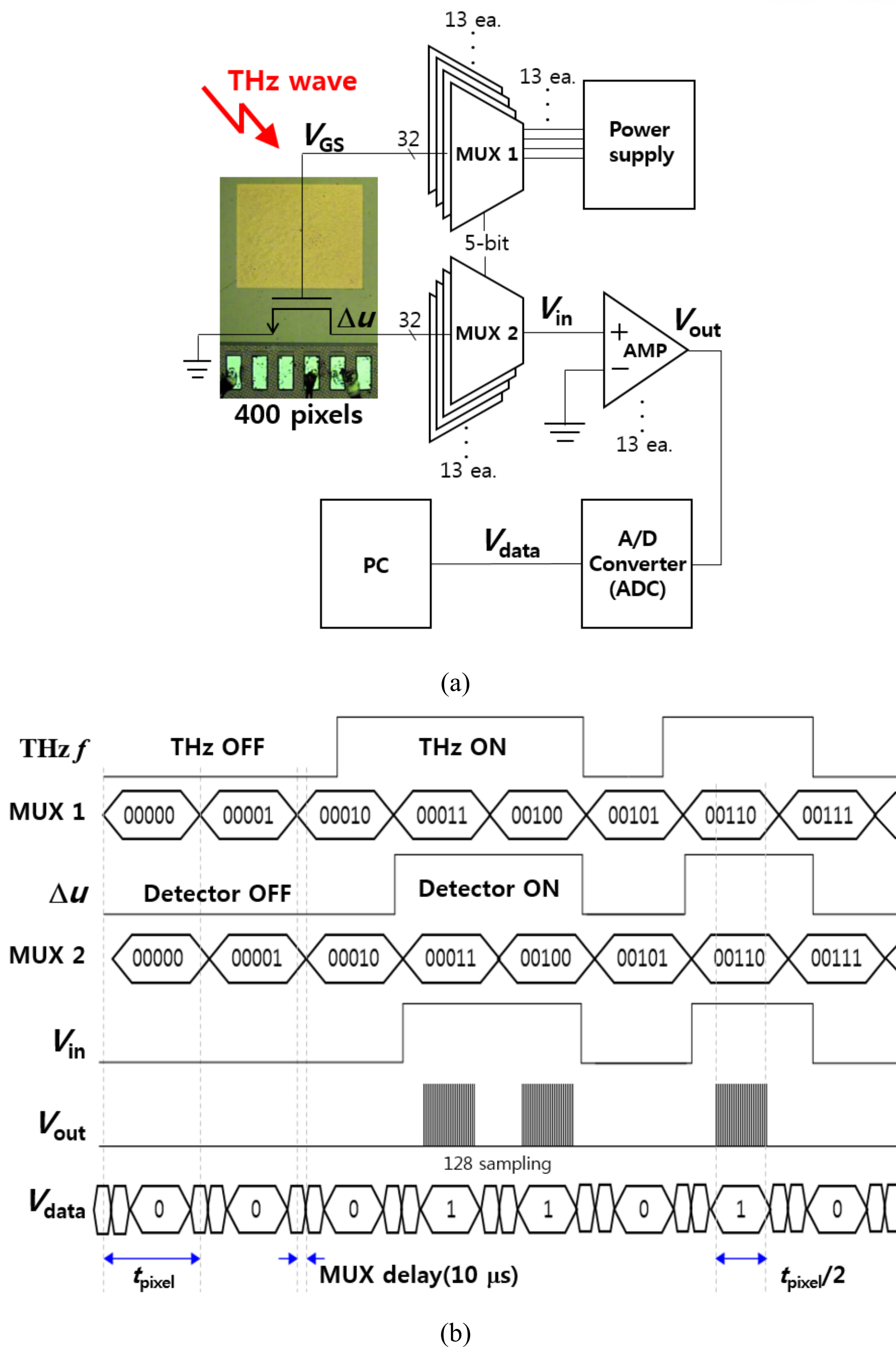

Figure 3-32. (a) The schematic circuit diagram of the 1x200 array scanner based on 13 x 32-channel MUX 1 for biasing V_{GS} and 13 pairs of 32-channel MUX 2 and amplifier for equalizing Δu in each pixel. (b) The timing diagram including MUX 1/MUX 2 stage according to output Δu by THz radiation ON/OFF. The average V_{out} can be obtained by 128-sampling for MUX channel modulation-induced noise reduction.

In addition, as shown in Figure 3-33, Δu was promptly changed from 104 mV to 10 mV by modulating V_{GS} from turn-on (V_{GS}= 0.2 V) to turn-off (V_{GS}= 0.8 V) with a 1 MHz modulation frequency. Therefore, the estimated detector delay (< 50 nsec) is also small enough to guarantee real-time video frame of 19.2 fps. From these results, Figure 3-34 shows that the 1x200 array scanner having 16 kHz with 62.5 μsec is demonstrated. When THz line beam is radiated, moving objects including human hand are being detected and displayed as real-time video signals on PC screen.

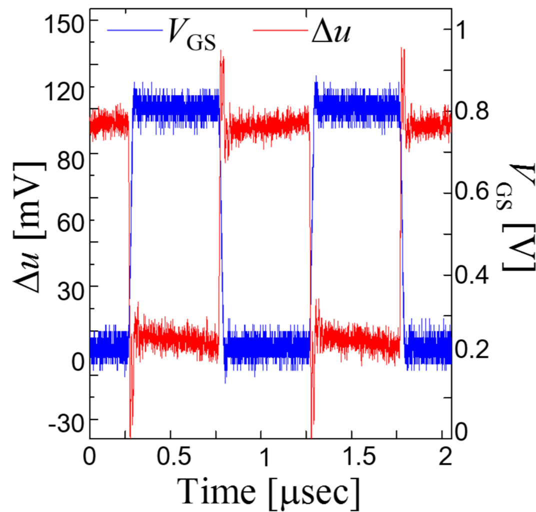

Figure 3-33. The promptly changed Δu from 104 mV to 10 mV by modulating V_{GS} from turn-on (V_{GS}= 0.2 V) to turn-off (V_{GS}= 0.8 V) with 1 MHz modulation frequency.

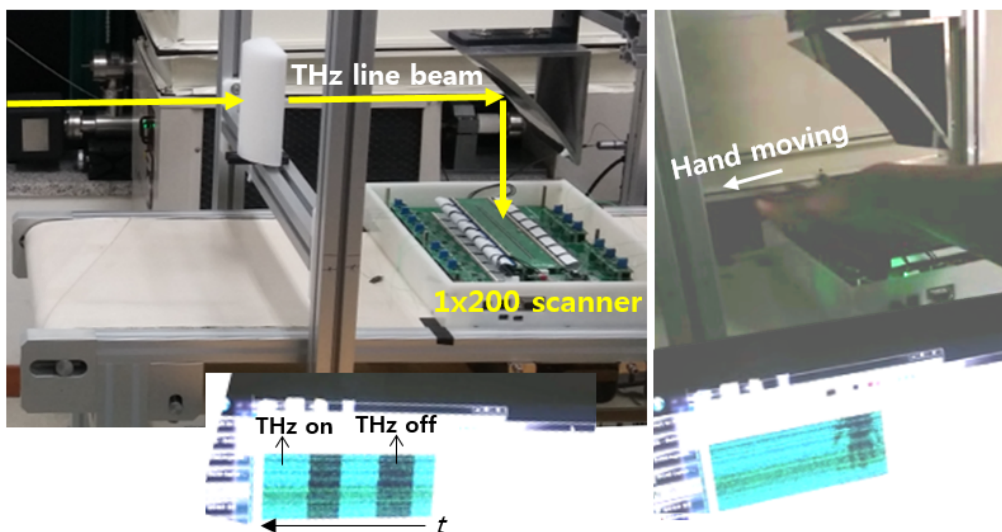

Figure 3-34. The successful working demonstration of a plasmonic 1x200 array scanner at f= 16 kHz with t_{pixel} = 62.5 μsec on real-time THz imaging system. Moving objects including human hand are being detected and displayed as real-time video signals on PC screen.

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3.6 Summary

High-performance plasmonic THz detector based on an asymmetric MOSFET with a vertically integrated antenna have been experimentally demonstrated at room temperature. The significant effects of asymmetric source and drain structure, channel shape on the charge asymmetry and performance enhancement have been analytically investigated based on non-resonant plasmonic THz detection theory. Through verification of the NQS compact model, the intrinsic MOSFET delay and total detector delay in THz plasmonic detection are successfully characterized and are small enough to guarantee a real-time operating detector. These results can provide the possibility of a real-time operating multipixel plasmonic THz detector through both R_v and NEP improvement while sustaining the total noise of the detector by only focusing on the elementary MOSFET design itself without additional considerations of amplifier integration. Since delay and uniformity have been guaranteed for real-time THz imaging, the real-time THz imaging of moving objects has been experimentally demonstrated based on plasmonic 1x200 array scanner by using the high/fast detecting performance asymmetric FET and multiplexer/amplifier circuits.

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Chapter IV
Monolithic transistor-antenna device

4.1 Introduction

Recently, plasmonic THz wave detectors based on Si MOSFETs have been attracting much attention in multi-pixel array detectors for real-time THz imaging [11-19]. For conventional sub-micron-scale Si MOSFETs to detect sub-millimeter-scale THz waves, all the reported plasmonic detectors inevitably have been integrated with large-size antennas considering quarter- or half-wavelength of sub-THz range (75~150 μm). In the connection between transistor and antenna, however, the input impedance mismatching and the feeding line loss are the most important issues in high-performance plasmonic THz detectors [46].

For sub-micron Si MOSFETs to detect sub-millimeter THz waves, FETs are generally integrated with antennas considering THz wavelength. At this point, careful MOSFET device design considering its input impedance and matching of the antenna is one of the most important issues in high-performance plasmonic THz detectors based on antenna integrated MOSFET. Although a high input impedance of FET is preferable for high responsivity in quasi-static RF analysis [12], it is difficult to realize antenna with ideal power matching because of high impedance [44]. Moreover, the width of the feeding line should become smaller for higher impedance, which results in performance variation by narrow margin of process tolerance. Thus, low-impedance FET can be a promising candidate for wideband multi-pixel detector with uniformly enhanced responsivity by characterizing its impedance exactly pursuing real-time large-area THz imaging. In spite of its significance, the systematic experimental investigations of Si MOSFET impedance in THz regime have not been reported yet.

In this chapter, monolithic transistor-antenna device by designing the ring-type asymmetric transistor itself as a circular antenna is propose for high-performance plasmonic THz detector. More enhanced charge asymmetry in a ring-type asymmetric transistor is analyzed in comparison with a bar-type one. Thus, record-highly enhanced detecting performance of the monolithic transistor-antenna is experimentally demonstrated by impedance matching without feeding line radiation loss.

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4.2 Preliminary results

Figure 4-1 (a) and (b) show top-view micrograph images of FET detectors integrated with monolithic patch antenna having the antenna characteristic impedance (Z_a) of 50 and 100 Ω, respectively. As shown in Figure 4-1, a width of feeding line is determined from the characteristic impedance (Z_0) and all the other dimensions are designed for detecting 0.2 THz signals by using three-dimensional (3D) electromagnetic simulation. For plasmonic THz detection of FET, antenna feeding lines are connected between gate (signal) and source (ground) of MOSFET and thus, FET gate-to-source input impedance (complex Z_{gs}) should be matched with Z_a=Z_0 (real) for smaller reflection and higher photoresponse (Δu) of drain (output) dc voltage. In terms of the matching between complex Z_{gs} and real Z_a=Z_0 with the feeding (transmission) lines, the equivalent transmission line model with the multiple reflection coefficient (Γ_m) should be considered and the matching condition given by

$$\left|Z_{gs}\right| = Z_0 \qquad for \quad \Gamma_m = 0 \tag{4-1}$$

only with $|Z_{gs}|$ (magnitude of complex Z_{gs}) can be derived from the equivalent quarter-wave transformer circuit analysis [61]. Therefore, higher Δu by smaller Γ_m means that $|Z_{gs}|$ become more close to Z_a=Z_0 from Eq. (4-1). For low-Z_{gs} Si MOSFET, the large micron-dimensions are simply applied to the asymmetric source (W_S= 2 μm) and drain width (W_D =10W_S) based on non-self- aligned gate-last process with gate length of L= 2 μm. The details of the asymmetric Si MOSFET fabrication can be found in our previous work [45].

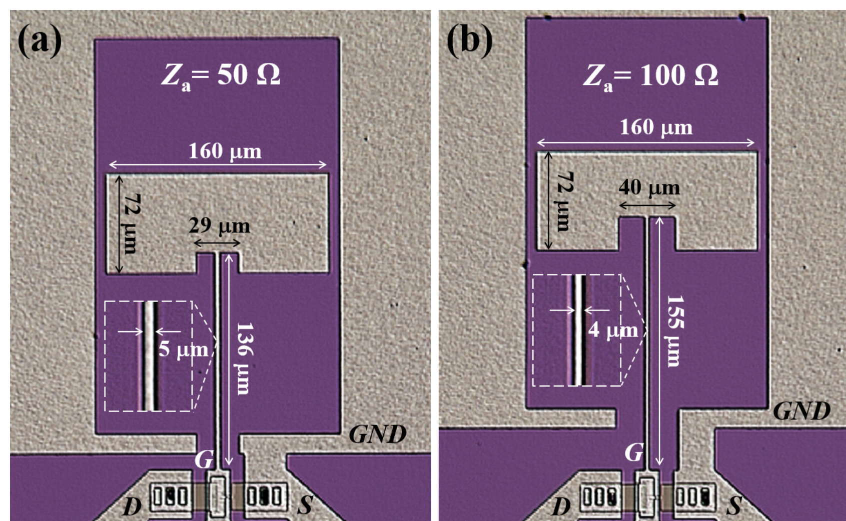

Figure 4-1. Micrograph images (top-view) of the fabricated Si MOSFET-based plasmonic THz detector with integrated patch antennas: (a) Z_a= 50 Ω and (b) Z_a= 100 Ω.

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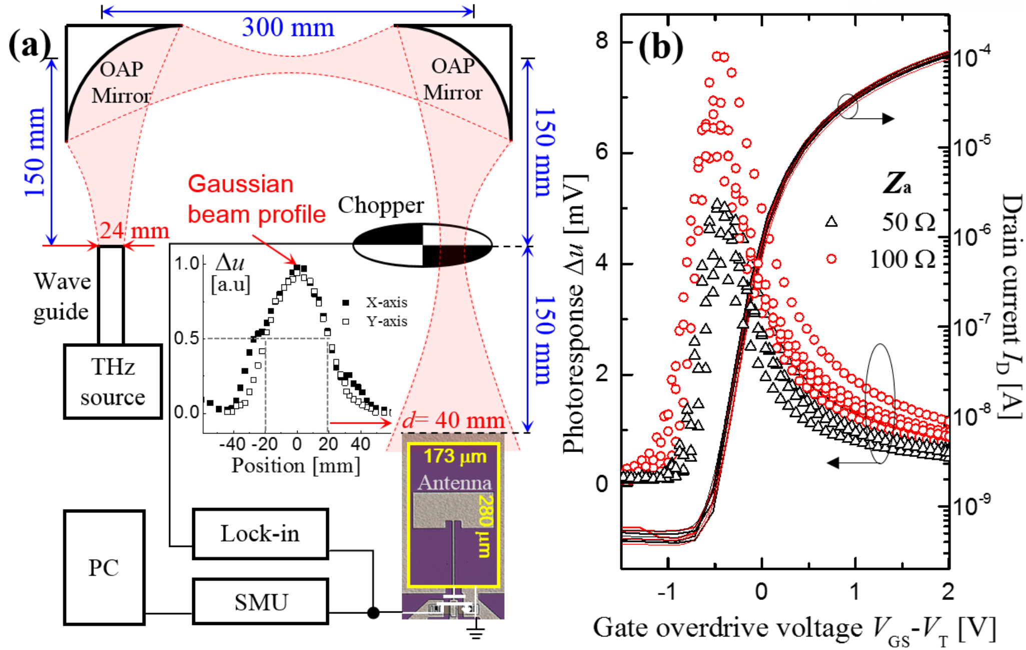

Figure 4-2. (a) Experimental setup for plasmonic THz detector using 0.2-THz gyrotron with Gaussian beam profile (inset). (b) Measurement results of uniform dc characteristic curves from the same MOSFETs (10 samples) at V_D= 50 mV and the Δu as a function of the $V_{GS} - V_T$ for different antennas with Z_a= 50 Ω and 100 Ω (5 samples for each group).

Figure 4-2(a) shows our experimental setup of THz detection for Δu measurement of the fabricated detector. Diverging Gaussian beam with 0.2-THz radiation was generated by a gyrotron source in higher-order mode resonator, which enables a large-area real-time detection with the CW method since it is stable in sub-THz frequency regime [58,59]. After the focused THz beam is passing through chopper hole by OAP mirrors, diverging THz beam with a full-width at half-maximum (FWHM) of 40 mm (inset) with attenuated source power (P_s~ 1 W) is absorbed by antenna, which transferred it to FET gate as an ac signal. Finally, dc Δu is measured by SMU (Agilent B2912A) through the background noise reduction using lock-in amplifier (SR830) by bandpass filtering around the chopper modulation frequency. Considering actual detector area (A_d= 173 x 280 μm^2, cf. beam area A_{beam}= π(20)^2 mm^2), the actual power (P_a= P_s x A_d /A_{beam}) on the antenna-integrated detector can be estimated as 0.038 mW.

Table 4-1. Device parameters of low-Z_{gs} Si MOSFET samples with L=W_S=W_D/10.

MOSFET	t_{ox} (nm)	Junction depth (nm)	Expected Z_{gs} (Ω)
Sample *A*	50	250	< 1 k (low)
Sample *B*	50	750	< 100 (lower)
Sample *C*	10	300	< 100 (lower)

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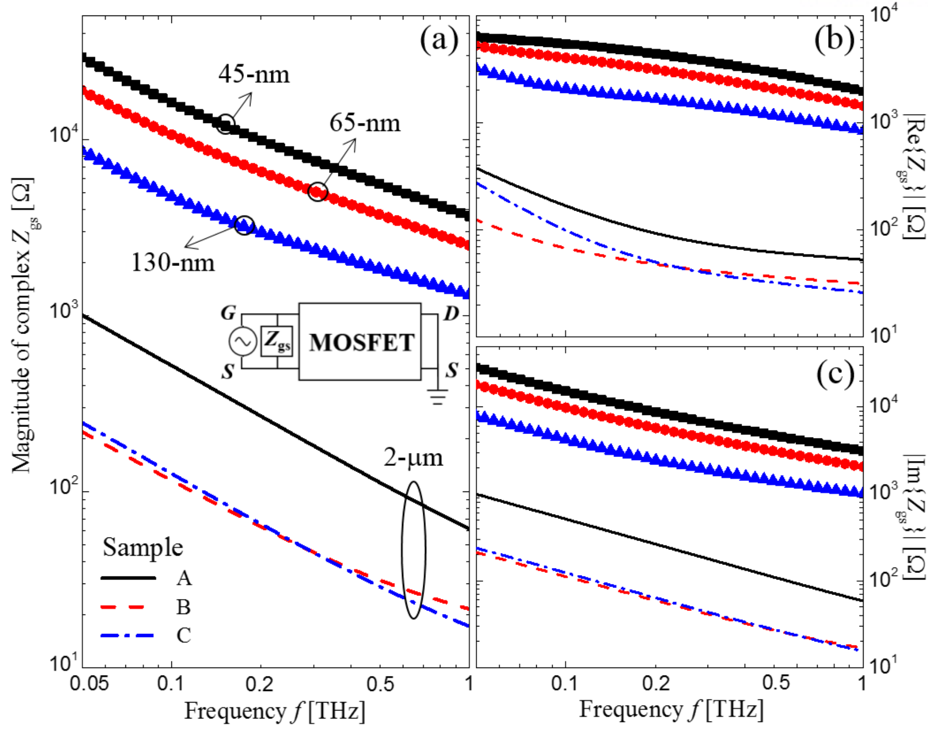

Figure 4-3. TCAD simulation results of Z_{gs} by two-port network analysis in the frequency range from 50 GHz to 1 THz for our low-impedance FETs and conventional nanoscale FETs. For each simulation, gate overdrive voltage of V_{GS}-V_T is -0.1 V. (a) Magnitude, (b) Real and (c) Imaginary part of Z_{gs}.

The measured Δu results of our low-Z_{gs} MOSFET are plotted in Figure 4-2(b). According to a non-resonant plasmonic detection theory [25], the peak points of Δu are observed in subthreshold region before the zero gate overdrive voltage (V_{GS}-V_T= 0 V). Interestingly, based on the same MOSFETs with uniform dc I-V curves from 10 samples, the distinguished group of the peak Δu values (i.e. detecting performance) are clearly observed by two different Z_a values. It should be noted that Δu enhancement according to the increase of Z_a from 50 Ω to 100 Ω provide an experimental evidence of the fabricated Si MOSFET input impedance of Z_{gs} > 50 Ω close to 100 Ω in 0.2-THz frequency.

For more systematic experiments on MOSFET impedance, different samples of low-Z_{gs} Si MOSFET are also taken as summarized in Table I. Based on the same layout dimensions with the reference sample *A*, which is presented in Figure 4-2(b), lower-Z_{gs} MOSFETs can be expected by increasing capacitance with junction broadening from 250 nm to 750 nm junction depth in sample *B* and thinner t_{ox} in sample *C*. These expected trends toward lower Z_{gs} in our Si MOSFET samples are confirmed by TCAD device simulation using two-port network analysis as shown in Figure 4-3. The estimated Z_{gs} (magnitude of complex impedance) of our low-impedance MOSFETs is below 1 kΩ around 0.2 THz, while the conventional nanoscale MOSFETs with smaller device dimensions (L= W= 45, 65, 130 nm, t_{ox}= 2.2 ~

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3.2 nm [62]) show high Z_{gs} above 1 kΩ, which is reasonable range when compared with low-Z_{gs} level in the multi-fingered (finger number $NF > 10$) RF MOSFETs [63] and single-fingered 130-nm MOSFETs with larger widths [64].

These estimated impedance ranges of our MOSFET samples (Z_{gs} < 1 kΩ) have been experimentally demonstrated in Figure 4-4, which present the extracted peak Δu results from the respective detector sample group (5 samples) combined with each Z_a split of 50 and 100 Ω. As observed in Figure 4-2(b), MOSFET sample *A* with the estimated Z_{gs} < l kΩ shows the higher Δu at Z_a= 100 Ω than those at Z_a= 50 Ω here confirmed by multiple uniform samples while sample *B* group with lower-expected Z_{gs} < 100 Ω shows the lower Δu at Z_a= 100 Ω than sample *A* and more enhanced Δu at Z_a= 50 Ω. Since there is no difference of t_{ox} and the plasmonic channel electron density modulation between sample *A* and *B*, it can be concluded that this result is the experimental evidence of the FET input impedance range in that Z_{gs} of sample *B* < 50 Ω while Z_{gs} of sample *A* > 50 Ω.

Sample *C* group shows more highly enhanced Δu with best R_v= 32 mV/0.038 mW= 842 V/W at Z_a= 50 Ω (325 times) than those of sample *B* (75 times) from the result of the detector without antenna as shown in inset from Ref. [45], even if sample *B* and *C* have same criterion of Z_{gs} < 50 Ω as expected in Figure 4-3. The lowest noise-equivalent-power (NEP) in sample C (inset) has been obtained as 18 pW/√Hz at V_{GS}-V_T= 0.25 V commonly based on the channel thermal noise (N= $(4kTR_{ch})^{0.5}$), which is comparable with the reported lowest NEP values for antenna-coupled plasmonic Si-based THz detectors [13], owing to the relatively low channel resistance (R_{ch}) from large micron-scale width for low-impedance MOSFET design. It can be noted that these enhancement trends of R_v and NEP in sample *C* with thinner t_{ox} mainly originate from increase of the plasmonic channel electron density modulation by t_{ox} scaling. Therefore, MOSFET for plasmonic THz detectors should be designed by considering both external impedance and internal plasmonics of the non-quasi-static channel electron density modulation.

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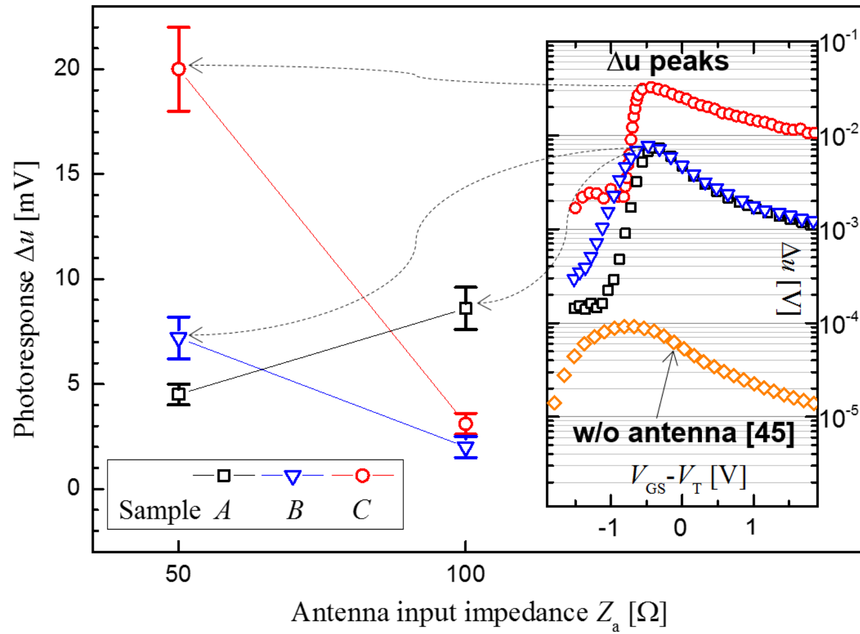

Figure 4-4. Extracted Δ*u* peaks from each detector sample group combined with Z_a splits of 50 Ω and 100 Ω. Inset shows Δ*u* as a function of V_{GS}-V_T for each sample with maximum Δ*u* peaks compared with detector without antenna [45]. Symbols and error bars show the average and standard deviation from 15 samples of each detector group, respectively.

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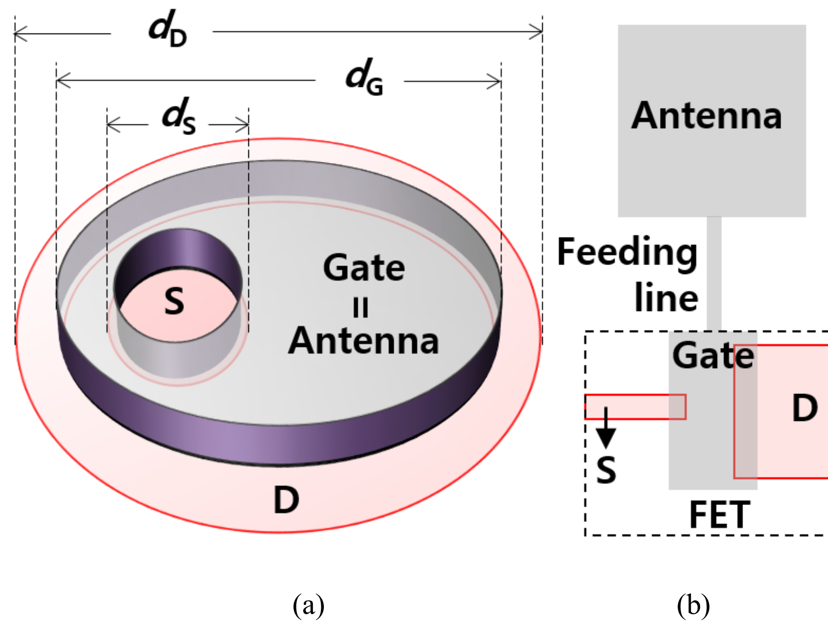
4.3 Device structure

Figure 4-5(a) shows the conceptual schematic of the proposed monolithic circular transistor-antenna structure. As compared with a conventional approach (Figure 4-5(b)), monolithic transistor-antenna itself can absorb the incoming THz wave and transfer power directly to the ring-type asymmetric channel without feeding line. Plasmonic THz detectors based on Si MOSFETs, which operate in non-resonant mode due to its relatively low mobility, can detect ac THz wave power by dc drain voltage (Δu) from a plasmonic 2-dimensional electron gas (2DEG) asymmetry with a propagation distance (l_{2DEG}) in the subthreshold conduction channel [48]. Therefore, the key design parameter in transistor level is the asymmetry ratio (η_a), which has been defined as source-to-drain width ratio (W_D/W_S) in conventional bar-type structure [46] and then, in the proposed ring-type asymmetric channel, the same source-to-drain top edge distance (l) should be used (Figure 4-6).



(a) (b)

Figure 4-5. (a) The conceptual schematic of the proposed monolithic circular transistor-antenna structure based on ring-type asymmetric channel with gate (d_G), drain (d_D), and source diameter (d_S) (b) Conventional bar-type FET integrated with antenna through feeding line as THz detector.

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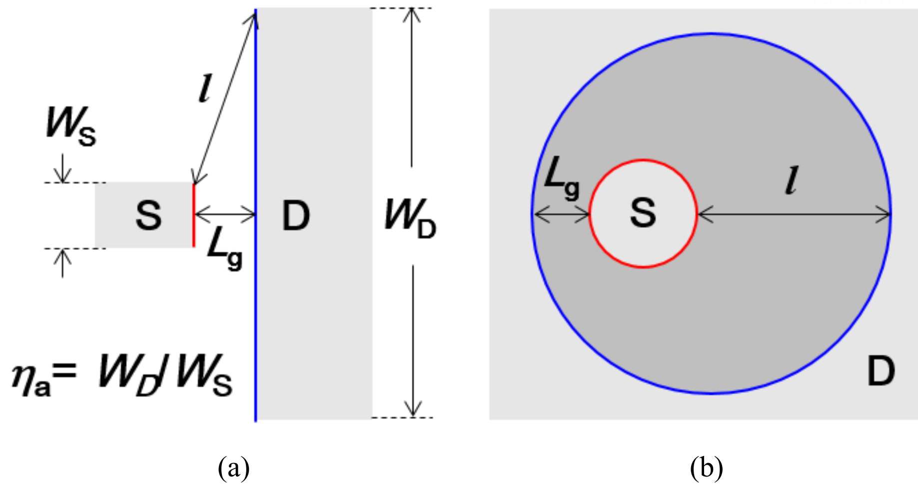

(a) (b)

Figure 4-6. (a) Bar-type structure. (b) Ring-type structure having η_a by keeping l in the asymmetric channel.

The effect of channel shape on the channel 2DEG density and its asymmetry has been investigated in comparison with a previous conventional bar-type structure [46]. By using 3-D TCAD device simulation framework, the bar-type and ring-type with source diameter (d_s) of 4 μm, and 1 μm on the same l= 9.2 μm are modeled as illustrated with contour plot of channel electron density showing the same l_{2DEG} in Figure 4-7(a), (b), and (c), respectively. These results indicate that the ring-type channel with the smaller d_s (Figure 4-7(c)) has more enhanced electron density near the source side than that of the bar-type structure (Figure 4-7(a)). It can be confirmed that this is due to a more confined channel around the source side by presenting the intermediate range of the channel 2DEG density profile in case of the source curvature close to bar-type structure (Figure 4-7(b)).

As shown in Figure 4-8, asymmetric electron density oscillations which has been obtained under the same I_{DS} (inset), confirms that the observed charge asymmetry only results from channel shape difference. By extracting the gradient of channel 2DEG density (N_{2DEG}), the increased charge asymmetry in the ring-type channel is clearly observed (Figure 4-9(a), which leads to the enhanced Δu as dc offset voltage in the ac output voltage of $v_{DS}(t)$ (Figure 4-9(b)).

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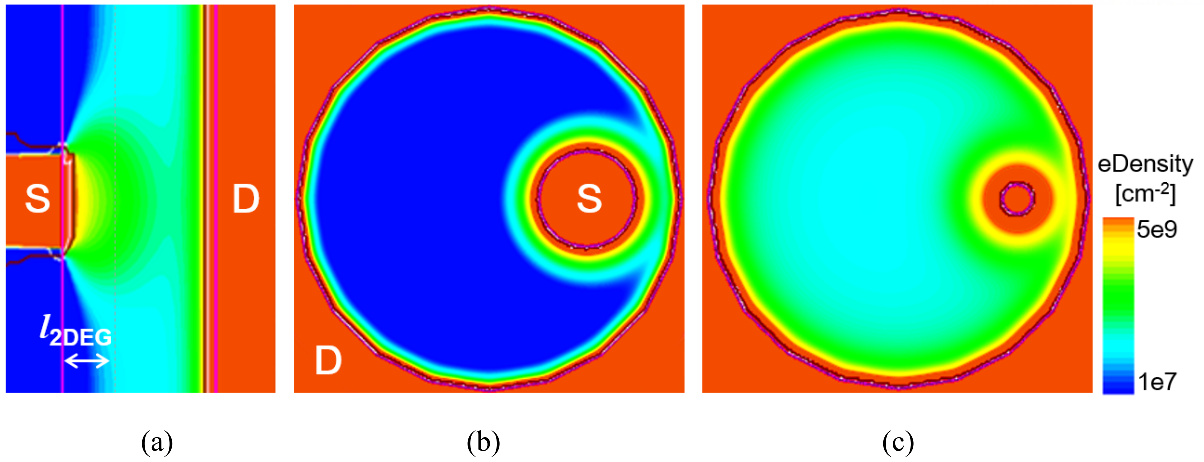

Figure 4-7. (a) the bar-type with η_a= 10 and (b) ring-type with source diameter (d_s) of 4 μm, and (c) 1 μm on the same l= 9.2 μm (η_a= 10) as illustrated with contour plot of channel electron density showing the same l_{2DEG} by using 3-D TCAD device simulation framework under THz wave radiation at 0.1 THz (ac signal).

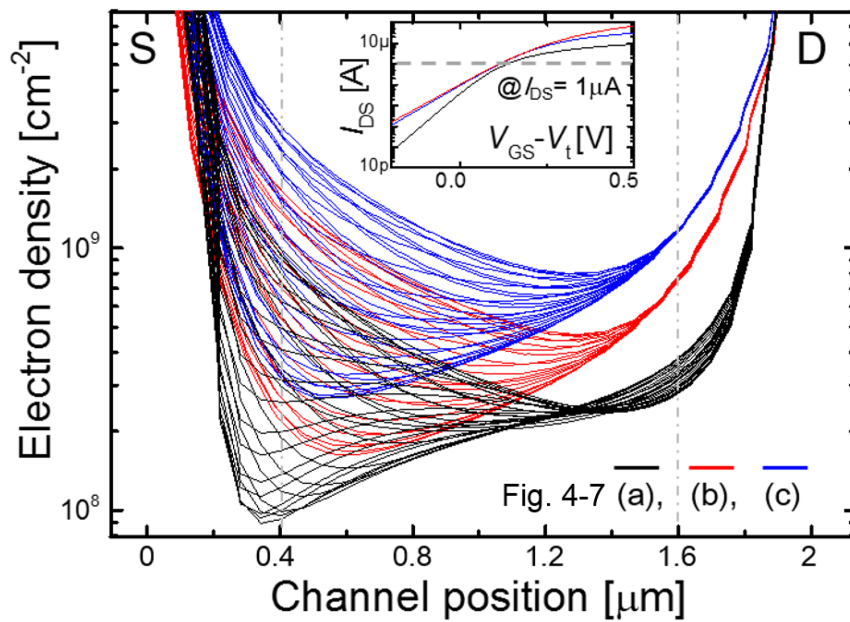

Figure 4-8. Electron density modulation as a function of channel position and time under a superimposed time-varying gate bias ($v_{GS}(t)$= V_{GS} +$v_i$sinwt) with dc and ac signal (v_i= 50 mV) as THz wave from 3-D device simulation at same I_{DS}.

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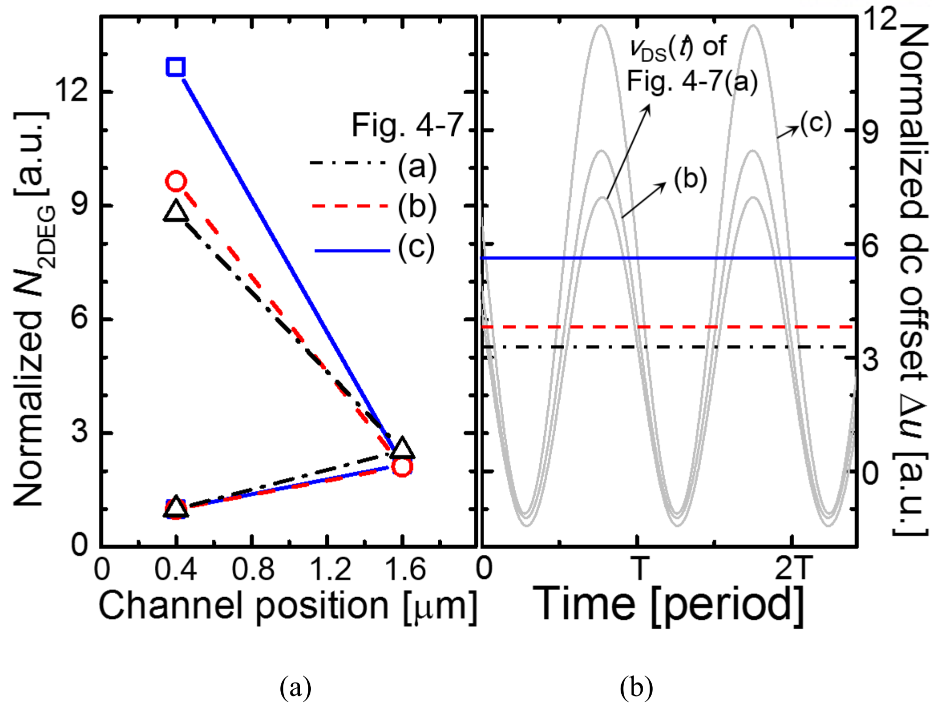
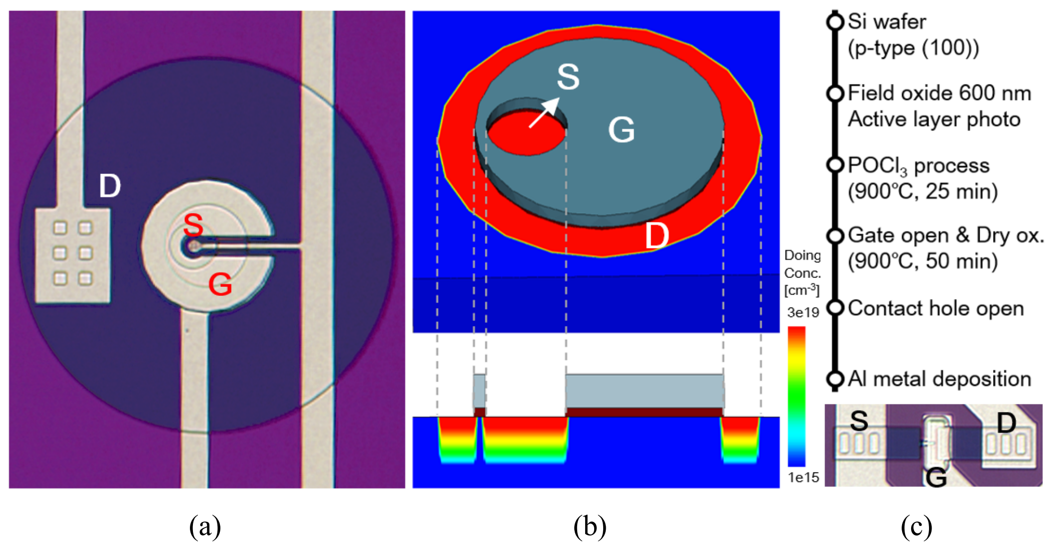


(a) (b)

Figure 4-9. (a) Normalized maximum and minimum N_{2DEG} by each minimum in Figure 4-8 at x= 0.4 μm (highly modulated) and x= 1.6 μm (almost invariable). (b) Simulation results of output $v_{DS}(t)$ with the normalized dc offset Δu by the lowest value in the case of Figure 4-7(a).

4.4 Device fabrication

Figure 4-10(a) and (b) show the top-view micrograph image of the fabricated asymmetric ring-type transistor-antenna device and schematics of 3-D device simulation, respectively. Monolithic transistor-antenna device is fabricated based on the conventional non-self-aligned metal-gate Si MOSFET fabrication process as same with bar-type structure in Chapter 3.3. At the first lithography step in FET, however, circular-shape asymmetric source/drain active region can be formed and the mask gate length (L_g) can be defined as the nearest distance between source and drain region. After the formation of *n*-type source and drain region with $POCl_3$ diffusion process, the gate open layer defines the gate-to-source/drain overlap region and 50-nm-thick thermal oxide was grown for the t_{ox}. After opening the contact holes at the source and drain regions, aluminum as metal layer was deposited by dc sputter and finally sintered. As shown in Figure 4-11, the successful transfer I_{DS}–V_{GS} curves of both ring-type (monolithic transistor-antenna) and bar-type (conventional) asymmetric transistors have been obtained with a well-matched 3-D device simulation results.



(a) (b) (c)

Figure 4-10. (a) The top-view micrograph image of the fabricated asymmetric ring-type transistor-antenna device based on conventional non-self-aligned metal-gate Si MOSFET fabrication process. (b) Schematics of 3-D device simulation. (c) conventional non-self-aligned metal-gate Si MOSFET fabrication process as same with bar-type structure.

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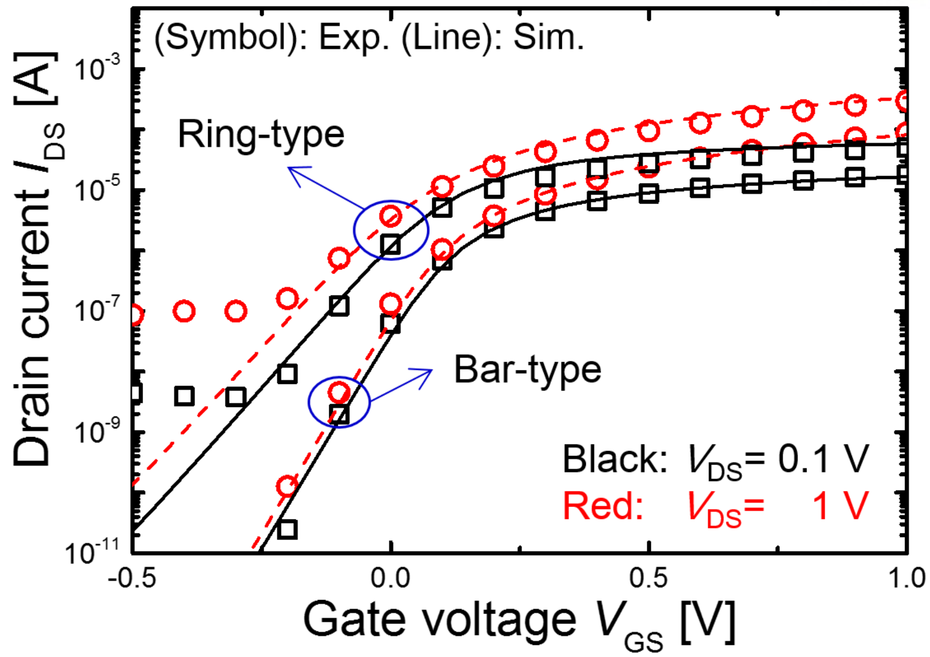

Figure 4-11. DC transfer I_{DS}-V_{GS} curves of both fabricated and simulated ring-type and bar-type asymmetric transistors with L_g= 2 μm and t_{ox} = 50 nm.

4.5 Device characteristics

4.5.1 Impedance matching

Figure 4-12(a) shows the measurement setup for reflection ($|S_{11}|$) and transmission coefficient ($|S_{21}|$) measurement of the fabricated monolithic transistor-antenna array (Figure 4-12(b)) by using quasi-optical system. Radiation at f= 0.12 THz was generated by vector network analyzer (VNA) with a Gaussian horn antenna and off-axis ellipsoidal (OAE) mirror is used to focus THz wave on the sample (Figure 4-12(c)).

In order to estimate the resonant frequency (fr) of monolithic transistor-antenna, the model equations have been derived through the following two-step process. In the first step, the monolithic transistor-antenna array system is considered as a 2-D periodic array of circular metal patch (silicon substrate thickness t_{Si}= 0) since the gate oxide and the contact oxide thickness are much smaller than the wavelength (λ_0) at 0.12 THz, so the drain, gate, and source acts as a single circular metal patch. The incident THz wave easily penetrate, as their thicknesses are thinner than λ_0. The system of a 2-D periodic array of circular metal patch can be described by the periodic conductivity profile [65] (Figure 4-13(a)). From Maxwell's equations, the wave field in 2-D periodic array of patch can be described as,

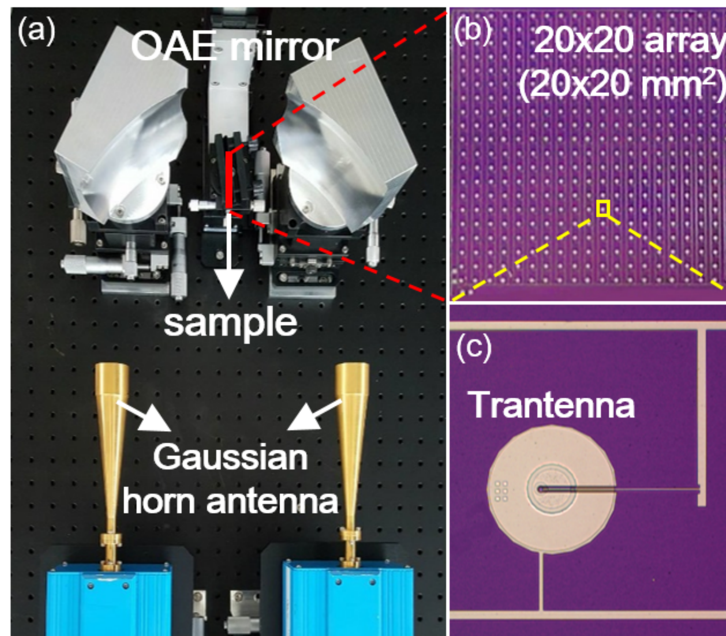

Figure 4-12. (a) The measurement setup for obtaining s-parameter of designed monolithic transistor-antenna by using quasi-optical system with Gaussian beam radius of 8 mm. (b) Sample of 20x20 array and (c) monolithic transistor-antenna device.

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$$\psi(x_{\perp},k_z,\omega)\iint\psi(x_{\perp},z,t)e^{i(k_z z-\omega t)}dzdt \tag{4-2}$$

where $x_{\perp} = x\hat{e}_x + y\hat{e}_y$. Assuming that frequency (ω) and longitudinal wave number (k_z) are fixed, so that the Helmholtz equation for $\psi(x_{\perp})$ follows the Maxwell's equations.

$$\nabla^2{}_{\perp}\psi(x_{\perp}) = (k_z{}^2 - \omega^2/c^2)\psi(x_{\perp}) \tag{4-3}$$

Equation (4-3) with boundary conditions given in [66] on the surface of the conducting posts for TM mode defines the eigenvalue problem of finding $\gamma^2 = \omega^2/c^2 - k_z^2$ as a function of $k_{\perp}$. The three special points in Figure 4-13(b), Γ, X, and M, correspond respectively to $k_{\perp} = 0$, $(\pi/a)\hat{e}_x$, and $(\pi/a)(\hat{e}_x+\hat{e}_y)$, where a is lattice constant. In-house Matlab code is developed for above mentioned equations to compute the eigenmodes for RF and high frequency range.

The second step is to model the dependency of f_r (from code) on t_{Si}. A unit cell simulation setup is used to analyze the parametric simulation results of monolithic transistor-antenna (Figure 4-14) and found that, the dominant factors for f_r are $d_D/2a$ and t_{Si} (Figure 4-15). The t_{Si} of monolithic transistor-antenna is thicker (~λ_0/7.15) than conventional patch antenna substrates, hence f_r varies inversely with respect to t_{Si}. The data values arrived from the parametric study of t_{Si} is used in Matlab's curve fitting tool, to get the following relation:

$$k_z \propto \pi\sqrt{\varepsilon_r}/t_{Si}, f_r \propto 1/t_{Si} \tag{4-4}$$

Finally, Eq. (4-4) is used in Eq. (4-3) to model the final parameter values of monolithic transistor-antenna device. The measured transmission and absorptance profiles are matched to simulation result as shown Figure 4-16. The -6 dB impedance bandwidth of detector is about 40 GHz. Furthermore, high THz power absorption is obtained with about 50 % of total THz power at 0.12 THz.

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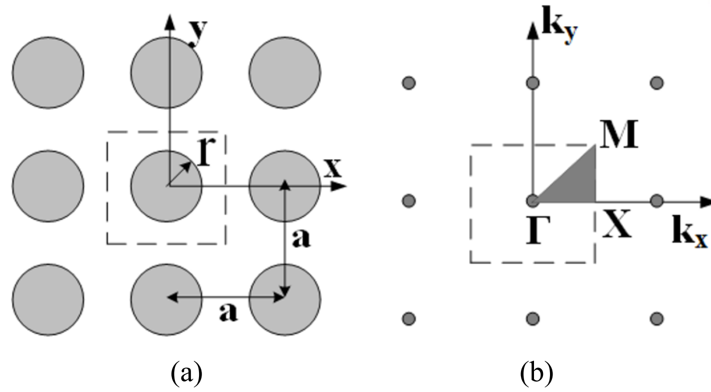

Figure 4-13. (a) Scheme of 2-D periodic array of metal circle patch with *a*. (b) Reciprocal lattice and Brillouin zones for square lattice.

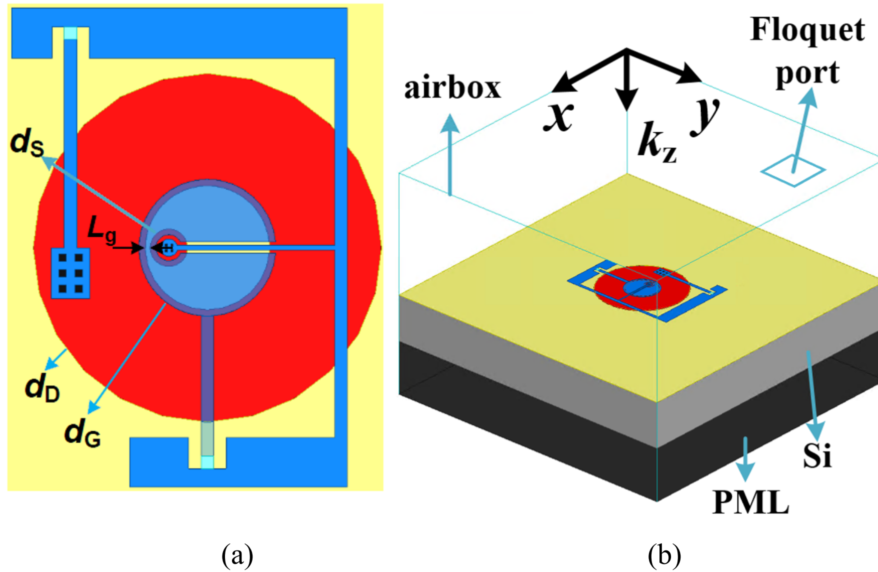

Figure 4-14. (a) Top view of ring-type FET-based monolithic transistor-antenna detector with d_S= 30 μm, d_G= 110 μm, d_D= 280 μm, and a= 1000 μm. (b) Unit cell simulation setup with in HFSS: periodic boundary conditions are applied for all lateral faces-Floquet port is set at top, perfectly matched layer (PML) is set at bottom.

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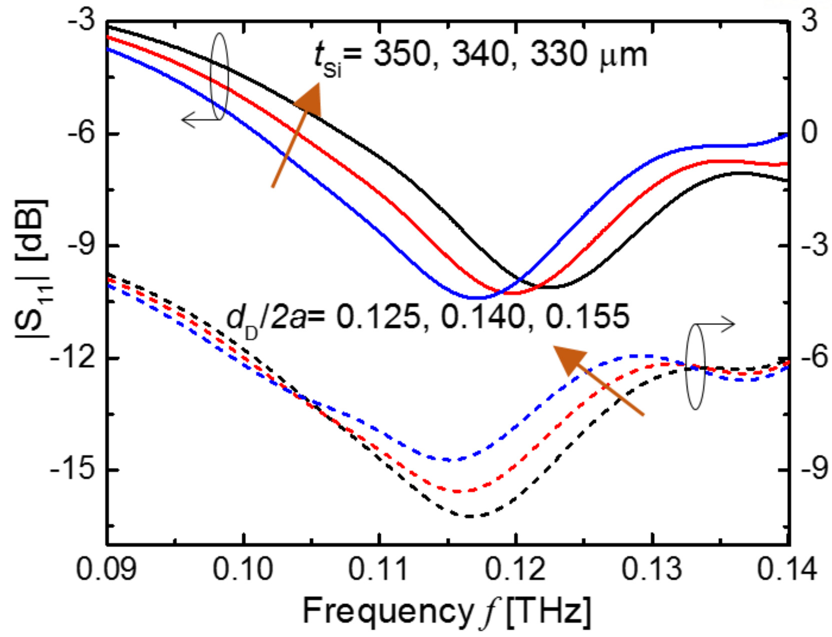

Figure 4-15. The parametric variation of simulated reflection coefficient with respect to $d_D/2a$ and t_{Si} to identify the dominant factors for resonance frequency of monolithic transistor-antenna detector.

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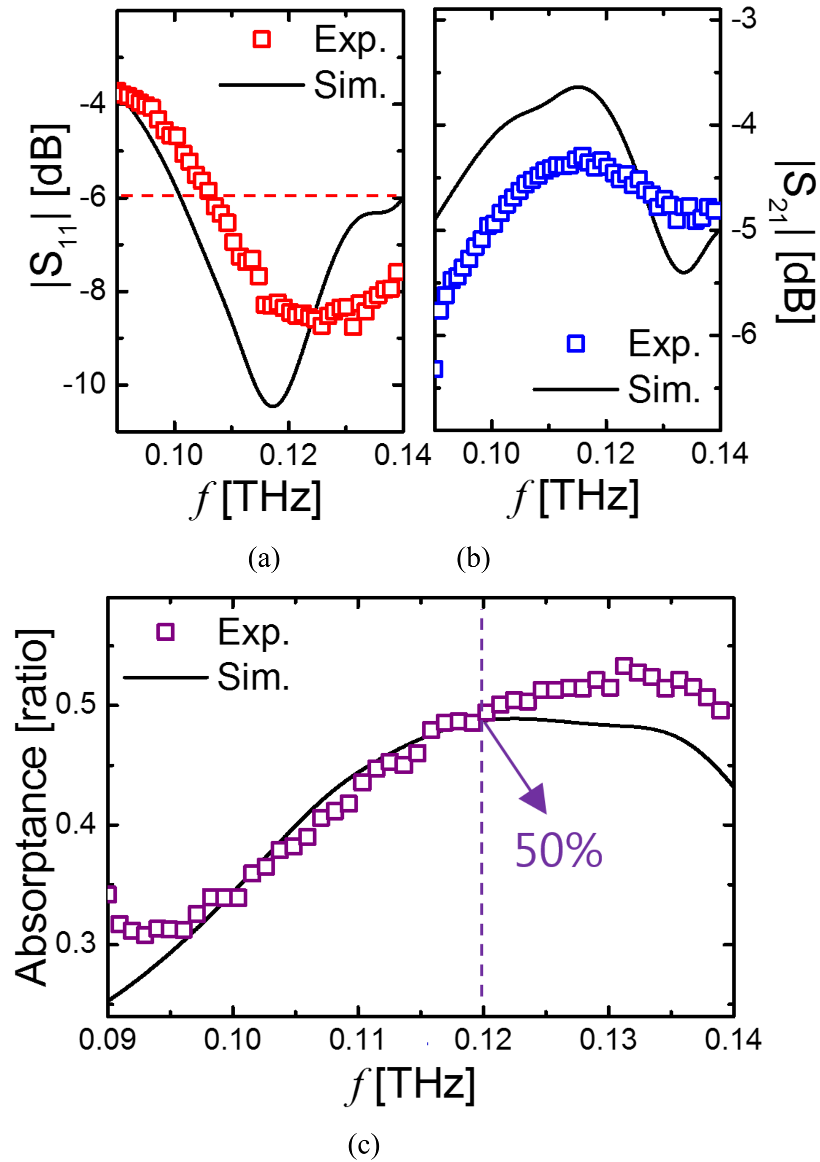

Figure 4-16. The measurement and simulation results of (a) Reflection coefficient |S11|, (b) transmission coefficient |S21|, and (c) absorptance $\{= 1-|S_{11}|^2-|S_{21}|^2\}$ for F-band (90 to 140 GHz).

4.5.2 Free-space and on-chip characteristics

The channel curvature effect by d_s control on the same l and η_a, Δu can be basically enhanced by increasing l and η_a by d_D control in ring-type structure. This design controllability is confirmed by on-chip measurement data as shown in Figure 4-17. Therefore, it should be noted that enhanced charge asymmetry in ring channel is responsible for performance enhancement of plasmonic detector.

Figure 4-18 shows the measurement setup for THz detection at 0.12 THz. DC gate bias was applied through the source meter. The output signal at the drain of monolithic transistor-antenna detector is delivered into a lock-in amplifier with a 10-MW load, which provide a 10-Hz trigger signal (f_{ref}) to modulate the THz signal. Measurement results of the monolithic transistor-antenna device and detector with feeding line are demonstrated in Figure 4-19 by following the full measurement protocol for determining responsivity (R_v) and noise-equivalent power (NEP). The Δu= 32 μV is highly enhanced from 5 μV of the detector (bar-type) with feeding line sample on the same η_a= 10 (Figure 4-19(b)). After the estimation of THz actual power (P_a) and cold-FET thermal noise (Figure 4-19(c)) by following standard procedure [46,52], the enhanced R_v > 1 kV/W (x 5) and reduced NEP < 10 pW/Hz$^{0.5}$ (x 1/10) are demonstrated. This record-high enhancement is due to antenna mismatching and feeding line loss reduction as well as the enhanced charge asymmetry in the proposed monolithic transistor-antenna device.

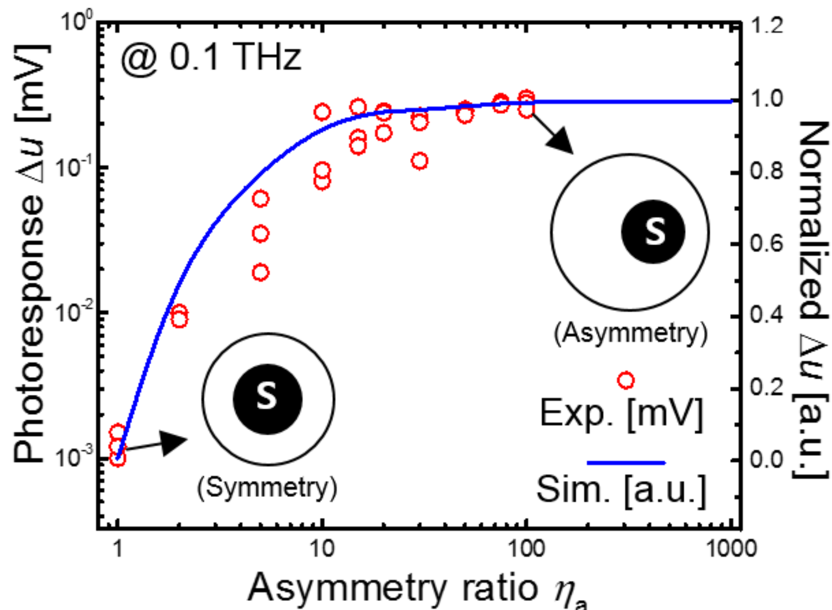

Figure 4-17. Measurement and normalized simulation results of photoresponse Δu as a function of asymmetry ratio η_a.

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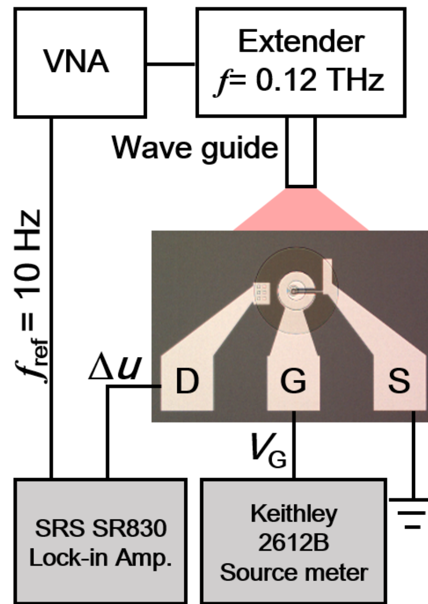

Figure 4-18. The measurement setup for plasmonic THz monolithic transistor-antenna detector at 0.12 THz system with synchronized reference frequency f_{ref}= 10 Hz.

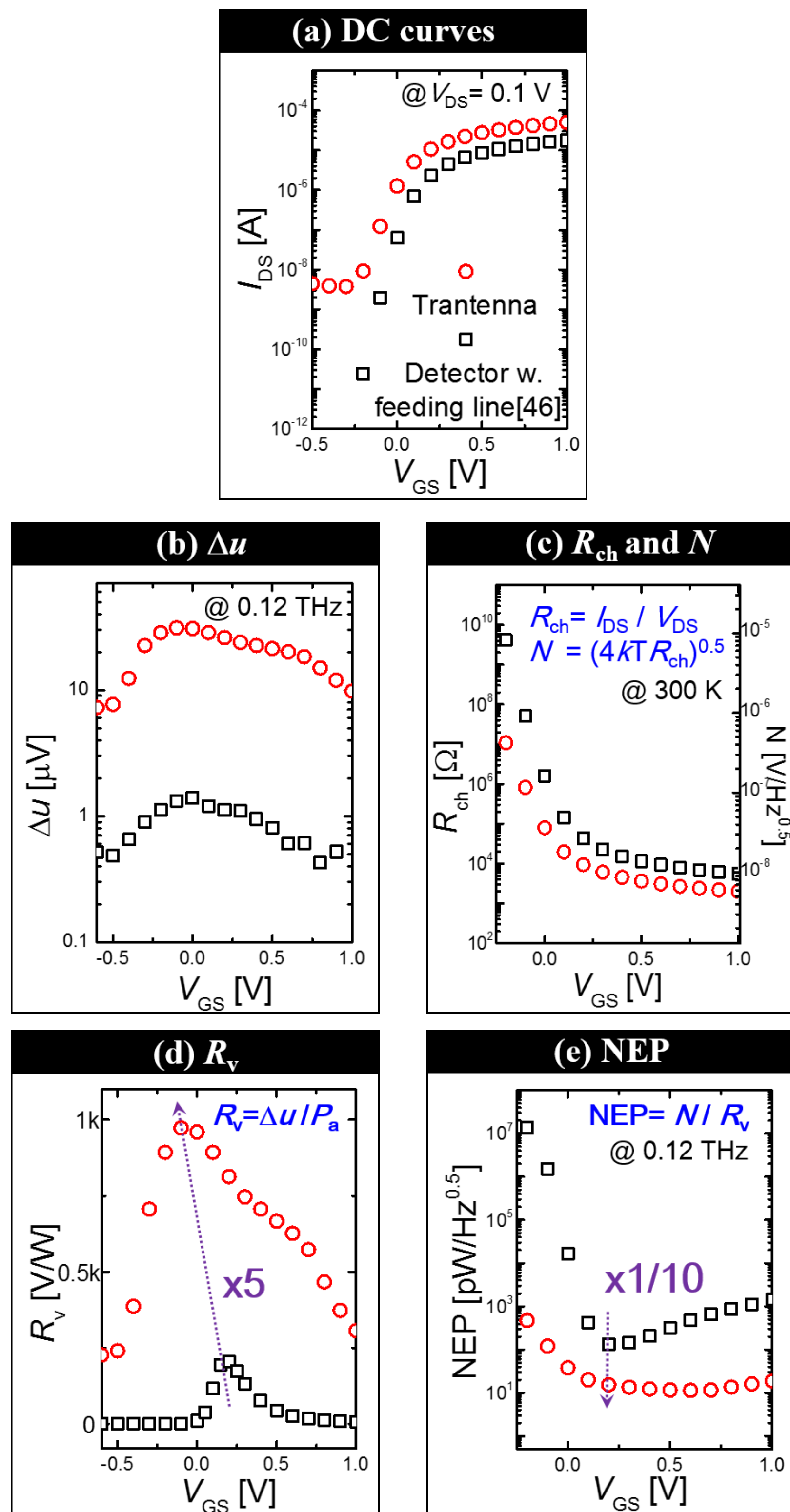

Figure 4-19. Full protocol for determining responsivity and NEP according to the monolithic transistor-antenna device and bar-type detector with feeding line [46]. (a) DC curves, (b) photoresponse Δu, (c) channel resistance R_{ch} and noise spectral density N, (d) responsivity R_v by P_a(ring-type detector)= 33 nW and P_a (bar-type detector)= 25 nW, (e) noise equivalent power NEP.

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4.6 Summary

A high-performance plasmonic THz detector have been experimentally demonstrated by a circular-shape monolithic transistor-antenna device. Asymmetry ratio and impedance matching of non-resonant mode THz detector integrated with antenna is significant factor for output signal increase. Hence, the enhanced plasmonic channel charge asymmetry by ring-type FET and antenna efficiency without feeding line loss have been analyzed. The record-high performance of the compact monolithic transistor-antenna pixel can provide the possibility of a mega-pixel-level plasmonic THz detector for large-scale real-time THz imaging system.

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4.7 Remaining work to be done

The multi-pixel THz detector based on high performance detection such as R_v and NEP should be demonstrated in real-time THz imaging system. However, many researches in THz detector have been reported with the level of under the kilo-volt per watt and upper the 10-pico-watt per square root hertz of R_v and NEP, respectively. In order to achievement of the performance-breakthrough as shown in Figure 4-20, firstly, by using a ring-type structure FET, maximized η_a and field-enhanced FET, which is designed to drain surrounding source, should be investigated. Since Δu have been saturated at upper the η_a of about 20 in previous works, precise approach in terms of device physics for enhanced asymmetric 2DEG in the channel. Secondly, high-efficient absorptance when THz wave is incoming should be achieved with the level of upper the 80%. By multi-pixel detector based on optimized monolithic transistor-antenna structure design according to the THz frequency, large-area detection can be observed in low THz wave source power. Thus, for real-time THz imaging system, mega-pixel scale THz imaging detector will be demonstrated with high-performance and high-resolution.

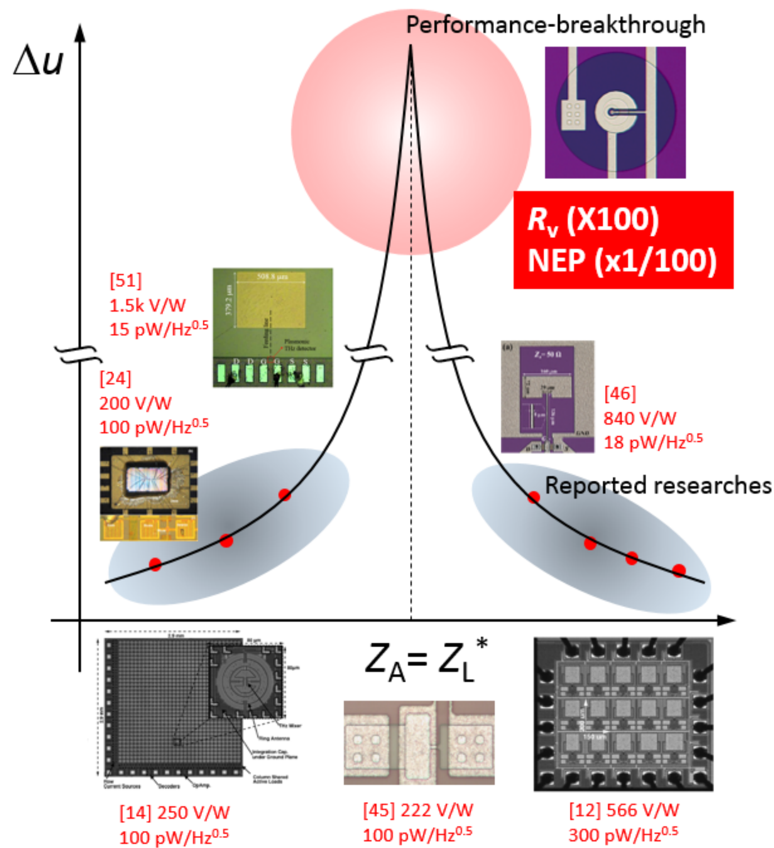

Figure 4-20. The roadmap of performance breakthrough research achievement based on monolithic transistor-antenna THz detector by impedance matching.

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Chapter V

Conclusion

In real-time THz imaging system, it is essential to demonstrate high-resolution, high-speed, and compactness of the measurements apparatus. These requirements for THz imaging system can be satisfied by Si CMOS technology which has high density integration, fast response time of pico-second scale, and concise circuitry by on-wafer fabrication. In this thesis, hence, the performance enhancement in plasmonic THz detectors have been investigated, and record-high results are established for competitive performances; the operation of plasmonic THz detector of THz response based upon existing theory have been discussed. Furthermore, we have demonstrated that novel methodology based on quasi-plasma 2DEG and advanced non-quasi-static compact model can provide an efficient simulation framework for the structural design and detection response characteristics, respectively. From these methodology, THz detector have been simulated based on Si FET. This simulation is closely related to our metal gate FET which is currently being fabricated at UCRF in UNIST because our metal gate FET has been made by using asymmetry characteristic between source and drain. Thus, the simulation results of performance metrics of the Si-MOSFET broadband detector are comparable to the experimental results of THz detectors. From the experiment demonstration, the plasmonic THz detector based on antenna-coupled asymmetric can enhance the responsivity and reduce NEP at room temperature. These results can provide the possibility of the performance enhancement focusing on the asymmetric design of source and drain structure under the gate in field-effect devices without additional considerations of amplifier integration.

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