Doctoral Dissertation

Process-induced Structural Variability-aware Performance Optimization for Advanced Nanoscale Technologies

Myunghwan Ryu

Department of Electrical and Computer Engineering

(Electrical Engineering)

Graduate School of UNIST

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submitted to the Graduate School of UNIST
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Myunghwan Ryu

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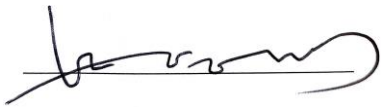

Advisor
Prof. Franklin Bien

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Myunghwan Ryu

This certifies that the dissertation of Myunghwan Ryu is approved.

6. 28. 2016

signature

Advisor: Prof. Franklin Bien

signature

Committee Member: Prof. Youngmin Kim

signature

Committee Member: Prof. Kyung Rok Kim

signature

Committee Member: Prof. Seokhyeong Kang

signature

Committee Member: Prof. Jongwon Lee

ABSTRACT

As the CMOS technologies reach the nanometer regime through aggressive scaling, integrated circuits (ICs) encounter scaling impediments such as short channel effects (SCE) caused by reduced ability of gate control on the channel and line-edge roughness (LER) caused by limits of the photolithography technologies, leading to serious device parameter fluctuations and makes the circuit analysis difficult. In order to overcome scaling issues, multi-gate structures are introduced from the planar MOSFET to increase the gate controllability.

The goal of this dissertation is to analyze structural variations induced by manufacturing process in advanced nanoscale devices and to optimize its impacts in terms of the circuit performances. If the structural variability occurs, aside from the endeavor to reduce the variability, the impact must be taken into account at the design level. Current compact model does not have device structural variation model and cannot capture the impact on the performance/power of the circuit. In this research, the impacts of structural variation in advanced nanoscale technology on the circuit level parameters are evaluated and utilized to find the optimal device shape and structure through technology computer-aided-design (TCAD) simulations. The detail description of this dissertation is as follows:

Structural variation for nanoscale CMOS devices is investigated to extend the analysis approach to multi-gate devices. Simple and accurate modeling that analyzes non-rectilinear gate (NRG) CMOS transistors with a simplified trapezoidal approximation method is proposed. The electrical characteristics of the NRG gate, caused by LER, are approximated by a trapezoidal shape. The approximation is acquired by the length of the longest slice, the length of the smallest slice, and the weighting factor, instead of taking the summation of all the slices into account. The accuracy can even be improved by adopting the width-location-dependent factor (W_{eff}). The positive effect of diffusion rounding at the transistor source side of CMOS is then discussed. The proposed simple layout method provides boosting the driving strength of logic gates and also saving the leakage power with a minimal area overhead. The method provides up to 13% speed up and also saves up to 10% leakage current in an inverter simulation by exploiting the diffusion rounding phenomena in the transistors.

The performance impacts of the trapezoidal fin shape of a double-gate FinFET are then discussed. The impacts are analyzed with TCAD simulations and optimal trapezoidal angle range is proposed. Several performance metrics are evaluated to investigate the impact of the trapezoidal fin shape on the circuit operation. The simulations show that the driving capability improves, and the gate capacitance increases as the bottom fin width of the trapezoidal fin increases. The fan-out 4 (FO4) inverter and ring-oscillator (RO) delay results indicate that careful optimization of the trapezoidal angle can increase the speed of

the circuit because the ratios of the current and capacitance have different impacts depending on the trapezoidal angle.

Last but not least, the electrical characteristics of a double-gate-all-around (DGAA) transistor with an asymmetric channel width using device simulations are also investigated in this work. The DGAA FET, a kind of nanotube field-effect transistor (NTFET), can solve the problem of loss of gate controllability of the channel and provide improved short-channel behavior. Simulation results reveal that, according to the carrier types, the location of the asymmetry has a different effect on the electrical properties of the devices. Thus, this work proposes the *n*/*p* DGAA FET structure with an asymmetric channel width to form the optimal inverter. Various electrical metrics are analyzed to investigate the benefits of the optimal inverter structure over the conventional GAA inverter structure. In the optimum structure, 27% propagation delay and 15% leakage power improvement can be achieved.

Analysis and optimization for device-level variability are critical in integrated circuit designs of advanced technology nodes. Thus, the proposed methods in this dissertation will be helpful for understanding the relationship between device variability and circuit performance. The research for advanced nanoscale technologies through intensive TCAD simulations, such as FinFET and GAA, suggests the optimal device shape and structure. The results provide a possible solution to design high performance and low power circuits with minimal design overhead.

Keywords: multi-gate transistors, nanoscale, optimization, process-induced structural variability, gate-all-around (GAA) transistors, double gate-all-around (DGAA) transistor, FinFET, technology computer-aided-design (TCAD), optimal layout, variability-aware, asymmetric channel width

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The material in this dissertation is based on the following publications.

• Chapter 3 is based on:

- M. Ryu and Y. Kim, “Trapezoidal approximation for on-current modeling of 45-nm non-rectilinear gate shape”, *IEICE Electronics Express*, Vol. 10, No. 11, May 2013.

- M. Ryu, H. V. Nguyen, and Y. Kim, “Diffusion-rounded CMOS for Improving Both Ion and Ioff Characteristics”, *IEICE Electronics Express*, Vol. 8, No. 21, pp. 1783-1788, Nov. 2011.

• Chapter 4 is based on:

- M. Ryu and Y. Kim, “Impacts of Trapezoidal Fin of 20-nm Double-Gate FinFET on the Electrical Characteristics of Circuits”, *Journal of Semiconductor Technology and Science (JSTS)*, Vol. 15, No. 4, Aug. 2015.

• Chapter 5 is based on:

- M. Ryu, F. Bien, and Y. Kim, “Optimal Inverter Logic Gate using 10-nm Double Gate-All-Around (DGAA) Transistor with Asymmetric Channel Width”, *AIP advances*, Vol. 6, No. 1, 015311, 2016.

- J. Lee, M. Ryu and Y. Kim, “On-chip interconnect boosting technique by using of 10-nm double gate-

all-around (DGAA) transistor", *IEICE Electronics Express*, Vol. 12, No. 12, Jun. 2015.

My coauthors (Donghu Kim, Jaemin Lee, H. V. Nguyen, Yesung Kang, and Prof. Youngmin Kim, listed in alphabetical order) have all kindly approved the inclusion of the aforementioned publications in my dissertation.

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NOMENCLATURE

BSIM	Berkeley Short-channel IGFET Model
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DGAA	Double gate-all-around
DIBL	Drain induced barrier lowering
EGL	Equivalent gate length
FinFET	Fin field-effect transistor
FO	Fan-out
GAA	Gate all around
IC	Integrated circuits
ITRS	International Technology Roadmap for Semiconductors
JL	Junctionless
JLFET	Junctionless field-effect transistor
LEE	Line-end extension
LER	Line edge roughness
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	*n*-type metal oxide semiconductor
NRG	Non-rectilinear gate
NTFET	Nanotube field-effect-transistor
OPC	Optical proximity correction
PDK	Process design kit
PLA	Post-lithography analysis

PLS	Post-lithographic simulation
PMOS	*p*-type metal oxide semiconductor
PR	Photoresist
PTM	Predictive technology model
RET	Resolution enhancement technology
RF	Radio frequency
RO	Ring oscillator
SCE	Short channel effects
SG INV	Sandwiched-gate inverter
SG	Sandwiched-gate
SNW	Silicon nanowire
SOI	Silicon-on-insulator
SPICE	Simulation program with integrated circuit emphasis
SRAM	Static random access memory
SS	Subthreshold swing
STI	Shallow trench isolation
TCAD	Technology computer-aided design
VLSI	Very-large-scale integration
WF	Workfunction
WPE	Well proximity effect

Chapter 1. Introduction

1.1 Device scaling and its challenges

1.1.1 Scaling theory

As semiconductor industries move to aggressive scaling to reduce the area and dynamic power consumption, the channel length has become as short as a few nanometers [17]. The most apparent motivation behind the rapid scaling down of CMOS technology is the increase of integration density. The cost of production per device can be reduced by packing more devices in a given area. Another significant motivation is the enhancement of the circuit performance. The propagation delay t_p of the inverter can be determined as

$$t_p = \frac{2L^2}{\mu_n V_{DD}} \tag{1.1}$$

where t_p, μ_n, V_{DD}, and L refer to the propagation delay, electron mobility, supply voltage, and the channel length, respectively. As can be seen above equation, smaller channel length is essential to the reduction of the propagation delay. As another motivation, through scaling down of the device dimension, the power consumption per device can be reduced. The dynamic power dissipation of an inverter is

$$P = fCV_{DD}^2 \tag{1.2}$$

where P, f, C, V_{DD} refer to the dynamic power dissipation, operating frequency, the capacitance, and supply voltage, respectively. The power supply voltage (V_{DD}) plays an important role in the dynamic power dissipation since reducing V_{DD} has a quadratic effect on dynamic power dissipation. However, in (1.1), if we reduce V_{DD}, the propagation delay would increase. Thus, in order to keep the performance and lower dynamic power dissipation, one must reduce the channel length L_g along with the reduction in V_{DD}. By scaling down the channel length, one can reduce supply voltage without degrading performance. Like this, until a recent date, transistor scaling traditionally followed simple rules [15] with slight modification Table 1-1 [16, 18]. In constant-field scaling [15], it was proposed that one can keep short-channel effect under control by scaling the device voltages and the device dimensions (both vertical and horizontal) by the same factor, κ, so that the electric field remains unchanged. Based on the assumption of maintaining constant electric field inside the transistor, Dennard's scaling theory

Table 1-1. Guidelines for MOSFET scaling [2] (adapted from [15, 16]). Constant electric-field (*E*-field) scaling was followed for MOSFET miniaturization to $L_g \sim 0.13$ μm. Due to the non-scalability of transistor threshold voltage (V_{th}) and *pn*-junction built-in potential, generalized scaling has been followed for deep sub-micron CMOS technologies.

Device and circuit parameters	Constant E-field scaling: Multiplicative factors	Generalized scaling: Multiplicative factors
Device dimensions (L_g, T_{ox}, X_j, W)	$1/\kappa$	$1/\kappa$
Body doping concentration (N_B)	κ	$\alpha\kappa$
Supply voltage (V_{DD})	$1/\kappa$	α/κ
Electric field (E)	1	α
Transistor current (I)	$1/\kappa$	α/κ
Area (A)	$1/\kappa^2$	$1/\kappa^2$
Capacitance ($C = \varepsilon_{ox} A / T_{ox}$)	$1/\kappa$	$1/\kappa$
Intrinsic delay ($\tau \sim CV_{DD} / I$)	$1/\kappa$	$1/\kappa$
Power dissipation ($P \sim IV_{DD}$)	$1/\kappa^2$	α^2/κ^2
Power density (P/A)	1	α^2

Table 1-2. Minimum feature size scaling from 22 nm to 14 nm technology [1].

	22 nm	14 nm	scale
Transistor fin pitch	60 nm	42 nm	.70×
Transistor gate pitch	90 nm	70 nm	.78×
Interconnect pitch	80 nm	52 nm	.65×

demonstrated that scaling the device by a factor κ improves the switching speed by κ, reduces the power dissipation by κ^2 and increases the power-delay product by κ^3 [9]. While the basic concepts proposed in the constant-field scaling [15] provide a basic guideline to the design of scaled devices, fundamental limits have imposed new boundary conditions for transistor scaling in the sub-100nm regime, resulting projected slowdown in the rate of gate length reduction [18, 19]. In addition, the power supply voltage (V_{DD}) could not be scaled in proportion to channel length since the oxide field had been increasing over the generations of CMOS technology. Thus, in generalized scaling [16], where two scaling factors are used (α, κ), it was proposed that if both the vertical and the lateral electric fields change by the same multiplication factor, the shape of the electric field pattern can be preserved. The scaling law was followed by the semiconductor industry until approximately 2005. However, these days, more complicated knowledge is needed to scale down the minimum feature size of state-of-the-art

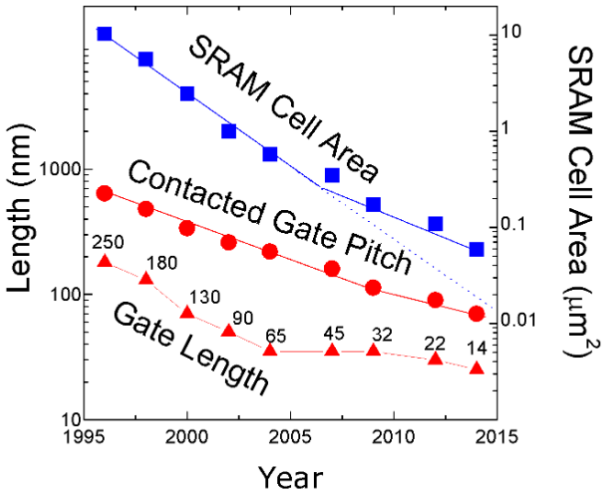


Figure 1-1. Historical trend of gate length, contacted gate pitch, and SRAM bit cell size based on Intel's publications.

microprocessor chips due to short-channel effects. For instance, Table 1-2 shows that dimension scaling from 22 nm to 14 nm technology [1]. In fact, an incredible scaling of the CMOS technology lasted over a period of nearly two decades as shown in Figure 1-1 [20]. However, scaling the planar bulk MOSFET beyond 22nm technology is not practical owing to severely reduced electrostatic behavior [21]. In the following Chapter 1.1.2, several short channel effects which affect electrostatic behavior are described.

1.1.2 Short channel effects

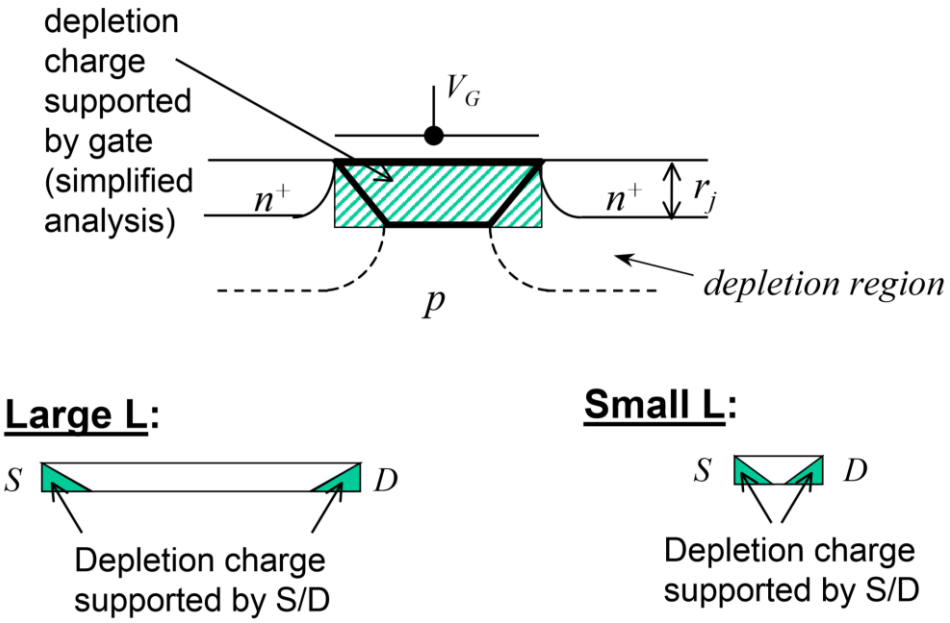


Figure 1-2. Cross-sectional view of MOSFET along the length showing depletion charge sharing between the source/drain and the gate [3].

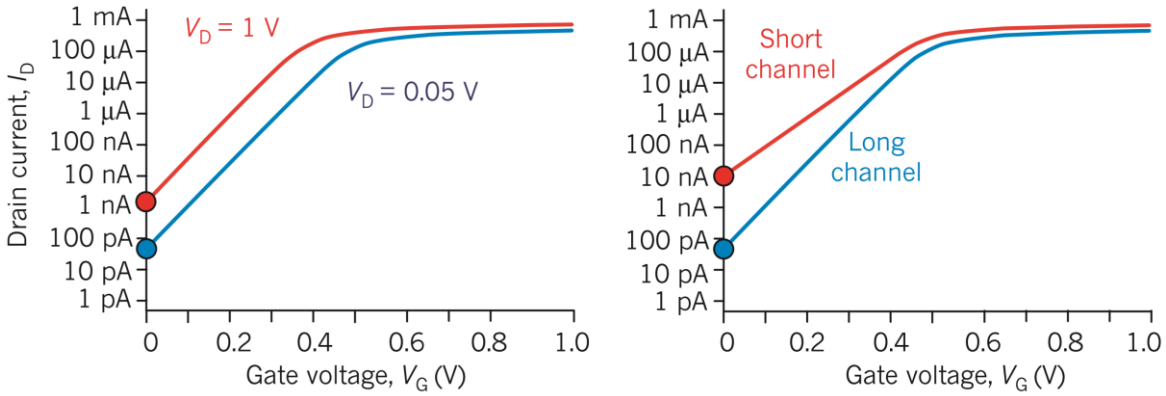


Figure 1-3. (a) DIBL effect shifts the blue curve to the red curve when the drain bias increases. (b) The subthreshold slope (*SS*) increases when the channel length becomes shorter. Both of these effects increase the off currents. [9].

In reality, the root cause of the short channel effects originated from the charge sharing between the source/drain and the gate [22]. As shown in Figure 1-2, the depletion charge is divided into a central trapezoidal shape region controlled by the gate and approximately triangular regions governed by the source/drain [3]. The depletion regions near the source and the drain penetrate the channel region, shortening the effective channel length. These depletion regions carry electric fields that penetrate the channel region to a certain distance and steal some of the control of the channel from the gate, thus reducing the ability of the gate on the channel [9]. As a result, the potential in the channel region underneath the gate is no longer controlled solely by the gate but also controlled by the drain. For a long channel transistor, the triangular depletion charge regions governed by the source and the drain are a small fraction of the total depletion charge under the gate. However, as the channel length are scaled down, the triangular shared charge becomes a larger fraction of the total.

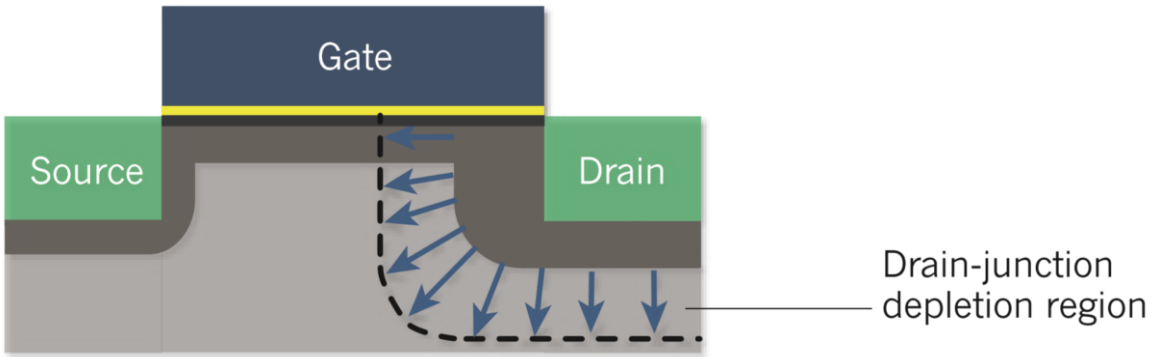


Figure 1-4. The width of the drain junction depletion region increases as the drain voltage increases, causing the drain-induced-barrier lowering (DIBL) effect [9].

Drain-induced barrier lowering (DIBL) results from the loss of charge control by the gate. DIBL causes the V_{th} to decrease when the drain bias increases.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{V_{th}\big|_{\text{at }(V_{DS1})} - V_{th}\big|_{\text{at }(V_{DS2})}}{V_{DS2} - V_{DS1}} \tag{1.3}$$

where V_{th} and V_{DS} refer to the threshold voltage and the drain voltage, respectively. The width of the depletion region governed by the drain junction extends laterally underneath the gate when the drain bias increases as shown in Figure 1-4. As another short channel effects, subthreshold swing (*SS*) degrades when the channel length becomes shorter.

$$SS = \frac{dV_G}{d(\log(I_D))} = n(\frac{kT}{q})\ln(10), \qquad \text{where } n = \frac{dV_G}{d\phi_{CH}} \tag{1.4}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, q is the charge of an electron, and n

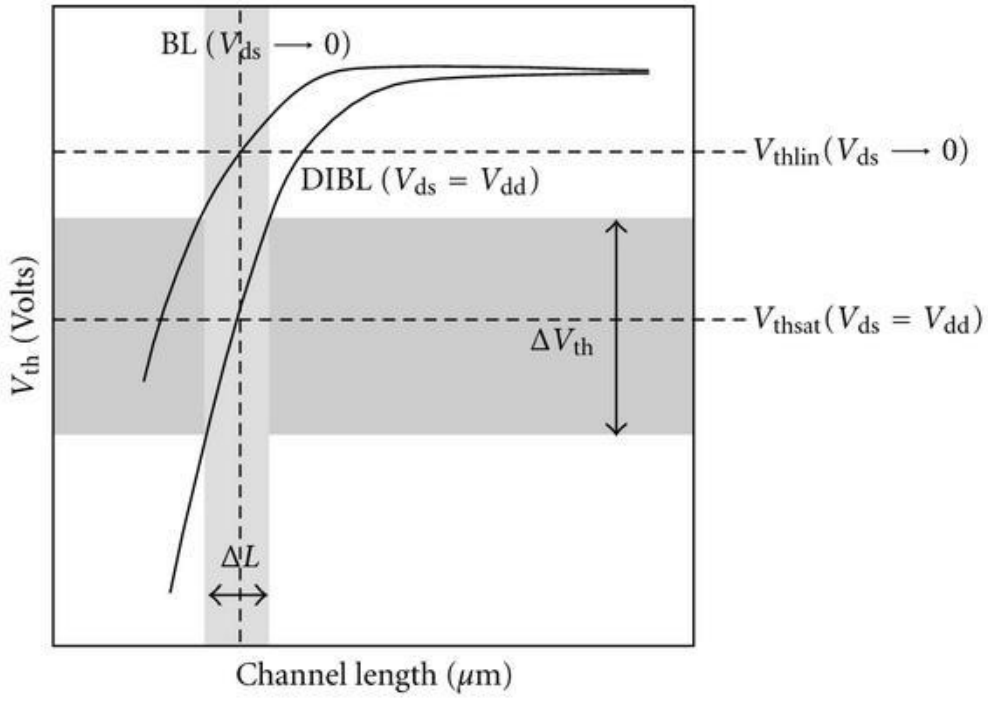


Figure 1-5. Barrier lowering (BL) resulting in threshold voltage roll-off [6].

is the body factor. For an ideal transistor with the best possible case, that is the electrostatic coupling between the gate and the channel region is 100% effective, *SS* becomes 59.6 mV decade^{-1} at room temperature (T = 300 K). Unfortunately, n is greater than 1 for actual devices due to the electrostatic coupling between the channel and the substrate through the depletion layer, thus n typically has a value between 1.2 and 1.5 in bulk MOSFET resulting in *SS* values of 70-90 mV decade^{-1}. These DIBL and *SS* are additive and increase the leakage current of the transistors, which is a serious impediment to further scaling of the transistors.

Another short channel effect is V_{th} roll-off as shown in Figure 1-5 [6]. This is undesirable since the circuit designers would like threshold voltage to be invariant with transistor dimensions or biasing conditions. In a VLSI technology, the channel length varies statistically from chip to chip, and wafer to wafer due to process variability. Therefore, in the device design, designer must ensure that several parameters are in process design margins.

1.2 Process-induced structural Variability

In the nanometer regime, the imperfect shape of patterning caused by process variation has increased significantly. Figure 1-6 shows a failure under certain process conditions for a design that meets design rules and the lines are not yet shorted but are already close that they pose a reliability hazard [5]. Because of the slow evolution of the photolithography technology, it is too difficult to obtain perfectly rectangular lithographic patterns. Therefore, line-edge roughness (LER) (Figure 1-7) occurs in the order

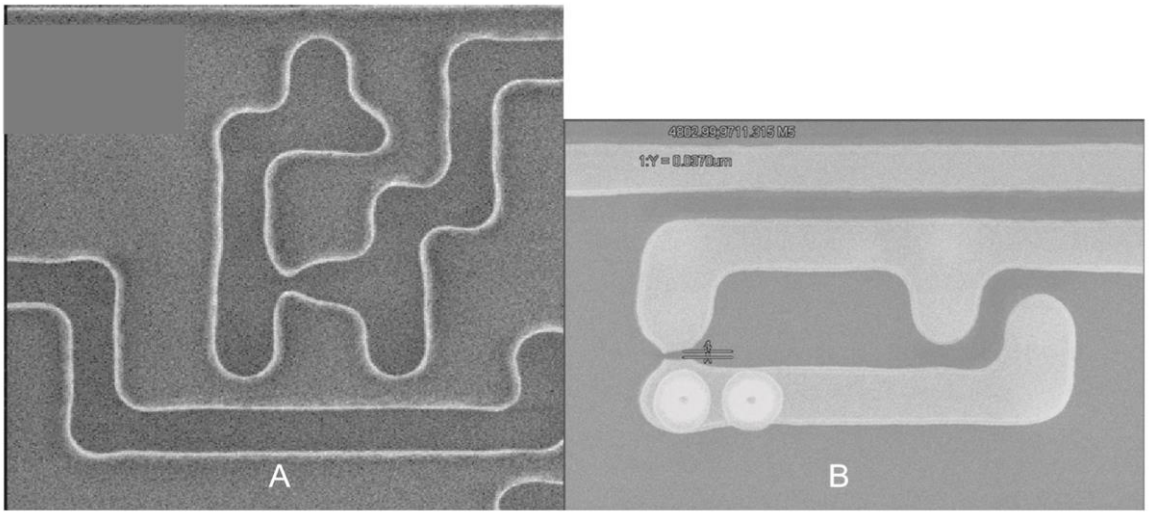


Figure 1-6. Failure at a process corner for a design that met design rules [5].

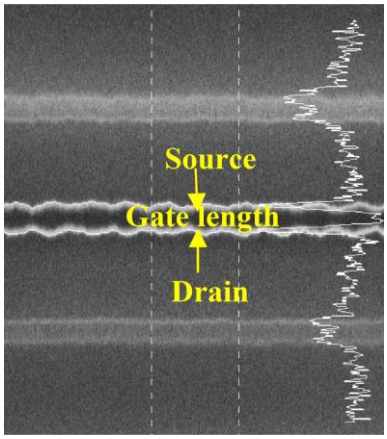


Figure 1-7. Top down scanning electron microscopy (SEM) image of line-edge roughness [4]

of several nanometers and does not decrease as the device shrinks [23]. This problem leads to serious device parameter fluctuations and makes circuit analysis difficult. Because of the LER effect, the discrepancies in the analysis of device performance caused by the non-rectilinear gate (NRG) effect have worsened with rapid CMOS technology scaling. Specifically, in circuit analysis, a substantial discrepancy is observed between the results of post-lithography simulations and the results of circuit simulations, leading to significant impacts on timing and power analysis [7]. The operation of a device with an NRG can be predicted by TCAD simulations; however, a circuit-level simulation involving a large number of transistors is very time consuming. Thus, it is important to not only capture the effect of an NRG with sufficient accuracy but also incorporate the effects into standard circuit simulation tools such as SPICE with a reasonable simulation time.

1.3 Progress of multi-gate technology

With the advancement of manufacturing technology, despite many obstacles such as short-channel effects or variability, the planar transistor has been successfully scaled down to a technology node of 32 nm [10, 24]. However, the ability for gate to effectively control the channel diminishes due to such an aggressive reduction in size. The reduced controllability of the gate over the channel results in a significant increase in the leakage current and short channel effects, leading to drastic change in the use of conventional planar devices for IC design [25]. The classical solution for the reduced gate controllability issues in deep submicron regime has been to increase the gate capacitance by reducing the oxide thickness in proportion to the channel length. However, this approach is no longer effective to meet the device requirements (e.g., leakage) beyond a 32-nm technology. To address this issue, multi-gate structures are introduced to increase the gate controllability as non-classical device architectures

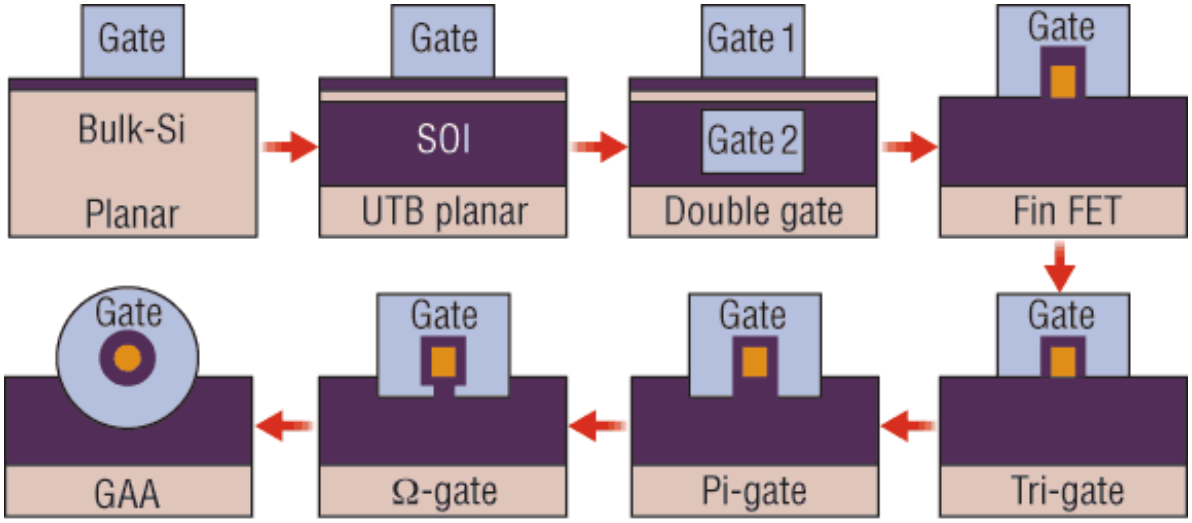


Figure 1-8. Evolution of field effect transistors from single-gate to multiple-gate structure [12].

[26]. The electrostatic control on the channel gets improved in multiple-gate structures as the gate control the channel from more than one side. Therefore, the concept of multi-gate, such as double-gate or FinFET and triple-gate transistors, has been proposed and heavily investigated to overcome the bottlenecks for the continuous scaling [9, 27].

Figure 1-8 shows the evolution of field effect transistors from single to multiple-gate structure [12].

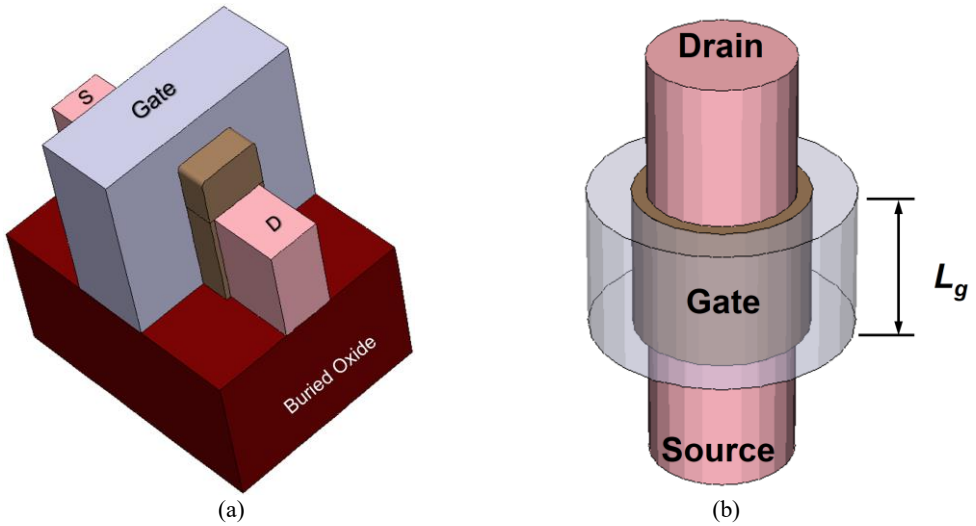


Figure 1-9. (a) Fin-field effect transistor (FinFET) and (b) gate-all-around (GAA) transistor.

Among the several structures of multi-gate transistors, the FinFET , as shown in Figure 1-9 (a), is one of the promising alternatives to conventional planar devices because of its better immunity to SCEs, higher current drive strength, and improved subthreshold swing [28]. In addition, the FinFET is the most promising alternative because the fabrication of FinFETs is very similar to that of conventional MOSFETs compared to other multi-gate technologies [29]. In fact, the leading IC manufacture company introduced the first 22-nm FinFET CMOS technology chip in mass production [30].

However, even for FinFET, the ability for gate to effectively control the channel is also expected to be diminished due to such an aggressive reduction in size. Beyond the 10-nm technology node, the gate-all-around (GAA) FET is the natural evolution of multi-gate architectures and is considered to be a promising solution for continuing Moore's law [13]. As next one of the most promising architectures for the ultimately scaled device the gate-all-around (GAA) silicon nanowire field effect transistor (SNW FET), as shown in Figure 1-9 (b), began to attract attention due to its excellent electrostatic capability of the channel control and efficiency of its practical design [31-33].

1.4 Dissertation outline

The original contributions and main focus of this dissertation include:

1. Development of simple and accurate modeling technique that analyzes a non-rectilinear gate (NRG) transistor with a simplified trapezoidal approximation method [34].
2. Utilizing diffusion rounding effect to optimized device layout for better electrical behavior of transistors [35].
3. Investigation of impacts of trapezoidal fin of 20-nm double-gate FinFET on the Electrical Characteristics of Circuits and optimal angle range. Analysis of this trapezoidal shape along the fin height can provide the optimum trapezoidal angle in circuit performance [36].
4. Investigation of the electrical characteristics of double gate-all-around (DGAA) transistor with an asymmetric channel width. Analysis of the asymmetry in the channel width can provide the optimal structures of the *n*- and *p*-type DGAA FETs to form a basic logic gate, the inverter [37].
5. Application of DGAA transistor to on chip interconnect boosting firstly. This work proposes a boosting structure that can significantly improve the performance of circuits by controlling the two gates of the DGAA independently [38].

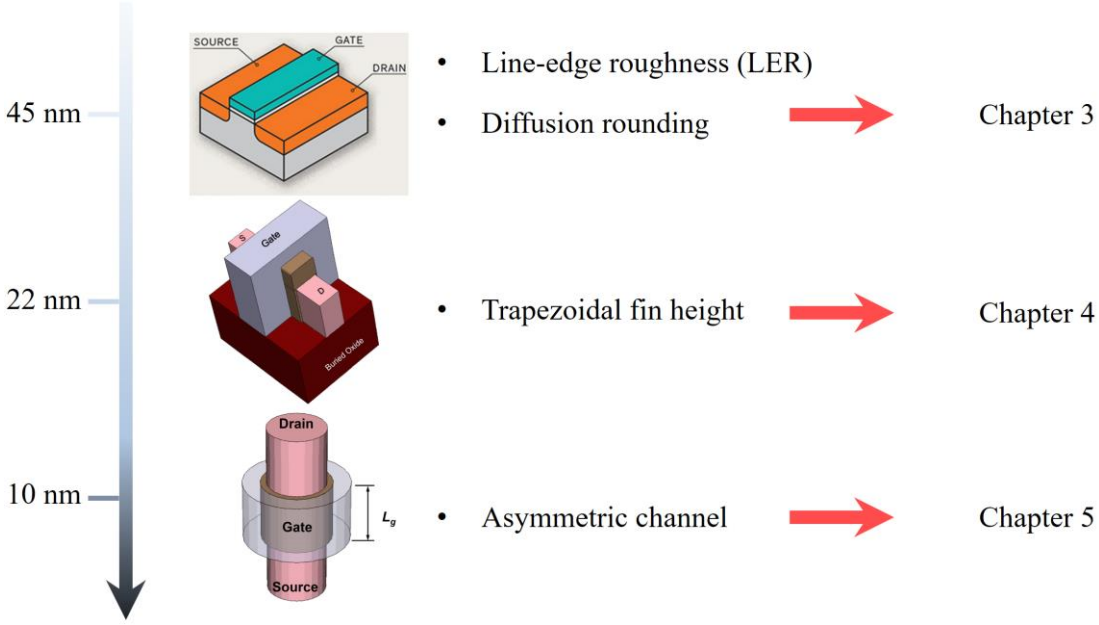


Figure 1-10. Process-induced variability problems in this dissertation.

This dissertation is organized as follows:

Chapter 1 covers fundamental background knowledge for the following chapters. More specifically, the history and principles of transistor scaling down are covered. And then the short channel effects are described, which is the limiting factor of the scaling of planar transistor beyond 32 nm. Following that, variability issues are reviewed, which becomes important as the technology node move to nanometer regime. Next, the progress of multi-gate technologies is reported.

Chapter 2 reviewed the previous works of other research groups and their limitations. The limitations become the motivation of this dissertation.

Chapter 3 of this dissertation focuses on the structural variability-aware optimization for CMOS technologies first. Non-rectilinear gate (NRG) transistors are approximated into trapezoidal shapes, three geometry-dependent parameters are extracted from post-lithographic patterns. Second, a simple optimization of device layout for CMOS technologies is presented. The optimized device layout is developed by using diffusion rounding effect for better electrical behavior of transistors.

Chapter 4 discusses the optimization and analysis of process-induced trapezoidal fin of double-gate FinFET. The performance impacts of the trapezoidal fin shape of a double-gate FnFET on the electrical characteristics of circuits are discussed. The trapezoidal nature of a fin body is generated by varying the angle of the sidewall of the FinFET. Several performance metrics are evaluated to investigate the impact

of the trapezoidal fin shape.

Chapter 5 focuses on the optimization of DGAA FET with process-induced asymmetric channel width. This work investigates the electrical characteristics of a DGAA transistor with an asymmetric channel width first. The channel width asymmetry is analyzed on both sides of the terminals of the transistors, i.e., source and drain. In addition, both *n*-type and *p*-type DGAA FETs are considered. Secondly, we propose the application of DGAA transistor to on chip interconnect boosting. This work proposes a boosting structure that can significantly improve the performance of circuits by controlling the two gates of the DGAA independently.

In Chapter 6, as a future work, a novel inverter structure is discussed. This structure named as sandwiched-gate inverter (SG INV) consisted of an NMOS GAA together with a donut-type PMOS, which can improve the overall circuit footprint area by combining separate *p*-type GAA and *n*-type GAA together. In addition, the proposed SG INV can be used to construct NAND, NOR, and SRAM cells and will significantly reduce the overall size of the chip when the manufacturability of the vertical GAA matures.

Finally, Chapter 7 concludes the whole project work of this dissertation.

Analysis and optimization for device-level variability are critical in integrated circuit designs of advanced technology nodes. Thus, the proposed methods in this dissertation will be helpful for understanding the relationship between device variability and circuit performance. The research for advanced nanoscale technologies through intensive TCAD simulations, such as FinFET and GAA, suggests the optimal device shape and structure. The results provide a possible solution to design high performance and low power circuits with minimal design overhead.

Chapter 2. Literature review and limitations of previous works

From the literature survey of various type of variability analysis methods in this Chapter, we will review several post-lithographic simulation (PLS) techniques, which can handle NRG transistors, have been proposed [7, 39-42]. Most of these techniques are based on a gate slicing method and an equivalent gate length (EGL) method, which use the summation of I_{on} and I_{off} in each slice after uniformly partitioning a given device channel into small slices as shown in Figure 2-1. The gate slicing method is used to compute the current of the NRG devices, and the EGL method maps the computed I_{on} or I_{off} to an equivalent device suitable for on or off state simulations [39]. The NRG channel region is divided uniformly along the width of the device, and then, the summation of each device slice is carried out to obtain the same current. Here, the previous works for variability analysis methods are as follows:

- In [7], a gate-voltage-dependent model of the equivalent gate length is developed. The proposed model is validated by TCAD simulations; however, the source codes inside the device simulator need to be modified, which complicates the implementation.

- In [39], both the gate slicing method and the EGL method are used. The disadvantage of this EGL method is that two equivalent devices are produced, namely, an on-EGL device for timing simulations and an off-EGL device for leakage simulations. As it is difficult to determine whether a device is in the on or off state, applying this EGL method could be problematic. In addition, the impact of the edge effects is not addressed in this study.

- In [40], the authors use the EGL method and consider the location-dependent threshold variation caused by the edge effects. However, this technique suffers from the same drawbacks because of the use of the EGL method.

- In [41], a unified model is proposed on the basis of a current-modification method; however, additional model cards are needed to adjust the device according to the gate shape. The application of this method increases circuit complexity and complicates its implementation.

- In [42], the authors model line-end extension (LEE) as a super-ellipse and also use the gate-slicing and EGL methods.

The on-off characteristics of the devices are modeled through these approaches, which can analyze the electrical characteristics caused by the imperfect gate shape of transistors and show good agreement with SPICE results. However, modeling using these approaches is not only cumbersome but also requires a large amount of resources (i.e., many mathematical calculations and a long runtime).

As an another result of variability on account of imperfect gate patterning, rounded diffusion shape

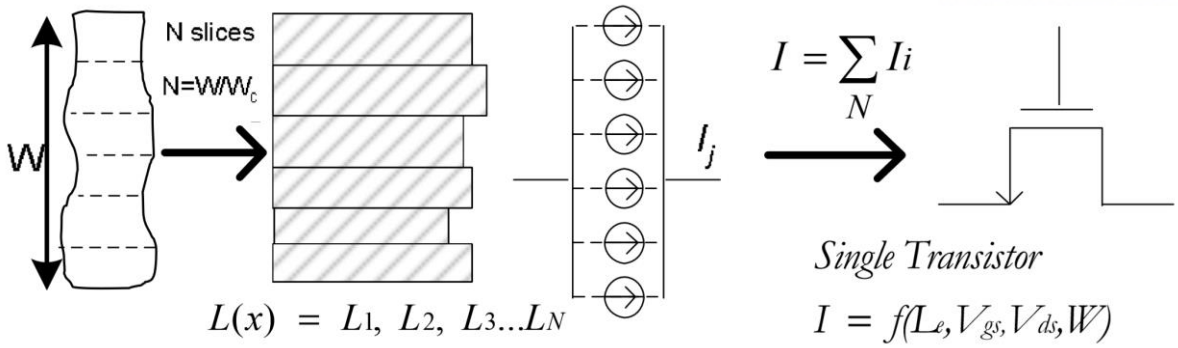


Figure 2-1. Equivalent transistor model for NRG effect [7].

happens in various locations with different forms as shown in Figure 2-2. A few attempts have been made to model the impact of diffusion rounding in the MOSFET. Several previous works are as follows:

- In [8] the authors proposed a simple model to capture the electrical effects by diffusion rounding in the NMOS and PMOS. It used effective width change by diffusion rounding for I_{on} and effective channel length change for I_{off}.
- Another work [43] proposed an analytical approach to calculate effective V_{th}, channel length and device width by diffusion rounding.

Both papers indicated that diffusion rounding has different effects on the transistors' electrical

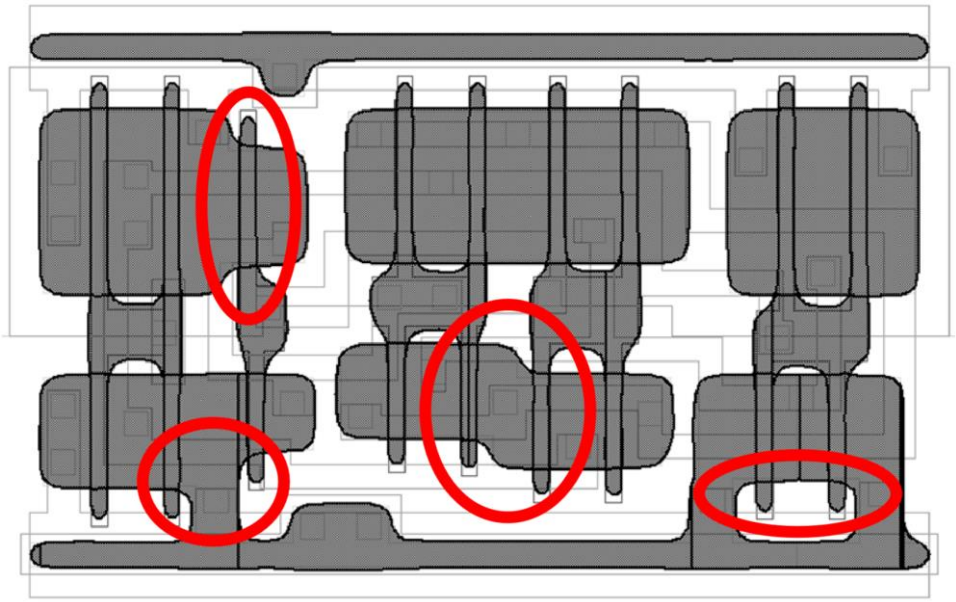
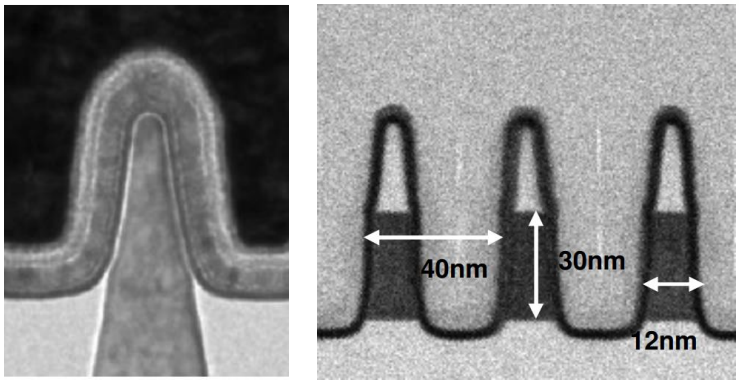


Figure 2-2. Lithography simulation contour showing diffusion rounding in a layout at the 90-nm technology node [8].



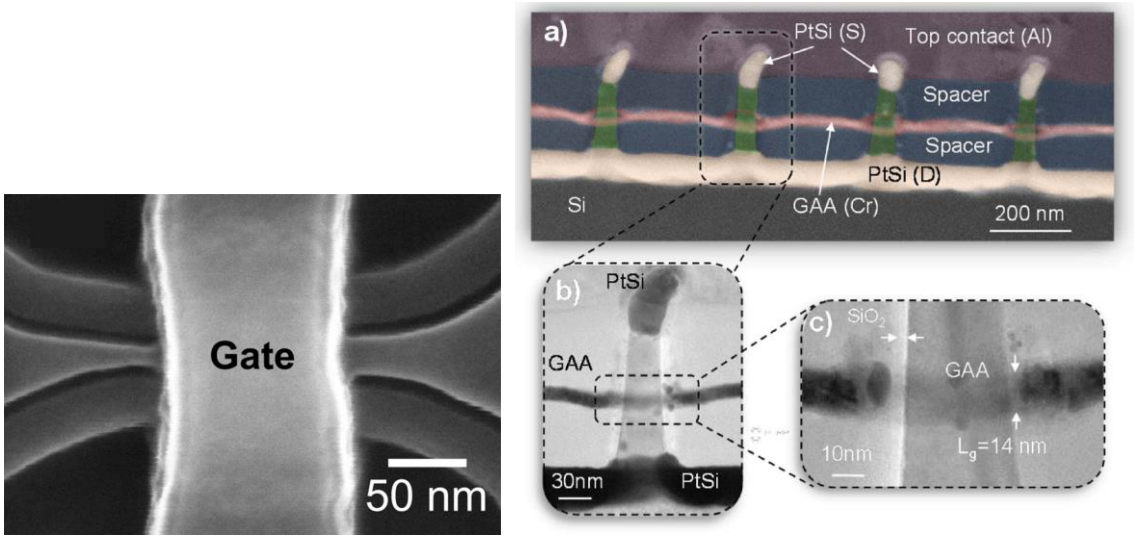
(a) (b)

Figure 2-3. Cross-sectional TEM images of (a) a FinFET channel [10] and (b) multi-finger FinFET arrays [14] under the gate along the fin-width direction.

characteristics depending on the location of the rounding (either source side or drain side).

With the advancement of manufacturing technology, despite many obstacles such as short-channel effects or variability, the planar transistor has been successfully scaled down to a technology node of 32 nm [10, 24]. However, the ability for gate to effectively control the channel diminishes due to such an aggressive reduction in size. The electrostatic control on the channel gets improved in multiple-gate structures as the gate control the channel from more than one side. Among the several structures of multi-gate transistors, FinFET is one of the promising alternatives to conventional planar devices because of its better immunity to SCEs, higher current drive strength, and improved subthreshold swing [28]. The trapezoidal nature of a fin body is generated by varying the angle of the sidewall of the FinFET. In fact, it was revealed that the microscopic cross sections of the fin body of the transistor in the processor actually have a trapezoidal shape, as shown in Figure 2-3 [10, 14, 44]. Although a FinFET is believed to have uniform thickness across the height of a fin, the trapezoidal cross section has been found to be markedly different from the idealized rectangular fin body in many studies [45]. It is not clearly known whether the non-vertical cross section of the fins are manufacturing artifacts or are deliberately engineered to provide useful benefits in the chip. In [10], the authors claimed that obtaining a uniform thickness across the entire height of the fin is extremely difficult in the current process technology. Thus, its real geometry has an angle of inclination along the fin height. Whether intentional or due to manufacturing imperfections, the real trapezoidal cross section requires appropriate models to predict electrical behaviors. The impacts of the angle variation along the height of the fin have been investigated by TCAD simulations in previous works [46-48].

- In [46], the impact of a nonrectangular fin cross section on the electrical characteristics of a FinFET was characterized. However, the paper analyzed the impact on the device level only and did not address the impact of angle variation on the circuit level.



(a) (b)

Figure 2-4. (a) A plan-view secondary-electron microscope image of an asymmetric silicon nanowire FET [11] and (b) Transmission electron micrographs of the vertical nanowire array transistor [13].

- In [47], although the electron and current density profiles as a function of inclination angle for various body doping levels are investigated by TCAD simulations, the authors did not take circuit-level performance into account.

- Another paper [48] has claimed that a triangular shape, an extreme case of a trapezoidal shape, of a FinFET provides advantages in performance and energy savings, resulting in the ring oscillator operating faster than a FinFET with rectangular fins. However, only two cases (rectangular and triangular case (8° inclination angle)) were analyzed in their work without analyzing other trapezoidal angle.

From the literature review of the FinFET, it is clear that very few studies have been conducted to investigate the optimum trapezoidal angle for the dynamic performance of the circuits for various angle.

As next one of the most promising architectures for the ultimately scaled device the gate-all-around (GAA) silicon nanowire field effect transistor (SNW FET) is noticeable. In fact, one recent study showed that junctionless silicon nanowire transistor device concept works at scales as small as wire diameter of ~ 1 nm and gate length of ~ 3 nm [49]. However, horizontal GAA nanowire transistors also have scaling down issues in the lateral direction due to increased parasitic resistances and capacitances resulting from decreased diameters and extension lengths [50-52]. Vertical GAA FET have been emerged to reduce parasitic components and for higher device integration without scaling down physical gate lengths and extension lengths [53-55]. Furthermore, vertical GAA approaches has merits by its fabrication process for nanoscale transistor realization because the gate length is merely defined

by the thickness of the deposited gate material, opening the way to scale down of gate length more [13].

Although the enhanced gate controllability on the channel of the multi-gate technology, the process-induced structural variation also happens in the multi-gate transistors and makes the design unpredictable. In fact, it is reported that asymmetric channel structure is expected for vertically stacked silicon nanowire FET due to the fabrication process [11] as shown in Figure 2-4 (a). In another research [13] on GAA array as shown in Figure 2-4 (b), the asymmetric channel structure is confirmed by TEM cross-section. The electrical properties of vertical silicon nanowire structures with an asymmetric channel width have been investigated in previous studies [53, 56] as follows.

- In [56], structural effects in sub-20-nm gate-all-around silicon nanowire field effect transistors having asymmetric channel width along the channel direction are demonstrated using three-dimensional device simulations.

- In [53], vertical gate-all-around (GAA) junctionless nanowire transistors (JNTs) with different diameters and underlap lengths are investigated using three-dimensional device simulations.

However, only *n*-type transistors were analyzed in these studies and the effective channel area was not considered. Moreover, in this case, it is difficult to determine whether the performance differences in comparison targets are caused by structural differences (i.e., asymmetry) or by effective area.

In the Chapter 4 and Chapter 5, the impacts of structural variation for multi-gate technology on the circuit level parameters are evaluated in detail and utilized to find the optimal device shape and structure.

Chapter 3. Structural variability-aware optimization for CMOS technologies

3.1 Trapezoidal approximation for on-current modeling of 45-nm non-rectilinear gate shape

In this work, a simple and accurate modeling technique that analyzes a non-rectilinear gate (NRG) transistor with a simplified trapezoidal approximation method is proposed. To approximate a non-rectangular channel shape into a trapezoidal shape, we extract three geometry-dependent parameters from post-lithographic patterns: the minimum channel length from the slices (L_{min}), maximum channel length from the slices (L_{max}), and effective channel width (W_{eff}). We slice the NRG transistor gate along its width, sort these slices according to their sizes, and then use trapezoidal approximation. Simple modeling using trapezoidal approximation becomes possible by using the above-mentioned three new parameters from the NRG shape in a post-lithographic simulation. A physics-based technology computer aided design (TCAD) simulation is used to verify our model in a typical 45-nm process. The developed model requires fewer computations and less runtime as compared to the previous approaches. Therefore, a full chip post-lithography analysis (PLA) becomes feasible. As the scale of semiconductor devices has decreased to the sub-wavelength regime, the imperfect shape of gate patterning caused by process variation has increased significantly. Because of the slow evolution of the photolithography technology, it is too difficult to obtain perfectly rectangular lithographic patterns. Therefore, line-edge roughness (LER) (Figure 3-1) occurs in the order of several nanometers and does not decrease as the device shrinks. This has evolved into a critical problem in nanometer regimes [23]. This problem leads to serious device parameter fluctuations and makes circuit analysis difficult. Because of the LER effect,

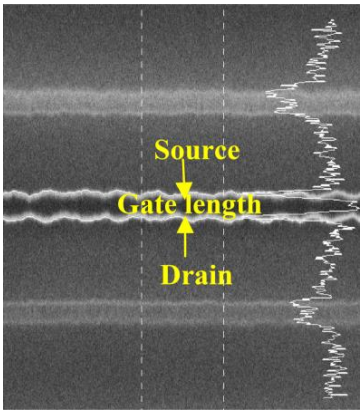


Figure 3-1. SEM image of line-edge roughness [4]

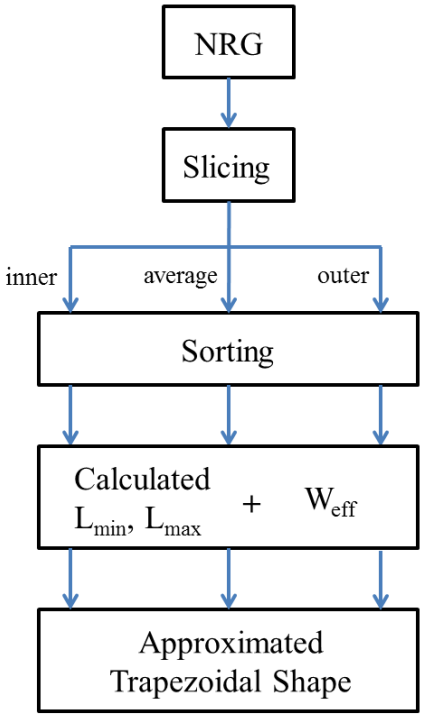


Figure 3-2. Procedure to approximate NRG transistor into trapezoidal shape.

the discrepancies in the analysis of device performance caused by the non-rectilinear gate (NRG) effect have worsened with rapid CMOS technology scaling. Owing to the shape of a non-rectilinear gate that is significantly distorted from the designed rectangular layout, the leakage current (I_{off}) of the device has increased considerably. Furthermore, in circuit analysis, a substantial discrepancy is observed between the results of post-lithography simulations and the results of circuit simulations, leading to significant impacts on timing and power analysis [7]. The operation of a device with an NRG can be predicted by TCAD simulations; however, a circuit-level simulation involving a large number of transistors is very time consuming. Thus, it is important to not only capture the effect of an NRG with sufficient accuracy but also incorporate the effects into standard circuit simulation tools such as SPICE with a reasonable simulation time. In this study, we propose a technique for simple and accurate modeling that analyzes an NRG transistor with a simplified trapezoidal approximation method. The procedure of the trapezoidal approximation method is shown in Figure 3-2. On the basis of our model, three geometry-dependent parameters (L_{min}, L_{max}, W_{eff}) from post-lithographic patterns are extracted in three different cases: inner, outer, and average approximations. The scanning electron microscope (SEM) images of the practical channel region of the metal-oxide-semiconductor (MOS) transistor that is distorted from the designed rectangular shape and one of the slices after slicing the channel region are shown in Figure 3-3 and Figure 3-4, respectively. To validate the trapezoidal approximation, we intentionally introduce irregularities in the length of the channel along the width of the channel. We

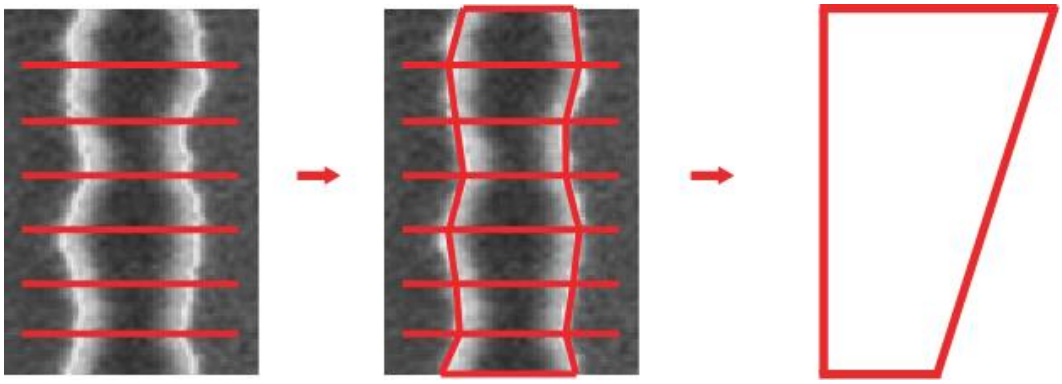


Figure 3-3. SEM image of a gate with LER with slicing and the final trapezoidal approximation.

analyze an NRG by slicing uniformly along the width of the channel, depending on the length of the slices, and then, the slices are sorted according to their sizes by the simple modeling method of trapezoidal approximation. This method is used to approximate an NRG into a trapezoidal shape with the length of the biggest slice (L_{max}) and the length of the smallest slice (L_{min}) to obtain the same electrical characteristics (I_{on}) of the transistors compared to the original NRG. The advantage of the proposed trapezoidal approximation models is to obtain accurate on-currents for various NRG devices with simple calculations without TCAD simulations and slicing methodology used in [7, 39, 40]. The accuracy and simplicity come from the consideration of edge effect by W_{eff} and the use of only three geometry parameters to obtain the model, respectively. This work is organized as follows. Chapter 2.1.1 proposes the trapezoidal approximation model and its application to a fictitious hexagonal shape considered to be a simple NRG. Chapter 2.1.2 includes TCAD simulation setup and model verification. In Chapter 2.1.3, real NRG shapes from a post-lithography simulation are analyzed, and Chapter 2.1.4 presents chapter summary.

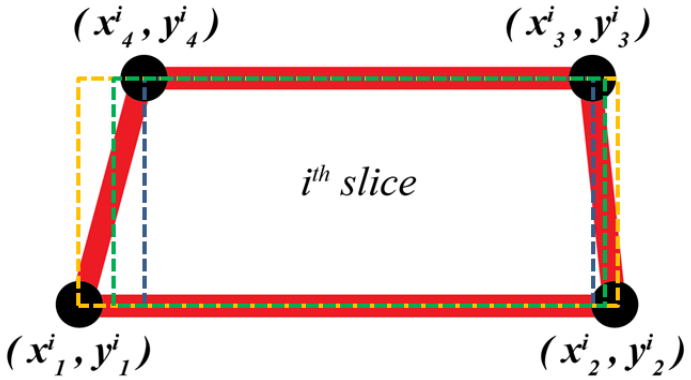


Figure 3-4. Blue line: inner approximation, green line: average approximation, and yellow line: outer approximation.

3.1.1 Trapezoidal approximation Model

$$
\begin{cases}
L^i_{inner} = \left|\min(x^i_2, x^i_3) - \max(x^i_1, x^i_4)\right| & , where\ 1 \le i \le n;\ \text{n = \# of slices} \\
L^i_{outer} = \left|\max(x^i_2, x^i_3) - \min(x^i_1, x^i_4)\right| & x^i_n \ \ in \ \ Fig.\ 3 \\
\begin{cases} L_{\min} = \min(L^1_{inner}, \cdots, L^i_{inner}, \cdots, L^n_{inner}) \\ L_{\max} = \max(L^1_{inner}, \cdots, L^i_{inner}, \cdots, L^n_{inner}) \end{cases} & : inner\ approximation \\
\begin{cases} L_{\min} = \min(L^1_{outer}, \cdots, L^i_{outer}, \cdots, L^n_{outer}) \\ L_{\max} = \max(L^1_{outer}, \cdots, L^i_{outer}, \cdots, L^n_{outer}) \end{cases} & : outer\ approximation \\
\begin{cases} L_{\min} = \min(\frac{L^1_{inner} + L^1_{outer}}{2}, \cdots, \frac{L^i_{inner} + L^i_{outer}}{2}, \cdots, \frac{L^n_{inner} + L^n_{outer}}{2}) \\ L_{\max} = \max(\frac{L^1_{inner} + L^1_{outer}}{2}, \cdots, \frac{L^i_{inner} + L^i_{outer}}{2}, \cdots, \frac{L^n_{inner} + L^n_{outer}}{2}) \end{cases} & : average
\end{cases}
\tag{3.1}
$$

Assuming that the NRG has a hexagonal shape, modeling with the trapezoidal approximation is proposed. As shown in Figure 3-5 (a) and (b), each shape has two points near the center, and the shapes are two representative examples (in the case of HDL > 0, HDL < 0, respectively, where HDL is the half delta length; variation of the gate shape at one side) of various hexagonal shapes. Once the coordinates of any LER shape are given, we can extract L_{min} and L_{max} on the basis of the inner, outer, and average approximations as shown in (3.1). In this study, the average approximation is used to obtain L_{min} and L_{max} since its result provides the minimum error with the original pattern compared to inner or outer

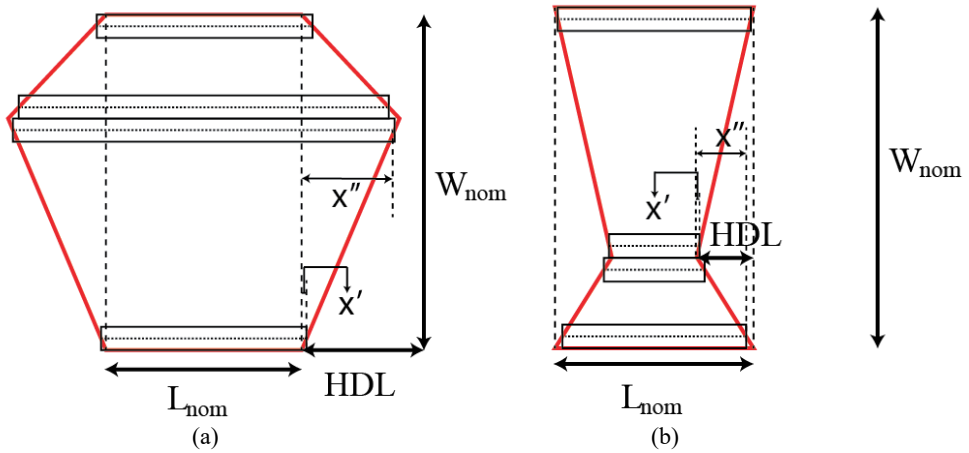


Figure 3-5. Two representative non-rectangular transistors in the channel region: (a) HDL > 0, (b) HDL < 0.

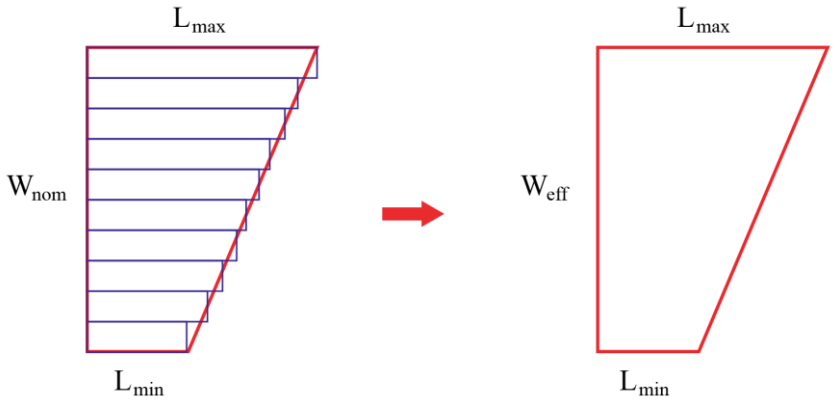


Figure 3-6. Approximated equivalent trapezoidal channel; (a) trapezoidal shape after sorting according to size, (b) trapezoidal shape with effective width.

approximations. The extracted L_{min} and L_{max} from our model can be used to approximate the fictitious NRG shape into a trapezoidal shape.

Figure 3-6 (a) shows an array of slices in the descending order of size, forming an approximated trapezoidal shape by connections between the upper right point in the largest slice and the lower right point in the smallest slice, and Figure 3-6 (b) shows the approximated trapezoidal shape with effective width W_{eff}. This figure shows the approximated shape as a trapezoid that has a length of the top aspect of L_{max} and a length of the bottom aspect of L_{min} as calculated by the equation proposed above.

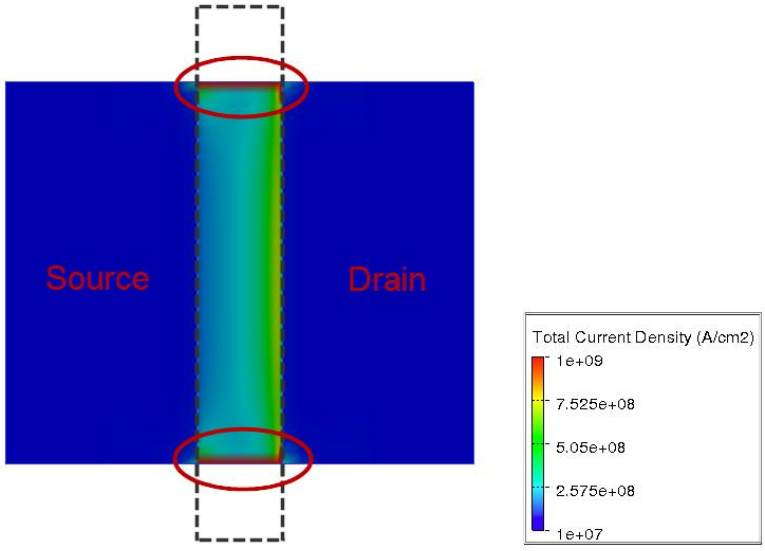


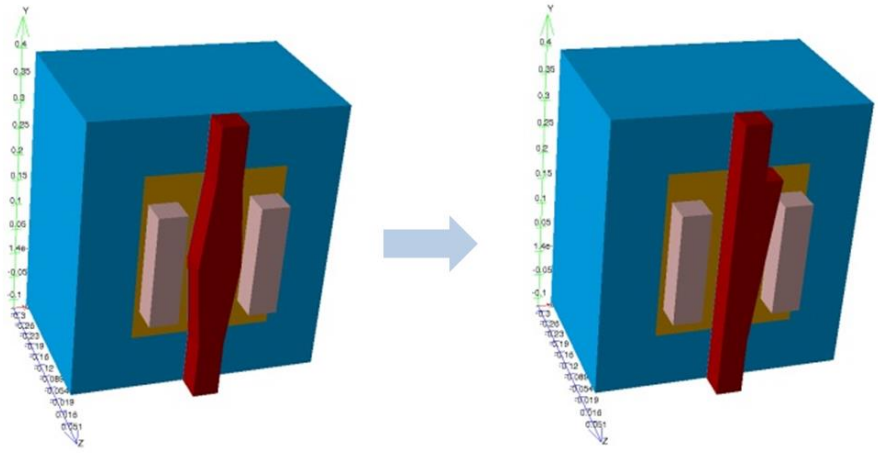
Figure 3-7. TCAD simulation showing edge effects; note that there is a much higher current density in the edge region than in the center.

It is known that threshold voltage (V_{th}) and the current characteristics are different along the channel, which is the so-called "edge effect"— a type of inverse narrow width effect [8, 57-60]. There are several factors causing the device threshold voltage to be non-uniform along the channel width, such as fringing capacitance due to line-end extension [58], dopant scattering due to shallow trench isolation (STI) edges [58], and the well proximity effect (WPE) [61, 62], which are pronounced near the device edges and roll off sharply towards the center of the device [40].

In this study, in order to consider the edge effects by the effective channel length, a weighting factor (effective width W_{eff}) is introduced. The current density profile over a metal-oxide-semiconductor field-effect transistor (MOSFET) device obtained in our simulation is shown in Figure 3-8. As shown in this figure, the current density in the edge region is higher than that in the center region of the channel. When only two parameters are used, i.e., L_{min} and L_{max}, there are still significant discrepancies between the original shape and the trapezoidal approximated shape. This is mainly because there is no way to know the slices are from the center or the edge. We extract L_{min} and L_{max} in a simple NRG channel that has a hexagonal shape. In addition, in order to reduce the approximation errors in the trapezoidal method, we extract W_{eff} by curve-fitting from the TCAD simulation results of the various NRG structures with sweeping of HDL amount and locations. The fitting is just one-time procedure, therefore, for different technology process, simple TCAD extractions are enough to extract W_{eff}. The equivalent trapezoidal shape is verified by TCAD to compare I_{on} of the original transistors.

3.1.2 TCAD setup & model verification

I_D versus V_{DS} data based on a published 45-nm SPICE model [63] is used to set up parameters for the TCAD simulation. To verify the accuracy of our model, a 3D TCAD simulation tool, Silvaco Atlas [64],



(a) (b)

Figure 3-8 3D TCAD structures for model verification: (a) hexagonal shape, and (b) approximated trapezoidal shape.

Table 3-1. 45-nm TCAD model parameters

Parameters	Value
Channel length (L_g) (nominal)	45 nm
Channel width (W) (nominal)	0.2 μm
Supply voltage (V_{DD})	1.0 V
Gate oxide thickness (T_{ox})	1.5 nm
Channel doping	3.92×10^{18} cm^{-3}
Substrate doping (N_{sub})	1×10^{15} cm^{-3}
Junction depth	20 nm
Source/drain region to gate poly	0.04 μm
STI width	0.1 μm
STI depth	0.3 μm

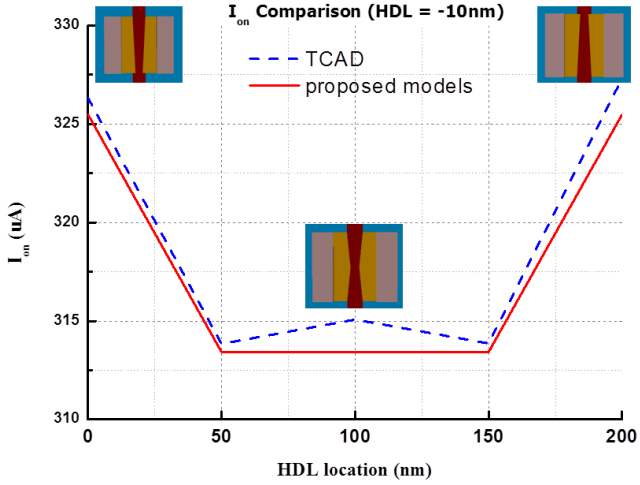
is used. The parameters used in the TCAD simulation are shown in Table 3-1.

The representative factitious NRG transistor structure created by TCAD is shown in Figure 3-7 (a), and the approximated trapezoidal structure calculated by the proposed modeling method is shown in Figure 3-7 (b). To generate simple and representative LER shapes, we sweep both the channel length variation (i.e., HDL from -10 to +10) and the location of the variation in the device width direction (with a step of 10nm). A comparison of I_{on} between the NRG transistor and the approximated trapezoidal transistor by the proposed model at HDL = -10 nm and +7 nm is shown in Figure 3-9 (a) and (b), respectively.

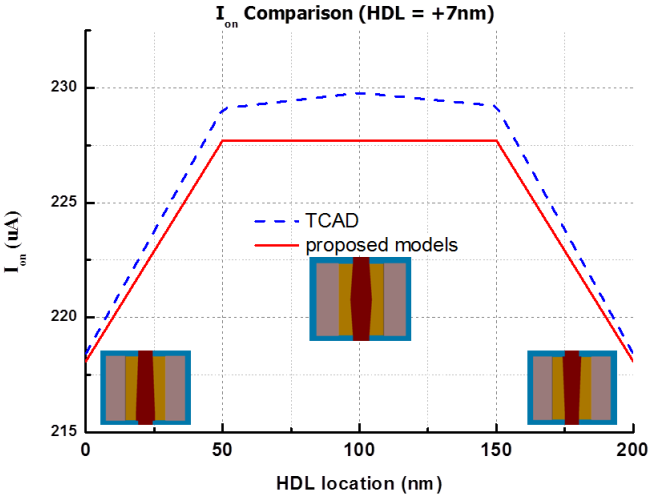
The model accuracy is verified for 40 transistor samples, and the error distributions for both the case of the simulated NRG transistor without W_{eff} and the proposed model with W_{eff} are shown in Figure 3-10. As shown in this figure, the error distribution decreases significantly in the case with W_{eff} compared to that without W_{eff}. The vacant black squares show the results when the trapezoidal approximations are followed by L_{min} and L_{max}. On the other hand, the red dots show the results when the NRG transistors are approximated by L_{min}, L_{max}, and W_{eff}, thus considering the edge effect. Without the weighting factor (W_{eff}), the absolute average error is 3.75%; however, this decreases to 0.6% after applying the weighting factor. As a result of the introduction of the effective width, the model accuracy is improved by 84% as compared to the case without the effective width.

3.1.3 Case study

The developed model is applied to the realistic NRG shapes generated from post-lithography



(a)



(b)

Figure 3-9. Comparison of on-current: (a) in the case of HDL = -10 nm and (b) HDL = +7 nm, where HDL location is the channel length variation point.

simulations of NOR and NAND gates. The post-lithography data are acquired from Mentor Graphics Calibre Workbench [65] simulations, and Figure 3-11 shows the post-lithography images of NOR3 and NAND3 gates. The polygon coordinates of the NRG shapes are obtained in the marked regions. As mentioned in Chapter 3.1.1, after the coordinates of the NRG shapes are acquired from the post-lithography images, the two parameters L_{min} and L_{max} are extracted as coarse tuning parameters, and the effective width parameter W_{eff} is applied as an additional fine-tuning parameter to our model. The weighting factor for the edge or center is selected depending on the dominant variation location along the channel width used to extract W_{eff}. The results of the TCAD simulations show sufficiently accurate agreement with the TCAD results whose three parameters are determined by the proposed trapezoidal approximation.

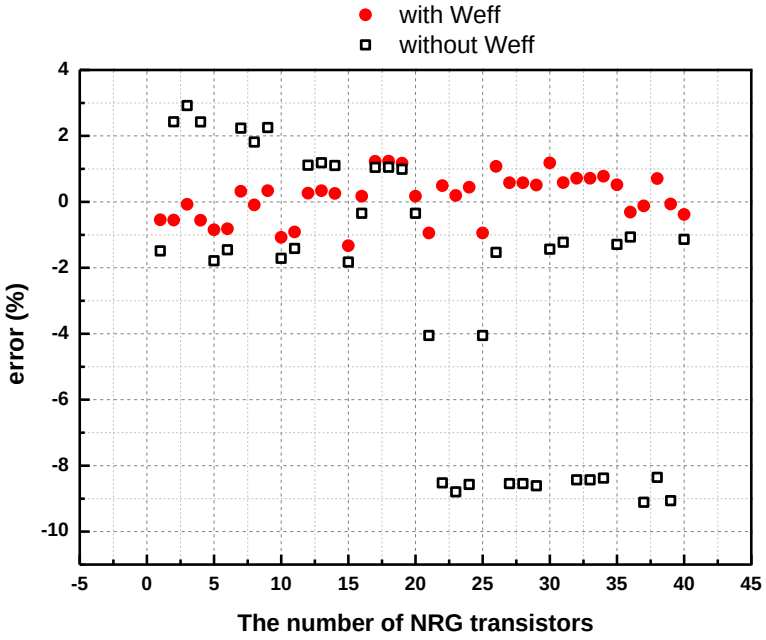


Figure 3-10. I_{on} error distribution.

The simulation results and comparison errors are summarized in Table 3-2. In the case of the on-state ($V_{DS} = V_{DD}$, $V_{GS} = V_{DD}$), the absolute errors of the developed model are only 0.15% and 0.12% for NOR and NAND cases, respectively. This result implies that the proposed model can be applied to an arbitrary imperfect shape with good accuracy, and the accuracy can be improved even more with a width-aware weighting factor. After applying the weighting factor, the absolute error is improved significantly (i.e., from 1% to less than 0.2%). This improvement in the model accuracy originates from the fact that the model with W_{eff} can capture the edge effect well and the results show the effectiveness of using the weighting factor in the approximation.

3.1.4 Chapter summary

We show that the I_{on} characteristics can be modeled by trapezoidal approximation with a simple and fast method using three parameters: L_{min}, L_{max}, and W_{eff}. The electrical characteristics of the LER gate are approximated by a trapezoidal shape, which is acquired by the length of the longest slice, the length of the smallest slice, and the weighting factor, instead of taking the summation of all the slices into account. The results of the TCAD simulation show that the proposed model is suitable for device simulation with edge effects, and its error for I_{on} is around 1% for various NRG transistors. For a more realistic application of the proposed model, we apply the model to NOR and NAND post-lithography images. The absolute errors of the model are 0.76% and 0.97% for the NOR and NAND cases,

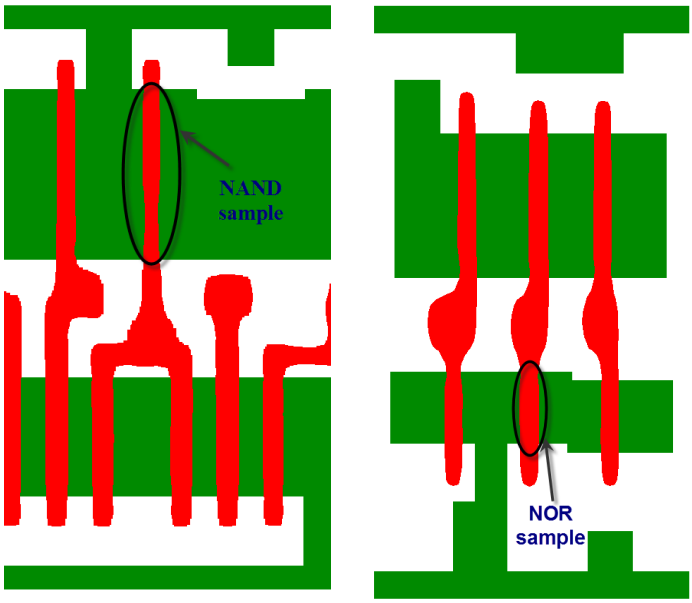


Figure 3-11. Post-lithography images of three-input (a) NAND3 and (b) NOR3.

Table 3-2. I_{on} comparison between TCAD results and the proposed models.

Test cells	**Litho. TCAD (μA)**	Proposed models			
		I_{on} (μA)		Absolute error (%)	
		w/o weighting	w/ weighting	w/o weighting	w/ weighting
NOR3	**288.9**	286.7	289.3	0.76	0.15
NAND3	**301.2**	304.1	301.6	0.97	0.12

respectively. The accuracy can even be improved to be within less than 0.2% by adopting the width-location-dependent factor (W_{eff}). However, a relatively simple model limits the off-current approximation. Therefore, we are going to continue studying the compact shaping modeling method that can be applied to both I_{on} and I_{off} while retaining the fast speed of the PLS and the simplicity of modeling. Furthermore, we intend to study not only gate shape variation but also the diffusion of devices (e.g., source and drain side) together, which are expected to increase the edge effects and thus require precise modeling.

3.2 Diffusion-rounded CMOS for improving both I_{on} and I_{off} characteristics

As semiconductor industries move to aggressive scaling to reduce the area and dynamic power consumption, the channel length has become as short as a few nanometers [17]. Thus imperfect patterning becomes significant not only in the poly gate channel shape but also in the diffusion profile. Many researches have been conducted to model and analyze the transistors' profile in terms of driving current (I_{on}) and leakage current (I_{off}) for post-lithographic simulations [7, 8, 23, 43]. In this work, we propose a novel layout approach to achieve a better driving capability and better leakage property by using imperfect diffusion rounding patterning. TCAD simulations. Analysis have shown that I_{on} and I_{off} characteristics behave differently depending on whether diffusion rounding occurs at the source side or at the drain side of the transistor. Both I_{on} and I_{off} properties become positive when the diffusion rounding happens at the source side. Therefore, the optimized layout provides enhanced device performance, and leakage power saving is made possible simultaneously. In other words, we propose a diffusion-rounded CMOS layout to exploit this positive effect of diffusion rounding at the transistor source side. This work is organized as follows; Chapter 3.2.1 explains electrical properties of diffusion rounding effect in detail, Chapter 3.2.2 investigates the proposed diffusion-rounded CMOS in delay and standby power. Chapter 3.2.3 analyzes several logic families to validate how much benefit we can achieve by employing the proposed diffusion-rounded CMOS. In Chapter 3.2.4, the layout issue of the proposed method is presented, and Chapter 3.2.5 concludes this work.

This work presents a simple and optimized device layout developed by using diffusion rounding effect for better electrical behavior of transistors. TCAD analysis shows that diffusion rounding at the transistor source side can provide increased I_{on} with decreased I_{off} because of the edge effect. The proposed diffusion-rounded CMOS shows as much as 10% improvement in the on-current (driving) and the off-current (leakage) is saved up to 10%. The inverter layout shows that proposed method requires less than a 4% cell area increase for the same driving strength of original cells.

3.2.1 Diffusion rounding effect

To quantify the benefit of diffusion rounding in the electrical characteristics of transistors, TCAD simulations of 45-nm bulk CMOS are conducted. The parameters of nominal devices are calibrated to match the 45-nm predictive models [66]. Table 3-3 lists the I_{on} and I_{off} comparison between nominal devices and diffusion-rounded devices. The source side diffusion rounding shows better property both in I_{on} and I_{off}. In other words, the driving current increases and the leakage current decreases at the same time when the source side diffusion shape rounded. Therefore, we can generate an optimized layout to achieve better I_{on}/I_{off} characteristics by shaping the rounding in the source side. In the conventional CMOS layout, the source side active area is connected to the power supply; V_{DD} for PMOS and GND for NMOS. And the diffusion rounding size depends not only on the manufacturing process but also on

the layout rules such as the gate channel line end extension (LEE) and distance between the gate poly and the active area bending. In the *gpdk45 nm* [67] layout, the design rule of the minimum distance from the poly edge to the diffusion is 50 nm. And the width of the active area (either source or drain) is 140 nm. Therefore, 90 nm width and 45 nm height bending shape to form diffusion rounding can be easily applied.

3.2.2 Electrical properties of diffusion-rounded MOSFET

To introduce diffusion rounding in the source side to improve both I_{on} and I_{off}, a 45-nm active area protrusion is chosen at both sides of the source area. The Sentaurus TCAD setup of NMOS/PMOS is calibrated to the SPICE I_{on}/I_{off} data in 45-nm BPTM [8]. After calibration, the diffusion-rounded NMOS and PMOS are generated by using analytical models which are proposed in [4]. We applied the models by changing width of the transistors for I_{on} and I_{off} to include the diffusion rounding effects. Figure 3-13 shows the proposed layout for NMOS. Table 3-3 shows that a 45-nm diffusion rounding at the source side can increase 10% of driving current (I_{on}), saving up to 10% leakage current (I_{off}). These observations led us to conclude that having diffusion rounding at the source side improves both I_{on} and I_{off} characteristics of the transistors. The effective channel width for the diffusion-rounded device is longer than that of the original device. Therefore, the driving current of the diffusion rounded transistors is greater than that of the original, non-diffusion-rounded transistors [8, 43]. The V_{th} of the device is not

Table 3-3. TCAD simulation results showing the effect of diffusion rounding.

	Length (nm)		**TCAD**		**Normalized**	
NMOS	**source**	**drain**	**I_{on} (μA)**	**I_{off} (nA)**	**I_{on}**	**I_{off}**
rectangular	155	155	**161.73**	**72.56**	**1.00**	**1.00**
source + 45nm	200	155	180.87	68.99	1.12	0.95
source + 90nm	245	155	199.15	65.57	1.23	0.90
drain + 45nm	155	200	175.80	77.61	1.09	1.07
drain + 90nm	155	245	188.91	81.92	1.17	1.13
PMOS	**source**	**drain**	**I_{on} (μA)**	**I_{off} (nA)**	**I_{on}**	**I_{off}**
rectangular	300	300	**184.31**	**67.18**	**1.00**	**1.00**
source + 45nm	345	300	194.40	63.85	1.05	0.95
source + 90nm	390	300	204.64	61.92	1.11	0.92
drain + 45nm	300	345	192.66	68.15	1.05	1.01
drain + 90nm	300	390	201.18	70.77	1.09	1.05

uniform along the channel width, but the V_{th} at the edge of the device is much smaller than that at the center [8]. The effective channel length at the edge of the device is longer for a diffusion-rounded device than that of the original device without diffusion rounding. Therefore, the diffusion-rounded CMOS shows less I_{off} than the original nominal devices. E-field and current density analysis of TCAD also indicate reduced I_{off} and increased I_{on} when we form rounding shape at the source side of the transistors. So it is confirmed that source side diffusion rounding provides higher driving current due the effective channel increment, at the same time, and lower leakage current due to the reduced edge effect and E-field.

3.2.3 Simulation results

Using the analytical diffusion rounding models proposed in [43], we generate the diffusion-rounded NMOS and PMOS by changing effective V_{th}, effective width, and channel length. And HSPICE simulations are conducted for several CMOS logic gates such as the inverter, NAND2, and NOR2 to measure the benefits of diffusion rounding. To investigate circuit level implication of diffusion rounding benefits, the 101-stage ring-oscillators and FO4 delay metrics are used. Figure 3-12 shows the inverter propagation delay result of original CMOS and diffusion-rounded CMOS. The diffusion-rounded

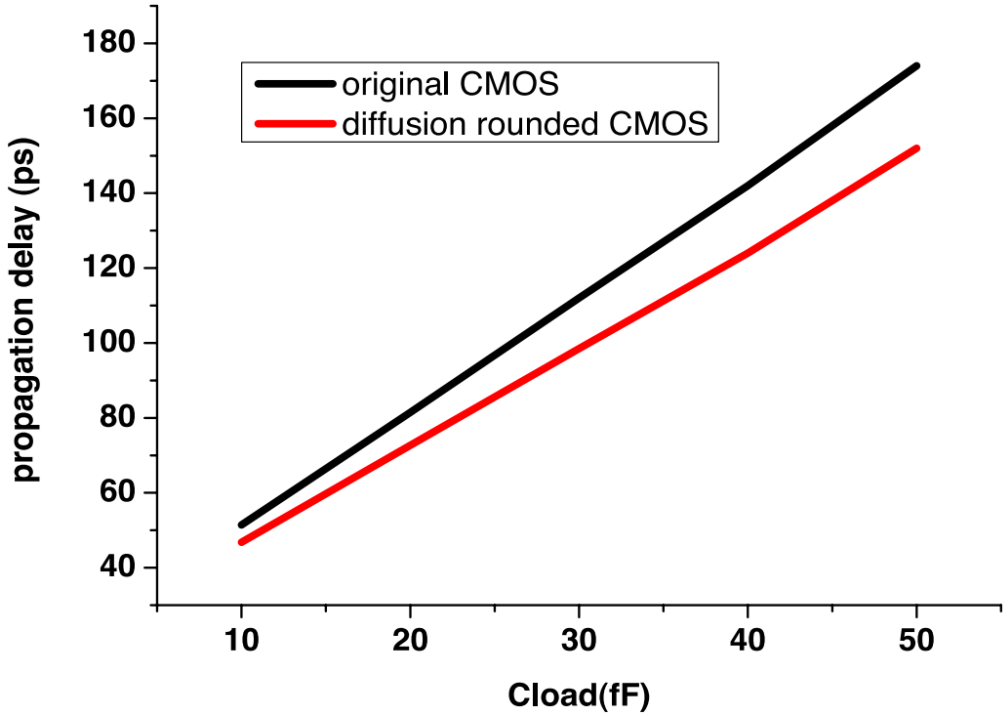
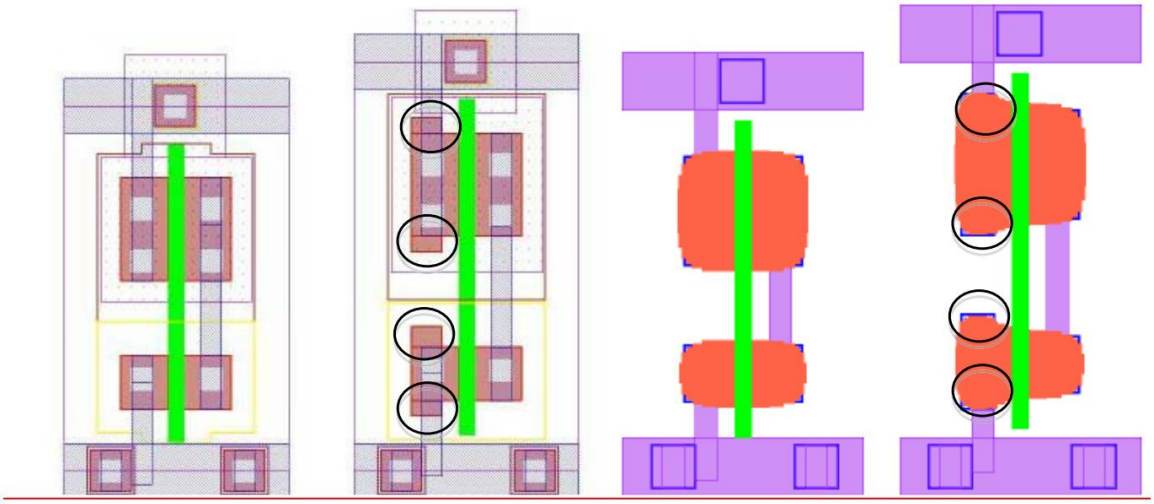


Figure 3-12. Propagation delay improvement with diffusion rounded CMOS.

CMOS inverter represents up to 13% speed up greater than the original CMOS inverter with 50 fF load capacitance. Power simulation shows that the leakage power of the original CMOS is 142 nW and that of the diffusion-rounded CMOS is 127 nW, which is nearly 10% smaller than the original CMOS inverter leakage power.

3.2.4 Layout perspective

To form diffusion-rounded transistors for PMOS and NMOS, the active area layout and thus mask design are modified and the overall cell layout is increased to meet the design rules. Several gate layouts (i.e., INV, NAND2, NOR2) are generated and compared to assess the layout tradeoff by improving electrical property in diffusion-rounded CMOS. The cadence generic 45 nm design package and the layout rules are used for the layouts [67]. Figure 3-13 shows the inverter layout comparison between the original and the diffusion-rounded CMOS. (a) shows the original layout of conventional CMOS and the proposed diffusion rounded one and (b) represents the printed images with OPC in Calibre Workbench [65] simulations. We used the minimum space for all the layers in the GPDK45nm design rule [67]. The minimum distance between the poly edge and the diffusion is 50nm. The 90nm width and 45nm height bending shape is inserted to form the rounding at the source side diffusion. As shown in Figure 3-13(b), the rounding shape at the source side appears with the 193nm wavelength optical lithography. The cell height increases from 1.07 μm to 1.19 μm, which is about 11% in the diffusion-rounded CMOS layout, but we have a better driving strength in the diffusion-rounded CMOS. Therefore,



(a) (b)

Figure 3-13. Inverter layouts of both original and diffusion rounded CMOS; (a) shows layouts and (b) shows the printed image with OPC. Note, black circles indicated the source side bending shape to form diffusion rounding.

we can match the same driving strength by using a smaller channel width in the diffusion-rounded CMOS gates. For the same driving strength, the diffusion-rounded CMOS cell height increases only 50nm that results in less than a 4% cell area increase compared to the conventional CMOS. In addition, as the gate width increases and the logic gates become complicated, the area penalty to form the diffusion rounding shape in the source sides will be minimal. As the minimum feature size of the chip becomes small, the cost for mask generation increases to apply intensive RET techniques including OPC. Thus the complexity and controllability of the proposed design layout might be worse. However, we can apply the proposed diffusion-rounded logics in minimal area where we require either faster transistors to improve overall speed and/or less leaky gates to reduce standby power for specific blocks.

3.2.5 Chapter summary

In this work, we propose a simple layout method to boost the driving strength of logic gates and also to save the leakage power with a minimal area overhead. The proposed method provides up to 13% speed up and also saves up to 10% leakage current in an inverter simulation by exploiting the diffusion rounding phenomena in the transistors. The layout of the diffusion rounded CMOS shows a minimal impact in the cell area compared to the original compact layout. To verify the feasibility and benefit of the diffusion rounding effect on the real wafer, further research and simulations are necessary on the layouts of transistors with different diffusion rounding size and locations.

Chapter 4. Optimization and analysis of process-induced trapezoidal fin of FinFET

4.1 Impacts of trapezoidal fin of 20-nm double-gate FinFET on the electrical characteristics of circuits

In this study, we analyze the impacts of a trapezoidal fin shape on the electrical characteristics of FinFET-based circuits. FinFET structures with angular variations of the sidewalls are exploited in 3D device simulations, and several circuit performance metrics such as the fan-out 4 (FO4) and ring oscillator (RO) delays and cut-off frequency are evaluated with a mixed-mode method (i.e., transient and AC analysis by TCAD) in Sentaurus Device [68] simulations for dynamic performance analysis. The main contributions of our work are summarized as follows:

- We exploit 3D TCAD simulations to analyze the device level effects by various trapezoidal angle variations.
- The device level analysis is extended to the circuit level performance metric by using of mixed-mode simulations.
- The optimum trapezoidal angle ranges in circuit performance are proposed through the combined analysis.

The rest of this study is organized as follows. Chapter 4.1.1 presents the base 3D structure and explains the electrical properties of the trapezoidal FinFET. Impact of angular variation is explained in Chapter 4.1.2. Simulation results of the impact on the circuit performance are discussed in Chapter 4.1.3, followed by conclusions in Chapter 4.1.4.

4.1.1 Trapezoidal FinFET

FinFETs with a rectangular channel shape and a trapezoidal (nonvertical) shape used in this work are shown in Figure 4-1 (a) and (b), respectively. The cross sections through the fin channel (perpendicular to the flow of the current) are shown in Figure 4-1 (c) and (d) for the rectangular and trapezoidal fins, respectively. The rectangular channel shape of the FinFET is used as the base structure. The Sentaurus Structure Editor [68] is used to construct the 3D FinFET structures. As can be observed, the FinFET is created on buried oxide (BOX). The parameters used in the TCAD simulation are shown in Table 4-1. A high-κ metal-gate (HKMG) process is used to construct the gate region. We implemented a thicker top oxide to form double-gate structures. The widths of the upper and lower parts of the fin channel are

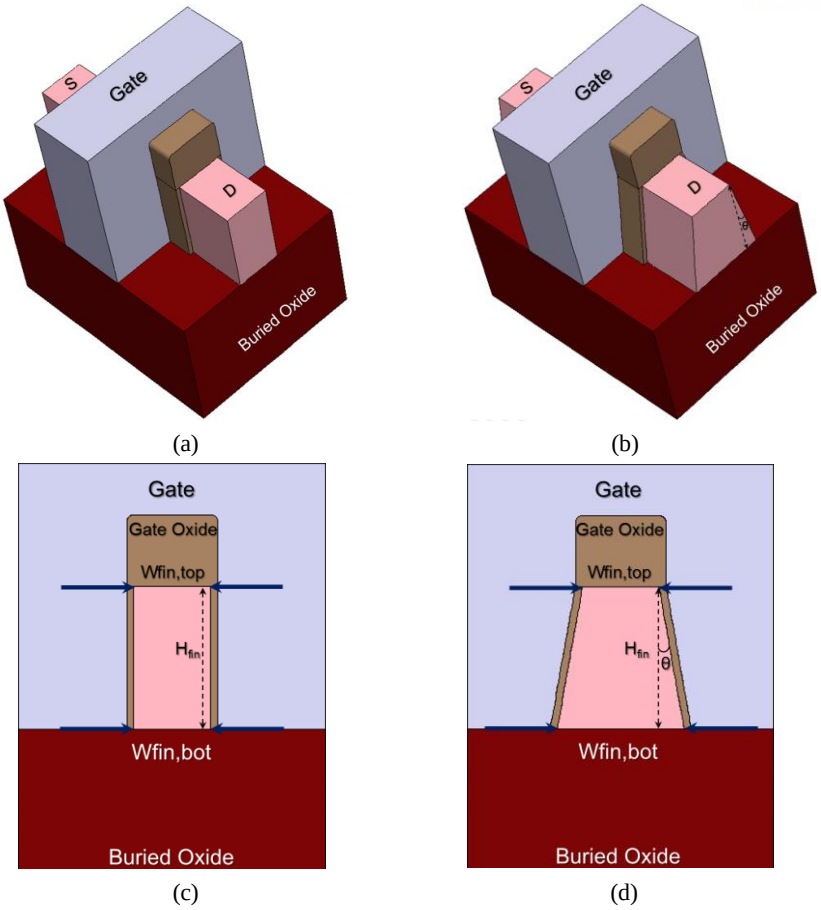


Figure 4-1. Schematic representation of double-gate SOI FinFET (a) rectangular FinFET, (b) trapezoidal FinFET in 3D view, (c) rectangular FinFET, and (d) trapezoidal FinFET in 2D cross-sectional view.

WFin,top and *WFin,bot*, respectively. Although the upper level of the fin is fixed to a constant value (e.g., fin width), the lower level of the fin becomes larger as the angle of the sidewall (θ) increases for generating trapezoidal FinFETs. While keeping the top fin width (*WFin,top*) constant, the inclination angle (θ) of the bottom fin width (*WFin,bot*) in Figure 4-1 (d) is a variable in the cross section geometry in this study. The 20-nm FinFET models [69] are used to calibrate the FinFET parameters. The parameters are based on the level 105.03 of BSIM compact models [70] for bulk FinFET devices. Model data is obtained using HSPICE simulation [71]. A comparison of the calibrated I_D-V_{GS} curve between the TCAD simulation and the models is shown in Figure 4-2, and good agreement is obtained for the TCAD structure. In reality, the post-lithography process of the photoresist (PR) results in a wider PR at the bottom with respect to the top, yielding a trapezoidal shape [72]. The nonideal geometry of the PR is eventually transferred to the fin during the etching process. If we have a constant top fin width and increased sidewall angle, we have a larger effective channel area of the fin, and this in turn causes higher conduction currents than a nominal rectangular area.

Table 4-1. Physical parameters used in the device simulation

Parameters	Value
Channel length (L_g)	23 nm
Height of fin (H_{fin})	28 nm
Width of top fin (*WFin,top*)	15 nm
Gate oxide thickness for top ($T_{ox,top}$)	14 nm
Gate oxide thickness for side ($T_{ox,side}$)	1.4 nm
Channel doping concentration	10^{17} cm^{-3}
Source/Drain doping concentration for NMOS	2.5×10^{19} cm^{-3}
Source/Drain doping concentration for PMOS	2.9×10^{19} cm^{-3}
Supply voltage (V_{DD})	0.9 V
Gate material	Tungsten
Gate oxide material	HfO_2

The electron density profiles in the on- and off-states are shown in Figure 4-3 to compare the electrical properties in both cases of the trapezoidal cross section. Figure 4-3 (a)-(c) show the profiles for the on-state, and (d)-(f) show the off-stage profiles. Figure 4-3 (b) and (e) are the cases with the same area for the on-state and off-state, and (c) and (f) are for the fixed *WFin,top* structures with a 10° angle. Figure 4-4 (a) shows the currents for a fixed-top width, and (b) shows the same-area case. As shown in the plots, the case of the same area for both states Figure 4-4 (b) produces lower conducting currents with

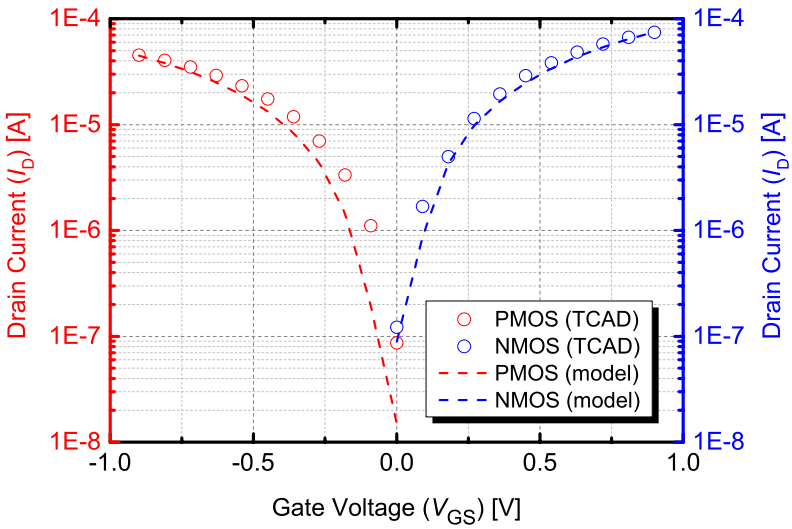


Figure 4-2. Calibrated I_D–V_{GS} curve. The data of a 20-nm FinFET model [14] is used to calibrate parameters for the TCAD simulations.

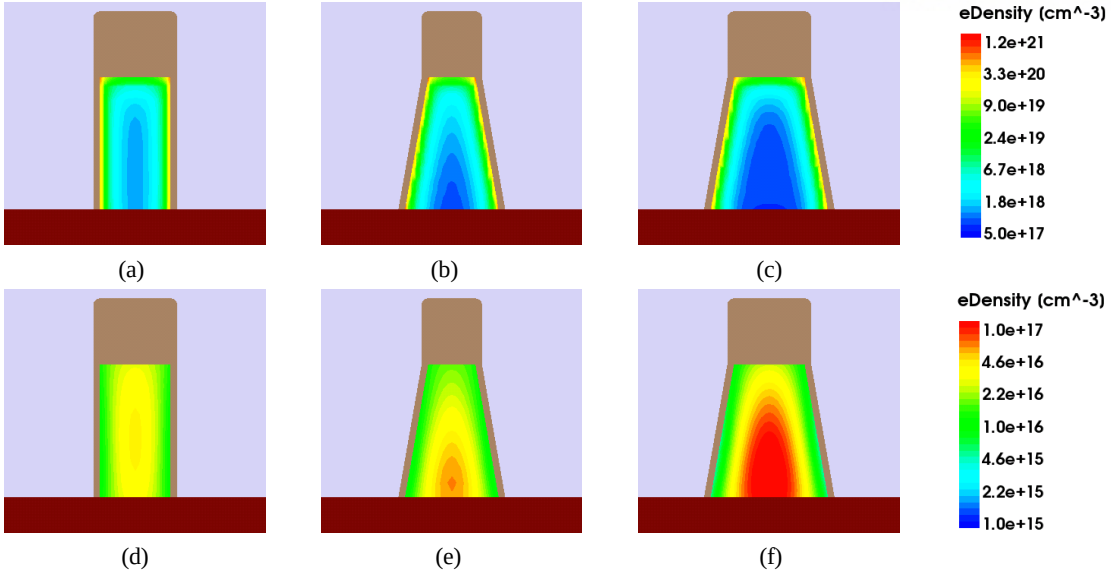


Figure 4-3. Calibrated Electron density profiles of the FinFET. (a)–(c) are for the on-state, and (d)–(f) are for the off-state. (a) and (d) are the nominal rectangular FinFETs, (b) and (e) are the on- and off-current profiles for the case with the same area for both states, and (c) and (f) are for the fixed *WFin,top* structures with a 10° angle. Note the higher current density in the outer fin region in the on-state but in the center in the off-state.

higher leakage currents as the angle increases. However, a FinFET with a fixed top width Figure 4-4 (a) produces higher conducting currents with increased leakage current. Therefore, it is highly probable that the originally desired fin width (W_{fin}) is assumed to be *WFin,top* defined by the photolithography, whereas the bottom of the fin (*WFin,bot*) has a larger thickness because of the technological limitations of the fin definition process (imperfect anisotropic etch) for devices with improved driving strength. As a result, trapezoidal FinFET structures with fixed tops and varying bottom widths are used in this study. Thus, the bottom width of the fin and the length of the fin sidewall are given by (4.1) as follows:

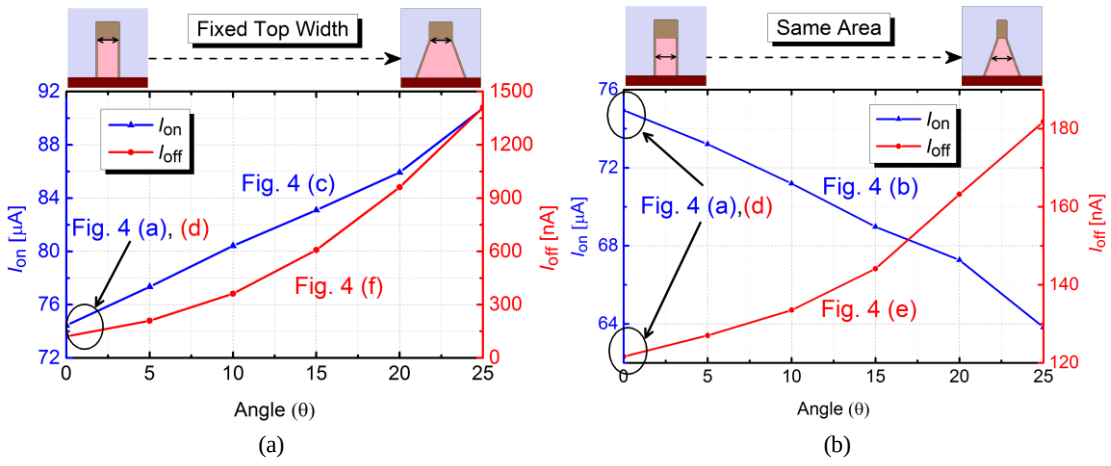


Figure 4-4. I_{on} & I_{off} according to the angle variation of fixed-top and same-area cases are shown in (a) and (b), respectively.

$$WFin,bot = WFin,top + 2 \cdot H_{fin} \cdot \tan\theta$$
$$Fin_{sidewall} = H_{fin} \cdot \frac{1}{\cos\theta} \tag{4.1}$$

A physics-based 3D TCAD simulation is used to analyze the impact of the trapezoidal fin shape in a typical 20-nm process. In the TCAD device simulation, the following models are used to consider the physical characteristics of the narrow-fin FinFET: the doping-induced bandgap narrowing model by Slotboom [73] and Philips unified mobility model [74], high-field mobility saturation [75], Lombardi mobility [76] to consider high-k degradation, and a thin-layer mobility model for accurate prediction of the mobility of the FinFET.

4.1.2 Impact of angle variation

The current compact model for a FinFET for a circuit simulation cannot handle the impacts of a trapezoidal fin shape. In other words, the inclination angle of the fin sidewall cannot be used as the input variable of the circuit simulator directly [69]. Thus, the properties of the trapezoidal FinFET can be analyzed in the TCAD simulations, and the impact on the electrical characteristics such as transient and AC behavior is investigated in mixed-mode simulations. As mentioned in the previous Chapter and shown in Figure 4-4 (a), the effective total channel width ($\approx 2 \times Fin_{\text{sidewall}}$) increases when the inclination angle of the fin height increases. Widening the angle of the fin height creates the possibility of increasing the channel surface area, which leads to a higher on-current. On the other hand, the gate controllability

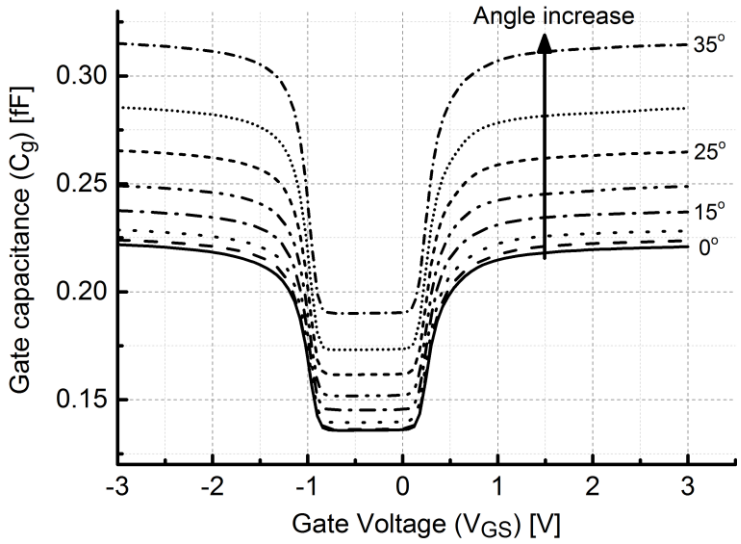


Figure 4-5. A simulated capacitance–voltage curve of the FinFETs with varying angle. Frequency is set to be 1 MHz for simulation. The curves move upward as the angle of the fin increases.

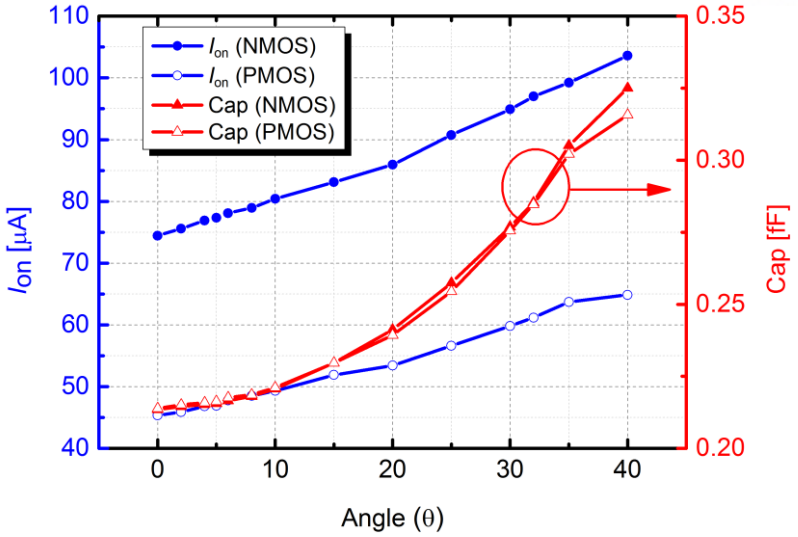


Figure 4-6. The drain current in red (left y-axis) and gate capacitance in blue (right y-axis) of FinFETs according to the inclination angle variation.

Table 4-2. Percentage increase in drive current and gate capacitance associated with Figure 4-6.

	I_{on} (n)	I_{on} (p)	C_g (n)	C_g (p)
0° to 20°	12 %	14%	8%	7%
20° to 40°	25%	25%	42%	37%
0° to 40°	39%	43%	52%	48%

in the channel becomes worse as the angle increases because of a thicker channel width between two side gates around the bottom of the fin, which becomes a penalty for the leakage current as shown in Figure 4-3 (f) and Figure 4-4 (a). Moreover, increasing the angle has a directly increases the gate capacitance because the gate capacitance is proportional to the channel area. In fact, in the case of a rectangular sidewall FinFET, the fin height is optimized for performance between the drive current and capacitance for the same reason as the channel area dependency of the gate capacitance [77]. Capacitance-voltage (*CV*) characteristics of trapezoidal FinFETs are investigated and are shown in Figure 4-5. As can be observed, the total gate capacitance increases as the angle of the fin height increases. The drain current (i.e., on-current or I_{on}) and gate capacitance according to the inclination angle variation are shown in Figure 4-6. The percentage increases are summarized in the table inside the figure. A 0° angle implies a perfectly rectangular FinFET. Note that for an angle up to approximately 20°, the percentage increase in I_{on} and the capacitance are relatively small (e.g., up to 14% for I_{on} and up to 8% for the capacitance). However, for angles greater than 20°, the capacitance increases significantly more than I_{on} (e.g., 42% versus 25% in an n-FinFET). This result indicates that there are

certain ranges of the trapezoidal angles for better dynamic performance than the nominal FinFET.

The delay of the transistor depends on the relationship between the driving current strength (I), the gate capacitance (C), and the supplied voltage of operation (V). The intrinsic delay (τ) of a conventional transistor is given by

$$\tau = \frac{C \cdot V}{I} \tag{4.2}$$

Thus, both I_{on} and the capacitance affect the dynamic performance of the circuits. In addition, there is a tradeoff between the two characteristics in the trapezoidal FinFET. As the inclination angle is varied in the fin sidewall according to the trapezoidal FinFET shape, the delay of the FinFET increases or decreases according to the relative percentage changes in the capacitance and drive current. Therefore, when the angle exceeds 20°, the benefit of having a larger current in the delay disappears because of the greater capacitance increase. In the following Chapter 4.1.3, several benchmark circuits are exploited in the mixed-mode simulations to investigate the impact of the trapezoidal angle on the circuit performance.

4.1.3 Impact on circuit performance

As explained in the previous Chapter 4.1.2, there is a trade-off between the driving current and the gate capacitance (and leakage current as well) as the trapezoidal angle increases. In other words, when the bottom of the fin width increases (i.e., wider inclination angle), the driving current increases, but the leakage current (and dynamic power) and gate capacitance increase simultaneously. However, their relative impacts on the dynamic characteristic of the circuit are different in various performance metrics.

In order to verify the impact of the trapezoidal FinFET on the circuit level quantitatively, four circuit examples are considered in the Sentaurus Device mixed-mode simulations as performance metrics, as depicted in Figure 4-7: a single inverter with a fixed loading cap, a fan-out 4 inverter, and a five-stage ring oscillator. In addition, the cut-off frequency (f_T) is measured in the AC simulation to investigate the impact of the trapezoidal FinFET on analog applications. The simulation results for the delays of the FO4 inverter and five-stage RO are shown in Figure 4-8. As expected, the propagation delays of the trapezoidal FinFETs always decrease (or faster) as the angle increases in the fixed loading capacitor case in Figure 4-8 (a) with penalty on the leakage power. In this study, the increased angle of the fin enables a larger area for the conduction channel because *WFin,bot* is assumed to have a larger thickness than the nominal thickness, and this, in turn, causes higher conduction currents. Therefore, the circuits

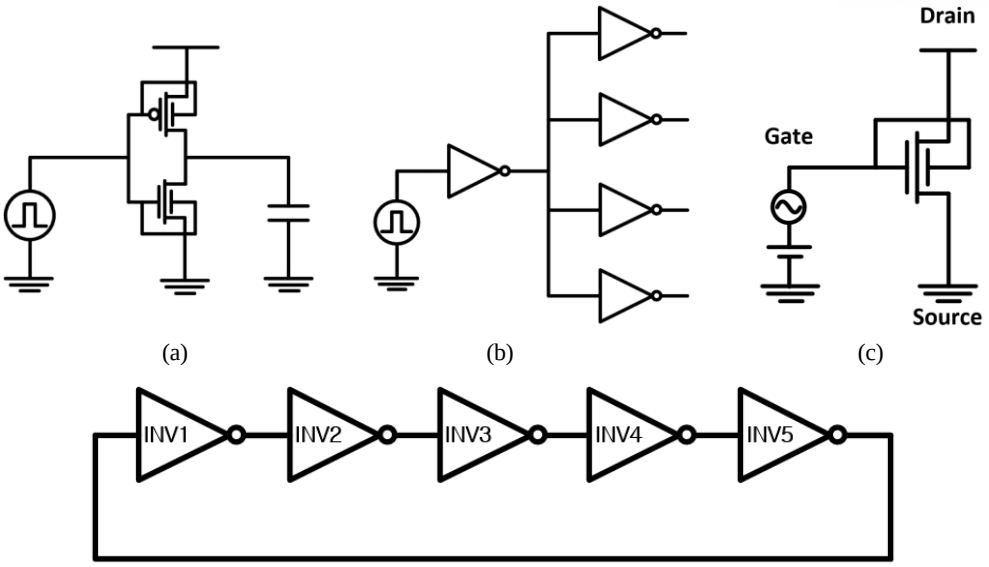


Figure 4-7. Schematics used in Sentaurus device mixed-mode simulations. (a) Inverter with fixed loading capacitance, (b) FO4 inverter, (c) NMOS for AC simulation, and (d) 5-stage ring oscillators.

in the trapezoidal FinFET with a fixed loading capacitor have a shorter delay than the nominal delay (i.e., 0°).

On the other hand, interesting results are observed for the FO4 inverter (Figure 4-8 (b)) and five-stage RO (Figure 4-8 (c)). The delays decrease up to some angle (e.g., 15° for the FO4 inverter and 10° for the RO) and increase for large r angles. In this case, as mentioned in Chapter 4.1.2, the penalty associated with an increase in the capacitance becomes larger for significantly larger angles and the ratio of the capacitance increase is similar to the ratio of driving current increase up to 20°. The impact on the oscillating frequency variations of ring oscillator at the output node (INV3) produced by the angle variations is shown in Figure 4-8 (c). As shown, the RO generates a higher frequency as the angle increases, and the maximum frequency occurs at 10° for the trapezoidal FinFET. However, the increased gate capacitance dominates from 20° by reducing the oscillating frequency than the optimum angle (e.g., 10° or 15°). The transient response of the RO in Figure 4-9 clearly shows the behavior of the frequency according to the angle. As the figure of merit for RF performance, f_T is observed to understand the device behavior for analog applications. f_T is extracted when the current gain is unity at the proper bias for trapezoidal NMOS FinFETs with various angles. As shown in Figure 4-8 (d), a smaller cut-off frequency is obtained as the trapezoidal angle of the FinFET increases owing to the larger capacitance effect, as observed from the following equation:

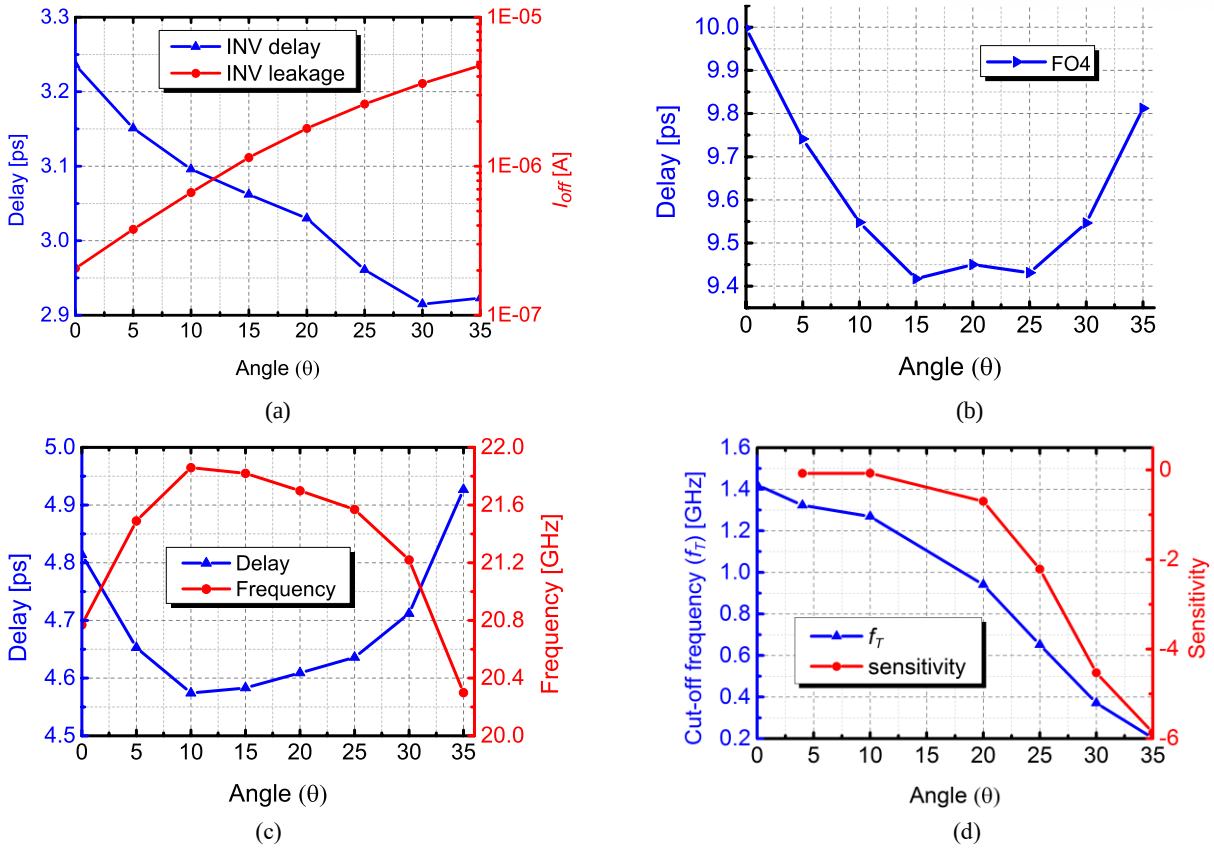


Figure 4-8. Impact on the performance according to inclination angle variation. (a) Inverter with fixed loading capacitance, (b) FO4 inverter, (c) ring oscillators, and (d) cut-off frequency.

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{4.3}$$

The gate-source (C_{gs}) and gate-drain (C_{gd}) capacitance components are proportional to the effective width of the device, and the effective width increases as the angle increases. Thus, even though a larger transconductance, g_m, is realized by the trapezoidal FinFET, the higher capacitance degrades f_T. We adopt the dimensionless derivatives of the cut-off frequency with respect to the inclination angle (θ) and their ratios as follows [78]:

$$f_{T\_\theta} = \frac{\theta}{f_T}\frac{\partial f_T}{\partial \theta} \tag{4.4}$$

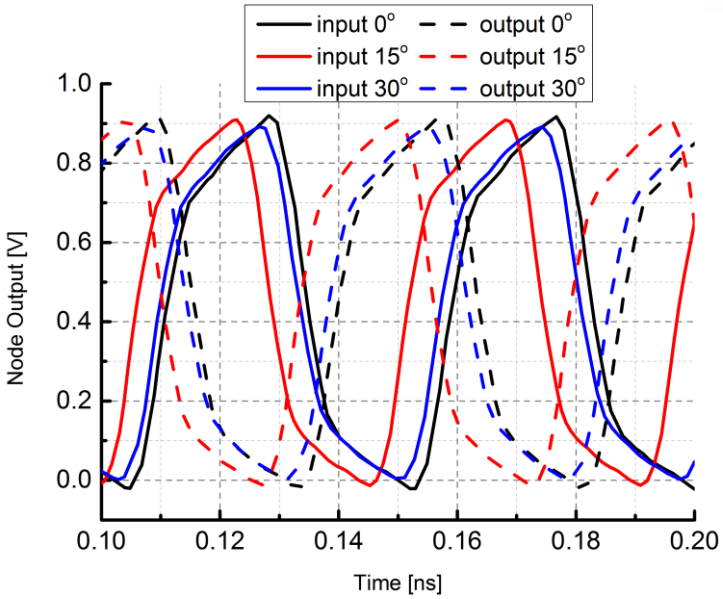


Figure 4-9. The node output (inv3) variations produced by the angle variations. The output is the third stage node output in the 5-stage ring oscillator.

The relative sensitivity according to the angle variation, f_{T_θ}, is shown in Figure 4-8 (d). As shown, f_T is weakly sensitive to the angle up to 20° but degrades significantly above 20°. This result agrees with the dominant effect of the capacitance for larger angles (e.g., $\theta \geq 20°$).

4.1.4 Chapter summary

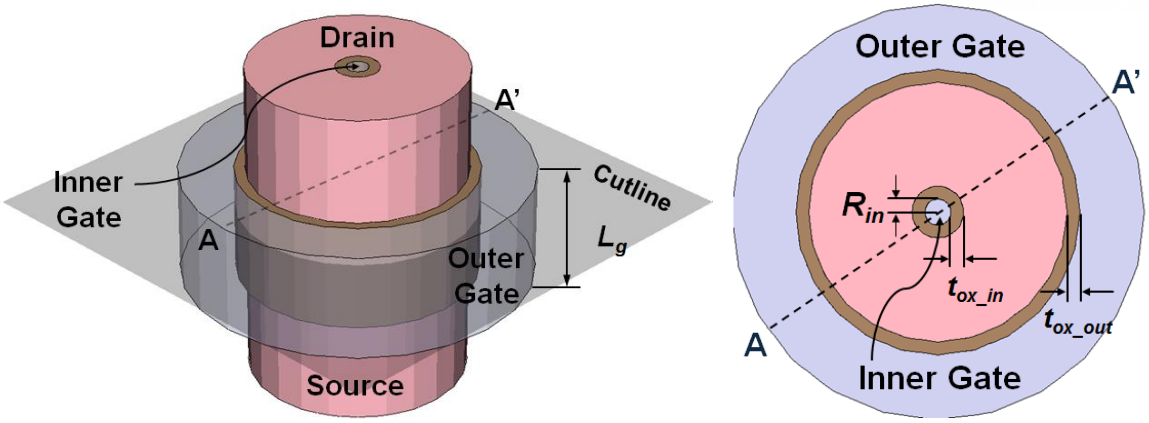
In this study, the performance impact of the trapezoidal fin shape of a double-gate FinFET is analyzed with numerous TCAD simulations. Several performance metrics are evaluated to investigate the impact of the trapezoidal fin shape on the circuit operation. The TCAD simulations show that the driving capability improves, and the gate capacitance increases as the bottom fin width of the trapezoidal fin increases. The trapezoidal FinFET with a fixed loading capacitance validates the increase in the driving current. However, the increase in the gate capacitance nullifies the benefit of the current increase due to the trapezoidal fin at larger angle. The FO4 inverter and RO delay results indicate that careful optimization of the trapezoidal angle can increase the speed of the circuit because the ratios of the current and capacitance have different impacts depending on the trapezoidal angle. f_T is observed to understand the device behavior at high frequencies. The impact of the trapezoidal FinFET on the cut-off frequency correlates well with the observations from the driving current and capacitance. As a result, careful control of the trapezoidal angle in the FinFET devices will be beneficial to circuit performance.

Chapter 5. Optimization of DGAA FET with process-induced asymmetric channel width

5.1 Optimal inverter logic gate using 10-nm double gate-all-around (DGAA) transistor with asymmetric channel width

We investigate the electrical characteristics of a double-gate-all-around (DGAA) transistor with an asymmetric channel width using three-dimensional device simulation. The DGAA structure creates a silicon nanotube field-effect transistor (NTFET) with a core-shell gate architecture, which can solve the problem of loss of gate controllability of the channel and provides improved short-channel behavior. The channel width asymmetry is analyzed on both sides of the terminals of the transistors, i.e., source and drain. In addition, we consider both *n*-type and *p*-type DGAA FETs, which are essential to forming a unit logic cell, the inverter. Simulation results reveal that, according to the carrier types, the location of the asymmetry has a different effect on the electrical properties of the devices. Thus, we propose the *n*/*p* DGAA FET structure with an asymmetric channel width to form the optimal inverter. Various electrical metrics are analyzed to investigate the benefits of the optimal inverter structure over the conventional inverter structure. Simulation results show that 27% delay and 15% leakage power improvement are enabled in the optimum structure.

The scaling limits of CMOS technology make it difficult to follow Moore's law, which would require novel device structures to increase gate controllability and suppress short channel effects (SCEs). Beyond the 10-nm technology node, the gate-all-around (GAA) FET is the natural evolution of multi-gate architectures and is considered to be a promising solution for continuing Moore's law [13]. However, contrary to general expectations, it was found that a conventional top-down process produces asymmetric channel structures rather than symmetric cylindrical shapes in the GAA structure [11]. The electrical properties of vertical silicon nanowire structures with an asymmetric channel width have been investigated in previous studies [53, 56]. However, only *n*-type transistors were analyzed in these studies and the effective channel area was not considered. In this case, it is difficult to determine whether the performance differences in comparison targets are caused by structural differences (i.e., asymmetry) or by effective area. To the best of our knowledge, the concept of the DGAA FET was first introduced in 2011; the device was an *n*-type nanotube FET [79]. A *p*-type DGAA nanotube FET was compared to the nanowire FET architecture in the following year [80]. In this study, we consider not only the asymmetry of the channel width at the source and drain sides but also two carrier types (i.e., *n* and *p*) in the DGAA FET. Then, analysis of the asymmetry in the channel width can provide the optimal



(a) (b)

Figure 5-1. DGAA FET structure used in device simulations in (a) bird's eye view and (b) cross-sectional view.

structures of the *n*- and *p*-type DGAA FETs to form a basic logic gate, the inverter. We investigate the electrical characteristics of the DGAA transistor with an asymmetric channel width using three-dimensional technology computer-aided design (3D TCAD) device simulation [68].

5.1.1 DGAA with asymmetric channel width

The nominal 3D device structure used in this study is shown in Figure 5-1. The DGAA has two gate terminals, inner and outer gate, and the gates can either be tied together to enhance device performance

Table 5-1. Physical parameters used in the device simulations.

Parameters	Value
Channel length (L_g)	10 nm
Inner gate oxide thickness (t_{ox_in})	1 nm
Outer gate oxide thickness (t_{ox_out})	1 nm
Radius of the inner gate electrode (R_{in})	1 nm
Radius of silicon channel (R_{ch})	10 nm
Channel doping concentration	1×10^{16} cm^{-3}
Source/Drain concentration	2×10^{19} cm^{-3}
Supply voltage (V_{DD})	0.75 V
Gate material	Tungsten
Gate oxide material	HfO_2
Workfunction (*n*-type)	4.5 eV
Workfunction (*p*-type)	4.8 eV

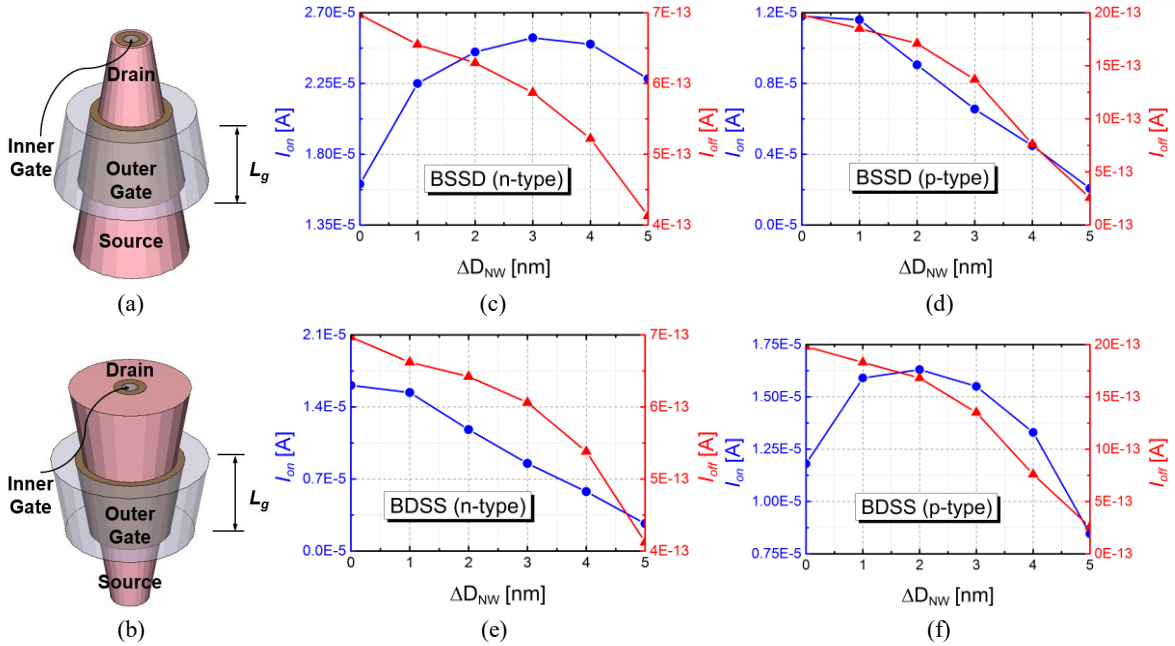


Figure 5-2. DGAA FET structure used in device simulations and simulation results. Structures of (a) BSSD (big-source small-drain), (b) BDSS (big-drain small-source), simulation results of (c) *n*-type BSSD, (d) *n*-type BDSS, (e) *p*-type BSSD, and (f) *p*-type BDSS.

or be controlled independently for threshold voltage (V_{th}) modulation and leakage minimization. The nominal physical parameters used in the device simulations are summarized in Table 5-1. The channel length (L_g) is 10 nm. Both inner and outer gate oxide thicknesses (t_{ox}) are set to 1 nm. The radius of the silicon channel is 10 nm. The channel region is lightly doped with 1×10^{16} cm^{-3} boron (for *n*FET) or arsenic (for *p*FET) to reduce random dopant fluctuation (RDF) effects and avoid mobility degradation. The source/drain are doped with 2×10^{19} cm^{-3} arsenic and boron for n-type and p-type, respectively. A high-κ metal-gate (HKMG) process, using tungsten and HfO_2 as gate electrode and gate dielectric, respectively, is used to construct the gate region. The supply voltage is set to 0.75 V, according to the ITRS roadmap [81]. TCAD Sentaurus Device software [68] is used to perform device simulations. Two types of channel width variation in the DGAA structure are investigated, as shown in Figure 5-2, (a) big-source small-drain (BSSD) and (b) big-drain small-source (BDSS). The variations in the diameters of the top and bottom of the nanotube are of the same value but have opposite sign; thus, the silicon channel maintains the same area with a nominally cylindrical channel so as to ensure the effective channel area.

5.1.2 Impact of asymmetry on device performance

As shown in Figure 5-2(c)-(f), variations in source- and drain-side parameters have different effects on

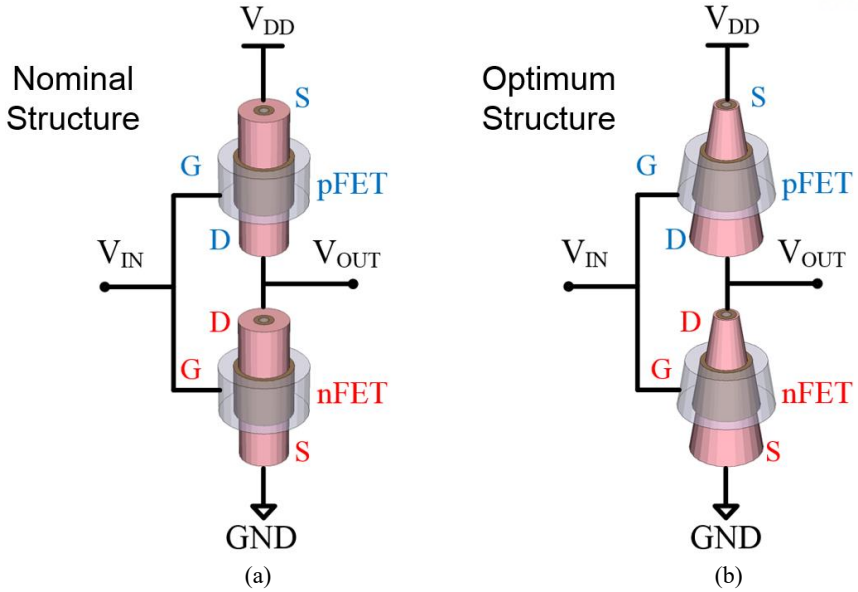


Figure 5-3. Circuit schematics of vertical Si DGAA FET-based inverter for (a) nominal structure and (b) optimal structure.

the electrical properties. In *n*-type FETs (NMOS), the static leakage current, I_{off} becomes better (less leaky) in both structures as the diameter variation increases and the driving current, Ion, improves only when the source side becomes wider (i.e., in BSSD) but degrades at a smaller source side diameter (i.e., in BDSS); Ion increases up to D_{NW} = 3 nm when the source side becomes wider. On the other hand, I_{on} of a *p*-type FET (PMOS) has the opposite trend because of the asymmetry of the source and drain; I_{on}

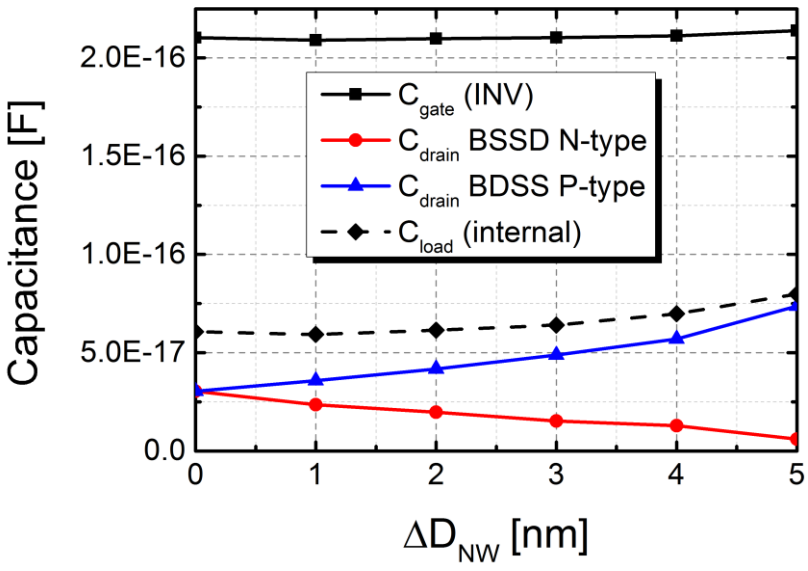


Figure 5-4. Capacitance of the asymmetric DGAA inverter.

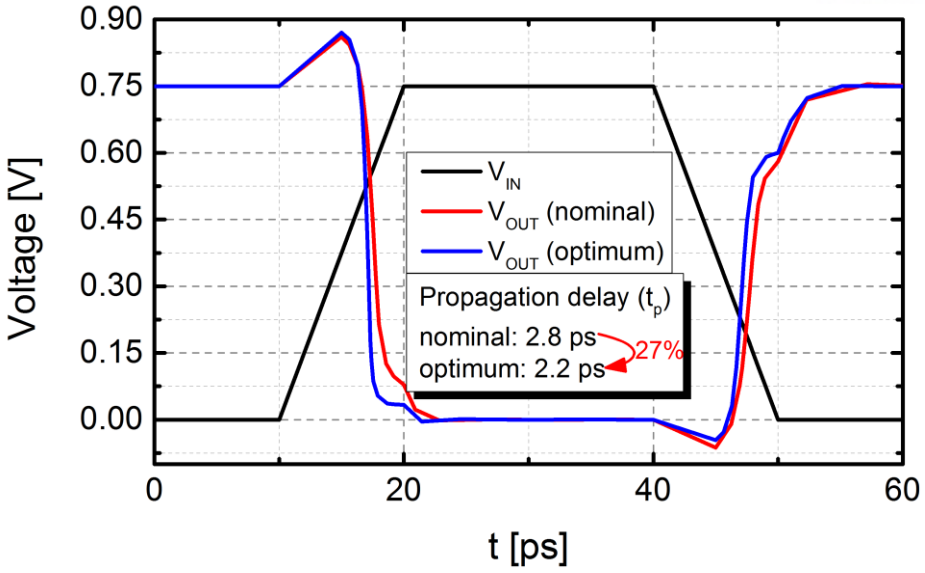


Figure 5-5. Transient simulation of DGAA inverter.

increases up to D_{NW} = 2 nm when the drain side becomes wider and I_{off} has the same trends. As a result, the BSSD structure shown in Figure 5-2(a) is expected to be a preferable structure for the NMOS and BDSS structure shown in Figure 5-2(b) for PMOS in terms of providing greater ability to drive current and maintain a lower off-state current. This finding leads us to propose an optimal complimentary metal-oxide-semiconductor (CMOS) logic gate, i.e., an inverter, by combining BSSD NMOS and BDSS PMOS, as schematically depicted in Figure 5-3.

5.1.3 Impact of asymmetry on circuit performance

To analyze the electrical characteristics of the optimal inverter using the asymmetric DGAA, several circuit-level metrics are investigated: propagation delay, dynamic power, leakage power, and ring oscillator (RO) frequency. The capacitance of the asymmetric DGAA inverter is shown in Figure 5-4. As the asymmetry increases, the drain capacitance of the BSSD *n*-type device decreases and the drain capacitance of the BDSS *p*-type device increases. Thus, the total gate capacitance (C_{gate}) and internal loading capacitance (C_{load} (internal)), which behave as a total loading component when the inverter is driving itself, are not significantly increased. Therefore, from the dynamic point of view, the impact of asymmetry on the capacitance of the inverter will be small. The propagation delay of the logic gate is a function of the capacitance and the current flowing through the transistor. As shown in the previous results, 58% and 38% larger currents flow, for NMOS and PMOS, respectively, for the optimal inverter relative to the nominal inverter. Additionally, because the device maintains the same channel area, there is a negligible discrepancy in the gate capacitance between optimal and nominal devices. Therefore,

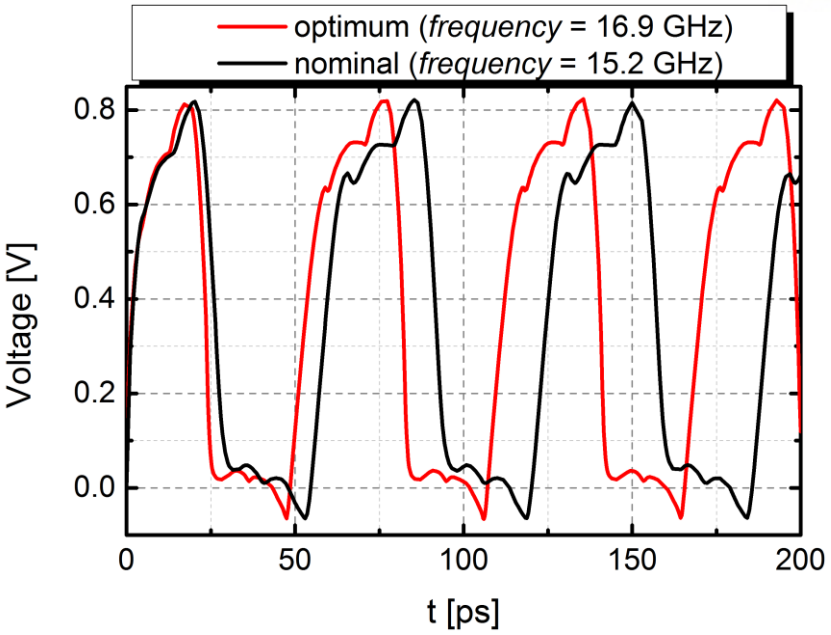


Figure 5-6. Transient simulation of DGAA-based five-stage ring oscillator.

transient simulations of the DGAA inverter show that the optimal structure is 27% faster than the nominal structure, as shown in Figure 5-5. In addition, the static leakage current of the DGAA inverter is 15% smaller than the nominal inverter (e.g., 1.34 pA for the nominal structure and 1.13 pA for the optimal structure). To quantitatively evaluate the impact of the asymmetric DGAA FET at the circuit level, a five-stage RO is considered in the Sentaurus Device mixed-mode simulations as performance metrics to investigate the frequency and dynamic behavior of the proposed structure. The outputs of the DGAA-based five-stage RO for both the nominal and the optimal inverter are shown in Figure 5-6. The signal oscillating through the RO chain is determined by each inverter stage; the RO composed of optimal inverters has a higher speed of signal transition. As expected, for the RO using optimal inverters, the signal oscillating frequency is improved by 11% (from 15.2 GHz to 16.9 GHz) consuming approximately 5% (9.3 μW vs. 9.8 μW) more dynamic power.

5.1.4 Chapter summary

In this study, the asymmetry of the DGAA channel width is analyzed; the source- and drain side asymmetry produces different electrical properties. The BSSD structure is expected to be preferable for NMOS devices, whereas the BDSS structure is expected to be preferable for PMOS devices, providing a greater ability to drive current and maintaining a lower off-current. Novel device structures are proposed to form the optimal inverter. Several electrical metrics are used to analyze the characteristics of the optimal inverter. The optimal inverter provides 27% faster propagation delay with 15% less leakage power than the nominal structure since the optimal amount of variation is carefully chosen in

the device analysis. RO simulation indicates that an 11% faster oscillating frequency (with a relatively small penalty in terms of dynamic power) can be achieved when using the optimal inverters. In a perspective of fabrication process, however, controlling the amount of variation to form asymmetric DGAA transistors may be challenging. If the amount of variation can be precisely controlled with advanced technology in near future, this work has significant meaning in DGAA-based circuit designs.

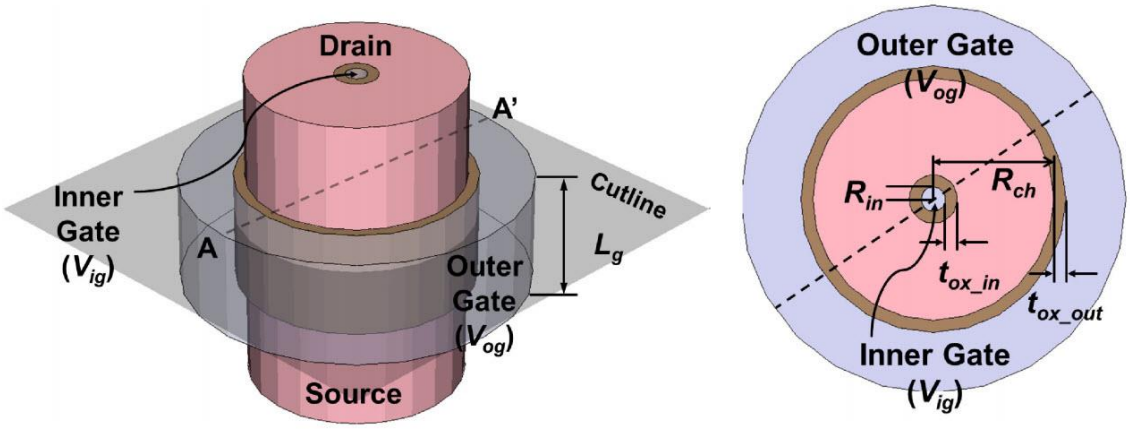
5.2 On-chip interconnect boosting technique by using of 10-nm double gate-all-around (DGAA) transistor

In this work, application of DGAA transistor to on chip interconnect boosting was proposed firstly. This work proposes a boosting structure that can significantly improve the performance of circuits by controlling the two gates of the DGAA independently. Circuit designers cannot change the V_{th} value of the device because V_{th} is set by channel doping (the traditional way) or the applicable gate workfunction. However, the threshold voltage of the transistor can be modulated by controlling the separated gate terminal. Using the independent-GAA (IGAA) scheme in circuit design, designers can control the V_{th} value of the device, which provides more design options.

As the technology scales down, the obtained gain of active devices degrades because of an increase of interconnect propagation delays. Thus, more concerns arise for especially long interconnects [82]. Repeaters, which divide a long interconnect into shorter sections, have been proposed and have successfully resolved the problems by improving the interconnect delay [83-87]. However, repeaters generate other problems: finding the optimal number and size of the repeaters has been nontrivial and additional power and area is required. In this study, a novel methodology to boost the signal propagation speed in repeaters using IGAA transistors in which the bias of each gate is controlled separately to obtain significantly better circuit performance is proposed and analyzed. This study is organized as follows. Chapter 5.2.1 explains the 3D TCAD structure and the properties of the DGAA. The proposed boosting techniques are presented in Chapter 5.2.2. Simulation results regarding performance and power consumption are discussed in Chapter 5.2.3, followed by conclusions in Chapter 5.2.4.

5.2.1 Double gate-all-around (DGAA) transistor

The 3D TCAD structure used in this study is shown in Figure 5-7. The nominal physical parameters



(a) (b)

Figure 5-7. DGAA FET structure used in device simulations in (a) bird's eye view and (b) cross-sectional view.

Table 5-2. Physical parameters used in the device simulations.

Parameters	Value
Channel length (L_g)	10 nm
Inner gate oxide thickness (t_{ox_in})	1 nm
Outer gate oxide thickness (t_{ox_out})	1 nm
Radius of the inner gate electrode (R_{in})	1 nm
Radius of silicon channel (R_{ch})	10 nm
Channel doping concentration	1×10^{16} cm^{-3}
Source/Drain concentration	2×10^{19} cm^{-3}
Supply voltage (V_{DD})	0.75 V
Gate material	Tungsten
Gate oxide material	HfO_2
Workfunction (*n*-type)	4.5 eV
Workfunction (*p*-type)	4.8 eV

used in the device simulations are summarized in Table 5-2. The channel length (L_g) is 10 nm and (both inner and outer) gate oxide thickness (t_{ox}) is set to 1 nm. The radius of the silicon channel is 10 nm. The channel region is lightly doped at 1×10^{16} cm^{-3} (boron for *n*-type FET and arsenic for *p*-type FET) to reduce RDF effects and avoid mobility degradation [88], and the source/drain region is doped at

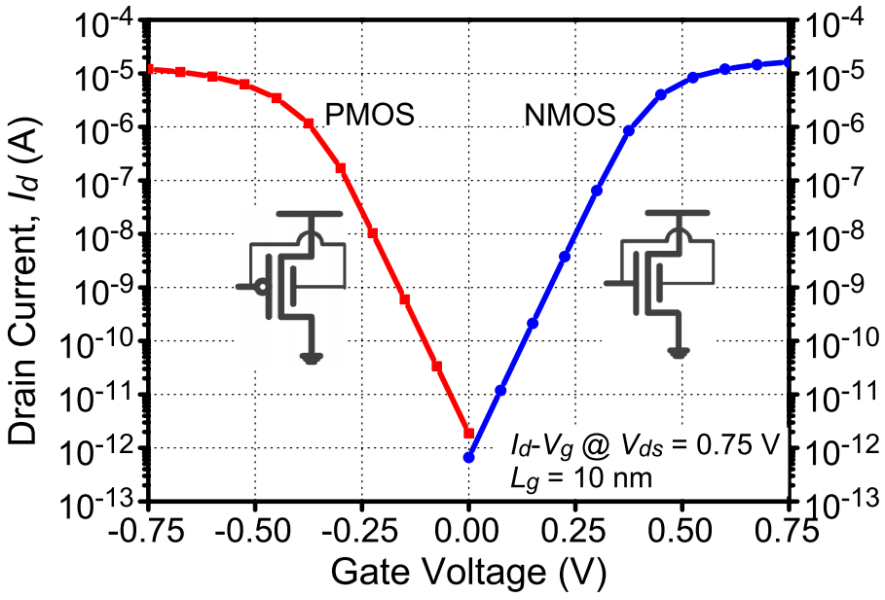
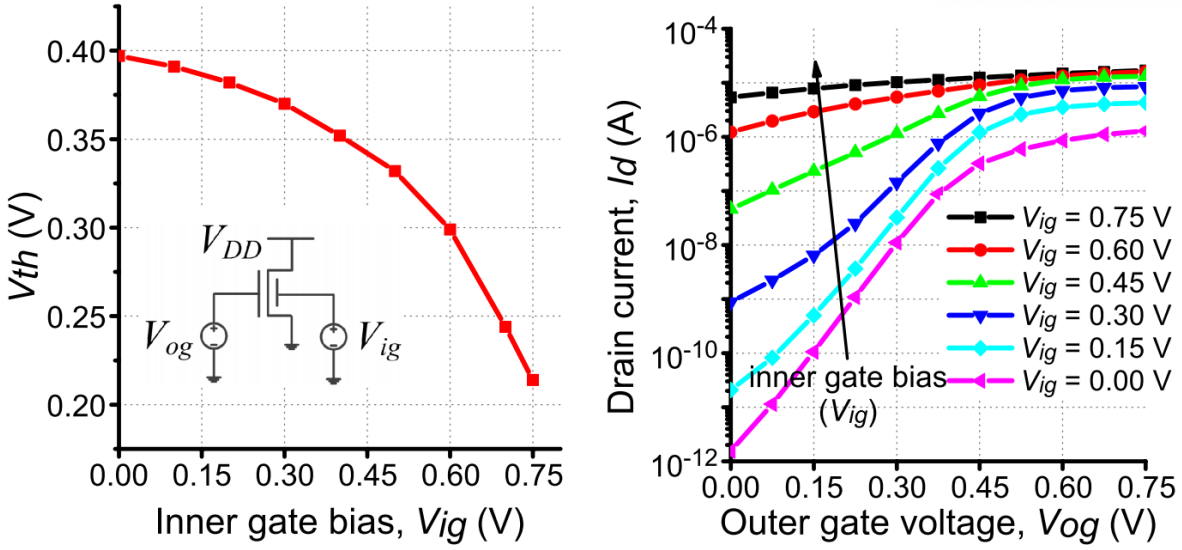


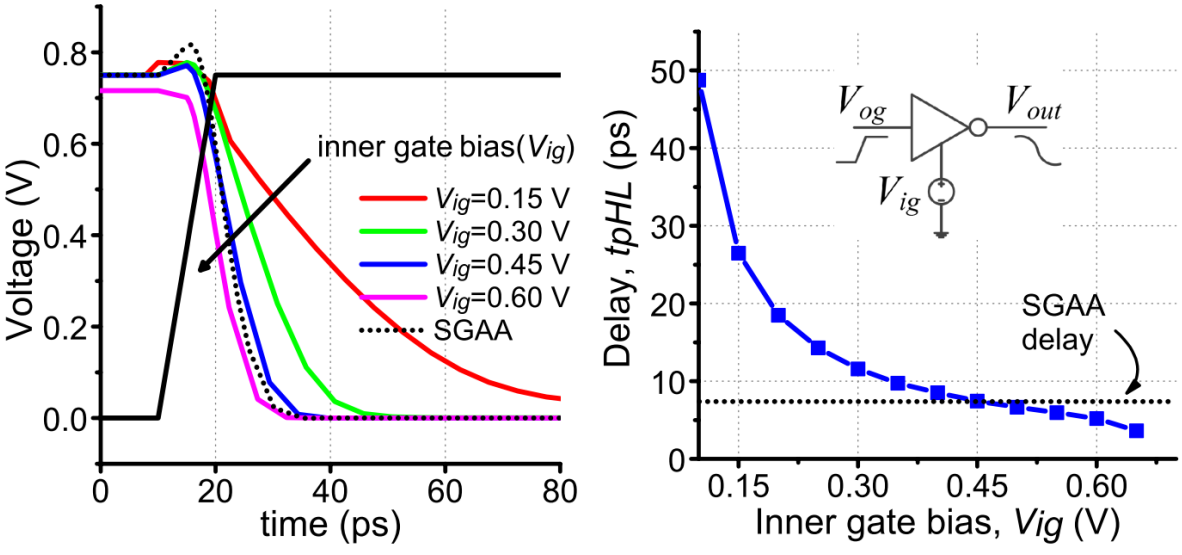
Figure 5-8. *I-V* characteristics of the GAA NMOS and PMOS devices used in this study. The schematics used in the simulations are shown in the figure.



(a) (b)

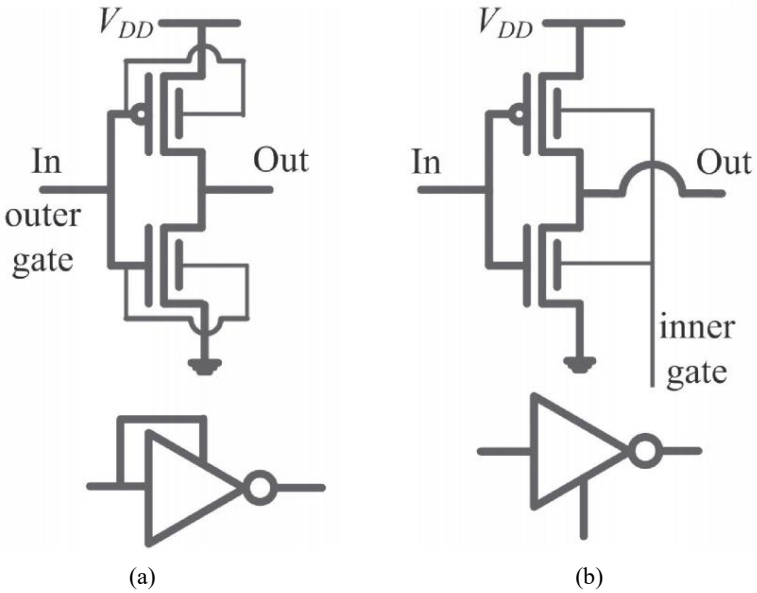
Figure 5-9. (a) Threshold voltage modulation by introducing additional inner gate bias and (b) drain current vs. outer gate voltage for various inner gate bias values. The test circuit used in the simulations is shown in the figure.

2×10^{19} cm^{-3} (arsenic for *n*-type FET and boron for *p*-type FET). A high-κ metal-gate (HKMG) process, with tungsten and HfO_2 as a gate electrode and a gate dielectric, respectively, is used to construct the gate region. The workfunctions for NMOS and PMOS are calibrated to maintain a sufficiently high I_{on} / I_{off} ratio [89-91]. The I_d-V_g curves of both transistors in shorted-gate mode (i.e., SGAA) at V_{ds} = V_{DD} are plotted in Figure 5-8. The supply voltage is set to 0.75 V according to the ITRS (International



(a) (b)

Figure 5-10. (a) Transient graph of one IGAA inverter simulated at various inner gate bias values and (b) delay vs. inner gate voltage. The SGAA delay is also plotted as a reference. The circuit for the simulations is shown in the figure.



(a) (b)

Figure 5-11. Schematic and symbol of inverter using (a) SGAA and (b) IGAA.

Technology Roadmap for Semiconductors) for 10-nm gate length [81]. The TCAD software, Sentaurus Device [68], is used to perform device-level and mixed-mode (e.g., transient) simulations. The gate voltage is applied to create a conductive channel between the source and drain to allow current to flow in the transistor. In this study, V_{th} is set by the metal-semiconductor workfunction difference. When the inner gate and outer gate terminal are tied together and biased equally, they function together to induce a conductive channel. However, when the inner gate is biased differently from the outer gate, the metal-semiconductor workfunction will differ between the vicinity of the inner gate and outer gate region. In

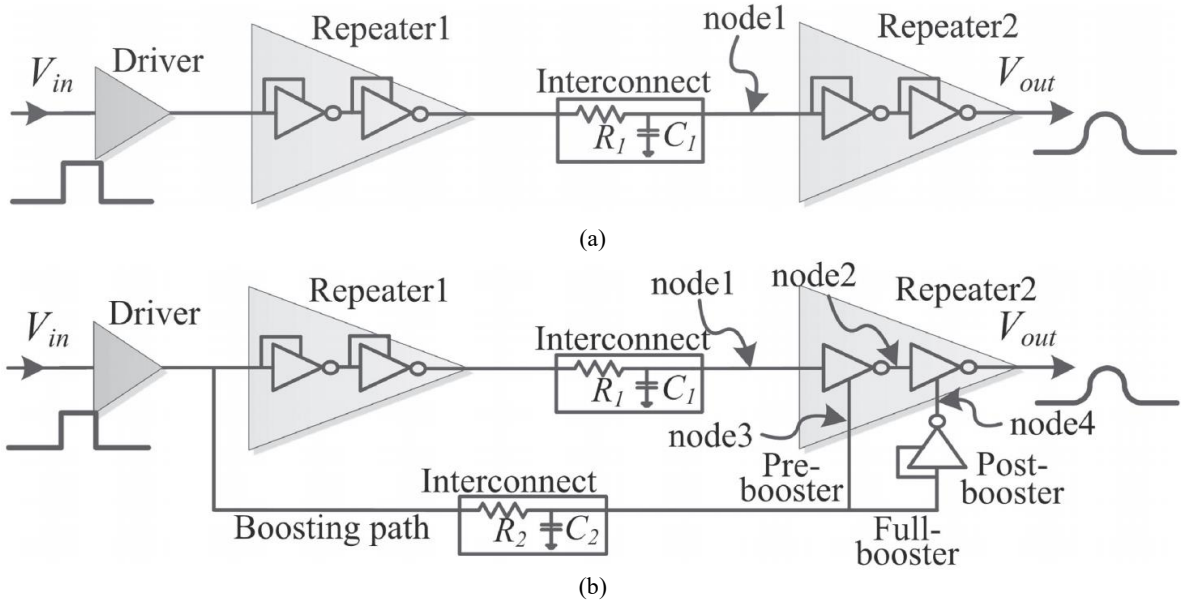


Figure 5-12. Architecture of two repeaters in (a) the nominal case and (b) the proposed boosting technique.

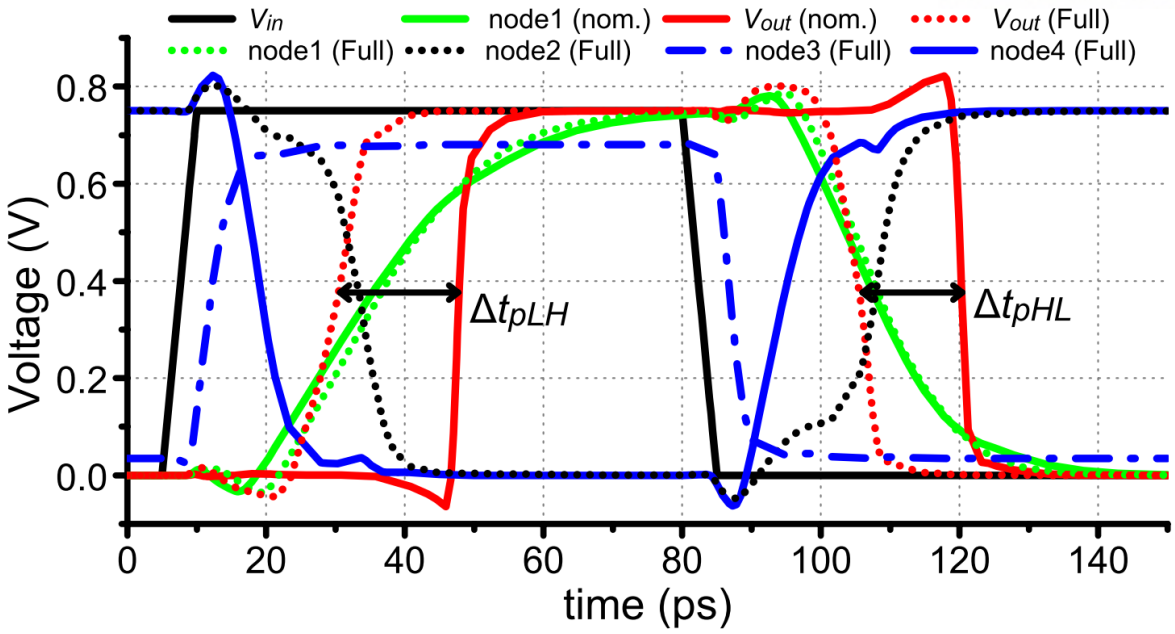


Figure 5-13. Transient graph of nominal case and full-booster.

other words, V_{th} modulation can happen by separating the two gates using IGAA methods. Figure 5-9 (a) represents the threshold voltage for different inner gate bias (V_{ig}) values in the IGAA FET. As shown, the Vth value falls from 0.397 V to 0.214 V when V_{ig} rises from 0 V to 0.75 V. The dynamic threshold voltage change in the IGAA transistors can provide additional options for circuit designers in terms of performance and power optimization according to the requirements of the integrated circuits. Figure 5-9 (b) shows the drain current (I_d) while increasing the inner gate voltage (V_{ig} in the n-type IGAA). As seen in the figure, the drain current increases dramatically when increasing the outer gate voltage V_{og} when V_{og} remains lower than the threshold voltage (e.g., $\leq$ 0.4 V). This phenomenon indicates that even though there is a large leakage current penalty, the increased drain current will boost the discharging for NMOS (charging for PMOS) capability of the transistor when V_{ig} is not tied together with V_{og}. Figure 5-10 (a) shows the transient graph of single-IGAA inverter simulations for various inner gate (V_{ig}) bias values. As V_{ig} increases, the output decreases earlier in the high-to-low transition. The high-to-low propagation delays are measured for increasing inner gate bias values in Figure 5-10 (b). As shown, the IGAA inverter is faster than SGAA when V_{ig} is larger than approximately 0.45 V. This result shows that the increasing V_{ig} can effectively lower the propagation delay.

5.2.2 Interconnect boosting technique

The schematics and symbols of (a) SGAA and (b) IGAA devices are shown in Figure 5-11. There are two different gates (inner gate and outer gate) for both SGAA and IGAA. In case of SGAA, the inner gate and the outer gate are connected. The inner gate and outer gate are separated and controlled independently in IGAA. The foregoing discussion demonstrates that by lowering the V_{th} value of one

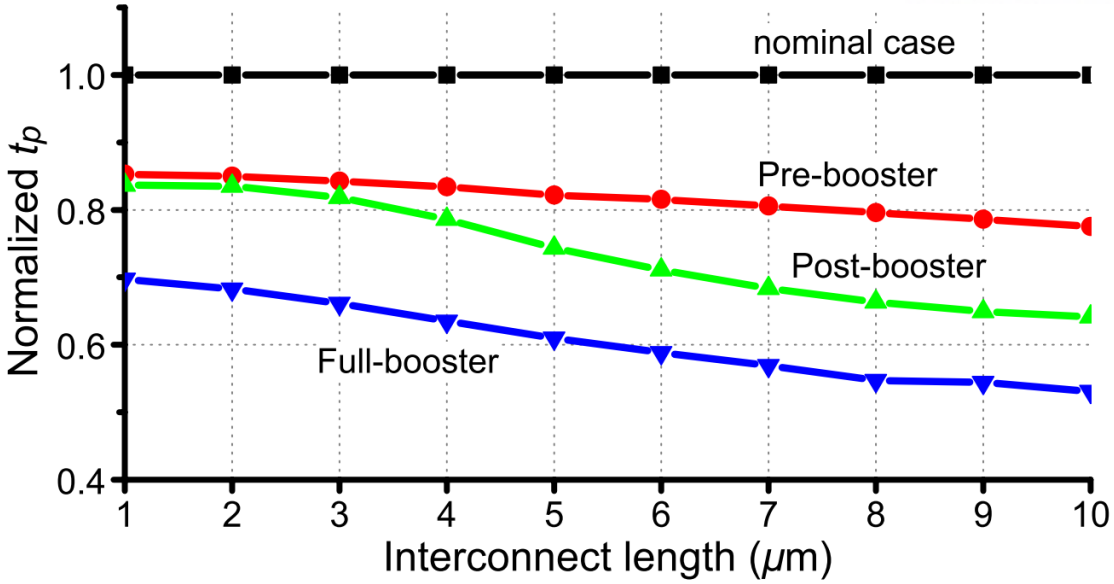


Figure 5-14. Normalized average propagation delays (t_p) among various architectures.

side of the gate, the signal can propagate through the transistor more quickly, and thus, improve the chip's performance. Particularly, following the input signal on its critical path, a boosting signal that is identical to the original input signal is routed to the inner gate of the IGAA device to lower V_{th} in advance. When distributing the digital signals inside the chip, the most popular design approach for reducing propagation delay is to introduce intermediate repeaters in the interconnect line [83-87]. To decrease the interconnect delay in modern IC design, a long interconnect is divided evenly into smaller segments with repeaters inserted between each segment (each repeater is responsible for driving one segment). Thus, the timing transmission is significantly reduced [92]. A traditional two-repeater chain structure using SGAA that is employed regularly in driving a long chain of interconnects is depicted in Figure 5-12 (a). In the repeaters, two identical inverters are connected in series; each inverter consists of two parallel SGAA devices (for double size). Multiple GAA devices should be connected in parallel to size up the GAA structure because the width of one GAA device is pre-defined by the diameter of the GAA. The proposed signal boosting technique is illustrated in Figure 5-12 (b). As shown, we develop a novel configuration that replaces the second repeater (Repeater2) with the IGAA device and keeps the first repeater (Repeater1) as an SGAA type. There are three possible boosting structures: the Pre-booster, in which only the first inverter of Repeater2 is IGAA type and where the inner gates are connected to the boosting path and the second inverter is normal SGAA without a boosting path; the Post-booster, in which only the second inverter of Repeater2 is IGAA type with a boosting path connection through the small SGAA to ensure proper polarity of the signal and the first inverter is normal SGAA type; and the Full-booster, in which both inverters of Repeater2 are IGAA type and the inner gates are connected to the boosting path directly. The driver is strong enough to drive both the repeater and the boosting path. We use five parallel SGAA inverters for the driver. The operation of the

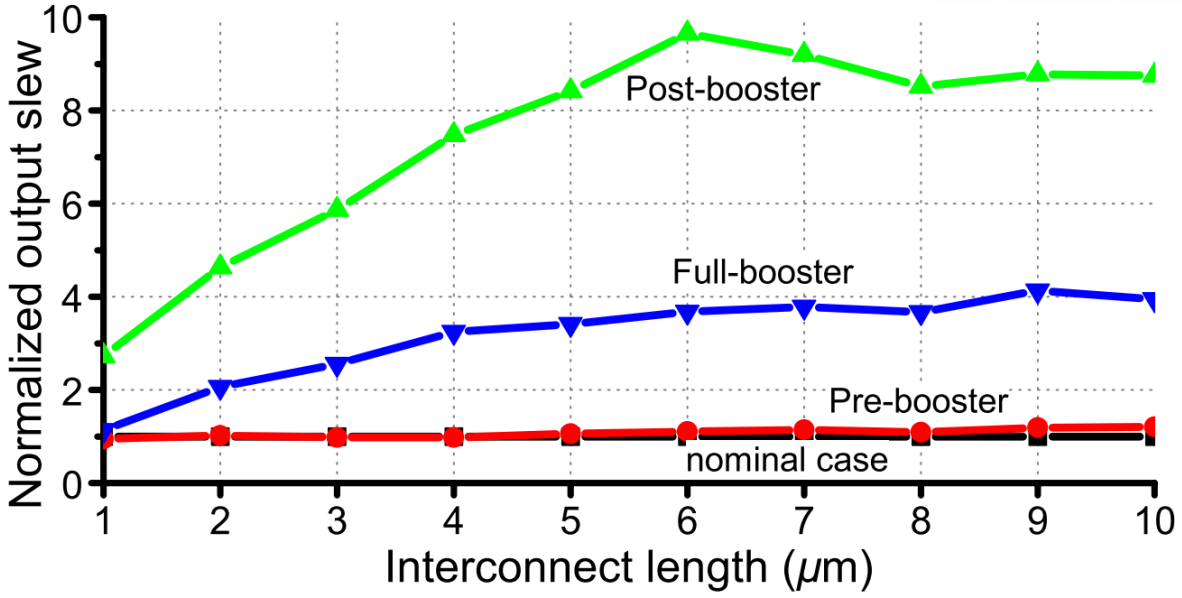


Figure 5-15. Normalized output slews among various architectures.

proposed boosting technique is as follows. When the input signal (V_{in}) changes, the signal is propagated both through Repeater1 and the boosting path. When the signal arrives at node1 (the outer gate of the first inverter), the same logic value has already arrived at node3 (the inner gate of the first inverter) and it lowers the threshold voltage of the inverter. Thus, discharging via NMOS (or charging by PMOS) can occur faster than when there is no boosting path. Additionally, the signal with opposite polarity arrives at node4 (the inner gate of the second inverter) earlier than at the input of the second inverter (the outer gate, node2). Thus, when the signal reaches the input of the inverter, the transition can occur significantly faster than when not using the boosting path. The boosting path plays a supporting role and runs parallel to the critical path, or it can be routed in a shorter path. Hence, the length of the interconnect in the boosting path is comparable to the critical path.

5.2.3 Simulation results

In this study, segments of interconnect with a specific dimension (60-nm height, 30-nm width and space, and 2.2 dielectric constant assuming 22-nm nodes [81]) are inserted between repeaters. These segments are analyzed using the distributed RC model and the parasitics are extracted in [93]. The extracted resistance and capacitance are 12.2 Ω/μm and 0.15 fF/μm, respectively. Mixed-mode transient analysis is performed in 3D TCAD [68] to measure the propagation delay between the input signal (V_{in}) and the final output (V_{out}) through the two-repeater structure for various interconnect lengths ranging from 1 μm to 10 μm. To evaluate our proposal, we compare the performance of all four repeater structures: SGAA without a boosting path (which is the nominal case), IGAA with a Full-booster (both Pre- and Post-booster paths in Repeater2), Pre-booster only, and Post-booster only. The results of the transient analysis

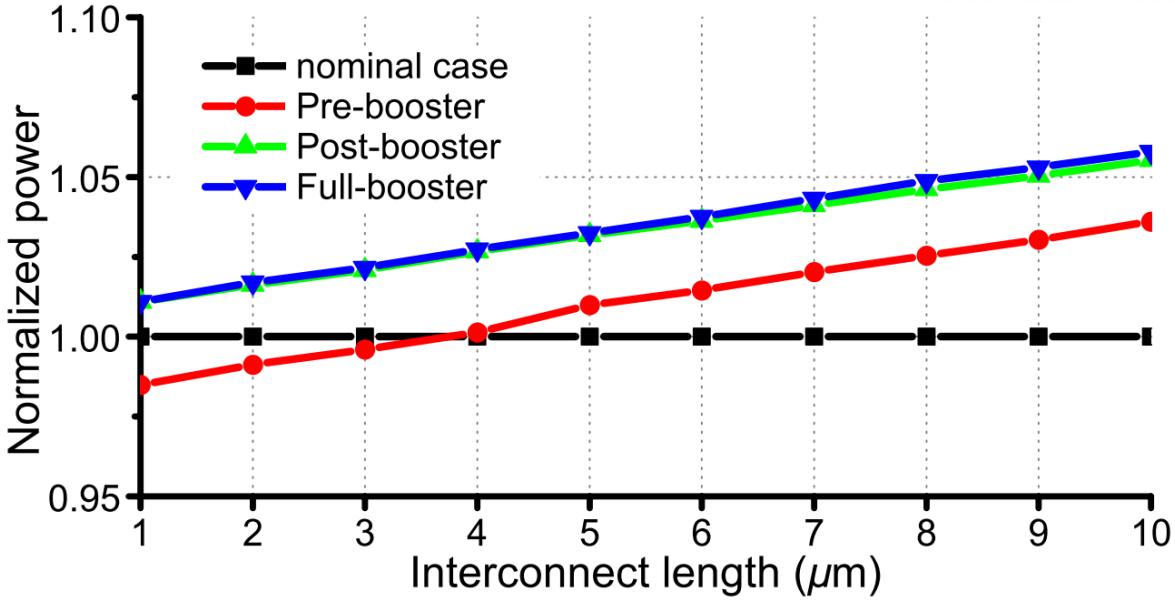


Figure 5-16. Normalized average power among various architectures.

with mixed-mode TCAD simulations of the nominal case and the Full-booster case when the interconnect length is 5 μm are plotted in Figure 5-13. As shown in the graph, V_{out} of the Full-booster rises 8.31 ps (Δt_{pLH}) earlier and falls 8.52 ps (Δt_{pHL}) earlier than the nominal case. As explained in the previous Chapter, in the Full-booster, node4 (blue solid line, the inner gate of the second IGAA inverter) is already low so as to pull-up and start charging the output node before node2 (black dotted line) arrives for the low-to-high transition case. The rise time, however, is slower than that of the nominal case because only one side of the gate is driving the output load, instead of both gates together in the nominal case. The same phenomenon occurs for the high-to-low transition and the falling time. Normalized average propagation delays (t_p) for a wide range of interconnect lengths are shown in Figure 5-14. At short interconnect lengths (i.e., 1 μm), the Pre-booster and the Post-booster can reduce the delay by as much as 15% and 16%, respectively, and the Full-booster reduces it by approximately 30%. When the interconnect becomes longer (i.e., 10 μm), our proposed structure enhances the repeater's speed effectively as demonstrated by the 22%, 36%, and 47% reduction in propagation delay with the Pre-booster, the Post-booster, and the Full-booster technique, respectively. To investigate the penalty on the driving capability caused by the single-side gate for IGAA in the boosting technique, normalized output slews (i.e., 20% – 80% rising and falling time of V_{out}) are also compared as shown in Figure 5-15. In case of the Pre-booster, the slew is comparable to that of the nominal case, because the last inverter, which is SGAA type, can recover the transition time of the output. However, high penalties on the slew rate are expected by the Post- and Full-booster because both inverters in the repeater are IGAAs. For example, the output transition time becomes up to 10× and 4× longer than in the nominal case for the sake of propagation delay improvement in the Post-booster and the Full-booster architecture,

respectively. Normalized dynamic power consumptions for both transitions are compared in various architectures for a wide range of interconnect lengths, as shown in Figure 5-16. In case of the Pre-booster, when the interconnect length is short (e.g., less than 4 μm), it consumes less power than the nominal case, because the transition slew (rise and fall time) of the first inverter in Repeater2 becomes slower in the boosting architecture. When the interconnect length is 10 μm, up to 3.5% more power is required than without the boosting path. In case of the Post- and Full-booster, there are similar power consumption penalties for all interconnect lengths because of the additional SGAA inverter and the boosting path. Up to 6% more power is required for the boosting technique when the interconnect length is 10 μm. Even though the Full-booster is the best choice for maximum signal propagation speeds for long interconnects, the Pre-booster technique provides a good tradeoff between performance (delay and slew) and power (or area) overhead The proposed configurations have been proven to be effective solutions for driving the interconnect line in the range of 1–10 μm. To apply these boosting techniques to a longer interconnect line (e.g., longer than 100 μm), we need to assemble a number of the proposed structures in series such that each boosting structure transfers the signal through a shorter length of interconnect (1–10 μm). Clearly, the proposed boosting technique takes up a portion of the area inside the chip to route the boosting path and accommodate the additional inverter; thus, it consumes a certain amount of power. Therefore, depending on the requirements of a given application, circuit designers can select Pre-booster or Full-booster to speed up performance with minimal area (and thus, power) and routing overhead. For example, the Full-booster technique is a good choice when increasing the

Table 5-3. Simulation results (normalized) when the length of the boosting path is the same as the length between repeaters.

Length (μm)	Nominal case			Pre-booster			Post-booster			Full-booster		
	Delay	Slow	Power	Delay	Slow	Power	Delay	Slow	Power	Delay	Slow	Power
1	1.00	1.00	1.00	0.85	0.95	0.98	0.84	2.72	1.01	0.7	1.14	1.01
2	1.00	1.00	1.00	0.85	1.02	0.99	0.83	4.64	1.02	0.68	2.06	1.02
3	1.00	1.00	1.00	0.84	0.98	1.00	0.82	5.87	1.02	0.66	2.56	1.02
4	1.00	1.00	1.00	0.83	0.98	1.00	0.79	7.48	1.03	0.64	3.25	1.03
5	1.00	1.00	1.00	0.82	1.06	1.01	0.74	8.42	1.03	0.61	3.41	1.03
6	1.00	1.00	1.00	0.82	1.11	1.01	0.71	9.65	1.04	0.59	3.68	1.04
7	1.00	1.00	1.00	0.81	1.14	1.02	0.68	9.19	1.04	0.57	3.78	1.04
8	1.00	1.00	1.00	0.8	1.09	1.03	0.66	8.52	1.05	0.55	3.67	1.05
9	1.00	1.00	1.00	0.79	1.19	1.03	0.65	8.78	1.05	0.54	4.13	1.05
10	1.00	1.00	1.00	0.78	1.20	1.04	0.64	8.75	1.06	0.53	3.94	1.06

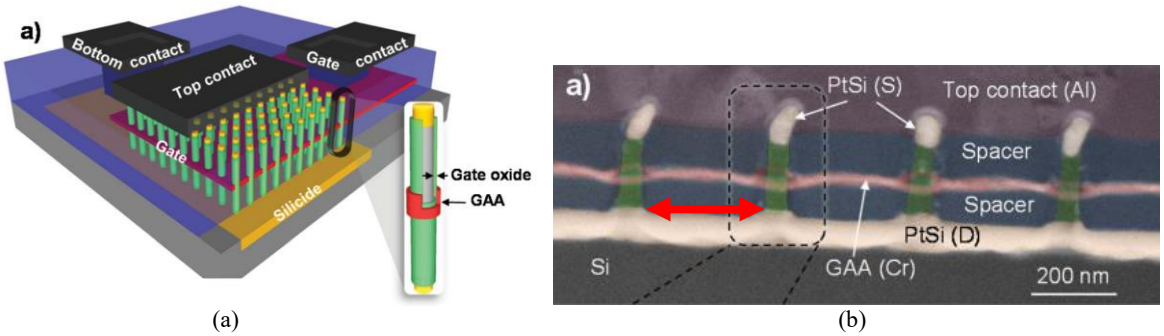
propagation delay is the primary concern whereas the Pre-booster provides a reasonable improvement in terms of delay with a small impact on the slew and power consumption. Simulation results are summarized in Table 5-3. Table 5-3 shows the results when the length of the boosting path is the same as the interconnect length between repeaters (i.e., $R_1 = R_2$ and $C_1 = C_2$ in Figure 5-12 (b)). As shown in the table, additional delay reduction and smaller power penalties can be achieved when the boosting path routed is shorter. For example, when the interconnect length between repeaters is 10 μm, up to 47% speed increase with 6% additional power can be expected. The Pre-booster provides a good trade-off between speed (delay and slew) and power consumption whereas the Post-booster is not recommended because of its significant slew rate and power consumption degradation.

5.2.4 Chapter summary

This work introduced a novel methodology for speeding-up signal propagation in the critical path by utilizing 10-nm double-gate GAAs. By taking advantages of independent control of two GAA gates, we developed boosting structures that can significantly improve the IC performance. Without considering the power consumption, propagation delay simulation on a wide range of interconnects with repeaters shows up to a 47% speed increase using the Full-booster structure. Therefore, the proposed technique may play an important role in high speed ICs, especially because critical path delay lowers the overall performance of the chips. However, when prioritizing low power consumption, the Pre-booster, which provides a good trade-off between performance and power, is an alternative solution. In addition, the improvement in the propagation delay when using the proposed boosting technique can lower overall power usage and area of the chip by reducing the number of repeaters required in the interconnect paths.

Chapter 6. Future works

This dissertation is all about process-induced structural variability-aware performance optimization for advanced nanoscale technologies. We will finish this dissertation discussing another research direction, a proposal of a novel GAA inverter unit based on the experience in Chapter 5. The proposed novel inverter will have structural variability as well due to limitations of process technology. The impact of structural variability will be a research subject as a future work. In this Chapter, the verification of the correct operation of the proposed novel GAA inverter is described. The idea comes from the literature review of vertical nanowire GAA FET [13]. The current flowing through GAA FET in the on state remains low due to the small cross-sectional area of the nanowire. As shown in Figure 6-1 (a), it is essential to implement vertical GAA FETs on nanowire arrays rather than a single nanowire in order to have excellent gate controllability on the channel with enhanced current capability [13]. Several researches have been conducted in terms of modified structure for GAA FET [79, 80, 94]. These papers suggest a nanotube architecture to enhance the performance per device with efficient area consumption. Although the fabrication process is not straightforward, it is valuable that the inventive structure is suggested. The inventive structure can be realized and produced massively if the fabrication process is mature. Here I thought that, if one implement the inverter unit by GAA FET arrays like Figure 6-1 (b), we can reduce the pitch between GAA arrays [13]. Thus, in this future work, a novel and modified structure for GAA junctionless transistor (JLT) is introduced. A sandwiched-gate (SG) logic family based on a sandwiched-gate inverter which consists of an NMOS GAA together with a donut-type PMOS is proposed and analyzed as shown in Figure 6-2. The feasibility of logic gates is demonstrated in extensive 3D TCAD simulations. The direct-current (DC) operation and the transient performance of the SG INV are investigated with TCAD simulations. The SG INV exhibits correct inverter operations with a high noise margin and speed. The proposed SG INV structure is then applied to form the fundamental logic gate cells such as NAND, NOR, and SRAM and their operations are verified. It is



(a) (b)

Figure 6-1. (a) representation of a vertical nanowire array-based GAA FET and (b) TEM cross-section of GAA FET array. [13]

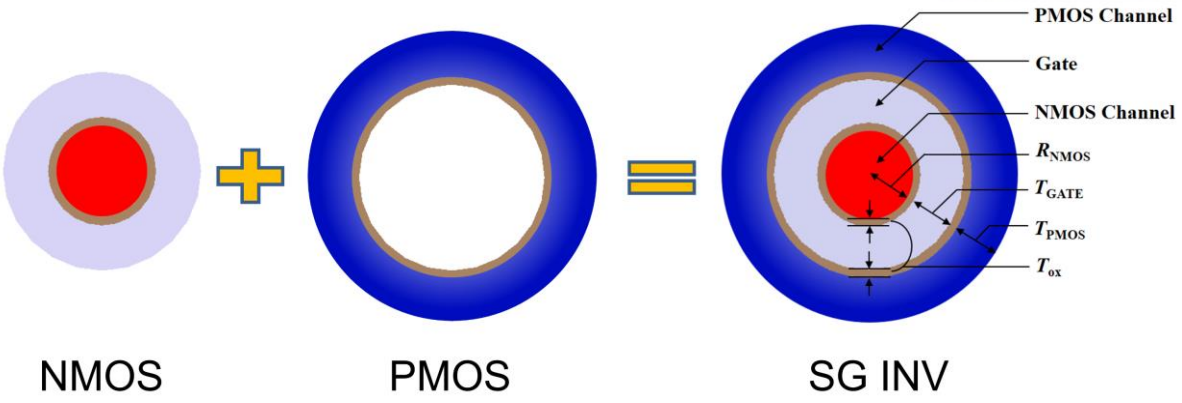
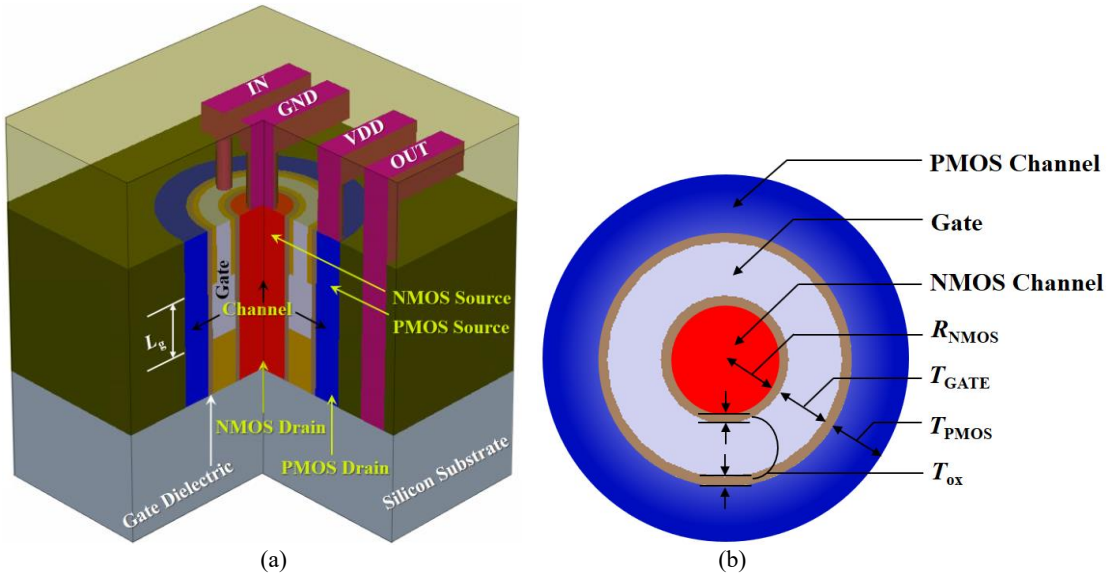


Figure 6-2. Illustration of proposed concept.

found that up to 20% area saving can be achieved by the proposed novel inverter structure.

The challenges for making an abrupt source/drain junction for inversion-mode (IM) vertical nanowire, which has $n^+/p^-/n^+$ junction structure for n-type have been much worsen. As a breakthrough for junction induced problems, the junctionless (JL) transistors have received much attention with simple process technology [95-97]. JLT has single-doping species and uniform doping concentration in source, channel, and drain, which has $n^+/n^+/n^+$ junction structure for *n*-type. JLT has no source/drain junctions and the operation is by current conduction through body channel, whereas the operation of a conventional IM transistor is controlled by current of sheet channel which is formed beneath the semiconductor-oxide interface.



(a) (b)

Figure 6-3. Illustration of the proposed sandwiched-gate inverter. (a) 3D cross section, (b) cross section cut through the channel region.

Table 6-1. Physical parameters used for simulations.

Parameters	Value
Gate length (L_g)	10 nm
Gate dielectric thickness (T_{ox})	1 nm
Gate metal thickness (T_{gate})	5 nm
P-type silicon thickness (T_{PMOS})	5 nm
N-type silicon radius (R_{NMOS})	5 nm
Source/channel/drain doping (N_{SCD})	2×10^{19} cm^{-3}
Supply voltage (V_{DD})	0.75 V

Our research focuses on the proposal of novel inverter structure and verification. A sandwiched-gate inverter forms this structure as shown in Figure 6-3 (a). A cross-section through the channel region is illustrated in Figure 6-3 (b). As shown in Figure 6-3 (a) and (b), the NMOS silicon body is in the center followed by the gate oxide. Then, the gate material is formed in the channel region surrounding the inner gate oxide to generate an *n*-type GAA transistor. In turn, the gate is surrounded by the outer gate oxide and, finally, the PMOS silicon body wraps around the outer gate oxide to make a sandwiched-gate structure. The regions between the sources and the drains of NMOS and PMOS are filled by spacer. To form a CMOS inverter, both the NMOS and PMOS drains are tied together at the bottom of the structure and connected to the contact (OUT) through the vertical metal. In addition, the source of NMOS is connected to the GND and the source of PMOS is connected to the V_{DD}. The source (S), drain (D), and channel (CH) regions are equivalently doped with (2×10^{19} cm^{-3}) concentration. The structure

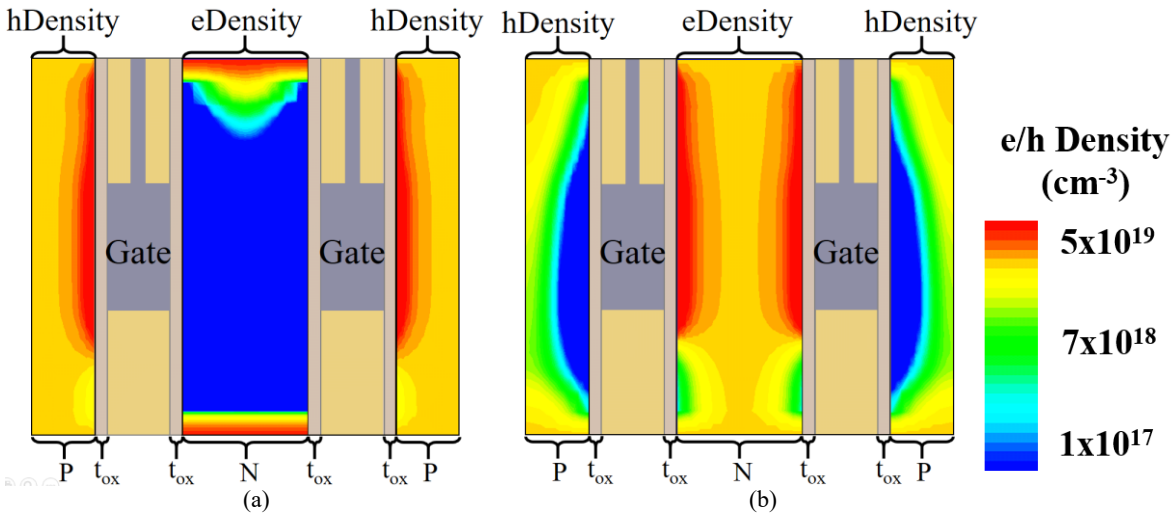


Figure 6-4. The electron/hole density profile for (a) V_{IN} = 0 V and (b) V_{IN} = 0.75 V. The NMOS and PMOS channel are successfully turned off by an opposite gate bias.

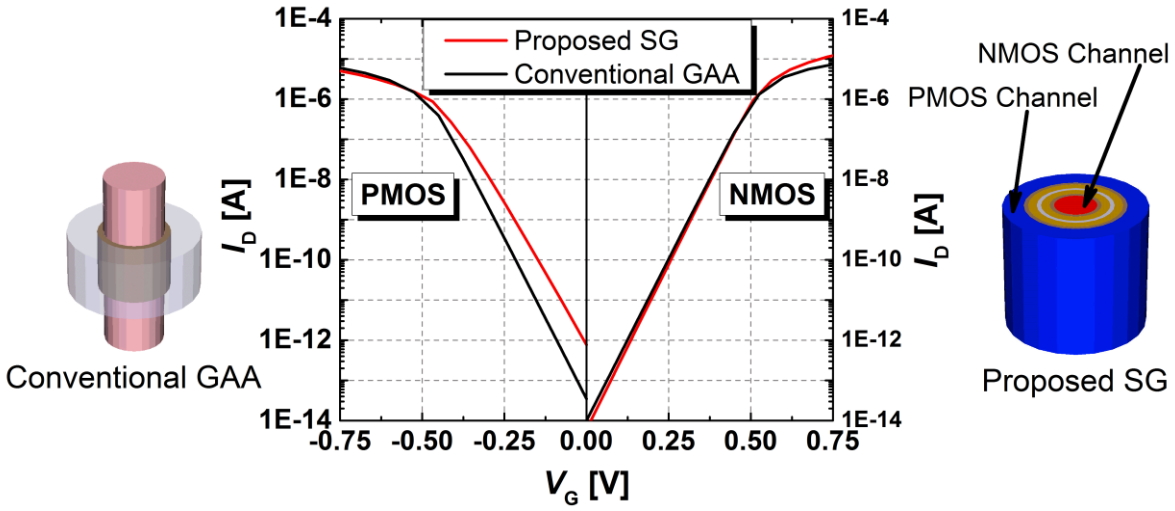
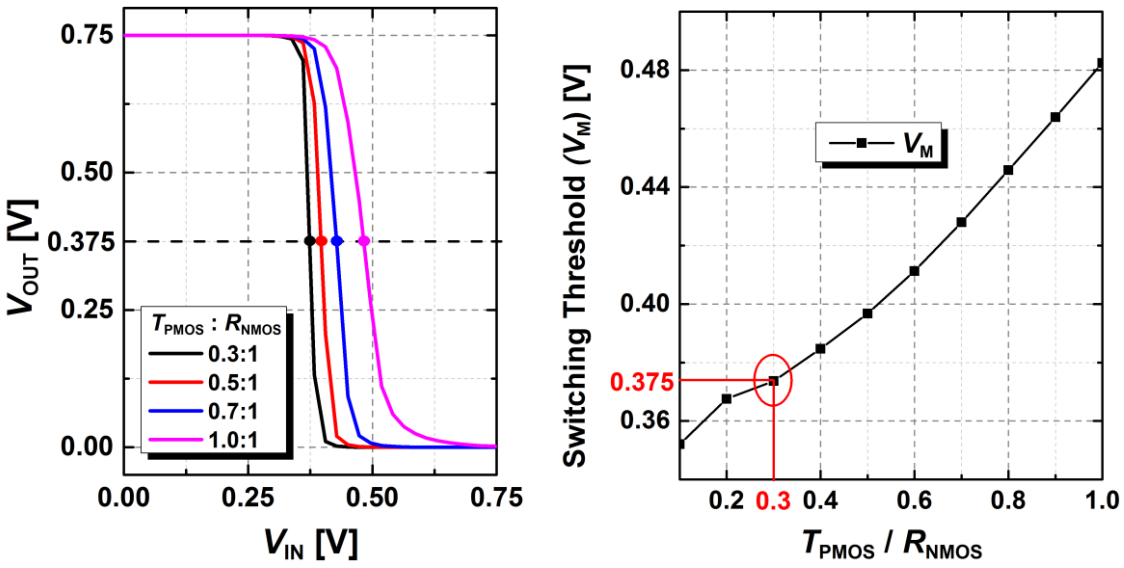


Figure 6-5. I_D-V_G characteristics of the PMOS/NMOS devices in the proposed inverter and individual conventional GAA SNWT (cylinder shape).

dimension and parameter values used in this study are summarized in Table 6-1.

To verify the correct operation of the proposed design as an inverter, DC simulations were conducted in a 3D-TCAD tool [68]. Figure 6-4 (a) and (b) show electron and hole density profiles for V_{IN} = 0.0 V and 0.75 V (V_{DD}), respectively. As shown in those figures, the conduction channel is formed at the PMOS region (outer donut) when the input voltage is low (Figure 6-4 (a) V_{IN} = 0.0 V) and the conduction



(a) (b)

Figure 6-6.(a) Voltage transfer curves (VTC) and (b) switching threshold (V_M) as a function of the T_{PMOS} to R_{NMOS} ratio. The V_M becomes the half of the V_{DD} (0.375 V) when the ratio is 0.3:1 (e.g., T_{PMOS} = 3 nm and R_{NMOS} = 10 nm)

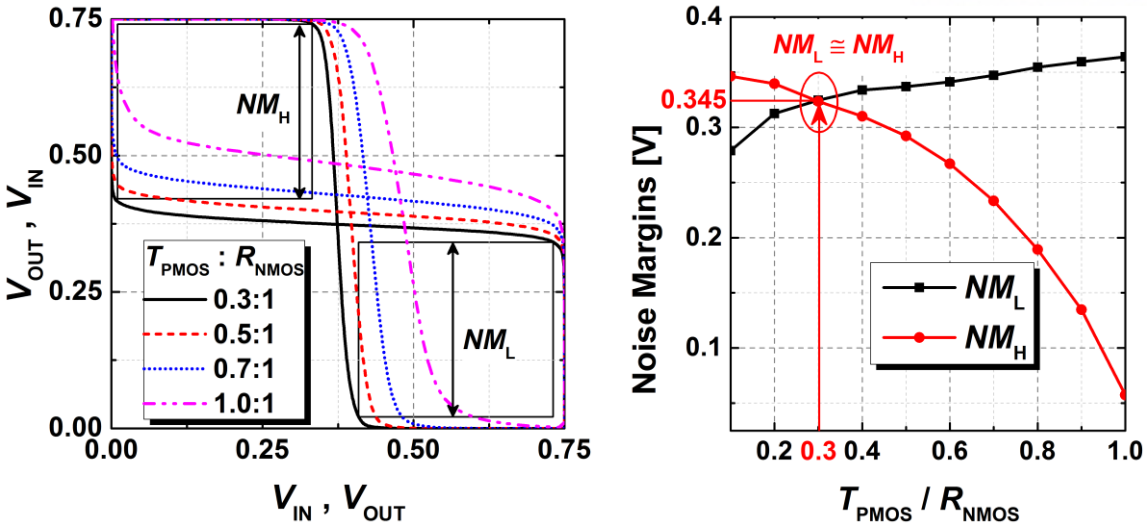


Figure 6-7. (a) Butterfly curves and (b) static noise margins.

channel is formed only at the NMOS region (core) when the input voltage is high (Figure 6-4 (b) $V_{IN} = 0.75$ V). At the same time, the NMOS and PMOS channels are successfully turned off by an opposite gate bias. $I_D - V_G$ characteristics of the individual conventional GAA SNWT (cylinder shape) and the PMOS/NMOS devices in the proposed inverter are shown in Figure 6-6. As shown, both NMOS and PMOS devices in our proposed inverter reveals similar electrical characteristics with the conventional cylinder shape GAA transistor. We investigated the relationship between the size of the NMOS (core radius, R_{NMOS}) and the size of the PMOS (the outer thickness, T_{PMOS}) so that the switching

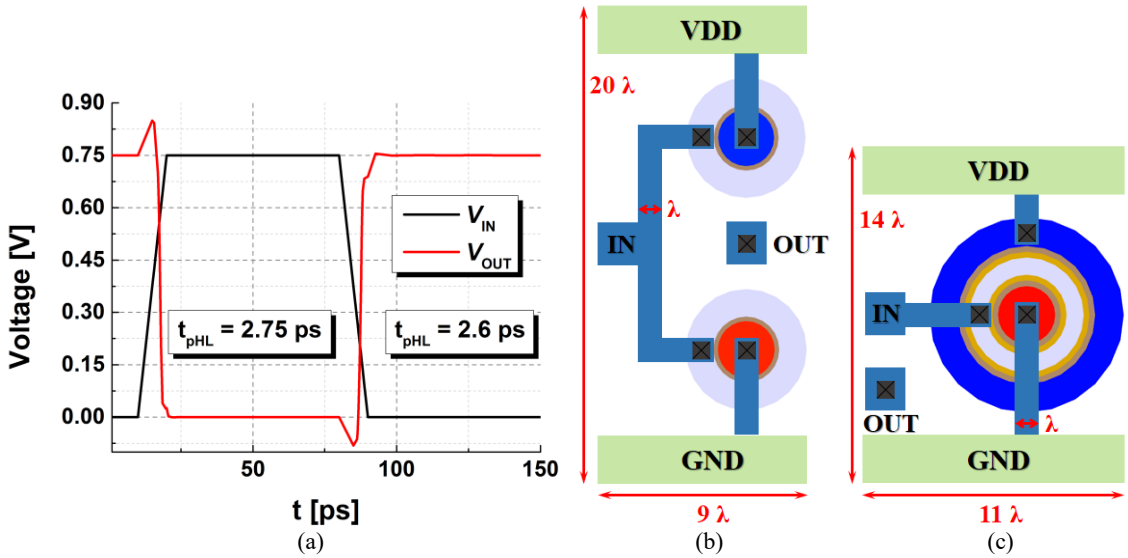
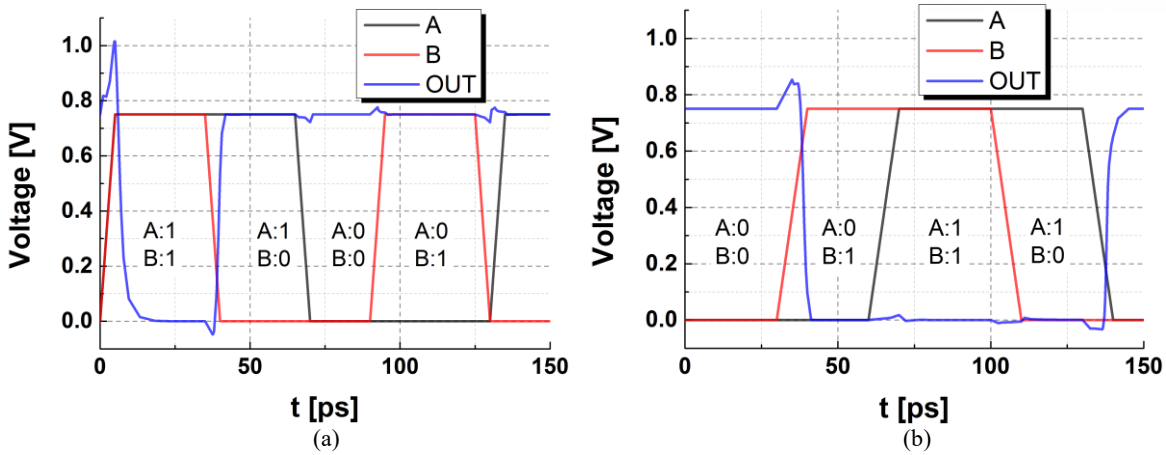


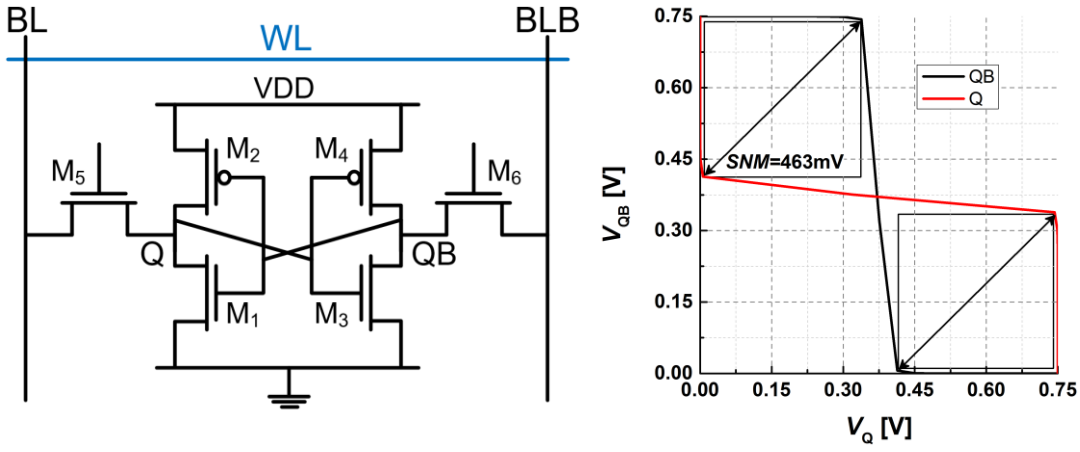
Figure 6-8. (a) Transient simulation of the proposed inverter. Layout examples of (b) general GAA inverter, (c) proposed SG INV. λ is the minimum feature. Proposed SG INV has 14% reduction in the layout area in this example.



(a) (b)

Figure 6-9. Transient simulation of the proposed NAND and NOR logic.

threshold (V_M) of a proposed CMOS inverter is located in the middle between the supply rails. The voltage transfer curves of the proposed inverter for various T_{PMOS} to R_{NMOS} ratios are shown in Figure 6-6 (a). The V_M values as a function of the T_{PMOS} to R_{NMOS} is plotted in Figure 6-6 (b). As shown in those figures, the V_M becomes the middle of the V_{DD} (0.375 V in this study) when the ratio of the PMO S thickness to NMOS radius is 0.3:1 (e.g., T_{PMOS} = 3 nm and R_{NMOS} = 10 nm). This PMOS/NMOS ratio can also be explained by considering effective channel area comparison. The s witching threshold is determined by the current driving strength of PMOS and NMOS. In this way, we can calculate approximate value of ratio. As shown in Figure 6-6 (a), the voltage transfer curve with adequate sizing provides a remarkably high gain during the switching transient exhibiting a very narrow transition zone. Therefore, the proposed inverter has outstanding noise margin because of the steep slope in transition zone. Figure 6-7 (a) shows the butterfly curves of the proposed inverter to estimate the static noise margins (N_{MH} and N_{ML}) for various PMOS-to-NMOS ratios. Both low and high noise margins as



(a) (b)

Figure 6-10. (a) 6T SRAM schematic and (b) static noise margin (SNM) of SRAM with proposed sandwiched-gate logic.

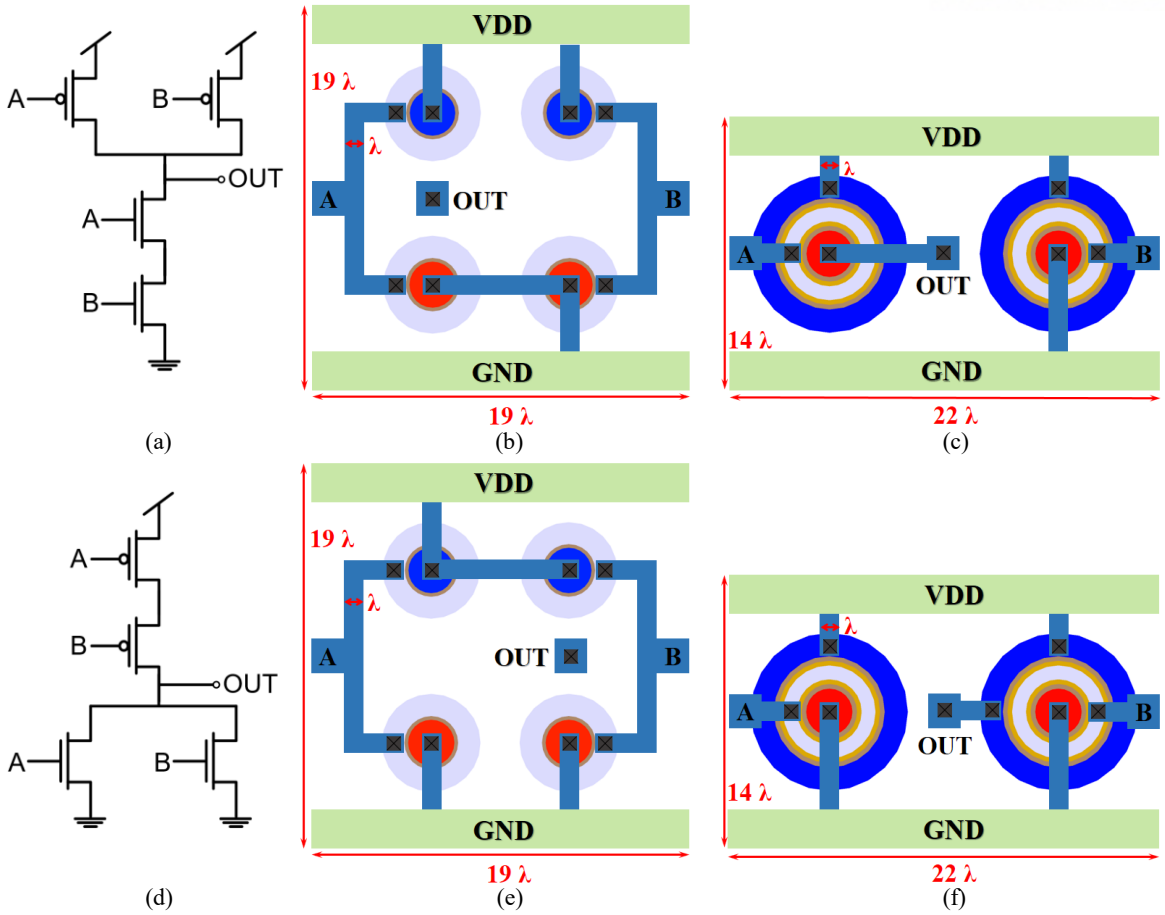


Figure 6-11. Layout example of NAND and NOR with gate-all-around transistor and with sandwiched-gate logic.

a function of the ratio are plotted in Figure 6-7 (b). The high noise margin (N_{MH}) degrades rapidly as the T_{PMOS} gets thicker. As expected, the ratio ranges of between 0.3 and 1.0 provides the optimum low and high noise margin characteristics with approximately 0.345 V. As shown, the static noise margin of 92% of the half V_{DD} can be achieved by the proper sizing. Transient simulations are conducted to analyze the dynamic performance of the proposed inverter. A pulse of 10 ps rise/fall time is applied to the gate terminal and the propagation delay is measured between the input and the output of the inverter. The unloaded propagation delay of the size-matched inverter is 2.75 ps in a high-to-low transition and 2.6 ps for a low-to-high transition as shown in Figure 6-8 (a). In order to check that the proposed inverter will reduce layout area, layout examples are illustrated in Figure 6-8 (b). In this example, 14% reduction in layout area can be achieved.

We have verified the feasibility and analyzed the performance and the area benefit of the proposed SG inverter which is the basic logic element of circuit design. To design more complex ICs, other logic gate families, such as NAND, NOR, and SRAM cells, are required. The proposed SG inverter structure can be easily applied to construct these complex logic gates. The source and drain of NMOS and PMOS can be configured to form required logic gates. For example, the drain and the source are tied together

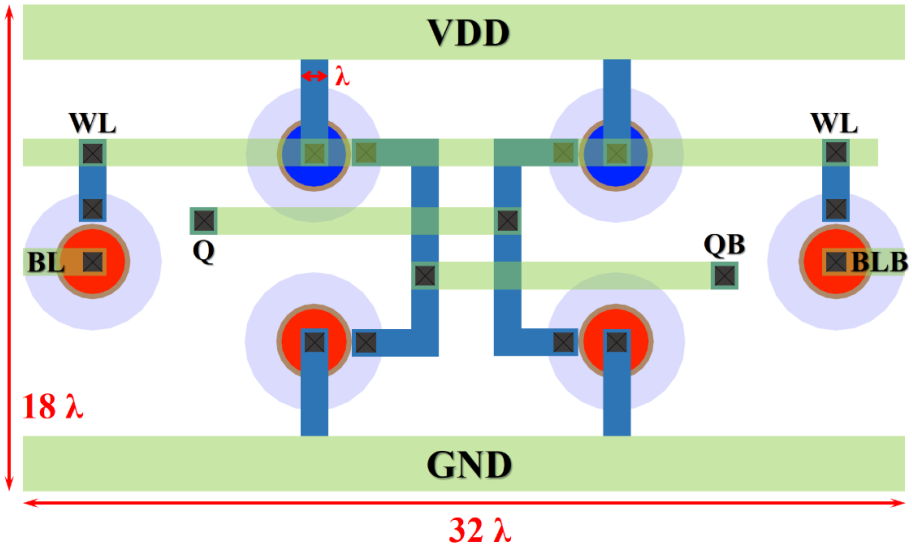


Figure 6-12. Layout example of SRAM with gate-all-around transistor.

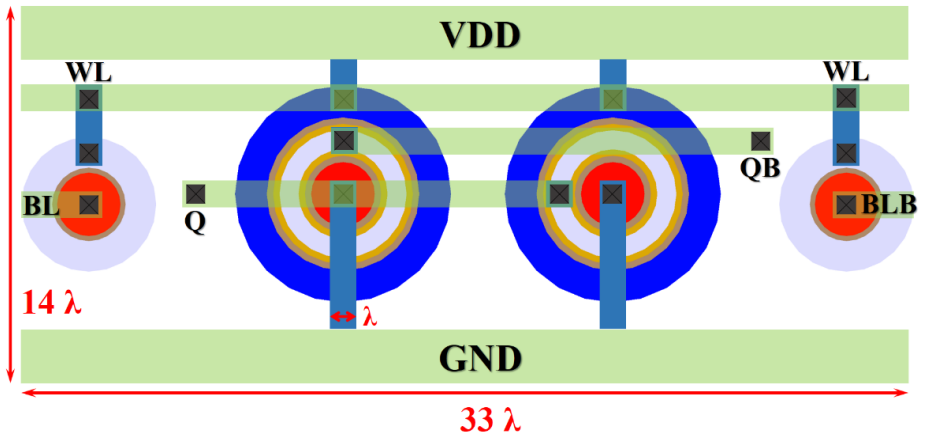


Figure 6-13. Layout example of SRAM with sandwiched-gate logic.

Table 6-2. Area improvement.

Area			
Logic	GAA-based	SG INV-based	Improvement
INV	180	154	14%
NAND2	380	308	19%
NOR2	380	308	19%
SRAM	576	462	20%

to make a series connection. On the other hand, two drains or two sources are tied together to form a parallel connection. The correct operation of NAND and NOR gates are verified by transient simulations

as shown in Figure 6-9. As shown, NAND and NOR gates based on the proposed SG inverter structure generate correct output patterns for all four input patterns. The static noise margin (SNM) of the SRAM cell based on the proposed SG inverter is analyzed in DC simulation as shown in Figure 6-10. As shown, the SNM of the SG inverter-based SRAM is 463mV. In order to quantify the amount of benefit of the NAND, NOR, and SRAM, each layout examples are shown in Figure 6-11-Figure 6-13. The area benefit in layout example using sandwiched-gate logic are summarized in Table 6-2.

As a future work, a novel sandwiched-gate inverter by using of an NMOS GAA together with a donut-type PMOS is proposed. The DC operation and the transient performance of the proposed inverter were investigated with 3D TCAD simulations. The proposed inverter exhibits a correct inverter operation with a high noise margin and speed. The novel inverter structure can be extended to more complex logic gates, such as NAND and NOR gates, and will significantly reduce the overall size of the chip when the manufacturability of the vertical GAA matures. For the future, the layout benefit will be investigated using precise design rules and the impact of structural variability will be a future work.

Chapter 7. Conclusion

The purpose of the device-circuit co-optimization is to take circuit-level considerations into account during device design. This dissertation solves problems that may arise between device and circuit development which causes difficulty in predictive modeling of emerging technologies, such as nano-scale MOSFET, FinFET, and gate-all-around (GAA) FET. Efficient models for device-level variability are critical in integrated circuit design using advanced technology nodes. Thus, the proposed methods in this dissertation will be helpful for understanding the relationship between device variability and circuit performance.

The overall dissertation is summarized as follows:

Chapter 3 focuses on a technique for simple and accurate modeling that analyzes non-rectilinear gate (NRG) CMOS transistors with a simplified trapezoidal approximation method. The electrical characteristics of the LER gate are approximated by a trapezoidal shape, which is acquired by the length of the longest slice, the length of the smallest slice, and the weighting factor, instead of taking the summation of all the slices into account. The results of the TCAD simulation dhow that the proposed model is suitable for device simulation with edge effects, and its error for Ion is around 1% for various NRG transistors. For a more realistic application of the proposed model, the model is applied to NOR and NAND post-lithography images. The absolute errors of the model are 0.76% and 0.97% for NOR and NAND cases, respectively. The accuracy can even be improved by adopting the width-location-dependent factor (W_{eff}). The positive effect of diffusion rounding at the transistor source side of a CMOS is then discussed. The proposed simple layout method provides boosting the driving strength of logic gates and also saving the leakage power with a minimal area overhead. The method provides up to 13% speed up and also saves up to 10% leakage current in an inverter simulation by exploiting the diffusion rounding phenomena in the transistors. The layout of the diffusion rounded CMOS shows a minimal impact in the cell area compared to the original compact layout.

Chapter 4 discusses the performance impacts of the trapezoidal fin shape of a double-gate FinFET is analyzed with numerous TCAD simulations. In this work, we extend the device level analysis to the circuit level performance metric by using mixed-mode simulations and propose the optimum trapezoidal angle ranges in circuit performance through the combined analysis. The TCAD simulations show that the driving capability improves, and the gate capacitance increases as the bottom fin width of the trapezoidal fin increases. The increase in the gate capacitance nullifies the benefit of the current increase due to the trapezoidal fin at larger angle. The FO4 inverter and RO delay results indicate that careful optimization of the trapezoidal angle can increase the speed of the circuit because the ratios of

the current and capacitance have different impacts depending on the trapezoidal angle.

Chapter 5 focuses on the investigation the electrical characteristics of a DGAA transistor with an asymmetric channel width. The channel width asymmetry is analyzed on both sides of the terminals of the transistors, i.e., source and drain. In addition, both *n*-type and *p*-type DGAA FETs are considered. The BSSD structure is expected to be preferable for NMOS devices, whereas the BDSS structure is expected to be preferable for PMOS devices, providing a greater ability to drive current and maintaining a lower off-current. The optimal inverter provides 27% faster propagation delay with 15% less leakage power than the nominal structure since the optimal amount of variation is carefully chosen in the device analysis. RO simulation indicates that an 11% faster oscillating frequency (with a relatively small penalty in terms of dynamic power) can be achieved when using the optimal inverters. Secondly, as an initial application of DGAA to interconnect, the application of double gate-all-around (DGAA) transistor to on chip interconnect boosting is proposed. This work proposes a boosting structure that can significantly improve the performance of circuits by controlling the two gates of the DGAA independently. A novel methodology is proposed for speeding-up the signal propagation in the critical path by utilizing 10 nm double-gate GAA. Without considering the power consumption, propagation delay simulation on a wide range of interconnects with repeaters shows up to a 47% speed increase using the full-booster structure.

In Chapter 6, as a future work, a novel inverter structure is discussed. Sandwiched-gate inverter (SG INV) consisted of an NMOS GAA together with a donut-type PMOS, which can improve the overall circuit footprint area by combining separate *p*-type GAA and *n*-type GAA together. The DC operation and the transient performance of the proposed inverter were investigated with 3D TCAD simulations. The proposed inverter exhibits a correct inverter operation with a high noise margin and speed. In addition, the proposed SG INV can be used to construct NAND, NOR, and SRAM cells, and will significantly reduce the overall size of the chip when the manufacturability of the vertical GAA matures.

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CURRICULUM VITAE

Myunghwan Ryu received a B.S. degree in electrical engineering and computer science from Kyungpook National University, Daegu, Korea, in 2010, and an M.S. degree in electrical and computer engineering from the Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, in 2012, where he is currently working toward a Ph.D. degree in electrical engineering. His current research interests include TCAD-based process-induced structural variability-aware optimization for nano-scale CMOS/FinFETs, and design/circuit co-optimization methodologies, and design/simulation/modeling for variability of gate-all-around (GAA) FET