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Optimal inverter logic gate using 10-nm double gate-all-around (DGAA) transistor with asymmetric channel width

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We investigate the electrical characteristics of a double-gate-all-around (DGAA) transistor with an asymmetric channel width using three-dimensional device simulation. The DGAA structure creates a silicon nanotube field-effect transistor (NTFET) with a core-shell gate architecture, which can solve the problem of loss of gate controllability of the channel and provides improved short-channel behavior. The channel width asymmetry is analyzed on both sides of the terminals of the transistors, i.e., source and drain. In addition, we consider both *n*-type and *p*-type DGAA FETs, which are essential to forming a unit logic cell, the inverter. Simulation results reveal that, according to the carrier types, the location of the asymmetry has a different effect on the electrical properties of the devices. Thus, we propose the N/P DGAA FET structure with an asymmetric channel width to form the optimal inverter. Various electrical metrics are analyzed to investigate the benefits of the optimal inverter structure over the conventional inverter structure. Simulation results show that 27% delay and 15% leakage power improvement are enabled in the optimum structure. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.* [http://dx.doi.org/10.1063/1.4940755]

The scaling limits of CMOS technology make it difficult to follow Moore's law, which would require novel device structures to increase gate controllability and suppress short channel effects (SCEs). Beyond the 10-nm technology node, the gate-all-around (GAA) FET is the natural evolution of multi-gate architectures and is considered to be a promising solution for continuing Moore's law.[1] However, contrary to general expectations, it was found that a conventional top-down process produces asymmetric channel structures rather than symmetric cylindrical shapes in the GAA structure.[2] The electrical properties of vertical silicon nanowire structures with an asymmetric channel width have been investigated in previous studies.[3,4] However, only *n*-type transistors were analyzed in these studies and the effective channel area was not considered. In this case, it is difficult to determine whether the performance differences in comparison targets are caused by structural differences (i.e., asymmetry) or by effective area. To the best of our knowledge, the concept of the DGAA FET was first introduced in 2011; the device was an *n*-type nanotube FET.[5] A *p*-type DGAA nanotube FET was compared to the nanowire FET architecture in the following year.[6]

In this study, we consider not only the asymmetry of the channel width at the source and drain sides but also two carrier types (i.e., *n* and *p*) in the DGAA FET. Then, analysis of the asymmetry in the channel width can provide the optimal structures of the *n*- and *p*-type DGAA FETs to form a basic logic gate, the inverter. We investigate the electrical characteristics of the DGAA transistor with an asymmetric channel width using three-dimensional technology computer-aided

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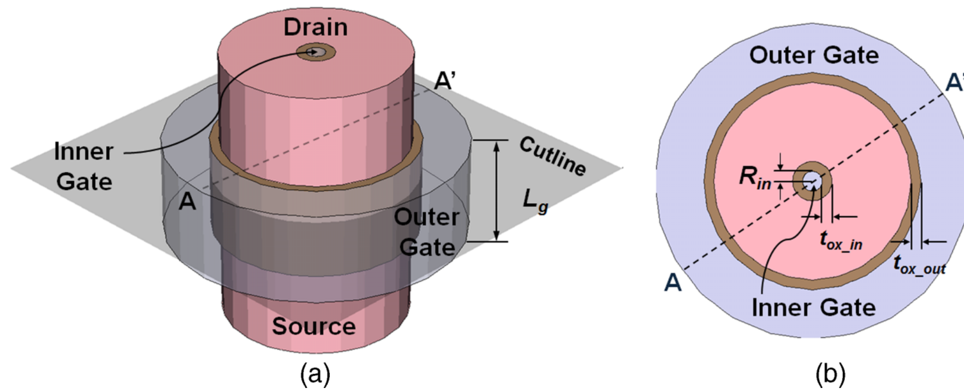

FIG. 1. DGAA FET structure used in device simulations. (a) bird's eye view and (b) cross-sectional view.

design (3D TCAD) device simulation. The nominal 3D device structure used in this study is shown in Fig 1. The DGAA has two gate terminals, inner and outer gate, and the gates can either be tied together to enhance device performance or be controlled independently for threshold voltage (V_{th}) modulation and leakage minimization. The nominal physical parameters used in the device simulations are summarized in Table I. The channel length (L_g) is 10 nm. Both inner and outer gate oxide thicknesses (t_{ox}) are set to 1 nm. The radius of the silicon channel is 10 nm. The channel region is lightly doped with $1 \times 10^{16} cm^{-3}$ boron (for nFET) or arsenic (for pFET) to reduce random dopant fluctuation (RDF) effects and avoid mobility degradation. The source/drain are doped with 2×10^{19} arsenic and boron for *n*-type and *p*-type, respectively. A high-k metal-gate (HKMG) process, using tungsten and HfO_2 as gate electrode and gate dielectric, respectively, is used to construct the gate region. The supply voltage is set to 0.75 V, according to the ITRS roadmap.[7] TCAD Sentaurus Device,[8] software is used to perform device simulations.

Two types of channel width variation in the DGAA structure are investigated, as shown in Fig. 2, (a) big-source small-drain (BSSD) and (b) big-drain small-source (BDSS). The variations in the diameters of the top and bottom of the nanotube are of the same value but have opposite sign; thus, the silicon channel maintains the same area with a nominally cylindrical channel so as to ensure the effective channel area. As shown in Fig. 2(c)-2(f), variations in source- and drain-side parameters have different effects on the electrical properties. In *n*-type FETs (NMOS), the static leakage current, I_{off} becomes better (less leaky) in both structures as the diameter variation increases and the driving current, I_{on}, improves only when the source side becomes wider (i.e., in BSSD) but degrades at a smaller source side diameter (i.e., in BDSS); I_{on} increases up to D_{NW} = 3 nm when the source side becomes wider. On the other hand, I_{on} of a *p*-type FET (PMOS) has the opposite trend because of the asymmetry of the source and drain; I_{on} increases up to D_{NW} = 2 nm when the drain side becomes wider and I_{off} has the same trends.

TABLE I. Physical parameters used in the device simulation.

Parameters	Value
Channel length (L_g)	10 nm
Inner gate oxide thickness (t_{ox_in})	1 nm
Outer gate oxide thickness (t_{ox_out})	1 nm
Radius of silicon channel	10 nm
Channel doping concentration	$1 \times 10^{16} cm^{-3}$
Source/drain concentration	$2 \times 10^{19} cm^{-3}$
Supply voltage (V_{DD})	0.75 V
Gate material	Tungsten
Gate oxide material	HfO_2

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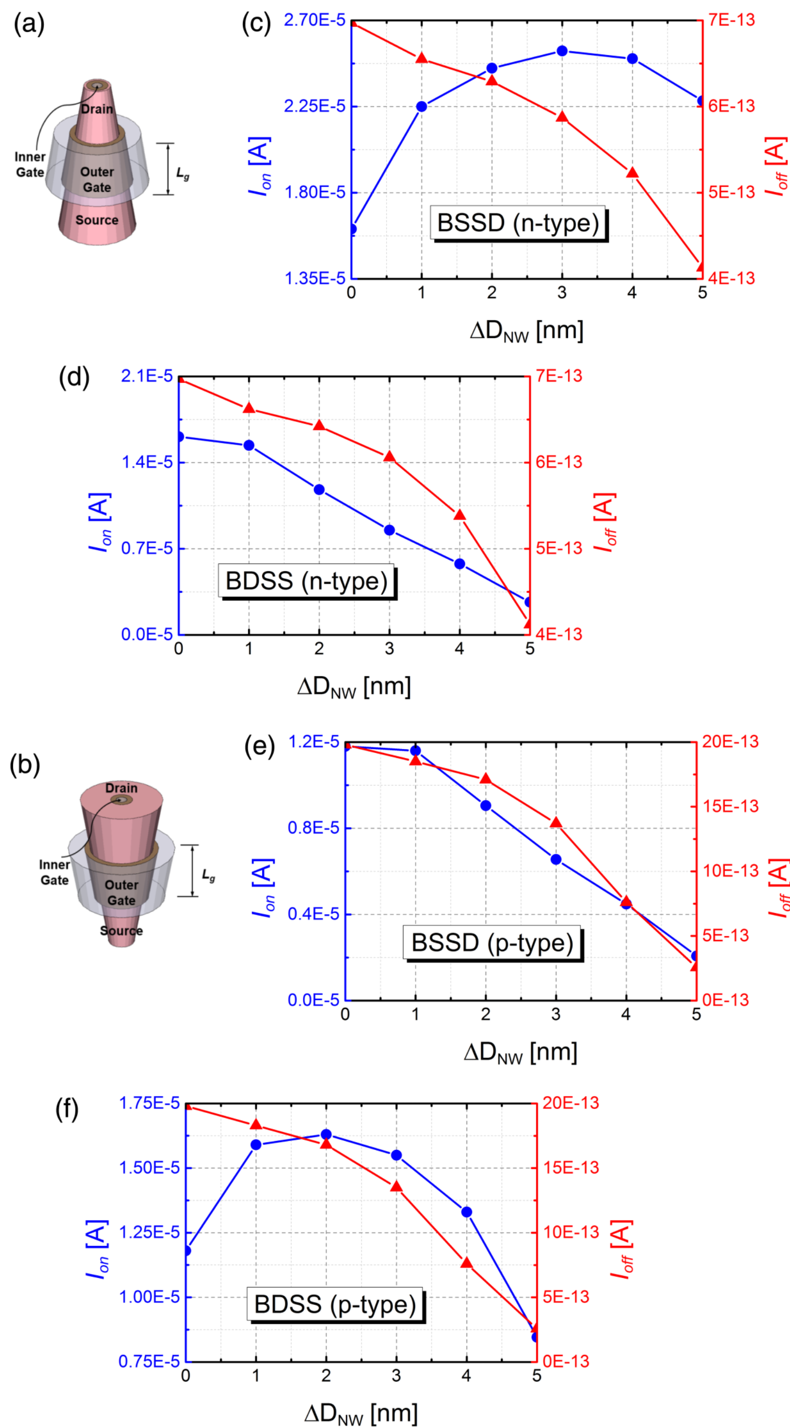

FIG. 2. DGAA FET structure used in device simulations and simulation results. Structures of (a) BSSD (big-source small-drain), (b) BDSS (big-drain small-source), simulation results of (c) n-type BSSD, (d) n-type BDSS, (e) p-type BSSD, and (f) p-type BDSS.

As a result, the BSSD structure shown in Fig. 2(a) is expected to be a preferable structure for the NMOS and BDSS structure shown in Fig. 2(b) for PMOS in terms of providing greater ability to drive current and maintain a lower off-state current. This finding leads us to propose an optimal complimentary metal-oxide-semiconductor (CMOS) logic gate, i.e., an inverter, by combining BSSD NMOS and BDSS PMOS, as schematically depicted in Fig. 3.

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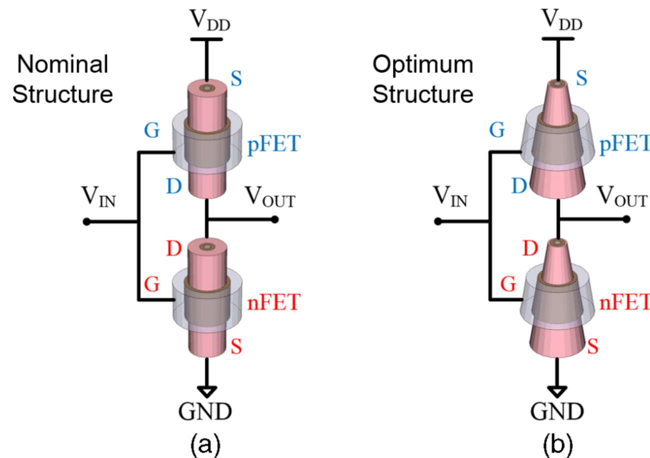

FIG. 3. Circuit schematics of vertical Si DGAA FET-based inverter for (a) nominal structure and (b) optimal structure.

To analyze the electrical characteristics of the optimal inverter using the asymmetric DGAA, several circuit-level metrics are investigated: propagation delay, dynamic power, leakage power, and ring oscillator (RO) frequency. The capacitance of the asymmetric DGAA inverter is shown in Fig. 4. As the asymmetry increases, the drain capacitance of the BSSD *n*-type device decreases and the drain capacitance of the BDSS *p*-type device increases. Thus, the total gate capacitance (C_{gate}) and internal loading capacitance (C_{load} (internal)), which behave as a total loading component when the inverter is driving itself, are not significantly increased. Therefore, from the dynamic point of view, the impact of asymmetry on the capacitance of the inverter will be small.

The propagation delay of the logic gate is a function of the capacitance and the current flowing through the transistor. As shown in the previous results, 58% and 38% larger currents flow, for NMOS and PMOS, respectively, for the optimal inverter relative to the nominal inverter. Additionally, because the device maintains the same channel area, there is a negligible discrepancy in the gate capacitance between optimal and nominal devices. Therefore, transient simulations of the DGAA inverter show that the optimal structure is 27% faster than the nominal structure, as shown in Fig. 5. In addition, the static leakage current of the DGAA inverter is 15% smaller than the nominal inverter (e.g., 1.34 pA for the nominal structure and 1.13 pA for the optimal structure).

To quantitatively evaluate the impact of the asymmetric DGAA FET at the circuit level, a five-stage RO is considered in the Sentaurus Device mixed-mode simulations as performance metrics to investigate the frequency and dynamic behavior of the proposed structure. The outputs

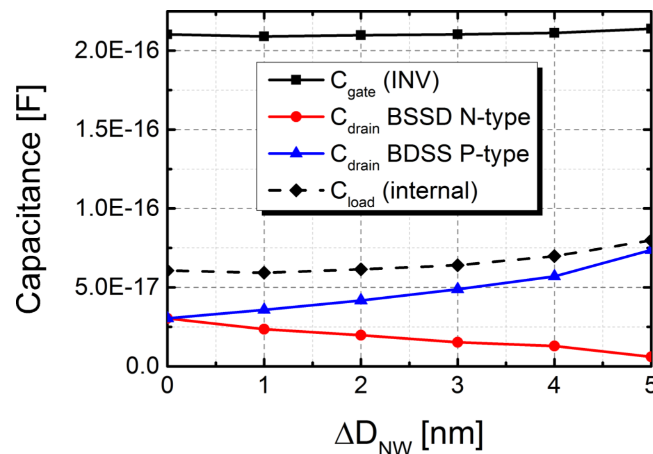

FIG. 4. Capacitance of the asymmetric DGAA inverter.

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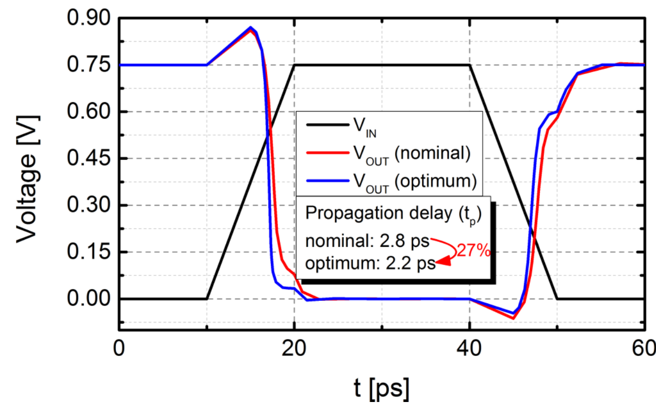

FIG. 5. Transient simulation of DGAA inverter.

of the DGAA-based five-stage RO for both the nominal and the optimal inverter are shown in Fig. 6. The signal oscillating through the RO chain is determined by each inverter stage; the RO composed of optimal inverters has a higher speed of signal transition. As expected, for the RO using optimal inverters, the signal oscillating frequency is improved by 11% (from 15.2 GHz to 16.9 GHz) consuming approximately 5% (9.3 μW vs. 9.8 μW) more dynamic power.

In this study, the asymmetry of the DGAA channel width is analyzed; the source- and drain-side asymmetry produces different electrical properties. The BSSD structure is expected to be preferable for NMOS devices, whereas the BDSS structure is expected to be preferable for PMOS devices, providing a greater ability to drive current and maintaining a lower off-current. Novel device structures are proposed to form the optimal inverter. Several electrical metrics are used to analyze the characteristics of the optimal inverter. The optimal inverter provides 27% faster propagation delay with 15% less leakage power than the nominal structure since the optimal amount of variation is carefully chosen in the device analysis. RO simulation indicates that an 11% faster oscillating frequency (with a relatively small penalty in terms of dynamic power) can be achieved when using the optimal inverters. In a perspective of fabrication process, however, controlling the amount of variation to form asymmetric DGAA transistors may be challenging. If the amount of variation can be precisely controlled with advanced technology in near future, this work has significant meaning in DGAA-based circuit designs.

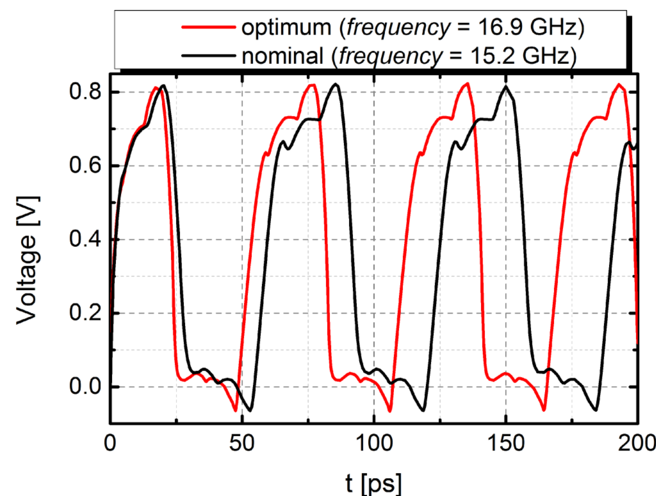

FIG. 6. Transient simulation of DGAA-based five-stage ring oscillator.

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