Design of Automotive Communication Local Interconnect Network Transceiver for Physical Layer

Daewung Kim

Department of Electrical and Computer Engineering
(Electrical Engineering)

Graduate School of UNIST

Design of Automotive Communication Local Interconnect Network Transceiver for Physical Layer

A thesis
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Daewung Kim

06. 08. 2016
Approved by

Advisor
Jae Joon Kim

Design of Automotive Communication Local Interconnect Network Transceiver for Physical Layer

Daewung Kim

This certifies that the thesis of Daewung Kim is approved.

06. 08. 2016

signature

Advisor: Jae Joon Kim

signature

Yunsik Lee

signature

Jaehyouk Choi

Abstract

Car electronic system have grown consistently based on the trend change of the automotive component. For advanced application, there is considerable demand for high specification as substitute for mechanical devices. The electronic components are suitable for satisfaction of vendor and consumer requirements.

There are various automotive communication for each application such as Controller Area Network(CAN), Local Area Network(LIN), FlexRay, Ethernet, etc. The automotive semiconductor is fundamental parts of the development trend for requirement trend based on vary communication. It has to endure artic condition for satisfaction of functional safety, because the automotive architecture must consider driver and passenger's safety to protect harmful condition. AEC Q-100 is one of the safety standard for requirement of prime supplier such as GM, TODOYA, Hyundai Motors, VOLVO, etc..

On the dissertation, it is main attention for implementation to satisfy standard of physical layer of LIN. Physical layer signal operating load can be described on International Standard Organization(ISO). There is under 20kbps input and output bit stream for communication, 5 us of overall system time constant and under 50% duty cycle.

It targets Local Interconnect Network's physical layer given by ISO 17987-4. ECU generate digital bits stream, transmitter makes LIN bus signal which is driving application. Under 40% of battery voltage, regarded as logical '0' which named Dominant state. Over 60% of battery voltage, regarded as logical '1', which named Recessive state. LIN bus signal apply voltage to receiver block. Receiver transfer bus signal to output RXD pin for MCU.

First implementation target complete signal data path to interconnection of input and output environment from ECU to application bus and application bus to ECU. It contains mode change option for resisting Electromagnetic Interference(EMI).

Second and third design has advanced architecture for protection and satisfaction of standard. One targets the design for protection of inrush current based on current cell approach. It has technique which is reducing way of unit current cell mismatch from conventional data converter. The other one is delay control technique of input and output bit stream. ISO 17987 gives delay margin for physical layer, developer should satisfy the restriction. The mechanism can be controllable delay control from internal digital blocks.

Contents

List of Figures

List of Tables

Abbreviations

BJT - Bipolar Junction Transistor

CAN – Controller Area Network

DAC - Digital to Analog Converter

ESA – Electronic Sub Assembly

EMI - Electromagnetic Interference

MOSFET - Metal Oxide Semiconductor Field Effect Transistor

LIN - Local Interconnect Network

OSI - Open System Interconnection

PCB – Printed Circuit Board

PRBS – Pseudo Random Bit Stream

ISO - International Standard Organization

IC - Integrated Circuit

Chapter 1

Introduction

This chapter demonstrate the number of automotive communication which cover their application. Many kinds of automotive communication contain their specification.

1.1. Automotive Electronics Technology

These days, automotive industry has been evolutionary change since convergence of information technology. Automotive usage coverage extend from only means of transportation to break and infotainment. Also, the intelligent safety technologies are applied to automotive for maximization of a driver's running stability[1] and ease. Convergence of mobile architecture is appropriate to control car information totally, driver can enjoy their contents. The car service will be developed standalone automobile to networked automobile platform.

Because of the trend, application of automotive electronic system is steady increasing. Automobile was mass assemble of mechanical engineering. After 2020, the automotive electric device will have growth rate of 7 % for the upcoming years all component[2]. Car is not machine anymore but huge architecture of electronics system. So credibility of software and hardware is more important than before these days.

The Electronic Sub Assembly means all of device and component that flows electrode their own. It covers from passive device such as register and capacitor to combined device which contains both sided PCB and mechanical structure. The ESA is essential component of automotive evolution. Now days, car is not mechanic but network communication system which contain wheel.

Table 1-1 shows category of intelligent automotive electronic system[3].

Category		**Technology**
Vehicle driving	Active Safety	Safety system
		Active restraint
		Autonomous navigation
		Automatic parking
	Active-Passive Safety Integration	Collision safety
		Harm damage prevention
Vehicle informatization	Automotive mobile communication system	Telematics, Navigation
	Automotive information system	Intelligent Information
		Vehicle mounted network
	Common infrastructure system	HMI, Embedded, HW,SW
Ease	Entertainment system	Digital AV system
	Comfort & Security	Security and safety

Table 1-1: Classification of automotive electronic technology

Like the categorization, strengthening of regulation and need of most advanced scientific technology from customer, there is ESA application is expanded continuously.

1.2. Automotive Semiconductor Technology

Automotive semiconductor contains sensor for information of automotive external and internal environment, ECU which controls engine, transmission and other actuator. For example, discrete device, microcomputer, custom IC and hybrid IC are category of the automotive semiconductor. .

Table 2-2 shows comparison of automotive semiconductor and normal.

	Consumer	**Industrial**	**Automotive**
Operating temperature	0 - 40 ℃	-10 - 70 ℃	-40 - 155 ℃
Life span	1-3 years	5-10 years	Over 15 years
Humidity	Low	Environment	0-100 %
Failure rate	3%	<<1%	Zero failure
Supply Commitment	2 year	5 year	30 year

Table 1-2: Automotive semiconductor reliability comparison[4]

Automotive semiconductor require higher requirement than normal semiconductor that is used on PC and mobile. Car functional safety related to save driver and passenger. Because of the reason, it should satisfy the requirement from AEC-Q100 which is automotive reliability certification.

1.3. Automotive Communication System

These days, there are many kinds of automotive communication. Figure 1-1 shows application of automotive communication. Controller Area Network covers high reliability application such as motor, ABS and transmission. Ethernet has highest data rate 100Mbps to cover infotainment, navigation, radar and camera system. It has wide bandwidth and inexpensive. Local Area Network has low specification for data rate. It has serial bus system and low cost. Also, applications of LIN are not related consumer's safety. Sensor system such as climate and computer is normal application from LIN.

Simply, CAN is dual wire, differential structure. LIN is single wire, single ended structure, low speed and low price. Table 1-3 shows the two similar automotive communication. LIN is a serial network protocol used for component communication in vehicle. The need for a cheap serial network arose as the facilities implemented in the car grew, while the CAN is too expensive to implement for every component in the car.

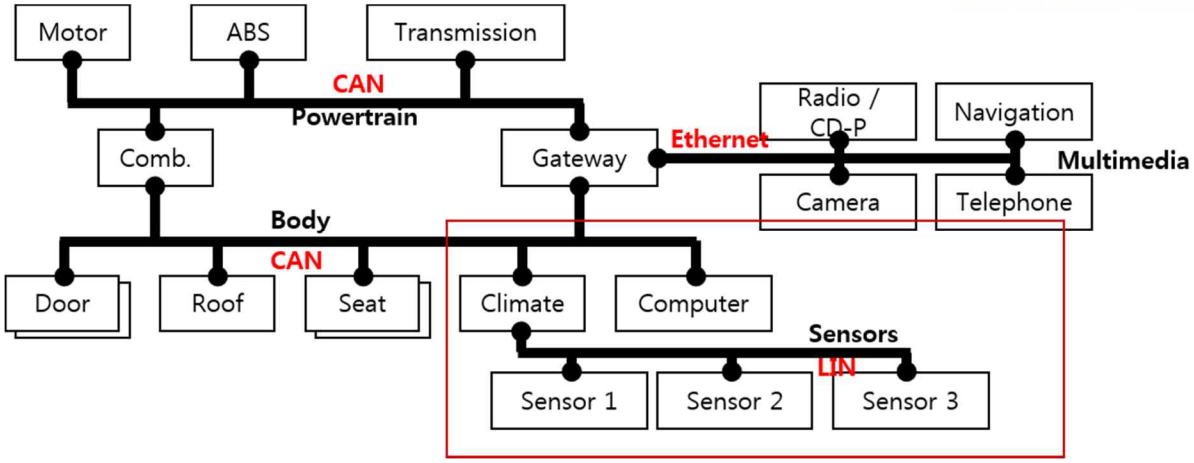


Figure 1-1: Application of automotive communication

Bus	CAN	LIN
Cost/Node [$]	3.00	1.50
Application domain	Powertrain, chassis	Sensors
Message transmission	Asynchronous	Synchronous
Architecture	Multi master	Single master
Medium	Dual wire[a] (twisted pair cable)	Single wire
Data rate	125Kbps-1Mbps	Max. 20Kbps
Access control	CSMA/CD	Polling
Latency	Load dependent	Constant
Error detection	CRC-15 (up to 5 corrupted bits)	Parity and checksum

Table 1-3: Comparison of CAN and LIN

Chapter 2

Local Interconnect Network

2.1. Background of Local Interconnect Network Transceiver

Table°1°—°LIN specifications applicable to the OSI layers

Applicability	OSI seven layer	LIN	Vehicle manufacturer enhanced diagnostics
Seven layer according to ISO°7498-1 and ISO/IEC 10731	Application (layer 7)	ISO 17987-1, ISO 17987-5	ISO°14229-1, ISO°14229-7
	Presentation (layer 6)	ISO 17987-5	vehicle manufacturer specific
	Session (layer 5)	ISO 17987-3	ISO°14229-2
	Transport (layer 4)	ISO 17987-2	
	Network (layer 3)		
	Data link (layer 2)	ISO 17987-3, ISO 17987-6	
	Physical (layer 1)	ISO 17987-4, ISO 17987-7	

Table 2-1: Standard classification

Local Interconnect Network is one of the network protocol. These days, communication system composed of layer structure[5]. Each layer has their own protocol, it communicates with each other system's layer. Other communication layers are not having an effects on the other layers. That means, the function influences only their own peer layer. Therefore it has OSI reference standards for each network layer function. The ISO give OSI seven layer standards for Local Interconnect Network from ISO 17987. ISO 17987 has their own classification of LIN. Table 1-1 shows classification of OSI layer for each standard documents.

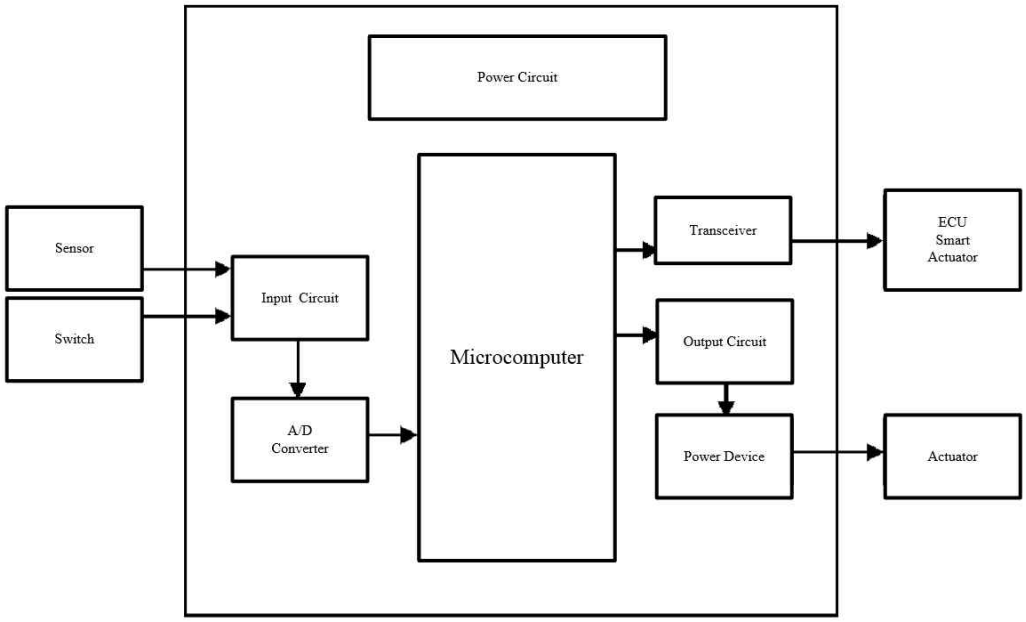


Figure 2-1: ECU block diagram[6]

Figure 2-1 shows block diagram of ECU. Almost automotive electronic parts contain ECU, process input signal, driving motor and actuator, interconnecting the information based on internal network protocol. Generally, ECU is composed of input processing circuit, A/D converter, microcomputer, power device and communication circuit. Semiconductor is main parts of the component. The ECU acts slave or master at automotive communication system.

This research targets LIN's physical that occupies first layer of the structure. The layer covers real signal communication. It defines real communication of device and terminal. Many kinds of electronical standard and bits synchronization are given by the layer. ISO 17987-4 and 17987-7 give specifications of physical environment for LIN.

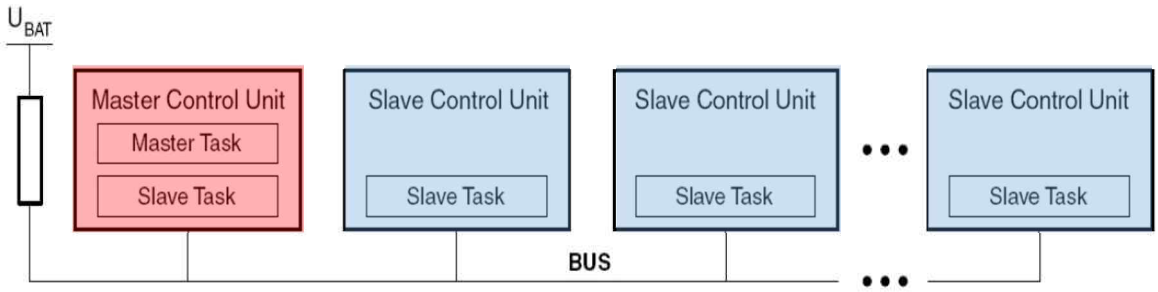


Figure 2-2: Master – Slave communication architecture

LIN has single master and multi slave structure like figure 2-2. Master transfers signal which satisfy frame standards for LIN to activate application. All of bus nodes share same signal that is generated by master's input bit stream. Bus signal's swing limited by automotive battery signal. Slaves take bus signal, generate bit stream and deliver their slave control unit. Finally, almost same bit stream which from master control unit's input will be delivered slave and activated their connected

application based on communication information. It permits 16 maximum node and 40 meter of maximum wire length. Based on the restriction, PHY layer architecture needs standards satisfaction for line capacitance and nodes.

2.2. General Configuration Design

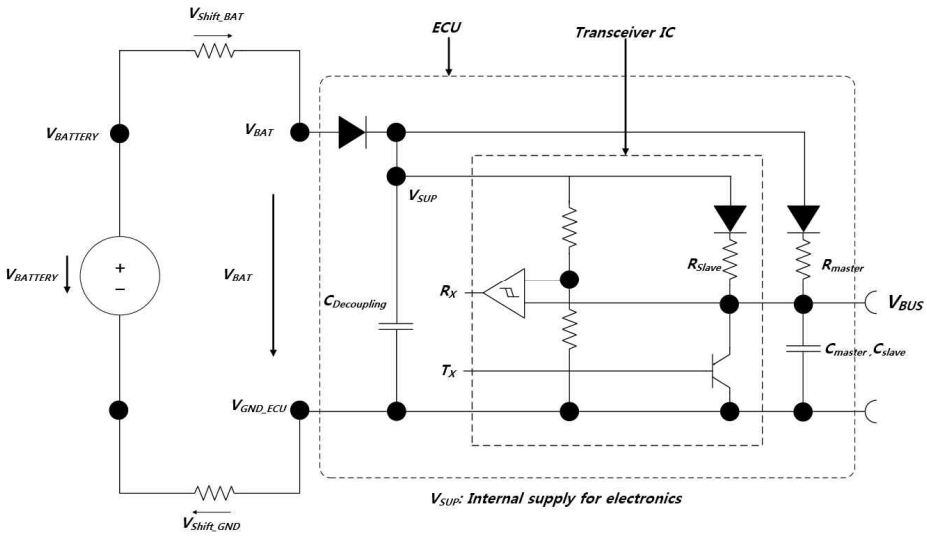


Figure 2-3: Definition of supply interface of Local Interconnect Network PHY

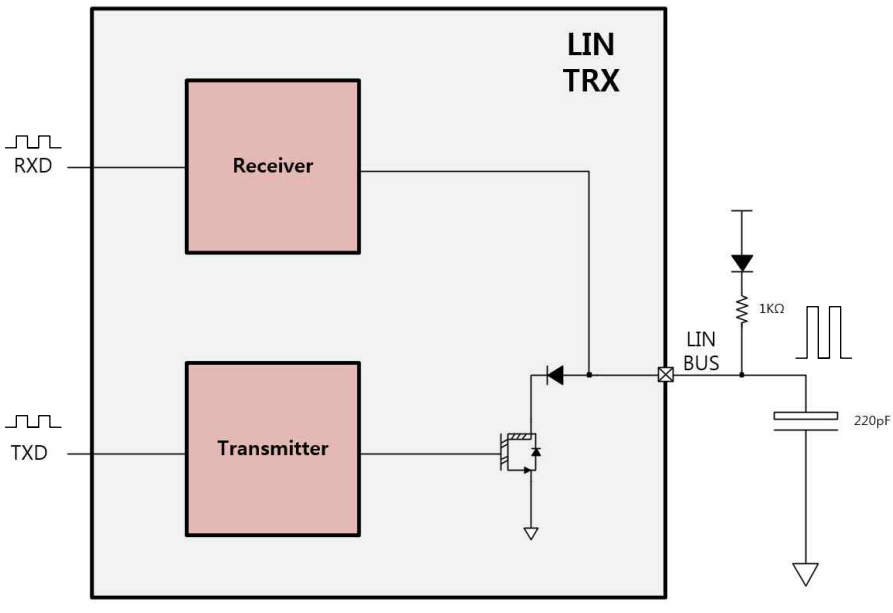


Figure 2-4: Simple structure of LIN transceiver

ISO 17987-4 gives basic physical interface of LIN from external power and signal line to internal transceiver IC like fig 2-3. It determines relation of ECU and IC. It must covers single ended bus node for each application. Same phase of bit stream,

TXD – LIN – RXD each are arranged. When power transistor turn on, LIN bus High. Inverse case, LIN bus low and the signal transferred internal receiver block. The architecture named open collector or open drain. Open collector and open drain structure share same node at BJT's collector and MOSFET's drain. In the LIN's single ended structure, they share bus node. When master's power transistor is turning on, bus node gets logic 'High'. It named 'recessive state'. Inverse case, when master's power transistor is turning off, bus node gets logic 'Low'. It named 'dominant state.

Internal and external diode is mandatory to maintain flow of current direction. It prevents damage from reverse current and protects internal device. Also, it is important for design transceiver IC to consider internal parasitic voltage drop based on diode and external connection states. When parallel value of pull up resistance is defined, the parallel value of bus node can be defined as below:

$$R_{BUS} = R_{MASTER} || R_{SLAVE\_1} || R_{SLAVE\_2} || R_{SLAVE\_3} || \dots || R_{SLAVE\_N} \quad (1)$$

External master resister 1k and internal slave resister 30k maintain parallel resistance value about 1kΩ. It can reserve internal value of current flow to power transistor and time constant of overall system.

The LIN transceiver IC is simplified like fig 2-4. Current design uses power MOSFET and selects open drain structure instead of power BJT. Transmitter block gets digital bit stream and control power transistor based on bit's phase. Power MOSFET is turning on and off for dominant and recessive state. Receiver block gets LIN bus's dominant or recessive state and transfer digital bit stream based on the state. Finally, ECU gets same phase digital bit stream like TXD signal from receiver block.

Chapter 3.

Implementation of Automotive Local Interconnect Network Transceiver

There are three design of LIN transceiver. All of them are based on LIN PHY standard which is implied on ISO 17987-4 and 17987-7. First one is basic signal path with control block which implies state diagram. Second and third are advanced structure of first design. Second design targets protection of unexpected current spike. Third one targets specification of delay margin which offered at LIN communication standard. All of design are aim to satisfy standard and functional safety for automotive application of high voltage region.

3.1. LIN Transceiver Signal Path System Design

First LIN transceiver design is aim to complete signal path of bit stream. The system needs to specify specification table of ISO 17987-4. Data path of low voltage region and protection of high voltage region which can damage internal transceiver IC is mainly considered part of the design.

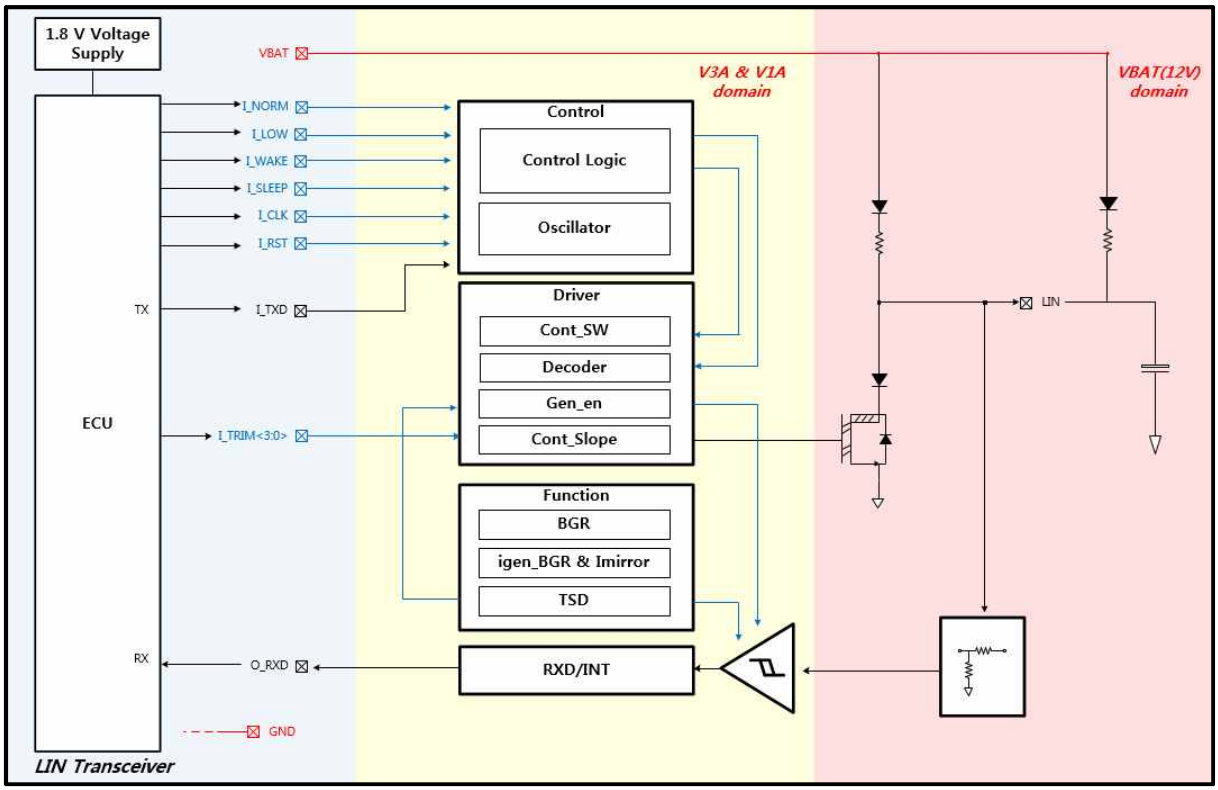


Figure 3-1: LIN transceiver basic implementation block diagram

Fig 3-1 is block diagram of signal path design that implies ECU – LIN transceiver – BUS nod connection structure. The block shows data transmission that pass ECU - Control – Driver – Power MOSFET – LIN bus – Divider – Comparator – RXD/INT – ECU. An ECU makes bit stream for control specific application that apply for LIN communication. The control block acts internal state diagram to avoid unwanted mode change. The driver controls power MOSFET based on TX signal. Also driver block adjusts power transistor's gate charging and discharging speed. It determines turning off and turning on time

of power MOSFET, that's time of threshold departure time will be controlled slower and faster. The Function block has bias injection for analog design and thermal shutdown for over temperature detection. The receiver which is composed of voltage divider, comparator and RXD/INT gets the bus data and accumulate the signal for ECU. It adjust LIN's high voltage for appropriate voltage region that ECU can be processing.

SIGNAL NAME	TYPE	DESCRIPTION
VBAT	power	12V Power from battery
V3A	power	3.3V Power for analog block
V1A	power	1.8V Power for digital logic
GND	ground	Ground
LIN	analog	Bus signal
I_TXD	input	Input digital bit stream
I_NORM	input	Normal slope mode enable
I_LOW	input	Low slope mode enable
I_WAKE	input	Wakeup enable
I_SLEEP	input	Sleep enable
I_TRIM[3:0]	input	Rise and fall time trimming
O_RXD	output	Output digital bit stream
I_CLK	input	Reference clock
I_RST	input	Reset

Table 3-1: Signal definition for MCU integrated version

3.1.1. Control Block Design

The control block contains clock synchronized sequential logic. Internal sequential logic determines state based on previous state and external binary signal. Combinational logics are made of storage device such as flip-flop are save pre-state and affect next state. The clocked synchronized circuits compose flip-flop and feedback path. It is appropriate for register array and counter to make full state sequence. That is synchronized by internal reference clock which from oscillator circuit.

The state gives four number of mode change such as sleep mode, standby mode, normal slope and low slope mode. Standby mode prepares activation of transceiver enable. Normal slope mode gives steep rise and fall time to fast transition. Low slope mode gives gradual edge time than normal slope mode. In case of low slope mode, it has high immunity of external unwanted EMI. Sleep mode deactivate operation of transceiver IC to reduce unnecessary power consumption.

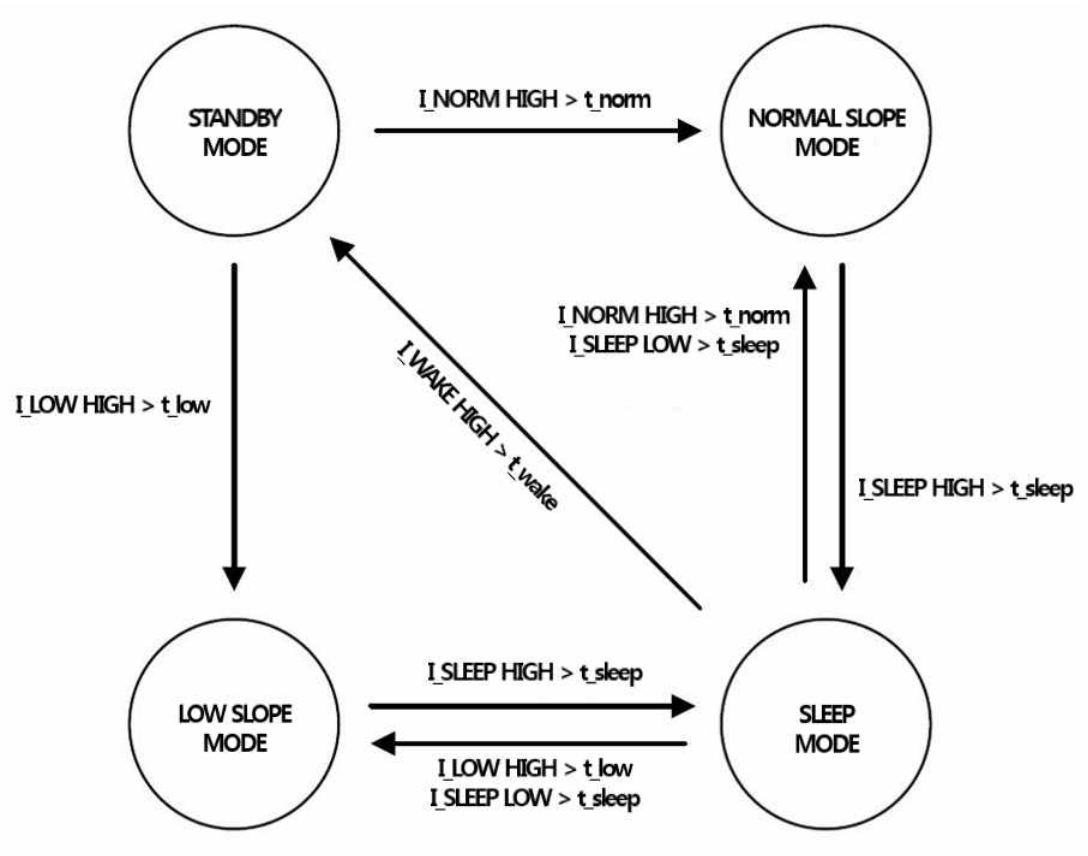


Figure 3-2: State diagram of Control block

	I_WAKE	I_NORM	I_LOW	I_SLEEP
Normal slope mode	1	1	0	0
Low slope mode	1	0	1	0
Sleep mode	1	X	X	1

Table 3-2: State table of Control block

After designated time, control block enters the signal for mode change. Fig 3-2 shows mode change state diagram for control block. After turn on, control block generates signal to maintain sleep mode. When apply wake up signal 'I_WAKE', the mode is changed to standby after few micro seconds. Waiting time for mode change 't_wake' which designated few micro seconds.

State control is activated by external enable signal. Table 3-2 show truth table of control block logic. In case of 'I_NORM' activation, normal slope mode applied. When 'I_LOW' activation, low slope mode applied. If 'I_SLEEP' enabled, sleep mode applied to logic and almost internal block stopped to reduce power consumption. Although other mode change signal enabled, sleep mode doesn't affect and maintains its mode. Mode change needs to apply after wake up mode, it can be controlled 'I_WAKE' signal from external controller or pin.

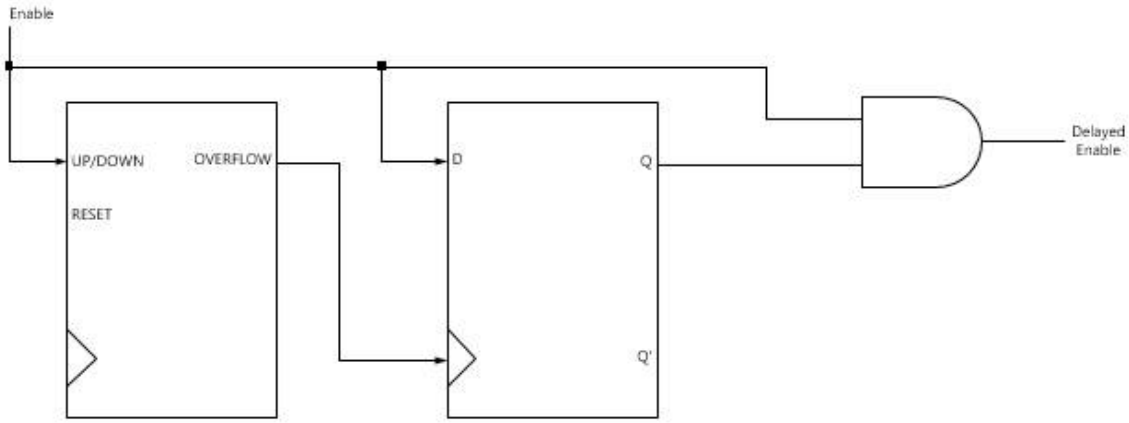


Figure 3-3: Delay time setup schematic using counter and d flip-flop

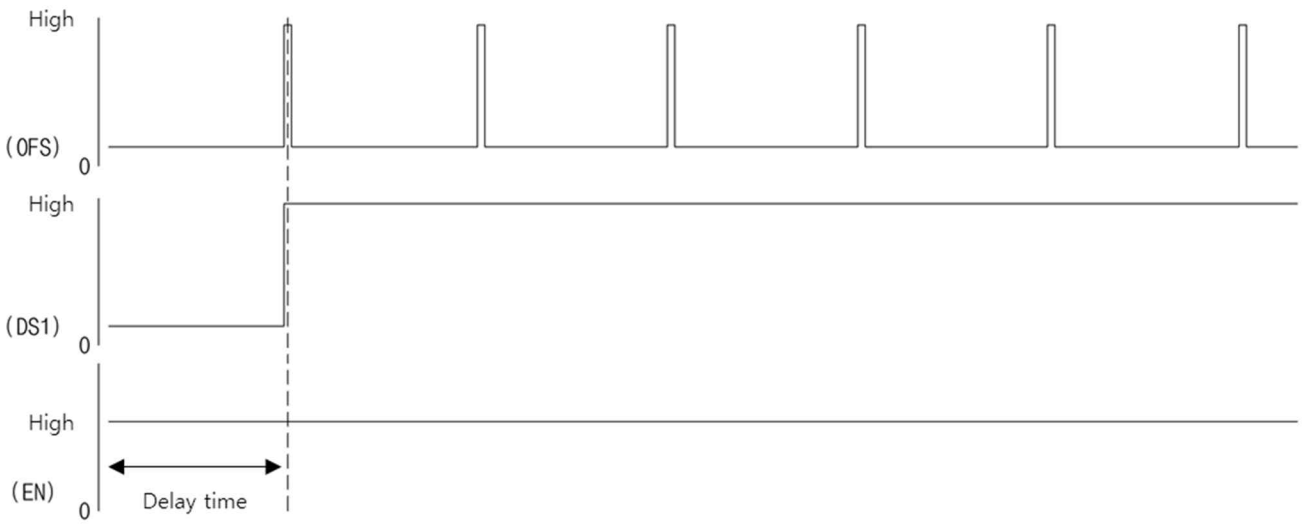


Figure 3-4: Delayed signal controlled by counter's overflow flag

The waiting set time of mode change is controlled by counter circuit. Fig 3-3 shows delayed enable circuit with counter and d flip-flop. Overflow signal is output by n bit counter which is synchronized with oscillator's reference clock. The signal flag arise after the product value that is expressed as $T \times 2^n$ second. T is clock period and n is counter's controllable bit. From reset to delay, overflow signal arise, it is injected to d flip-flop's clock. When enable signal that is active high maintained, d flip-flop generates the delayed enable signal. And gate gets input signal from d flip-flop's output Q and enable signal, finally deliver delayed enable signal to next logic.

3.1.2. Driver Block Design

Driver controls power MOSFET's gate charging and discharging. The design provide two option of slope control. First one is selection of normal and low slope mode. From external mode change signal, control block generates signal for each mode. Second is segmented selection option of rise and fall time. A number of current cell is selected by thermometer decoder in case of switch controller enable.

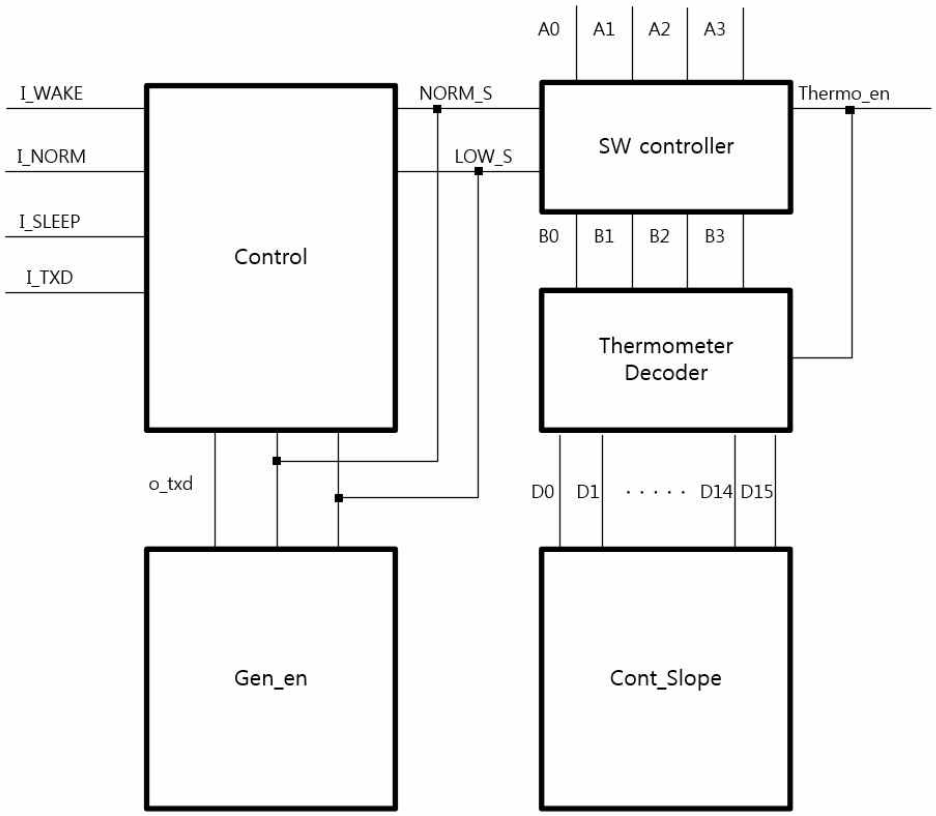


Figure 3-5: Control block connected driver function

Fig 3-5 shows driver sub block which connected previous control logic. SW controller block gets enable signal from external pin or control block's slope control mode enable output. In normal condition, mode change only depends on control block's output signal 'NORM_S' and 'LOW_S' which is activated by state of external mode enable pin I_WAKE, I_NORM, I_SLEEP. If external enable signal activated, thermometer decoder block is worked based on pin A0, A1, A2, A3. Also switch controller makes enable signal for IC's internal sub blocks to turn on and off. If there is no active high slope control enable and switch controller input, all sub blocks are not operate. Gen_en block can generate enable signal for other sub block to

transfer bit stream. The most important thing is slope control function. Cont_Slope block gets control signal from thermometer decoder.

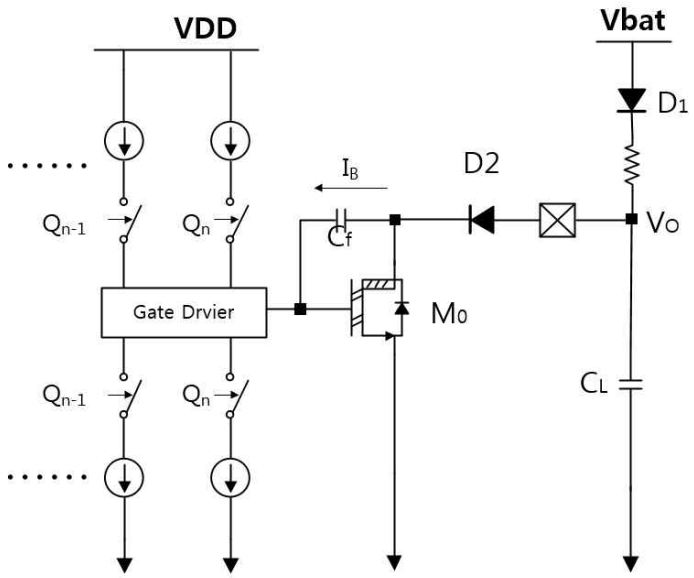


Figure 3-6: Slope control for trimming edge time of LIN bus

Slope control function is composed of current cell array which can inject current to gate driver. Fig 3-6 show schematic of structure for LIN bus slope control. Gate driver controls power MOSFET's gate charging and discharging speed based on injected current from high and low side current mirror array. Charging speed is effected by high side current cell's quantity. Fall time of LIN bus depends on the charging speed. Discharging speed is effected by low side current cell's quantity. Rise time of LIN bus depends on the discharging speed. Charging and discharging speed determine arrive time of power MOSFET's threshold voltage. Also capacitance of feedback capacitor C_f affects output voltage value of LIN bus. The relation of equation among feedback current I_B, feedback capacitance C_f, common source gain A_v is expressed as below[7]:

$$C_f \frac{d\left(V_{C_f}(t)\right)}{dt} = I_B \Rightarrow V_{C_f}(t) = \frac{I_B}{C_f}(t - t_0) \tag{3}$$

$$V_O(t) = \left(\frac{|A_v|}{1+|A_v|}\right) V_{C_f}(t) \fallingdotseq V_{C_f}(t) \tag{4}$$

Output voltage depends on feedback capacitor's voltage value. If common source has large value of gain, little value of error can be negligible.

3.1.3. Receiver Block Design

Receiver block convert voltage region from high voltage to low voltage and prevent unpredictable output logic value change from noise. The design use 3.3 volt analog region, so battery voltage region needs to change low voltage. This can be represent from the simple schematic in Fig 3-7. Voltage divider needs to protect receiver part from high voltage which overs

device endurance. Because the process doesn't provide rigid device which gate condition to protect over 12 volt that from LIN bus.

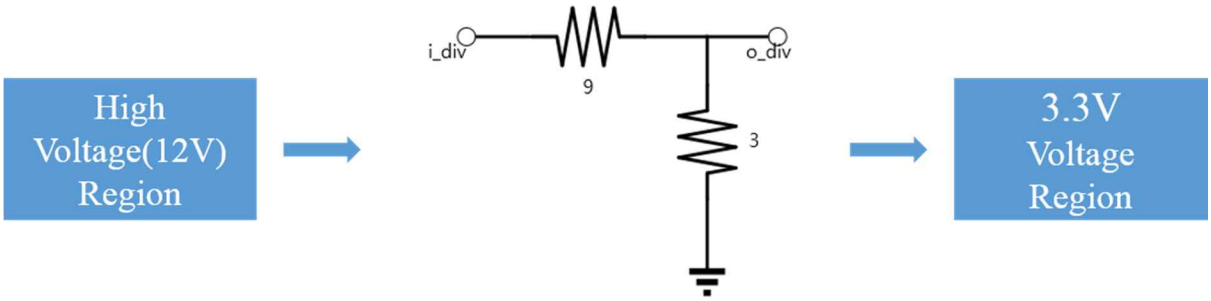


Figure 3-7: Simplified voltage divider structure

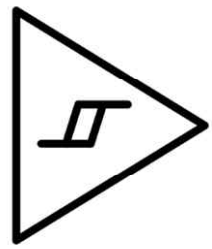


Figure 3-10: Symbol

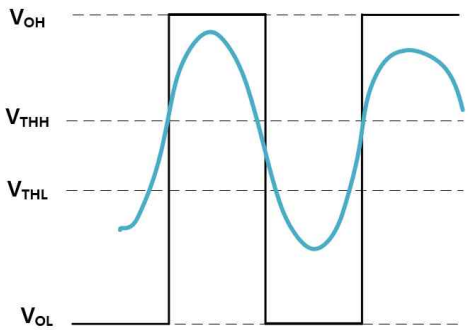


Figure 3-10: Hysteresis comparator waveform

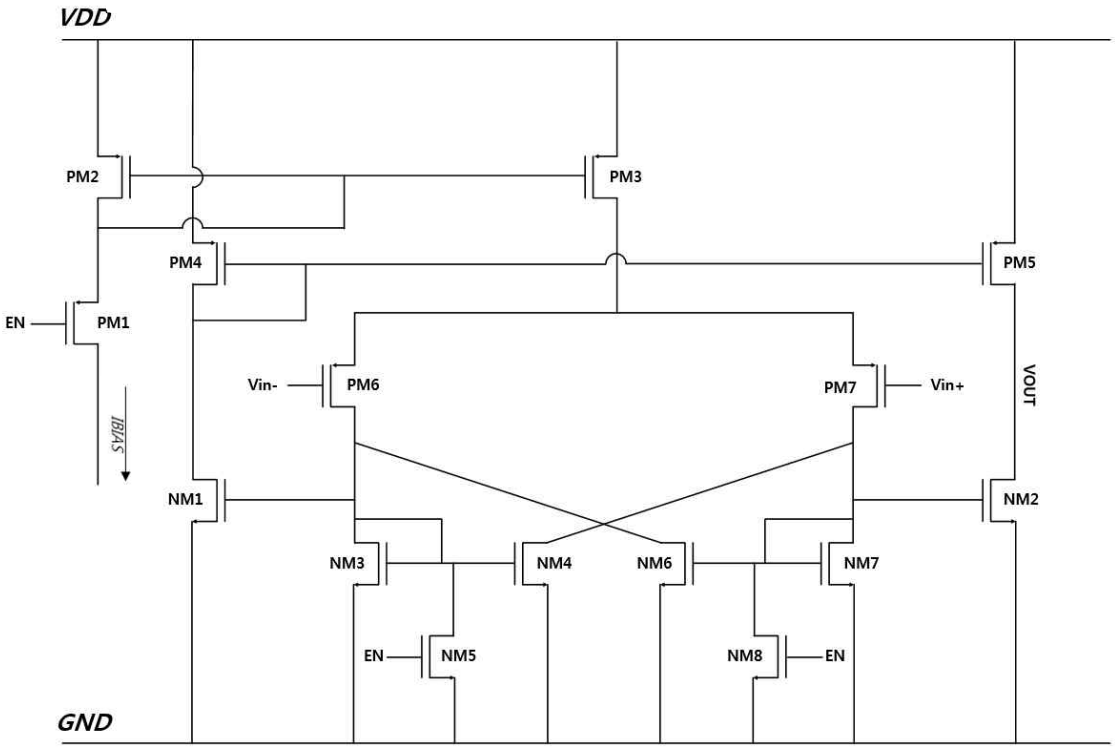


Figure 3-10: Hysteresis comparator schematic with controllable enable

Hysteresis comparator can endure risk of bit error in case of noise. The noise can be generated from input voltage which come from LIN bus has multiple transition. To cover receiver hysteresis voltage V_{hys} that from table of ISO 17987-4's parameter 20.

Using hysteresis property, waveform gets high state over certain voltage value output and low state under the other certain voltage value[8]. The property can prevent vibration from noisy signal. Like fig 3-9, it operates at low threshold voltage(V_{THL}) and high threshold voltage(V_{THH}). So, it is able to protect fine change of input voltage value. PM1, NM5, NM8 are controlled by enable signal which is activated low.

Let V_{in-} is connected reference voltage.

1) $V_{in+} > V_{in-}$

   PMOS PM6 is dominant so, large current from PM3 flows PM6 path than PM7. Drain of PM6's nodes are turn on simultaneously. NM1 turns on and PM4-5 current mirror acts. Finally V_{OUT} connects with VDD and maintains logic 'High'.

2) $V_{in+} < V_{in-}$

   PMOS PM7 is dominant so, large current from PM3 flows PM7 path than PM6. Drain of PM7's nodes are turn on simultaneously. NM2 turns on and PM4-5 current mirror does not act. Finally V_{OUT} connects with GND and maintains logic 'Low'.

3) V_{THL}

   Size of NM4 determines low threshold voltage of comparator. Current flow to PM4 is that's products of $\left(\frac{W_{NM4}}{W_{NM3}}\right)$ which from PM7's drain. If NM4's width higher, although low voltage is injected to PM7's gate, appearing low value V_{SG} of PM6, V_{OUT} can be high. It means threshold is lower than before.

4) V_{THH}

   Size of NM6 determines low threshold voltage of comparator. Current flow to PM4 is that's products of $\left(\frac{W_{NM6}}{W_{NM7}}\right)$ which from PM6's drain. If NM6's width higher, PM7'current injection is lower. So, higher V_{SG} needs to drive PM7 and maintains logic 'High'. It means maximum V_{INP} voltage value which is endure logic 'High' is higher than before.

3.1.4. Simulation Result

Fig 3-11 shows typical environment at analog 3.3V, digital 1.8V and 12V battery voltage. Input and output bit stream is 20kbps to apply class-α from ISO 17987. TXD and RXD bit stream swings 0 to 1.8 V. LIN bus has dominant or recessive state based on 12V. Region ① is normal slope mode on. It has steep edge time and fast transition. Region ② is sleep mode on state. There is no signal path transfer because of internal power MOSFET turned off. After entering sleep mode, same phase output can't be seen. In case of region ③ is low slope mode on. It has gradual slope of rise and fall time than before mode.

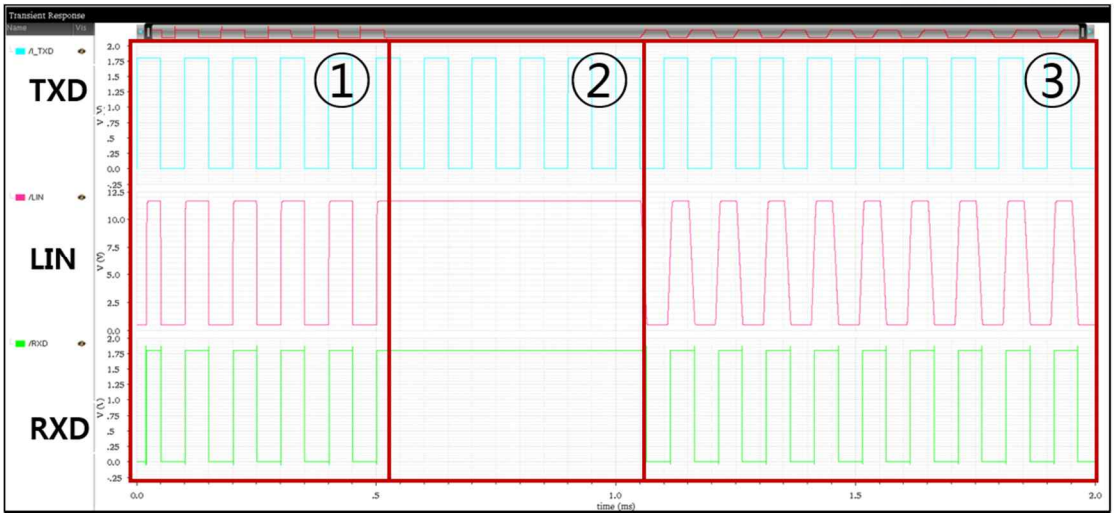


Figure 3-11: Cadence simulation waveform of mode change

Specification	Value	Unit
Battery Voltage	8 ~ 18	V
Voltage Guarantee	0 ~ 40	V
Digital VDD	1.8	V
Analog VDD	3.3	V
Data Rate	10.4 / 20	kbps
System Clock	800	kHz
Peak current	37	mA
Current Limitation	40 ~ 200	mA
Leakage Current	1.5 (Dom) ~ 16.5 (Rec)	μA

Duty cycle	48 – 52	%
Max Propagation Delay	0 ~ 6	us
Time constant	1 ~ 5	us
Receiver symmetry	-2 ~ 2	us
Master Capacitance	220	pF
Slave Capacitance	220	pF

Table 3-3: Specification result of signal path design

Time Characteristics					
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
$t_{\_wake}$	Time from sleep mode to standby mode	18.75	20	20	us
$t_{\_norm}$	Time for mode change to normal slope mode from others	3.75	4	5	us
$t_{\_low}$	Time for mode change to low slope mode from others	3.75	4	5	us
$t_{\_sleep}$	Time for mode change toward sleep mode and away from sleep mode	3.75	4	5	us
$t_{\_clk}$	Reference clock period	-	1.25	-	us

Table 3-4: Time characteristics of control block

3.1.4. Layout Result

Fig 3-11 shows top layout with core and pad connection. Magnachip AP18E50 process is used to complete design from low voltage to high voltage. That occupies 1900 micro meter by 1580 micro meter. There are thirty eight pad with high voltage IO for measurement.

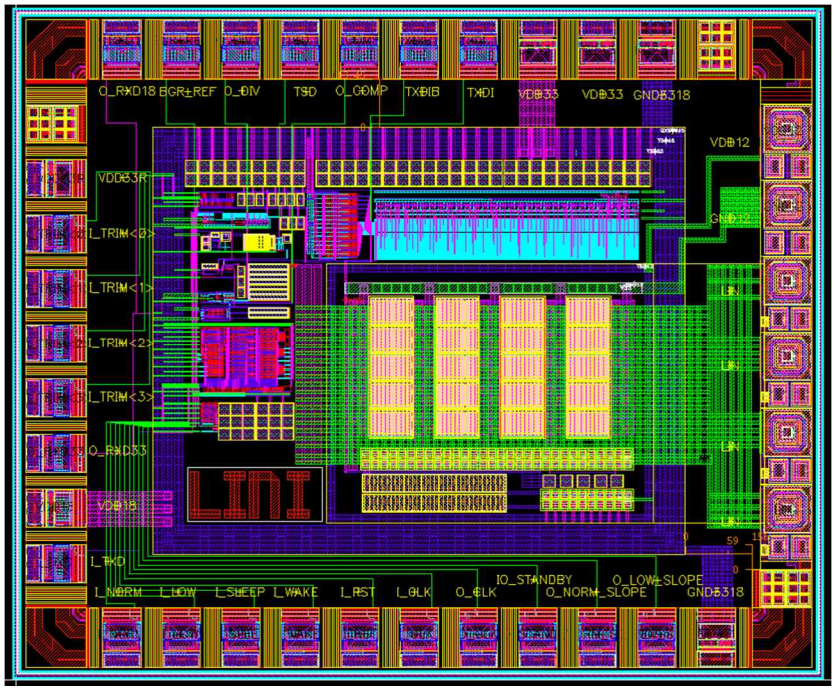


Figure 3-12: Top layout of LIN transceiver standalone version

3.2. Divided Power MOSFET design for Open Drain Function

The proposed design suggests protection technique for IC which control open drain driver structure. Appended protection technique is main approach of the design.

3.2.1. Technical Challenges & Approaches

Power MOSFET connected bus node which needs to cover high voltage from battery. When device is first turned on, a large amount of current flows that exceeds the steady-state value. Also, in case of abnormal low resistance, there is high current injection appeared. This current is called an inrush current[9]. Fig 3-13 shows inrush current appeared when IC turned on. Unpredicted condition make current spike and it can damage transceiver IC. Also, it makes unwanted noise and derive EMI issues.

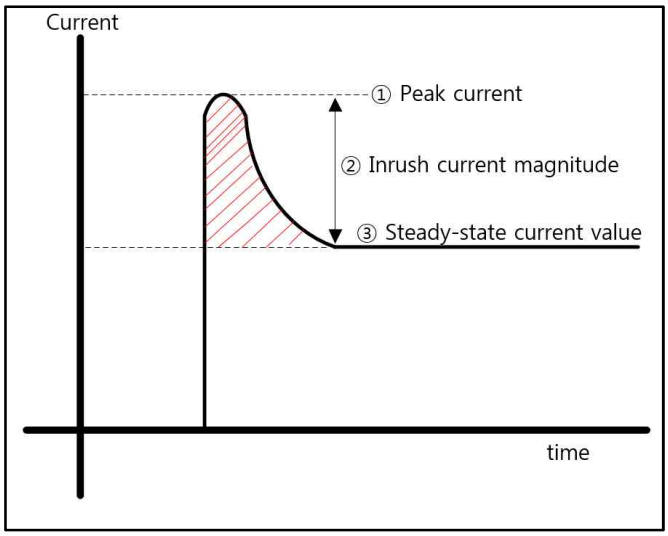


Figure 3-13: Inrush current problem in IC

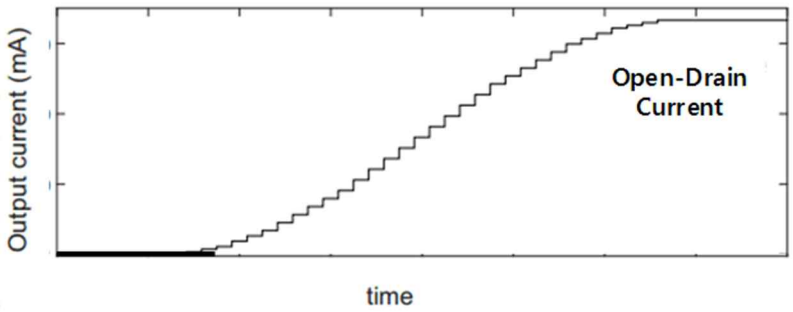


Figure 3-14: Spread current value for peak current

Design issue is technique to spread unexpected current which can be dangerous event of connect device from bus nodes. Fig 3-14 shows stepwise current rising. These days, many automotive IC manufacturer such as Infineon, NXP, Texas Instrument design LIN transceiver's bus node controlled by open drain structure. In the design, open drain structure regarded as current source in case of state change transition, such as dominant to recessive or recessive to dominant. The design targets

two. First one is dividing one current cell to a number of that[10]. Second one is convergence LIN and reducing current cell mismatch technique from current steering DAC.

3.2.2. Concept of Divided Power MOSFET

Also only one current source may has probability of incorrect activation from process mismatch. In other words, one current source has to endure all unwanted external issue. The approach is split big size power MOSFET to a number of small size power transistor like current cell array. A (W / L) Size of power MOSFET is divided into n number of unit cell size ($\frac{W}{n}$ / L). Fig 3-15 can be shown split concept for open drain.

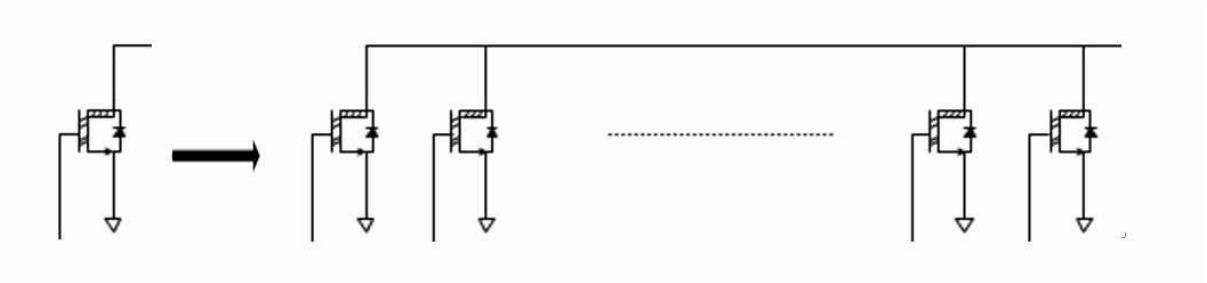


Figure 3-15: Concept of split power MOSFET

3.2.3. Concept of Dynamic Element Matching.

It is the technique for digital-to-analog converter to select each current cell randomly. Normal case of bit input, only connected the number of current cells are activated. After activate on DEM function, turn on the number of current cell randomly. If current cells are turned from bit input, randomizer scramble the connect path. The number of cell turned among the internal $k \cdot N$ numbers current cell array.

The technique can reduce probability of selecting mismatched current cell. Because of process variation, current cell mismatch is usually occurred. If specific input bit connected errored current cell, they occurred current mismatch when turning on. After DEM, it has probability to avoid selecting mismatched unit current cell. Finally, output can be reduce influence of errored signal.

3.2.4. Divided Power MOSFET Implementation with Signal Path Structure

Main approach is convergence dividing power MOSFET and select using Dynamic Element Matching. The most important thing is dividing power MOSFET like current cell and reduce the mismatch from introduction of the technique. It contains mixed two technique on the basic LIN transceiver signal path. The design come from fig 2-3's simple structure.

Fig 3-15 shows block diagram of full structure. All of internal analog block's reference current comes from **'BIAS'** block. It sends current to activate block which needs current driving except for high voltage region. '**Oscillator**' makes reference

clock for system driving. Internal inverter arrays compose ring structure and make fast transition to generate square wave. '**Clock divider**' block gets reference clock from oscillator. It split pulse signal to expand sort of selectable clock based on reference. The block makes output pulse signal which gets the value of input frequency's 1/n and multiple n of input period. It composed of JK flip-flop array like n-bit digital binary counter. The divided clock period is time step width of unit current injection. '**Clock Selector'** creates '**Shift Register**'s reference clock 'clk_s' to synchronize. '**Binary Decoder**' generates controllable enable output to select clock from clock divider.

A0	A1	A2	D0	D1	D2	D3	D4	D5	D6	D7	clk_s
0	0	0	1	0	0	0	0	0	0	0	clk0
0	0	1	0	1	0	0	0	0	0	0	clk1
0	1	0	0	0	1	0	0	0	0	0	clk2
0	1	1	0	0	0	1	0	0	0	0	clk3
1	0	0	0	0	0	0	1	0	0	0	clk4
1	0	1	0	0	0	0	0	1	0	0	clk5
1	1	0	0	0	0	0	0	0	1	0	clk6
1	1	1	0	0	0	0	0	0	0	1	clk7

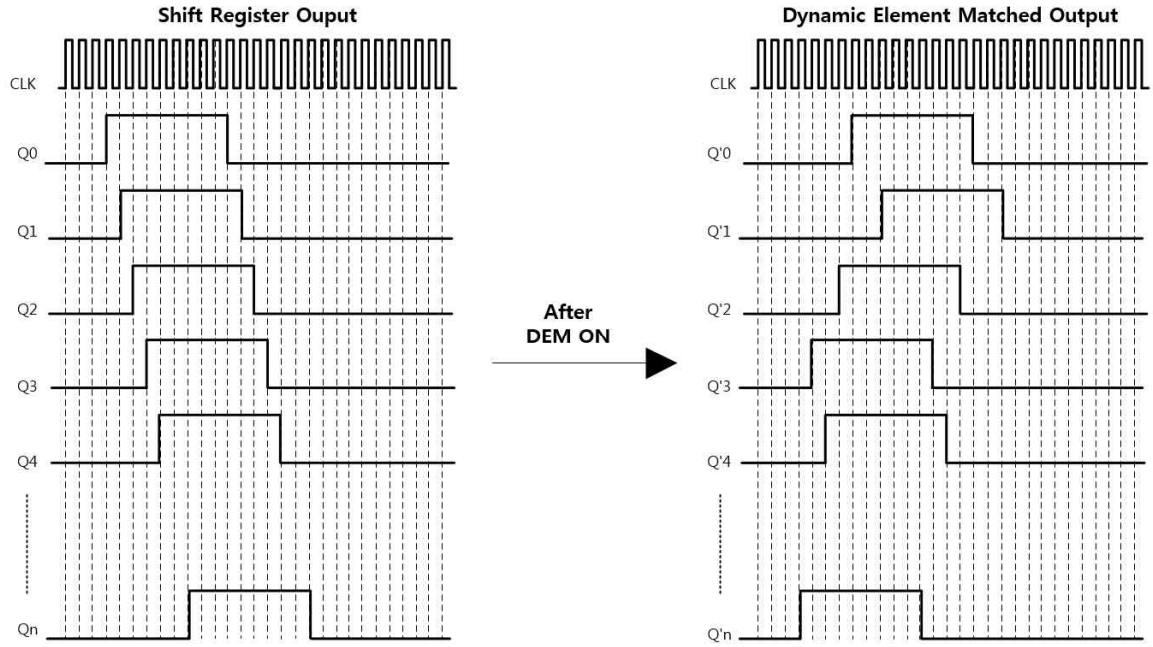
Table 3-5: Truth table for clock selector

Relation of clock divider and binary decoder truth table given by table 3-3. Like the truth table, clk_s is chosen by binary decoder's A0-A2 and D0-D7. Each binary decoder output determines clock period for stepwise current rising and falling. The current maintains steady state high or low, power MOSFET turn on or off.

Shift register generates enable signal for turning on switch. The pulse signal clk_s can be used for synchronization of shift register's internal flip-flop series arrangement. Fig 3-16 shows switching signal for turn on power MOSFET unit current cell. First waveform means shift register output. D input of first flip-flop gets bit stream TXD signal. There are n-number of output shifted on-off signal. If TXD is changing low to high, shift register makes output Q_k logic high state. Adversely, TXD is changing high to low, shift register makes output Q_n logic low state. Time delay that based on reference clock clk_s signal is appeared between Q_k and Q_{k-1}. In case of lengthened of decreased reference clock period, delay time of Q_k and Q_{k-1} is also lengthened or decreased.

First turn on signal Q_0 to last one Q_n determine all power MOSFET activation. That is to say, if all of shift resister output maintain high state output, all power MOSFET turn on, so it's common drain which is connected bus takes dominant

state. On the other hand, if all of shift resister output maintain low state, all power MOSFET turn off, so it's common drain which is connected bus takes recessive state.



(1) (2)

Figure 3-16: Output signal from shift register and dynamic element matched signal

Second wave form of fig 3-16 shows dynamic element matched shift register output. After '**DEM'** turns on, every signals enabled on randomly. N-number of Q_k signals are scrambled by DEM's randomization logic. It composed of random number generator and multiplexer array for mixed output. Output Q_k' are randomly scrambled signal than previous normal shift register output. Each signals are used to enable signal for each power MOSFET current cell.

'**SW Selector**' block can be trimming function for each unit cell's current driving. It is prevention approach for difference value of current cell to match preferred design result. Each switch of MOSFET's gate is connected SW selector block's output signal. All of them are connected 2 by 2 binary decoder, so cell switches of MOSFET are selectable. Ones of them are activated based on switch selector's binary output.

Next stage, a number of divided power MOSFET are connected same drain. After each switch transistor turns on, current driving at each clock signal at shift register's. They are linked protection diode for reverse current prevention. That's anode is connected external LIN bus node.

LIN bus signal from battery voltage makes transition high to low and low to high. Voltage divider gets the signal and induce voltage drop to low voltage region. Hysteresis comparator outputs logic high and low for ECU to transfer data bit

stream.

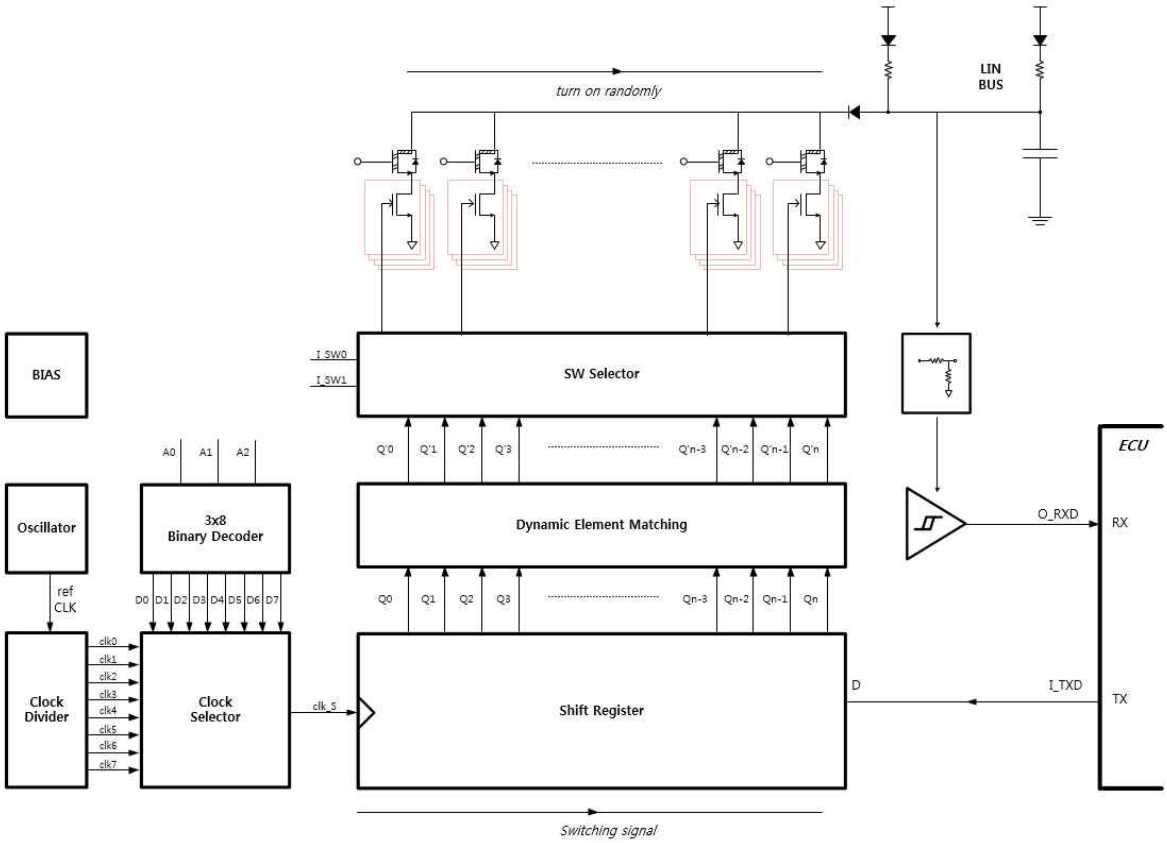


Figure 3-17: Full structure of convergence DEM and power MOSFET current cell

3.2.5. Simulation Result

Fig 3-18 shows waveform of conventional signal path based on environment of table 3-6. TXD –LIN – RXD has same phase with delay. Fig 3-19 shows transient waveform of LIN bus current at each temperature condition. In case of transition low – to – high, the stepwise current rising is stacked up before high steady state. Inversely, in case of transition high – to – low, the stepwise current falling is stacked down before low steady state.

Simulation Environment	Value	Factor	Value
Transient	0 – 0.12 ms	Edge time	2.765 – 3.3 us
Corner	TT	Max Peak current	11.21 mA
Temperature	-40, 27, 150 ℃	Max Steady State current	10.86 mA
Performance Result	Spectre	Max Current step	0.882 mA

Table 3-6: Simulation environment

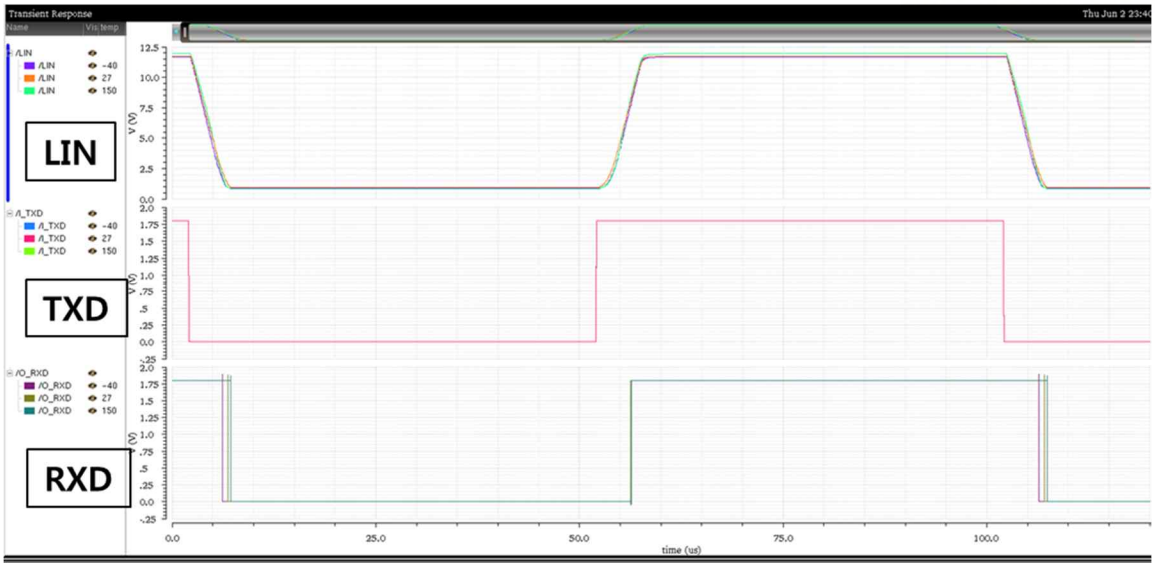


Figure 3-18: Signal path waveform of the divided power MOSFET

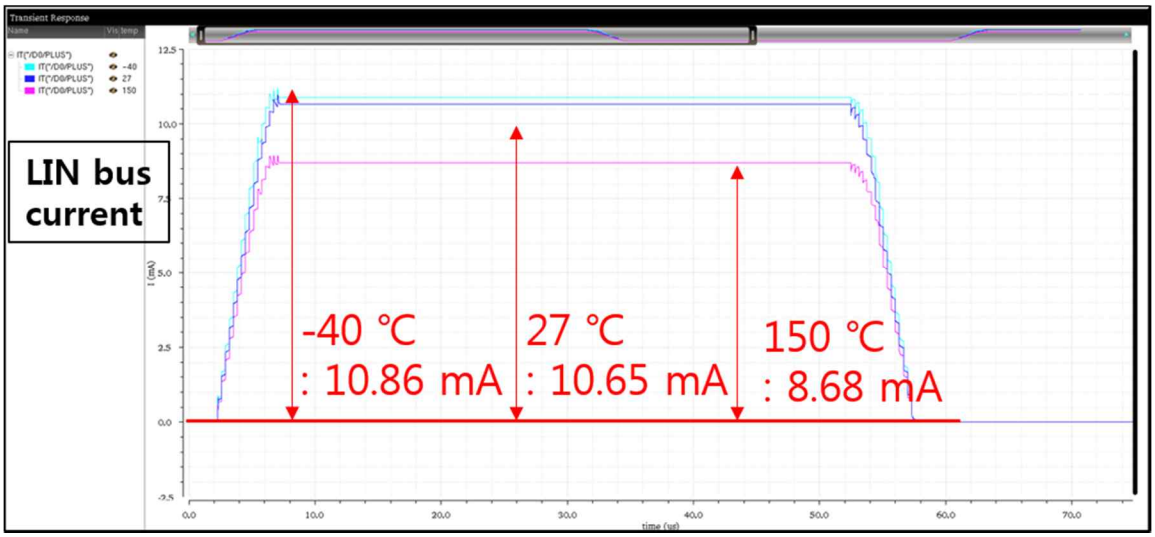


Figure 3-19: Stepwise current transition low to high and high to low

Case	SS			TT			FF			unit
Temperature	-40	27	150	-40	27	150	-40	27	150	℃
Peak current(A)	0.394	0.431	0.501	0.6139	0.6547	0.7151	0.867	0.934	0.981	mA
Average/RMS Current(A)	0.352	0.384	0.433	0.4989	0.5313	0.5895	0.702	0.736	0.8	mA
Peak current(D)	20.95	2.829	16.9	33.37	29.85	30.05	8.159	46.44	36.94	mA
Peak reverse current(D)	0.455	0.4527	0.4468	0.4703	0.4678	0.4565	0.429	0.476	0.438	mA
Average/RMS Current(D)	0.733	0.464	0.714	0.9423	0.9471	2.342	0.994	1.447	2.132	mA
LIN BUS(clk 120n)										
Rise time	4.009	3.66	2.771	2.7652	2.96	3.243	2.132	2.32	2.559	μs
Fall time	4.027	4.397	3.201	2.806	3.007	3.368	2.427	2.62	2.907	μs
Knee freq	0.12471	0.13661	0.18044	0.18081	0.16891	0.15417	0.23452	0.21551	0.19538	MHz
current step	0.602	0.501	0.591	0.882	0.513	0.772	1.189	1.084	0.916	mA
Peak current(H)	9.055	7.948	7.035	11.2104	10.984	8.939	11.61	11.639	11.503	mA
Steady State Current(H)	9.003	7.935	6.795	10.8691	10.6528	8.684	11.25	11.2861	11.1713	mA
DELAY										
TXD- RXD	3.25	3.42	4.24	4.218	4.169	4.23	5.532	6.146	6.329	μs

Table 3-7: Electric specification of the design

3.2.6. Layout Result

Fig 3-11 shows top layout with core and pad connection. Magnachip AP18E50 process is used to complete design from low voltage to high voltage. That occupies 2280 micro meter by 1890 micro meter. There are 41 pad with high voltage IO for measurement.

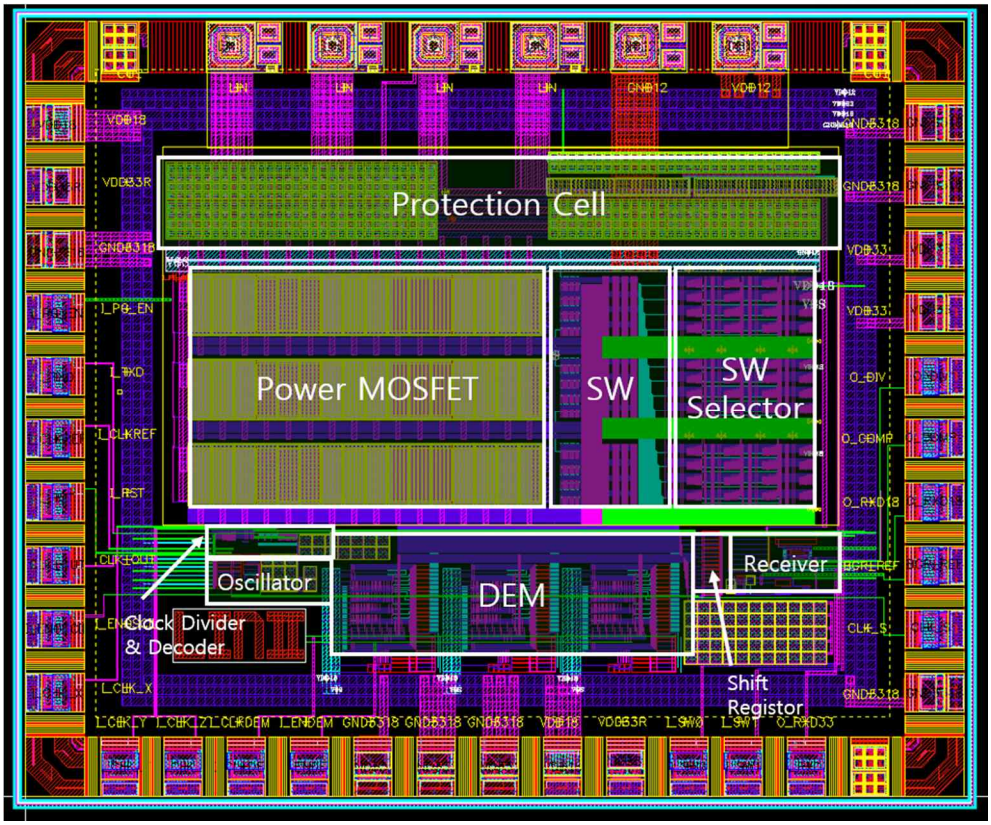


Figure 3-20: Top layout of divided power MOSFET approach

3.3. Auto Slope Control using Propagation Delay Detection

This part describe Local Interconnect Network LIN bus edge time control through internal cell delay control. Unwanted time difference of input and output bit stream occurs from cell delay. Table 3-8 shows electric AC parameter for transceiver's receiver. Parameter 31 says propagation delay margin at proposed conditions. The design targets rise and fall time control, at the same time, satisfy delay margin that is described by physical layer standards.

Table 11 — Receiver electrical AC parameters of the LIN electrical physical layer

Number	Parameter	Min.	Typ.	Max.	Unit	Comment / condition
LIN receiver, RXD load condition (C_{RXD}): 20 pF; (if open drain behaviour: R_{pull_up} = 2,4 kΩ)						
Param 31	trx_pd	---	---	6	µs	propagation delay of receiver
Param 32	trx_sym	-2	---	2	µs	symmetry of receiver propagation delay rising edge with respect to falling edge

Table 3-8: Receiver electric AC parameters from ISO 17987-4 Table 11

3.3.1. Technical Challenges & Approaches

The delay of transceiver IC comes from internal cell delay. The cell day is accumulated by passing each blocks. The delay is mainly appeared by LIN bus. The LIN bus signal has high voltage region over 12V comes from automotive battery. It is slow for transition to change dominant-recessive and recessive-dominant. High voltage state to almost ground state is very slower than normal voltage state change such as 0V to 1.8V or 0V to 3.3V.

The delay can be changed some reason. First, driving current value of current source which is shown fig 3-6 is not accurate like simulation result. After fabrication, there are mismatched current cell appeared[11] based on semiconductor manufacturing environment. Because of process inaccuracy, the possibility of difference can be come. By any possibility, if current driving value is constant, signal path of input and output parasitic capacitance or resistance make additional time constant of the system. Also IO pads which are given by process manufacture make additional capacitance.

Because the reason, the design targets control of LIN bus rise and fall time automatically. It is technique for overcoming to satisfy receiver electric AC parameter from standard at unwanted different condition than before fabrication.

3.3.2. Proposed Interface Description

The procedure of auto slope control is given by fig 3-21. It shows feedback loop for proposed design.

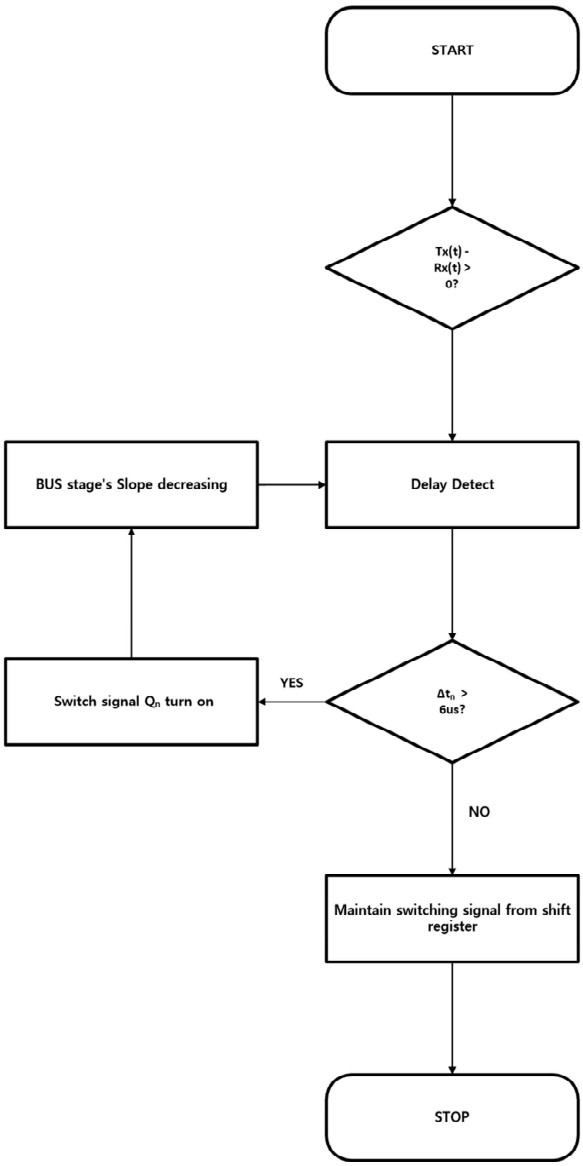


Figure 3-21: Flowchart procedure of delay control

First, detect time difference of input bit stream TXD and output bit stream RXD. The delay is always occurred by internal cell. Delay detection block checks the amount of input and output difference time. And then, Δt_n is over 6 us which is the time determined by digital block. If Δt_n is over the designated time, turn on switching signal for LIN bus slope decreasing. After finish the first loop, delay detection acts again and checks decreased input to output delay. Then, check value of Δt_n and switch signal turn on. Slope control decreasing and delay detection again. Proposed loop action repeat and stop when Δt_n takes under designed time. Maintain number of switching signal Q_k is shift register's output signal.

In figure 3-23, there is relation of input, output, switching signal and transition of LIN bus node. **Delay** signal is generated by difference of TXD and RXD. The delay value Δt_k is decreasing after Q_{k-1} signal turns on. Ordinal 'k' is delay detection step for auto slope control. After Q_{k-1} turns on, LIN bus rise time Δt_{kr} and fall Δt_{kf} are decreasing than previous step. Under inequality signs show relation of each time value. The 6us means reference restriction time based on parameter 31 from table 3-5.

$$\Delta t1 > \Delta t2 > \Delta t3 > \cdots > 6us > \Delta tn+1 = \Delta tn \quad (2)$$

$$\Delta t_{1r} > \Delta t_{2r} > \Delta t_{3r} > \cdots > \Delta t_{nr} \quad (3)$$

$$\Delta t_{1f} > \Delta t_{2f} > \Delta t_{3f} > \cdots > \Delta t_{nf} \quad (4)$$

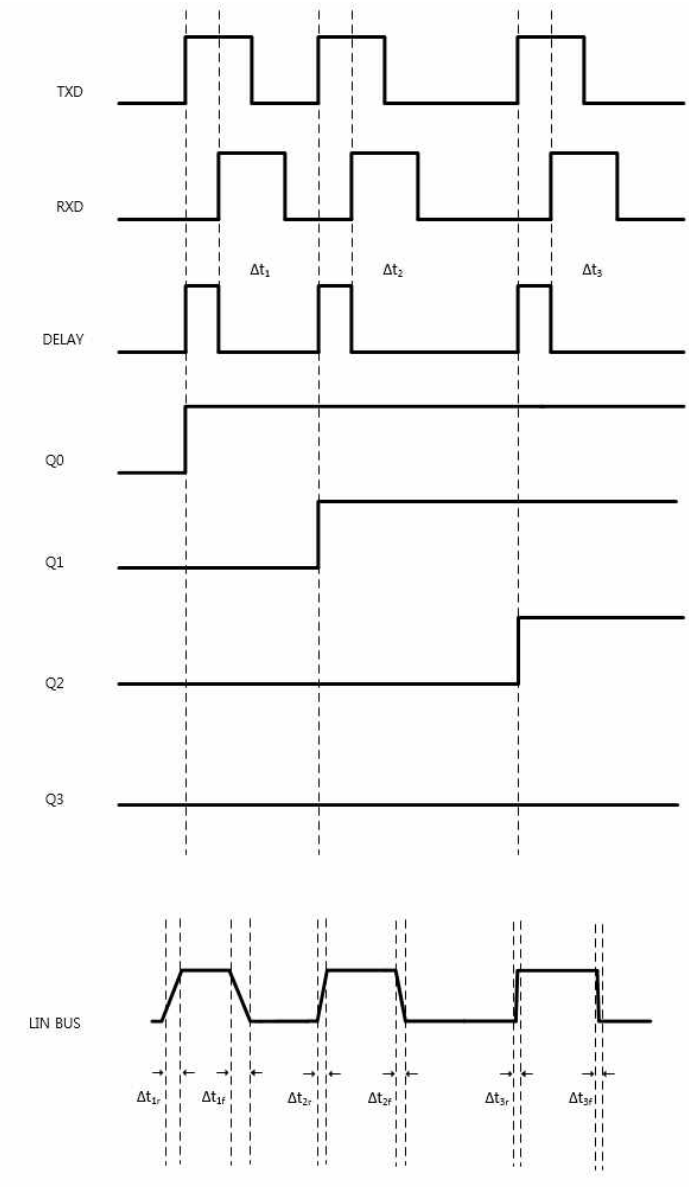


Figure 3-22: Pseudo waveform of signal relation

There is the block diagram of delay calibration with signal path transfer shown in figure 3-22. First, '**Delay Detector**' catch the input TXD and output RXD. It is compose of Phase Frequency Detector connection. '**Switching Signal Generator**' compares detected delay time and assigned delay time. If previous block transfers switching signal, '**Slope control**' injects current faster than before. Current cell pair array of figure 3-6 are turning at a time after enabled switching signal. In the design power transistor and connected protection device are assorted '**Driver**' block. It's departure time of power MOSFET's threshold voltage is controlled by 'Slope Control's current injection. 'Driver' induces recessive and dominant state based on activation control of power MOSFET. 'Receiver' get LIN bus signal and transfer RXD signal to return path for delay detector and ECU's input.

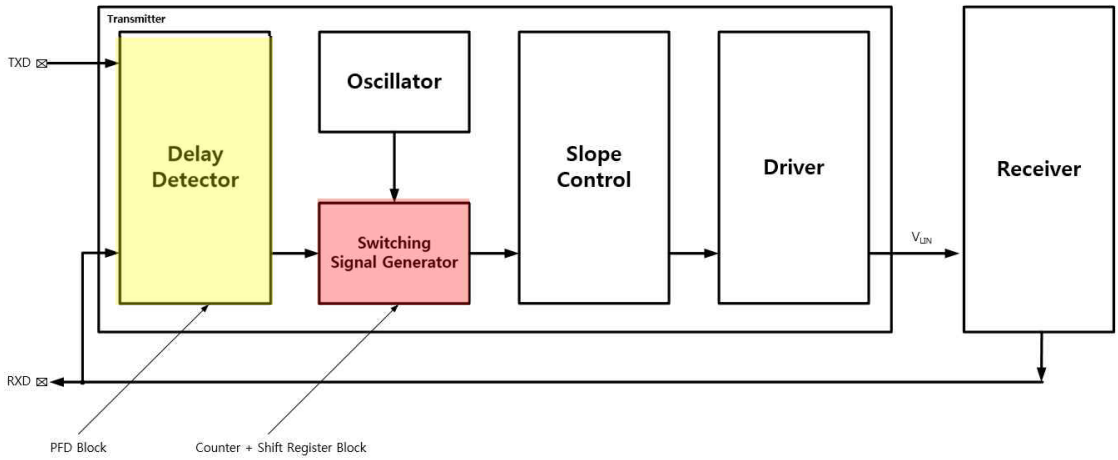
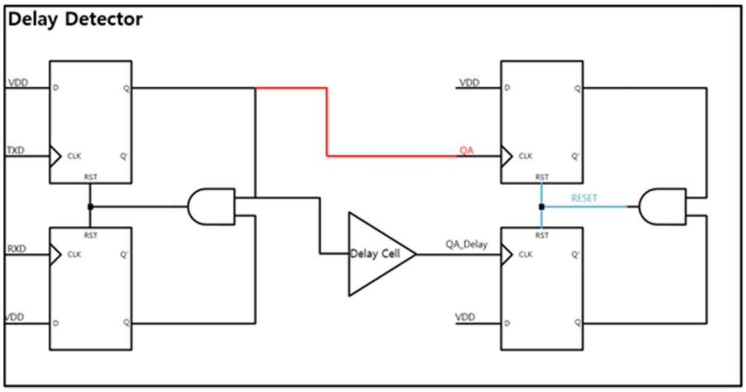


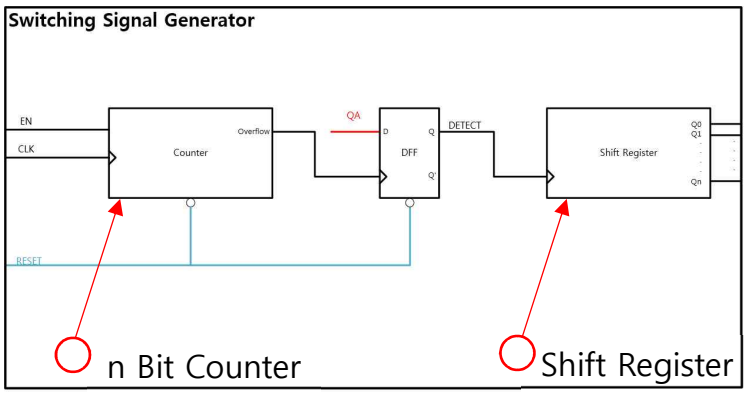
Figure 3-23: Simplified block diagram of proposed design

In figure 3-23, there are specific schematic of **Delay Detector** and **Switching Signal Generator**. Two block of transmitter is the core logic for additional proposed design. The Delay Detector has connected two Phase Frequency Detector. Two input can be clock of each d flip-flop. PFD can sense two pulse input difference while first d flip-flop input remains at low state while first input of d flip-flop remains at high state[12]. When first input remains high state, if second input changes low to high, the AND gate inputs are high state. So, the output can be high and it drives reset for each d flip-flop. And then, the output of delay detection signal QA takes low state. If the inputs which have little difference phase, PFD generates delay pulse signal again.

Delay Detector makes pulse which has delay duration and reset signal. First PFD catches delay of two input TXD and RXD. QA can be delay detection pulse for two bit stream. Second PFD takes two input which are pure delay pulse QA and little shifted delay pulse QA_Delay. Buffer array can be **Delay cell** for second d flip-flop's clock input. Based on Delay Cell, momentary shift range of QA and QA_Delay can be determined. The second PFD generates difference of two pulse signal which can be made by Delay cell. It's AND gate output can be RESET signal for next stage.



(1)



(2)

Figure 3-24: Schematic of Delay Detector block and Switching Signal Generator

Switching Signal Generator makes switching signal for turning on slope control block's current cell array. The block composed of counter, d flip-flop and shift register. Counter makes overflow signal to compare with period of delay. Counter's overflow signal is occurred after clock period of oscillator× 2^{n-1}, n is bit of counter. Counter and d flip-flop use 'RESET' signal from previous block to their reset signal. So after entering RESET which is starting with QA signal, counter outputs overflow signal also starting with QA signal.

When appearing overflow signal, next d flip-flop gets that signal on positive edge triggered clock and takes delay pulse on D input. If QA signal maintain high state when overflow occurred, d flip-flop generates DETECT signal. Shift register takes DETECT on positive clock. When DETECT signal is injected shift register, shift register outputs switching signal Q_k. Feedback loop of fig 3- 21 acts repeatedly, before detect signal doesn't appear anymore. Shift register maintains signal for slope control switching.

3.3.3. Simulation Result

Figure 3-24's feedback procedure waveform given by the figure 3-25. Fourth pulse signal means TXD and RXD delay Δt_k of figure 3-22. When the signal duration is over than 6us which is set-upped by internal counter, d flip flop output

DETECT from fig 3-24 (2) generated by overflow signal which is injected to its clock. After the auto slope control, in case of the delay signal is entering under 6us, there is no DETECT signal and maintains steady-state delay duration like the waveform.

As shown in figure 3-25, transient signal path at auto slope control is plotted. Rise time Δt_{kr} and fall time Δt_{kr} is gradually slow down after turn on auto slope control function enable. Maintain the edge time when TRX-RXD delay under 6 us after DELAY signal didn't apply anymore.

Figure 3-26 shows pseudo random bit stream transient for signal path. 20kbps data bit stream can be transferred at each data path.

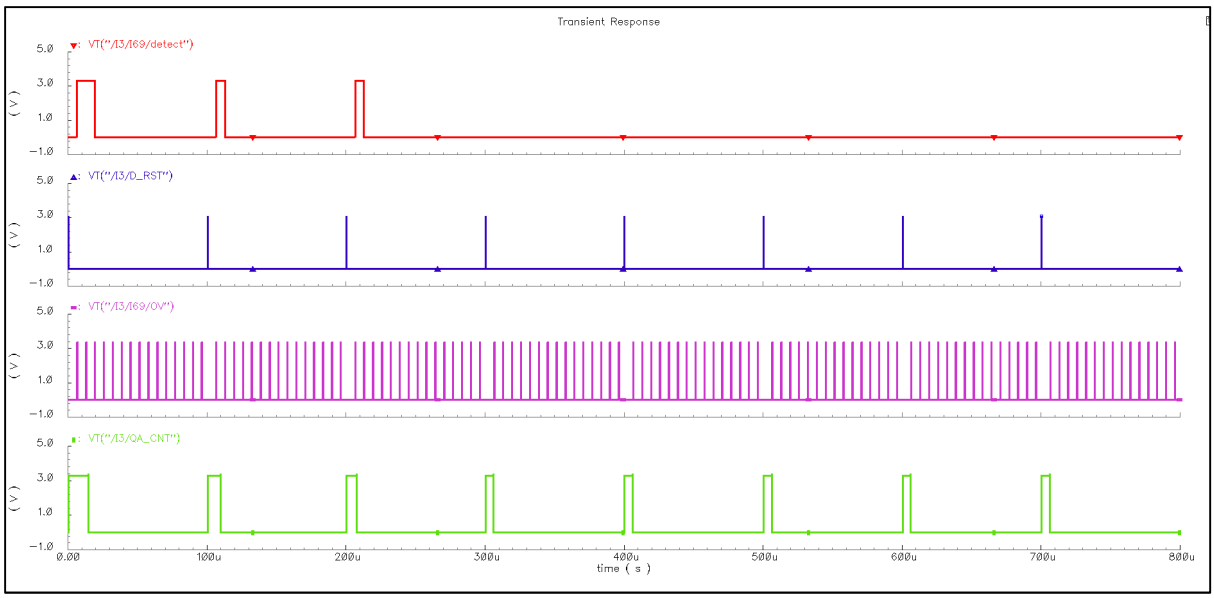


Figure 3-25: Auto slope control detection signal waveform

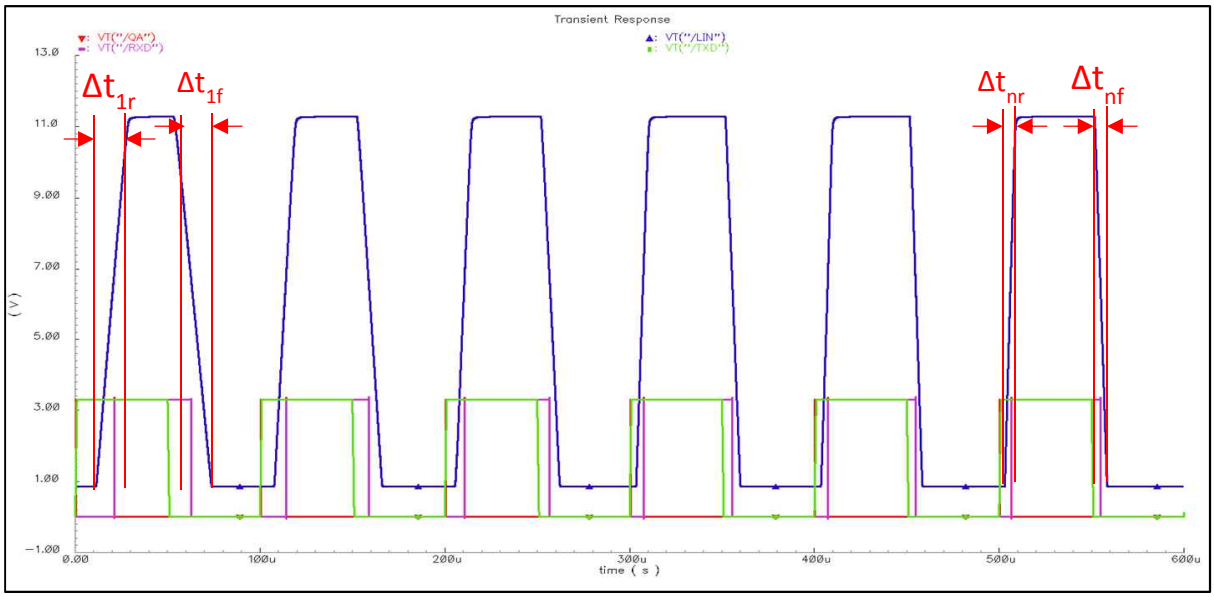


Figure 3-26: Signal path waveform with enabled auto slope control

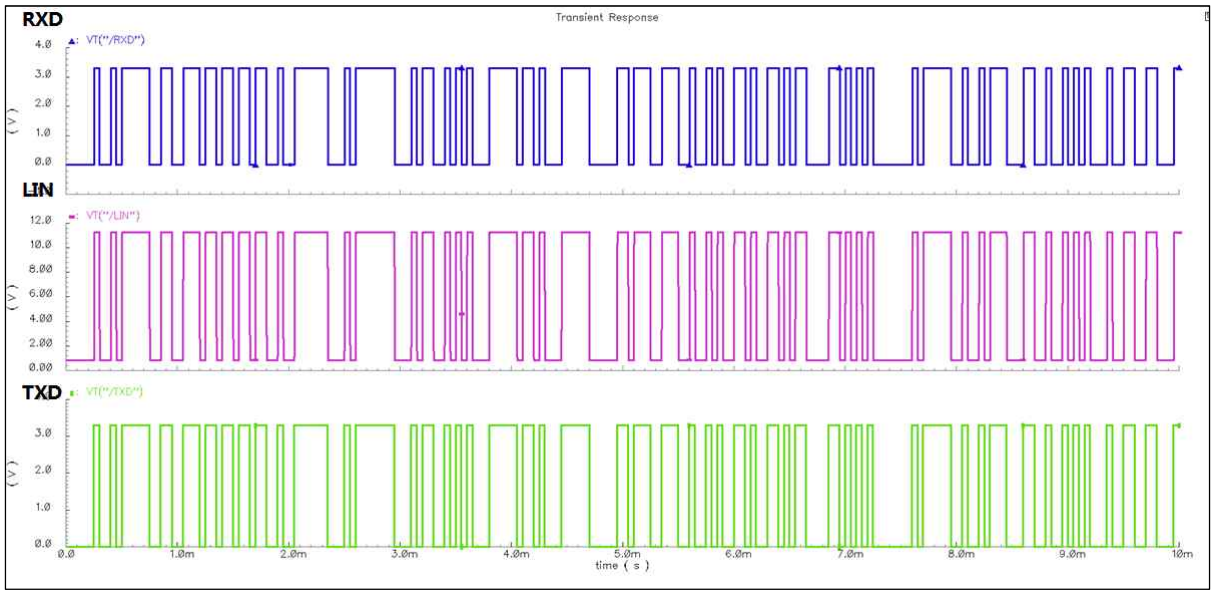


Figure 3-27: Pseudo random bit stream input and output signal path of transceiver

Specification	Value	Unit
Battery Voltage	12	V
Voltage Guarantee	0 ~ 40	V
Digital VDD	3.3	V
Analog VDD	3.3	V
Data Rate	20	kbps
Current Limitation	40 ~ 200	mA
Leakage Current	1.5 (Dom) ~ 16.5 (Rec)	uA
Max Propagation Delay	0 ~ 6	us
Time constant	1 ~ 5	us
Receiver symmetry	-2 ~ 2	us
Master Capacitance	220	pF
Slave Capacitance	220	pF

Table 3-9: Specification of transceiver with auto slope control

3.3.4 Layout & Fabrication Result

Fig 3-28 shows top layout with core and pad connection. SK Hynix HB130GS process is used to complete design from low voltage to high voltage. That occupies 1175 micro meter by 1585 micro meter. There are 28 pad with high voltage IO for measurement. Fig 3-29 shows real chip photograph after fabrication with bonding line.

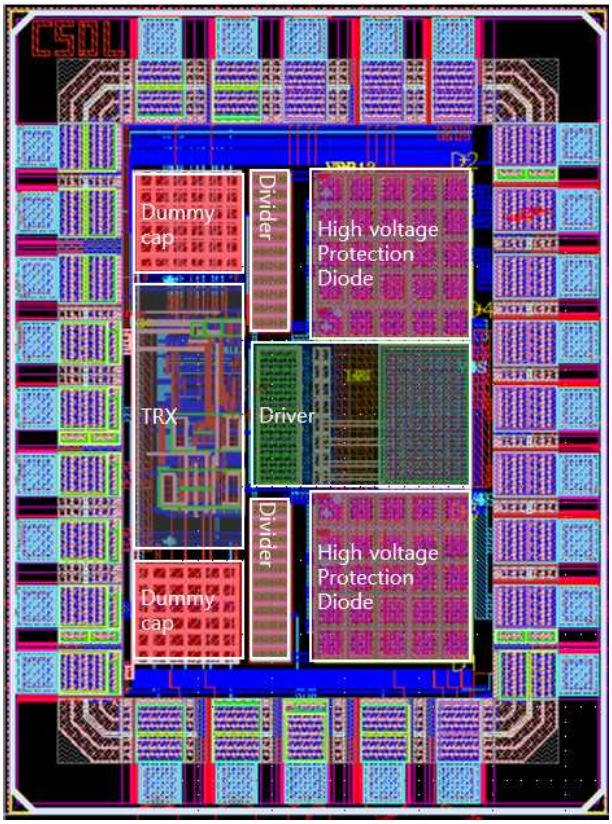


Figure 3-28: Top layout of auto slope control

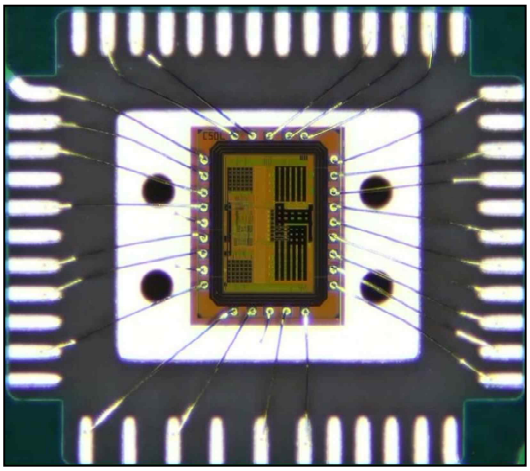


Figure 3-29: Chip photograph

3.3.5 Measurement Result

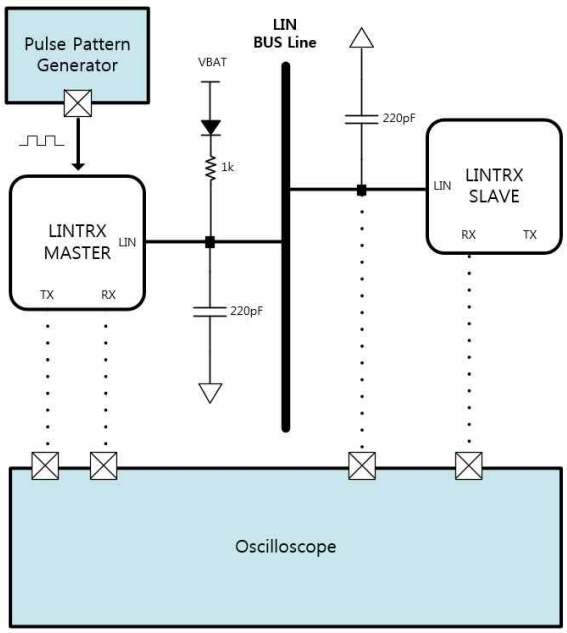


Figure 3-30: Measurement plan for master-slave configuration

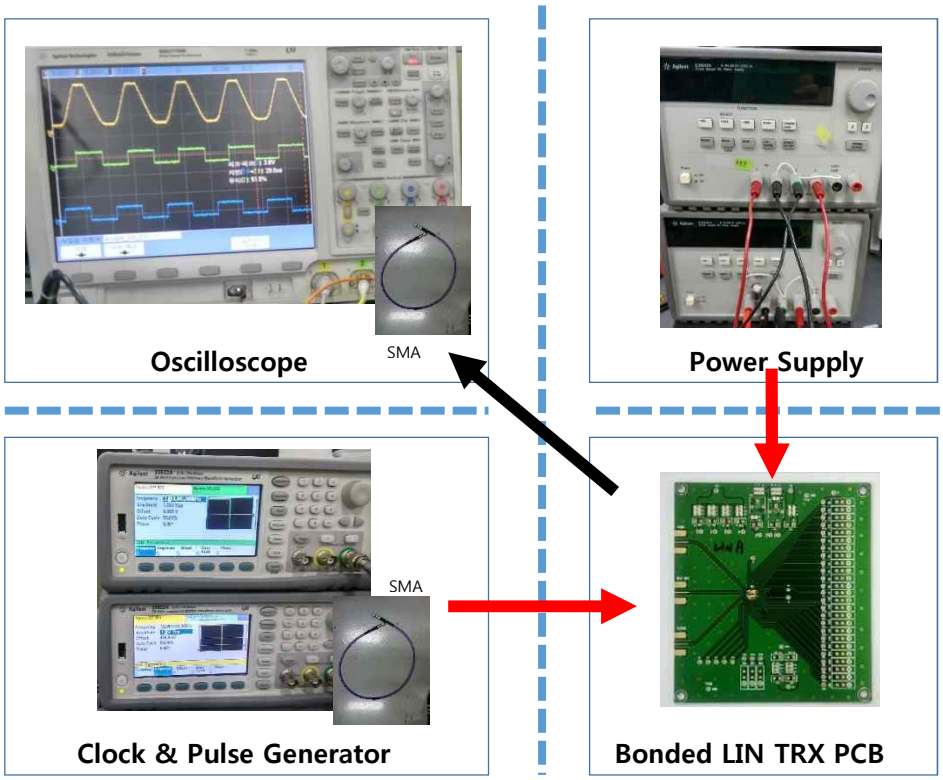


Figure 3-31: Experimental environment

Figure 3-30 shows measurement plan for data path master-slave configuration. Figure 3-31 contains measurement setup for the transient result. The setting based on schematic from fig 3-30. Pulse generator makes pseudo random bit stream. Alpha and beta case input which from LIN ISO standard.

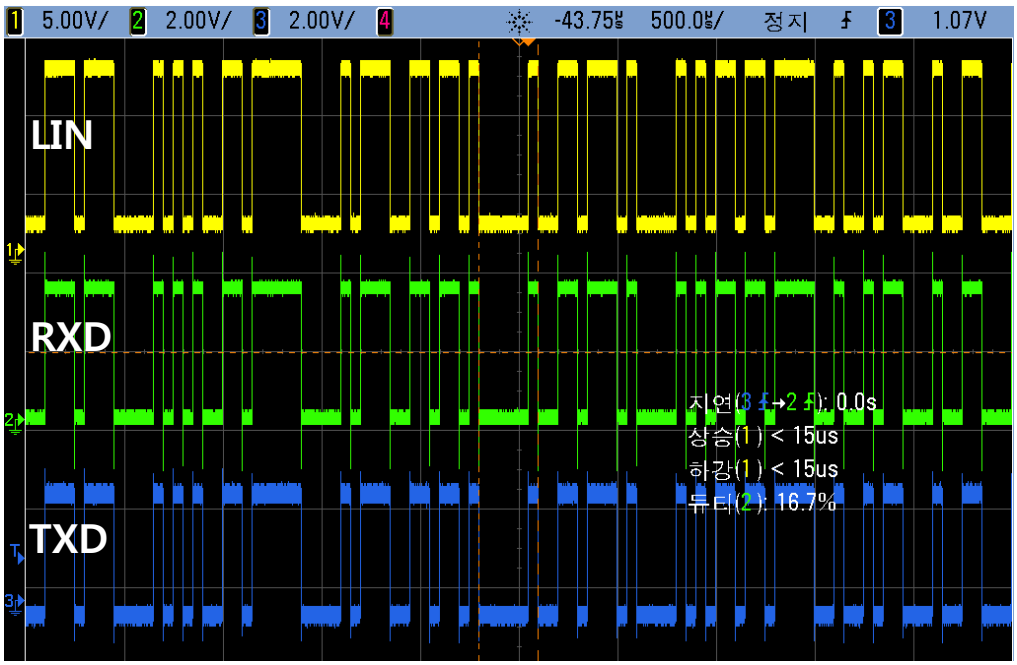


Figure 3-32: Class alpha(20kbps) PRBS measurement result

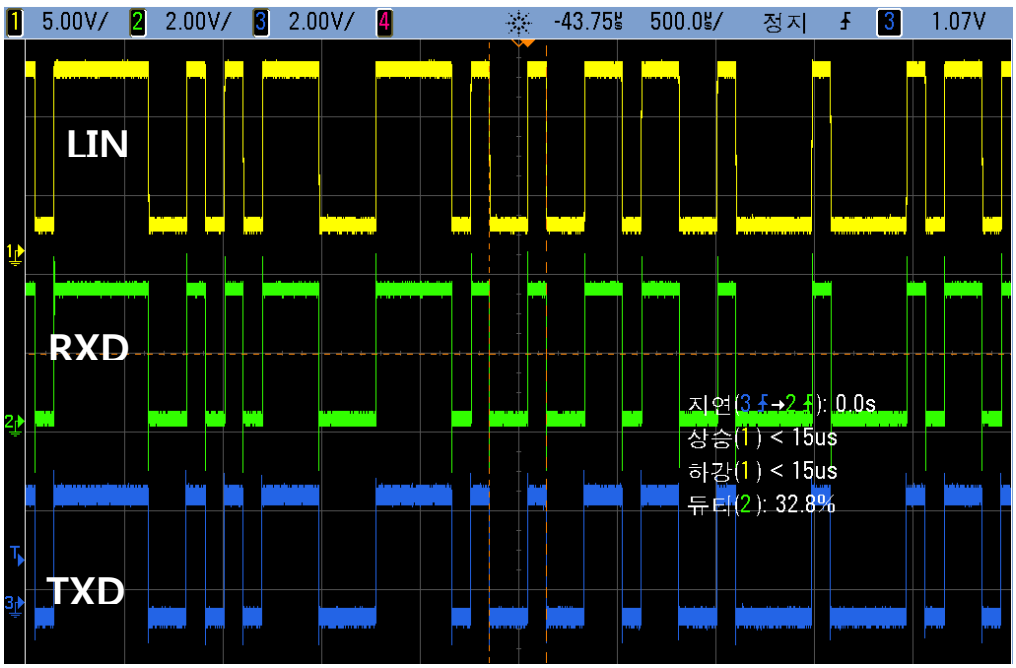


Figure 3-33: Class beta(10.4 kbps) PRBS measurement result

Figure 3-30 shows FFT result of measurement normal slope and low slope mode. Low slope mode(LSM) has lower knee frequency, so high frequency components are lower than normal slope′s. An upper bound frequency below which most energy in digital pulse concentrates. The knee frequency equation is given by below.

$$F_{knee} \equiv \frac{0.5}{\tau_{r10-90\%}} \tag{5}$$

A point of intersection -20dB/dec and -40dB/dec. Low slope mode(LSM) has lower knee frequency, so high frequency components are lower than normal slope's. It is robust to endure EMI which contain high frequency noise components.

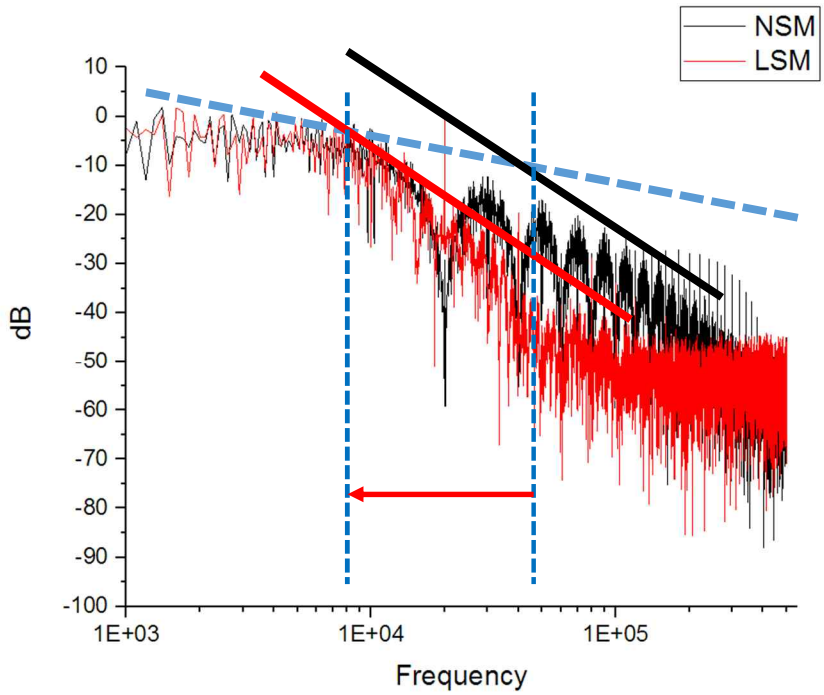
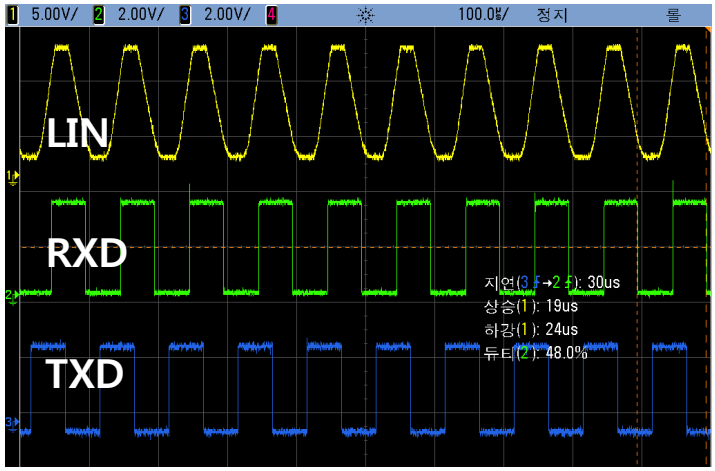
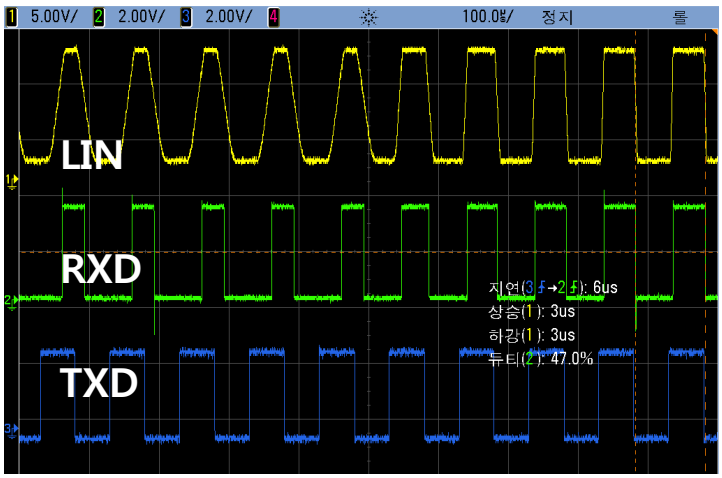


Figure 3-34: FFT result of normal and low slope mode

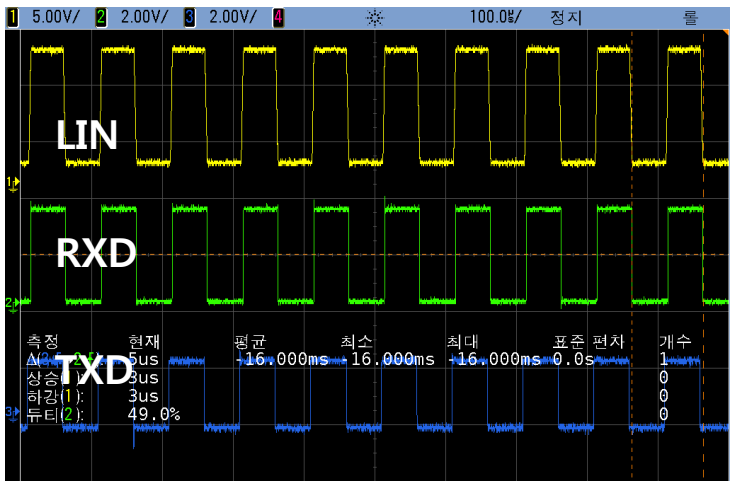
There is auto slope control monitoring in figure 3-35. After auto slope control enable, observe the waveform using oscilloscope′s roll mode. Roll mode is data acquisition function for saving transient before stop. It scroll on very low speed to observe signal trace from right to left. First waveform shows before auto slope control enable. LIN bus has edge time from 19us to 24us. That is fig 3-22's Δt_{kr} and Δt_{kf}. Measured 30us is the delay of transceiver's input TXD and output RXD. That is fig 3-22's Δt_{k}. If there is no calibration, it is can be over standard delay margin certainly. After auto slope control is turned on, TXD-RXD delay and edge time of LIN bus are decreasing gradually like the second waveform. When entering the steady state condition, there is no DETECT signal of fig 3-25. Third wave form of fig 3-35 show steady state signal path. LIN bus has edge time about 3us. Measured 5us is the delay of transceiver's input TXD and output RXD. It is under condition of designated time from internal counter overflow signal.



- (1)



- (2)



- (3)

Figure 3-35: Auto slope control measurement

Chapter 4

Future work

4.1. Measurement plan for Platform Integration through MCU

Due to urgent environment, there is no chance to confirm practical MCU and transceiver configuration. Most of all, the interface of MCU needs to share for applying to connection between transceiver and MCU in automotive network condition. Not only standalone version but also inside of ECU is important challenge to complete the physical layer interface. After fabrication, it will be proceeding the verification of integrated platform.

The application test with MCU is the part of verification for practical environment for automotive network system. After fabrication, connection of chip-real application needs to express stability of the design. Then, AEC Q-100 test which from a public institution can be affordable to certify.

4.2. Convergence of Previous Work

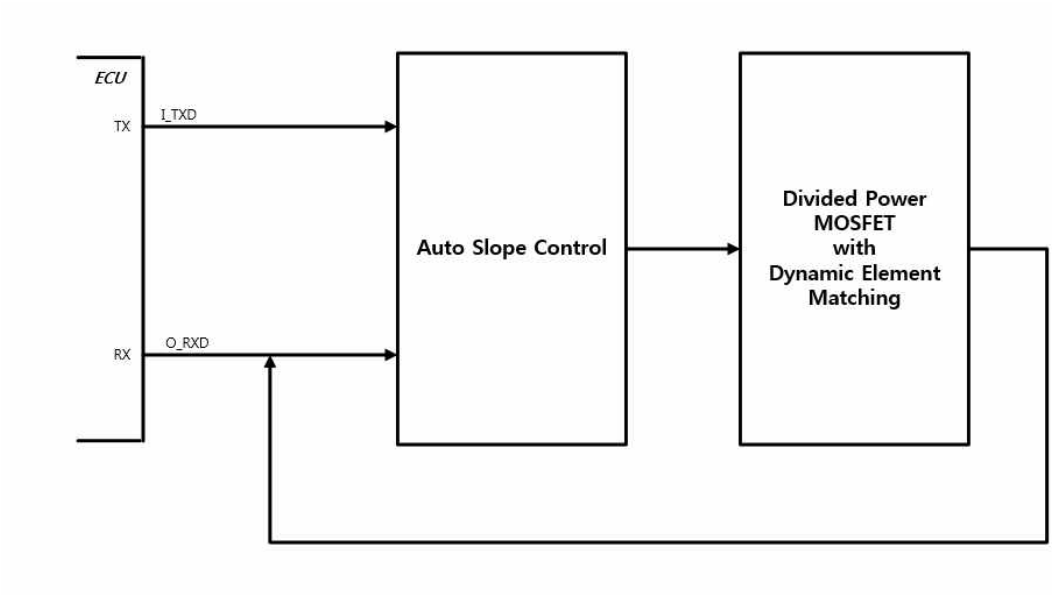


Figure 4-1: Convergence of proposed two design

Future additional implementation is given by figure 4-1. It symbolize convergence of two previous work Auto Slope Control and Divided Power MOSFET with Dynamic Element Matching technique. Main target of the proposed work implies propagation delay control based on bus edge time calibration that can be modulated by the power MOSFET dividing technique. Auto slope control block can detect delay from input bit stream TXD and output bit stream RXD. After delay detection, the block compare delay and designated time like fig 3-23 procedure. If the delay can't come with in the set value, next block decease rise and fall time which is dominant for total delay of the signal path. The second stage then ECU increase clock period which can be controlled by internal clock divider and switch binary decoder. The reference clock can be changed by

mentioned block. It increases and decreases each cell of stepwise current's maintained period, so total rise and fall time can controlled by sum of all current cells turn on time. The convergence design can be affordable to take advantages of previous work.

Chapter 5

Summary & Conclusion

The paper describes design procedure and result for LIN which is suitable network for sensor automotive communication. The input and output bit stream is under 20kbps and complete signal path of slave-master configuration. They can endure high voltage 12 V batter condition affordable to use automotive environment. The first chip covers signal path with state machine for interface of ECU. It gives option for mode change standby, sleep normal and low slope mode.

The second design contains protection technique for inrush current. It complete the signal path and attach technique to scatter unwanted high peak current. Also, to reduce current cell mismatch, dynamic element matching technique is used. For measurement after fabrication, switch selector block is attached in front of current cell array to select switch size in case of occurring difference of unit current cell driving.

Propagation delay control is given by the third design. Using auto slope control with internal digital blocks, it can modulate delay of input TXD and output RXD and time constant control with in ISO 17987-4. The delay restricted 6us which designated by overflow signal and time constant can be measured under 5us which is maximum boundary of the system from standard.

The proposed design needs to satisfy ISO 17987 – 4 and 7 to communicate ordinarily with master and slave for low speed application. Above all, it needs to transfer signal perfectly with no error because of passenger's safety. This design targets durability of external unexpected environment which has possibility of bit stream error. Also controllable timing factor for changeable environment.

All the process are designed by Cadence virtuoso based on Linux system. There are two process, Magnachip AP18E50 and SK Hynix HB130GS can be used to realize the proposed implementation.

Acknowledgements.

교수의 시간을 아껴주는 학생이 좋은 대학원생이라는 말을 들은 적이 있습니다. 그만큼 바쁜 직업이기에 나오는 말 일 것입니다. 시간을 쪼개어 심사에 참여해주신 교수님들의 시간이 너무나 귀중하기에, 어떤 감사의 인사도 부족할 것입니다.

대형 센서 과제를 진행하고 계셔 하루하루 바쁜 나날을 보내시는 이윤식 교수님.

DBOUT 을 위해 학생들 지도에 여념 없으신 최재혁 교수님.

그리고, 지난 시간 동안 매일 매일 연구를 향한 열정으로 저와 연구실 학생들의 롤 모델이 된 지도교수님.

모두 감사합니다.

짧으면 짧고 길면 긴 타지생활을 잘 적응할 수 있게 도와준 CSDL 식구들 광묵, 원진, 수빈, 종규, 명우, 동윤, 찬샘, 동일형, 기현, BICDL 형님들, ICSL 학생들, AESL 학생들, 나의 친구 원희 주협 희영, 그리고 나의 또 다른 스승 성우형, 경환. 나의 오랜 파트너 승목.

모두 감사합니다.

마지막으로 나의 사랑하는 아버지 어머니 동생에게 감사의 인사를 올립니다.

어디에 있든 늘 빚진 마음으로 살아가겠습니다.

Reference

[1] Advanced MP Technology, 'Semiconductor Market in the Automotive Industry', viewed 14 May 2016, http://www.advancedmp.com/semiconductor-market-in-the-automotive-industry

[2] V. v. Tils, "Trends and Challenges in Automotive Electronics," in *2006 IEEE International Symposium on Power Semiconductor Devices and IC's*, 2006, pp. 1-3.

[3] Dohyun Jung, "Trends of Intelligent Vehicles and Future Vehicle Technology Development Project", Korea Automotive Technology Institute, viewed 6 May 2016, http://www.kipo.go.kr/club/file.do?attachmentId=4060

[4] Stress Test Qualification for Integrated Circuits; published by the Automotive Electronics Council (AEC)

[5] L. F. Roger, "CCITT Signaling System No. 7," in *Fundamentals of Telecommunications*, ed: Wiley-IEEE Press, 2005, pp. 361-386.

[6] Young-Jun-Yoo, Status and Future Trend of Automotive Electronics, Y.J.Yoo, KETI , viewed 2 June 2016, http://203.253.128.6:8088/servlet/eic.wism.EICWeb?Command=0

[7] J. M. Redoute and M. Steyaert, "An EMI Resisting LIN Driver in 0.35-micron High-Voltage CMOS," *IEEE Journal of Solid-State Circuits,* vol. 42, pp. 1574-1582, 2007.

[8] P Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design (Oxford University Press, Ine, USA, 2002), 2 edition, pp. 259-397

[9] O.H., "What is inrush current?" Component Business Unit Murata Manufacturing Co. viewed 15 June 2016, http://www.murata.com/products/emiconfun/emc/2012/10/29/en-20121029-p1

[10] M. Deloge, A. v. d. Wel, S. Goyal, G. Kwakernaat, and A. Schoof, "A highly-digitized automotive CAN transceiver in 0.14um high-voltage SOI CMOS," in Electromagnetic Compatibility of Integrated Circuits (EMC Compo), 2015 10th International Workshop on the, 2015, pp. 13-17.

[11] J. P. d. Gyvez and H. P. Tuinhout, "Threshold voltage mismatch and intra-die leakage current in digital CMOS circuits," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 157-168, 2004.

[12] Behazd Razavi "RF Microelectronis", PEARSON, pp. 612-613, 2012.