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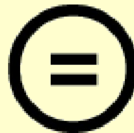

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An Approach to Assess Solder Interconnect Degradation Using Digital Signal

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An Approach to Assess Solder Interconnect Degradation Using Digital Signal

A thesis
submitted to the Graduate School of UNIST
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Master of Science

Jeong-ah Yoon

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Approved by

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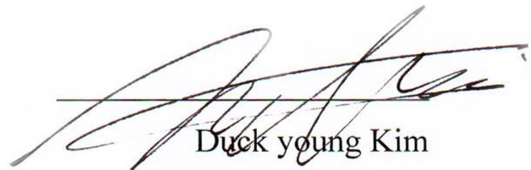

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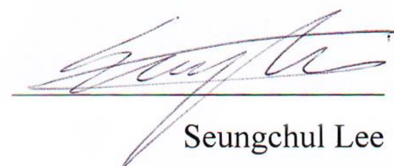

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Abstract

Digital signals used in electronic systems require reliable data communication. It is necessary to monitor the system health continuously to prevent system failure in advance. Solder joints in electronic assemblies are one of the major failure sites under thermal, mechanical and chemical stress conditions during their operation. Solder joint degradation usually starts from the surface where high speed signals are concentrated due to the phenomenon referred to as the skin effect. Due to the skin effect, high speed signals are sensitive when detecting the early stages of solder joint degradation.

The objective of the thesis is to assess solder joint degradation in a non-destructive way based on digital signal characterization. For accelerated life testing the stress conditions were designed in order to generate gradual degradation of solder joints. The signal generated by a digital signal transceiver was travelling through the solder joints to continuously monitor the signal integrity under the stress conditions. The signal properities were obtained by eye parameters and jitter, which represented the characteristics of the digital signal in terms of noise and timing error. The eye parameters and jitter exhibited significant increase after the exposure of the solder joints to the stress conditions. The test results indicated the deterioration of the signal integrity resulted from the solder joint degradation, and proved that high speed digital signals could serve as a non-destructive tool for sensing physical degradation. Since this approach is based on the digital signals used in electronic systems, it can be implemented without requiring additional sensing devices. Furthermore, this approach can serve as a proactive prognostic tool, which provides real-time health monitoring of electronic systems and triggers early warning for impending failure.

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I. Introduction

1.1 Background

Electronic systems have been widely used for not only user-friendly products such as appliance, smart phone and tablets but automotive, aviation and manufacturing systems which have been regarded as traditional mechanical systems. For instance, manufacturing or shipbuilding industry has been implementing a monitoring system based on sensors and electronic control devices. In order to satisfy demand for enhanced performance, electronic systems have been developed by applying elaborated structures with high speed signal.

Electronic systems are subjected to stress conditions such as thermal, mechanical, electrical and chemical stress during their life cycle. The stresses applied to electronic systems result in cumulative damage in the electronic systems and malfunctioning can occur. The system malfunctions initiated from the accumulated damage may lead to catastrophic failure, which is directly related to safety and economic losses. For this reason, it is critical to guarantee failure free time for system design stage, moreover the timely actions to avoid system failure are necessary during the system operation.

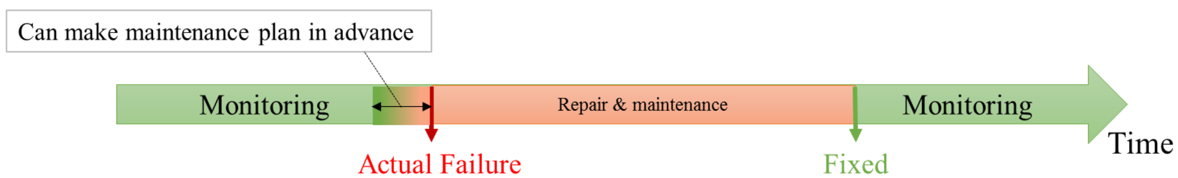

Figure 1. Predictive maintenance

In terms of maintenance policies for system management, schedule based maintenance (SBM) has been one of the popular maintenance policies for a long time. The maintenance schedule is conducted at specified times. Maintenance activities for SBM usually follow the pre-determined schedule with the aim of anticipating the process failures [1]. Since this approach often requires extra cost for unexpected maintenance due to sudden system failure, condition based maintenance (CBM) is suggested as an alternative. CBM basically accompanies in-situ monitoring and preventive actions are decided based on the system status at that moment. CBM has now been extended to predictive maintenance (PdM) which predicts the system states and decides on corrective action in advance using real-time health monitoring data. Compared to CBM, the duration of corrective action can be predicted by PdM based on statistical modeling [2, 3], thus PdM reduces idle time for maintenance activities and can contribute to continuous system operation.

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1.2 Motivation and Problem definition

Real-time monitoring data acquisition in CBM or PdM is based on sensor measurements or relative physical quantity measurements. Data acquisition often requires to establish additional monitoring system using sensing apparatus. However, there could be limitations of implementation depending on the apparatus used for the data acquisition. In order to overcome the limitations, the thesis will introduce a new approach to characterize the system health by digital signal. Digital signal has been used for data communication in electronic systems, and has unique characteristics which enable the digital signal to sense damage propagation without additional apparatus. Thus, the characterized data can represent the system state more sensitively including intermediate stages of degradation.

The thesis is organized as follows. The second chapter introduces existing methodologies for system assessment in the literatures, and the third chapter will cover theoretical aspects related to digital signals and parameters used for characterization. All experimental processes are explained in the fourth chapter. Data produced from the experiments are analyzed including discussions in the fourth chapter as well. In the final chapter, the conclusion and expected applications will be presented with several examples.

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II. Literature survey

The signal used for data communication has been assessed by quantitative indices which represent the signal quality in the circuit. Following literatures in this chapter will cover techniques for degradation monitoring, especially for partial degradation. Several literatures will introduce the use of digital signals for system assessment based on case studies. At the end of this chapter, a concrete problem statement will be established considering the limitations of existing studies.

2.1 Detection methods for partial degradation

DC resistance have been widely used because it can indicate electrical discontinuity explicitly. However, it is not suitable for sensing the intermediate stages of the failure (e.g. partial open). Thus, the methods of detecting the partial degradation have been actively studied in order for continuous system monitoring and predictive maintenance.

Voutilainen [4] reported that the voltage measured from off balanced bridge circuit (i.e. off-balance voltage) can be a precursor of solder interconnection failure. A test vehicle which included BGA type package was exposed to thermal cycling load, and the off-balance voltage obtained from the embedded bridge circuits was continuously monitored. There were continuous voltage changes as the number of cycles increased, and the results indicated the off-balance voltage can detect gradual failure. However, bridge circuits should be additionally designed for off-balanced voltage acquisition in this case.

Gershman [5] examined the relationship between ohmic resistance and a crack growth at solder joint. The ohmic resistance indicates the resistance which is calculated by considering the rectangular cross-sectional area of the solder joint. The solder joint crack was induced by thermal cycling, and the ohmic resistance was measured once in a week. The results showed that the resistance monotonically increased during the crack propagation. This relationship between ohmic resistance and solder joint cracking was applied to a method for health monitoring of quad flat no-lead (QFN) package. However, an additional bridge circuit for health monitoring was required, and the crack length behavior needed to be determined in advance in this case.

Ji [6] conducted a study for IGBT health monitoring in terms of bond wire degradation. A linear relationship between the voltage across the IGBT and temperature of the bond wire were used to decide the IGBT degradation under thermal cycling. As the bond wires were lifted off during the degradation, the temperature of the remaining bond wires in IGBT increased due to the self-heating induced by

current concentration. The voltage drop can represent the behavior of the bond wire temperature based on their linear relationship, thus the degradation monitoring of the IGBT was possible. In this study, the partial degradation of the IGBT was described as a state that some of bond wires in IGBT were disconnected. It is necessary to consider the degradation of each individual bond wire such as heel cracking, in order to be more sensitive health monitoring.

TSV is a technique used for 3D chip stacking, and Okoro [7] introduced the RF-based monitoring method for TSV degradation. Thermal cycling was applied to TSV in the experiment and, the RF signal integrity of the TSV daisy chain was assessed by transmission coefficient (i.e. S-parameter). The transmission coefficient was recorded at every 500 cycles after, until reached to 2000 cycles. The results showed that the transmission coefficient gradually increased as the number of cycles increased. A destructive inspection process proved the void formation and propagation at the TSV, and found that the RF transmission coefficient could explain the TSV degradation. There are other types of signals which have similar characteristics to RF signals, for example digital signal. It is worth using digital signals or other similar type of signals for degradation monitoring in order to extend the application range.

2.2 Use of digital signals for system assessment

Quality of digital signal (i.e. signal integrity) has been used as an assessment tool in terms of circuit design. Wu [8] introduced an overview of assessing the digital signal travelling through the link-path such as trace, solder balls and strip lines. Signal integrity (SI) of link-path can be affected by its geometrical design such as width of strip line. An eye diagram is one of a common way of evaluating SI and is constructed by superimposing the bits. SI depending on the link-path design has been assessed by using eye diagram metrics which represents voltage attenuation and timing errors. Crosstalk is another critical aspect of SI degradation, and the electromagnetic interference is usually explained by crosstalk.

Several specific examples have been reported, and Alessandro [9] introduced a thermal modeling process based on SI analysis for highly integrated electronic systems. In the case study, the test vehicle had an ultra-thin interconnect for chip stacking, and temperature of the interconnect was measured during the operation. The thermally-induced SI deterioration was characterized by the relationship between behavior of SI indicators (e.g. propagation delay, impedance change) and the interconnect temperature. The results can be considered at the design stage in order to reduce the thermal effect to digital signal.

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Interconnect SI assessment was conducted in [10] by using built-in sensors designed for high speed signal monitoring, and the sensor measured undershoots and overshoots of a traveling digital signal. A signal integrity fault indicated the violation of assessment criteria for signal integrity. In this study the signal misinterpretation at the receiving gate was regarded as a signal integrity fault. The signal misinterpretation was induced by overshoot or undershoot which exceeded the acceptable logic interpretation region. In this literature, circuit design was considered as a major cause of signal degradation. Another studies related to SI assessment for PCB structures have been conducted through the literature [11, 12].

2.3 Problem statements

The detection methods for partial degradation and use of digital signals introduced in this chapter have several limitations. First of all, parameter measurement required additional sensing devices including multi-meter, sensors and power sources. Some studies demonstrated continuous RF monitoring processes but, the processes are encouraged to use other similar types of signals which used for the electronic system operation, such as digital signals. An approach to assess the partial degradation by using digital signal will be introduced, and the succeeding experiment will prove that this method can be developed a continuous monitoring tool. The following chapters will cover the detailed process, and how this approach can deal with the limitations from the existing literatures.

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III. Digital signal characterization

The main concept of the method in this thesis is characterizing digital signal deterioration depending on the health state of the signal path. Several characteristics of digital signal which support the method will be presented first, then the characterization process will be provided at the last part of the chapter.

3.1 Characteristics of high speed digital signal

The skin effect is a phenomenon that the alternating current penetrates through the surface of the conductors. AC current generates magnetic flux, then inductance at the central part of the conductor increases because the magnetic flux near the periphery of the conductor is cancelled out. Thus, the surface has relatively lower inductance, and the main current is more concentrated.

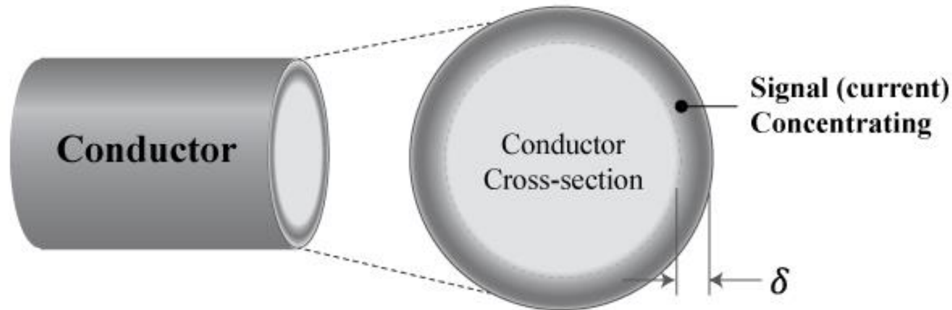

Figure 2. Skin effect

Skin depth is the layer up to the thickness where approximately 63% of the travelling current is concentrated. The following equation shows that skin depth depends on the frequency *f*, the resistivity of the conductor ρ, and the material's permeability μ, thus a higher frequency signal that has the a shallower skin depth.

$$\delta = \sqrt{\frac{\rho}{f\pi\mu}} \tag{1}$$

A higher frequency induces more dense surface current which means the current can change more sensitively depending on the stimulus at the surface. Degradation of electronic systems including interconnects usually initiates from the exterior, for instance, a crack on the solder interconnect propagates toward the interior as well. The high frequency signal traveling through the solder interconnect can be adversely affected by the physical damage, accordingly. A case shows that a crack

at the solder joint can be detected by using the skin effect of the RF signal [13]. Therefore, the skin effect is applicable to detecting cracks that initiates at the surface of the solder joint where the RF signal is travelling.

3.2 Signal integrity

Signal integrity (SI) simply means signal consistency between a transmitter and a receiver. For proper functioning of the electronic system, sufficient fidelity between the signal transmitter and receiver should be ensured [14]. Signal integrity is a critical factor in high-speed digital circuit design, and there are various factors which can affect signal integrity such as signal interference, asymmetries in clock cycles, EMI, and impedance mismatch. Thus, the signal integrity can serve as a criterion for assessing the quality of the signal in a high-speed digital circuit.

There are several concepts generally used in SI analysis: BER (Bit error rate), crosstalk, eye diagram and jitter. BER is the ratio of misinterpreted logics between the transmitter and the receiver. A phenomenon called crosstalk is applied to confirm electromagnetic interference among the signal transmissions. Eye diagram including eye parameters shows the signal integrity in both a visual and numerical way. Jitter indicates timing errors which can occur in the digital signal.

Impedance mismatch usually occurs when the impedance controlled signal trace in a high speed digital circuit is degraded by external stresses. The transmitted signal is reflected at the damaged point due to the impedance mismatch and finally the reflected signal deteriorates the signal consistency at the receiver. In this thesis, jitter based on an eye diagram is used to characterize the deterioration of the signal integrity before and after the solder joint degradation in a non-destructive way.

3.2.1 Eye parameters

The preliminary process to produce the eye diagrams is signal sampling from the original signal waveforms, and the sampling is conducted on the possible bit sequences of the signal at regular intervals. The results of the sampling are superimposed within unit intervals, then the eye diagram is created. The eye diagram implies the trajectory of the original signal waveforms, and the overall state of the signal can be confirmed accordingly.

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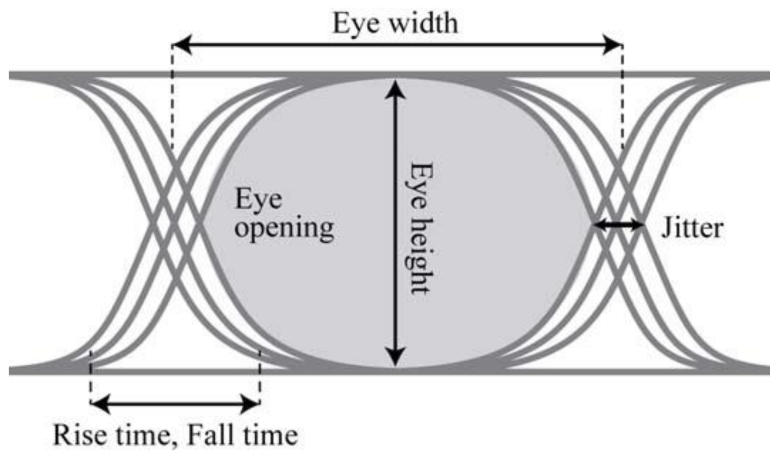

Figure 3. Eye diagram and associated parameters

The eye parameters which explain the eye diagram in quantitative ways include the followings: rise time and fall time associated with the signal transition time; eye height and width which explain the eye opening; and jitter which conveys the timing errors in digital signals. Distributions are generated at the points where the transition edges are crossed during the signal superimposition. The mean and the deviation of the distributions are in charge of determining the eye parameters.

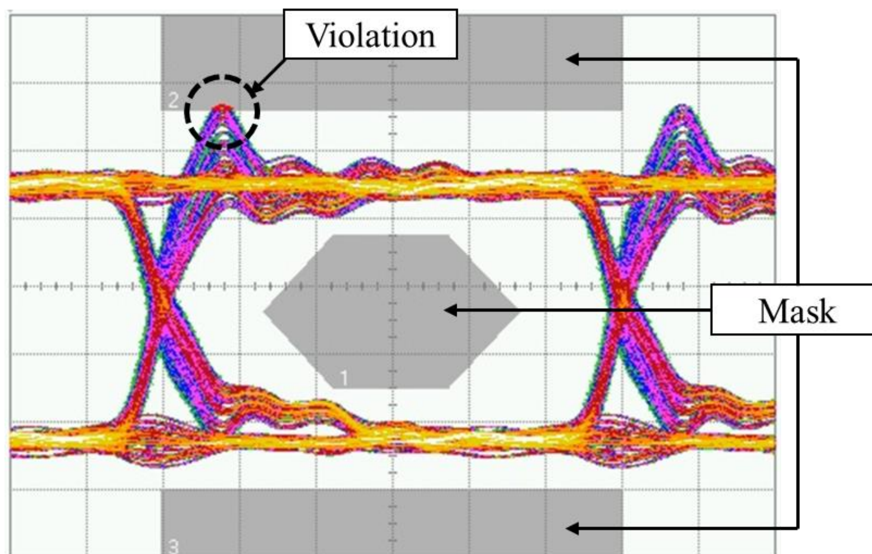

Figure 4. Eye mask test

In addition, a technique called the eye mask test validates the signal performance using the templates characterized by industry standards (e.g. Gigabit Ethernet mask). A signal which does not violate the three mask zones in Figure 4 is assessed to be proper for the target system operation [15].

3.2.2 Jitter

A data communication signal needs to be stable as electronic systems which require more than Gbps signal are becoming more numerous. Jitter has been often used as a significant way to assess the signal integrity for high-speed digital circuit in terms of design and performance. Thus, the signal integrity of the circuit including the solder joint is characterized by jitter in this study.

Jitter can be generated by different mechanisms; sampling is one of a mechanism which has no reference signal pattern but provides the jitter data based on the superimposed bit sequences. Another mechanism uses reference signal pattern captured at the instant of measurement initiation, and calculates jitter based on the timing errors between cumulative bit sequences and the reference pattern.

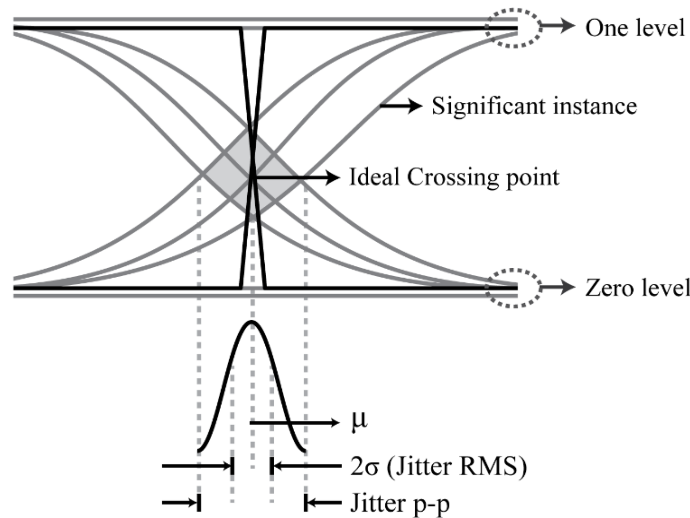

Figure 5. Definition of jitter in eye diagram (Sampling)

The sampling mechanism usually accompanies eye diagram, and the jitter is calculated based on the histogram generated in the eye diagram. The sampling based jitter defined as the deviation of the significant instants of a signal from the ideal crossing point where the signal transition edges should be crossed [16]. The sources of jitter are widely known as: the signal reflection caused by impedance mismatch; the matter of transmitted data dependent duty cycle distortion (DCD); and the random noise [17]. They can lead to the higher jitter values, as the deviation of the distribution increases at the crossing points. Jitter RMS and jitter peak-to-peak (i.e. jitter p-p), sampling based jitter, are determined by the distribution produced where the significant instants of the signal intersect each other. The jitter RMS is the distance between ±1σ from the mean, and the full width of the distribution corresponds to the jitter p-p.

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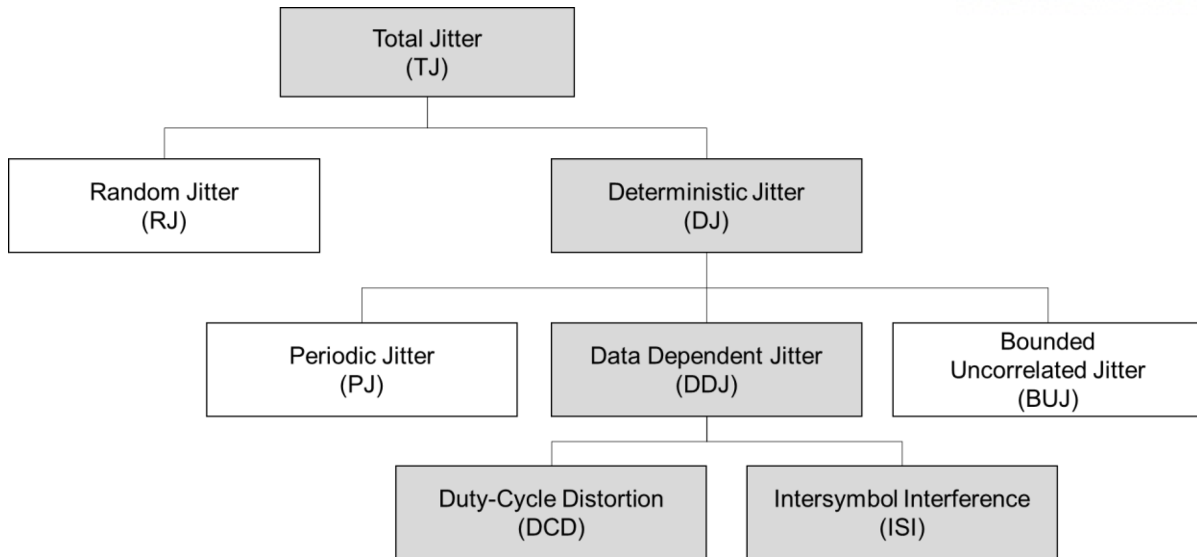

Figure 6. Jitter hierarchy

Though the sampling jitter indicates the signal integrity, it is hard for the sampling jitter to figure out the detailed causes of signal integrity change (i.e. jitter RMS, p-p). Thus, jitter decomposition is conducted for further analysis. Jitter is decomposed into several components as shown in Figure 6 depending on the jitter source or measurement mechanism, thus they can help root cause analysis of signal integrity change. Those jitter components were measured by a Keysight 86100D Digital communication analyzer (DCA) with enhanced jitter analysis software. When jitter starts to be measured, DCA initiates a pattern lock process which automatically detects the clock rate, pattern length, and trigger to make a reference pattern for jitter measurement [18]. The jitter components are measured when the accumulated bit sequences reach 1.06 megabytes of data.

The first classification is total jitter (TJ) decomposition into random jitter (RJ) and deterministic jitter (DJ), which are based on inevitable noise and signal characteristics, respectively. DJ has 3 components: periodic jitter (PJ), data dependent jitter (DDJ), and bounded uncorrelated jitter (BUJ). PJ mainly depends on clock errors and the data patterns can affect DDJ deterioration. Duty cycle distortion (DCD) and intersymbol interference (ISI) are subcomponents of DDJ, and those parameters can explain jitter sources in greater detail.

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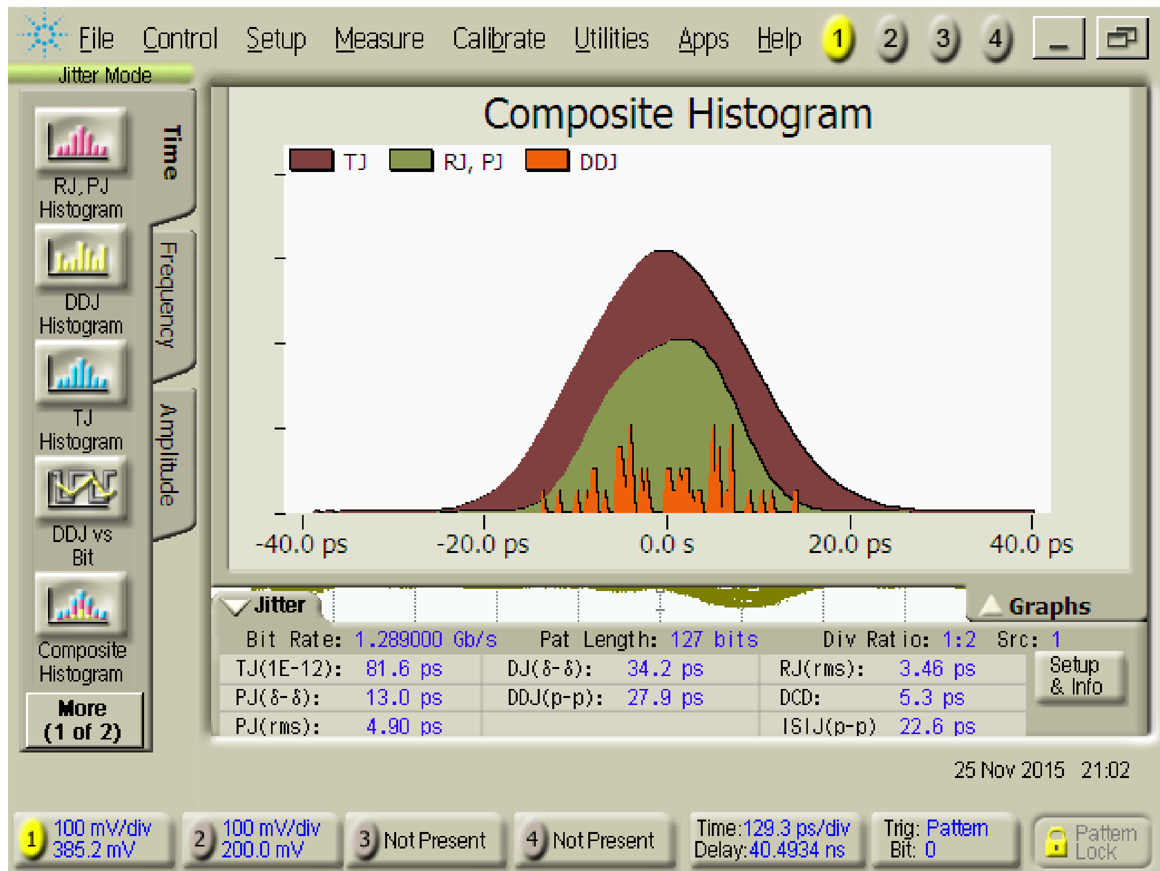

Figure 7. Composite histogram of TJ, RJ, PJ and DDJ

TJ is computed by convolving the RJ histogram with the DJ histogram. The computation process indicates that TJ includes all data correlated or uncorrelated information. The TJ value increases when the signal is travelling through a path degraded by physical damage, so the TJ is regarded as a representative parameter for the overall state of device under test (DUT).

RJ is inevitable Gaussian noise and the sources are thermal and white noise generated in a high-speed digital system. DJ components are generated by relative jitter sources rather than defined randomly and the components are classified into data uncorrelated and correlated jitters. PJ is an uncorrelated jitter, and estimated by the dual Dirac delta model which is a Gaussian approximation to the outer edge of the jitter distribution [19]. Limitation of signal coupling or EMI often result in PJ. In this thesis, RJ and PJ are not critically considered since those are hard to show DUT degradation in terms of signal integrity deterioration.

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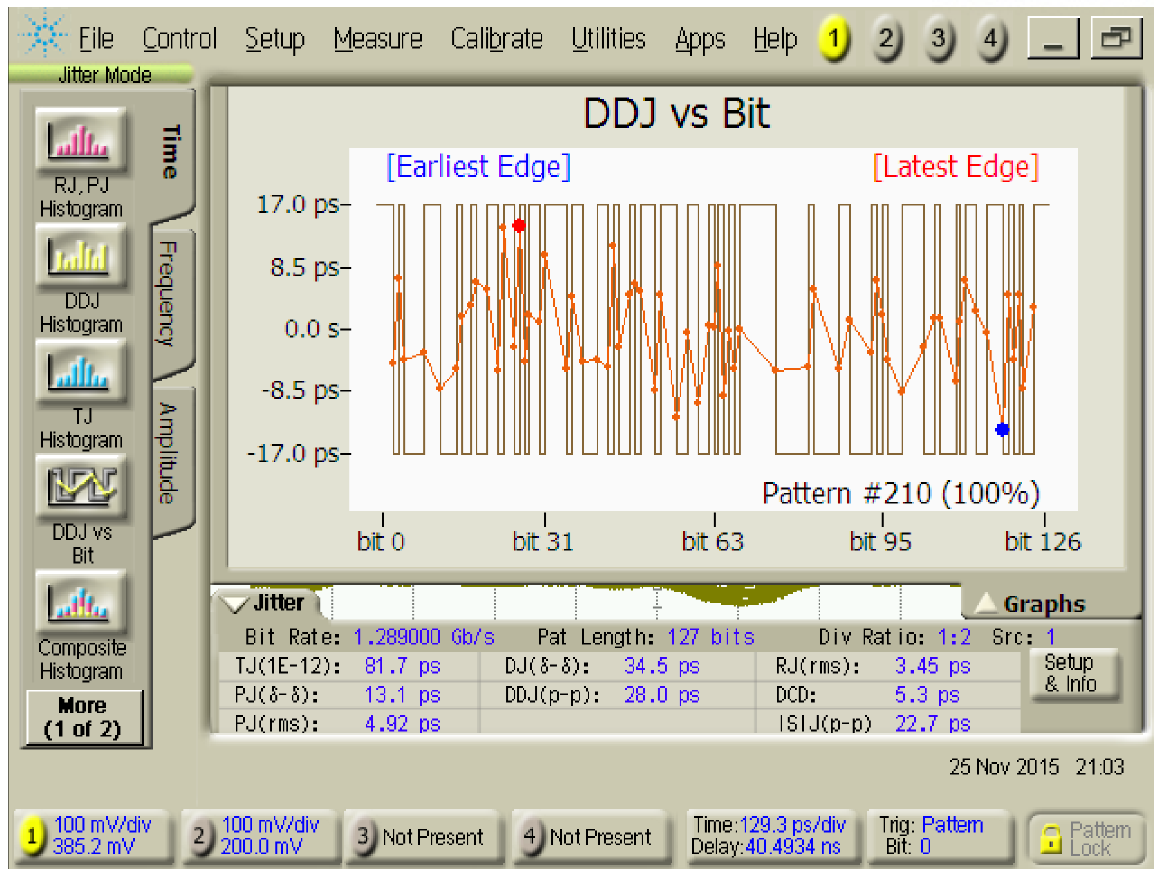

Figure 8. Data dependent jitter

DDJ is a data correlated DJ component and includes information of all rising and falling edges accumulated during a certain period of time. The DDJ subcomponent DCD is defined as the difference between the average of all rising edges and that of falling edges. There are two major causes of DCD: threshold offset of transmitter and asymmetry in rising and falling edge speed [17]. ISI excludes uncorrelated jitter effects by averaging the earliest rising edge and the latest one. ISI is affected by the bandwidth limitation of measurement devices and impedance mismatch at the signal path. A study introduced the ISI application for signal integrity analysis with respect to impedance matching circuit design [20]. ISI was applied for I/O link's BER performance which requires a Gbps-speed signal to characterize signal integrity considering the signal reflection due to the impedance mismatch as well [21, 22]. Therefore, ISI data are used as a key parameter to analyze signal integrity of the degraded DUT in this thesis.

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3.3 Characterizing degradation progress by digital signal

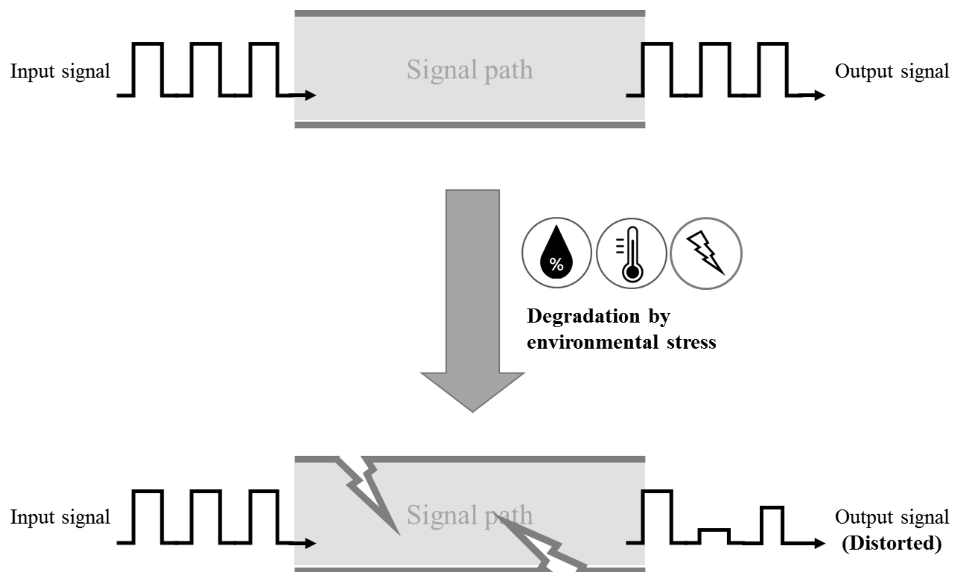

Figure 9. Schematic of signal deterioration due to physical degradation

A sensing method for physical degradation introduced in this thesis starts from the fundamental concept described in Figure 9. Physically damaged signal path can adversely affect to the signal and finally induce system malfunctioning. With this concept, digital signal based sensing method will be explained in this subsection. Followings are the overall boundaries and assumptions of the sensing method.

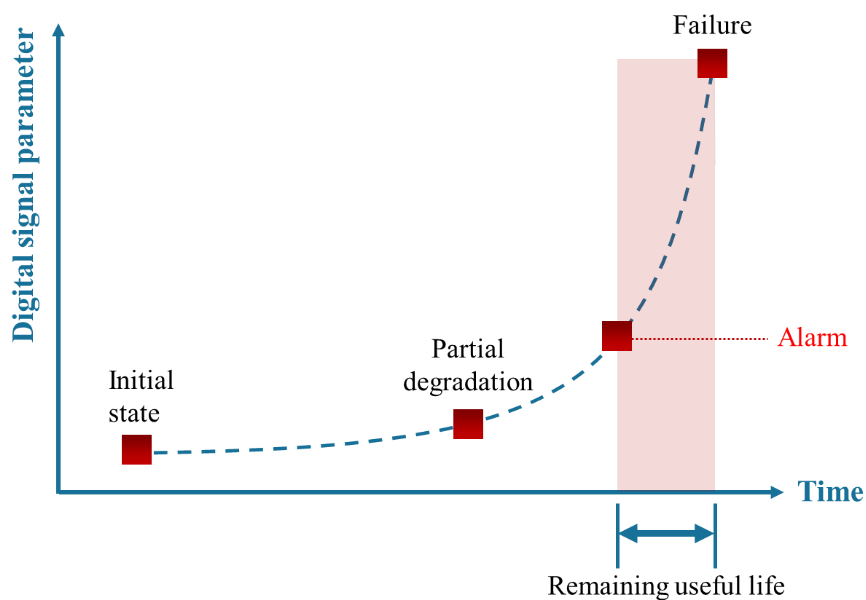

Figure 10. Schematic of characterizing degradation progress

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The digital signal based monitoring basically uses quantitative parameters which represent signal integrity, and final form of the monitoring method would be a prognostic tool for electronic system management. This thesis will cover preliminary study to develope health monitoring and prognosis process. Capability of the digital signal for degradation sensing will be examined through experiments. The examination process is focused on characterizing of the intact and partial degradation states. Thus, the results are expected to support non-destructive failure sensing for electronic systems by digital signal, and be grounds for further development of the system health monitoring. The detail process and expected results of this approach are explained below, and examined through the experiments in the following chapter.

1) Initial state of the target system is confirmed by SI based test.
2) It is necessary to determine the signal specification depending on the system characteristics (e.g. signal speed, clock, and pattern).
3) The target system is exposed to stress conditions which accelerate the degradation until it fails.
4) The partial degradation of the target system is manually reproduced, and compare the parameter values of initial and partially degraded states.
5) Failure analysis (FA) is conducted after the parameter comparison in order to confirm the physical damage of the target system.
6) The significant difference of parameters and FA results will be able to indicate the feasibility of the sensing approach which uses digital signal.

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IV. Partial degradation detection by digital signal

The stress conditions usually induce cumulative damage in the electronic systems including their components and interconnects such as solder joints. Interconnects, especially solder joints in the electronic systems are often considered as major degrading locations by stress conditions. Crack propagation at the solder joints is one of a failure modes, and can lead to the system malfunction. Thus, in this thesis, solder joints will be used as experimental target for partial degradation detection using digital signal.

4.1 Experiment

The experiment conducted in this thesis aims at measuring digital signal parameters with respect to solder joints on the circuit in a non-destructive way. Since the solder joint states are defined depending on the degree of degradation, thermo-mechanical stress was applied at DUT to produce physical damage. This section starts with an introduction of the DUT fabrication process, then the damage application process and measurement setup for digital signal parameters will follow.

4.1.1 DUT Fabrication

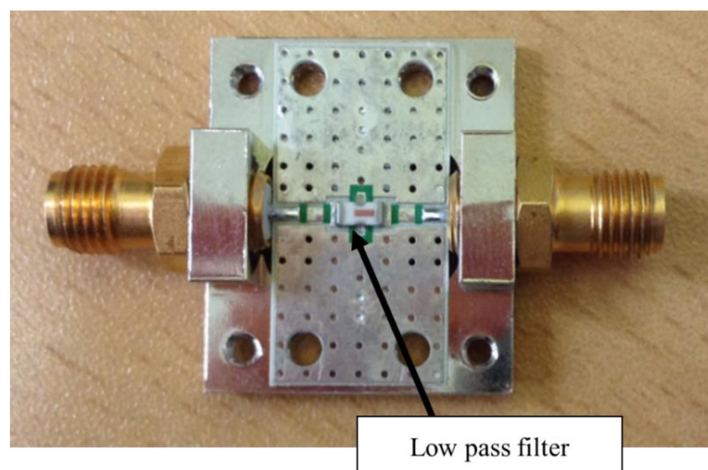

Figure 11. Test board with surface mounted LPF

RF signal requires some specific circuit conditions for stable signal transmission, such as impedance matching. The DUT used in this experiment, TB-270 manufactured by minicircuits, has coplanar waveguide design which has broadband performance and less EMI effect. Surface mounted components on the test board is a sort of low pass filter (LPF) manufactured by minicircuits with 6.7GHz of cutoff frequency. LPF is known as a high frequency factor remover (i.e. HF harmonic, ripples), thus the LPF

can serve as a conductive pass for RF signal within given 6.7GHz cutoff frequency.

The LPF should be surface mounted on the test board with SAC305 which is one of a lead-free solder alloy used for interconnects in electronic system. SAC305 composes of 96.5% Tin, 3% silver and 0.5% copper. Surface mounting process starts from solder paste application on solder mask using stencil, then heat the solder paste by electronic heat gun. Fabricated test boards were examined in order to check initial quality based on test standard which will be introduced in following section (i.e. eye mask test).

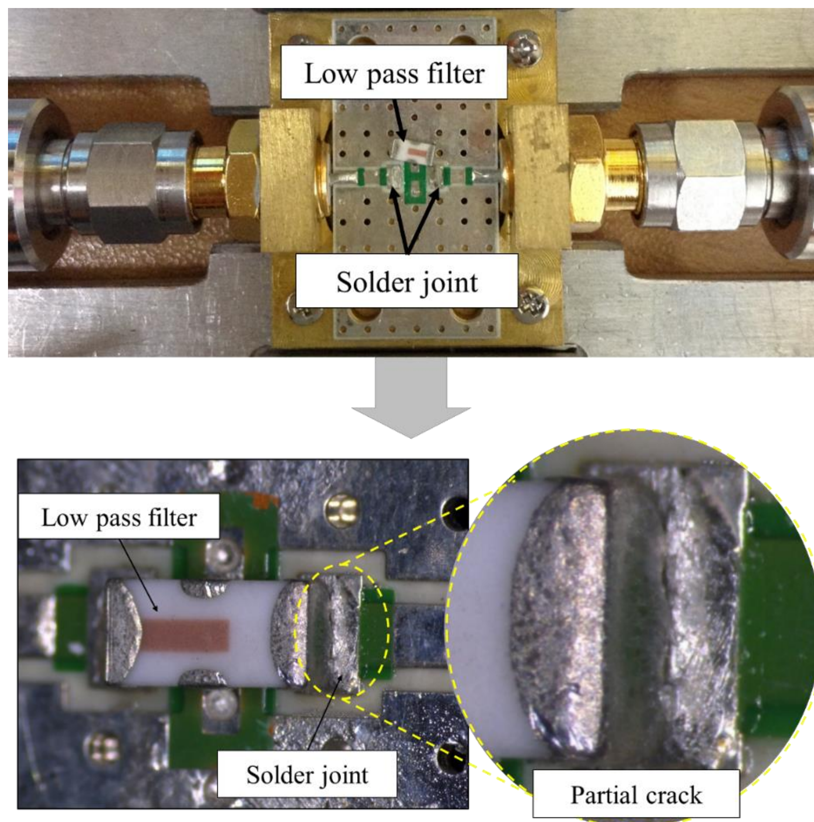

Figure 12. Partial crack reproduction at solder joint

DUT which has been passed the quality test and not been applied designed stress was defined as 'intact' state in the experiment. The constant thermo-mechanical stress was applied until the LPF was completely separated from the test board. Cracked state was reproduced by placing the separated the LPF back on the remaining solder where the LPF was originally connected. Due to the remaining solder, the cracked state DUTs can complete the circuit, preserving the partial crack at the solder joint shown in Figure 12.

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4.1.2. Stress application

Cracked DUT state was reproduced by wear-out failure considering failure mechanisms possible to be occurred in electronic systems, which were creep and stress relaxation. Creep and stress relaxation are defined as a plastic deformation which depends on the time, and those are significantly affected by high temperatures [23]. In addition, homologous temperature, a ratio between the material temperature and the melting point of the material in Kelvin, exceed 0.5 in case of SAC305. Thus, deformation related to creep prone to be occurred [24], and it can be regarded as dominant failure mode. The homologous temperature of SAC305 exceeds 0.5 at room temperature, the elevated temperature and additional stress can effectively accelerate the deformation of SAC305. In case of stress relaxation, stress was applied by constant displacement from the solder joint to the silicon ring, whereas the creep was based on constant stress induced by gravity force. Both mechanical stress conditions were implemented under high temperature, since the deformation induced both failure mechanisms can be accelerated [25].

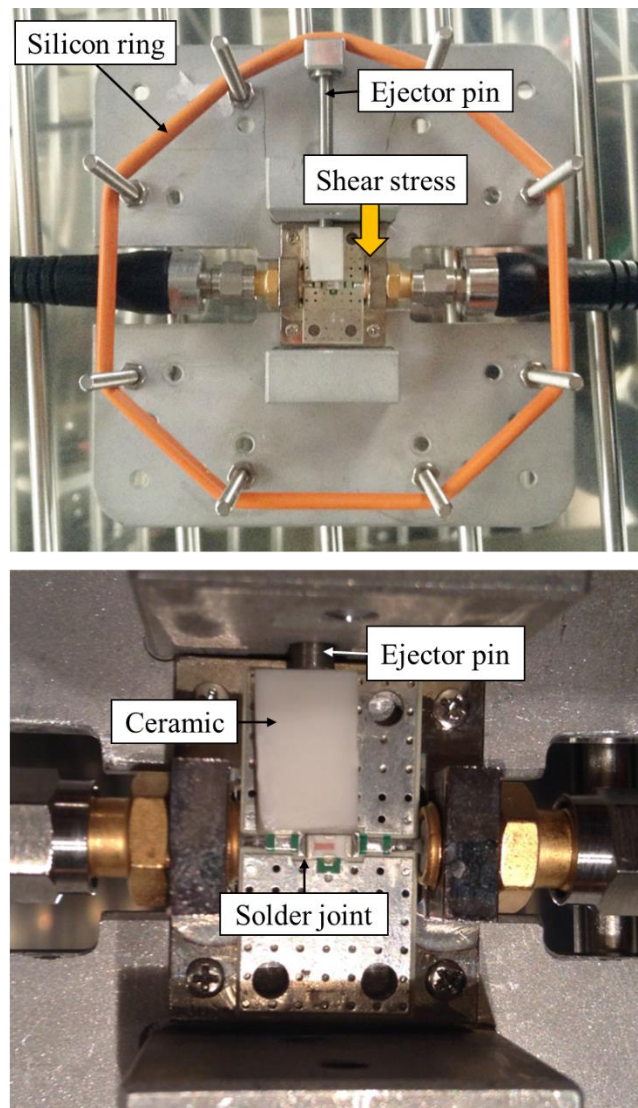

Figure 13. Stress relaxation test setup

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Figure 13 describes a fixture for the mechanical stress application in stress relaxation experiment. The DUT was on the fixture, and SMA coaxial cables connected the DUT to the experimental devices. Heat-resistive silicon ring rings hanging on the 8 bolts applied stress by maintaining constant displacement up to the solder joint and the ejector pin helps stress localization. Since the ejector pin was conductor, a ceramic piece was used to avoid direct contact between the solder joint and the ejector pin.

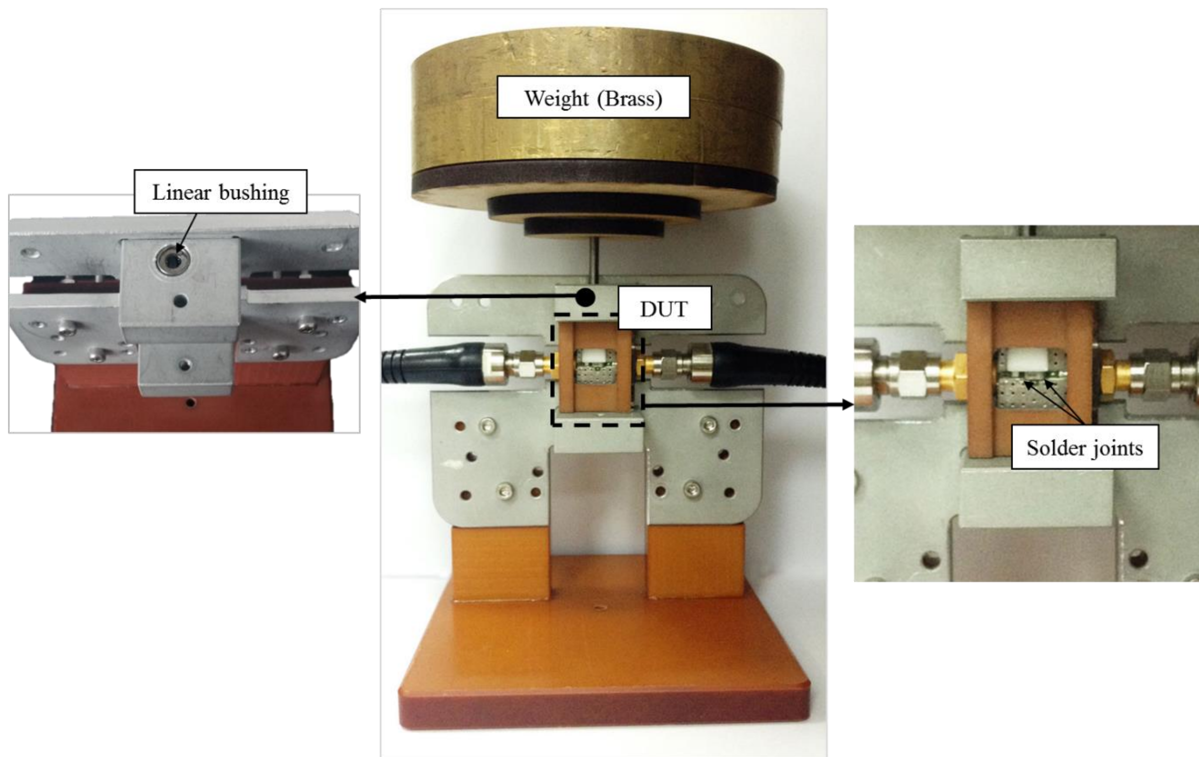

Figure 14. Creep test setup

Another fixture shown in Figure 14 for creep test mainly aimed at applying stress induced by gravity force, and brass weights were placed on the DUT accordingly. 1.9kg of bronze weight was used in order to be stable fixture structure by reducing the volume of the weights compared to other material such as Aluminum. A linear bushing is placed in the hole for the ejector pin and it can serve as a linear guide with less friction during the stress application.

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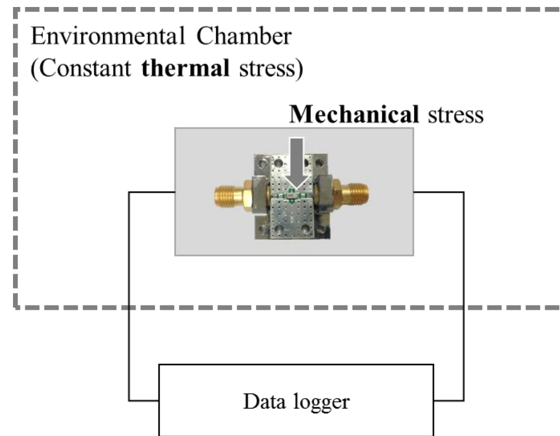

Figure 15. Schematic of stress application setup

Figure 15 shows the schematic of implementation setup to degrade the solder joint. DUT on the fixture was placed in an environmental chamber, and constant themal stress was applied to the DUT. A data logger was connected to DUT, and recorded DC resistance to confirm time-to-failure when the circuit is open.

4.1.3. Measurement setup

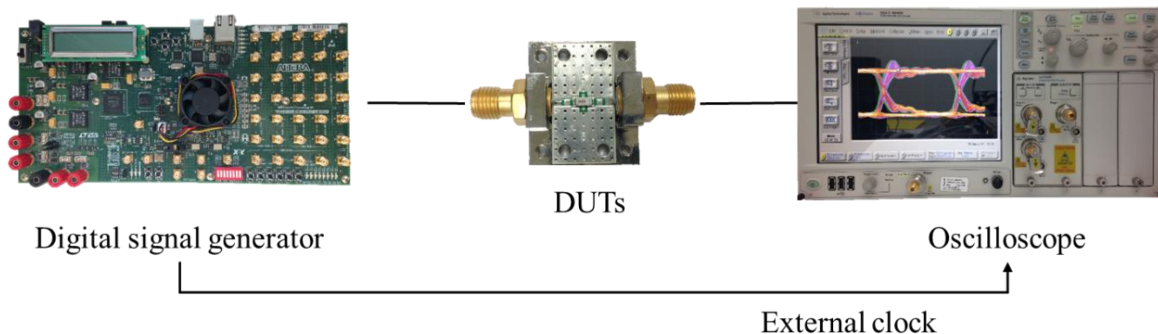

Figure 16. Schematic of parameter measurement setup

Digital signal was generated by Altera Stratix IV, and the signal has Pseudo random binary sequence 7 (PRBS7) pattern with 1.25Gbps of bit rate. The PRBS7 pattern was used for testing the signal path because of its random property. The clock speed was supplied in a frequency of 625MHz from external source at the same time. Keysight 86100D, an oscilloscope, generated eye diagrams which represented the signal integrity of DUTs. Since the eye diagram was generated clearly with large eye opening, 5V of differential output voltage was used. The eye mask test was conducted using the oscilloscope, and the standardized mask (i.e. Gigabit Ethernet mask) was provided.

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4.2 Results

In case of the partially cracked DUTs produced by stress relaxation test, jitter RMS and peak to peak values were analyzed. Then other eye parameters and subcomponents of jitter were used to characterize the partially cracked DUTs produced by creep test in order for further analysis.

Table 1. Jitter variations between intact and cracked states (Stress relaxation test)

Sample ID	Jitter p-p (ps)			Jitter RMS (ps)		
	Intact	Cracked	Variations	Intact	Cracked	Variations
	Mean (Std dev.)	Mean (Std dev.)		Mean (Std dev.)	Mean (Std dev.)	
1	54.15 (3.95)	65.86 (1.44)	21.63%	11.70 (0.50)	13.51 (0.44)	15.45%
2	57.64 (1.42)	64.34 (1.85)	11.62%	11.98 (0.10)	13.45 (0.18)	12.30%
3	45.84 (2.32)	61.42 (1.16)	33.99%	9.56 (0.14)	11.96 (0.14)	25.10%
4	56.82 (2.21)	69.50 (2.40)	22.32%	11.78 (0.16)	13.56 (0.17)	15.11%
5	53.80 (2.02)	65.49 (1.80)	21.72%	10.70 (0.22)	13.24 (0.18)	23.72%
6	55.44 (1.14)	65.06 (2.16)	17.36%	11.51 (0.12)	13.37 (0.10)	16.12%
7	53.16 (1.92)	67.13 (2.14)	26.27%	10.74 (0.17)	13.26 (0.220	23.53%

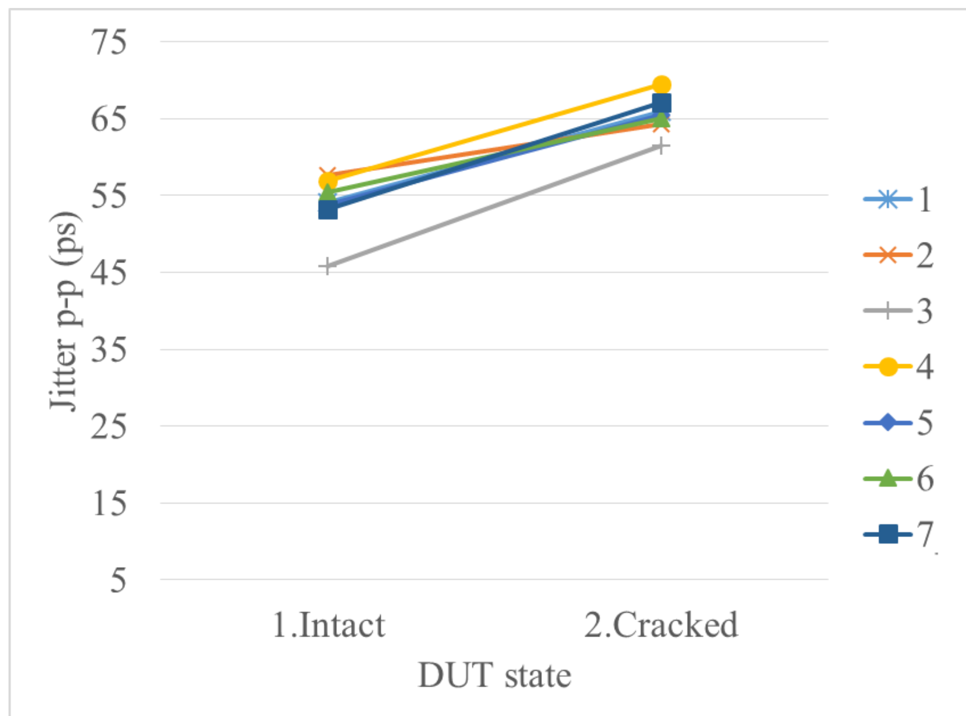

Figure 17. Jitter p-p variations for each sample

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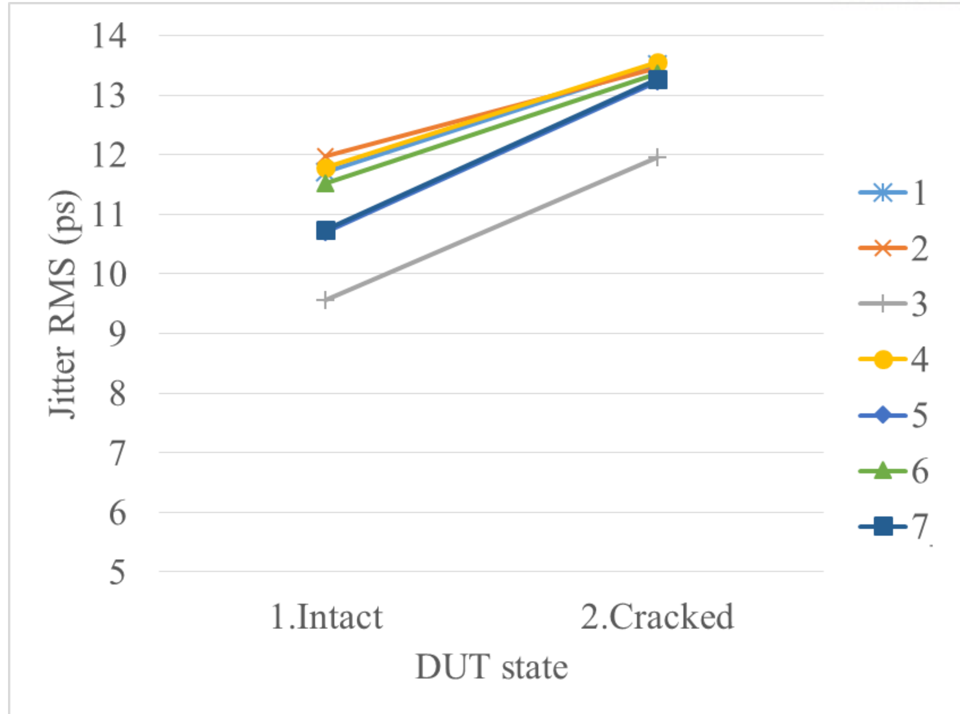

Figure 18. Jitter RMS variations for each sample

The two types of jitters (i.e. jitter RMS and peak to peak) with respect to 7 samples were collected before and after the stress applied to the solder joint. In case of the intact states, the jitter RMS and the jitter p-p were measured with 5 times of repetitions before applying the stress. The measurement procedure was exactly the same in case of the cracked states. The collected data was summarized by the mean value and standard deviation of the repetitions in Table 1, and the mean values were compared to examine the signal integrity in both intact and cracked solder joint states. The results in Figure 17 and Figure 18 showed that the mean values of the jitters increased. ANOVA with 0.05 of significant level was conducted to ensure the meaningful value change based on the measurements. Then, it was confirmed that the jitter variations were statistically significant for all samples and parameters.

Since the jitter RMS and peak to peak proved its capability to distinguish the DUT states, the same analysis procedure was applied to other signal integrity indicators in order to demonstrate that they can show the value difference between the DUTs in opposing states with further information. Following tables and figures will cover the measurement results of eye height, eye width, and jitter components (i.e. TJ and ISI).

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Table 2. Jitter variations between intact and cracked states (Creep test)

Sample ID	Jitter p-p (ps)			Jitter RMS (ps)		
	Intact	Cracked	Variations	Intact	Cracked	Variations
	Mean (Std dev.)	Mean (Std dev.)		Mean (Std dev.)	Mean (Std dev.)	
8	33.87 (3.13)	39.95 (2.33)	17.93%	6.08 (0.14)	6.62 (0.12)	8.80%
9	34.72 (1.91)	39.48 (2.49)	13.71%	6.10 (0.10)	6.58 (0.20)	7.77%
10	34.31 (3.39)	37.78 (2.26)	10.12%	6.05 (0.14)	6.34 (0.150	4.72%
11	34.50 (2.50)	39.30 (3.74)	13.91%	6.09 (0.12)	6.58 (0.150	7.98%
12	36.15 (2.23)	39.42 (1.59)	9.03%	6.03 (0.13)	6.61 (0.130	9.59%
13	36.46 (3.04)	38.79 (2.22)	6.40%	6.13 (0.11)	6.37 (0.20)	3.98%
14	36.95 (2.32)	38.98 (2.92)	5.49%	6.00 (0.13)	6.59 (0.18)	9.85%

Table 3. Eye parameter variations between intact and cracked states (Creep test)

Sample	Eye height (ps)			Eye width (ps)		
	Intact	Cracked	Variations	Intact	Cracked	Variations
	Mean (Std dev.)	Mean (Std dev.)		Mean (Std dev.)	Mean (Std dev.)	
8	327.30 (0.48)	317.40 (0.52)	-3.02%	736.65 (1.33)	734.12 (1.39)	-0.34%
9	328.90 (0.32)	306.20 (4.92)	-6.90%	736.68 (0.60)	735.88 (1.21)	-0.11%
10	330.10 (0.32)	323.60 (0.52)	-1.97%	737.79 (0.87)	736.47 (1.95)	-0.18%
11	329.10 (0.32)	317.10 (0.32)	-3.65%	738.37 (1.38)	715.22 (1.49)	-3.14%
12	329.00 (0.00)	308.70 (0.48)	-6.17%	737.73 (0.77)	715.15 (0.78)	-3.06%
13	327.50 (0.53)	306.90 (0.32)	-6.29%	735.56 (0.64)	715.15 (1.20)	-2.77%
14	329.70 (0.48)	315.30 (0.48)	-4.37%	738.49 (1.77)	715.69 (2.21)	-3.09%

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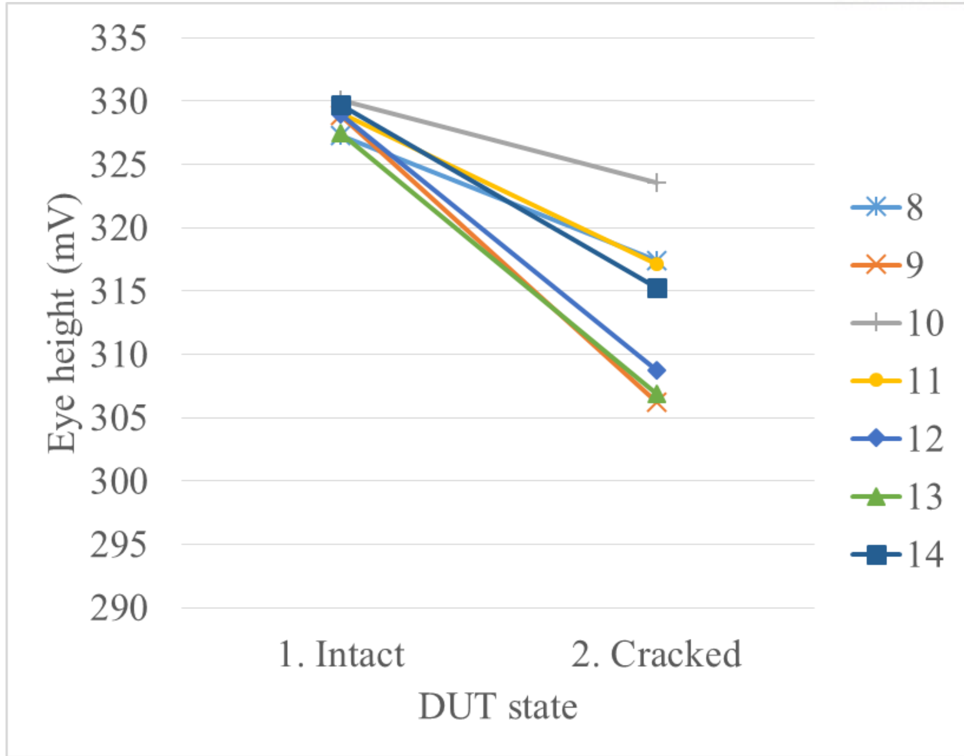

Figure 19. Eye height variations for each sample

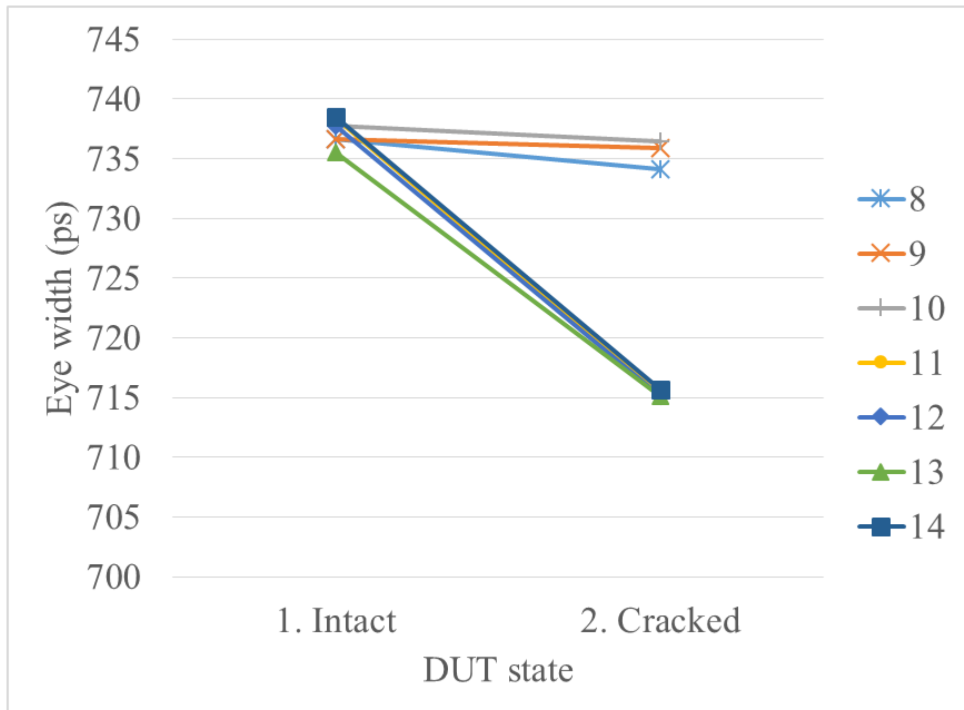

Figure 20. Eye width variations for each sample

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Table 4. TJ and ISI between intact and cracked states (Creep test)

Sample	**TJ(ps)**			**ISI (ps)**		
	Intact	Cracked	Variation	Intact	Cracked	Variation
	Mean (Std Dev.)	Mean (Std Dev.)		Mean (Std Dev.)	Mean (Std Dev.)	
8	77.61 (0.37)	79.32 (0.35)	2.20%	20.61 (0.07)	21.85 (0.11)	6.02%
9	77.65 (0.27)	80.15 (0.27)	3.21%	20.71 (0.17)	23.53 (0.17)	13.56%
10	77.22 (0.44)	79.74 (0.27)	3.27%	19.92 (0.18)	22.27 (0.12)	11.76%
11	77.80 (0.22)	82.20 (0.51)	5.66%	20.42 (0.16)	22.82 (0.19)	11.75%
12	79.04 (0.25)	82.70 (0.34)	4.63%	20.69 (0.46)	24.58 (0.25)	18.81%
13	79.36 (0.42)	81.92 (0.29)	3.23%	21.90 (0.17)	22.44 (0.09)	2.47%
14	78.26 (0.38)	81.18 (0.35)	3.73%	21.16 (0.19)	23.84 (0.11)	12.67%

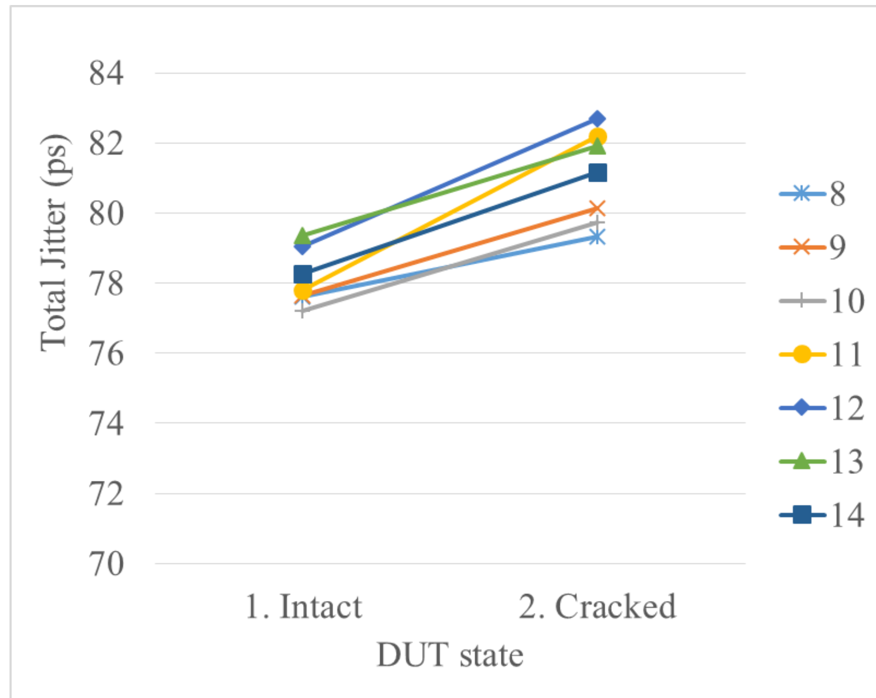

Figure 21. Total jitter variation for each sample

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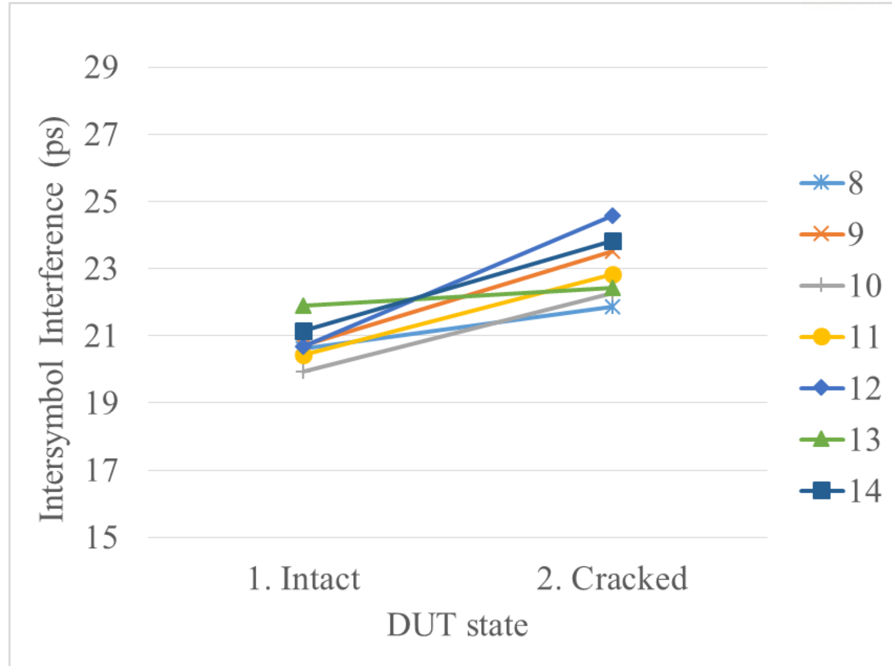

Figure 22. ISI variation for each sample

The results in Table 2 and Table 3 exhibit sampling jitters: eye height and eye width. Significant difference was confirmed through ANOVA except eye width of sample #9 and #10, because the p-values in ANOVA were higher than the significant level in case of both #9 and #10 samples. Jitter components introduced in previous chapters were measured, and the comparison results in Table 4 showed that there were significant jitter variation. Both TJ and ISI significantly increased with respect to all samples.

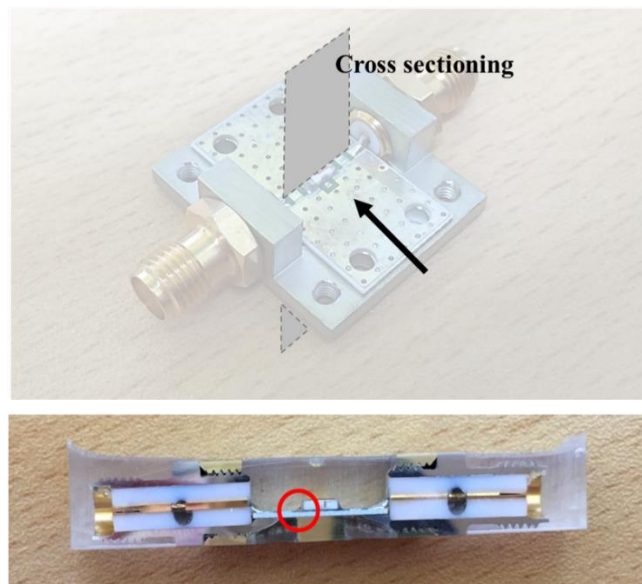

Figure 23. Direction of the DUT cross section

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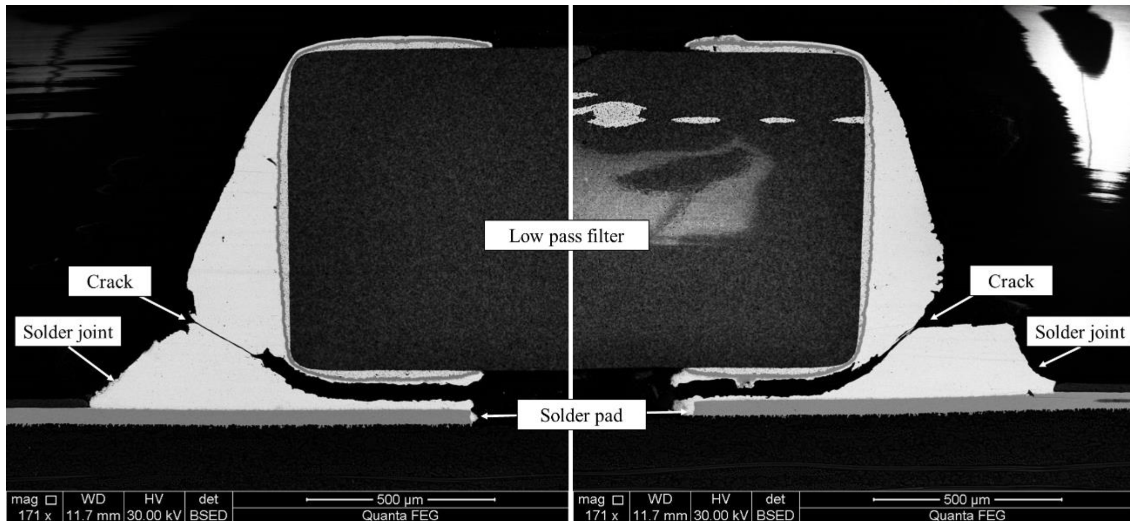

Figure 24. Cross section image of cracked state

The partially cracked state of the DUT was preserved by curing with epoxy resin, and the cross section of the cured DUT was observed by scanning electron microscope (SEM). Figure 24 is the cross section SEM image of sample ID #11.

4.3 Discussions

The increased sampling jitters (i.e. jitter RMS and peak to peak) in the cracked states indicated the deterioration of the signal integrity compared to the intact states. The results can explain the increased deviation of the significant instants of the signal according to the jitter definition. In addition, other SI indicator, eye height, showed signal deterioration in terms of voltage errors. Both eye height and width significantly decreased at the same time, which means eye opening area was reduced due to the DUT degradation. Moreover, it is confirmed that the parameter change actually represents the partial degradation of the solder joint by destructive analysis of the DUT.

As the random noise and the signal data patterns were controlled in both intact and cracked states, the most probable factor that affected to the jitter variations was impedance mismatch caused by the crack at the solder joint. The signal was partially reflected due to the impedance mismatch at the solder joint. This assumption was confirmed through ISI jitter value shown in Table 4, since ISI can be induced by impedance mismatch as explained in the previous chapter. In consequence, the adverse effects on the signal caused by the reflection were detected in a form of jitter variations, especially ISI jitter.

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V. Conclusions and Applications

This study demonstrated that the high speed digital signal characterized the partial crack at the solder joint by eye parameters and jitter. The eye parameters and jitter were determined by the PRBS7 signal travelling the solder joint in a speed of 1.25Gbps. The partial crack at the solder joint was reproduced by using the DUT which went through thermo-mechanical stress. The parameter measurements provided that there were significant variations between the intact and the cracked states of the solder joint. In addition, destructive analysis of the cracked DUT was conducted by using cross-sectioning images, and the results showed that the parameters changed due to partial degradation of the solder joint.

The thesis contributes to develop a non-destructive sensing approach in order to detect the partial degradation of solder interconnect in electronic assemblies by digital signal. A feasibility test conducted in this study can be used as a non-destructive diagnosis method for electronic systems by digital signal characterization. The significant variations of parameters between the solder joint states imply that damages accumulated to an electronic system can be continuously monitored by the digital signal parameters. In order to confirm the continuous monitoring, it is necessary to examine gradual changes in digital signal parameters while electronic systems are being degraded under various stress conditions. The gradual changes can quantify the degradation process which contains precursors of the impending failure.

Succeeding topics should be considered for further development and practical applications in the future. One of topics is applying the approach introduced in the thesis to other types of electronic structures. Most of electronic components are surface mounted on the board, but some components are implemented by using BGA type package. Due to the criticality of those components, BGA health monitoring could help this sensing approach to be extended to commercial application. Putaala [26] introduced solder ball monitoring with RF signal, and the test vehicle included 1 isolated solder ball in impedance controlled signal path. The structure introduced in that literature could be a reference for new test vehicle for future experiments.

Impedance matching is an important issue for digital signal based monitoring especially in terms of practical application. Not all electronic components are impedance controlled, and thus digital signal cannot be fully transmitted due to impedance mismatch. Future studies need to be redefined the parameter sensitivity depending on the physical degradation considering the signal noise induced by impedance mismatch.

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Further research issues need to focus on monitoring the critical failure sites, because it is hard to monitor everywhere in electronic system. Each electronic assemblies or components require specific digital signals for their operation, depending on the functions or performance. Thus, additional experiments are necessary to demonstrate the sensing capability of the specific signals. As aforementioned, the key idea of degradation sensing by digital signal is to quantify relative changes under time dependent degradation. For example, the degradation of the electronic system can be continuously monitored by various speed of digital signals, finally it could improve the applicable scope of the proposed sensing approach.

Towards the parameter sensitivity, the examined parameters have different variations though the parameters were acquired from the same samples. Quantitative analysis for parameter sensitivity was not conducted in this thesis, however the different variation among the parameters provided a possibility of sensitivity difference with respect to the identical physical damage. Thus, the sensitivity analysis will encourage to select the failure critical parameters, and to decide the most proximate cause of the failure.

The sensing approach introduced in this thesis is available as a non-destructive monitoring sensor for electronic systems. It can be developed as a diagnosis and prognosis tool, once the precursors for impending failure are defined by the gradual change of digital signal. The ultimate goal of this approach is to support predictive maintenance of the electronic systems in various fields such as the finished electronic products, systems from defense industry and manufacturing systems.

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