Master's Thesis

Design, Control, and Implementation of High Frequency LLC Resonant Converter

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Approved by

Advisor
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Abstract

A high switching frequency operation has been introduced with much interest in research and industrial areas to improve the power density of power converters. However, its implementation is difficult for an elaborate switch mode power supply which has high efficiency and stable operation. In this paper, a power stage and a feedback controller design will be considered for proper operation, stability, and high power conversion efficiency of the high frequency LLC resonant converter. The power density can be improved by adopting high switching frequency which allows small sized passive components. At the high switching frequency, the size reduction of the passive components such as transformer, and output capacitor will be estimated to obtain the high power density design. In addition, the design method of the magnetizing inductance design method will be derived to achieve the zero voltage switching (ZVS) at the high switching frequency operation.

In aspect of frequency domain, the smaller output capacitor which has small capacitance and low effective series resistance (ESR) changes the small-signal behavior of the converter's power stage. It can make the converter unstable by increasing the crossover frequency in the loop gain of the small-signal model. The effect of the smaller output capacitance should be analyzed for stability analysis using a proper small-signal model of the LLC resonant converter. Therefore, the proper design methods of the feedback compensator are derived to obtain sufficient phase margin in the bode plot of the converter's loop gain for its stable operation. The design considerations of the power stage and the feedback loop will be verified with the performance comparison of 100 kHz and 500 kHz switching frequency LLC resonant converters.

Since the switching performance of state-of-art power switches has been improved, the power converter can operate over a 1 MHz switching frequency. In this paper, GaN E-HEMTs are used to achieve the high switching frequency operation due to its small channel resistance and small output capacitance. However, the GaN E-HEMTs also have different switching operation characteristics to other conventional silicon-based MOSFETs. Therefore, the high speed switching characteristics of the GaN E-HEMT should be analyzed to obtain proper operation for a half-bridge type LLC resonant converter using a boostrap gate drive circuit. Moreover, a soft start algorithm for the high switching frequency is analyzed to suppress inrush currents at the cold start operation of the converter. All the design considerations using the GaN E-HEMT are verified with a 240 W prototype LLC resonant converter operating at 1 MHz switching frequency.

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I. Introduction

Recently, a LLC resonant converter is one of the most attractive topologies in the industrial fields such as LED, TV, computer, and other home appliances. It has many advantages of fewer components than other topologies, small circulating current, and low switching losses using soft switching methods such as zero current switching (ZCS) for the secondary side diode, and zero voltage switching (ZVS) for a MOSFET over entire load condition [1]-[10]. Since the LLC resonant converter has many advantages and has been widely used in industrial field, it is one of the candidates to implement the high switching frequency operations which is one of the latest trends of the switch mode power supply (SMPS). The high frequency switching operation makes the size of passive components small, which increases the power density of the converter. In addition, comparing with conventional hard-switching converters and asymmetrical half-bridge converter, the LLC resonant converter has small switching and conduction losses by the soft switching and the symmetric operation [11]-[15].

To operate the converter with optimal design in aspect of power density, the design considerations for high switching frequency should be derived. When the switching frequency increases, the size of passive components is proportionally decreasing [16]-[20]. The relationship between the cross-sectional area of the transformer's core and the switching frequency should be investigated to design small-sized transformer properly under high frequency operation. In addition, the size of output capacitor can be decreased using the relationship among the effective series resistance (ESR), capacitance, and the switching frequency. They can be mathematically induced and be verified with simulation and experimental results.

As switching frequency increases, the size of the resonant components will be inevitably reduced through proper design methods of the LLC resonant converter. Moreover, small capacitance and small ESR can reduce the size of the output capacitor. However, the small output capacitance induces stability problems due to the lack of phase margin. Therefore, the effect of the output capacitor such as the capacitance and the ESR are investigated using the small-signal model of the LLC resonant converter, which is derived using the extended describing function (EDF) method. Using the small-signal model, the theoretical open-loop gain is measured to obtain the information of the crossover frequency and phase margin according to the conditions of the output capacitor [21]-[26]. Using the measured open-loop gain, the proper output capacitor is then selected for stability. Moreover, the proper feedback compensator can then be designed to obtain sufficient gain and phase margins.

To verify the validity of the proposed design methodology, LLC resonant converters operating at 100 kHz and 500 kHz are implemented with the theoretical method using MATLAB, simulation method using PSIM, and experimental measurements using prototype converters. Comparing with the size of the passive components of 100 kHz switching frequency, the smaller size of the passive components is

proposed at 500 kHz switching frequency. Poor stability due to the small size of the output capacitor is analyzed with the small-signal model. Dominant poles and zeros of the transfer function are measured as the capacitance and the ESR value change. The theoretical open-loop gains are obtained to design the proper feedback loop for enough gain and phase margin. The theoretical control-to-output transfer function using the open-loop gain and the feedback compensator is compared with experimental measurements using an impedance analyzer to verify the results. In addition, to obtain the response of the output impedance of the power converter, the step load responses are measured to verify stable operation indirectly.

In aspect of switching devices, Silicon-based MOSFETs and Silicon Carbade (SiC) MOSFETs cannot ensure stable operation at very high switching frequency, above 1 MHz. Recently, Gallium Nitride High Electron Mobility Transistor (GaN_HEMT) has developed as a high performance switching device at high frequency. In other words, the properties of the GaN device such as temperature characteristics, low drain-source capacitance, low on-resistance, and low gate-source capacitance are better than the performance of the Silicon-based and SiC devices [27]. However, the different operating characteristics of GaN E-HEMT compared with Silicon-based MOSFET should be investigated for extremely high switching frequency power converters using GaN. Therefore, the design methodologies of a 1 MHz LLC resonant converter using GaN E-HEMTs are proposed.

As the switching frequency is increased, the control bandwidth of a digital signal processor (DSP) as a feedback controller is limited to regulate output voltage. Moreover, pulse frequency modulation (PFM) control requires much higher switching frequency for a soft start operation than the switching frequency under steady state operation. To protect the converter from high inrush current at a cold start, a new soft start method is proposed using a PWM and PFM hybrid control method. To verify the validity of all the proposed design method and analysis, LLC resonant converter operating at 1 MHz is implemented with the theoretical method using MATLAB, simulation method using PSIM, and experimental measurements using 240 W prototype converter.

II. Design Considerations for High Power Density

The conventional medium switching frequency LLC resonant converter has been designed with the relationship among Q-factor (Quality factor), voltage gain, and λ which is defined as L_r/L_m, where L_r is the leakage inductance and L_m is the magnetizing inductance. The converter which has high λ needs small frequency modulation to control the output voltage since the higher gain variation is introduced by the higher λ. High λ has small conduction losses with small circulating currents, however it has a demerit under over-load condition because of non-monotonic gain curves.

Small λ is convenient to control the output voltage under over-load condition, however, it requires high frequency modulation to obtain enough voltage gain. Moreover, small λ has high conduction loss which comes from high circulating current. The Q-factor changed by load condition shows the sharpness of the voltage gain near the resonant frequency. Fig. 1 shows the scheme of the LLC resonant converter and Fig. 2 shows the voltage gain curve according to the switching frequency. In this section, design considerations of the resonant network and output capacitance of the LLC resonant converter for high frequency operation will be discussed.

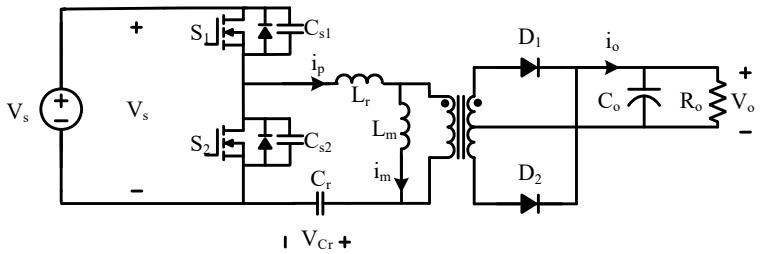


Fig. 1 Circuit diagram of the LLC resonant converter

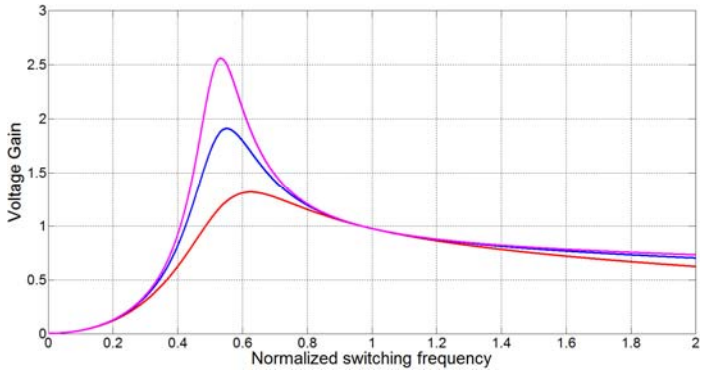


Fig. 2 DC gain characteristics of the LLC resonant converter

2.1 Design for Soft Switching Condition

To verify the validity of the proposed design methodology, a prototype converter is implemented with

an analog controller (ST L6599) which has a fixed dead time (0.2-0.4 μs). Comparing with the switching frequency of 500 kHz (2 μs) in the prototype converter, the dead time is longer than 10% of the switching frequency. Fig. 3 shows theoretical waveforms whose dead time from t_c to t_e is large enough to influence the shape of the primary current. The primary current cannot follow the magnetizing current during the dead time, and it is collapsed by the secondary parasitic capacitance before the end of the dead time.

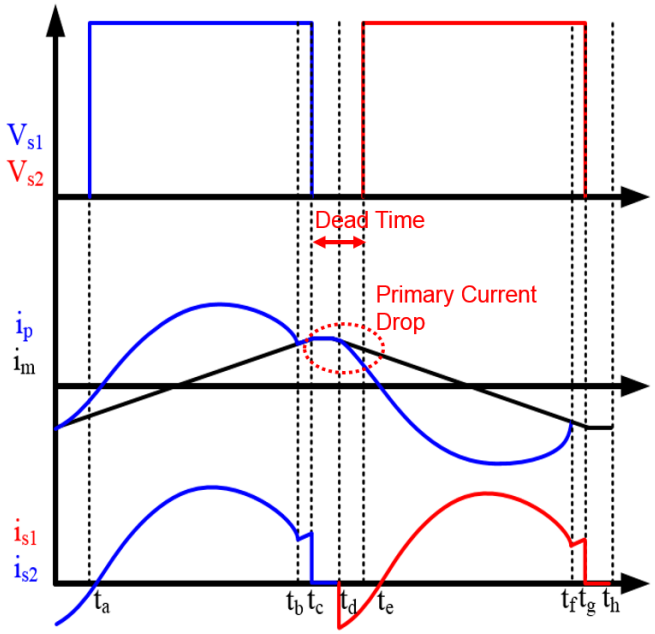


Fig. 3 Operational waveforms of the primary and magnetizing current during dead time

From the above reasons, the conventional design method of the magnetizing inductance is not a proper to obtain the ZVS operation in the high switching frequency operation. Since the conventional design method is derived using the approximation of constant primary current during the dead time, it introduces considerable errors for the ZVS condition. From the conventional design method, the primary current can be expressed as follows:

$$i_p(t_c) = \frac{n(V_o + V_{Df})T_s}{4L_m} \tag{1}$$

where t_c is start point of dead time, $i_p(t_c)$ is the constant value of the primary current during the dead time, n is the turn ratio, V_o is the output voltage, V_{Df} is the forward voltage drop of the secondary diode, and T_s is the switching period.

At the high switching frequency, equation (1) cannot be retained during the dead time. Therefore, after t_c, the variation of the primary current during the dead time can be derived as follows:

$$i_p(t) = i_p(t_c)\cos\omega_{r1}(t) + \frac{V_b}{Z_{r1}}\sin\omega_{r1}(t) \tag{2}$$

where $\omega_{r1} = 2\pi f_{r1}$, $V_b = V_s - V_{cr} - n(V_o + V_{Df})$, V_s is input voltage, f_{r1} is the resonant frequency between the leakage inductance and the resonant capacitor.

The conventional design guide of the magnetizing inductance shown in (3) has high error to obtain the ZVS condition with high dead time ratio.

$$L_m \le \frac{t_{dt}}{16 C_s f_{s,\max}} \tag{3}$$

where t_{dt} is the dead time duration, C_s is the parasitic capacitance of primary side MOSFET, and $f_{s,max}$ is the maximum switching frequency.

To obtain proper ZVS condition at the high switching frequency condition, equation (4) is proposed as follows:

$$\frac{V_s t_{dt}}{8 L_m}(T_{s,\min} - 2t_{dt}) \ge 2 C_s V_s \tag{4}$$

where $T_{s,min}$ is switching period. Equation (4) considers the current drop during the dead time. Assuming that magnetizing current is linear for the dead time, the current drop can be measured using the average primary current from the start of the dead time (t_c, $T_s/4$) to the end of the dead time (t_e, $T_s/4$ – t). Using (4), a proper design guide of the magnetizing inductance to obtain the ZVS condition at the high switching frequency can be derived as follows:

$$L_m \le \frac{t_{dt}}{16 C_s}(T_{s,\min} - 2t_{dt}) \tag{5}$$

Therefore, the magnetizing inductance which guarantee the ZVS of the MOSFET considering the high switching frequency operation with long dead time can be designed.

2.2 Design for Smaller Output Capacitance

At the high switching frequency operation, small-size passive components such as transformer and output capacitor can be used in the converter for high power density. In the case of the output capacitance, the relationship between ESR (effective series resistance) and the output capacitance is important to analyze output voltage ripple as follows:

$$\Delta V = ESR \times \left(\frac{\pi}{2} - 1\right) \times I_o + \frac{\Delta Q}{C_o} \tag{6}$$

where I_o is the output current, T_s is the switching period, and $\Delta Q = 0.363 \times I_o T_s$.

The conventional converter uses high capacitance to reduce the output voltage ripple, but it is not

effective method to increase power density, because capacitance is proportional to the size of the capacitor. From (6), the voltage ripple related with the output capacitance is proportional to the output current and inversely proportional to the switching frequency. The voltage ripple from the ESR, however, is only related to the output current.

Fig. 4 shows output voltage ripple variations according to the switching frequency, which is derived from (6). Using Fig. 4 and (6), it is verified that the ESR is dominant factor to reduce the output voltage ripple than output capacitance at the high switching frequency. Therefore, the small ESR, and output capacitance is selected to improve the output voltage ripple, and the power density of the converter at the high frequency operation. The table 1 and Fig. 5 show three simulation results to verify (6) and Fig. 4.

The case 1, which has normal ESR, and small capacitance condition, shows that capacitance is not dominant to the output voltage ripple at high frequency operation, comparing with normal frequency operation. The case 2, which has high ESR, and small capacitance condition, shows that ESR has a high effect on the output voltage ripple at high switching frequency.

TABLE I

DESIGN SPECIFICATIONS AND SIMULATION RESULTS OF OUTPUT RIPPLE VOLTAGE

Specification		Value
Input Voltage		420 V
Output		30 V/10 A
Case 1	Output Capacitance (ESR)	3 μF (15mΩ)
Case 2	Output Capacitance (ESR)	3 μF (100mΩ)
Case 3	Output Capacitance (ESR)	6600 μF (100mΩ)

Simulation Condition		Output Ripple Voltage
Case 1	100 kHz	5.84 V_{pk_pk}
	500 kHz	1.37 V_{pk_pk}
Case 2	100 kHz	6.86 V_{pk_pk}
	500 kHz	2.81 V_{pk_pk}
Case 3	100 kHz	2.06 V_{pk_pk}
	500 kHz	2.63 V_{pk_pk}

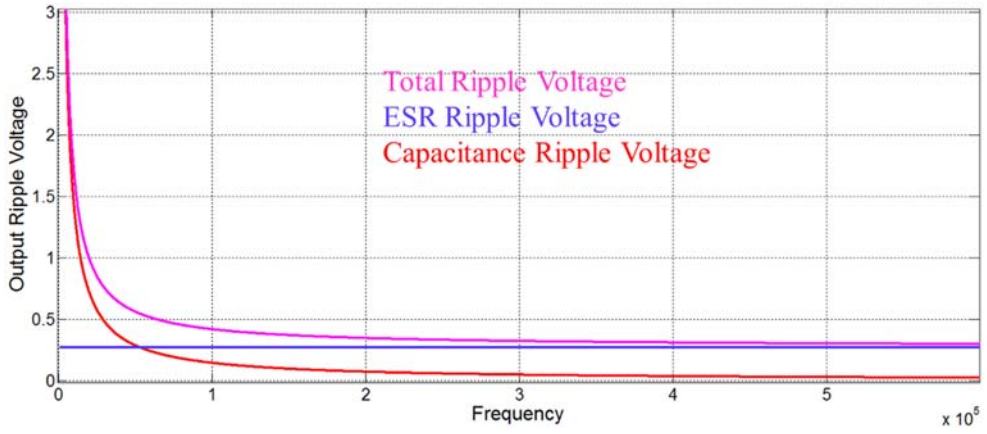
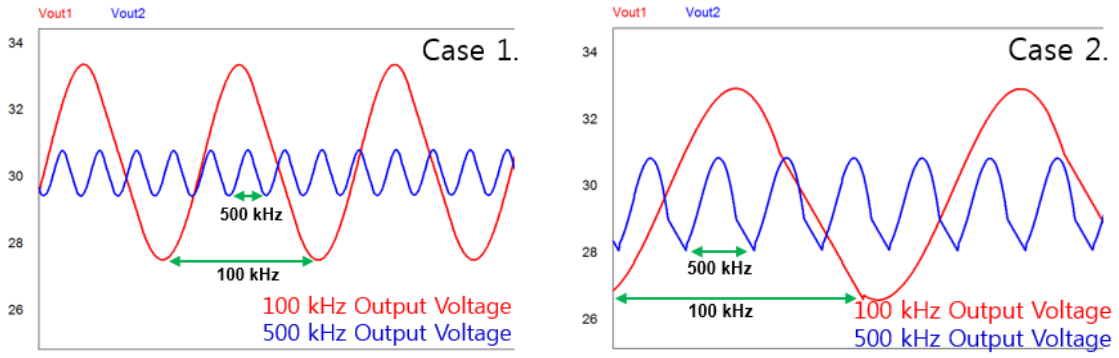
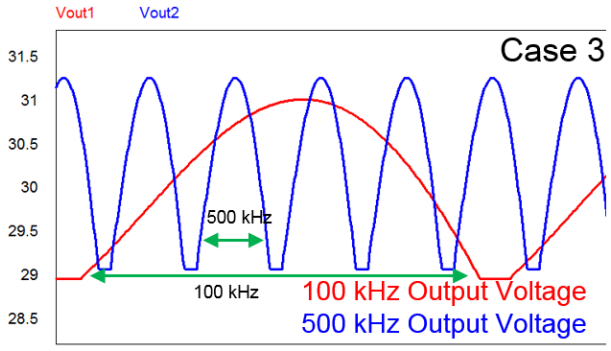


Fig. 4. Ripple voltage variation according to the switching frequency



(a) (b)



(c)

Fig. 5 Simulation waveform of output ripple voltage: (a) normal ESR, and small capacitance condition, (b) high ESR, and small capacitance condition

2.3 Design for Smaller Transformer

The size of the transformer is determined by the cross-sectional area of the core. Equations (7) and (8) show the relationship of the cross-sectional area using the faraday's law as follows:

$$V_1(t) = N_p \times \frac{d\Phi}{dt} = N_p \times \frac{d(B \times A_c)}{dt} \tag{7}$$

$$A_c = \frac{\overline{V_1} \times D \times T_s}{\Delta B \times N_p} \tag{8}$$

$$L = L_m + L_{l1} + L_{l2} = \frac{N_p{}^2}{(R_c + R_g)} \tag{9}$$

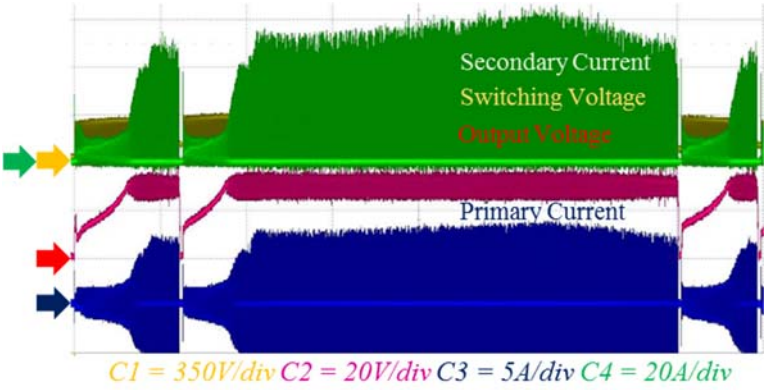
$$A_c = \frac{(D \times \overline{V_1})^2}{\Delta B^2 \times f_s^2 \times L} \times \mu_0 \times \left(\frac{\mu_e}{l_e} + \frac{1}{l_g} \right) \tag{10}$$

where Ac is the cross-sectional area, V_1(t) is the input voltage, $\overline{V_1}$ is the average value of the input voltage, D is the duty ratio, ΔB is the maximum flux density, N_p is the primary turn number of the transformer, μ_o is the free-space permeability, μ_e is the relative magnetic permeability, R_c is the reluctance of core, R_g is the reluctance of air gap, l_e is the effective magnetic length, and l_g is the air gap length.

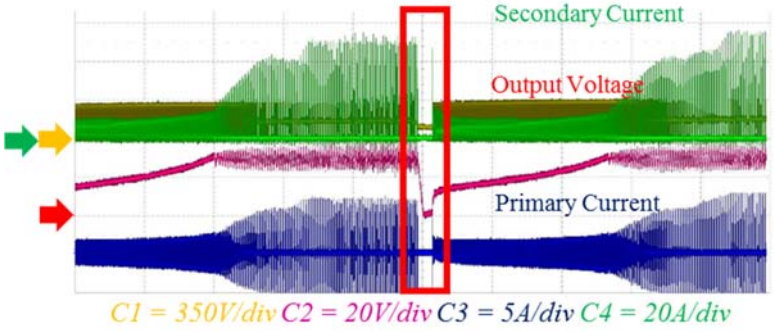
As shown in (8), the cross-sectional area is proportional to the input voltage, the duty ratio, and the switching period. It is inversely proportional to the maximum flux density and the primary turn number. In addition, N_p in (8) can be substituted with (9) as shown in (10). In (10), the transformer permeability and the length of the air gap is derived from (8) and its air gap resistance. The size reduction of the transformer and the air gap length is proportional to the square of the switching frequency. Also, the small leakage and magnetizing inductance value at high switching frequency induces large air gap length. Assuming that the square of ΔB and ($D \times V_1$) is constant, the small-sized transformer can be used at 500 kHz switching frequency since $\mu_o(\mu_e l_e^{-1} + l_g^{-1})$ value increases about 2 times and the value of L decreases about 3.5 times. Consequently, the transformer size at 500 kHz switching frequency can be reduced around 3.5 times than the transformer at 100 kHz switching frequency.

III. Feedback Loop Design for High Power Density

To improve the power density of the power stage, the size of the passive components in the converter must be reduced. The resonant components such as the magnetizing inductance, the leakage inductance, and the resonant capacitance are inevitably reduced with the increase of the switching frequency. The small output capacitor is selected to improve the power density. However, it induces poor stability as shown in Fig. 6.



(a)



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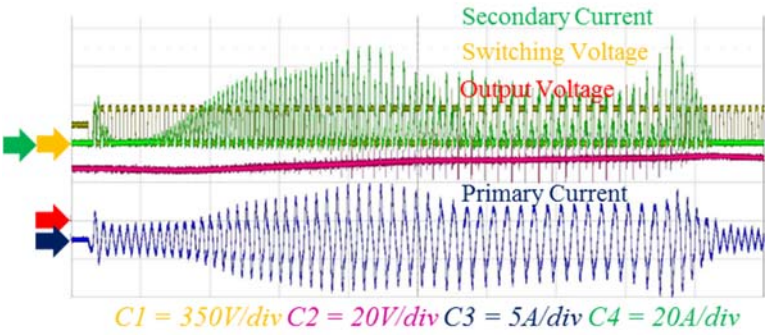


(c)

Fig. 6. Unstable operation of 500 kHz prototype converter: (a) High current peak by burst mode, and brownout protection, (b) Operational waveform of brownout protection, (c) Unstable current waveform

by drastic frequency variation.

The output voltage cannot be regulated by the feedback control, which operates in a burst mode which induces high peak current at full load. The burst mode should be activated to save the standby power at light load. However, burst mode operation at full load induces high peak current which break the switching devices down. Due to the burst mode even at full load, the brownout protection is activated to prevent high circulating current on the primary side. The solution of the unstable operation will be a proper design of the feedback compensator to obtain adequate stability margin.

The theoretical analysis of open-loop gain is important to design an optimal feedback-compensator for stable and fast dynamic operations. The conventional small-signal model of PWM converters is obtained from the state-space averaging method derived by approximations when the natural frequency is much lower than the switching frequency. However, the state-space averaging method has no validity for resonant converters because the switching frequency is located near the natural frequency. The small-signal model using an EDF is considered for the high natural frequency and switching harmonics to improve the model accuracy for the LLC resonant converter [26]. Using the EDF method, transfer functions of the LLC resonant converter such as control-to-output and input-to-output transfer functions can be obtained.

In this section, the analysis of the small-signal model is shown according to the variation of the output capacitance and the ESR at high switching frequency to obtain the variation of the locations of crossover frequency and phase margin. In addition, a proper design method of the feedback compensator will be proposed to achieve high power density with small output capacitance and ESR.

3.1 Instability of Power Converter and Derivation of Small-Signal Model

The small-signal model of the LLC resonant converter has been proposed in previous researches [18]-[21]. To obtain a high accuracy model of the converter, the line resistance and the effective series resistance (ESR) of the output capacitor should be considered. The average model is illustrated in Fig. 7, which contains the line resistance, and the ESR of the output capacitor [23].

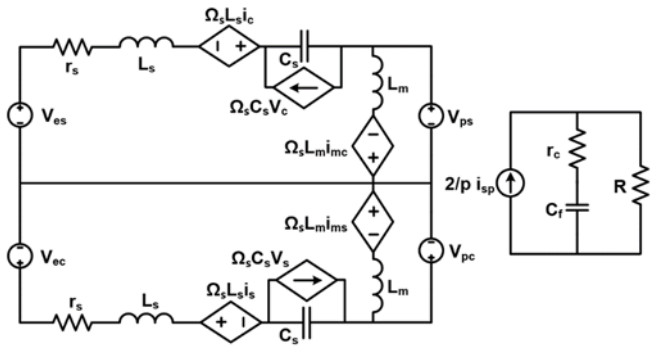


Fig. 7. Average circuit model of the LLC resonant converter

This average model is separated into DC components and small-signal AC components to analyse the small-signal response. Therefore, the small-signal model can be derived with linearization of average model using the small-signal AC components at the DC operating point. The state-space model of the LLC resonant converter is shown as follows:

$$A=\begin{bmatrix} -\frac{H_{ip}+r_s}{L_s} & -\frac{\Omega_s L_s+H_{ic}}{L_s} & -\frac{1}{L_s} & 0 & \frac{H_{ip}}{L_s} & \frac{H_{ic}}{L_s} & -\frac{H_{vcf}}{L_s} \\ \frac{\Omega_S L_s-G_{ip}}{L_s} & -\frac{G_{ic}+r_s}{L_s} & 0 & -\frac{1}{L_s} & \frac{G_{ip}}{L_s} & \frac{G_{ic}}{L_s} & -\frac{G_{vcf}}{L_s} \\ \frac{1}{C_s} & 0 & 0 & -\frac{C_s\Omega_s}{C_s} & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & \frac{C_s\Omega_s}{C_s} & 0 & 0 & 0 & 0 \\ \frac{H_{ip}}{L_m} & \frac{H_{ic}}{L_m} & 0 & 0 & -\frac{H_{ip}}{L_m} & -\frac{H_{ic}+L_m\Omega_s}{L_m} & \frac{H_{vcf}}{L_m} \\ \frac{G_{ip}}{L_m} & \frac{G_{ic}}{L_m} & 0 & 0 & -\frac{G_{ip}-L_m\Omega_s}{L_m} & -\frac{G_{ic}}{L_m} & \frac{G_{vcf}}{L_m} \\ \frac{K_{is}r_c'}{C_f r_c} & \frac{K_{ic}r_c'}{C_f r_c} & 0 & 0 & -\frac{K_{is}r_c'}{C_f r_c} & -\frac{K_{ic}r_c'}{C_f r_c} & -\frac{r_c'}{RC_f r_c} \end{bmatrix}$$

$$B=\begin{bmatrix} -\frac{L_s w_0 I_c}{L_s} & \frac{L_s w_0 I_s}{L_s} & -\frac{C_s w_0 V_c}{C_s} & \frac{C_s w_0 V_s}{C_s} & -\frac{L_m w_0 I_{mc}}{L_m} & \frac{L_m w_0 I_{ms}}{L_m} & 0 \end{bmatrix}$$

$$C=\begin{bmatrix} K_{is}r_c' & K_{ic}r_c' & 0 & 0 & -K_{is}r_c' & -K_{ic}r_c' & \frac{r_c'}{r_c} \end{bmatrix}$$

$$D=0$$

$$\frac{d\hat{x}}{dt}=A\hat{x}+B\hat{u},\quad \hat{y}=C\hat{x}+D\hat{u}$$

$$\frac{\hat{v}_o}{\hat{w}_{sn}}=C(SI-A)^{-1}B+D \tag{11}$$

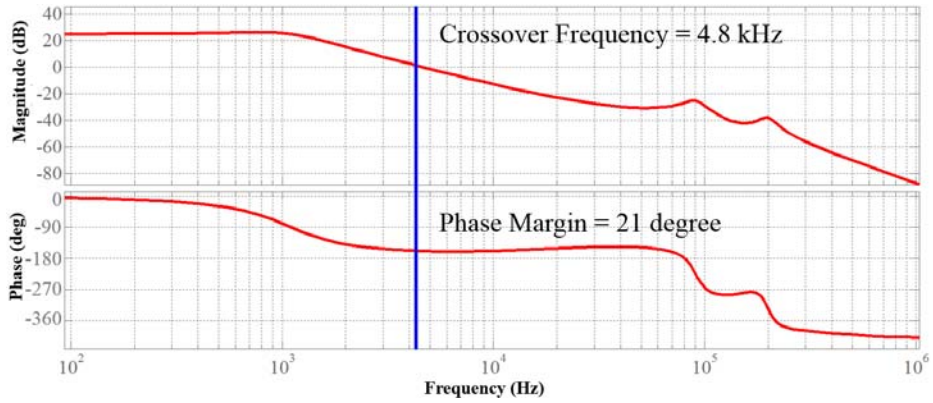
where $\hat{x}=(\hat{i}_s,\hat{i}_c,\hat{v}_s,\hat{v}_c,\hat{i}_{ms},\hat{i}_{mc},\hat{v}_{cf})$ are variables of the LLC resonant converter, $\hat{u}=(\hat{w}_{sn})$ is the control input, and $\hat{y}=(\hat{v}_o)$ is the output.

Table II shows the parameters of the theoretical model derivation. The theoretical results are obtained by the model derivation with MATLAB software, and experimental results are measured using a gain-phase analyser (PSM3750 manufactured by N4L). Fig. 8 shows the theoretical analysis and the experimental results at 100 kHz switching frequency. The closed-loop gain at 100 kHz switching frequency shows a stable operating condition with sufficient phase margin of 65°. To achieve phase margin like 65° at 100 kHz, the effect of the output capacitance should be considered to properly design the feedback compensator for high power density.

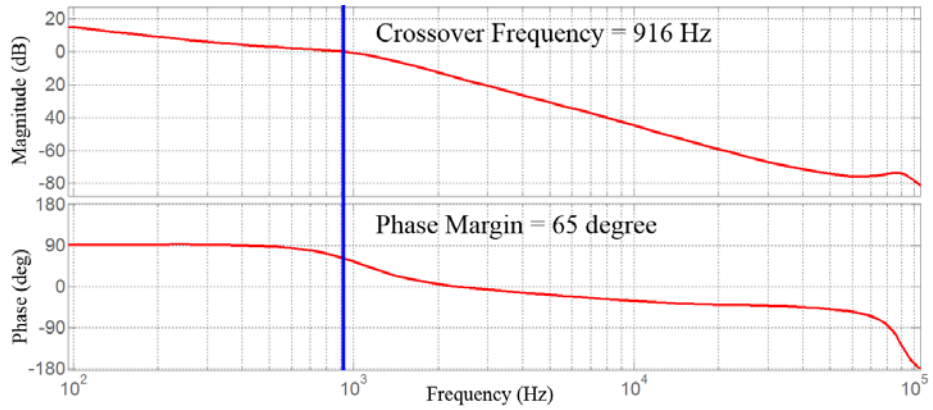
TABLE II

SPECIFICATION OF THEORETICAL SIMULATION

Specification	100 kHz frequency	500 kHz frequency
Input Voltage	420 V	420V
Output Load	30V/10A	30V/10A
Magnetizing Inductance	280 μH	63 μH
Leakage Inductance	90 μH	20 μH
Resonant Capacitance	18 nF	4 nF
Output Capacitance	6600 μF 9 mΩ	1049 μF 5.6 mΩ
Line Parasitic Resistance	1 Ω	1 Ω
Resonant Frequency	125 kHz	562 kHz



(a)



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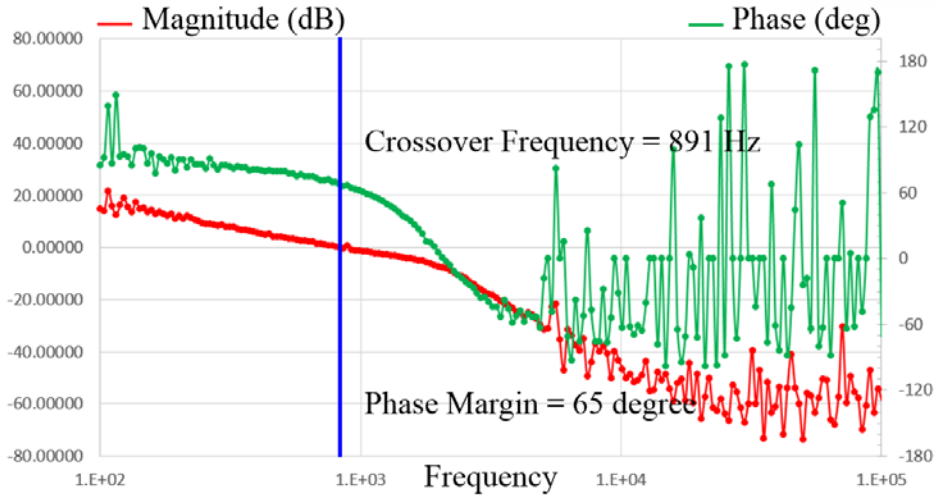
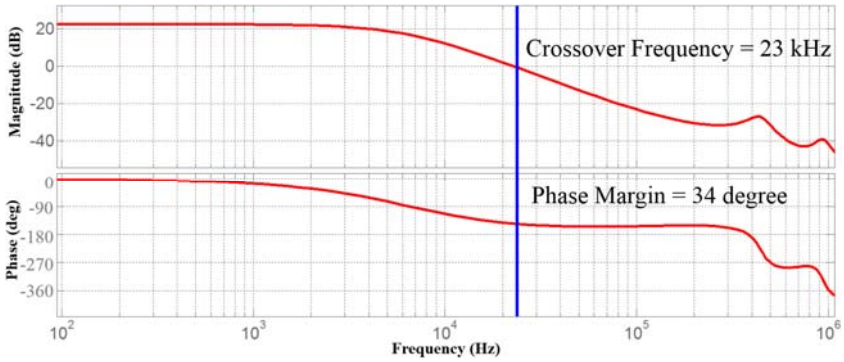


(c)

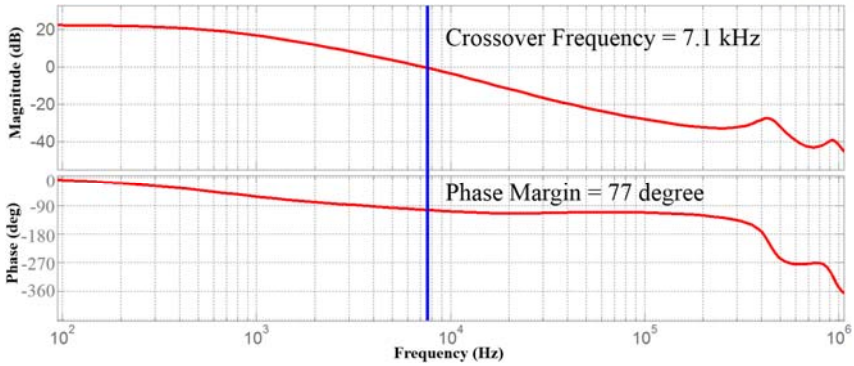
Fig. 8. Theoretical and experimental results of 100 kHz small-signal response: (a) Theoretical result of open-loop gain, (b) Theoretical result of closed-loop gain, (c) Experimental result of closed-loop gain

Fig. 9 shows the comparison of the pole placements of the open-loop gain according to the output capacitance at 500 kHz switching frequency with bode plot and pole-zero map. The small output capacitance results in a much higher frequency location of the first two poles and the zero, which makes higher crossover frequency than with high output capacitance. Moreover, the significant frequency difference between the poles and the zero induces the drastic drop of phase margin in the open-loop gain. In addition, the effect of the high ESR is investigated to obtain the overall effects of the output capacitor for high power density. Fig. 10 shows the characteristics of the 1000 μF and 100 mΩ case compared with the 1049 μF and 5.6 mΩ case that is already shown in Fig. 9 (a).

The high ESR results in a much lower frequency location of the zero, which induces high crossover frequency and high phase margin by the gradual magnitude slope and earlier phase boost. Therefore, the high ESR has advantages in terms of stability with fast dynamics and high phase margin; however, it induces high output voltage ripple and high power loss in the output capacitor at high switching frequencies.



(a)



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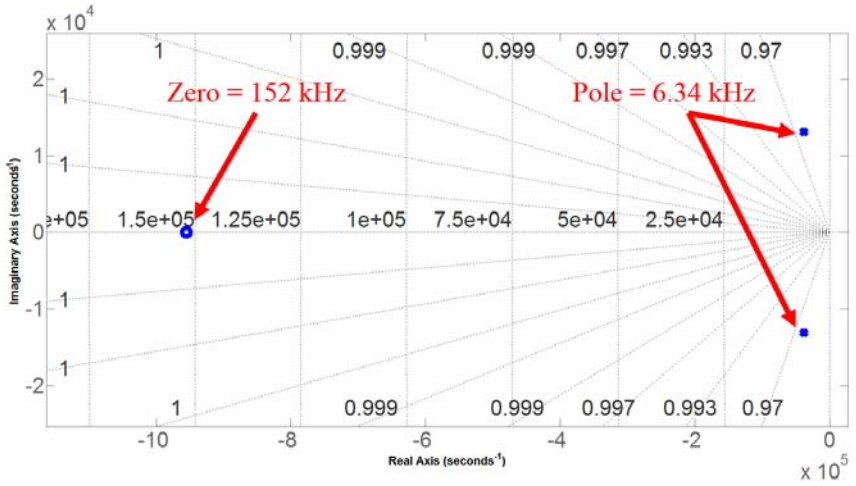

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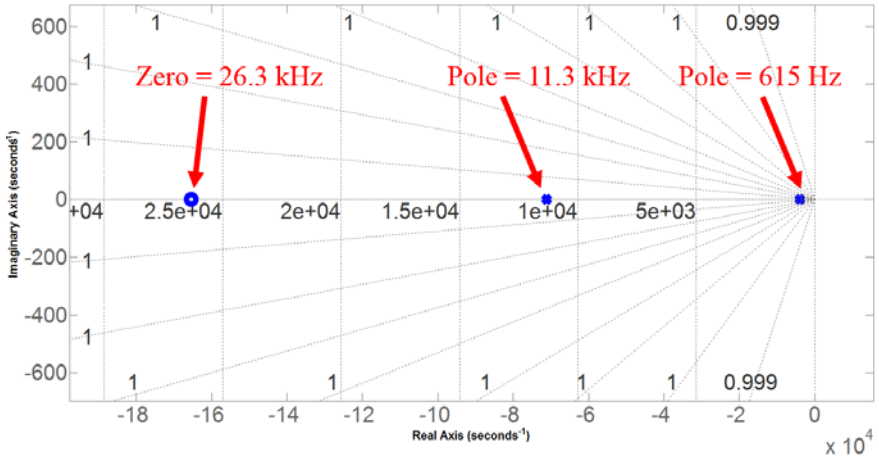
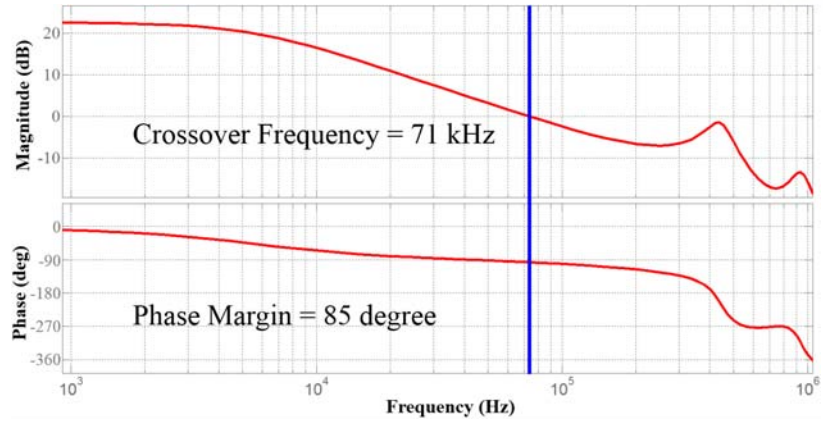
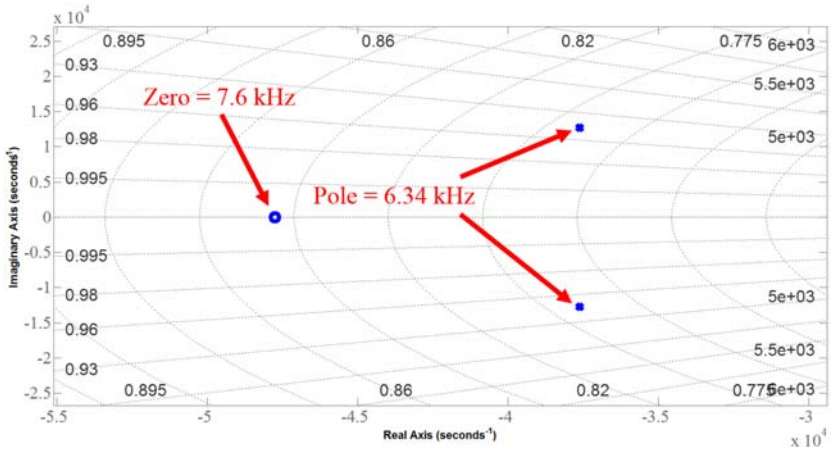


(d)

Fig. 9. Pole placement comparison of open-loop gains according to output capacitance: (a) Bode plot of 1049 μF output capacitance, (b) Bode plot of 6600 μF output capacitance, (c) Pole-zero map of 1049 μF output capacitance, (d) Pole-zero map of 6600 μF output capacitance



(a)

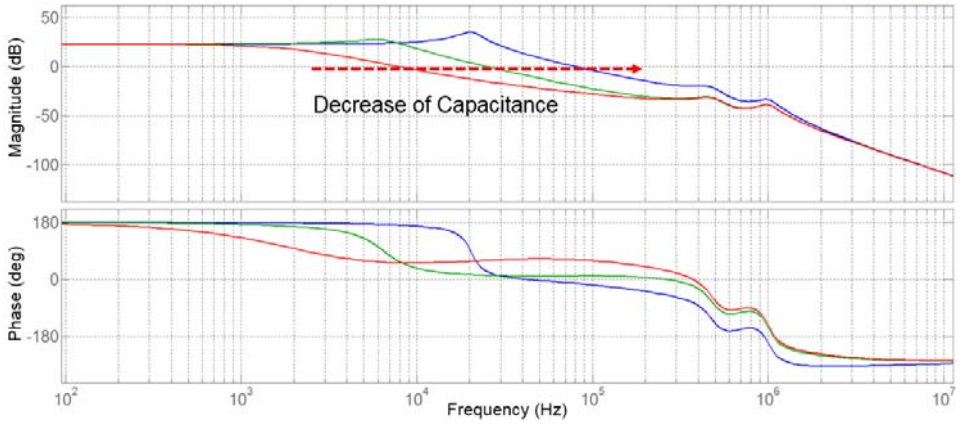


(b)

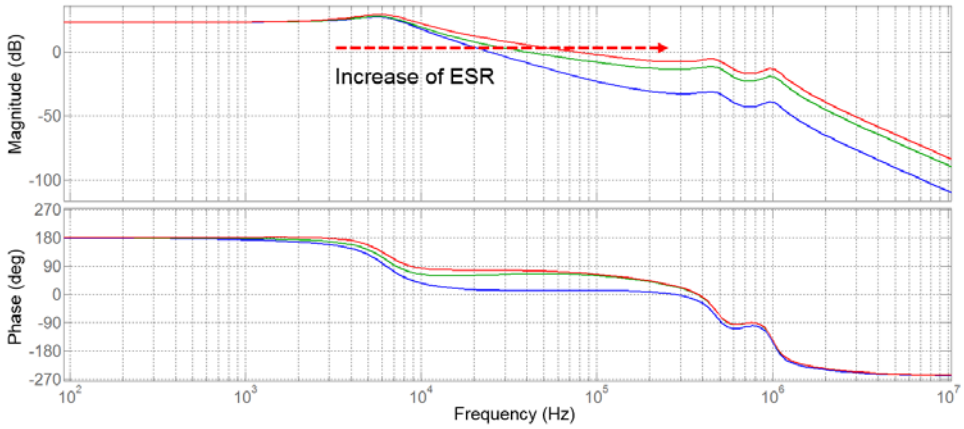
Fig. 10. Theoretical small signal response and pole-zero placement with small capacitance and high ESR: (a) Bode plot of 1049 μF and 100 mΩ case, (b) Pole-zero map of 1049 μF and 100 mΩ case

The open-loop gain with respect to the output capacitance and the ESR is obtained to analyze the variation of the crossover frequency as shown in Fig. 11. The smaller output capacitance induces a higher crossover frequency and smaller phase margin. The higher ESR induces higher crossover frequency and bigger phase margin. The small output capacitor that induces high crossover frequency and low phase margin incurs unstable operation of the converter, as shown in Fig. 12. Therefore, a proper output capacitor must be selected for stability, power conversion efficiency, and high power density.

Without considering the nonlinearities of the transfer function, such as sampling effect and the nonlinear transfer function of a PWM generator in the high frequency region, the high crossover frequency has better performance at high ESR condition in the viewpoint of fast dynamics. However, in order to select the proper capacitor, the nonlinearity should be considered to obtain the loop-gain for high accuracy in the high frequency region.



(a)



(b)

Fig. 11. Comparison of open-loop gain according to output capacitance and its ESR: (a) Gain curve variation according to output capacitance (100 μF, 1000 μF, and 1mF), (b) Gain curve variation according to ESR (1 mΩ, 10 mΩ, and 20 mΩ)

The nonlinearity induces an undesired phase drop of the small-signal response, which is significant at the high frequency region. To reduce the side effect of the nonlinearity, the crossover frequency should be lower than the Nyquist frequency. Moreover, to provide the attenuation of high frequency noise caused by switching devices, the magnitude of the small-signal response of the feedback loop should descend over the crossover frequency [19]. In addition, the higher ESR induces more power losses and the larger output voltage ripple, which is not proper to the precise regulation of the output voltage. Therefore, the output capacitor that has smaller capacitance and smaller ESR should be selected to obtain smaller output voltage ripple, lower power losses, and higher power density, even though the high ESR has high phase margin and high crossover frequency in the open-loop gain. Finally, the feedback compensator should be designed by considering the above effects to obtain enough phase margin with proper crossover frequency under high power conversion efficiency operation of the LLC resonant converter.

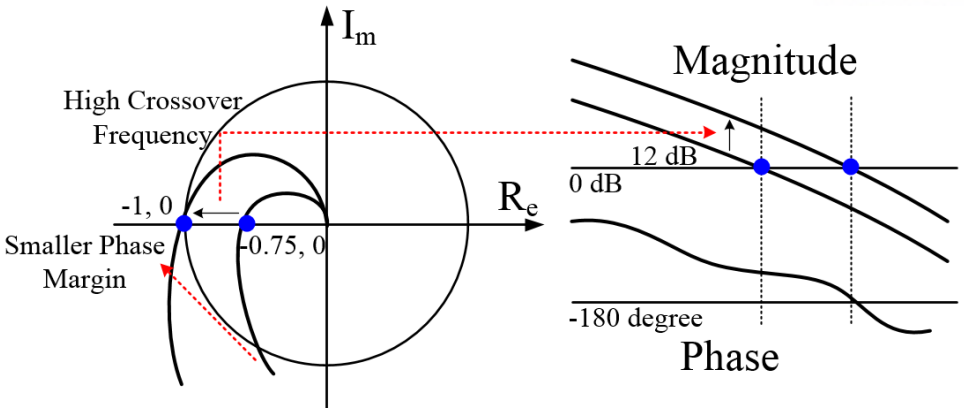


Fig. 12. Destabilizing effect of high crossover frequency in a 500 kHz LLC resonant converter

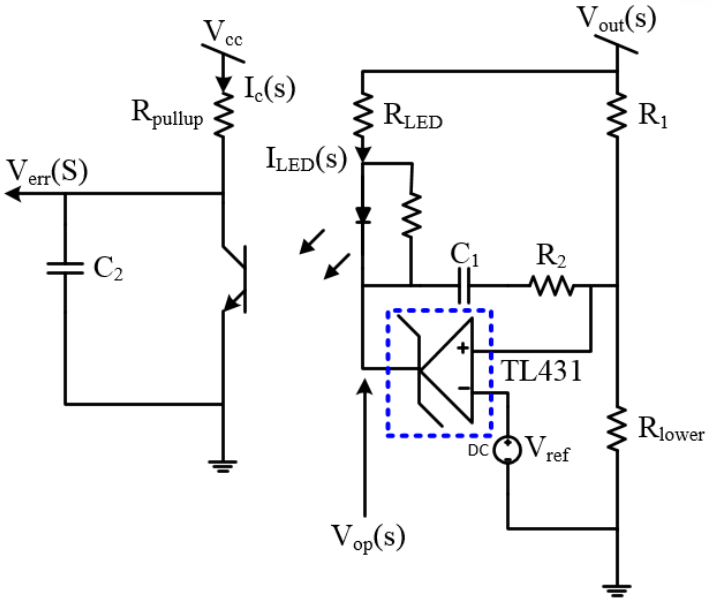
3.2 Design of the Feedback Compensator

The small output capacitance and small ESR induce a high crossover frequency and drastic decrease of the phase margin. To obtain enough phase margin for stability, the feedback loop design is crucial for the closed-loop gain. The compensator is configured with two poles and one zero, which is widely used in power converters. Fig. 13 shows a circuit diagram of the two-pole one-zero feedback compensator and its Bode plot. The transfer function of the error amplifier in Fig. 12 can be represented as follows:

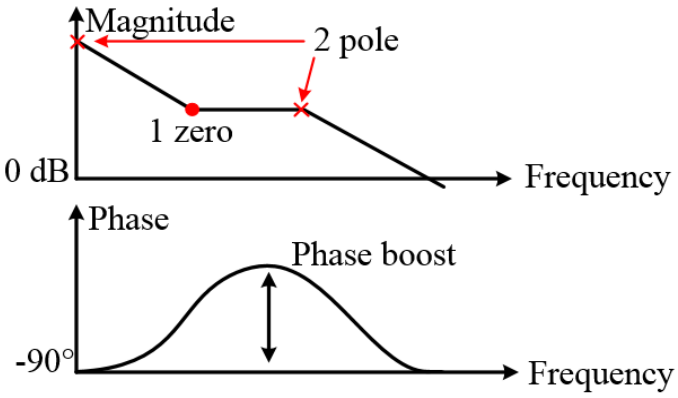
$$V_{err}(s) = \frac{R_{pullup}}{R_{LED}} \times CTR \times \frac{1 + s(R_1 + R_2)C_1}{sR_1C_1(1 + sR_{pullup}C_2)} \tag{12}$$

where CTR is the current transfer ratio and $V_{err}(s)$ is the output voltage of the feedback loop.

To design a proper feedback loop, the K-factor approach method [24] is used to obtain the desired crossover frequency and phase margin using the theoretical open-loop transfer function. In the conventional design method, a phase boost should be placed slightly beyond the resonant frequency of the output filter to obtain high dynamics by the high crossover frequency. In addition, the maximum phase drop in the loop gain is located at the resonant frequency. However, in the case of high switching frequency operation, the small capacitance already sets the high frequency location of first two-poles (6.3 kHz). It induces high crossover frequency that makes fast transient response, drastic phase drop, and high switching noise. From these reasons, designed crossover frequency and phase boost (5 kHz) should be placed slightly below the double pole of the resonant frequency of the output filter (6.3 kHz) to obtain enough phase margin, gradual phase variation, and small nonlinearity near the crossover frequency. Therefore, with the magnitude compensation using the feedback loop, the crossover frequency of the closed-loop gain can be placed slightly below the resonance frequency of the output filter, which is much lower than the crossover frequency of the open-loop gain.



(a)



(b)

Fig. 13 Circuit diagram and bode plot of a two-pole one-zero feedback compensator: (a) circuit diagram of a two-pole one-zero feedback compensator, (b) bode plot of a two-pole one zero feedback compensator

The crossover frequency of the closed loop (5 kHz) should be selected to achieve enough phase margin through the feedback compensator, which is configured with two poles and one zero. To achieve the lower crossover frequency that is not affected by the nonlinearity effect, the magnitude of the closed loop should be smaller than the magnitude of the open-loop gain. However, the magnitude reduction is limited by the values of R_{LED} and R_{pullup} of the compensator, as shown in Fig. 13. The high resistance of R_{LED} to reduce the magnitude of the open-loop gain prevents current flow to the optocoupler, which requires 0.15 mA as a minimum current. R_{pullup} is a fixed small value to control the range of the switching frequency. Therefore, 5 kHz is selected as the lowest crossover frequency, which is slightly below the resonant frequency of the output filter. When the desired phase margin is specified as 60° to achieve the

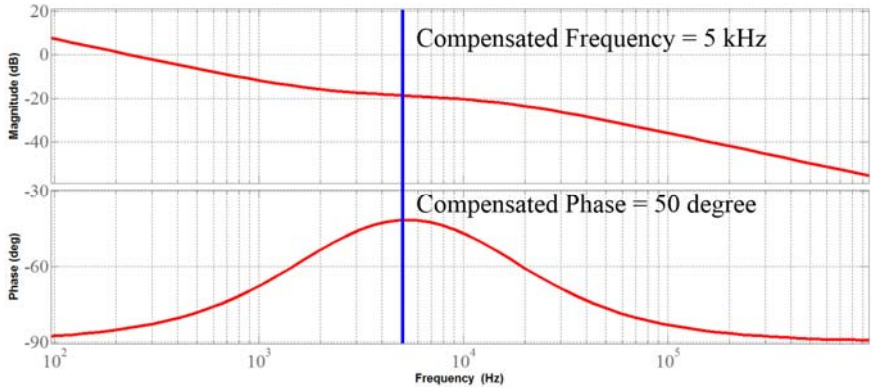
fast settling response without oscillation, the phase boost is calculated as follows:

$$\phi_{boost} = -90 + \phi_{pm} - \angle G_{ps}(s)_{fc} \tag{13}$$

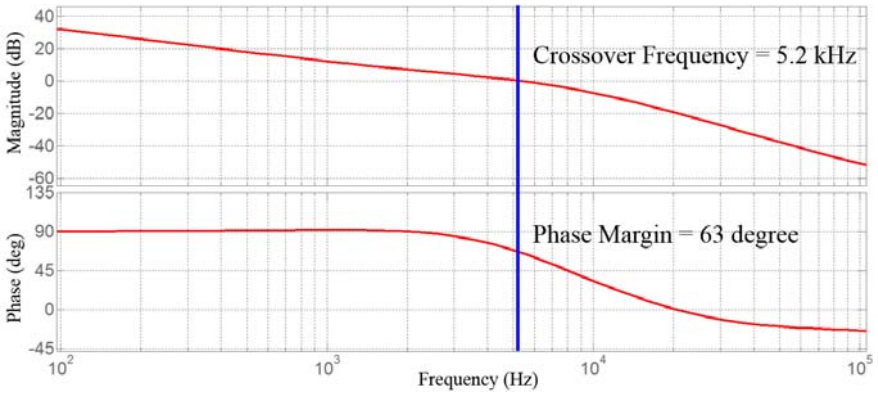
where ϕ_{boost} is the desired phase boost, ϕ_{pm} is the desired phase margin, and $\angle G_{ps}(s)_{fc}$ is the phase of the crossover frequency at the open-loop condition. Using ϕ_{boost}, the coefficient of the K-factor approach, K_{boost}, can be determined to specify the location of the pole and zero of the feedback compensator. The pole and zero are placed at f_z and f_p, which can be calculated as follows:

$$K_{boost} = \sqrt{\frac{f_p}{f_z}} = \tan\left(45^\circ + \frac{\phi_{boost}}{2}\right), \quad f_z = \frac{f_c}{K_{boost}}, \quad f_p = K_{boost} f_c \tag{14}$$

The designed feedback compensator, theoretical closed-loop gain, and experimental closed-loop gain are shown in Fig. 14. The 500 kHz high frequency LLC resonant converter has sufficient phase margin and lower crossover frequency than the open-loop gain. The theoretically designed closed-loop gain has a 5 kHz crossover frequency with 63° of phase margin. The experimental closed-loop gain has 5.2 kHz crossover frequency with 66° of phase margin. The theoretical models and the experimental measurements are well matched to each other. Comparing with the 100 kHz switching frequency case, the closed-loop gain of the 500 kHz high frequency LLC resonant converter has much higher crossover frequency to achieve high power density.



(a)



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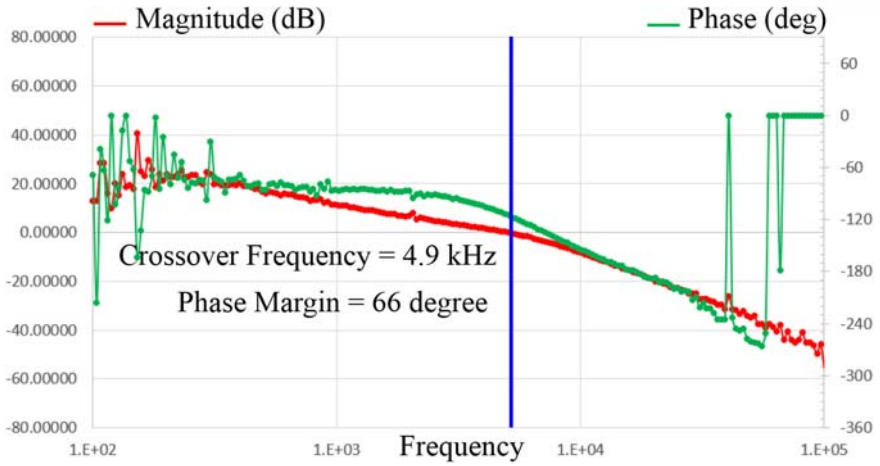
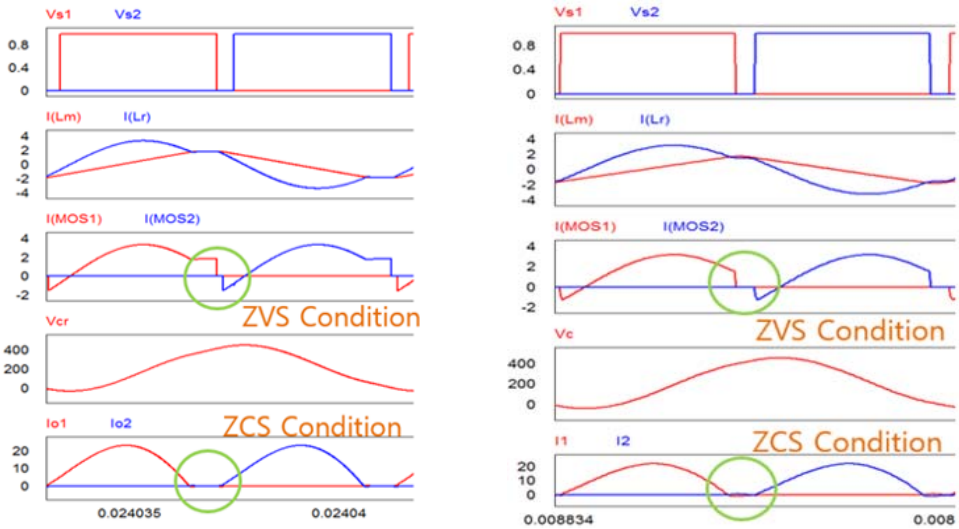


(c)

Fig. 14. Theoretical and experimental Bode plots of 500 kHz small-signal response: (a) Theoretical Bode plot of open-loop gain, (b) Theoretical Bode plot of closed-loop gain, (c) Experimental Bode plot of closed-loop gain

3.3 Simulation and Experimental Results with 500 kHz LLC Resonant Converter

The simulation results of the LLC resonant converter show ZVS operation of power MOSFETs and ZCS operation of secondary diodes, which can reduce switching losses, as shown in Fig. 15. The ideal condition of the simulation does not consider the effects of parasitic components. The specific parameters of the simulation and the experimental measurements are shown in Table II. Compared with 100 kHz switching frequency operation, the size of the passive components drastically reduces at 500 kHz operation.

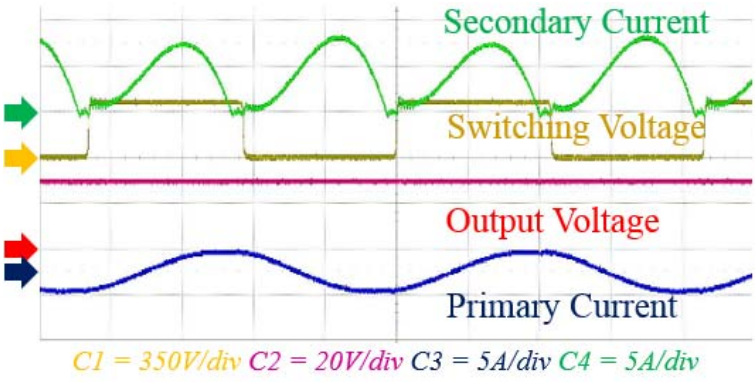


(a) (b)

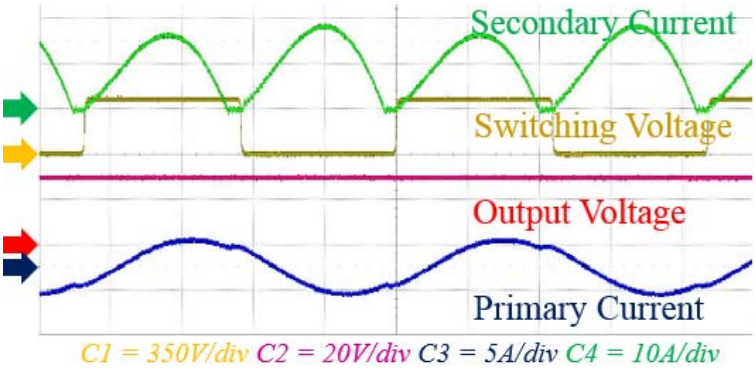
Fig. 15. Simulation waveforms under 100 kHz and 500 kHz switching frequency operation: (a) Operational waveform of 100 kHz switching frequency, (b) Operational waveform of 500 kHz

switching frequency

Fig. 16 and 17 show the experimental waveforms at 100 kHz and 500 kHz switching frequency, which shows the operations of the power MOSFETs under the ZVS condition and the secondary diodes under the ZCS condition. Compared with operational waveforms at 100 kHz, the operation at 500 kHz has high frequency ringing in the current waveform caused by the influence of parasitic capacitance and stray inductance.

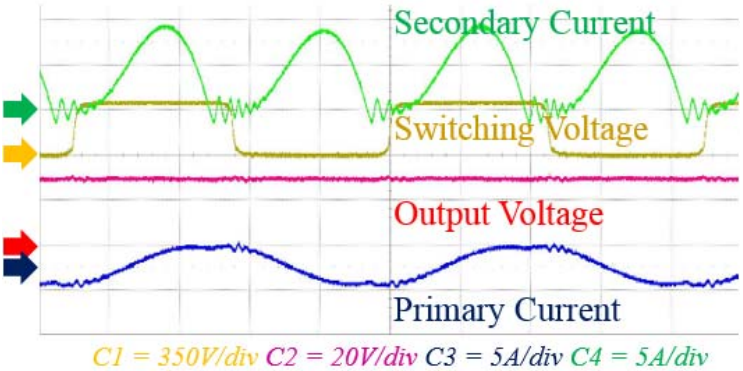


(a)

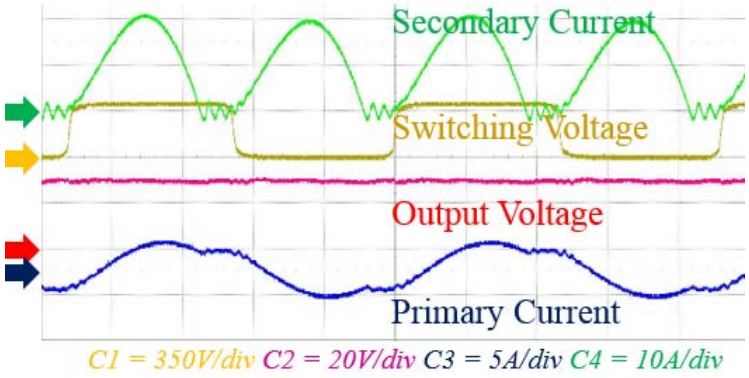


(b)

Fig. 16. Experimental waveforms of 100 kHz LLC resonant converter: (a) 4 A light load case, (b) 10 A full load case



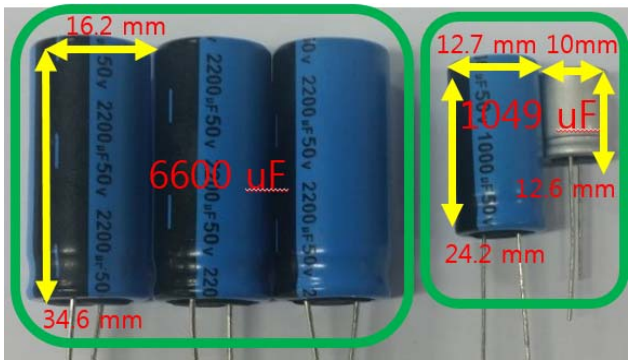
(a)



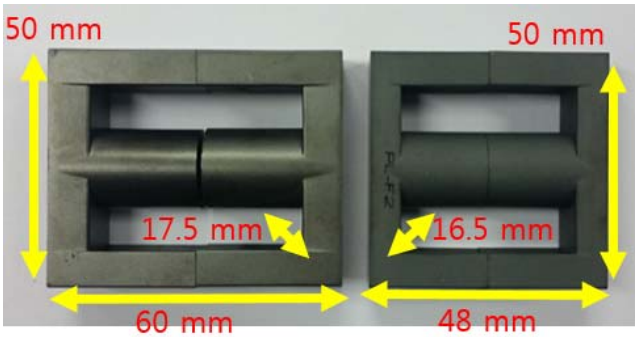
(b)

Fig. 17. Experimental waveforms of 500 kHz LLC resonant converter: (a) 4A light load case, (b) 10 A full load case

The size reduction of passive components can be achieved at high switching frequency as derived in (4). Fig. 18 shows the size reduction of the passive components. The volume of the output capacitor and the transformer reduces around 5.2 and 1.3 times, respectively.



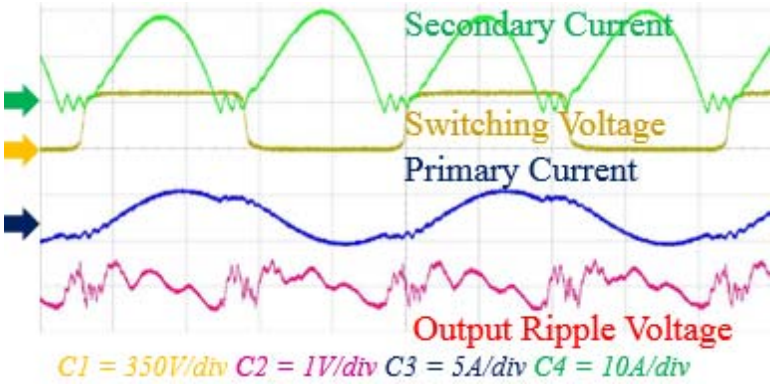
(a)



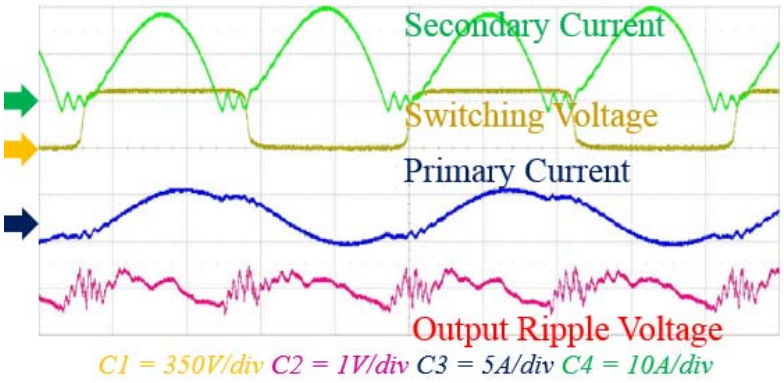
(b)

Fig. 18. Size reduction of passive components under high switching frequency operation: (a) Comparison of output capacitor sizes, (b) Comparison of transformer sizes

Moreover, the high frequency LLC resonant converter that adopts smaller output capacitance and smaller ESR has an advantage of smaller output voltage ripple as derived in (5) and Fig. 2. Fig. 19 shows the output voltage ripple with respect to the output capacitance and ESR conditions. Smaller capacitance and ESR case has smaller output voltage ripple (1049 μF, 5.6 mΩ, 1.01 V_{pp}) than the case of higher capacitance and ESR (6600 μF, 9 mΩ, 1.21 V_{pp}).



(a)



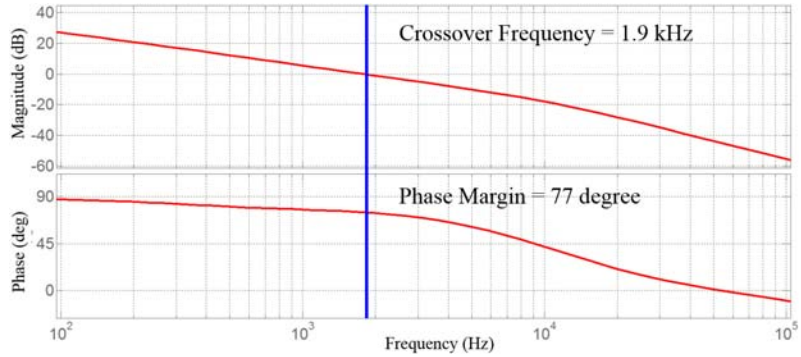
(b)

Fig. 19. Comparison of output voltage ripple according to output capacitor cases: (a) High capacitance and ESR case, (b) Small capacitance and ESR case

To verify the variation of the relative stability according to the output capacitor, the high output capacitance case (6600 μF, 9 mΩ), as shown in Fig. 20, shows higher phase margin and lower crossover frequency compared to the small output capacitance case. The higher phase margin can induce a smaller output impedance, which makes smaller output voltage variation under step load changes.

Fig. 21 shows the step load response of the output voltage at 500 kHz switching frequency from no load to full load. In Fig. 21, the higher output capacitance supresses output voltage spikes. As a result, the higher output capacitance makes the smaller output voltage variation according to load changes.

Compared with the 100 kHz converter, the power conversion efficiency of the 500 kHz converter decreases 2% at the rated load, as shown in Fig. 22. This efficiency drop comes from higher switching losses and higher hysteresis losses in spite of the soft switching techniques.



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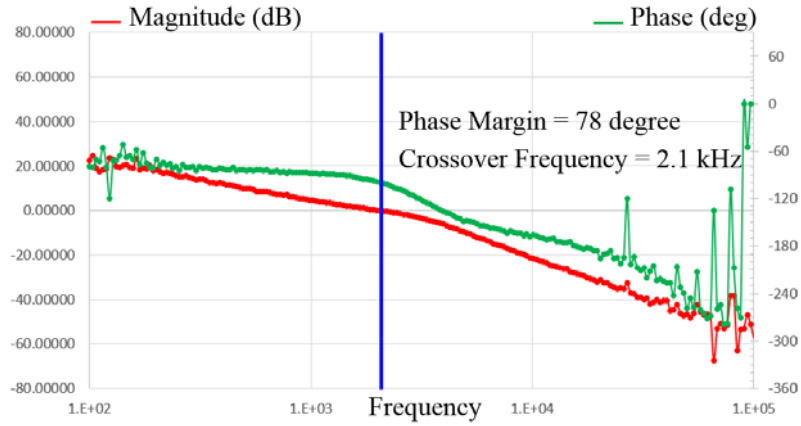
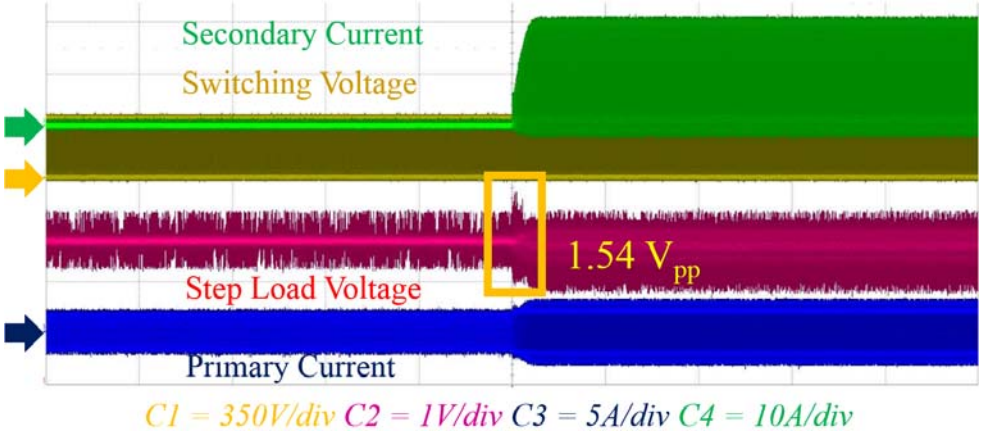
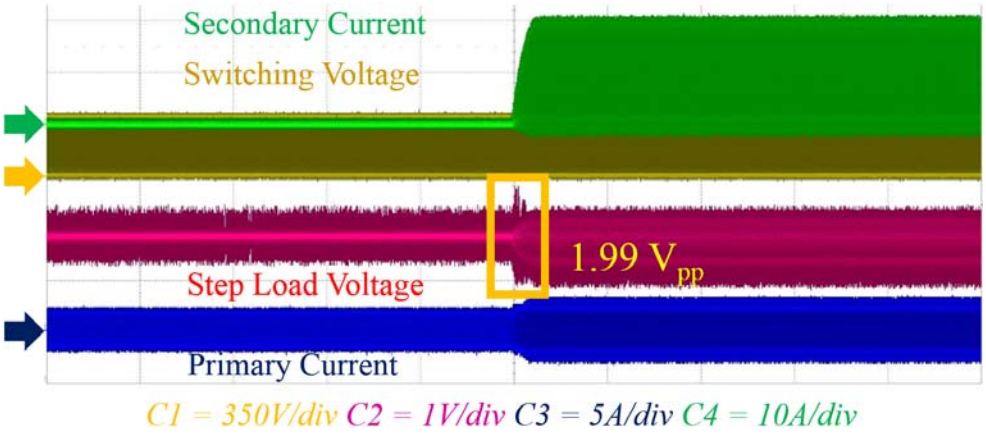


(b)

Fig. 20. Theoretical and experimental Bode plot of 500 kHz small-signal response using high capacitance: (a) Theoretical Bode plot of the closed-loop gain, (b) Experimental Bode plot of the closed-loop gain



(a)



(b)

Fig. 21. Step load response according to output capacitance: (a) Step load waveforms using small output capacitance, (b) Step load waveforms using high output capacitance

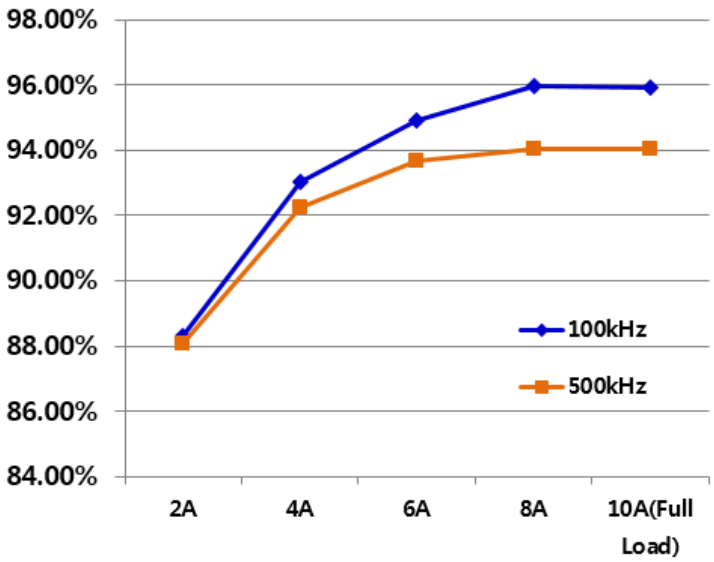
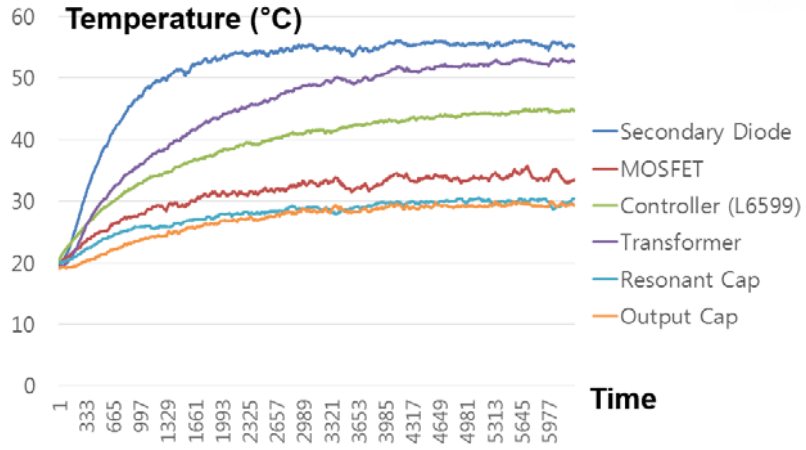
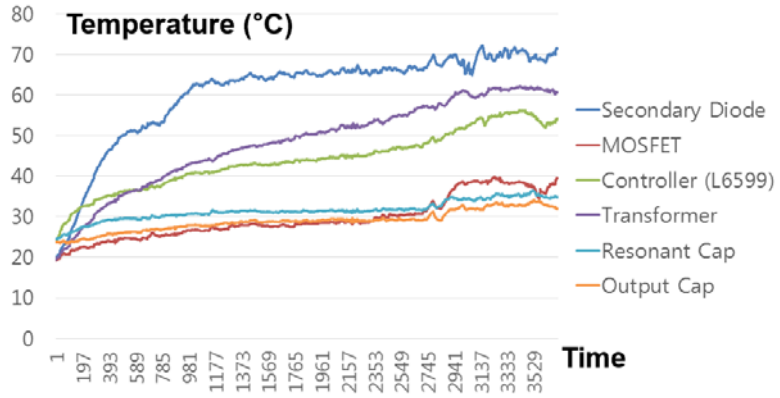


Fig. 22. Power conversion efficiency of 100 kHz and 500 kHz LLC resonant converter

The temperature is measured using ZR-RX25 (OMRON) with an ambient temperature of 20.6 ℃. Heat sinks (25mm×16.5mm×16mm) are attached to all the switching components which have temperature variations as increasing the switching frequency. Table III shows the temperature variations with respect to the switching frequency. Comparing with the 100 kHz operation, the switching components and the transformer have higher operating temperature. Other passive components also have the temperature increment, however, the difference is smaller than the case of the active and magnetic components.



(a)



(b)

Fig. 23. Temperature variations of converters' components according to operating time: (a) 100 kHz case, (b) 500 kHz case.

TABLE III

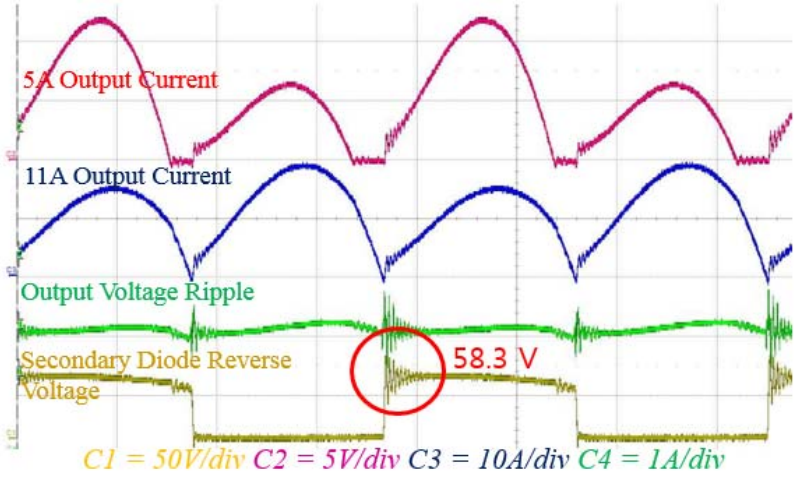
COMPARISON OF COMPONENTS TEMPERATURE WITH RESPECT TO THE SWITCHING FREQUENCY

Specification	100 kHz	500 kHz
Diode	57℃	71℃
MOSFET	35℃	41℃
L6599 (gate driver)	45℃	56℃
Transformer	51℃	63℃
Resonant capacitor	33℃	38℃
Output capacitor	31℃	34℃

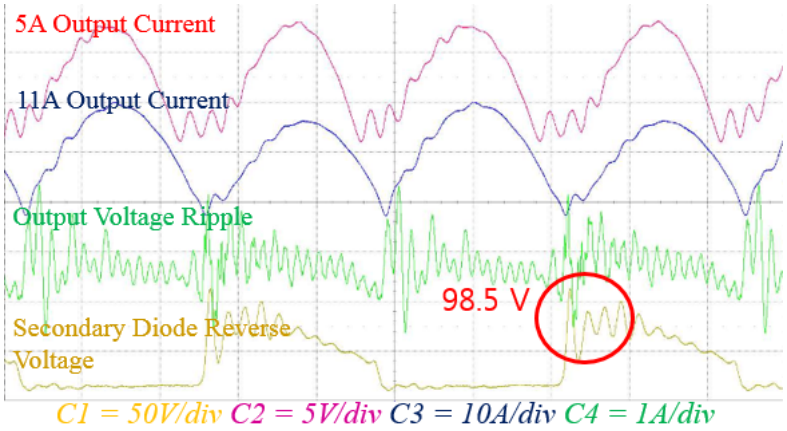
IV. Peripheral Circuit Design and Control Strategy for High Switching Frequency Operation

4.1 Side effect of high speed switching

The high frequency operation induces the high frequency ringing caused by parasitic components in the converter. The parasitic inductance of the PCB is one of the dominant factors as increase of the switching frequency. Fig. 24 shows that experimental results of the reverse voltage in the secondary diode rectifiers. Ideally, the secondary diode reverse voltage should be $2V_o$. Fig. 24 (a) shows the experimental waveforms of the 100 kHz LLC resonant converter. Here, the secondary side reverse voltage is 1.5 times higher than ideal condition which should be considered to select the secondary diode. Fig. 24 (b) shows the experimental waveforms of the 1 MHz LLC resonant converter. The reverse voltage of the secondary diode is 2.5 times higher than the case of the ideal condition.



(a)



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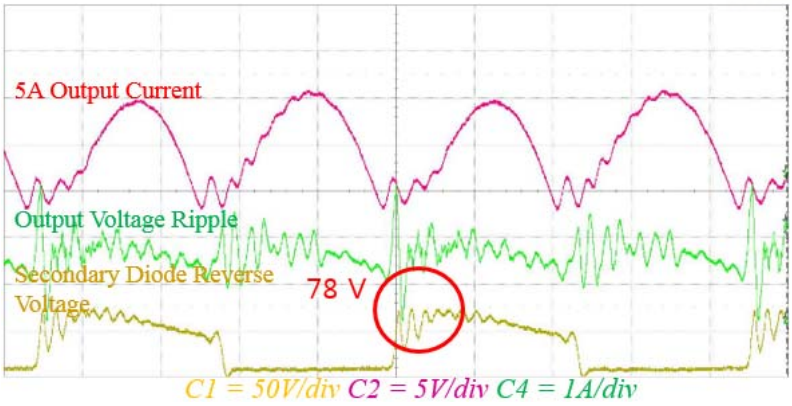

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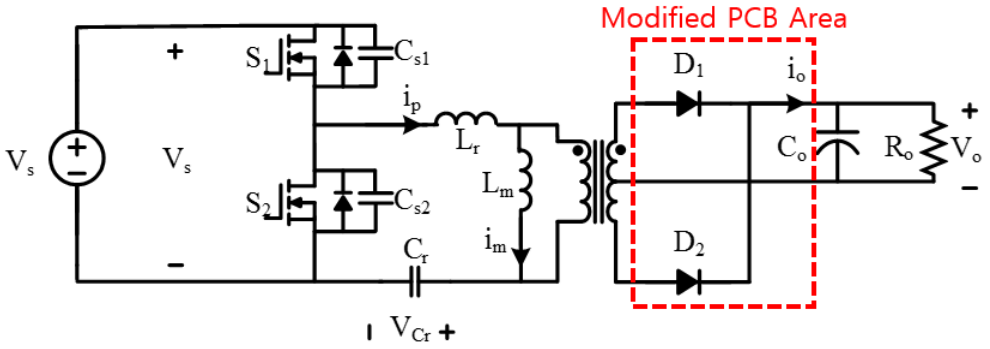
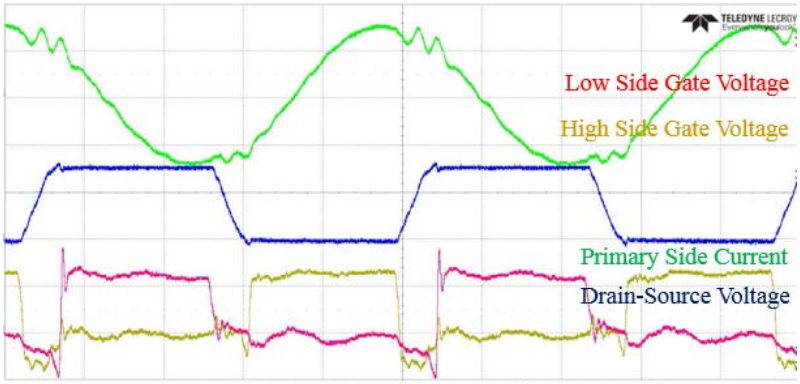


(d)

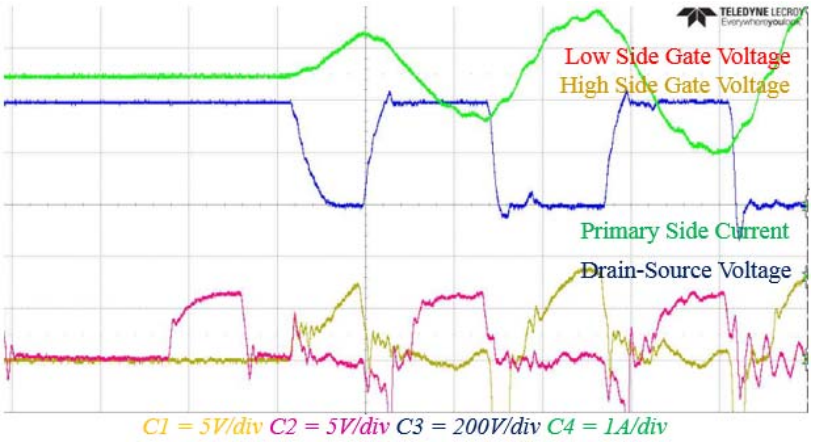
Fig. 24. Experimental results of reverse voltage waveforms in secondary rectifying diode: (a) 100 kHz case, (b) 1 MHz case (10 nH case), (c) 1 MHz case with short PCB path (6 nH case), and (d) Modified area of PCB pattern

Therefore, the secondary diode should have high reverse voltage characteristics at the high frequency operation. However, a schottky diode which has higher reverse voltage shows higher forward voltage drop, higher parasitic capacitance, and higher reverse recovery loss. Basically, the stray inductance in the PCB should be reduced. Fig. 24 (c) shows the secondary diode reverse voltage using short PCB path. The reverse voltage is 2 times higher than the ideal case. From Fig. 24 (c), the stray inductance of the secondary side makes high reverse voltage spikes on the secondary rectifying diode, which can be reduced by the short PCB path. Fig. 24 (d) shows the modified PCB area to reduce the secondary side stray inductance.

In addition, the parasitic inductance in the gate driver makes undesired spike and ringing which can induce shoot-through or malfunction of the switching operation of E-HEMTs. Even though the permitted gate voltage level is 10V for the GaN E-HEMT, the spike and off state ringing in the gate voltage can be induced by the parasitic inductance (1 nH) as shown in Fig. 25. To reduce the stray inductance, the path between the gate driver and the gate of the E-HEMT should be as short and wide as possible.



(a)



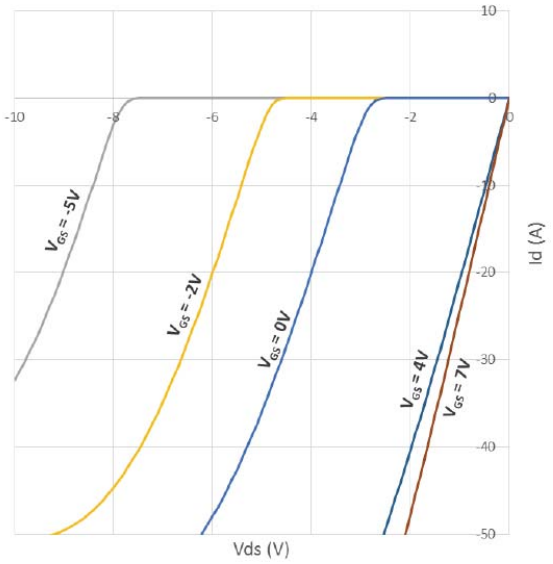
(b)

Fig. 25. Gate signal waveforms with high spike voltage and ringing: (a) High spike gate voltage waveforms, (b) Turn-off state gate voltage waveforms

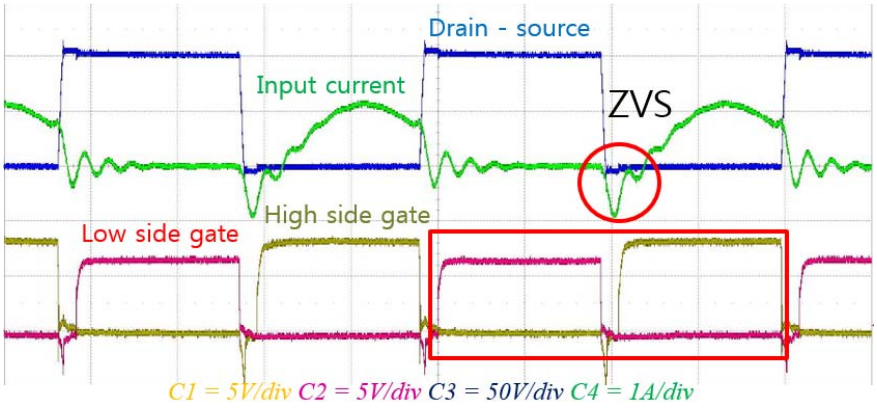
4.2 High speed switching characteristics of GaN E-HEMT

The GaN E-HEMT has proper characteristics for the high switching frequency operation such as smaller gate and output capacitance, and smaller on resistance, which can reduce switching losses [28]. However, a reverse conduction voltage of the GaN E-HEMT which is approximately 2.5V as shown in Fig. 26 (a) can be a challenge of designing a bootstrap gate driver for a high side power switch.

Comparing with the GaN E-HEMT which has zero reverse recovery theoretically, the Silicon-based MOSFET has reverse recovery losses. However, its reverse conduction voltage is limited to the forward voltage drop of an anti-parallel diode. In the case of the GaN E-HEMT, the high reverse conduction voltage should be compensated in the bootstrap driver for the stable operation of the high-side switch as shown in Fig. 26 (b). Fig. 27 shows the comparison of high-side gate voltage levels using different bootstrap diodes. Using a bootstrap diode which has high forward voltage drop around the reverse conduction voltage of the GaN E-HEMT can compensate the unbalance of the high side gate voltage.

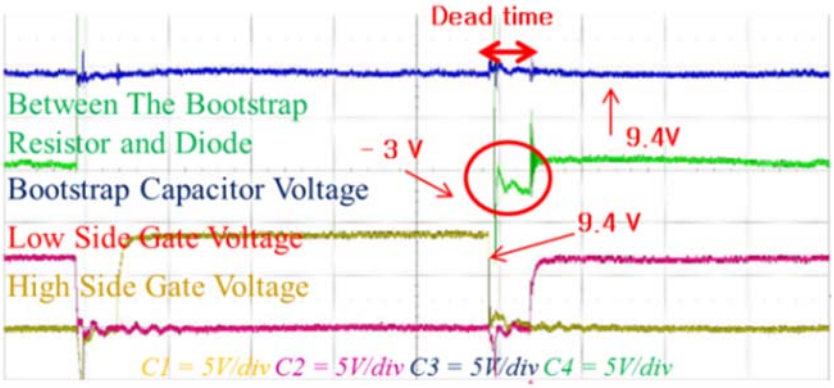


(a)

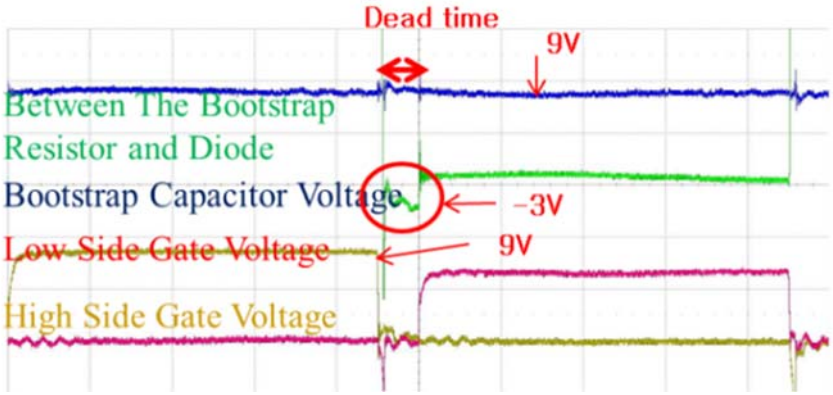


(b)

Fig. 26 Characteristics of GaN E-HEMT: (a) High reverse conduction voltage of GaN E-HEMT, (b) Unbalanced gate voltage waveform



(a)



(b)

Fig. 27. Comparison of high side gate voltage level using different bootstrap diodes: (a) Low forward voltage drop of bootstrap diode, (b) High forward voltage drop of bootstrap diode

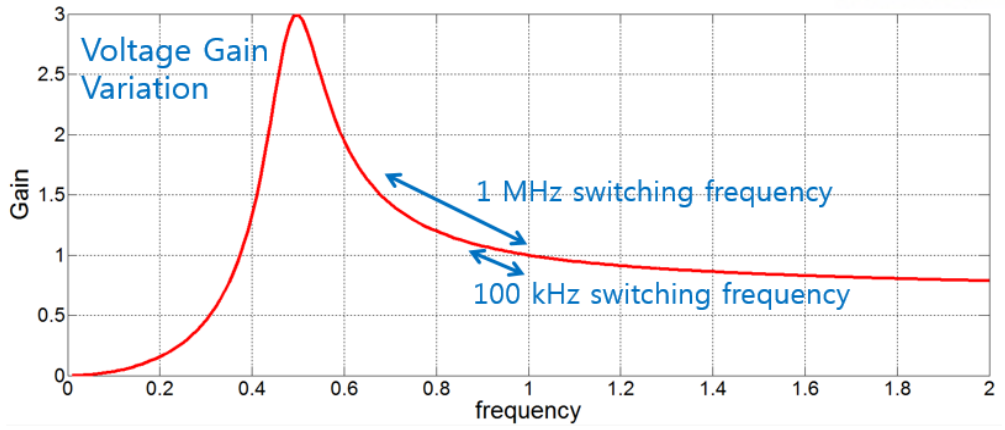
4.3 Soft start algorithm for high switching frequency

The PWM controller is implemented with a DSP (TI TMS28335) to provide the switching signal around 1 MHz switching frequency. However, it cannot provide sufficient control bandwidth for the pulse frequency modulation (PFM) control method of the LLC resonant converter at 1 MHz. Moreover, the converter requires much higher switching frequency for soft start duration to suppress inrush current at the beginning of the cold start. As a conventional soft start algorithm of the LLC resonant converter, the switching frequency is reduced from two times higher switching frequency than the nominal operating frequency and it decreases till the nominal frequency for steady state operation. However, this conventional method has two demerits: it is not effective to the first inrush current and it starts from very high switching frequency.

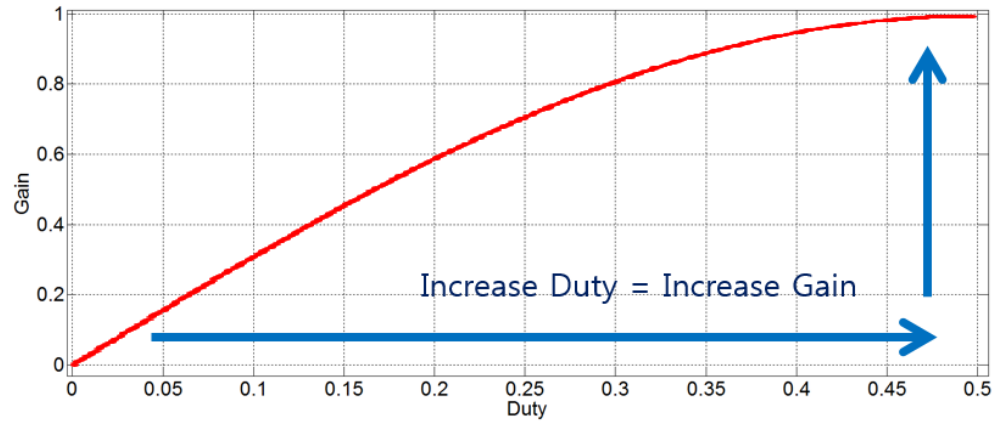
The proposed method uses both pulse width modulation (PWM) and PFM. First, the duty ratio increases from 0% to 80% at the fixed switching frequency which is 1.4 times higher than the nominal frequency. Then, this soft start frequency decreases to the nominal frequency with 80% duty ratio. Using the proposed soft start algorithm, the inrush current can be suppressed with lower voltage gain and lower soft start frequency. Equation (7) shows voltage gain variations according to the duty cycle. Fig. 28 shows voltage gain variations according to the switching frequency and the duty cycle.

$$\left.\frac{V_o}{V_{in}}\right|_{1st-SS} = \left\| H_r(f_{n,\max}) \right\| \sin \pi(\frac{T_d}{T_s}) \tag{15}$$

where $H_r(f_{n,max})$ is input-output voltage gain at maximum switching frequency, T_d is duty cycle, and T_s is switching period.

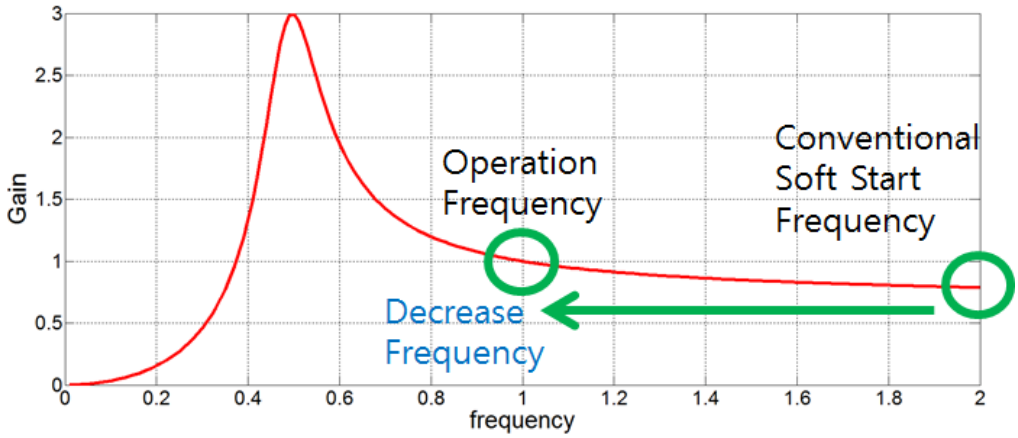


(a)

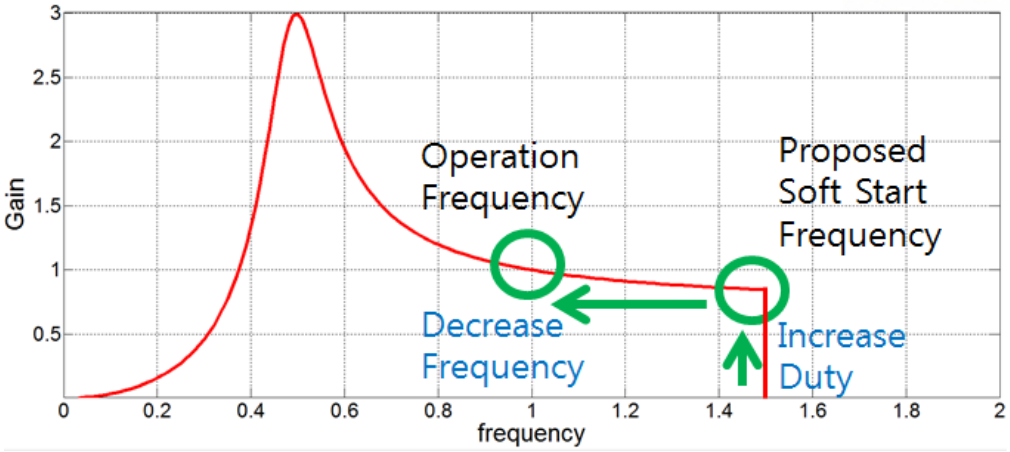


(b)

Fig. 28. Voltage gain variations according to switching frequency and duty cycle: (a) Conventional voltage gain curve of LLC resonant converter, (b) Voltage gain curve of LLC resonant converter according to duty cycle



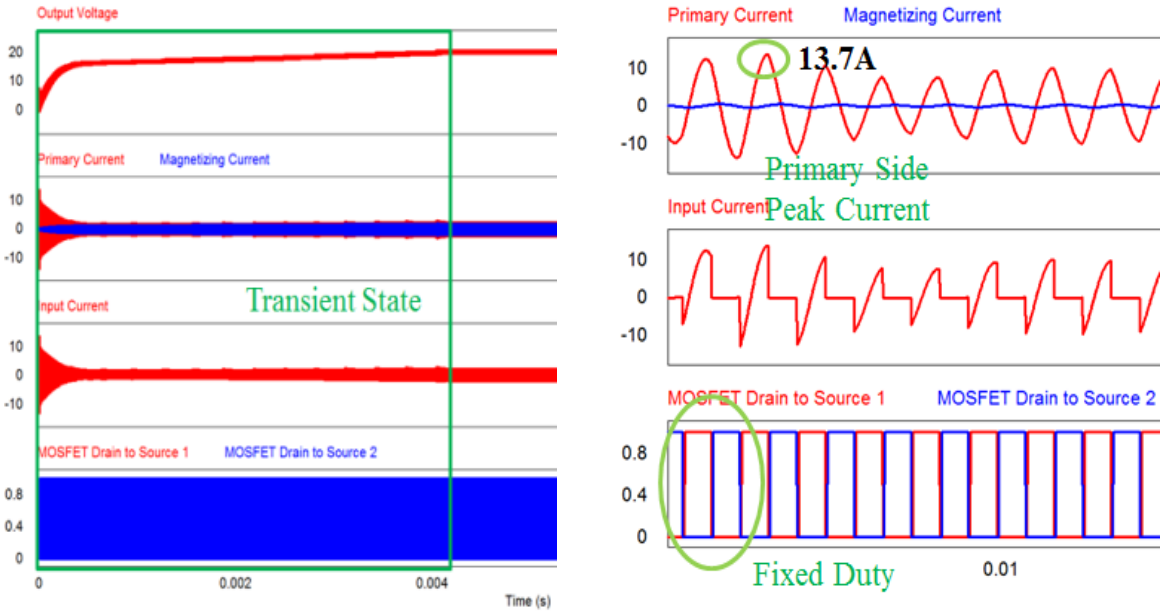
(a)



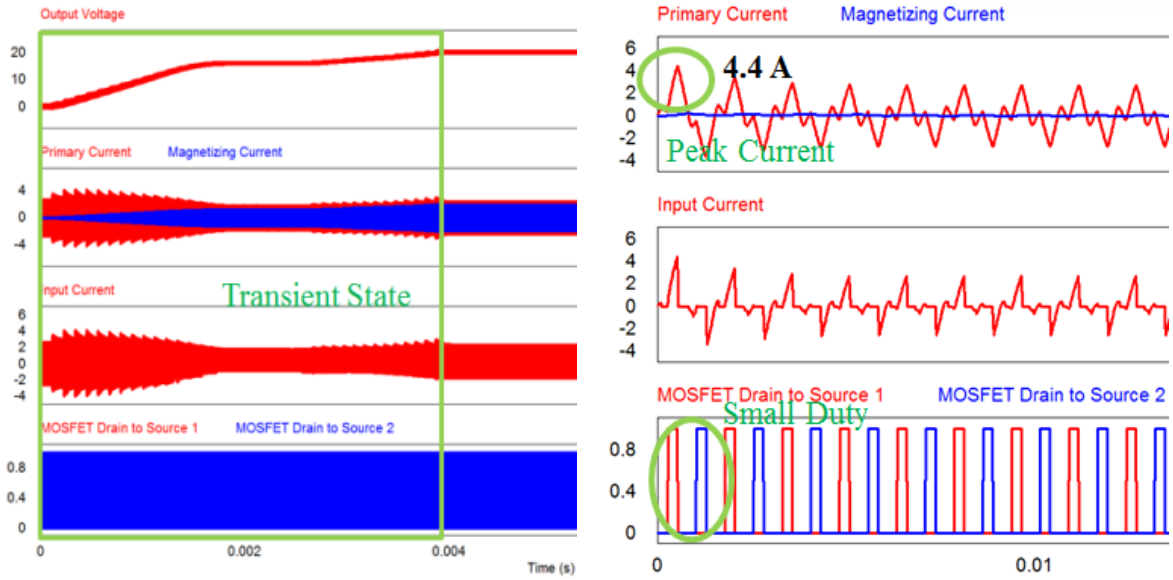
(b)

Fig. 29. Voltage gain curves of conventional and proposed soft start algorithms: (a) Conventional soft start algorithm, (b) Proposed soft start algorithm using proposed hybrid control

Using the voltage gain variation as shown in (7) and Fig. 28, Fig. 29 (b) can be obtained as the operating waveform of the proposed soft start algorithm. Comparing with Fig. 29 (a), it shows much smaller voltage gain at the cold start. Fig. 30 and Fig. 31 show simulation and experimental results of the proposed soft start algorithm. Comparing with the conventional algorithm, the peak inrush current in the transient state is reduced from 13.7 A to 4.4 A, which is more than three times higher reduction of the inrush current.



(a)



(b)

Fig. 30. Simulation waveforms of conventional and proposed soft start algorithms: (a) Conventional soft start waveforms, (b) Proposed soft start waveforms

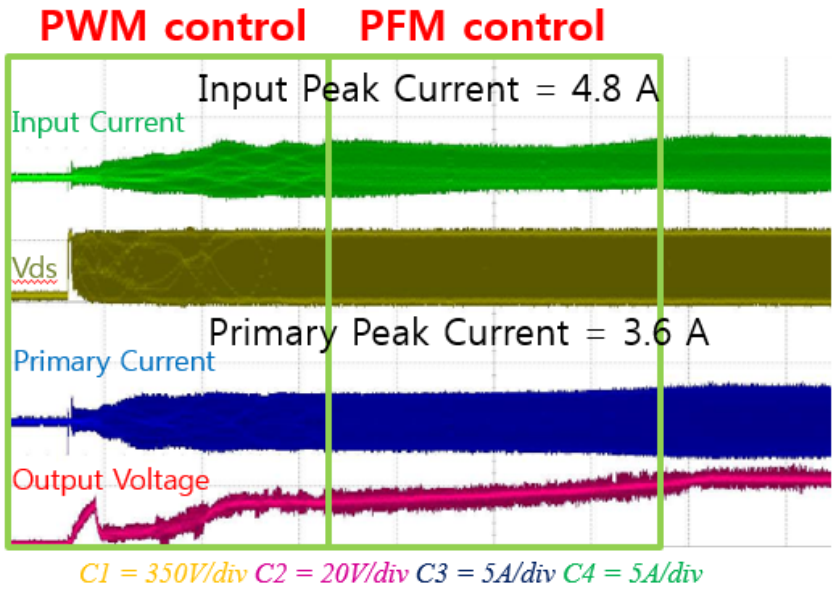
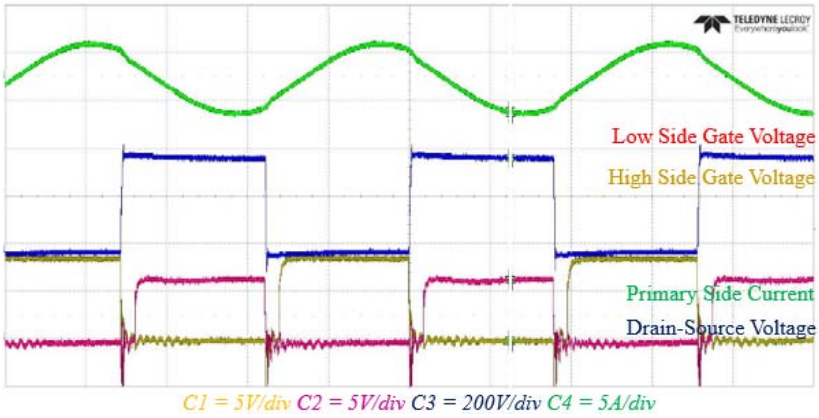


Fig. 31. Experimental waveforms of proposed soft start algorithm

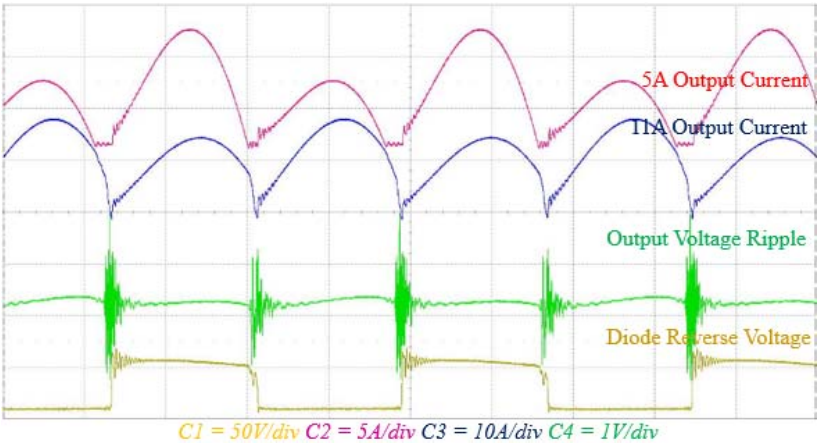
4.4 Simulation and Experimental Results with 1 MHz LLC Resonant Converter

The simulation results of the LLC resonant converter show the ZVS operation of E-HEMTs and the ZCS operation of secondary diodes, which can reduce switching losses. The simulation does not consider the effects of parasitic components. The specific parameters of the simulation and the

experimental measurements are shown in Table II.

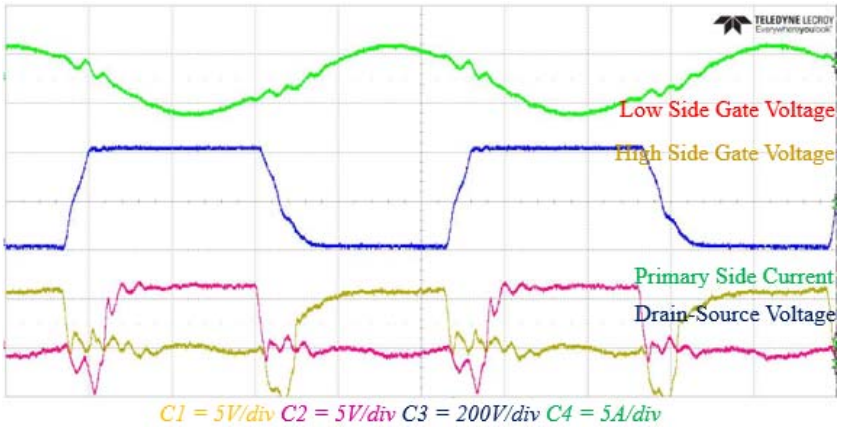


(a)

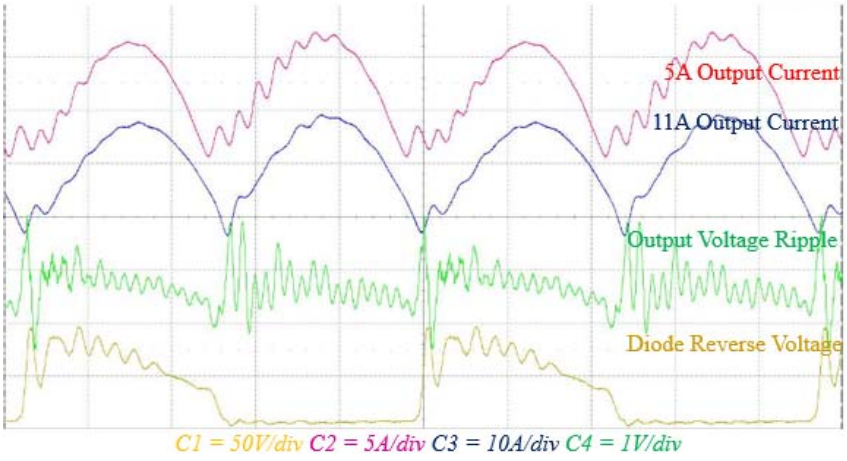


(b)

Fig. 32. Steady state operational waveform at 100 kHz switching frequency: (a) Experimental waveforms in the primary side, (b) Experimental waveforms in the secondary side



(a)



(b)

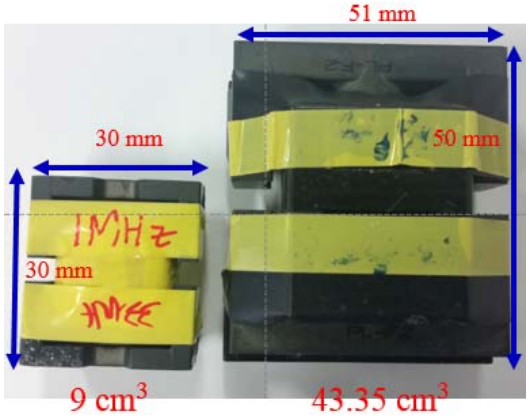
Fig. 33. Steady state operational waveform at 1 MHz switching frequency: (a) Experimental waveforms in the primary side, (b) Experimental waveforms in the secondary side

Compared with the 100 kHz switching frequency operation, the capacitance and inductance of the passive components drastically reduces at the 1 MHz operation. Fig. 32 and 33 show the experimental waveforms at 100 kHz and 1 MHz switching frequency. The operations of the E-HEMTs under the ZVS condition and the secondary diodes under the ZCS condition are verified using the proposed design. Compared with the operational waveforms at 100 kHz, the 1 MHz converter has high frequency ringing in the current waveform caused by the parasitic capacitance and the stray inductance on the PCB.

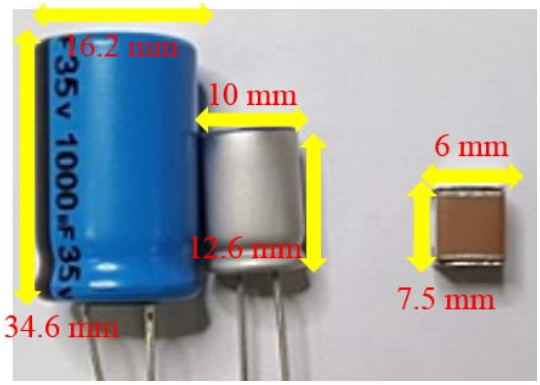
TABLE IV

SPECIFICATION OF EXPERIMENTAL CONDITIONS OF 1 MHZ LLC RESONANT CONVERTER

Specification	100 kHz frequency	1 MHz frequency
Input Voltage	400 V	400V
Output Load	20V/12A	20V/12A
Magnetizing Inductance	280 µH	43 µH
Leakage Inductance	90 µH	11 µH
Resonant Capacitance	18 nF	2 nF
Output Capacitance	2200 µF 9 mΩ	120 µF 2.1 mΩ
Line Parasitic Resistance	1 Ω	1 Ω
Resonant Frequency	125 kHz	1.07 MHz



(a)



(b)

Fig. 34. Comparison of passive components size of 1 MHz switching frequency: (a) Size reduction of transformer, (b) Size reduction of output capacitor

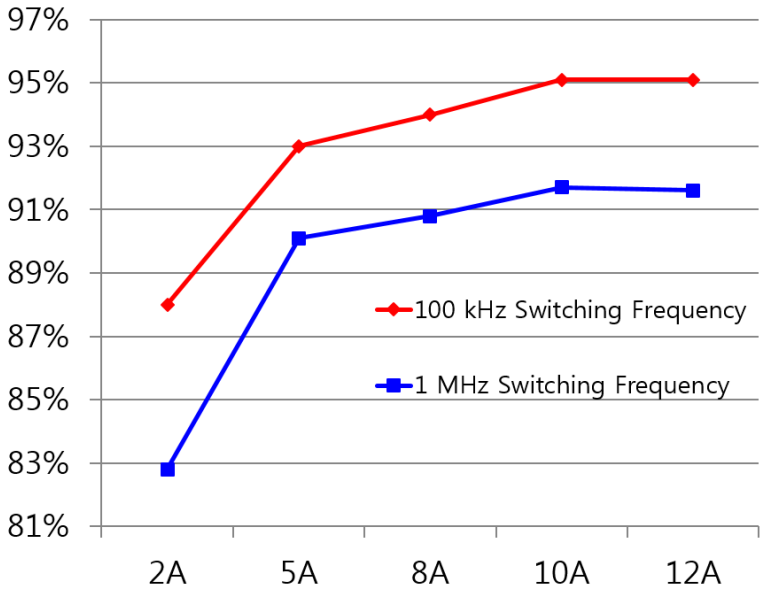


Fig. 35. Power conversion efficiency of 1 MHz switching frequency

Fig. 34 (a) shows the size comparison of the transformer and the output capacitor with respect to the

switching frequency. The size of the transformer is around 5.1 times smaller than the 100 kHz case, and the capacitance is reduced from 2200uF to 141uF with decreasing the volume of the capacitor around 7.75 times smaller than the 100 kHz case. Fig. 35 shows power conversion efficiency curves according to load variation comparing with three different cases. From Fig. 35, the efficiency of the 1 MHz converter is lower than the efficiency of the 100 kHz converter because of higher switching losses. For the 1 MHz operation, two transformers are designed with almost same magnetizing and leakage inductance to compare power losses in the transformer. Since the small-sized transformer which has smaller cross-sectional area limited by smaller window area has higher conduction losses in its windings, the efficiency is poor, however, the power density can be improved. Moreover, the 1 MHz switching frequency induces higher magnetizing current than 100 kHz switching frequency case to achieve ZVS condition.

V. Summary

In this paper, the design considerations such as power stage design, feedback loop analysis, and peripheral circuit design are introduced for high switching frequency LLC resonant converter. As results, the 1 MHz LLC resonant converter has 7 times higher power density with proper stability compared with 100 kHz LLC resonant converter.

5.1 Design Considerations for High Power Density

In this chapter, the proper power stage design methodology is introduced for the high switching frequency LLC resonant converter to improve the power density. First, the design of proper magnetizing inductance is proposed to obtain the ZVS condition in the high frequency operation for high power conversion efficiency. Second, the proper output capacitor design is proposed to improve the power density and small output voltage ripple at high switching frequency. Third, the smaller transformer size is proposed to improve the power density with output saturation.

5.2 Feedback Loop Design

In this chapter, the analysis of small signal model and design of proper feedback loop are introduced to obtain the stability and dynamics using 500 kHz and 100 kHz switching frequency operations. The improvement of power density induces smaller passive component values which makes high crossover frequency and small phase margin. It makes unstable power converter operations which can be solved with proper feedback loop design. The unstable operation caused by the small-sized output capacitor is verified with the small-signal model. To overcome the stability problem, the open-loop gain is investigated to obtain the variation of the crossover frequency and the phase margin according to the output capacitor. As a result, the feedback compensator for the high frequency operation is designed to obtain sufficient phase margin with proper crossover frequency.

5.3 Peripheral Circuit Design and Control Strategy for High Switching Frequency

In this chapter, the characteristics of the GaN E-HEMT are discussed by comparing it with the Silicon-based MOSFET. The proper gate driver design is introduced to implement the PWM signals with stable operational range. As the switching frequency increases, the side effect of the parasitic capacitance and stray inductance of the PCB, and the limitation of the DSP control bandwidth are fully considered to obtain stable operation and high power conversion efficiency of the converter.

VI. Future Plan

6.1 Improvement of Power Density

The high switching frequency converter can be optimized to achieve smaller power loss and high power density. In aspect of power stage, the parasitic components make side effects which induces undesired operating waveforms. The differences between conventional switching frequency and high switching frequency should be reflected to the power stage design. The proper passive and active components are selected to minimize the power loss. In addition, the proper magnetics design is required to improve the power density and small power dissipations from the transformer. The high switching frequency converter can be integrated within the smaller PCB size, since the well-designed power converter has smaller power losses which make small heat dissipation.

6.2 Feedback Loop Design with High Performance FPGA

In aspect of the controller of the power converter, the general-purposed digital micro-controller provides a low switching frequency resolution which has limited control performance for the pulse frequency modulation (PFM) in several mega-hertz switching operation and poor dynamics. However, the high performance FPGA makes high switching frequency resolution and fast computation speed compared with general purposed DSP. The LLC resonant converter can achieve well-regulated output voltage and fast dynamics with high performance FPGA.

6.3 Small Signal Modeling for Other Applications

In this paper, the small signal model is analyzed for LLC resonant converter and its characteristics as increasing switching frequency. The other applications can be also considered to analyze stability and dynamics with small signal model. Using the analyzed open-loop model, the proper feedback compensator can be derived to achieve stable and fast dynamic closed-loop gain.

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