AIP | Applied Physics Letters

Schottky barrier modulation of metal/4H-SiC junction with thin interface spacer driven by surface polarization charge on 4H-SiC substrate

Gahyun Choi, Hoon Hahn Yoon, Sungchul Jung, Youngeun Jeon, Jung Yong Lee, Wook Bahng, and Kibog Park

Articles you may be interested in

Diameter dependent thermal sensitivity variation trend in Ni/4H-SiC Schottky diode temperature sensors
J. Vac. Sci. Technol. B **33**, 052207 (2015); 10.1116/1.4929890

Vertically grown Ge nanowire Schottky diodes on Si and Ge substrates
J. Appl. Phys. **118**, 024301 (2015); 10.1063/1.4923407

High-temperature and reliability performance of 4H-SiC Schottky-barrier photodiodes for UV detection
J. Vac. Sci. Technol. B **33**, 040602 (2015); 10.1116/1.4923083

Electrical characterization of (Ni/Au)/Al0.25Ga0.75N/GaN/SiC Schottky barrier diode
J. Appl. Phys. **110**, 013701 (2011); 10.1063/1.3600229

Fabrication of n-type 4H–SiC/Ni junctions using electrochemical deposition
Appl. Phys. Lett. **76**, 1300 (2000); 10.1063/1.126015

AIP | Applied Physics Reviews

NEW Special Topic Sections

NOW ONLINE
Lithium Niobate Properties and Applications: Reviews of Emerging Trends

AIP | Applied Physics Reviews

Schottky barrier modulation of metal/4H-SiC junction with thin interface spacer driven by surface polarization charge on 4H-SiC substrate

Gahyun Choi,[1] Hoon Hahn Yoon,[1] Sungchul Jung,[1] Youngeun Jeon,[2] Jung Yong Lee,[1] Wook Bahng,[3] and Kibog Park[1,2,a)]

[1]Department of Physics, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, South Korea
[2]School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, South Korea
[3]Power Semiconductor Research Center, Korea Electrotechnology Research Institute (KERI), Changwon 642-120, South Korea

The Au/Ni/Al$_2$O$_3$/4H-SiC junction with the Al$_2$O$_3$ film as a thin spacer layer was found to show the electrical characteristics of a typical rectifying Schottky contact, which is considered to be due to the leakiness of the spacer layer. The Schottky barrier of the junction was measured to be higher than an Au/Ni/4H-SiC junction with no spacer layer. It is believed that the negative surface bound charge originating from the spontaneous polarization of 4H-SiC causes the Schottky barrier increase. The use of a thin spacer layer can be an efficient experimental method to modulate Schottky barriers of metal/4H-SiC junctions. © 2015 AIP Publishing LLC.
[http://dx.doi.org/10.1063/1.4938070]

Silicon carbide (SiC) has been considered as a prominent wide band-gap semiconductor for high power device applications. Its superior material properties including high breakdown voltage and high thermal conductivity make it possible to overcome the limitations of silicon as the base material for power devices.[1–3] It is well-known that SiC forms various polytypes differentiated by the stacking sequence of Si-C bilayer and some material properties of SiC are strongly dependent on polytype.[4–7] *Spontaneous Polarization* (SP) is one of the polytype-dependent material properties. 3C-SiC with cubic symmetry does not have SP. However, all other polytypes with so called hexagonal turn in stacking (Antiphase boundary), where the tetrahedral sp3 bonds of Si and C atoms are out of balance, possess SP.[8–10] In this letter, we address the influence of the SP of 4H-SiC on the Schottky barrier (SB) at the metal/4H-SiC interface when a small gap between a metal contact and the 4H-SiC substrate is created by inserting a thin spacer film. In case of n-type Si-face 4H-SiC substrate, the interface SB is expected to increase due to the negative polarization charges induced on the 4H-SiC surface.[11,12] As model systems to evaluate this idea, Au/Ni/4H-SiC and Au/Ni/Al$_2$O$_3$/4H-SiC junctions are compared in terms of their electrical properties including current-voltage (I-V) and capacitance-voltage (C-V) characteristics.

Au/Ni/4H-SiC and Au/Ni/Al$_2$O$_3$/4H-SiC junctions were fabricated on an n-type 4H-SiC wafer purchased from Cree Inc. The 4H-SiC wafer contains a 17.8 μm thick n-type 4H-SiC epilayer of $\sim 2 \times 10^{15}$ cm^{-3} doping. The epilayer was grown on an n-type 8.06° miscut 4H-SiC substrate with a 0.5 μm thick n-type buffer layer of $\sim 1 \times 10^{18}$ cm^{-3} doping grown beforehand. Two small pieces cut from the 4H-SiC wafer were degreased with trichloroethylene, acetone, and methanol and then cleaned by HF(49%) dipping and a

methanol rinse to remove any oxide layer residing on the 4H-SiC wafer. After cleaning, the deposition of a $\sim$3 nm thick Al$_2$O$_3$ thin film was carried out on one of the two pieces by using atomic layer deposition (ALD) (LUCIDA D100 system, NCD Corporation, South Korea). The Al$_2$O$_3$ film was grown at 200 °C under constant N$_2$ flow (50 sccm) by using trimethylaluminum (TMA) and water (H$_2$O) as precursors. The growth rate was $\sim$1.2 Å per one complete ALD cycle which was composed of 0.2 s pulse of TMA followed by 10 s pause and 0.2 s pulse of H$_2$O followed by 10 s pause. Once all ALD cycles were completed, N$_2$ flow increased to 500 sccm and continued for 3 min as a post process. Then, Au/Ni electrodes (200 nm/500 nm) were deposited through a metal shadow mask on both pieces by using e-beam evaporation at room temperature. Fig. 1(a) shows the cross-sectional high resolution transmission electron microscopy (HRTEM) image of the Au/Ni/Al$_2$O$_3$/4H-SiC junction. In the HRTEM image, the oxide layer is measured to be $\sim$4.3 nm thick, which is somewhat larger than the thickness of the Al$_2$O$_3$ film expected from the ALD process. It is considered that the oxide layer observed in the HRTEM image is a stack of the deposited Al$_2$O$_3$ film and a native oxide known to be $\sim$1.0 nm on 4H-SiC surface.[13] It is quite probable to have some native oxide grown during device fabrication, although the wafer surface is cleaned with HF in advance. This very thin native oxide is expected to exist in the Au/Ni/4H-SiC junction as well. Fig. 1(b) shows the cross-sectional HRTEM image of the Au/Ni/4H-SiC junction where the native oxide is barely seen at the interface of the 4H-SiC substrate and the Ni film, implying that it is quite thin.

After the device fabrication was completed, the current-voltage (I-V) curves were measured on the Au/Ni/4H-SiC and Au/Ni/Al$_2$O$_3$/4H-SiC junctions by using a KEITHLEY current amplifier (Model 428) which is capable of amplifying current signals while applying biases simultaneously. As shown in Fig. 2(a), both junctions show the normal rectifying

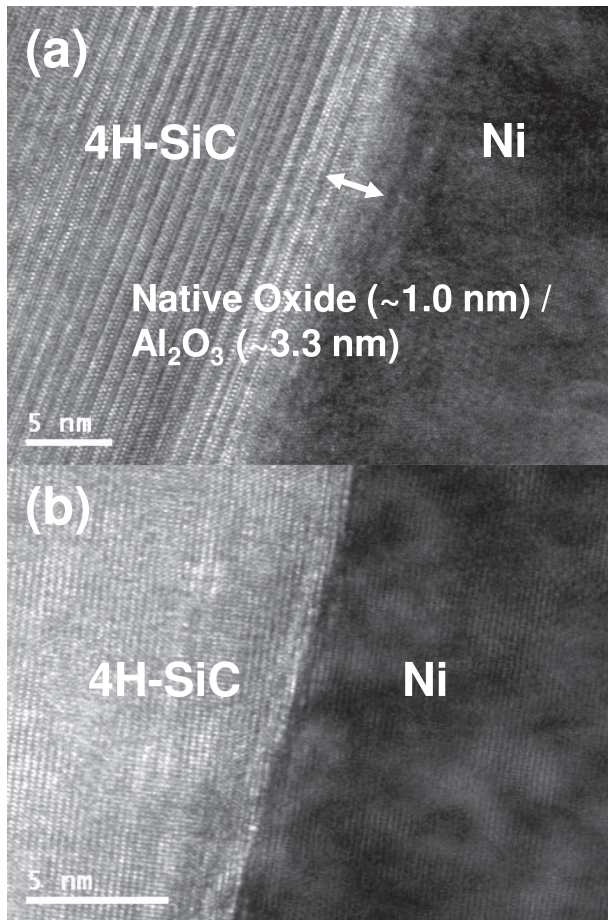a)Electronic mail: kibogpark@unist.ac.kr. Tel.: +82522172111.

FIG. 1. (a) Cross-sectional HRTEM image of Au/Ni/Al$_2$O$_3$/4H-SiC junction: The oxide thickness between metal electrode and 4H-SiC substrate is estimated to be ~4.3 nm, which is considered to be a stack of native oxide (SiO$_2$, ~1.0 nm) and ALD-grown Al$_2$O$_3$ (~3.3 nm) layers. The crystal plane of 4H-SiC in the image is (11–20). (b) Cross-sectional HRTEM image of Au/Ni/4H-SiC junction: A very thin native oxide (SiO$_2$) that is not noticeable obviously is expected to reside at the Ni/4H-SiC interface. The crystal plane of 4H-SiC substrate in the image is (1–100).

FIG. 2. (a) The current density vs. forward bias curves for Au/Ni/4H-SiC (black) and Au/Ni/Al$_2$O$_3$/4H-SiC (red) junctions in semi-logarithmic scale (b) The linear correlation between measured Schottky barrier and corresponding ideality factor for Au/Ni/4H-SiC (black) and Au/Ni/Al$_2$O$_3$/4H-SiC (red) junctions: The Schottky barrier excluding the influences of low-barrier areas can be estimated from the intercept of the fitted straight line with the $n = 1.01$ vertical line.

I-V characteristics of an n-type Schottky contact. The Schottky behavior shown in the Au/Ni/Al$_2$O$_3$/4H-SiC junction even with the Al$_2$O$_3$ spacer layer inserted is considered to be due to the leakiness of the spacer layer itself, associated with direct tunneling or trap-assisted conduction through it. Even though the Al$_2$O$_3$ spacer layer is quite transparent in electron transport, it can still be resistive. Hence, the larger junction resistance (above threshold region) observed in the I-V curve of the Au/Ni/Al$_2$O$_3$/4H-SiC junction, compared with the Au/Ni/4H-SiC junction, is considered to rely on the additional resistance through the Al$_2$O$_3$ spacer layer. One important feature to be emphasized in Fig. 2(a) is that the I-V curve of the Au/Ni/Al$_2$O$_3$/4H-SiC junction appears to turn on at a voltage substantially higher than the Au/Ni/4H-SiC junction. According to the thermionic-emission theory,[14–17] the current density of a Schottky contact near threshold at temperature T can be described as $J = A^* T^2 \exp\left(-q\phi_B/k_B T\right) \left[\exp\left(qV/nk_B T\right) - 1\right]$, where A^* is the effective Richardson constant, q is the magnitude of electron charge, k_B is the Boltzmann constant, ϕ_B is the Schottky barrier, V is the sample bias, and n is the ideality factor. By fitting the semi-log plot of the measured I-V curves shown in Fig. 2(a) to the thermionic-emission
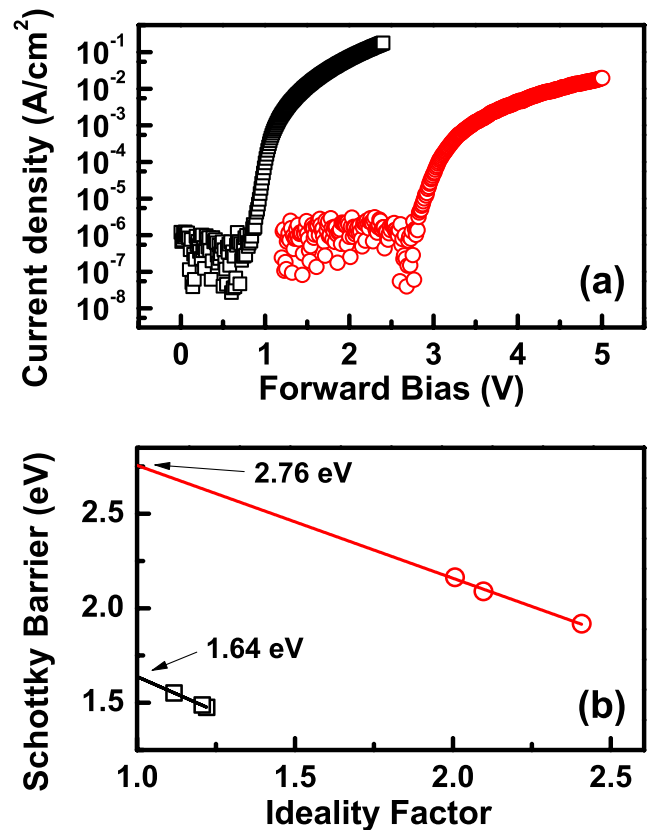
theory with the effective Richardson constant of 4H-SiC (~146 A cm^{-2} K^{-2}),[18] the Schottky barrier of the Au/Ni/4H-SiC junction is estimated to be 1.51 ± 0.04 eV and that of the Au/Ni/Al$_2$O$_3$/4H-SiC junction be 2.06 ± 0.13 eV. It is also relevant here to note that the ideality factor (n) of the Au/Ni/Al$_2$O$_3$/4H-SiC junction is estimated to be 2.17 ± 0.21 much larger than the ideal Schottky case ($n = 1$). In case of the Au/Ni/4H-SiC junction, the ideality factor is estimated to be 1.18 ± 0.06. The non-ideal behavior of the Au/Ni/Al$_2$O$_3$/4H-SiC junction is considered to be associated mainly with the non-uniform thickness of the Al$_2$O$_3$ spacer layer, implying the existence of some areas with their *local* Schottky barriers lower than the surrounding. Several previous works[19–21] have demonstrated that these low-barrier areas influence I-V curves quite significantly, even though their relative portion in the entire contact is small. They tend to increase the ideality factor of a measured I-V curve and make the Schottky barrier to be estimated lower than the one on the prevailing surrounding area.[20–23] As Tung pointed out,[24] the energy band profile of low-barrier area on the semiconductor side will be pinched off due to the influence of high-barrier surrounding. If the low-barrier area is small enough, the pinch-off will be enhanced to almost close the low-barrier area. In this case, the low-barrier areas become invisible in terms of carrier transport, and the Schottky junction will show more ideal behavior. Hence, the large ideality factor of our

TABLE I. Electrical properties of Au/Ni/4H-SiC and Au/Ni/Al$_2$O$_3$/4H-SiC junctions.

	J_0 (A/cm^2)	Ideality factor	ϕ_B from I-V (eV)	ϕ_B from C-V (eV)
Au/Ni/4H-SiC	$(1.06 \pm 0.91) \times 10^{-18}$	1.18 ± 0.06	1.51 ± 0.04	1.97 ± 0.027
Au/Ni/Al$_2$O$_3$/4H-SiC	$(2.26 \pm 2.25) \times 10^{-26}$	2.17 ± 0.21	2.06 ± 0.13	3.21 ± 0.082

Au/Ni/Al$_2$O$_3$/4H-SiC junction indicates that some low-barrier areas with non-negligible sizes exist in the junction. The relevant electrical parameters of the Au/Ni/4H-SiC and Au/Ni/Al$_2$O$_3$/4H-SiC junctions including the reverse saturation current density (J_0), the ideality factor, and the Schottky barrier (ϕ_B) extracted from the measured I-V curves are listed in Table I. Fig. 2(b) shows the linear correlation between the Schottky barriers and the corresponding ideality factors extracted from the measured I-V curves. By finding the intercept of the straight line fitted to the measured data with the $n = 1.01$ vertical line, the Schottky barrier excluding the influences of low-barrier areas can be estimated. The estimated Schottky barrier is ~1.64 eV for the Au/Ni/4H-SiC junction and ~2.76 eV for the Au/Ni/Al$_2$O$_3$/4H-SiC junction.

In order to extract the Schottky barriers on the prevailing areas of the two (*with* and *without* Al$_2$O$_3$ spacer layer) junctions, C-V curves were measured with an Agilent E4980 LCR meter by applying a reverse bias (V_r) ranging from 0 V to 2.2 V. An AC voltage with its amplitude of 50 mV and frequency of 1 MHz was added to the reverse bias for measuring the bias-dependent differential capacitance per unit area $C = dQ/dV$. Fig. 3(a) shows the C-V curves measured
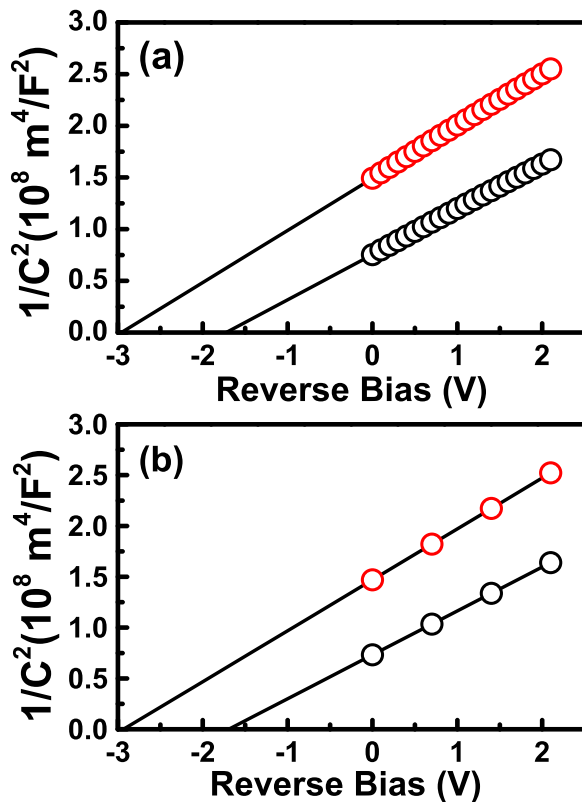

FIG. 3. The capacitance-voltage ($1/C^2$ vs. V_r) plots (a) measured and (b) obtained by performing finite element electrostatic modeling for Au/Ni/4H-SiC (black) and Au/Ni/Al$_2$O$_3$/4H-SiC (red) junctions with the linearly fitted lines (black lines). The calculation is found to best-fit the measurements with the spontaneous polarization of 4H-SiC assumed to be 3.00×10^{-2} C/m^2.

on the Au/Ni/4H-SiC (black circles) and Au/Ni/Al$_2$O$_3$/4H-SiC (red circles) junctions. The measured data are plotted as $1/C^2$ vs. V_r, with the linearly fitted lines (black lines). According to the abrupt depletion approximation,[16,17,25] $1/C^2$ satisfies the relation $1/C^2 = 2/qN_d\varepsilon_s\varepsilon_0(\phi_B - \xi + V_r - k_BT/q)$, where N_d is the donor density, ε_s is the static dielectric constant of the semiconductor, ε_0 is the vacuum permittivity, and ξ is the difference in energy between the Fermi level and the conduction band minimum in the semiconductor bulk. The doping concentration (N_d) can be obtained from the slope of the linearly fitted line by using the relation $N_d = (2/q\varepsilon_s\varepsilon_0)/[d(1/C^2)/dV_r]$. The extracted N_d was $(3.34 \pm 0.23) \times 10^{15}$ cm^{-3} for the Au/Ni/4H-SiC junction and $(2.90 \pm 0.10) \times 10^{15}$ cm^{-3} for the Au/Ni/Al$_2$O$_3$/4H-SiC junction. Both are close to the value 2.00×10^{15} cm^{-3} provided by the wafer vendor. The Schottky barrier ϕ_B can also be extracted from the $1/C^2$ vs. V_r plot by using the relation $\phi_B = -V_i + \xi + k_BT/q$, where V_i is the intercept of the fitted straight line with the V_r axis. Using this procedure, the Schottky barrier of the Au/Ni/Al$_2$O$_3$/4H-SiC junction is estimated to be 3.21 ± 0.082 eV, while that of the Au/Ni/4H-SiC junction is 1.97 ± 0.027 eV (Table I). Here, it is noticeable that the Schottky barriers extracted from C-V measurements are larger than the I-V measurement counterparts, even after excluding the influences of low-barrier. The discrepancies between C-V and I-V measured Schottky barriers exceed the amounts expected from the image force lowering which is estimated to be ~29 meV and ~25 meV for the Au/Ni/Al$_2$O$_3$/4H-SiC and Au/Ni/4H-SiC junctions, respectively. It is thought that the capacitive component in the substrate ohmic contact and the stray capacitances associated with the configuration of our measurement system are the main contributors. These additional capacitive components tend to make the measured capacitance of Schottky junction smaller than its actual value. Then, the smaller measured capacitance will bear a larger intercept of the fitted straight line with the V_r axis in the $1/C^2$ vs. V_r plot so that the Schottky barrier is estimated to be higher. The additional capacitive components are expected to be quite similar for both Au/Ni/Al$_2$O$_3$/4H-SiC and Au/Ni/4H-SiC junctions. Therefore, their influences on determining the increase of Schottky barrier with the Al$_2$O$_3$ spacer inserted will be negligible. Similar to the I-V measurements, the C-V measured Schottky barrier of the Au/Ni/Al$_2$O$_3$/4H-SiC junction is much higher by an amount of ~1.24 eV than that of the Au/Ni/4H-SiC junction. Just as a note, the difference of I-V measured Schottky barriers for the two junctions is ~1.12 eV when excluding the influences of low-barrier areas. Related to the inertness to low-barrier areas, there is one important aspect to note for C-V measurements. For both Au/Ni/4H-SiC and Au/Ni/Al$_2$O$_3$/4H-SiC junctions, the oxide layer is much thinner than the depletion region in the 4H-SiC substrate which is estimated to be ~900 nm thick for ~2×10^{15} cm^{-3} doping. Accordingly, the
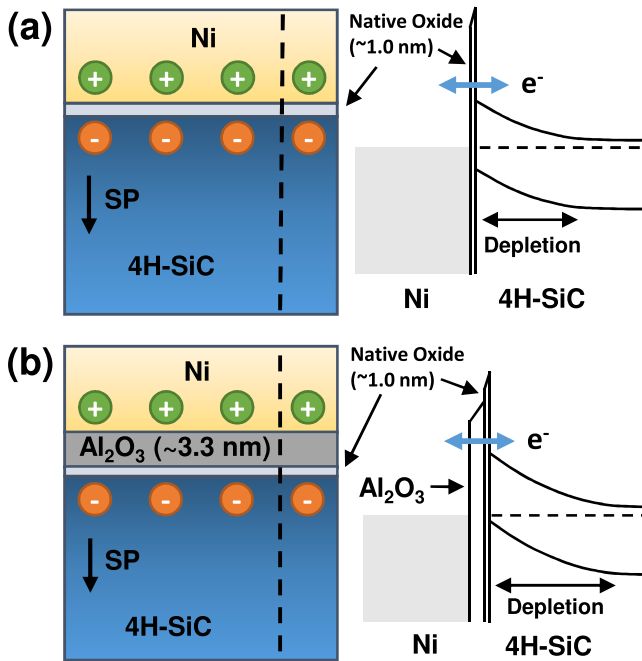
FIG. 4. Schematics of layer structure and energy band profile of (a) Au/Ni/4H-SiC and (b) Au/Ni/Al$_2$O$_3$/4H-SiC junctions. The energy band profiles are drawn along the dashed lines. In the Au/Ni/Al$_2$O$_3$/4H-SiC junction, the electrostatic potential energy for electron will jump noticeably across the oxide layer (Al$_2$O$_3$ spacer + native oxide). This electrostatic potential energy jump will be much smaller in the Au/Ni/4H-SiC junction (only native oxide). The jump of electrostatic potential energy causes the increase of Schottky barrier, and the depletion region in the 4H-SiC substrate is enlarged accordingly. The change of depletion region can be detected as the change of measured capacitance.

capacitance of the oxide layer (C_{ox}) will be much larger (over 200 times) than that of the depletion region (C_d). The measured capacitance (C_{eff}) is then almost entirely the one of the depletion region, since the oxide layer and the depletion region are connected in series ($C_{eff} = C_d/(1 + C_d/C_{ox}) \sim C_d$). Hence, the Schottky barrier with one-to-one correspondence to the depletion region thickness can be extracted from C-V measurements without being influenced by the small-portion low-barrier areas and also by the capacitive properties of the Al$_2$O$_3$ spacer layer in the surrounding high-barrier area.

The increase of Schottky barrier with the Al$_2$O$_3$ spacer layer observed in I-V and C-V measurements is believed to originate from negative charges bound on the 4H-SiC surface associated with the surface termination of the SP of 4H-SiC. As shown in Fig. 4, the negative polarization charges on the 4H-SiC surface will form a dipole layer together with the same amount of positive charges induced on the metal electrode surface. The electrostatic potential energy will increase linearly across the dipole layer (from metal surface to 4H-SiC surface). It is noted that the electrostatic potential energy here is for electron. With this increase of electrostatic potential energy, the position of the conduction band minimum on the 4H-SiC surface specified from

the Fermi level in the metal electrode will be raised, implying the increase of Schottky barrier. In case of the Au/Ni/4H-SiC junction, the electrostatic potential energy increases only across the thin native oxide (Fig. 4(a)). On the other hand, for the Au/Ni/Al$_2$O$_3$/4H-SiC junction, there will be an additional jump of electrostatic potential energy through the Al$_2$O$_3$ spacer, resulting in a much higher Schottky barrier than the Au/Ni/4H-SiC junction (Fig. 4(b)).

In order to evaluate the idea of dipole layer formation driven by the surface polarization charge, finite element electrostatic modeling was performed to calculate the C-V curves theoretically using a commercial software package FLEXPDE.[26] By following the procedure used in Ref. 27, we define the total electron potential energy in the oxide layer and 4H-SiC substrate as $\phi_{tot} = \phi(x,y,z) + (\phi_m - \chi)$, where $\phi(x,y,z)$ is the electrostatic potential energy, ϕ_m is the work function of the metal electrode (Ni), and χ is the electron affinity of Al$_2$O$_3$, SiO$_2$, or 4H-SiC. $\phi(x,y,z)$ is determined by solving the Poisson's equation $\nabla^2[\phi/(-q)] = -\rho(x,y,z)/\varepsilon_0\varepsilon$, where $\rho(x,y,z)$ is the net charge density in the oxide layer or 4H-SiC substrate, and ε is the relative dielectric constant of Al$_2$O$_3$, SiO$_2$, or 4H-SiC. The net charge density is assumed to be zero inside the oxide layers and is given as $\rho(x,y,z) = q[N_d - n_c(x,y,z)]$ in the 4H-SiC substrate, where n_c is the free electron density. The free electron density is calculated as $n_c = N_c \exp[(E_{F,S} - \phi_{tot})/k_BT]$, where N_c is the electron effective density of states for 4H-SiC ($1.83 \times 10^{19} cm^{-3}$), and $E_{F,S} = -qV_r$ is the Fermi level energy inside the 4H-SiC substrate with an applied reverse bias V_r. For the dopant density, the extracted value from the measured C-V curve was used. The negative polarization charge on the 4H-SiC surface was implemented in the calculation as the boundary condition at the oxide/4H-SiC interface. The material parameters used in the modeling are listed in Table II. The differential capacitance was obtained by quantifying the change of the charge Q_m induced on the metal electrode surface as the applied reverse bias varies by a small amount, i.e., $C = \Delta Q_m/\Delta V_r$, where $\Delta Q_m = Q_m(V_r) - Q_m(V_r + \Delta V_r)$. The calculation was repeated by varying the SP of 4H-SiC, and the calculated C-V curves were found to best-fit to the measured ones with the SP of 4H-SiC assumed to be 3.00×10^{-2} C/m^2, as shown in Fig. 3(b). This best-fit SP of 4H-SiC is a bit larger but fairly close to the theoretically predicted[5,8,9] or experimentally estimated values,[32,33] ranging between $(1.10 - 2.16) \times 10^{-2}$ C/m^2.

In conclusion, it has been demonstrated experimentally that the Au/Ni/Al$_2$O$_3$/4H-SiC junction with a thin Al$_2$O$_3$ film as spacer layer shows normal rectifying behavior of a Schottky contact, with its threshold voltage significantly higher than the Au/Ni/4H-SiC junction with no spacer. Direct tunneling or trap-assisted conduction is considered to occur through the thin Al$_2$O$_3$ spacer to yield the rectifying characteristics of the junction. The significant threshold voltage increase of the Au/Ni/Al$_2$O$_3$/4H-SiC junction is believed

TABLE II. The material parameters used for finite element electrostatic modeling.

ϕ_m(Ni) (Ref. 28)	χ_{4H-SiC} (Ref. 28)	χ_{SiO_2} (Ref. 29)	$\chi_{Al_2O_3}$ (Ref. 30)	ε_{4H-SiC} (Ref. 27)	ε_{SiO_2} (Ref. 31)	$\varepsilon_{Al_2O_3}$ (Ref. 31)
5.10 eV	4.05 eV	0.9 eV	1.35 eV	9.7	3.9	9.0

to result from the jump in electrostatic potential energy for electron across the dipole layer composed of the negative spontaneous polarization charges bound on the 4H-SiC surface and the compensating positive charges induced on the metal electrode surface. The finite element electrostatic modeling reproduces the measured C-V curves correctly when the SP of 4H-SiC is assumed properly. This assumed SP of 4H-SiC is found to be fairly close to the theoretical and experimental values reported previously. Our results suggest that the SP of 4H-SiC can be an efficient tool to modulate Schottky barriers of metal/4H-SiC junctions, in conjunction with thin interface spacer layers.

[1]V. E. Chelnokov, A. L. Syrkin, and V. A. Dmitriev, Diamond Relat. Mater. **6**, 1480 (1997).

[2]J. B. Casady and R. W. Johnson, Solid-State Electron. **39**, 1409 (1996).

[3]*Diamond, SiC, and Nitride Wide Bandgap Semiconductors*, edited by C. H. Carter, Jr., G. Gildenblat, S. Nakamura, and R. J. Nemanich (Materials Research Society, Pittsburgh, 1994).

[4]A. R. Verma and P. Krishna, *Polymorphism and Polytypism in Crystals* (Wiley, New York, 1966).

[5]A. Qteish, V. Heine, and R. J. Needs, Physica B **185**, 366 (1993).

[6]C. H. Park, B.-H. Cheong, K.-H. Lee, and K. J. Chang, Phys. Rev. B **49**, 4485 (1994).

[7]F. Bechstedt, P. Käckell, A. Zywietz, K. Karch, B. Adolph, K. Tenelsen, and J. Furthmüller, Phys. Status Solidi B **202**, 35 (1997).

[8]A. Qteish, V. Heine, and R. J. Needs, Phys. Rev. B **45**, 6534 (1992).

[9]S. Yu. Davydov and A. V. Troshin, Phys. Solid State **49**, 759 (2007).

[10]S. Yu. Davydov, A. A. Lebedev, and O. V. Posrednik, Semiconductors **46**, 913 (2012).

[11]E. H. Nicollian, B. Schwartz, D. J. Coleman, R. M. Ryder, and J. R. Brews, J. Vac. Sci. Technol. **13**, 1047 (1976).

[12]K. Park, H. S. Go, Y. Jeon, J. P. Pelz, X. Zhang, and M. Skowronski, Appl. Phys. Lett. **99**, 252102 (2011).

[13]Z. Zolnai, N. Q. Khánh, E. Szilágyi, Z. E. Horváth, and T. Lohner, in XV International Conference for Physics Students ICPS 2000, Zadar, Croatia, 4–11 August 2000 (IAPS, France, 2000).

[14]C. R. Crowell and S. M. Sze, Solid-State Electron. **9**, 1035 (1966).

[15]E. H. Rhoderick, J. Phys. D **3**, 1153 (1970).

[16]E. H. Rhoderick, Solid-State and Electron Devices, IEE Proceedings I **129**, 1 (1982).

[17]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, New York, 2006).

[18]A. Itoh, T. Kimoto, and H. Matsunami, IEEE Electron Device Lett. **16**(6), 280 (1995).

[19]R. T. Tung, Appl. Phys. Lett. **58**, 2821 (1991).

[20]Q.-W. Song, Y.-M. Zhang, Y.-M. Zhang, F.-P. Chen, and X.-Y. Tang, Chin. Phys. B **20**, 057301 (2011).

[21]R. T. Tung, Mater. Sci. Eng., R **35**, 1 (2001).

[22]R. F. Schmitsdorf, T. U. Kampen, and W. Monch, J. Vac. Sci. Technol., B **15**, 1221 (1997).

[23]T. N. Oder, T. L. Sung, M. Barlow, J. R. Williams, A. C. Ahyi, and T. Isaacs-Smith, J. Electron. Mater. **38**, 772 (2009).

[24]R. T. Tung, Phys. Rev. B **45**, 13509 (1992).

[25]L. J. Brillson, Surf. Sci. Rep. **2**, 123 (1982).

[26]PDE Solutions, Inc., Spokane Valley, WA, U.S.A., http://www.pdesolutions.com

[27]K.-B. Park, Y. Ding, J. P. Pelz, M. K. Mikhov, Y. Wang, and B. J. Skromme, Appl. Phys. Lett. **86**, 222109 (2005).

[28]T. V. Blank, Yu. A. Goldberg, E. A. Posse, and F. Yu. Soldatenkov, Semiconductors **44**, 463 (2010).

[29]R. Williams, Phys. Rev. **140**, A569 (1965).

[30]J. Ren, B. Li, J.-G. Zheng, and J. Liu, Solid-State Electron. **67**, 23 (2012).

[31]C. M. Tanner, Y.-C. Perng, C. Frewin, S. E. Saddow, and J. P. Chang, Appl. Phys. Lett. **91**, 203510 (2007).

[32]S. Bai, R. P. Devaty, W. J. Choyke, U. Kaiser, G. Wagner, and M. F. MacMillian, Appl. Phys. Lett. **83**, 3171 (2003).

[33]A. Fissel, U. Kaiser, B. Schröter, W. Richter, and F. Bechstedt, Appl. Surf. Sci. **184**, 37 (2001).