Analytical Probability Density Calculation of Power-Supply-Induced Jitter in high-speed Tx circuits

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Abstract

As the speed of I/O interface has increased up to multi-gigabit data rates [1], the research of signal integrity issues for the I/O channel is more demanding. The statistical approach to get jitter in time domain can reduce computational time and effort compared to the typical transient SPICE simulations.

In this paper, the output voltage waveforms of the multi-stage buffers are calculated with simpler analytical solutions. The driving non-linear MOSFETs are replaced by Thevenin equivalent voltages and impedances, and the solutions of differential equations can be simply expressed with corresponding impulse responses. Also, the jitter induced by the supply voltage fluctuations can be calculated. The supply voltage fluctuations in the time domain are directly convolved with the impulse responses to obtain the output waveforms.

The validation of the proposed analytic method is done by experiments. In the experiments, the voltage fluctuations in time domain are measured both at the integrated circuit (IC) and printed circuit board (PCB) pads simultaneously. Then, the on-chip supply voltage fluctuations are extracted from the measured results. The Power Distribution Network (PDN) of the IC and PCB are modeled from impedance measurements on the pads. Using the PDN model, the measured power and ground voltage fluctuations are validated with the SPICE simulation. The output off-chip channel of the victim buffer can be modeled as parasitic inductances and capacitances from the measured two-port S-parameters at the designed PCB channel. As the number of buffer stages connected to the fluctuating supply voltages are varied from one to three in the experiments, the effect on the output waveform induced by supply voltage fluctuations can be investigated. The calculated step responses and jitter PDFs of the multi-stage buffers are all validated with measured output waveforms and jitter histograms.

In addition, the Electrostatic discharge (ESD) protection structures which are commonly employed at near the I/O pins can induce parasitic junction capacitance (C_{ESD}) and parasitic resistance (R_{ESD}) causing parasitic effects. Thus, the supply voltage fluctuations also can couple through ESD parasitic. The step responses of a linear output driver with silicon interposer channel are derived including the parasitics of ESD protection circuits. The probability density functions of the output voltage due to supply voltage fluctuations are also analytically calculated. With changing the frequency of supply voltage fluctuations, the effect of ESD parasitics on the output jitter is calculated and compared.

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I. Introduction

1.1 Research background

1.1.1 Jitter and Eye diagram

As the speed of data rates increased, higher jitter levels and degraded waveforms are becoming problem. Jitter can be defined as "the short term deviation of a signal from its ideal location." Both amplitude and phase noise can generate jitter as shown in Figure 1. These variations fundamentally limit the noise margin of signal and degrade the reliability of system.

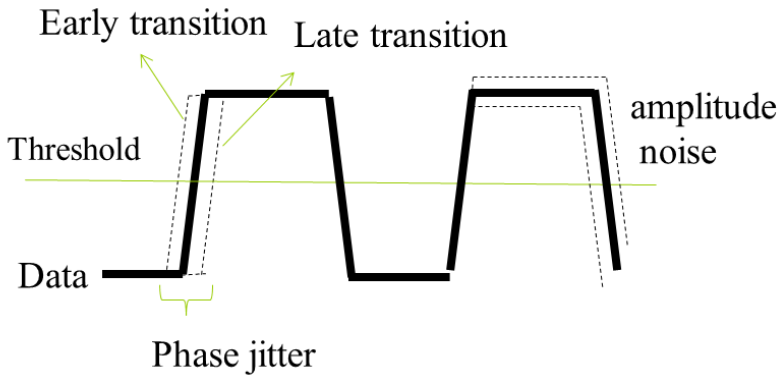


Figure 1. Jitter caused by phase noise and amplitude noise

An Eye diagram is commonly used as quality indicator of signals in high speed digital data system, verifying transmitter output compliance and revealing the amplitude and time distortion elements. As shown in Figure 2, eye diagram is obtained by the superimposing the data sequence. The more opened eye means the lower possibility for happening error at the transmitter. Eye diagram gives intuitive information for the reliability of data signal.

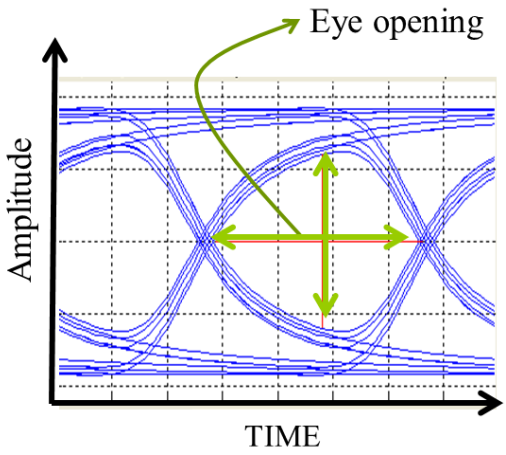


Figure 2. The example for Eye diagram

1.1.2 Jitter components

As shown in Figure 3, jitter can be distinguished as two categories, random jitter(RJ) and deterministic jitter(DJ). The cause of random jitter is mainly external factors such as thermal noise, and the probability density function(PDF) of RJ follows a Gaussian distribution. Because RJ is unbounded, peak-to-peak value of RJ is not well defined. On the contrary, deterministic jitter is bounded, and it concludes periodic jitter(PJ), data-dependent jitter(DDJ), etc. Supply voltage fluctuation is one of the main causes for DDJ or PJ.

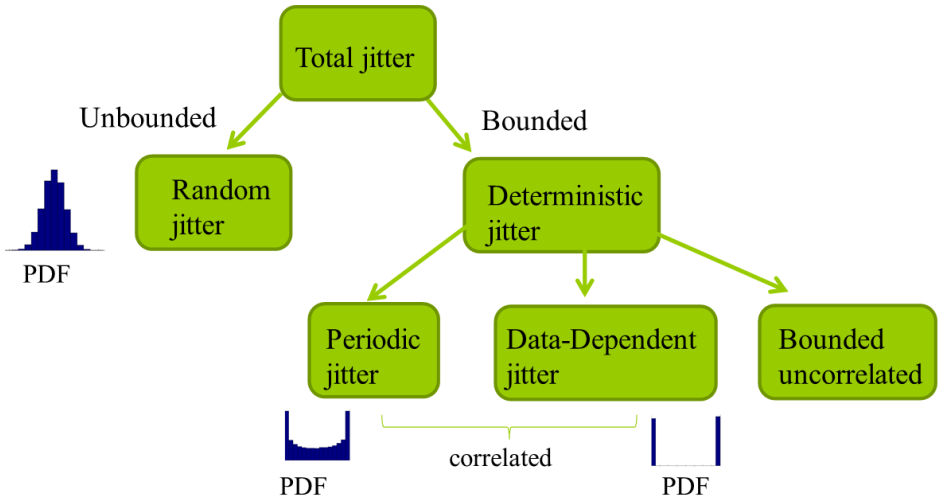


Figure 3. Categories of jitter

1.1.3 Bit Error Rate(BER)

To figure out the integrity of the transmitted data the Bit Error Rate (BER) can be measured. When a known pseudo-random bit stream is supplied as input signal, the output of the device under test (DUT) can be compared with known data. The number of total data patterns and errors are counted as N_{Bits} and N_{Err}, respectively. Thus, the BER can be obtained as

$$BER = N_{Err} / N_{Bits}$$

However, measuring BER requires huge effort and time. It can be obtained considering all possible data patterns. Instead, BER can be statistically calculated using given jitter PDF as shown in Figure 4. If we have information about the jitter PDF, BER can be easily calculated.

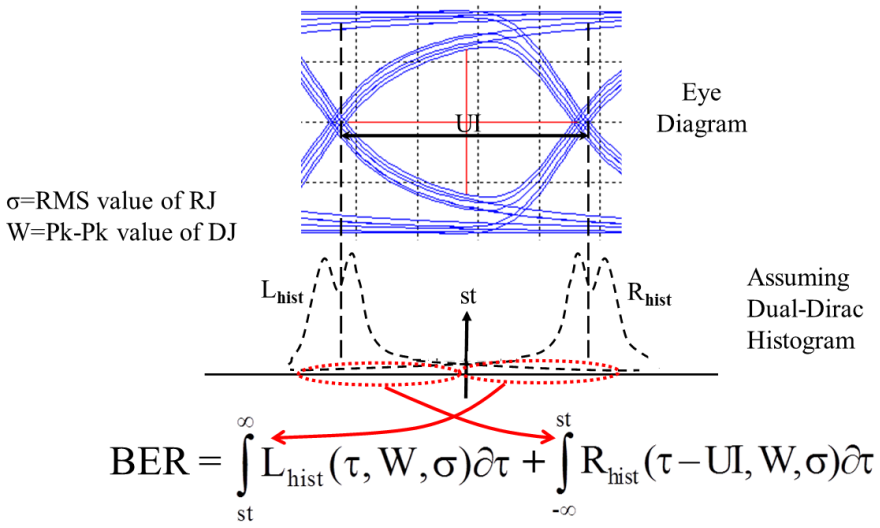


Figure 4. Statistical calculation of BER

1.1.4 Supply Voltage Fluctuations

Supply voltage fluctuations are mainly generated by the switching of large number buffers on logic circuits which is highly input pattern dependent. When buffers switch in the circuit, the shoot-through current is generated as shown in Figure 5. The current flowing through parasitic inductance of the circuit results in voltage fluctuations as shown in Figure 6. If the amount of current increased and the clock frequency are increased, the more voltage fluctuations will be induced.

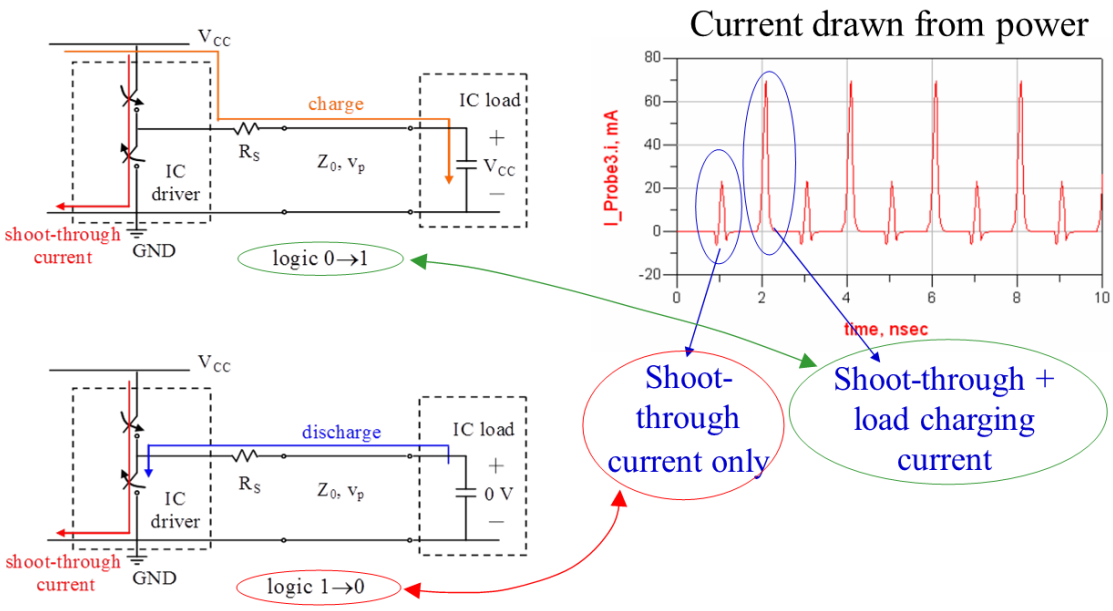


Figure 5. Generation of shoot-through current from buffer switching

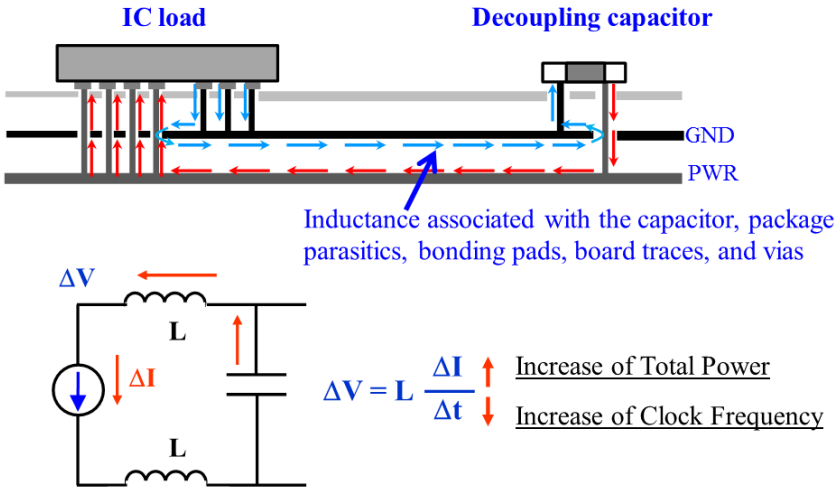
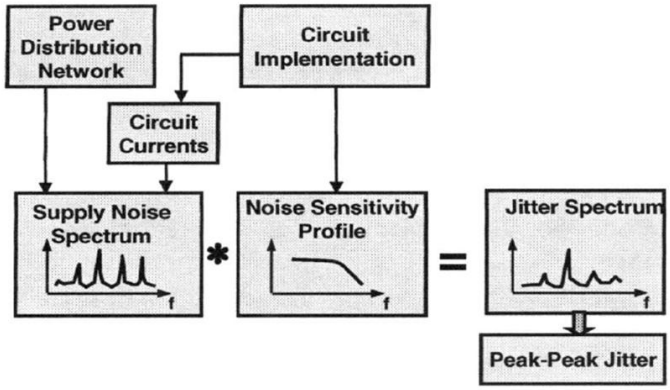


Figure 6. The supply voltage fluctuations induced by parasitic inductance

In this paper, the jitter caused by supply voltage fluctuation is mainly investigated. Also, in the experiment, on-chip power and ground fluctuations which are generated by aggressor buffers are obtained from the direct measurement results at the pads on the IC and PCB.

1.2 Previous Research

There have been several studies related to the jitter induced by supply voltage fluctuations. In 2003, Lauren Hui Chen has solved the delay change of the inverter induced by the DC level shift of power and ground. In 2007, Ralf Schmitt have defined jitter sensitivity due to supply voltage fluctuation as shown in Figure 7, and investigate the relation between jitter spectrum and supply noise spectrum.



$$Sensitivity = \frac{Jitter(f_{sample})}{Noise(f_{sample})}[ps/mV]$$

Figure 7. Schematic of the relation between supply noise and jitter in frequency domain

In 2013, Chulsoon Hwang have analytically derived the transfer function relating supply voltage fluctuations to jitter in closed form expressions for a single-ended buffer. In the Table 1, the previous researches are briefly compared to the work handled in this paper.

Table 1. Comparison to the previous researches

Title	Buffer delay change in the presence of power and ground noise	Investigating the impact of supply noise on the jitter in gigabit I/O interfaces	Analytical Transfer Functions relating Power and Ground Voltage Fluctuations to Jitter at a Single-Ended Full-Swing Buffer	**This work**
Authors	Lauren Hui Chen	Ralf Schmitt	Chulsoon Hwang	**Eunkyeong Park**

Publish (Year)	IEEE Transactions on Very Large Scale Integration (VLSI) Systems (2003)	IEEE Electrical Performance of Electronic Packaging (2007)	IEEE Transactions on Components, Packaging and Manufacturing Technology (2013)	**A master's thesis (2015)**
Main Contribution	Calculation for the output delay change	The sensitivity of jitter was defined and demonstrated	The transfer function relating supply voltage fluctuations to jitter were analytically derived	**Jitter PDF at multi-stage buffer was calculated, validated with measurement**

II. Probability Density Function of Power-Supply-Induced Jitter (PSIJ) at Multi-stage Output Buffers

2.1 Why Multi-stage Buffers

In the common integrated circuit (IC) designs in practice, clock networks with multi-stage repeating buffers are typically used to distribute a global reference clock to various parts of the chip [2]. Also, several pre-buffers are inserted at I/O buffers in ICs to reduce signal delays for driving the off-chip loads [3]. Both the clock tree and pre-buffers consist of multi-stage buffers, as depicted in Figure 8. Skew and jitter are major issues in the clock tree and I/O designs, and can fundamentally limit the performance of the IC.

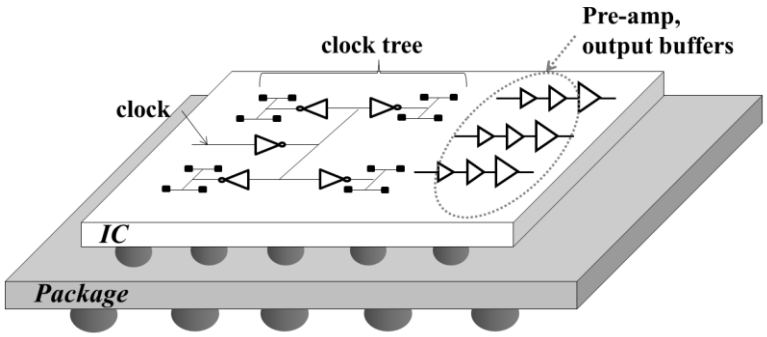


Figure 8. Clock tree and repeaters on the IC

2.2 Analytic Calculation for the Output of Multi-stage Buffers

2.2.1 Derivation for Single-stage Buffer Output

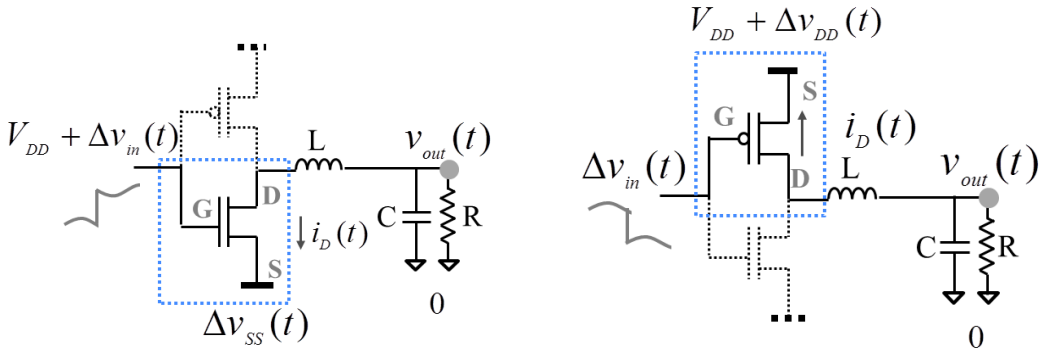
Non-linear MOSFETs can be piecewise linearly modeled. Both NMOS and PMOS can be divided into two regions, the triode and saturation regions depending on the magnitude of drain-

source voltage. When the magnitude of drain-source voltage, $|v_{DS}(t)|$ is sufficiently large, the MOSFET is in the saturation region. In the saturation region, the drain current of MOSFETs can be expressed with gate-source voltage and drain-source voltage as:

$$I_D(t) = G_{mp}V_{GS} + g_{mp}\Delta v_{GS}(t) + \lambda_p v_{DS}(t) \text{ for PMOS (1)}$$

$$I_D(t) = G_{mn}V_{GS} + g_{mn}\Delta v_{GS}(t) + \lambda_n v_{DS}(t) \text{ for NMOS (2)}$$

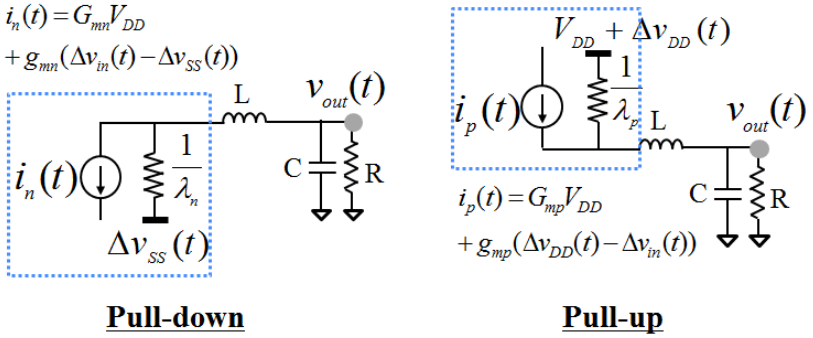
where G_{mp} and g_{mp} are the large- and small-signal transconductances of the PMOS; G_{mn} and g_{mn} represent the corresponding parameters of the NMOS; and λ_p and λ_n are the output conductances of the PMOS and NMOS relative to the drain-source voltage, respectively. $v_{DS}(t)$ is the drain-source voltage, and V_{GS} and $\Delta v_{GS}(t)$ are the dc level and fluctuation of the gate-source voltage, respectively. In the triode region of the MOSFETs with relatively small $v_{DS}(t)$, the PMOS and NMOS can be replaced by turn-on resistors, r_{onp} and r_{onp} respectively. With the modeling parameters of the MOSFETs, the expressions for a single-stage buffer output transition can be analytically calculated with given load conditions. As an example, the final stage buffer driving the parallel connection of C and R through L is calculated, as shown in Figure 9. C, R, and L represent the load capacitance, termination resistance, and parasitic inductance of an off-chip channel, respectively. When the fluctuating voltages on the power, ground, and input nets of the buffer are denoted as $\Delta v_{DD}(t)$, $\Delta v_{SS}(t)$, and $\Delta v_{in}(t)$, each equivalent MOSFET model in pull-down and pull-up transitions is expressed, as shown in Figure 10(a) and (b) for saturation and triode regions, respectively. The input voltage fluctuation, $\Delta v_{in}(t)$, may be caused by the output of the previous buffers in the multi-stage buffers. The reference of the load capacitance and termination resistor is assumed as zero potential.



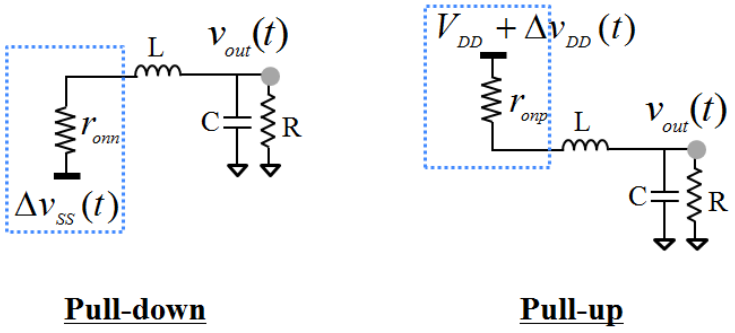
(a) (b)

Figure 9. Buffer configurations used in the analysis for (a) pull-down and (b) pull-up transitions

In the pull-down transition, the NMOS is firstly in the saturation region, because the magnitude of v_{DS}(t) is relatively large. As the output rises, $|v_{DS}(t)|$ gets smaller. After $|v_{DS}(t)|$ exceeds the boundary voltage between the triode and saturation regions, NMOS moves to the triode region. Similarly, the operation condition of the PMOS is changed from the saturation to the triode region in the pull-up transition.



(a)



(b)

Figure 10. The equivalent MOSFET models (a) in the saturation region and (b) in the triode region

The piecewise linear models of the MOSFETs in the dotted blue box of Figure 10(a) and (b) can be universally expressed using the Thevenin equivalent voltage source and resistor, v_{Thev}(t) and

R_{Thev}, as shown in Figure 11. All the expressions of v_{Thev}(t) and R_{Thev} for the pull-up and pull-down transitions are summarized in Table 2.

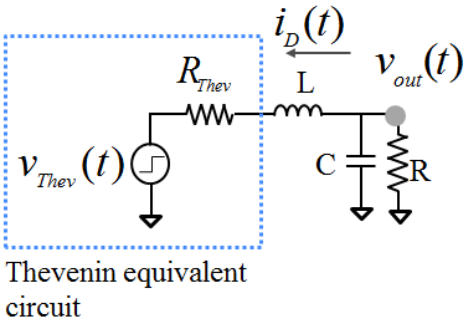


Figure 11. The universal buffer model using Thevenin equivalent circuits

Using the universal equivalent circuit of Figure 11, the output voltage v_{out}(t) is simply expressed with i_D(t), v_{Thev}(t), and R_{Thev} as:

$$v_{out}(t) = v_{Thev}(t)u(t) + R_{Thev}i_D(t) + L\frac{di_D(t)}{dt} \quad (3)$$

The drain current flowing through inductance is obtained from the summation of the current on the load capacitor, C, and the current on the load resistor, R, as:

$$i_D(t) = -C\frac{dv_{out}(t)}{dt} - \frac{v_{out}(t)}{R} \quad (4)$$

From (3) and (4), the second-order differential equation for v_{out}(t) can be obtained as:

$$v_{Thev}(t)u(t) = LC\frac{d^2v_{out}(t)}{dt^2} + \left(R_{Thev}C + \frac{L}{R}\right)\frac{dv_{out}(t)}{dt} + \left(1 + \frac{R_{Thev}}{R}\right)v_{out}(t) \quad (5)$$

The differential equation applies to both the saturation and triode regions. By converting to Laplace s-domain with the initial value and slope of the output voltage, $v_{out}(0)$ and $v_{out}'(0)$, the equation (5) is written as:

$$\frac{V_{Thev}(s)}{s} = LC\left(s^2V_{out}(s) - sv_{out}(0) - v_{out}'(0)\right) + \left(R_{Thev}C + \frac{L}{R}\right)\left(sV_{out}(s) - v_{out}(0)\right) + \left(1 + \frac{R_{Thev}}{R}\right)V_{out}(s) \quad (6)$$

The output voltage in the s-domain, $V_{out}(s)$, can be expressed with the transfer function $H(s)$ as:

$$V_{out}(s) = \frac{v_{out}(0)}{s} + \frac{1}{s}\left(V_{Thev}(s) - \left(\frac{R_{Thev}}{R} + 1\right)v_{out}(0)\right)H(s) + LCv_{out}'(0)H(s) \quad (7)$$

Where:

$$H(s) = \frac{1}{LCs^2 + s\left(\frac{L}{R} + R_{Thev}C\right) + \frac{R_{Thev}}{R} + 1}$$

By taking the inverse Laplace transform of (7), the output voltage in the time domain is obtained as:

$$v_{out}(t) = v_{out}(0) + \left(v_{Thev}(t) - \left(\frac{R_{Thev}}{R} + 1\right)v_{out}(0)\right)u(t) * h(t) + LCv_{out}'(0)h(t) \quad (8)$$

where $h(t)$ is the inverse Laplace transform of the transfer function, $H(s)$, which represents the transient impulse response of the circuit model in Figure 11.

The expression of the impulse response is solved as:

$$h(t) = \begin{cases} \frac{1}{LC\sqrt{\alpha^2 - \omega^2}} e^{-\alpha t} \sinh\left(\sqrt{\alpha^2 - \omega^2}\, t\right) u(t), (\alpha > \omega) \\ \frac{1}{LC\sqrt{\omega^2 - \alpha^2}} e^{-\alpha t} \sin\left(\sqrt{\omega^2 - \alpha^2}\, t\right) u(t), (\omega > \alpha) \end{cases}$$
$$\omega = \sqrt{\frac{1}{LC}\left(1 + \frac{R_{Thev}}{R}\right)} \quad (9)$$
$$\alpha = \frac{1}{2}\left(\frac{R_{Thev}}{L} + \frac{1}{RC}\right)$$

The initial conditions, $v_{out}(0)$ and $v_{out}'(0)$ for a triode region are the value and slope of the output voltage at the end of the previous saturation region. Also, the initial conditions for a saturation region can be obtained from the output voltage at the triode region in the previous opposite transition. As a result, the output voltage of the buffer for both pull-up and pull-down transitions can be calculated directly in the time domain using equations (8), (9), and Table 2.

Table 2. Equivalent Thevenin voltage and impedance

		$v_{Thev}(t)$	R_{Thev}
Pull-down	saturation region	$-\frac{G_{mn}V_{DD}}{\lambda_n}+\frac{g_{mn}}{\lambda_n}\left(\Delta v_{SS}(t)-\Delta v_{in}(t)\right)+\Delta v_{SS}(t)$	$\frac{1}{\lambda_n}$
	triode region	$\Delta v_{SS}(t)$	r_{onn}
Pull-up	saturation region	$\frac{G_{mp}V_{DD}}{\lambda_p}+\frac{g_{mp}}{\lambda_p}\left(\Delta v_{DD}(t)-\Delta v_{in}(t)\right)+V_{DD}+\Delta v_{DD}(t)$	$\frac{1}{\lambda_p}$
	triode region	$V_{DD}+\Delta v_{DD}(t)$	r_{onp}

The output voltage of a buffer driving only a capacitor load can also be calculated in the same way. In this case, the differential equation is given in the first order, and the output voltage is obtained as:

$$v_{out}(t)=v_{out}(0)+\left(v_{Thev}(t)-v_{out}(0)\right)u(t)*h(t) \quad (10)$$

Where:

$$h(t)=\frac{1}{R_{Thev}C}\exp\left(-\frac{1}{R_{Thev}C}t\right) \quad (11)$$

Also, for the analysis of the initial stage buffer, the input fluctuation of a buffer gate would not exist, and the v_{in}(t) is just removed in the Thevenin voltage sources of Table 2.

The calculation of the output voltage with power and ground fluctuations using (8)-(11) is much easier in practical use than the equations in the previous works [4]-[8].

2.2.2 Procedure to get Multi-stage Buffer output from the Single-stage Buffer Expressions

When a buffer in the multi-stage buffers makes a transition, the gate input of the next stage buffer behaves as a capacitor load. Therefore the multi-stage buffers can be regarded as separated single-stage buffers with appropriate load capacitances, as shown in Figure 12.

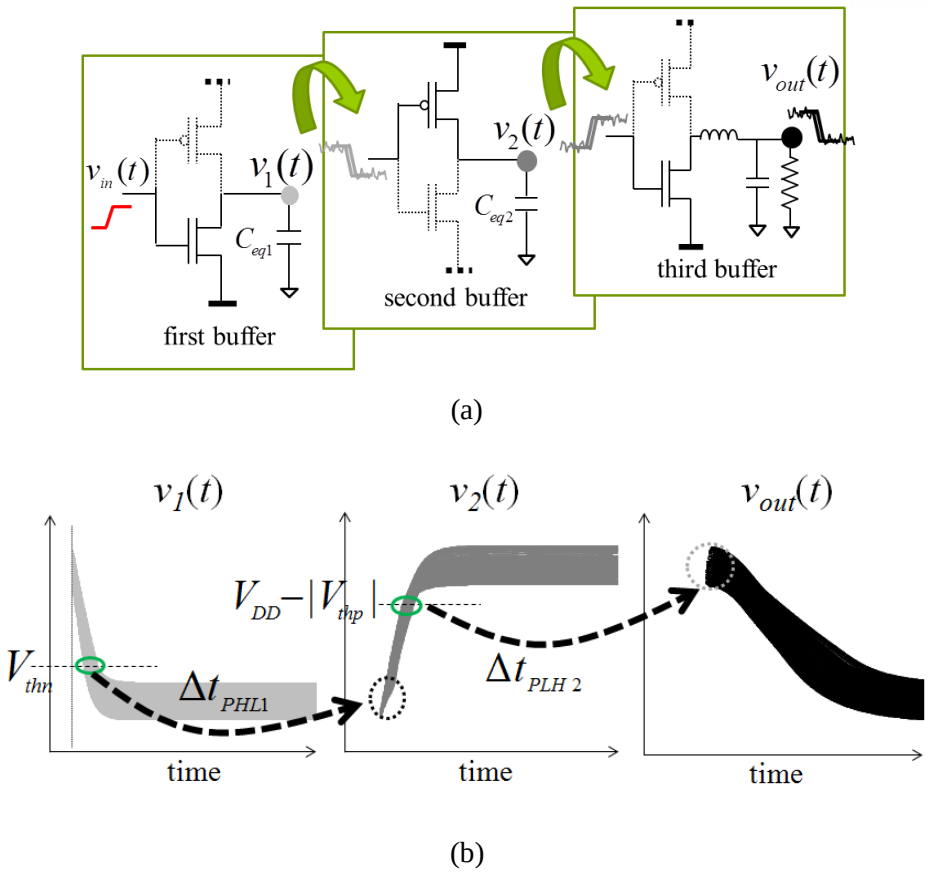


Figure 12. (a) The procedure to calculate the output voltage of three-stage buffers (b) output voltages of each stage considering the delay variation.

As an example, the procedure to calculate the output of three-stage buffers is described, when the first input voltage rises. With arbitrary supply voltage fluctuations, the output waveforms of the first buffer, v_1(t), are calculated with equivalent loading capacitance, C_{eq1}, according to the switching time of the input voltage. As the gate input voltage of the first buffer rises, the output transition starts after the first buffer PMOS is turned off. The output waveforms of the second buffer, v_2(t), are also calculated with equivalent loading capacitance, C_{eq2}, with the gate input voltage as v_1(t). The delay variation from the first buffer output, Δt_{pLH1}, is the time for the second buffer output to start the pull-up transition, which is obtained from the crossing point of v_1(t) at the threshold voltage of the second stage NMOS, V_{thn}. Similarly, the delay variation from the second buffer output, Δt_{pLH2}, is the time for the third buffer output to start the pull-down transition. It is approximately obtained from the crossing point between v_2(t) and V_{DD} minus the threshold voltage of the third buffer PMOS, $|V_{thp}|$, since the PMOS has to be turned off in the pull-down transition.

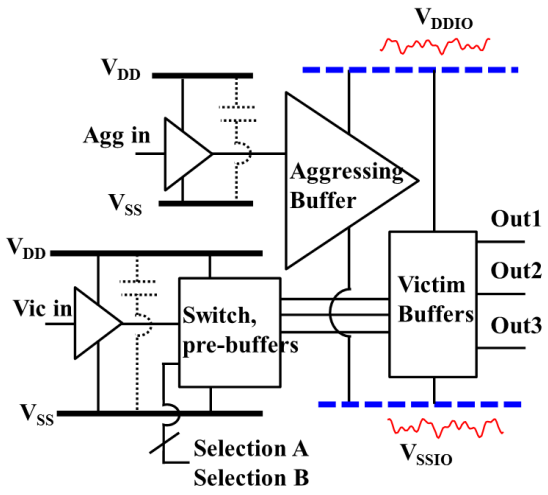
Conversely, when the falling voltage is applied to the first stage input, the delay variations for turning off the opposite MOSFETs are considered. Consequently, the output voltage waveforms for the three-stage buffers, $v_{out}(t)$, are calculated using three separated single-stage buffers.

2.3 Experimental Setup and Results

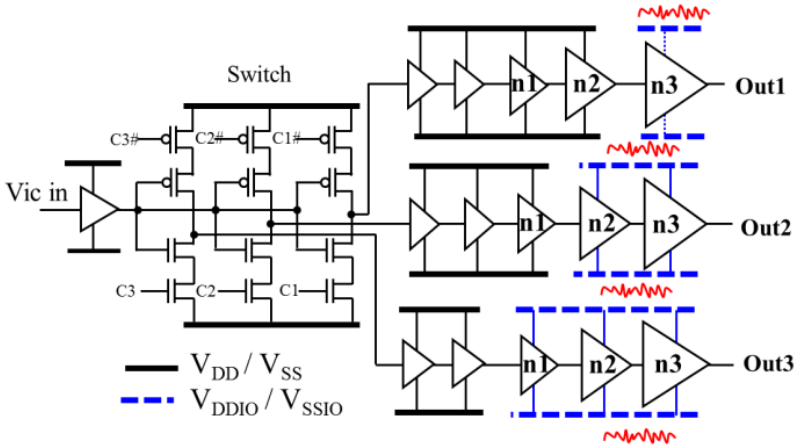
A silicon IC has been designed and fabricated using a 0.11um CMOS process to validate the proposed methodology in Section 2.2. The experimental setup for the designed printed circuit board (PCB) assembled with IC is described and various measurement results are shown in this section.

2.3.1 Design of IC

The designed IC is composed of victim buffers and aggressing buffer, as depicted in Figure 13(a). The supply voltage fluctuations on the victim buffers are generated by the large switching current of the large-sized aggressing buffer. Whenever the aggressing buffer switches, shoot-through current is generated on the path between power and ground for a short period of time. As shown in Figure 13(b), two separated power-ground nets were used in the IC. The power and ground nets (V_{DDIO}-V_{SSIO}) are connected to the aggressing buffer and victim buffers. There are three outputs (Out1, Out2, Out3) from the victim buffers. All the output paths are designed to have the same number of buffers in series to maintain the same fan-out and overall delay. The only difference between each output is the number of buffer stages connected to the fluctuating supply voltages V_{DDIO} and V_{SSIO}. The other power-ground nets (V_{DD}-V_{SS}) are separated from the aggressing buffer to avoid voltage fluctuations and used to drive the pre-buffers, except for the buffers connected to the fluctuating supply voltages. Active MOSFET capacitors were inserted between V_{DD} and V_{SS} as an on-chip decoupling capacitor for minimizing voltage fluctuation on the nets.



(a)



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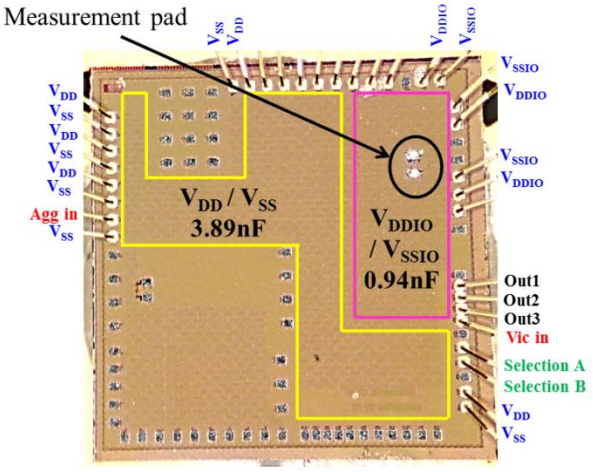
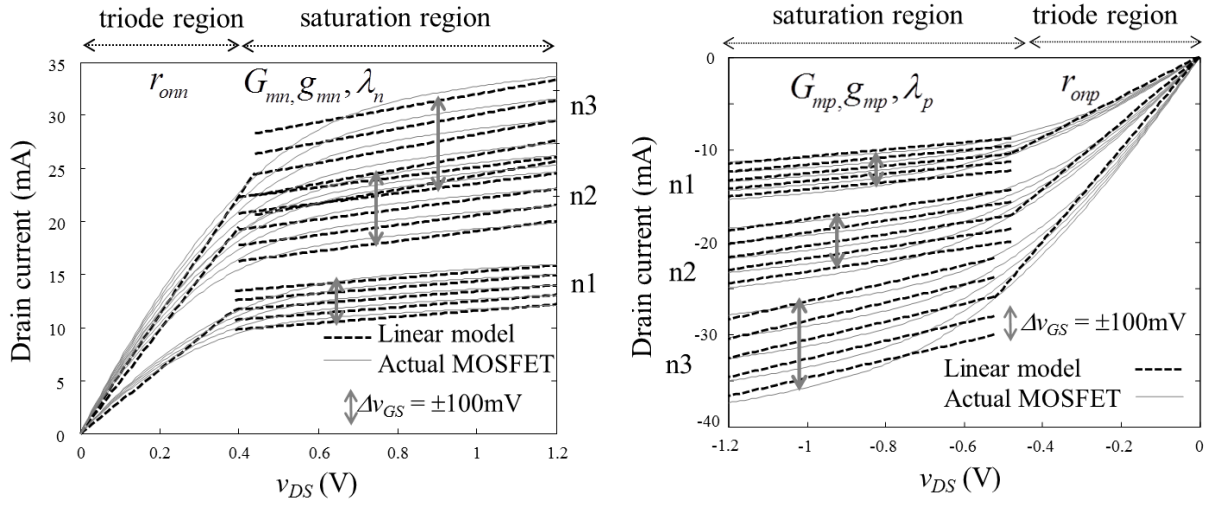


(c)

Figure 13. (a) The schematic of IC (b) designed victim buffers with pre-buffers (c) layout of IC including the measurement pads

As the output delay variations at the pre-buffers should be negligible compared to those at the buffers connected to the fluctuating supply voltage, the output voltage waveforms measured from 'Out1', 'Out2', and 'Out3' can be compared with the calculated results for the single- , two-, and three-stage buffers, respectively. The layout of the designed IC is illustrated in Figure 13(c) including a pair of pads to measure voltage between V_{DDIO} and V_{SSIO}.

Controlling the 2-bit binary selection inputs 'Selection A' and 'Selection B', the switch control signals 'C1', 'C2', and 'C3' choose one of the paths between the victim input signal and the multiple outputs. The final three stages of the victim buffers are named n1, n2, and n3. The I-V curves of MOSFETs for the three stages, n1, n2, and n3, are obtained from the post-layout SPICE simulations and piecewise linearly modeled, as shown in Figure 14. The values of the modeling parameters, G_m, g_m, λ, and r_{on}, are extracted from a numerical algorithm using the method of least-squares for minimizing the error between the linear model and the actual MOSFET curves. The obtained parameters are summarized in Table 3.



(a) (b)

Figure 14. Linearly approximated I-V curves of (a) NMOS and (b) PMOS for the victim buffers.

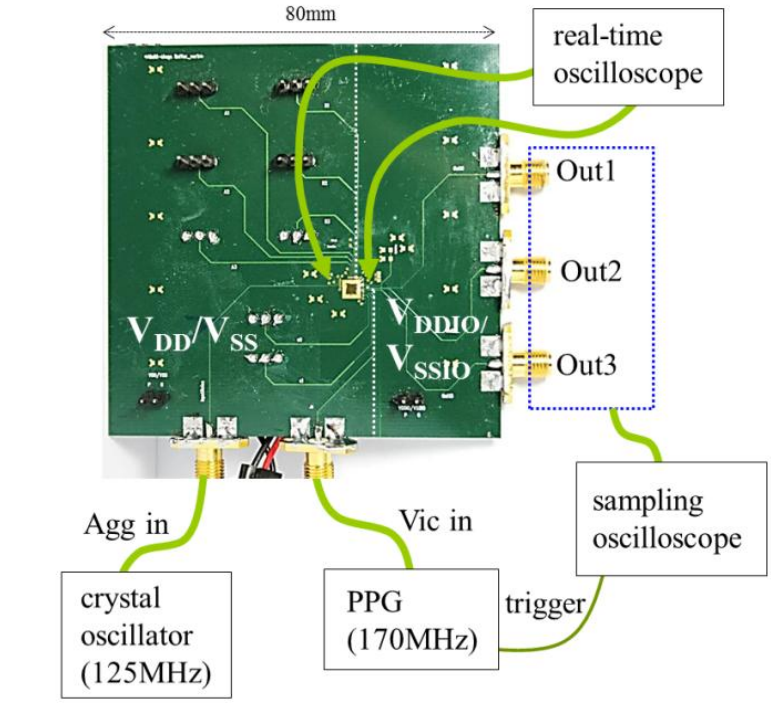
Table 3. Modeling Parameters of MOSFETs

		G_m	g_m	λ	r_{on}
n1	NMOS	8.8mS	18.3mS	2.9mS	33.47Ω
	PMOS	7.2mS	17.5mS	3.9mS	45.71Ω
n2	NMOS	14.5mS	30.1mS	4.8mS	20.54Ω
	PMOS	11.8mS	28.5mS	6.3mS	27.96Ω
n3	NMOS	17.9mS	38.4mS	6.7mS	17.88Ω
	PMOS	17.3mS	41.6mS	9.9mS	19.97Ω

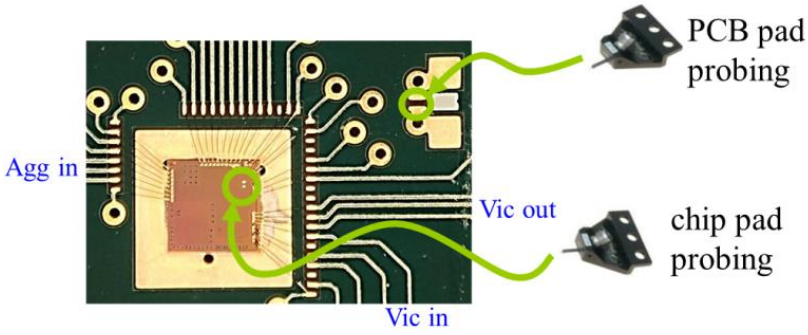
To calculate the outputs of two- and three-stage buffers and compare with the measured waveforms from Out2 and Out3, the equivalent capacitance for each stage is extracted using the SPICE simulation. In the same way as the previous work [8], the equivalent loading capacitances seen at the outputs of stages ‘n1’ and ‘n2’ are obtained as 0.49pF and 0.8pF, respectively.

A PCB is also designed, manufactured, and assembled with the fabricated IC. The assembled PCB and the experimental setup are shown in Figure 15. The IC is directly wire-bonded to the PCB to simplify the interconnection. The power and ground nets of the pre-buffers (V_{DD}-V_{SS}) are separated from those of the aggressing and victim buffers (V_{DDIO}-V_{SSIO}) also in the PCB. The victim buffers are excited by the pulse pattern generator (PPG) to guarantee sufficiently fast rising and falling time and an exact frequency of 170MHz. To avoid synchronization between the input clocks of the victim buffer and aggressing buffer, the clock of the aggressing buffer is supplied using an external clock buffer excited by a crystal oscillator with a frequency of 125MHz. The main frequency of supply voltage fluctuations would be twice the frequency of the oscillator used for the aggressing buffer, because the switching currents are generated both in the rising and falling edges of the input clock.

To measure the voltage between V_{DDIO} and V_{SSIO} on the PCB, a pair of pads is also printed on the PCB as shown in Figure 15(b). The voltages from the chip and PCB probing pads are measured simultaneously using a real-time oscilloscope. Also, the waveforms and jitter histograms of the victim buffer outputs, which are excited by the PPG, are measured from Out1, Out2, and Out3 using a sampling oscilloscope.



(a)



(b)

Figure 15. (a) The experimental setup and (b) measurements at the chip and PCB probing pads

2.3.2 Extraction of Supply Voltage Fluctuations from the Measurement Results

The supply voltage fluctuations on the victim buffer can be extracted from the measured voltage at the chip and PCB pads. The circuit model for the overall PDN of IC connected to the PCB through bonding wires is depicted in Figure 16. The reference of the receiving load at the victim buffer output is set as the zero potential in the derivation of Section 2.2. As the victim output channel from the PCB to the oscilloscope consists of microstrip lines and coaxial cables, the PCB ground can be considered as the zero potential, which is the same as the reference of the receiving load. Thus the on-chip power and the on-chip ground voltages at the victim buffer

should be treated separately with regard to the PCB ground, as denoted as V_{DDIO1} and V_{SSIO1}. When the measured voltages at the chip and PCB pads are expressed as V_{chip} and V_{PCB}, respectively, they can be expressed with the node voltages with reference to the zero potential as:

$$V_{chip} = V_{DDIO1} - V_{SSIO1} \qquad (12)$$

$$V_{PCB} = V_{DDIO0} - 0 \qquad (13)$$

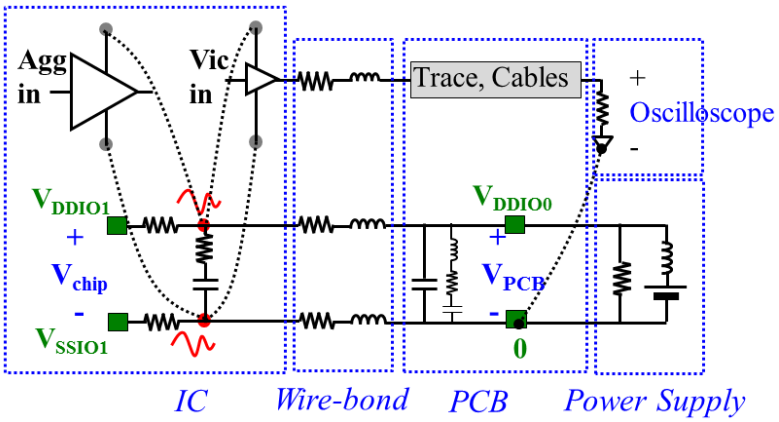


Figure 16. Overall equivalent circuits for the PDN and output channel

Since the power net in the IC and wire-bonding were designed to be symmetrical to the ground net, the voltage drops between the IC and PCB at the power and ground nets should be approximately opposite:

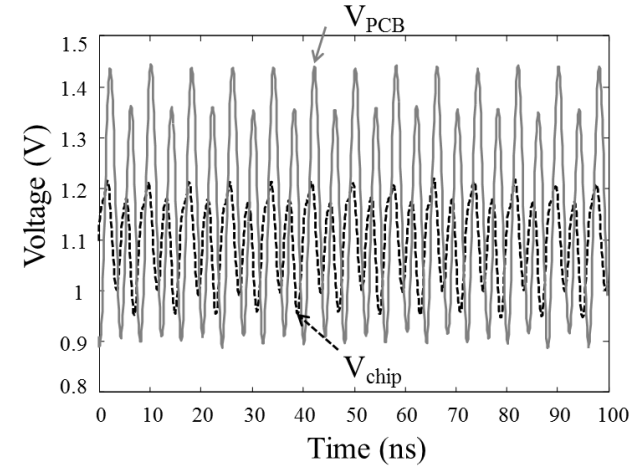
$$V_{DDIO1} - V_{DDIO0} = 0 - V_{SSIO1} \qquad (14)$$

Solving equations (12)-(14), the on-chip power and ground voltages with regard to the PCB ground can be obtained as:

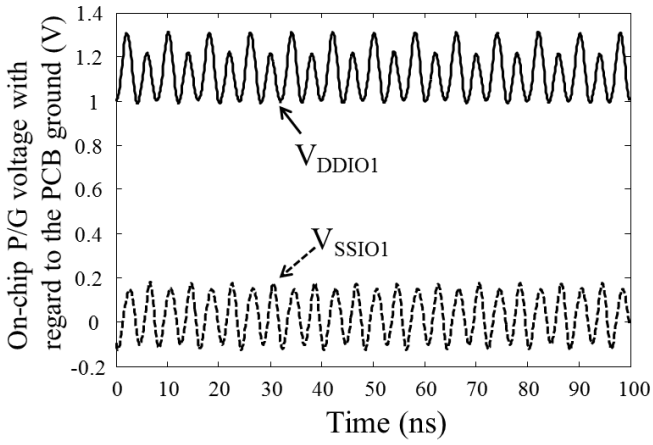
$$V_{DDIO1} = (V_{PCB} + V_{chip})/2 \qquad (15)$$

$$V_{SSIO1} = (V_{PCB} - V_{chip})/2 \qquad (16)$$

Figure 17(a) shows the measured voltages at the chip and PCB pads, and the on-chip power and ground voltages are extracted using equations (15), (16) and plotted in Figure 17(b). It is noticeable that the voltage fluctuation in the PCB pad is larger than that in the chip pad.



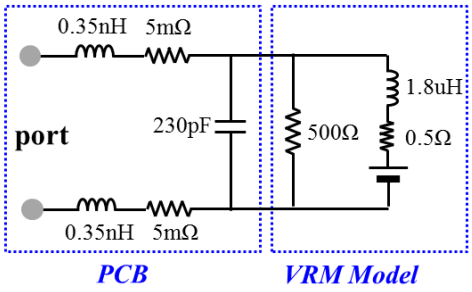
(a)



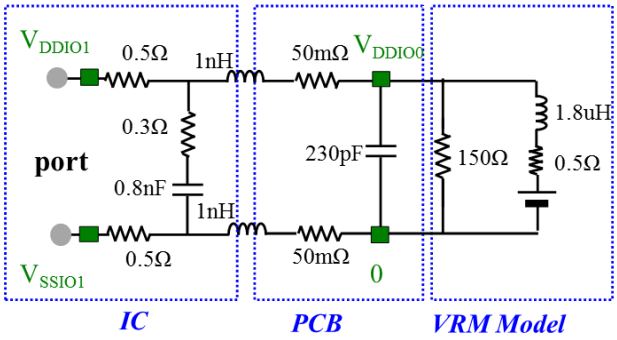
(b)

Figure 17. (a) Measured voltage waveforms on the chip and PCB pads (b) extracted on-chip power and ground voltages

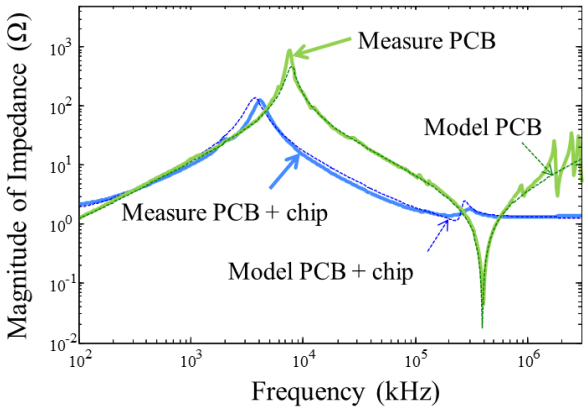
The extracted on-chip supply voltage fluctuations are validated by simulation using equivalent PDN circuit models. Using the vector network analyzer (VNA), the PDN impedance of the PCB without IC was measured at the PCB pad, and the total PDN impedance with IC assembled was also measured at the chip pad. Considering the structure of PDN and measured impedances, the elements and values in the circuit model are determined. The models for the PCB PDN and the total PDN are obtained as shown in Figure 18(a) and (b), respectively. The impedances simulated using the PDN models agree quite well with the measured impedances, as shown in Figure 18(c).



(a)



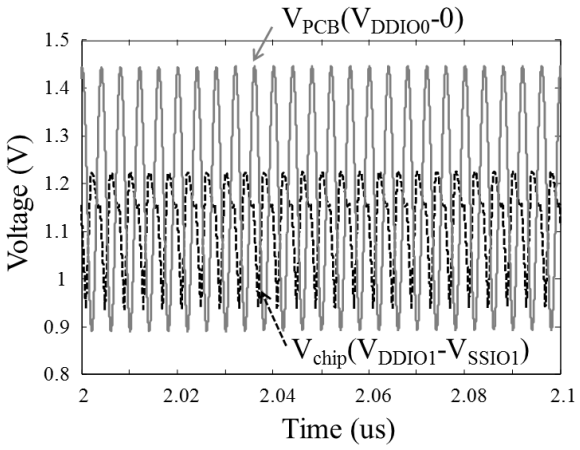
(b)



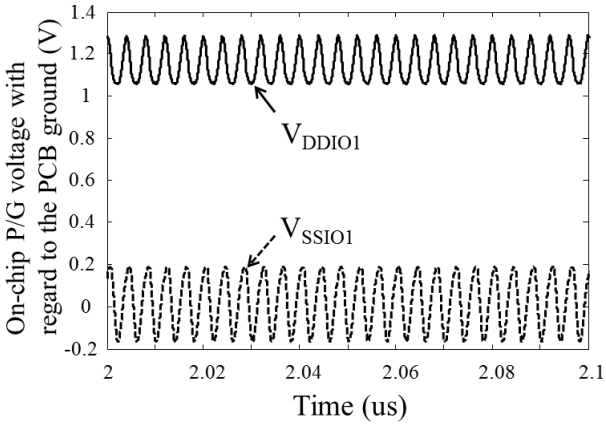
(c)

Figure 18. The PDN model (a) at the PCB pad without IC and (b) at the chip pad assembled with IC (c) impedance results from measurement and model

When the periodic triangular impulse current with magnitude of 180mA and frequency of 250MHz is applied to the port of the PDN model in Figure 18(b), the fluctuating power and ground voltage waveforms are obtained from SPICE simulation, as shown in Figure 19. The simulated results and experimental results in Figure 17 are quite similar.



(a)

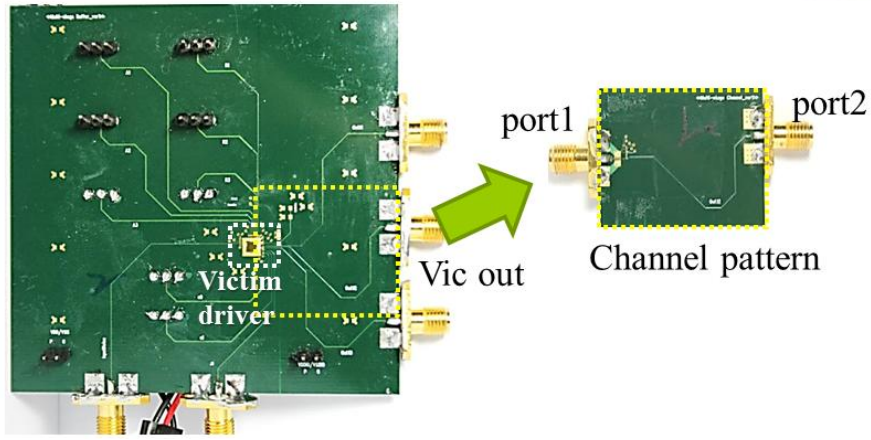


(b)

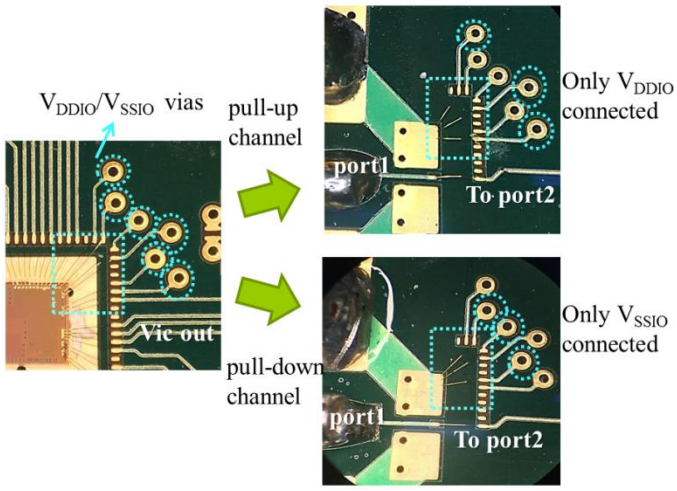
Figure 19. The simulated voltage waveforms (a) at the chip and PCB pads and (b) at on-chip power and ground nodes

2.3.3 Modeling of Output Channel

All the channels connecting from the victim driver in the IC to the oscilloscope can be characterized by measuring the designed PCB channel pattern as shown in Figure 20(a). When the victim driver is replaced by port1, the designed channel pattern replicates the output trace of the victim output and V_{DDIO}/V_{SSIO} nets in the original PCB.



(a)



(b)

Figure 20. (a) Desgiend channel pattern (b) wire-bond connections in the pull-up and pull-down channel patterns

As the PCB assembled with IC has separated power and ground layers, the output signals from the IC at pull-up and pull-down transitions would have different return paths through the power and ground planes on PCB, respectively. To measure the characteristics of the output channel at each pull-up and pull-down transition, two kinds of channel patterns were designed, as shown in Figure 20(b). In the pull-down channel, only V_{SSIO} vias are connected to the reference of port1 through the wire-bonds. Conversely, the wire-bonds between the port1 reference and the V_{DDIO} vias construct the return path in the pull-up channel.

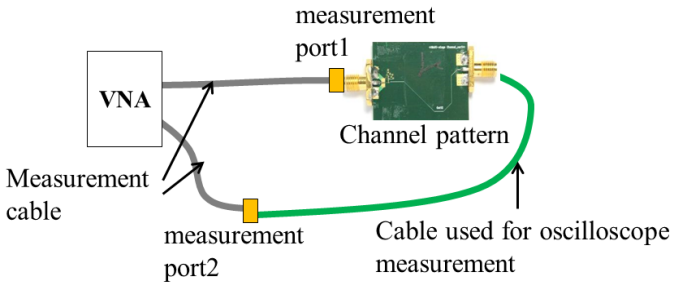


Figure 21. Measurement setup for output channel of the victim driver

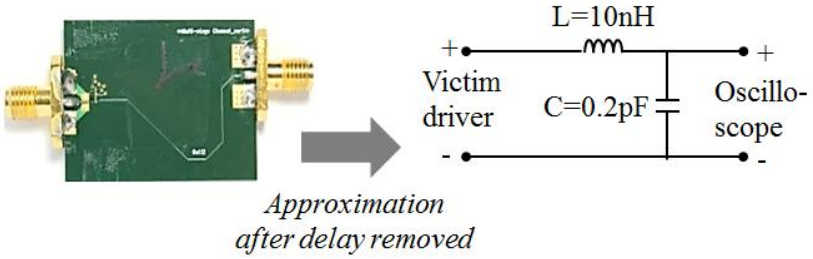
When measuring the output channel from the victim driver to the oscilloscope, not only the channel patterns but also the cable used in the oscilloscope measurement should be included, as shown in Figure 21. The characteristics of output channels both in pull-up and pull-down transitions were individually measured as two-port S-parameters with the two pull-up and pull-down channel patterns using the VNA. The analysis method in this paper can consider only the off-chip load consisting of lumped circuit elements. Thus, the measured S21 parameter of the channel should be approximated to an equivalent lumped circuit model as the off-chip load for the victim buffer. The propagation delay between measurement ports can be separately calculated and enforced [9]. The minimum phase of the S-parameter after the delay removal is related with its magnitude by the Hilbert Transform as:

$$\angle S_{\min}(f) = -\frac{1}{\pi}\int_{-\infty}^{+\infty}\frac{\ln|S(f)|}{f-f'}df' \qquad (17)$$

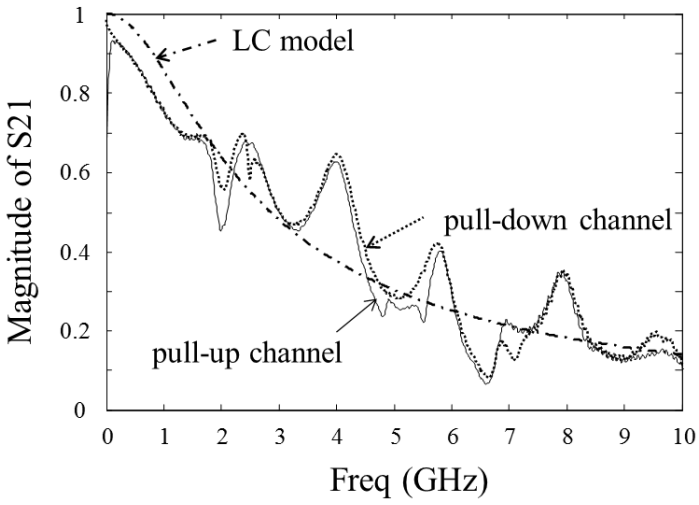
The propagation delay between measurement ports can then be extracted as:

$$T_d(f) = -\frac{\angle S(f) - \angle S_{\min}(f)}{2\pi f} \qquad (18)$$

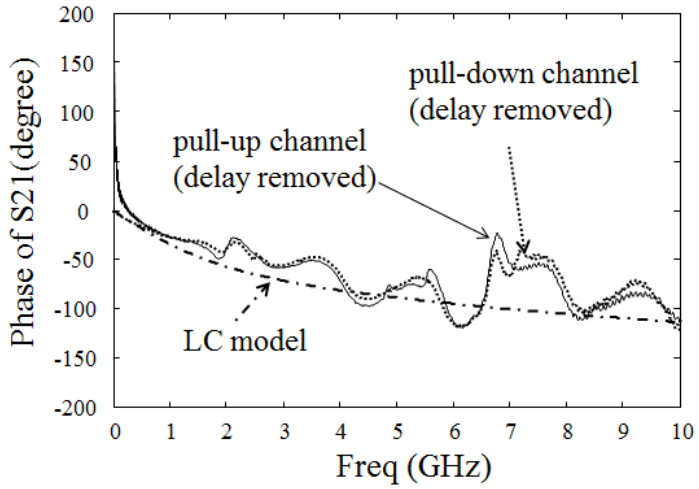
The delays extracted from the measured S21 parameters of the pull-up and pull-down channel patterns are approximately 6.4ns regardless of frequency.



(a)



(b)



(c)

Figure 22. (a) Approximation of the output channel to a circuit model, and comparison of (b) magnitudes and (c) phases

After removing the propagation delay from the S21 phase, the magnitude and phase of the S21 parameter are approximated to a lumped circuit model with 10nH inductance and 0.2pF capacitance, as shown in Figure 22. The wirebonds, microstrip line on the PCB, and the measurement cable may cause significant inductances. Including the termination resistor inside of the oscilloscope, the off-chip load for the final stage buffer is built as a 10nH series inductance and a 0.2pF capacitance in parallel with a 50Ohm resistor.

2.4 Validation with Measurement Results

Using equations (8)-(11) and Tables 2 and 3, the step responses for each single-stage buffer are firstly calculated with the on-chip supply voltage fluctuation waveforms in Figure 17(b). While changing the switching time of the first-stage input with regard to the fluctuating supply voltages, the step responses of the victim buffer are piled up as 'Multiple step responses' in Figure 23. However, since the multiple step responses do not provide sufficient information on how often the transitions arise, they should be converted into PDFs.

At every time step after the initial switching to first-stage input, the variations in the multiple step responses according to the initial switching time can be calculated. The initial switching input can occur at any arbitrary time with regard to the supply and ground fluctuations, and the channel response due to the power supply fluctuations is also a function of the input switching time. Mathematically, when a random variable Y is given as a function of a random variable X, the PDF of Y, $f_Y(y)$, can be calculated from the PDF of X, $f_X(x)$, as [7]

$$f_Y(y) = \frac{f_X(x_1)}{\left|dy/dx\right|_{x=x_1}} + \frac{f_X(x_2)}{\left|dy/dx\right|_{x=x_2}} + \ldots + \frac{f_X(x_k)}{\left|dy/dx\right|_{x=x_k}} \quad (19)$$

where x_1, x_2, …, and x_k represent the value of X when the random variable Y has the value of y.

Then, the value of the output fluctuation voltage is swept increasing y from the smallest to the largest, while finding the corresponding input switching time, x_1, x_2, …, and x_k, for the value of y. The derivative of y at each value of x_k is also calculated. Assuming a uniform PDF of the buffer switching event, $f_X(x)$, the PDFs of the output fluctuations, $f_Y(y)$, can be numerically computed using (19).

After calculating the PDF of step responses due to the supply voltage fluctuations, the Gaussian jitter PDF is convolved with the supply-induced PDF to include the random noise effect. The standard deviation of the Gaussian jitter PDF used in the convolution is 3ps, which is the measured standard deviation of the jitter with the aggressing buffer turned off.

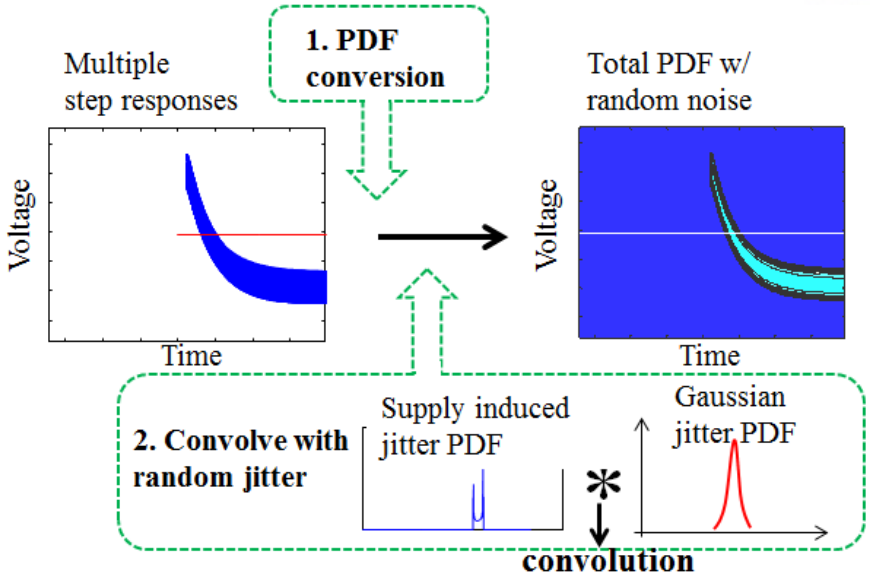


Figure 23. Procedures to calculate the total PDF including supply fluctuations and random noise

After convolving with the Gaussian jitter PDF, the total PDFs for the victim buffer at 'Out1' are plotted in Figure 24(a). The jitter PDF at 0.384V is obtained and compared with the measured jitter histogram. The values of the deterministic jitter (DJ) are also approximately obtained from the time interval between the two peaks in the jitter histogram, as the tails of the histograms should correspond to the random jitter. The PDFs and jitters for the victim outputs at 'Out2' and 'Out3' are also calculated and plotted in Figure 24(b) and (c), respectively. The measured output waveforms and jitter histograms at 0.384V from the designed IC assembled with PCB are plotted in Figure 25.

Both in calculation and measurement results, the deterministic jitter for 'Out2' is smaller than those for 'Out1' and 'Out3'. That is, the jitter decreases when the number of buffer stages that are connected to the fluctuating supply voltages is two. The reason can be explained. Consider the falling input into the first stage. If the power voltage level is increased, the rising time of the first stage output decreases due to the increased gate-source voltage of the first stage PMOS. However, the falling output of the second stage should start from the higher initial voltage due to the increased power level, which makes a longer falling time in the second stage output. Thus, the fast rise time of the first stage output would compensate the longer falling time of the second stage, which results in less change in the total transition time of the buffer output at 'Out2'. As a result, some of the jitter is canceled by the even number of buffer stages. If the number of buffer stages that are connected to the fluctuating supply voltages is odd, such as one or three, the jitter from one of the stages is not cancelled.

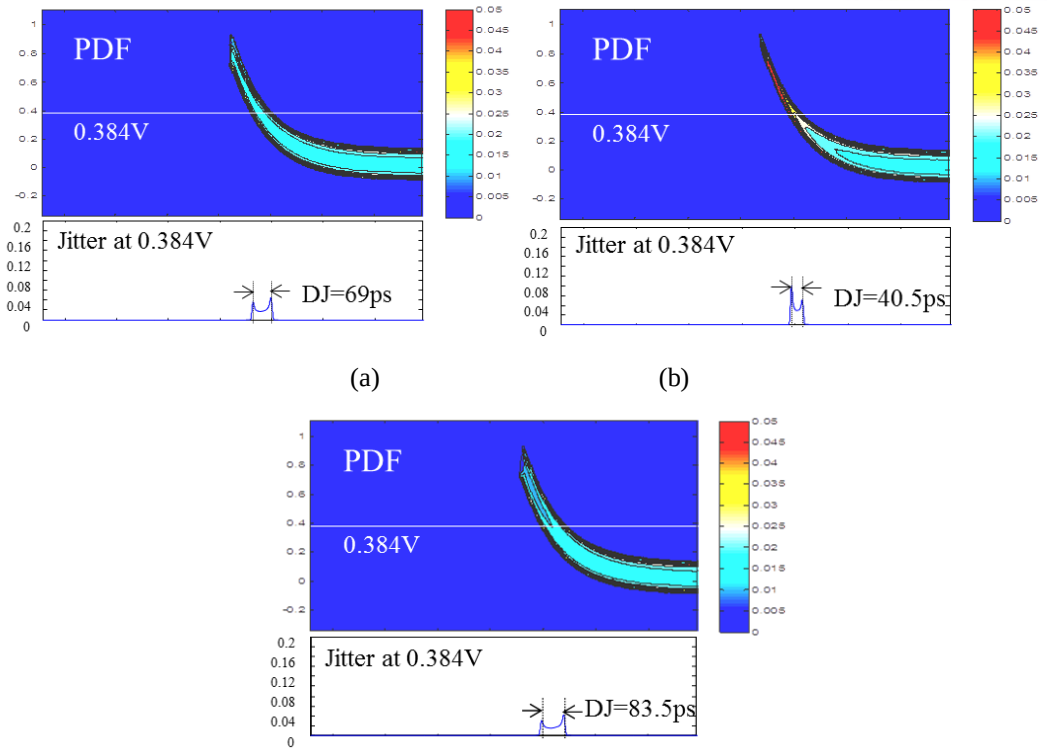


Figure 24. PDFs and jitter at 0.384 from (a) Out1 (b) Out2 (c) Out3

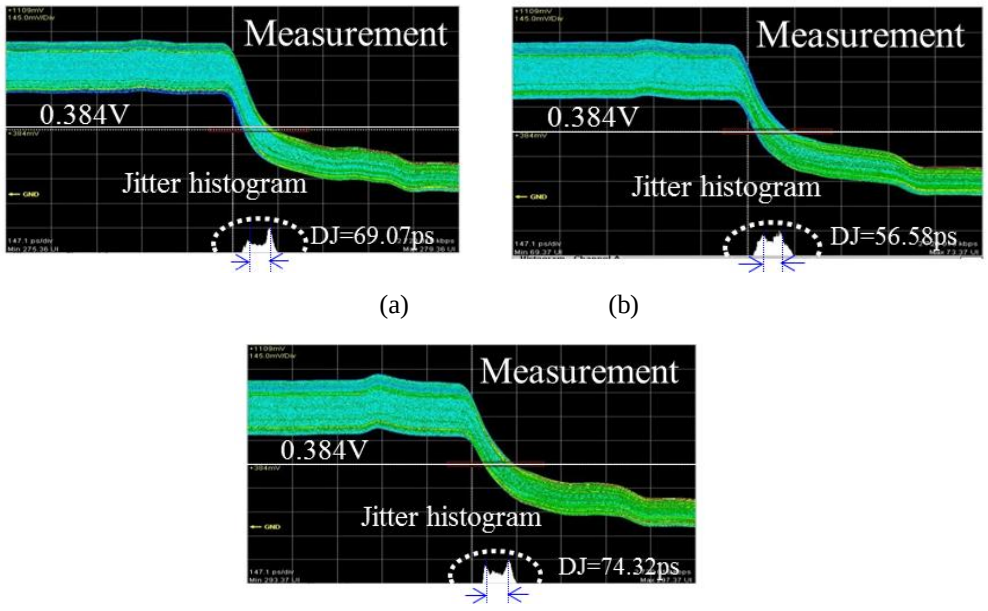


Figure 25. Measured output voltage waveforms and jitter histogram from (a) Out1 (b) Out2 and (c) Out3

III. Propose Method to calculate PSIJ at Si-interposer Channel including ESD Protection Circuit

Electrostatic discharge (ESD) is one of the main reliability issues in IC manufacturing. On-chip ESD protection design is commonly employed near the I/O pins to alleviate the impact of ESD events [10]. However, the ESD protection structures induce parasitic junction capacitance (C_{ESD}) and parasitic resistance (R_{ESD}) causing parasitic effects such as RC delay, noise coupling through ESD parasitic capacitance and self-generated noise [11]. Especially, the supply voltage fluctuations which are caused by the switching current of logic circuit and I/O buffer can couple through ESD parasitic capacitance on the output of an IC. The noise propagation through the ESD protection circuits degrades the signal integrity of high speed I/O interface and even can reduce the voltage and timing margin of the I/O link. In the previous works, the expressions of the output voltages and the PDF of the step responses were calculated on the assumption that the supply voltage fluctuations are only propagated through MOSFETs of the buffer. In this paper, the transfer function of the 3-D IC channel including the ESD protection circuits is calculated. The output jitter induced by propagation of the supply voltage fluctuations ($v_{DDIO}(t)$, $v_{SSIO}(t)$) through the parasitics of ESD protection circuits is then calculated and included to get the precise output jitter PDFs, as shown in Figure 26. In addition, the relation between the frequency of the supply voltage fluctuations and the output jitter induced by ESD protection parasitic is estimated from the calculated transfer function, and investigated by comparing the output PDFs.

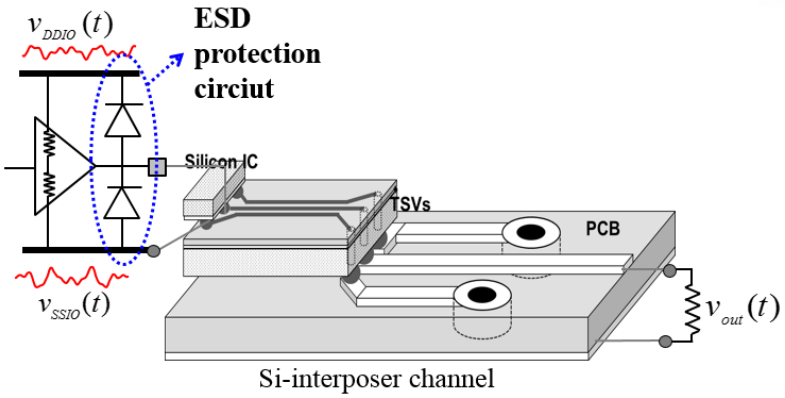


Figure 26. A linear output driver with ESD protecion circuits and a Si-interposer channel

3.1 Derivation of the step response at a Si-interposer Channel including ESD Protection Circuit

3.1.1 Equivalent Circuit including ESD Protection Parasitic

In the Si interposer channel, the IC is flipped down and the pads are directly connected to the interposer by micro-bumps, and the interposer is then connected to the PCB with through–silicon-vias (TSVs). The characteristics of the signal transmission from a silicon IC to an off-chip trace on PCB were simulated using a full-wave electromagnetic tool in a previous paper [12]. The simulated S-parameters of the channel can be used to calculate the transfer function from the driver of IC to a receiver at the PCB including ESD protection parasitics. The step response of the Si-interposer channel including the ESD parasitics can also be calculated.

For simplicity, the driver of an IC is assumed as a linear buffer which can be modeled as a voltage source v_{in}(t) and a source resistance R_S; the impedance of the receiver is also set as a linear resistor, R_L. The schematic of the output driver with the channel can be simplified as Figure 27, where the ESD protection circuits are modeled just as the C_{ESD} for normal operating conditions. There are three noise sources which make variation on the output voltage, v_{out}(t). The transfer function relating each noise sources to the output voltage can be seperately treated using Superposition theorem. The transfer function H_1(f) represents the relation between input voltage and output voltage in the frequency domain; the H_2(f) relates the power or ground voltage fluctuations to the output voltage. Using the transfer functions, the output

variations caused by the input voltage and the supply voltage fluctuations can also be calculated in the time domain.

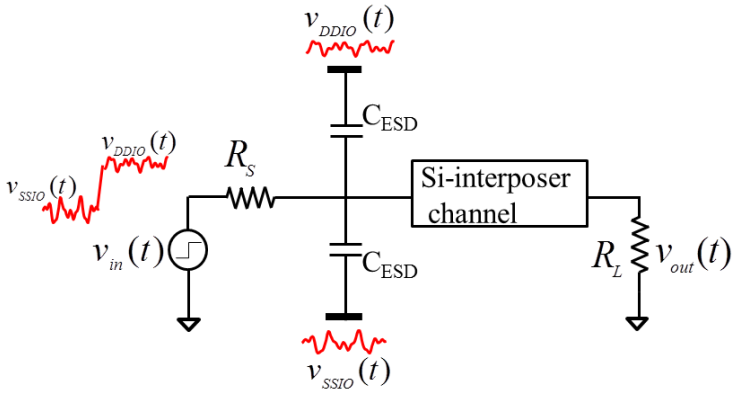
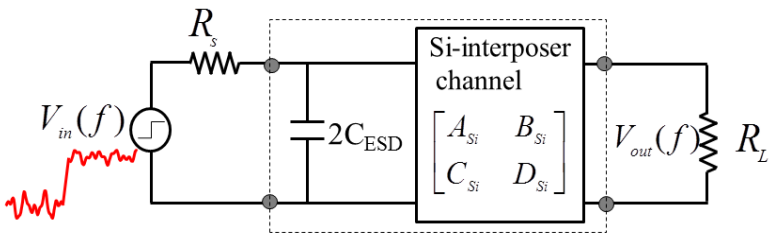
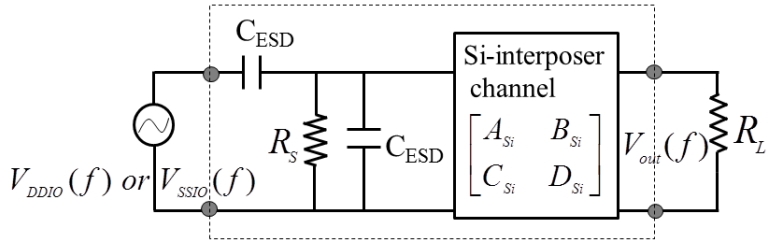


Figure 27. Simplified schematic of the output driver with Si-interposer channel including ESD protection parasitics

3.1.2 Derive Voltage Transfer Functions of the Equivalent Circuit



(a)



(b)

Figure 28. The equivalent circuits (a) from the input voltage $V_{in}(f)$ to the output voltage, $V_{out}(f)$ and (b) from the supply voltage fluctuations ($V_{DDIO}(f)$ or $V_{SSIO}(f)$) to the $V_{out}(f)$

To calculate each transfer function, the simulated S-parameters of the Si-interposer channel are firstly converted into ABCD parameters, which are denoted as A_{si} B_{si} C_{si} D_{si}. The total ABCD parameters for the two-port networks of the dotted boxes in Figure 28(a) and (b) are calculated respectively as

$$\begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 4\pi f C_{ESD} & 1 \end{bmatrix} \begin{bmatrix} A_{Si} & B_{Si} \\ C_{Si} & D_{Si} \end{bmatrix} \quad (20)$$

$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{2\pi f C_{ESD}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_S} + 2\pi f C_{ESD} & 1 \end{bmatrix} \begin{bmatrix} A_{Si} & B_{Si} \\ C_{Si} & D_{Si} \end{bmatrix} \quad (21)$$

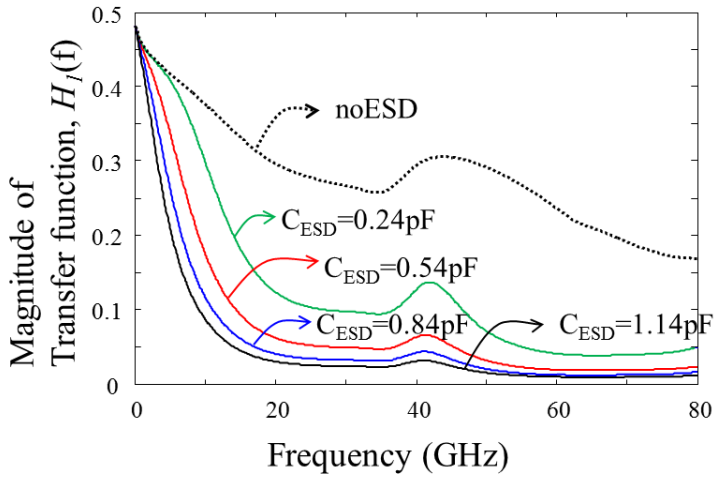
Using the total ABCD parameters (20)-(21), the transfer functions, $H_1(f)$ and $H_2(f)$ can be calculated as

$$H_1(f) = \frac{V_{out}(f)}{V_{in}(f)} = \frac{R_L}{A_1 R_L + B_1 + C_1 R_S R_L + D_1 R_S} \quad (22)$$

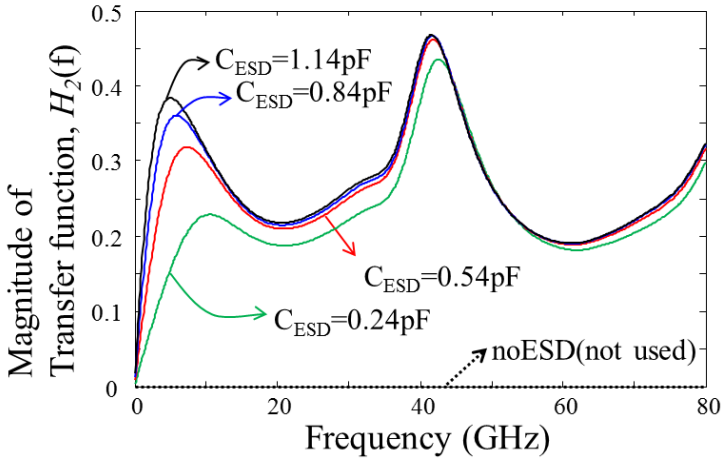
$$H_2(f) = \frac{V_{out}(f)}{V_{DDIO}(f)} = \frac{V_{out}(f)}{V_{SSIO}(f)} = \frac{R_L}{A_2 R_L + B_2} \quad (23)$$

When the value of source and receiver resistance, R_S and R_L are both given as 50 Ω, the magnitudes of the transfer functions, $H_1(f)$ and $H_2(f)$, are calculated and plotted for several values of the parasitic capacitance, C_{ESD}, in Figure 29(a) and (b), respectively. As increasing the value of C_{ESD}, the overall magnitude of $H_1(f)$ decreases but that of $H_2(f)$ increases. That means the output variations due to the supply voltage fluctuation propagated through ESD parasitic capacitance is large with the larger ESD parasitic capacitance. In addition, the magnitude of $H_2(f)$ above 4GHz is even larger than that of $H_1(f)$, which represents the noise propagated through ESD parasitic is more crucial for the IC with higher operating frequency.

Since the parasitic capacitance value of the conventional MOS ESD protection structure was approximated as 0.84pF in [11], the transfer functions $H_1(f)$ and $H_2(f)$ with 0.84pF C_{ESD} in Figure 29 have been used to obtain the step responses and output PDFs. For comparison, the transfer function without ESD parasitic is also calculated and denoted as $H_{1,noESD}(f)$. The transfer functions with ESD parasitic are represented as $H_{1,ESD}(f)$ and $H_{2,ESD}(f)$.



(a)



(b)

Figure 29. The magnitude of the transfer functions (a) H_1(f) and (b) H_2(f) with several values of ESD parasitic capacitance

The port-to-port propagation delay is extracted from the transfer functions, and separately enforced for causality in the step response calculation as the same way in [9]. The propagation delays extracted from the transfer functions, $H_{1,noESD}$(f), $H_{1,ESD}$(f) and $H_{2,ESD}$(f) are obtained as 40ps, 42ps and 39ps, respectively, which are then used to calculate the step responses.

3.1.3 Calculation of the Step response using the Transfer Functions

The impulse responses with delay removed, $h_{1,noESD}(t)$, $h_{1,ESD}(t)$ and $h_{2,ESD}(t)$ are obatined by inverse Fourier transform of the transfer function after removing the propagation delay from each transfer function. The rising step input voltage source, $v_{in}(t)$, with 60ps rise-time, T_r, along with the corresponding power and ground voltage fluctuations can be expressed as

$$v_{in}(t) = v_{DDIO}(t) \cdot \frac{t \cdot u(t) - (t - T_r) \cdot u(t - T_r)}{T_r} + v_{SSIO}(t) \cdot \left(1 - \frac{t \cdot u(t) + (t - T_r) \cdot u(t - T_r)}{T_r}\right) \quad (24)$$

The output voltage without ESD parasitics, $v_{out,noESD}(t)$, is then calculated as the convolution of the input voltage and impulse response, $h_{1,noESD}(t)$ with the delay $T_{d1,noESD}$ as

$$v_{out,noESD}(t) = v_{in}(t) * h_{1,noESD}(t - T_{d1,noESD}) \quad (25)$$

On the other hand, there are three noise sources by including ESD protection parasitics. The input voltage is convolved with the impulse response, $h_{1,ESD}(t)$, with the delay $T_{d1,ESD}$ and the power and ground voltage fluctuations are both convolved with $h_{2,ESD}(t)$ including the delay $T_{d2,ESD}$. The output voltage including ESD parasitic, $v_{out,ESD}(t)$, is calculated as the sum of the three convolution terms as

$$v_{out,ESD}(t) = v_{in}(t) * h_{1,ESD}(t - T_{d1,ESD}) + v_{DDIO}(t) * h_{2,ESD}(t - T_{d2,ESD}) + v_{SSIO}(t) * h_{2,ESD}(t - T_{d2,ESD}) \quad (26)$$

Without any power and ground voltage fluctuations, the second and third convolution terms result in zero, since the DC power and ground voltage is blocked by the ESD parasitic capacitor, as shown in Figure 28(b). The output voltages due to the rising step intput with no power and ground voltage fluctuations are plotted for the cases with and without ESD parasitic capacitance, respectively, in Figure 30. It is shown that the output rising time is significantly increased due to the ESD parasitic capacitance.

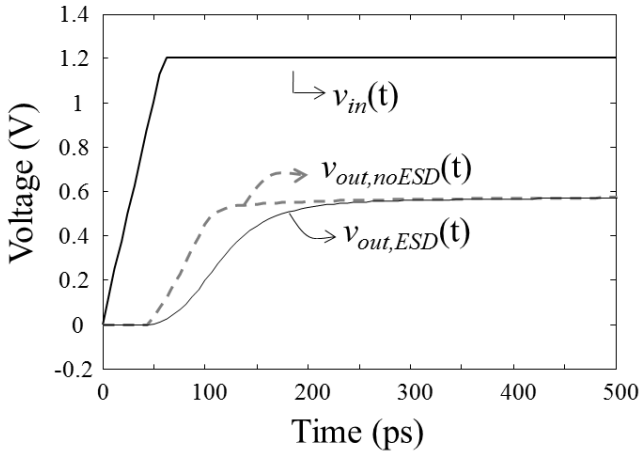


Figure 30. The calculated step responses of the Si-interposer channel with and without ESD parasitic capacitance

3.2 Calculated Probability Density Results

The step responses including supply voltage fluctuations can be obtained using the equations (25)-(26). As numerical examples, the power and ground fluctuations composed of four cosine terms were artificially made as

$$v_{DDIO}(t) = V_{DD} + 0.06\cos(2\pi f_1 t - \frac{\pi}{4}) + 0.05\cos(2\pi f_2 t + \frac{\pi}{3}) + 0.045\cos(2\pi f_3 t - \pi) + 0.04\cos(2\pi f_4 t - \frac{\pi}{5}) \quad (27)$$

$$v_{SSIO}(t) = 0.055\cos(2\pi f_1 t - \frac{\pi}{6}) + 0.045\cos(2\pi f_2 t + \frac{4\pi}{5}) + 0.04\cos(2\pi f_3 t) + 0.035\cos(2\pi f_{\backslash 4} t - \frac{3\pi}{4}) \quad (28)$$

where the V_{DD} is set as 1.2 V.

Two kinds of fluctuation voltages with different frequency components were tested. In the first case, the frequencies of the supply voltage fluctuations are set as relatively low frequencies with f_1=100MHz, f_2=200MHz, f_3=500MHz, and f_4=700MHz. In the second case, the magnitude and phase of the cosine terms are the same but the frequencies are much higher as f_1=1GHz, f_2=2GHz, f_3=5GHz and f_4=7GHz. The two kinds of power and ground voltage fluctuations with low and high frequencies are plotted together in Figure 31. As the only difference between the two kinds of

fluctuation voltages is frequency, the effect of fluctuation frequency can be directly captured. In reality, however, power and ground fluctuations are related each other, because the supply noise is predominantly generated by switching currents flowing through power and ground. Also, the on-chip supply voltage fluctuations at high frequency range above GHz is greatly reduced when a sufficient amount of on-chip decoupling capacitor are employed.

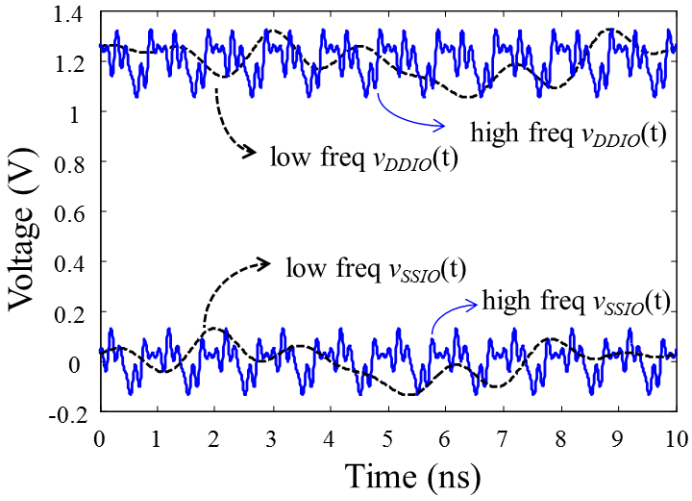
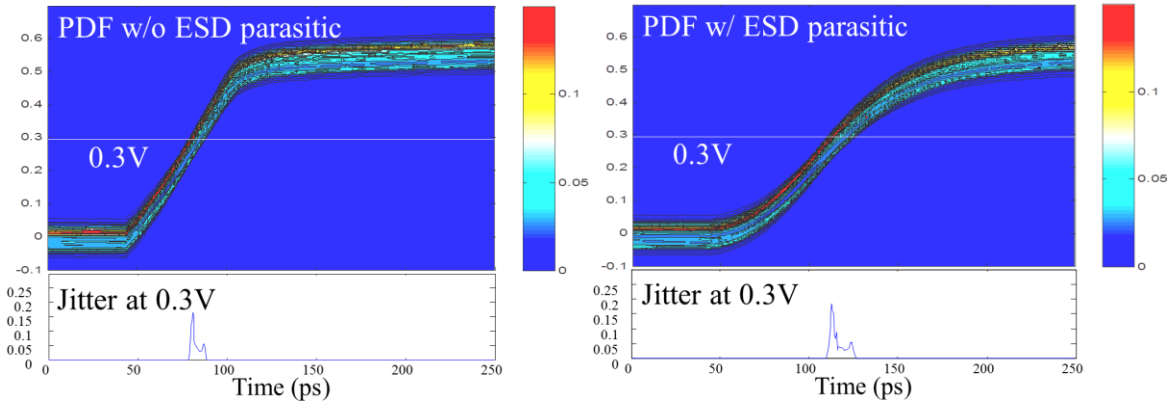


Figure 31. Two kinds of artificial supply voltage fluctuations with low and high frequency componets

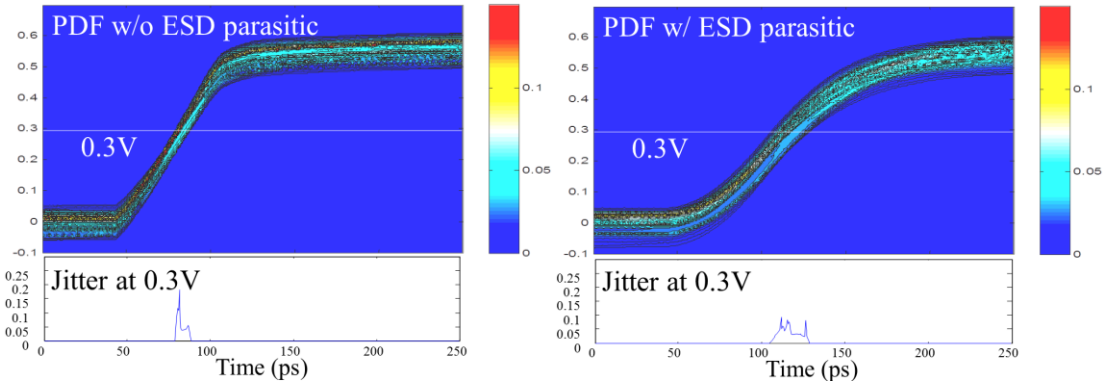
After calculating the step responses with low frequency supply voltage fluctuations, the output PDFs are calculated. Since the step pulse transition can occur at any arbitrary time with regard to the supply voltage fluctuations, the channel response with the power and ground fluctuations is also a function of the input switching time. Using the PDF conversion process of random variables, the PDF of the output voltage variation can be calculated from the output voltage variation at a fixed time and the PDF of the input switching events [7]. On the assumption that input switching PDF is uniform, the output waveform PDFs and the output jitter PDFs at 0.3V due to the low frequency supply voltage fluctuations are calculated and plotted in Figure 32. Comparing the output jitter at 0.3V for the cases with and without ESD parasticis, as shown in Figure 32(a) and (b), the shapes of jitter PDF are similar but there are a certain delay caused by the ESD parasitic capacitance. Also, the step rise time with ESD parasitic is smoother than that without ESD parasitic.



(a) (b)

Figure 32. The calculated output waveform and jitter PDFs at 0.3V due to low frequency supply voltage fluctuations (a) without ESD parasitics (b) with ESD parasitics

As the same way, the PDFs of output waveforms and jitters with high frequency supply voltage fluctuations are also obatined and plotted in Figure 33. Overall output waveforms look similar between the cases with high- and low- freqency supply voltage fluctuations. However, the output jitter PDF at 0.3V shown in Figure 33(b) is quite different from that in Figure 32(b). The width of the output jitter PDF is considerably increased in the high frequency fluctuations. The reason can be understood from the magnitude of transfer functions in Figure 29. Since the magnitude of $H_{2,ESD}(f)$ increases with freuqency up to 7GHz, the output voltage fluctuations transferred through ESD parasitics from the higher supply voltage fluctuations should be larger.



(a) (b)

Figure 33. The calculated output waveform and jitter PDFs at 0.3V due to high frequency supply voltage fluctuations (a) without ESD parasitics (b) with ESD parasitics

IV. Summary and Conclusion

In this paper, an analytical methodology to calculate the jitter PDFs at multi-stage buffers due to supply voltage fluctuations has been derived. The equations to get the output voltage waveform of a single buffer are firstly derived. With the expressions for the single buffer, output waveforms of the multi-stage buffers can be calculated including the delays extracted from each buffer stage.

For experimental validation of the proposed method, a silicon IC is designed and fabricated. The PCB is also designed and assembled with IC. On-chip power and ground voltage fluctuations are extracted from the directly measured voltages at pads on the IC and the PCB simultaneously. The extracted on-chip power and ground fluctuations are also validated from the SPICE simulation using the equivalent PDN model. Also, the off-chip channel characteristics are measured as a two-port S-parameter with specially designed PCB channel patterns. After removing the delay from the measured S-parameters, the off-chip load is approximated to a lumped circuit model. Then, the calculated output PDFs of multi-stage buffers are compared with the measured output voltage waveforms and jitter histograms. In addition, the reason why an even number of buffer stages has low deterministic jitter is explained. However, the lumped circuit model for the off-chip load is not accurate, and the calculated waveforms do not accurately capture the details of the measured output waveforms.

Also, the step response of a linear output driver with Si-interposer channel in presence of supply voltage fluctuations has been analytically derived with including the ESD protection circuits. The output voltage variations from three different noise transfer paths can be separately calculated, and superimposed to obtain the total step output responses of the channel. By comparing the jitter PDFs with and without ESD parasitics, the impact of the ESD protection circuits on the output jitter can be identified. In addition, the PDFs due to the supply voltage fluctuations at different frequency ranges are calculated and compared. The relation between the magnitudes of the transfer functions and the output jitter has been investigated. The jitter PDFs are calculated on the assumption that ESD protection parasitics can be regarded as simple capacitance. However, in I/O design, the structure of equalization network is usually employed on the output of transmitter for compensating the loss of signal in high frequency ranges. Thus, the transfer function including not only capacitance but also equalization network has to be calculated for getting more realistic results

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