Master's Thesis

Indirect Contact Probing Method for Characterizing Vertical Interconnects

Jongwoo Jeong

Department of Electrical Engineering

Graduate School of UNIST

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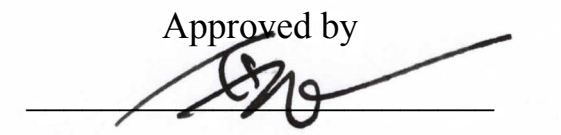
Approved by



Advisor
Ki Jin Han

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This certifies that the thesis/dissertation of Jongwoo Jeong is approved.

7. 15. 2015

signature

Advisor: Ki Jin Han

signature

Jingook Kim: Thesis Committee Member #1

signature

Youngmin Kim: Thesis Committee Member #2

Abstract

Recently, vertical interconnects in wafer-level are used to achieve system integration with stacked chips. Although the wafer-level vertical interconnects provide smaller interconnection delay and lower power consumption, popularizing the technology is difficult due to testing issues. A main difficulty in testing vertical interconnects comes from that possible damages caused by the direct-contact probing. Therefore, an indirect contact probing method is presented for safe characterization in waver level. The proposed method is based on the capacitive coupling method. Utilizing a dielectric contactor, the sensitivity of capacitive coupling can be improved with ensuring the protection of vertical interconnects. In addition, extra probe control module and sensor electronics are not required since the dielectric contactor maintains the constant gap. The proposed method is verified in both cases of a single-pair via and multiple vias.

The procedure of the proposed method for a single-pair vias starts with one-port calibration. To apply one-port calibration, we have measurements on three different calibration vias by the indirect and the direct-contact probing. From the measurement data, the characteristic of dielectric contactor is fully characterized. After the dielectric contactor is mounted on the DUT containing vertical interconnects, the DUT is measured by the indirect-contact probing manner. Finally, de-embedding the dielectric contactor portion, we can obtain the characteristic of a single-pair via. The proposed method is verified in printed circuit board (PCB) level. The extracted via impedances show a good agreement with the direct-contact probing in frequency ranges 0.8 GHz to 30 GHz and 2.5 GHz to 18 GHz by simulations and measurements, respectively.

In the case of multi-via testing, the procedure is similar to a single-pair via extraction but additional fixtures are required. By adopting the socket and calibration substrates, the dielectric contactor consisting of multiple pads can be characterized. From dielectric contactor characteristics corresponding to each via, multiple vias can be extracted based on the reference plane. The extracted impedances of multiple vias show a good agreement with the direct-contact probing up to 24 GHz by simulations and 22 GHz by measurements. From the extracted impedances, we can diagnose all defects among multiple vias. Since the proposed method for multi-via test is limited to testing, the indirect contact probing method for the multi-port characterization is also proposed. It characterizes a multi-port network of a DUT by de-embedding the multi-port characteristics of the dielectric contactor, hence we can also capture inter-via couplings from a multi-port network. Based on simulations, a two-port network is successfully characterized in the range of 0.8 GHz to 24 GHz.

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Nomenclature

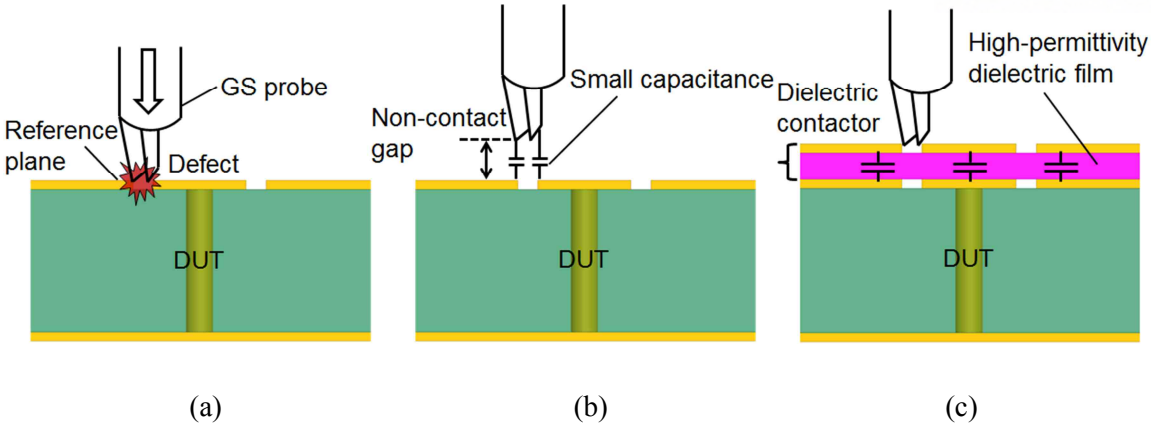
3D IC	Three-dimensional Integrated Circuit
DUT	Device Under Test
LDT	Laser-direct Technology
PCB	Printed Circuit Board
ECM	Embedded Capacitance Material
TRL	Thru Reflect Line
SOLT	Short, Open, Load and Thru

Chapter I

Introduction

Recently, vertical interconnects in wafer-level packaging are key elements for realizing 3D ICs, featured by smaller interconnection delay, lower power consumption, and heterogeneous technologies integration [1]. To achieve these benefits and reduce time-to-market, efficient test methods on vertical interconnects in early-stage are required for lower production cost. Conventionally, the direct-contact probing method is used, but vertical interconnects can be damaged by the probe tips while making suitable electrical contact as shown in Fig. 1-1(a). For this reason, non-contact probing methods have been introduced to protect vertical interconnects.

Several non-contact probing methods have been proposed, based on either the inductive [2]-[4] or the capacitive coupling method [5]-[10]. The inductive coupling method takes advantages of longer non-contact distance and more flexible design using the number of turns. However, increasing the inductive coupling for better sensitivity requires large inductor area, degrading a performance of a device under test (DUT). The capacitive coupling method in Fig. 1-1(b) provides a simple and cost effective characterization, since it is available by using pads only. However, it cannot characterize the vertical interconnects due to the dominant effect of the small capacitances in the non-contact gap between the probe tips and the via pads. Furthermore, maintaining the constant non-contact gap requires a fine vertical control module and sensor electronics [11], increasing the measurement cost. Apart from the coupling methods, the laser-direct technology (LDT) system is described in Fig. 1-2 [12]. Based on the photoelectric effect, the extracted electrical charge from the trace and the voltage gap enables the identification of the trace capacitance. After filling the capacitance database as the reference, the DUT can be tested as compared to the reference. Although the testing speed is faster, adopting the laser system is not cost-effective due to additional devices for laser control and measuring the electrical charge.



(a) (b) (c)

Fig. 1-1. Issues in the contact and the capacitive coupling methods, and the proposed indirect contact probing method: (a) defects caused by direct contact probing (b) small capacitances of non-contact probing (c) indirect contact probing

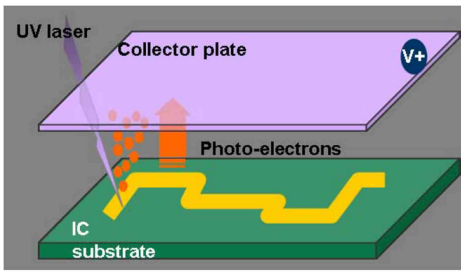


Fig. 1-2. Laser-direct technology system [12]

We present an indirect contact probing method based on the capacitive coupling method. The proposed method improves the conventional capacitive coupling method by adopting a dielectric contactor that protects vertical interconnects in the DUT as shown in Fig. 1-1(c). The high-permittivity dielectric contactor enhances the sensitivity by increasing the capacitive coupling. Furthermore, control and sensor electronics are not necessary since the non-contact gap is stably maintained by the dielectric contactor. With the aid of additional fixtures, the proposed method can extend on multi-via testing not limited to a single pair of vias. In this thesis, we discuss the procedures for characterizing a single-pair vias and testing multiple vias, including its hardware, the calibration and the measurement procedure. The proposed method is verified by both simulations and measurements in printed circuit board (PCB) level. For capturing the inter-via coupling, the feasibility of the multi-port characterization is also investigated.

The rest of this thesis is organized as follows. Section II presents the indirect contact probing method for a single-pair vias. The target is extracting the impedance of a single-pair vias as shown in Fig.1-3(a). The hardware, the procedure for extracting a single-pair vias and the calibration via design are investigated. The extracted characteristics of vias are shown based on both simulations and

measurements. The proposed method is limited to the characterization of single-pair vias, hence the proposed method extends on multi-via testing. In section III, the proposed method for multi-via test is investigated as shown in Fig.1-3(b). Additional fixtures to support multiple vias, the procedure and its calibration via design are presented. Via defects among multiple vias are diagnosed based on simulations and measurements. The proposed method for multi-via test only extracts a single-port network of each via, which means it cannot characterize a multi-port network of vias. Therefore, the proposed method is improved to characterize the multi-port network of multiple vias to capture inter-via couplings as shown in Fig.1-3(c). The feasibility of the proposed method for multi-port characterization is described in section IV. From the multi-port extraction method, a two-port network is characterized based on simulations. Section V draws the conclusion. For fast testing of the proposed method in package and wafer-level, the future work is introduced.

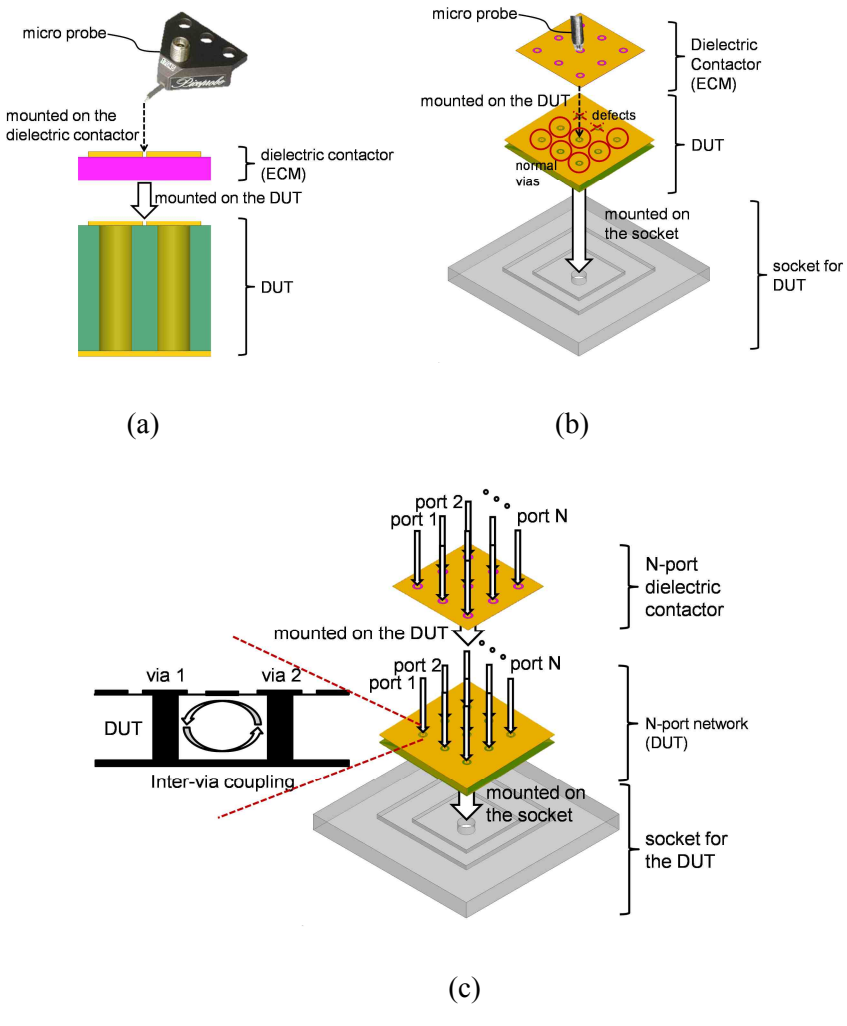


Fig. 1-3. Three cases of the proposed method: (a) a single-pair vias extraction (b) multi-via testing (c) multi-port characterization

Chapter II

Indirect contact probing method for characterizing a single pair of vias

For the protection of a DUT from the direct-contact of micro probe tips, the key element of the indirect contact probing method is the dielectric contactor that consists of high-permittivity embedded capacitance material (ECM) film and metal pads as shown in Fig. 1-1(c) [13]. After applying de-embedding technique, the impedance of a single-pair vias in the DUT can be characterized by the indirect-contact probing. In the following subsections, the indirect contact probing method for characterizing a single pair of vias is investigated.

2.1 Setup and procedure

The procedure of the proposed method is illustrated in Fig. 2-1. The first step is a one-port calibration to characterize the dielectric contactor as a two port network parameter $[S]_{dcon}$. Since the reciprocal $[S]_{dcon}$ contains three unknowns ($S_{11,dcon}$, $S_{22,dcon}$ and $S_{12,dcon}$ =$S_{12,dcon}$), three one-port measurements should be performed using three different calibration vias. To extract two-port network parameters from the three one-port measurements, we adopt the following formulas [14]:

$$
\begin{aligned}
S_{11,\mathrm{dcon}} &= -\frac{\Gamma_a\Gamma_b\Gamma_{s,c}\Delta_1 + \Gamma_b\Gamma_c\Gamma_{s,a}\Delta_2 + \Gamma_a\Gamma_c\Gamma_{s,b}\Delta_3}{\Delta} \\
S_{22,\mathrm{dcon}} &= \frac{\Gamma_c\Delta_1 + \Gamma_a\Delta_2 + \Gamma_b\Delta_3}{\Delta} \\
S_{12,\mathrm{dcon}}S_{21,\mathrm{dcon}} &= \frac{(\Gamma_a-\Gamma_b)(\Gamma_b-\Gamma_c)(\Gamma_c-\Gamma_a)\Delta_1\Delta_2\Delta_3}{\Delta^2},
\end{aligned}
\tag{1}
$$

where

$$
\Delta = \Gamma_c\Gamma_{s,c}\Delta_1 + \Gamma_a\Gamma_{s,a}\Delta_2 + \Gamma_b\Gamma_{s,b}\Delta_3,
$$
$$
\Delta_1 = \Gamma_{s,a} - \Gamma_{s,b}, \Delta_2 = \Gamma_{s,b} - \Gamma_{s,c}, \Delta_3 = \Gamma_{s,c} - \Gamma_{s,a}
$$

, where $\Gamma_{s,a}, \Gamma_{s,b}, \Gamma_{s,c}$ are the known reflection coefficients at the three calibration vias and $\Gamma_a, \Gamma_b, \Gamma_c$ are the reflection coefficients at the calibration vias from indirect-contact measurements using the dielectric contactor. From (1), we can calculate $[S]_{dcon}$ for the only contactor portion. Using the *S*-parameter of the contactor, an actual DUT can then be characterized from the indirect-contact measurements. The dielectric contactor is mounted on the DUT, and the one-port *S*-parameter is measured at the contactor. The reflection coefficient at the DUT can be calculated from the following de-embedding formulation derived from the signal flow graph as shown in Fig. 2-2:

$$\Gamma_{DUT,con} = \frac{\Gamma_{DUT,ncon} - S_{11,dcon}}{\Gamma_{DUT,ncon} S_{22,dcon} - S_{11,dcon} S_{22,dcon} + S_{21,dcon}^{\ 2}} \quad (2)$$

, where $\Gamma_{DUT,ncon}$ represents the reflection coefficients at the contactor from the indirect-contact measurement, and $\Gamma_{DUT,con}$ represents the extracted reflection coefficients at the DUT. To identify the type of defective vias by observing the impedance curves of short or open defects, respectively, we transform $\Gamma_{DUT,con}$ to the *Z*-parameter.

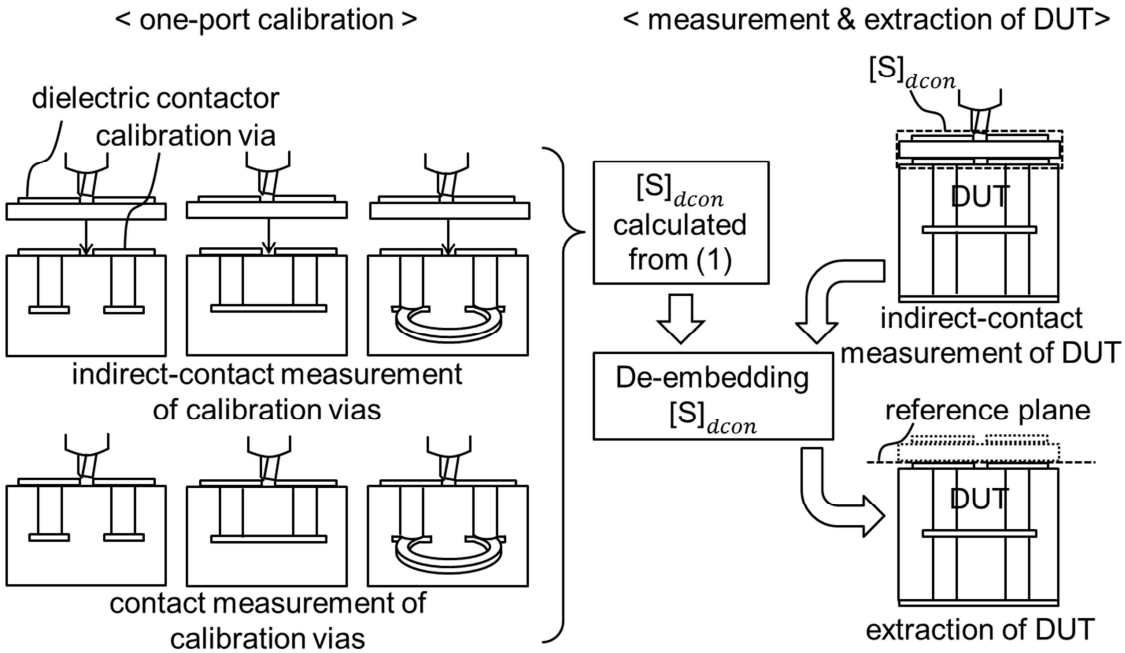


Fig. 2-1. Procedure of the indirect contact probing method

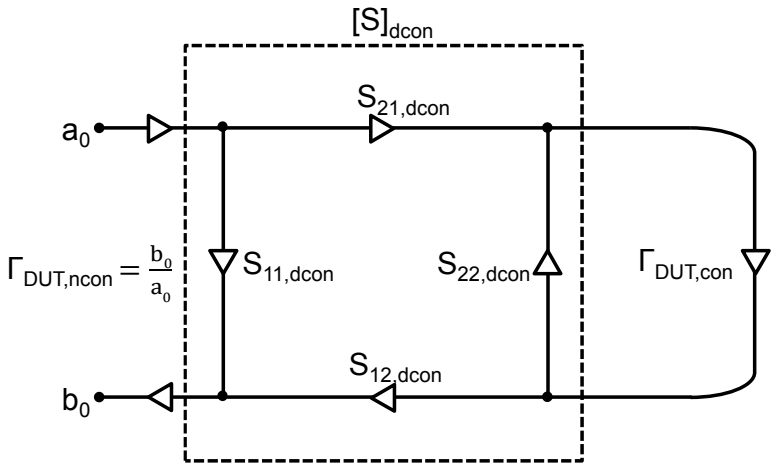


Fig. 2-2. Signal flow graph representing the series connection between the dielectric contactor and the DUT

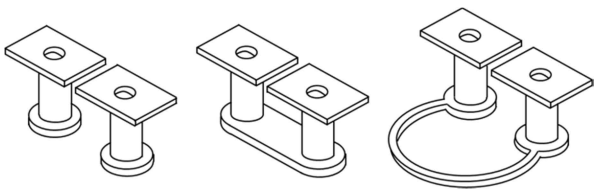
2.2 Design of calibration vias

A main difficulty of using calibration structures including vias is that a finite via length limits the available frequency range of calibration. To obtain a required calibration frequency range, the following design rules are considered:

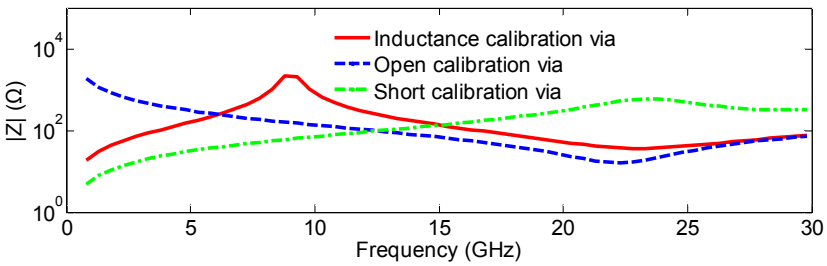
1) When the reflection coefficients of any different calibration vias coincide, Δ in (1) becomes zero, causing singular points in (1) [14]. For this reason, the three calibration vias should have fully different characteristics over the frequency band of interest. For example, a matched load, which is commonly used in the Thru-Reflect-Line (TRL) technique [15], is not distinguishable from shorted calibration vias at high frequencies since their stray via inductances are dominant.

2) When the via length is $\lambda/4$ or $\lambda/2$, the via becomes resonant, and the one-port calibration cannot characterize $[S]_{dcon}$. Therefore, calibration vias with shorter length are better to cover a wider frequency range.

Considering the rules discussed above, we designed the calibration vias with an open end, a short end, and an inductance pattern, as shown in Fig. 2-3(a). Fig. 2-3(b) shows the simulation results of the calibration vias. Although there are the crossing points around 15 GHz, they do not cause singularity in $[S]_{dcon}$ since the phases at the crossing points are not the same.



(a)



(b)

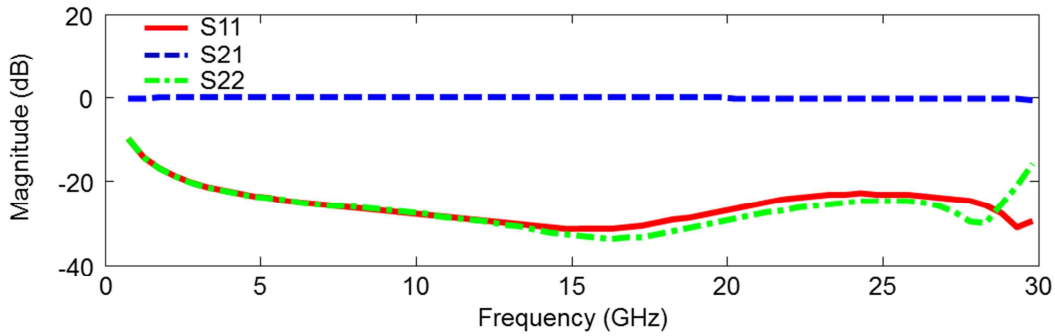
Fig. 2-3. Structures of the three different calibration vias as (a) the open-end (left), the short-end (center), and the inductance patterns (right) (b) simulated input impedances of the three calibration vias

2.3 Verification of the method by simulation

We have designed four-layer PCBs, including the DUTs of the normal via, the open and the short via defects, as shown in Fig. 2-4(a)-(c). The length of the calibration vias and the defective vias are 0.8 mm and 1.6 mm, respectively, with the copper thickness of 1 oz and the pad dimension of 0.75 mm by 1 mm on the top layer. A dielectric contactor has pads of the same size with PCBs. The thickness and the permittivity of the contactor, which have been chosen to maximize the capacitive coupling, are 12 μm and 22, respectively.

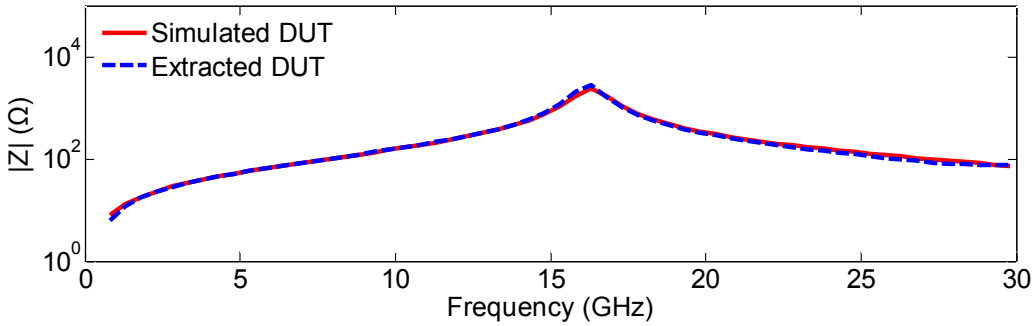
Fig. 2-4. DUTs of (a) the normal via, (b) the open via defect, and (c) the short via defect

The simulation has been performed using Ansys HFSS [16] at the frequency range of 0.8-30 GHz. In Fig. 2-5(a), the extracted $[S]_{dcon}$ represents the characteristic of the dielectric contactor including couplings from vias under the contactor. In Fig. 2-5(b)-(d), the impedances of the extracted DUTs from the indirect contact probing show a good agreement with those obtained from the direct contact probing.

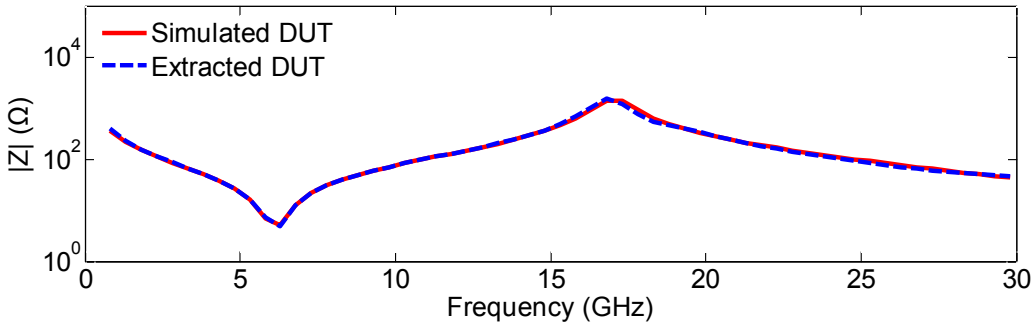


(a) extracted $[S]_{dcon}$

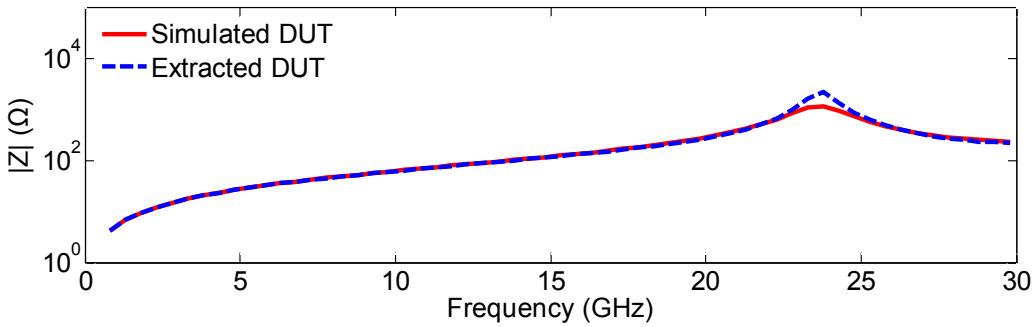
Fig. 2-5. Extracted via characteristics from the simulation results



(b) normal via



(c) open via defect



(d) short via defect

Fig. 2-5. (continued)

2.4 Verification of the method by measurement

We have implemented the dielectric contactor, the calibration vias, and DUTs for the verification through measurements as shown in Fig. 2-6. The dielectric contactor is specially manufactured due to the limitation on PCB production process. The dielectric contactor consisting of a thin ECM film in Fig. 2-7(a) cannot withstand an etching process. To alleviate this issue, only the top layer of the ECM

film is processed with etching and gold plating as shown in Fig. 2-7(b). The remaining copper layer on the bottom of the ECM film is then removed by using the iron(II) chloride solution as described in Fig. 2-7(c). After washing the dielectric film, the process of manufacturing dielectric contactor is completed. Fig. 2-8 shows how probes are mounted on the dielectric contactor and the DUT using GGB 40A-GS-250 probe connected to Agilent N5242A covering 0.8-26.5 GHz. For calibration, short, open, load and thru (SOLT) method [17] has been used with CS-8. With the calibration, we repeatedly measured Γ_a, Γ_b and Γ_c using direct contact and confirmed the maximum variation of 0.33 dB up to 18 GHz. For comparison, DUTs were extracted from indirect-contact measurement data, and the same DUTs were directly measured after the dielectric contactor removed. Although $[S]_{dcon}$ in Fig. 2-9(a) is different from $[S]_{dcon}$ in the simulation shown in Fig. 2-5(a), we can extract the DUT characteristics if the environment to obtain $[S]_{dcon}$ is consistently maintained during the indirect-contact process. In Fig. 2-9(b)-(d), the extracted results on the normal via, the open and the short via defects correspond with the results of the contact measurements at frequencies ranging from 2.5 GHz to 18 GHz except at low frequencies, where the resolution is very sensitive to the alignment between the dielectric contactor and the DUT.

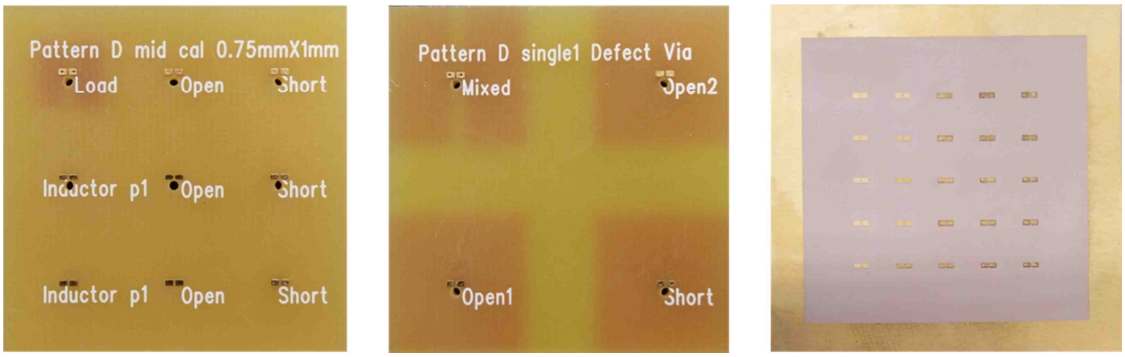
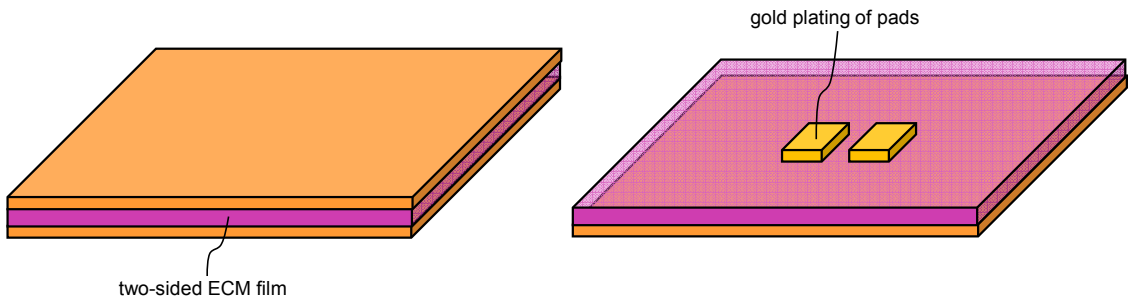
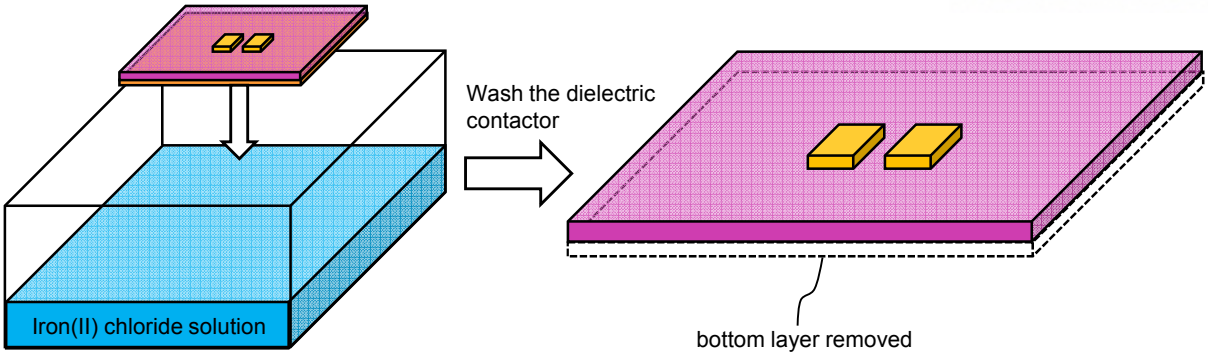


Fig. 2-6. Implemented structures: calibration vias (left), DUTs (center), and the ECM contactor (right)



(a) (b)

Fig. 2-7. Process of manufacturing the dielectric contactor: (a) the raw ECM film (b) the etched top copper layer with gold plating



(c)

Fig. 2-7. (c) the process of removing the bottom layer (continued)

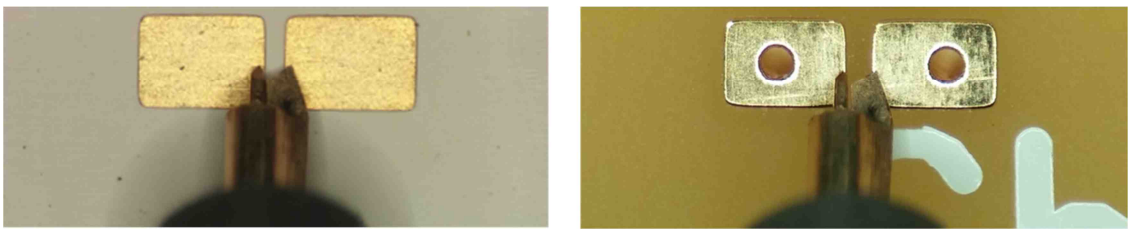
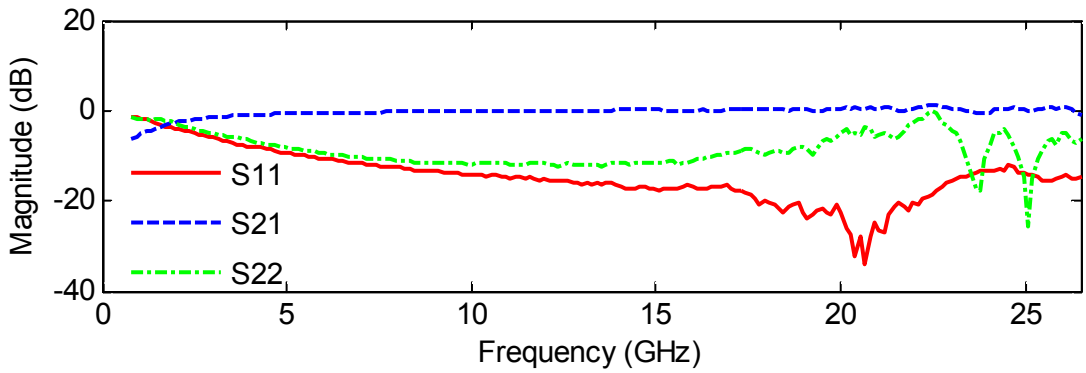
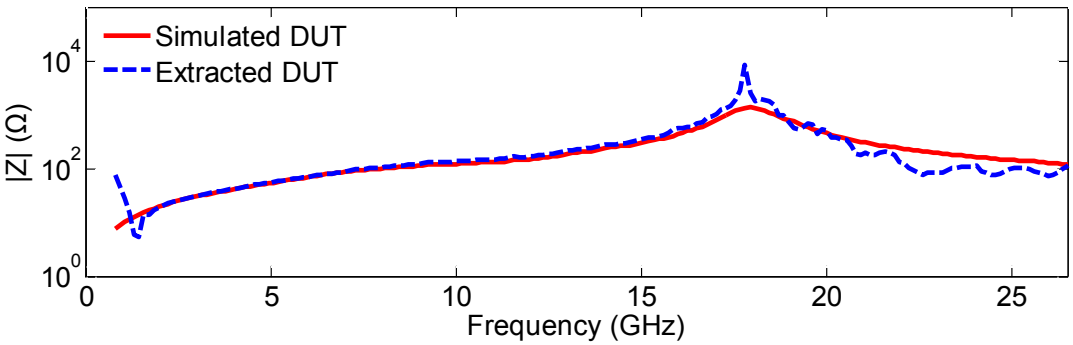


Fig. 2-8. Probing examples: the indirect-contact probing on the dielectric contactor mounted on the DUT or the calibration vias (left) and the contact probing (right)

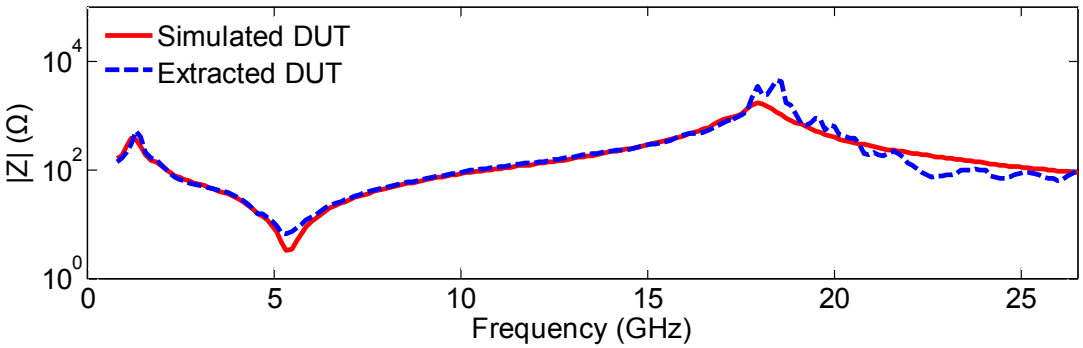


(a) extracted $[S]_{dcon}$

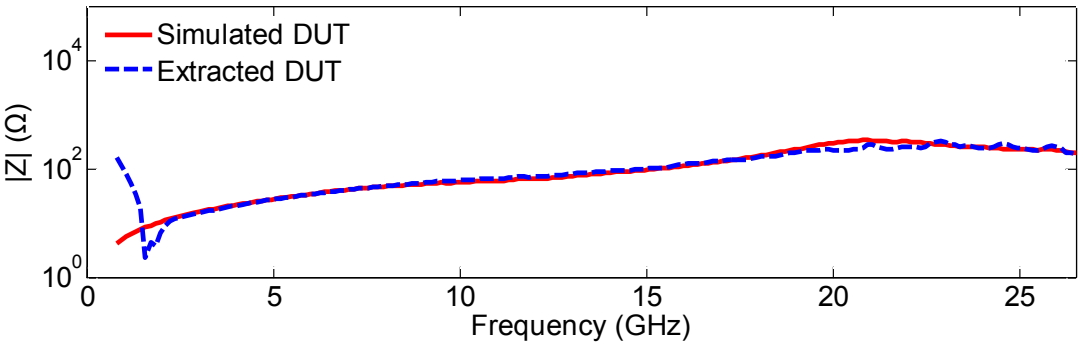
Fig. 2-9. Extracted via characteristics from the measurement results



(b) normal via



(c) open via defect



(d) short via defect

Fig. 2-9. (continued)

Chapter III

Indirect contact probing method for multi-via test

In most cases, packages or interposers require multiple vertical interconnects or vias. They should be properly tested with ensuring protection from direct contact probing. Since the multiple vias usually share the common reference plane, resonances of calibration vias due to a cavity effect should be minimized. With the consideration of these issues, the proposed method for the single-via extraction in the previous chapter can extend on the multi-via test. The proposed method is limited to extract single-port of a via. By extracting the impedances from single-port networks of each via, they can be used to diagnose via defects rather than characterize multiple vias.

3.1 Setup and procedure

The indirect contact probing method for multi-via test should extract characteristics of each via to detect via defects. To realize this, the metal socket and the dielectric contactor are adopted [18]. The socket and its cover enclose the DUT or the calibration substrate to provide the current return path, as shown in Fig. 3-1. The current return path to the reference plane enables multiple vias to be extracted based on the common reference. In addition, the vacuum pump connected to the socket absorbs the air through the hole in the socket. The air flow provides stable contact between the dielectric contactor and the DUT. The multi-pad dielectric contactor is also designed to cover multiple vias. It consists of the multiple pads, where each pad is located to positions corresponding to the multiple vias in the DUT, and the ground plane fabricated on the ECM film as shown in Fig 3-2(b). Fig. 3-2(a) and (b) show the measurement setups for the indirect-contact probing and the direct-contact probing, respectively, after the DUT or the calibration substrate is assembled with the socket and the socket cover. For the indirect-contact probing, after the dielectric contactor is mounted on the DUT or the calibration substrate, the probe contacts the dielectric contactor pad, whereas the direct-contact probing is conducted without the dielectric contactor.

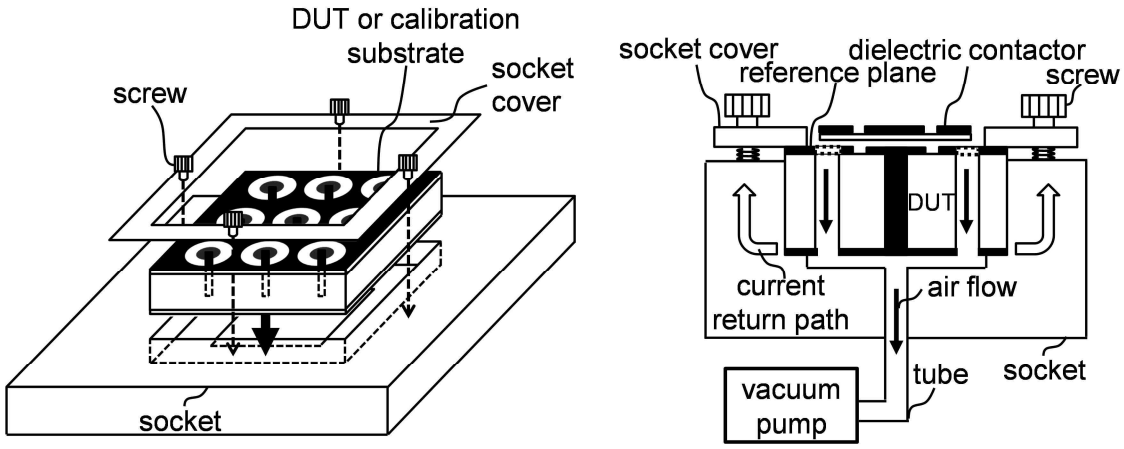
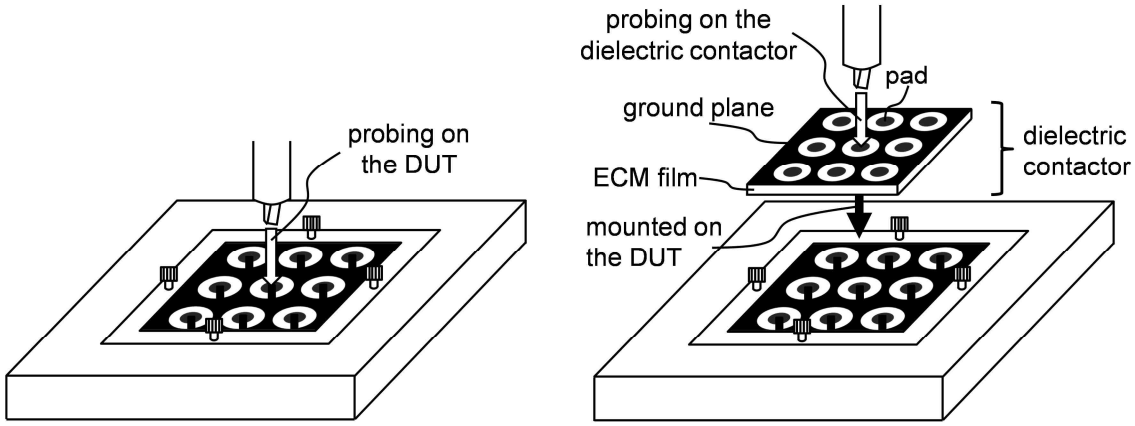


Fig. 3-1. Assembling the socket and its cover (left) and the cross section of the socket (right) that shows the current return path and the connection between the vacuum pump and the socket



(a) (b)

Fig. 3-2. Measurement setups: (a) direct-contact probing (b) indirect-contact probing

The proposed method can extract a via among multiple vias. Therefore, it should be performed n times, where n is the number of vias. The numbering of the vias in the DUT and the pads on the dielectric contactor are described in Fig. 3-3, in the case of n = 9. The explanation here is based on i th via and i th dielectric contactor pad, where i = 1 to n, and all DUTs and calibration substrates are inserted in the sockets. The procedure for the indirect contact probing method is presented in Fig. 3-4. The first step starts with one-port calibration. From one-port calibration, we can characterize the portion between the dielectric contactor pad and the via pad expressed as $[S]^{(i)}_{dcon}$, where the two-port measurement of probing is not available. One-port calibration requires the three calibration vias of different characteristics. Performing the indirect-contact and the direct-contact probing measurements on the calibration vias, similarly to the single-pair vias case, the two-port network parameter $[S]^{(i)}_{dcon}$ consisting of $S^{(i)}_{11,dcon}$, $S^{(i)}_{22,dcon}$ and $S^{(i)}_{12,dcon}=S^{(i)}_{21,dcon}$ due to reciprocity can be calculated in terms of

reflection coefficients of the three calibration vias as shown below [14], [17]:

$$S_{11,dcon}^{(i)} = -\frac{\Gamma_a^{(i)}\Gamma_b^{(i)}\Gamma_{s,c}^{(i)}\Delta_1^{(i)} + \Gamma_b^{(i)}\Gamma_c^{(i)}\Gamma_{s,a}^{(i)}\Delta_2^{(i)} + \Gamma_a^{(i)}\Gamma_c^{(i)}\Gamma_{s,b}^{(i)}\Delta_3^{(i)}}{\Delta^{(i)}}$$
$$S_{22,dcon}^{(i)} = \frac{\Gamma_c^{(i)}\Delta_1^{(i)} + \Gamma_a^{(i)}\Delta_2^{(i)} + \Gamma_b^{(i)}\Delta_3^{(i)}}{\Delta^{(i)}} \quad (3)$$
$$S_{12,dcon}^{(i)}S_{21,dcon}^{(i)} = \frac{(\Gamma_a^{(i)} - \Gamma_b^{(i)})(\Gamma_b^{(i)} - \Gamma_c^{(i)})(\Gamma_c^{(i)} - \Gamma_a^{(i)})\Delta_1^{(i)}\Delta_2^{(i)}\Delta_3^{(i)}}{\Delta^{(i)2}}$$

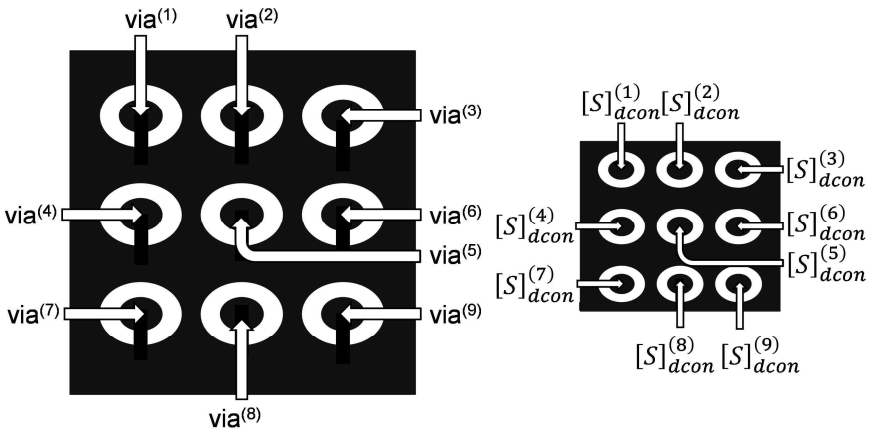
,where

$$\Delta^{(i)} = \Gamma_c^{(i)}\Gamma_{s,c}^{(i)}\Delta^{(i)}_1 + \Gamma^{(i)}_a\Gamma^{(i)}_{s,a}\Delta^{(i)}_2 + \Gamma^{(i)}_b\Gamma^{(i)}_{s,b}\Delta^{(i)}_3,$$
$$\Delta^{(i)}_1 = \Gamma^{(i)}_{s,a} - \Gamma^{(i)}_{s,b}, \Delta^{(i)}_2 = \Gamma^{(i)}_{s,b} - \Gamma^{(i)}_{s,c}, \Delta^{(i)}_3 = \Gamma^{(i)}_{s,c} - \Gamma^{(i)}_{s,a},$$

$\Gamma^{(i)}_{s,a}, \Gamma^{(i)}_{s,b}, \Gamma^{(i)}_{s,c}$ are the reflection coefficients measured by the direct-contact probing and $\Gamma^{(i)}_a, \Gamma^{(i)}_b$, $\Gamma^{(i)}_c$ by the indirect-contact probing. Until now, we have characterized the dielectric contactor. Following that, the DUT is measured by the indirect-contact probing. The reflection coefficient of the DUT as shown below can be obtained from de-embedding formula derived from the signal flow graph in Fig. 3-5:

$$\Gamma_{DUT,con}^{(i)} = \frac{\Gamma_{DUT,ncon}^{(i)} - S_{11,dcon}^{(i)}}{\Gamma_{DUT,ncon}^{(i)}S_{22,dcon}^{(i)} - S_{11,dcon}^{(i)}S_{22,dcon}^{(i)} + S_{21,dcon}^{(i)\,2}} \quad (4)$$

, where $\Gamma^{(i)}_{DUT,ncon}$ and $\Gamma^{(i)}_{DUT,con}$ are the reflection coefficients measured by the indirect-contact probing and extracted by the de-embedding formula, respectively. To detect the types of defects by using impedance curves, $\Gamma^{(i)}_{DUT,con}$ is converted to *Z*-parameter. Applying this procedure to entire vias, *i*=1 to *n*, we can obtain the impedances of all vias.



(a) (b)

Fig. 3-3. Numbering of (a) the vias in the DUT and (b) the pads on the dielectric contactor

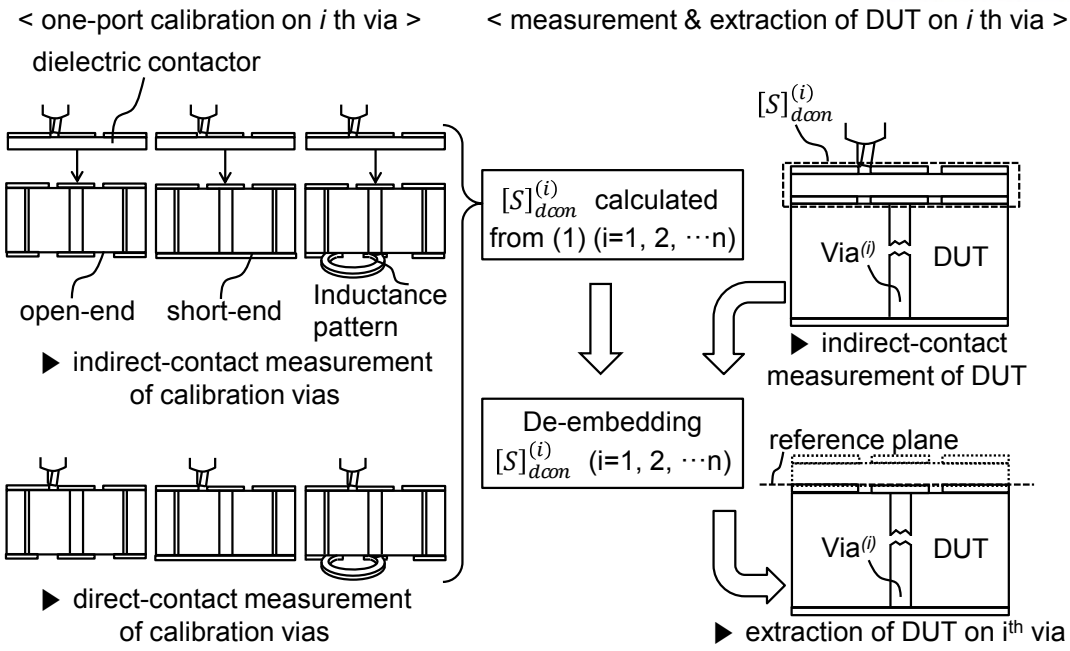


Fig. 3-4. Procedure for the indirect contact probing method

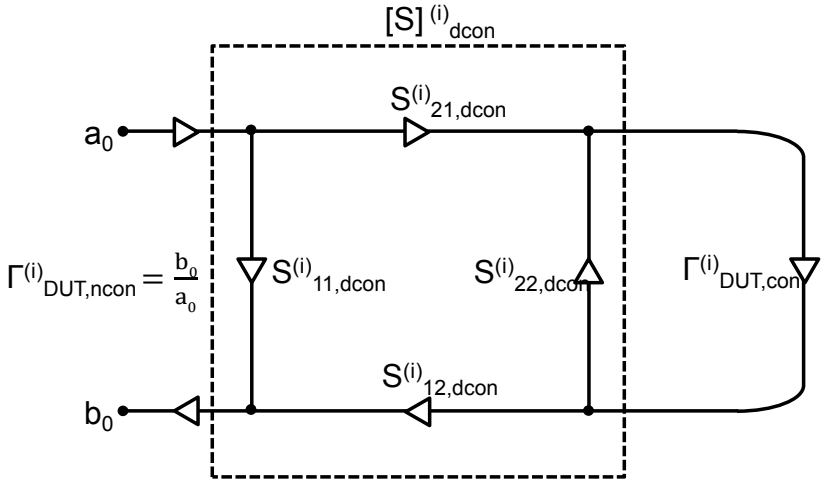


Fig. 3-5. Signal flow graph representing the series connection between the dielectric contactor and the multiple vias

3.2 Design of calibration vias

Calibration via design is important to perform the one-port calibration. As basic design, the calibration vias in its substrate are located to positions corresponding to vias in the DUT. At the end of via, one of three types of patterns is fabricated. The major issues on designing calibration vias are cavity resonance and impedance coincidence of calibration vias. Without considering these issues, poorly designed calibration vias cause the ill-characterization of the dielectric contactor and the

reduction of available frequency ranges in the one-port calibration. To address the issues, we discuss solutions in this subsection.

3.2.1. Cavity resonance

Cavity resonance is inevitable due to the calibration vias surrounded with conductors of the socket and its ground plane as shown in Fig 3-1. In a rectangular shaped cavity, the lowest resonant frequency is determined as [19]:

$$f = \frac{1}{a\sqrt{2\mu\varepsilon}} \tag{5}$$

, where a is the width of the calibration substrate and ε, μ are its permittivity and permeability. At the resonant frequency of the cavity, the dielectric contactor characteristic cannot be characterized due to the uncertainty in the calibration process. For this reason, dense ground vias are inserted near the calibration vias to increase the lowest cavity resonance frequency by reducing the paths for return currents, as shown in Fig. 3-6. As a result, the cavity resonant effect can be suppressed by the ground vias.

3.2.2. Coincidence of calibration via characteristics

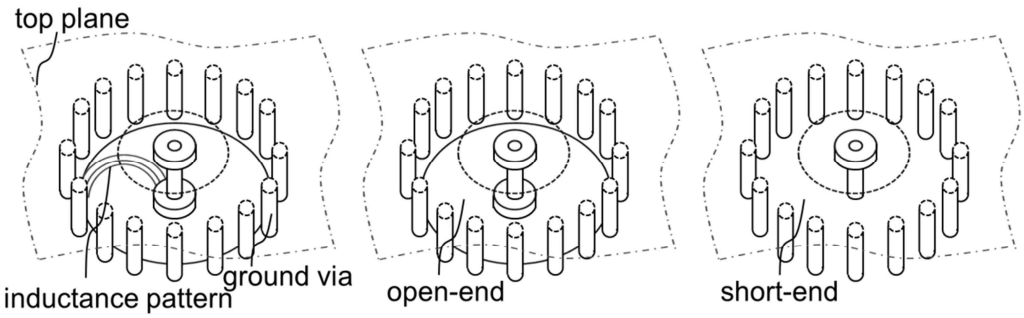
As discussed in the single-via case, impedance coincidences of the calibration vias cause the singular point of $\Delta^{(i)}$ in (3). For ensuring significant difference of calibration via characteristics, an open-end, a short-end and an inductance pattern calibration vias are selected as shown in Fig. 3-6. Following that, we should find resonant frequencies of calibration vias to increase an available frequency range. Due to dense ground vias near the calibration via introduced in the previous subsection, calibration vias can be modeled as a coaxial transmission line with lumped element terminations. The inductance pattern, the open-end and the short-end calibration vias, where the cross section views are shown in Fig. 3-7(a)-(c) on the left, can be modeled in Fig. 3-7(a)-(c) on the right. From the models, the input impedances of the calibration vias can be obtained as follows:

$$\begin{aligned}
Z_{\text{inductance cal}} &= \frac{j(Z_0 \tan\beta l + wL_{\text{pattern}}Z_0 - w^2 L_{\text{pattern}}C_{\text{pad end}}Z_0 \tan\beta l)}{w^3 C_{anti\,pad}L_{\text{pattern}}C_{\text{pad end}}Z_0{}^2 \tan\beta l - w^2 L_{\text{pattern}}Z_0(C_{\text{anti pad}}+C_{\text{pad end}}) - w\tan\beta l(C_{\text{anti pad}}Z_0{}^2 + L_{\text{pattern}}) + Z_0} \\
Z_{\text{open cal}} &= \frac{j(Z_0 + wC_{\text{pad end}}Z_0{}^2 \tan\beta l)}{w^2 C_{\text{anti pad}}C_{\text{pad end}}Z_0{}^2 \tan\beta l - wZ_0(C_{\text{anti pad}}+C_{\text{pad end}}) - \tan\beta l} \\
Z_{\text{short cal}} &= \frac{jZ_0 \tan\beta l}{1 - wZ_0 C_{\text{anti pad}} \tan\beta l},
\end{aligned} \tag{6}$$

where

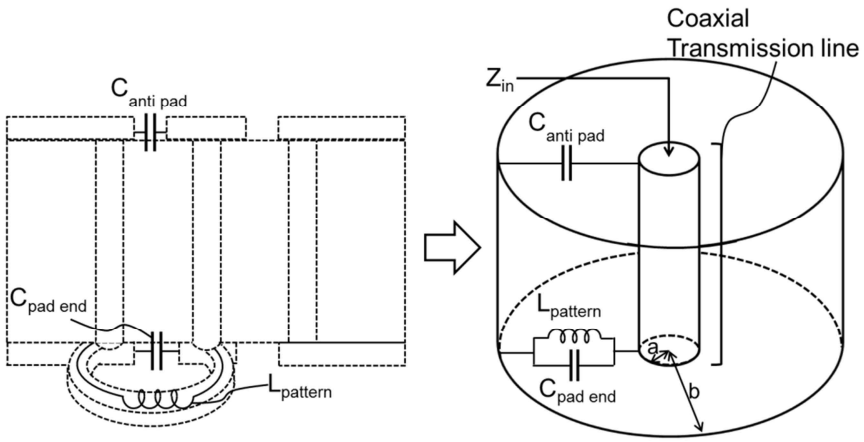
$$\beta = w\sqrt{\mu\varepsilon}, Z_0 = \frac{\ln(b/a)}{2\pi}\sqrt{\frac{\mu}{\varepsilon}},$$

a is the radius of the calibration via and *b* is the radius of the outer cylinder consisting of ground vias as shown in Fig. 3-7(a), and ε, μ are permittivity and permeability of FR-4 substrate. $C_{\text{pad end}}$, $C_{\text{anti pad}}$, $C_{\text{anti pad}}$ and L_{pattern} are the capacitance and the inductance, respectively, corresponding to Fig. 3-7(a)-(c). The lumped element values can be adjusted from geometry parameters of the anti-pad gap and the length of inductance pattern on the bottom layer. Simulated in Q3D Extractor 12.0 [20], L_{pattern}, $C_{\text{pad end}}$ and $C_{\text{anti pad}}$ of the lumped element values are 1.38 nH, 38.8 fF and 98.8 fF, respectively. From (6), the resonant and the anti-resonant frequencies are obtained as shown in Table 3-1. As a result, the impedances of the calibration vias do not coincide due to the resonant frequencies separated by manipulating the lumped element values.



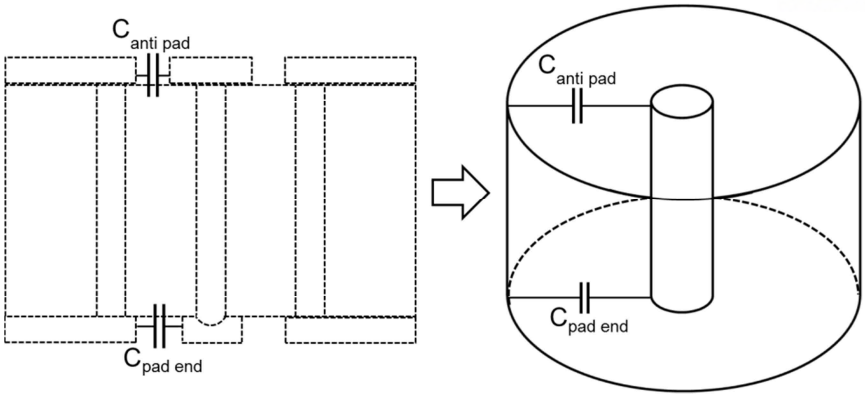
(a) (b) (c)

Fig. 3-6. Calibration vias: (a) the inductance pattern (b) open-end (c) short-end

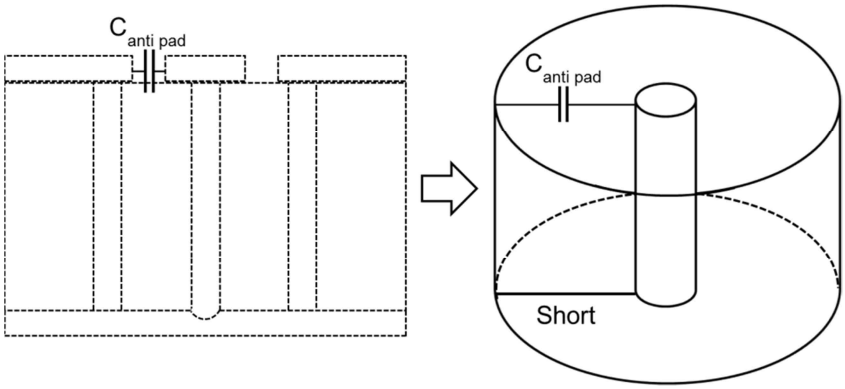


(a)

Fig. 3-7. Modeling for finding resonant frequencies: (a)-(c) the cross section of the inductance pattern, the open-end and the short-end calibration vias (left) and their coaxial transmission line models with lumped elements (right)



(b)



(c)

Fig. 3-7. (continued)

	Anti-resonant frequency		Resonant frequency
Inductance pattern cal.	7.3 GHz	28.5 GHz	25.6 GHz
Open-end cal.	25.6 GHz		18 GHz
Short-end cal.	14 GHz		

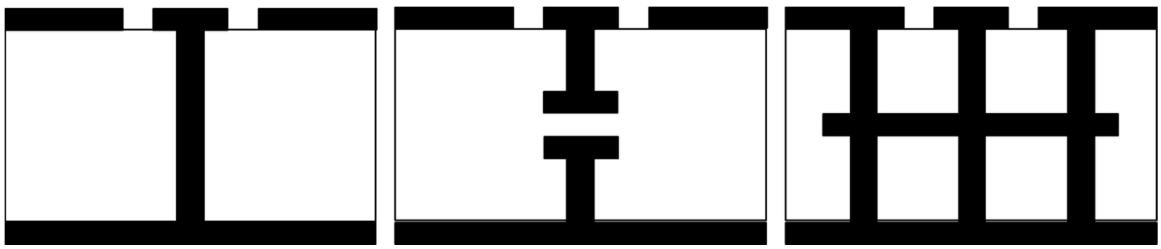
Table 3-1. Calculated resonant frequencies

3.3 Verification of the method by simulation

We have designed four-layer PCBs of calibration substrates and DUTs to verify the proposed method. Three calibration substrates contain the inductance pattern, the open-end and the short-end calibration vias, respectively. For detection test, DUTs include normal vias, open and short defects as via arrays, where the cross sections are shown in Fig. 3-8(a)-(c). The dimension of DUTs and calibration substrates are denoted in Fig. 3-9(a). The dielectric constant and the thickness of the dielectric contactor are chosen as 22 and 0.012 mm in Fig. 3-9(b), respectively, to maximize the

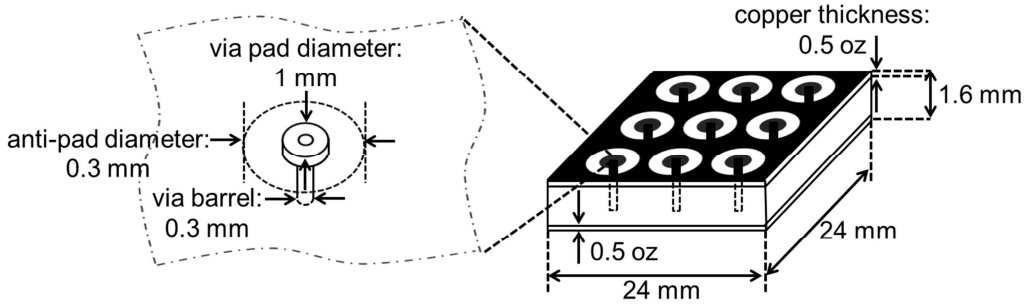
capacitive coupling. In addition, the dielectric contactor pads are designed larger than via pads to ensure the one-port calibration in a low frequency range.

Simulation results are conducted by Ansys HFSS 15.0 in the frequency range from 0.8 to 30 GHz. The locations of the via defects in two DUTs, where one contains open defects among vias and another one short defects, are shown in Fig. 3-10(a)-(b). $[S]^{(1)}_{dcon}$, $[S]^{(4)}_{dcon}$ and $[S]^{(5)}_{dcon}$, which is the dielectric contactor characteristic at the locations corresponding to i = 1, 4, 5, are characterized up to 24 GHz as shown in Fig. 3-11(a)-(c). In Fig. 3-12(a)-(c), the extracted via impedances corresponding to their locations are identical with those conducted by the direct-contact probing within the available calibration frequency range.

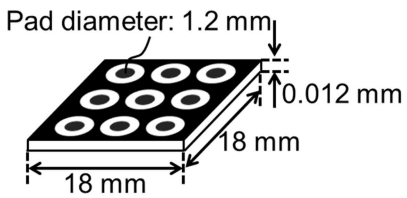


(a) (b) (c)

Fig. 3-8. Cross sections of the vias in DUTs: (a) normal via (b) open defect (c) short defect

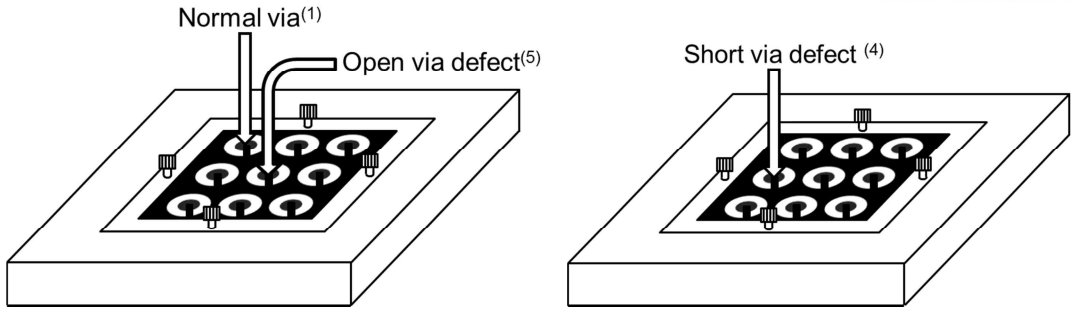


(a)



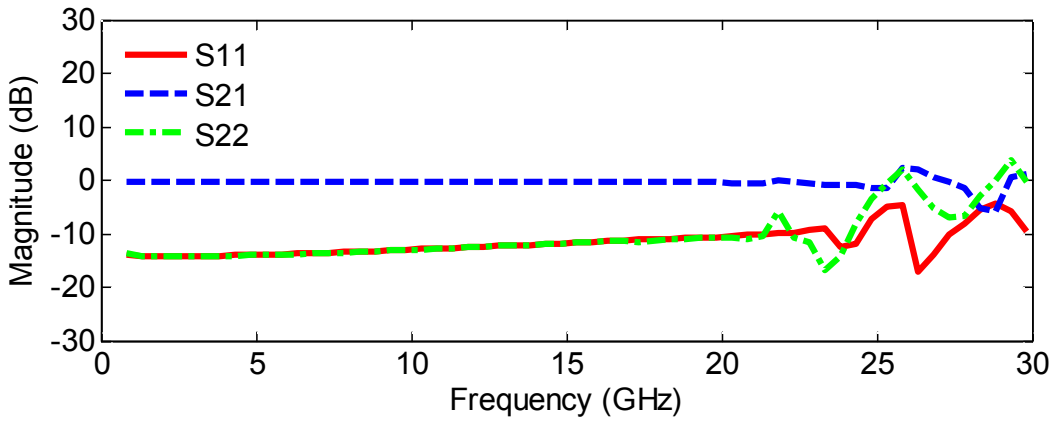
(b)

Fig. 3-9. Dimension of PCBs: (a) the DUT or the calibration substrate (b) the dielectric contactor

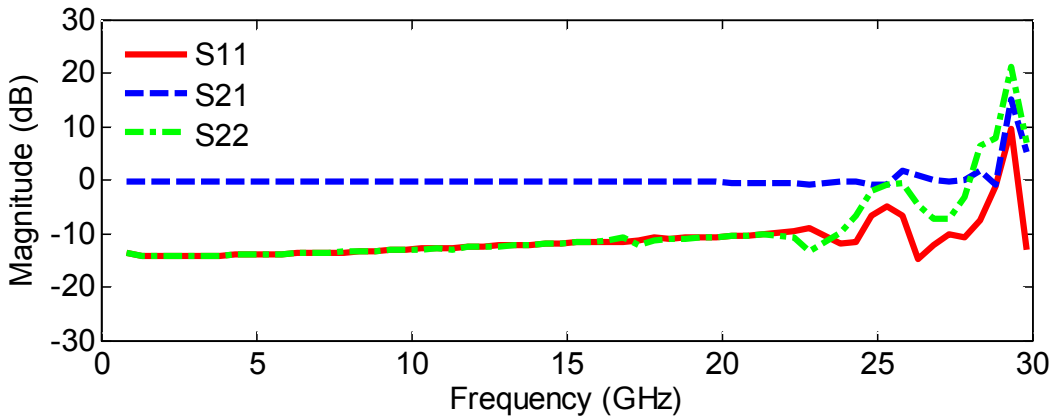


(a) (b)

Fig. 3-10. Locations of via defects in each DUT: (a) the normal via and the open via defect (b) the short via defect

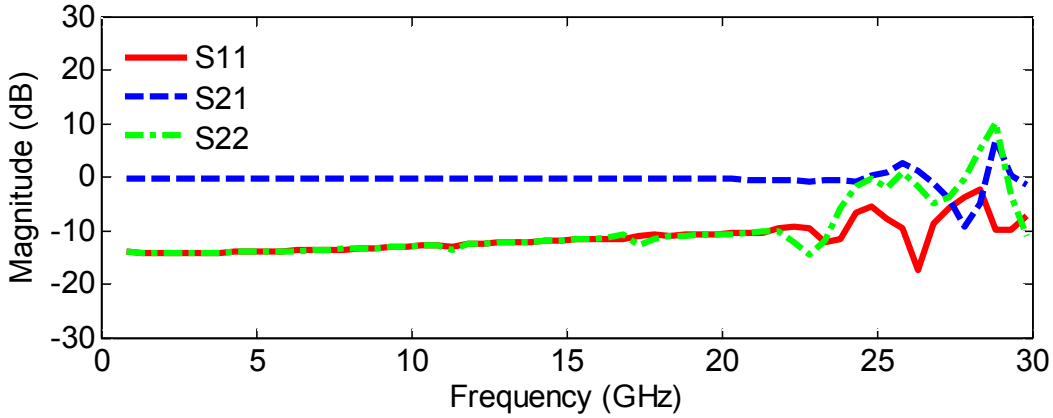


(a) $[S]^{(1)}_{dcon}$



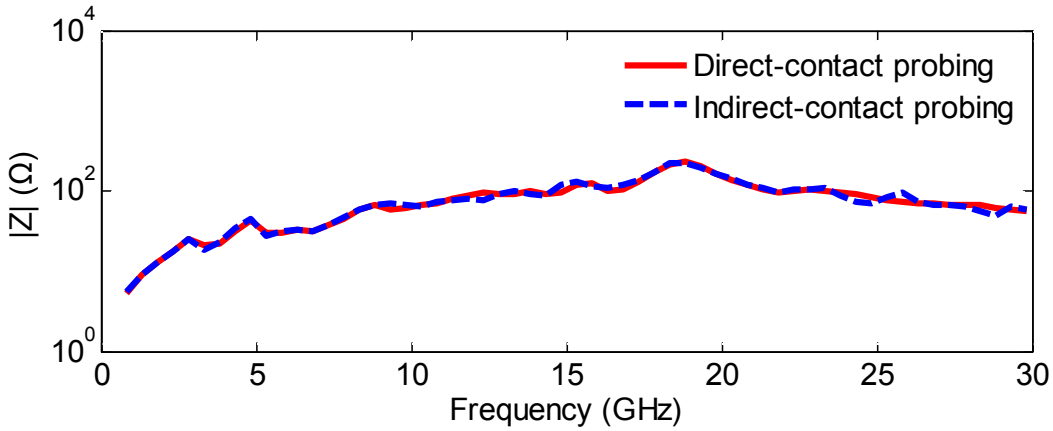
(b) $[S]^{(5)}_{dcon}$

Fig. 3-11. Characterized dielectric contactor

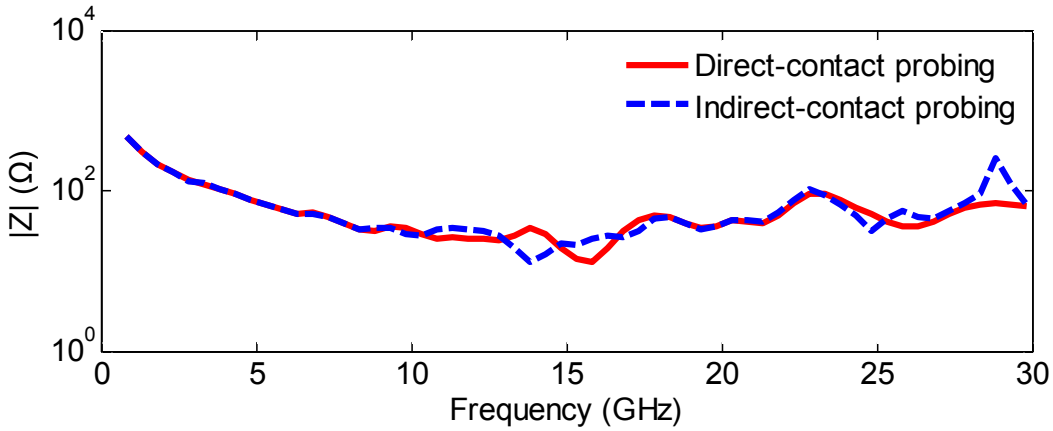


(c) $[S]^{(4)}_{dcon}$

Fig. 3-11. (continued)

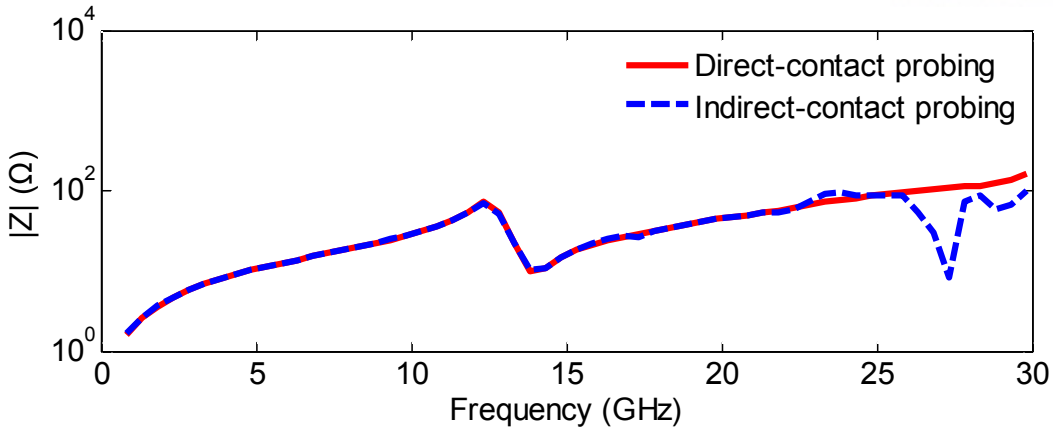


(a) via$^{(1)}$



(b) via$^{(5)}$

Fig. 3-12. Extracted vias in each DUT



(c) via[4]

Fig. 3-12. (continued)

3.4 Verification of the method by measurement

Based on measurements, we have verified the proposed method. As shown in Fig. 3-13(a)-(h), the calibration via substrates, the DUTs, the dielectric contactor and the socket with its cover are manufactured as designed in the previous subsection. The assembled one is shown in Fig. 3-13(i). Due to the limitation of the PCB production process, the ECM film is processed in the same way as shown in Fig.2-7(a)-(c). For the measurement setup, the socket is connected to the vacuum pump in Fig. 3-14(a). The air flows to the hole in the middle of the socket, providing better contact between the dielectric contactor and the PCB. Connected to Agilent N5242A covering a frequency range 0.8 GHz to 26.5 GHz, GGB 40A-GS-500 micro probe is attached to the probe station as shown in Fig 3-14(b). Using SOLT method with CS-11 calibration substrate, the micro probe is calibrated. Under this measurement setup, the direct-contact and the indirect-contact probing measurement are described in Fig. 3-14(c) and (d), respectively.

For the detection of via defects, Fig. 3-15(a)-(b) shows the types and locations of via defects in each DUT, where normal vias are not denoted. In Fig. 3-16(a)-(i), the dielectric contactor characteristics corresponding to each location are characterized within a frequency range 0.8 GHz to 22 GHz. Due to the calibration via manufacturing error, there are a few unexpected resonant frequencies. Moreover, the contact between pads of the dielectric contactor and the vias is not perfect, which means actual capacitances in Fig. 1-1(c) are smaller than in simulations. As a result, all $[S]^{(i)}_{dcon}$ in measurements are not the same as obtained by simulations. As discussed in the single-via extraction case, maintaining the same condition of the indirect-contact process to obtain $[S]^{(i)}_{dcon}$, we can extract the impedances of multiple vias by applying the de-embedding technique. Fig. 3-17(a)-(i) show the extracted via impedances in the DUT containing the open defects among multiple vias. The

impedance curves at i = 4, 5, 7 representing open defects are successfully detected. The impedances of the short defects and normal vias in another DUT are also extracted as shown in Fig. 3-18(a)-(i). From the impedance curves at i = 4, 7, the short via defects are also found. The via impedances extracted by the proposed method and measured by the direct-contact probing show a good agreement from 2.5 GHz to 22 GHz except low frequencies, where the accuracy is very sensitive depending on alignment between pads of the via and the dielectric contactor, and the resonant frequencies in $[S]^{(i)}_{dcon}$. The extracted impedance of the frequency range here is higher than the case of the proposed method for a single-pair vias.

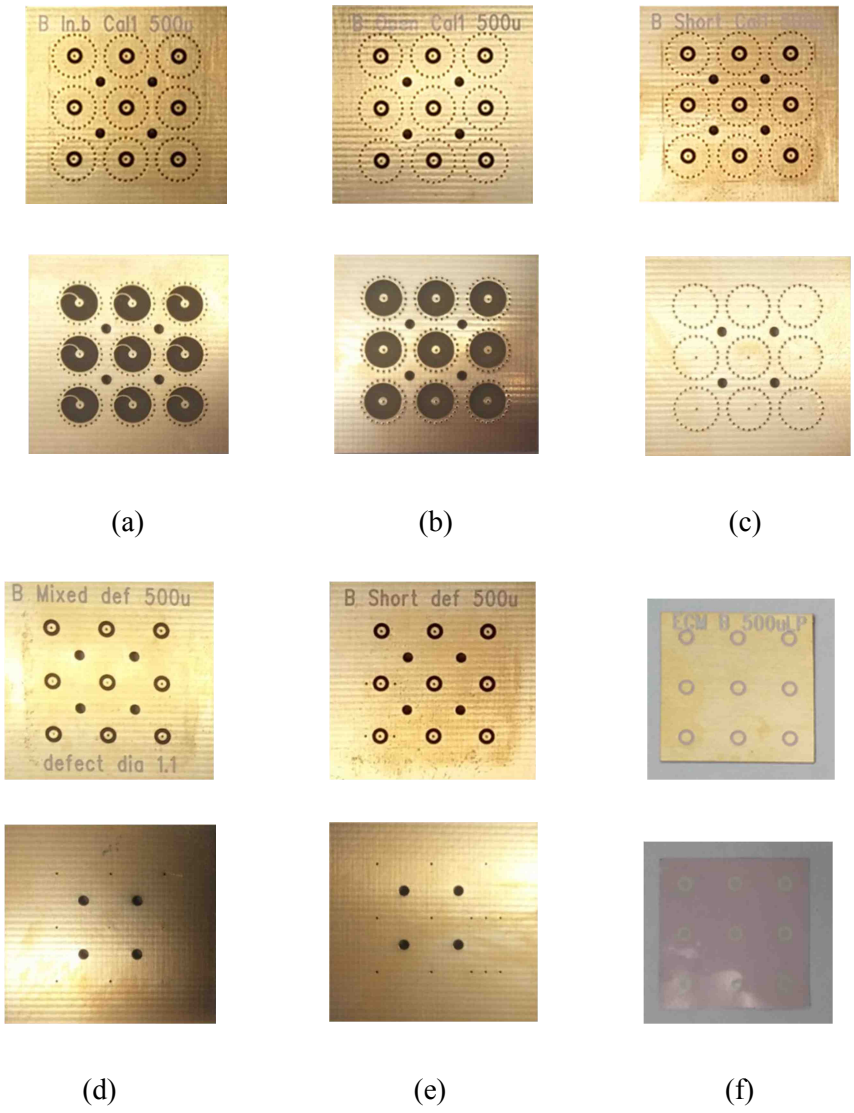
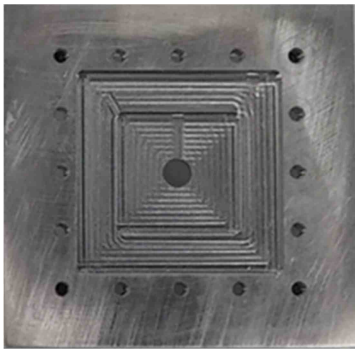
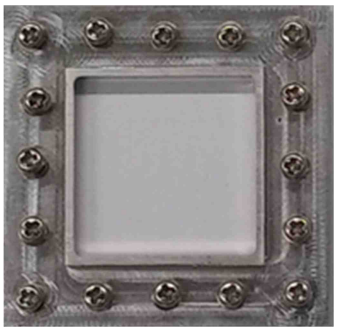


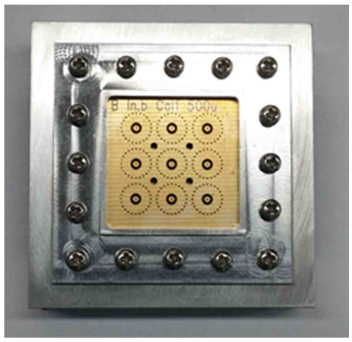
Fig. 3-13. Manufactured devices for measurements: (a) inductance pattern, (b) open-end and (c) short-end via calibration substrates, DUTs containing (d) open via defects and (e) short via defects, (f) the dielectric contactor (the top and the bottom surface of PCBs and the dielectric contactor are shown),



(g)

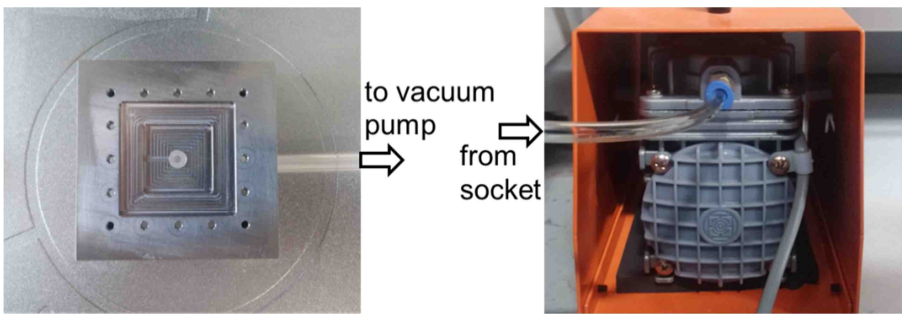


(h)



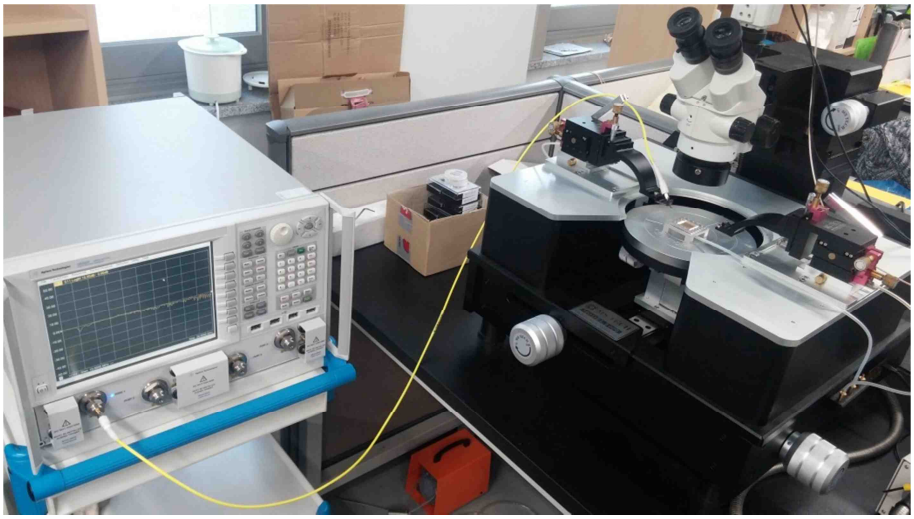
(i)

Fig. 3-13. (g) the socket and (h) the socket cover, (i) the assembled one (continued)

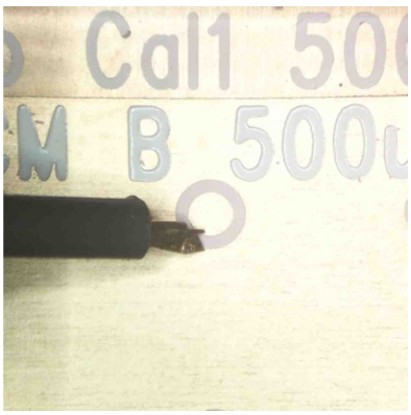


(a)

Fig. 3-14. Measurement setup for the proposed method: (a) the vacuum pump connection (b) measurement devices (c) the direct-contact probing (d) the indirect-contact probing

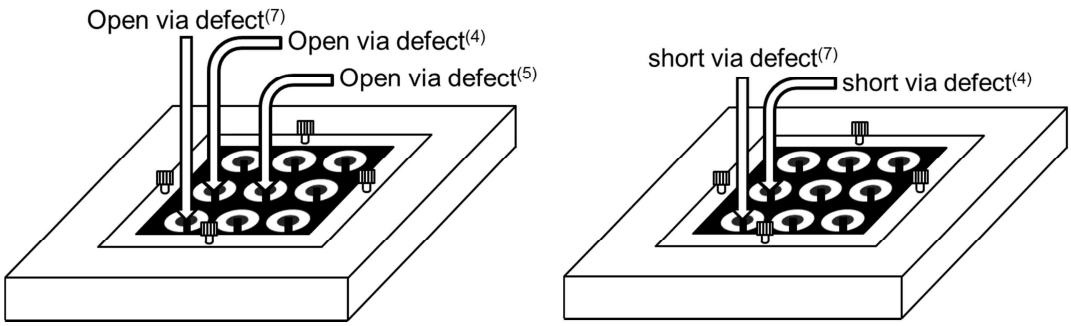


(b)



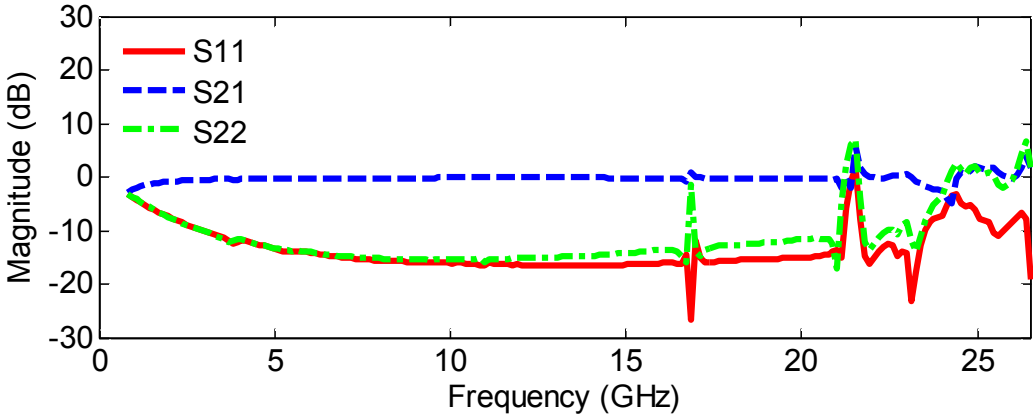
(c) (d)

Fig. 3-14. (continued)

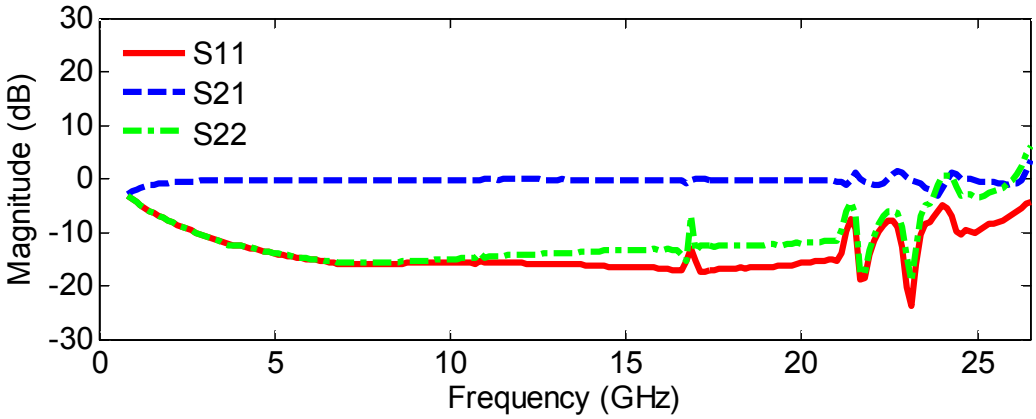


(a) (b)

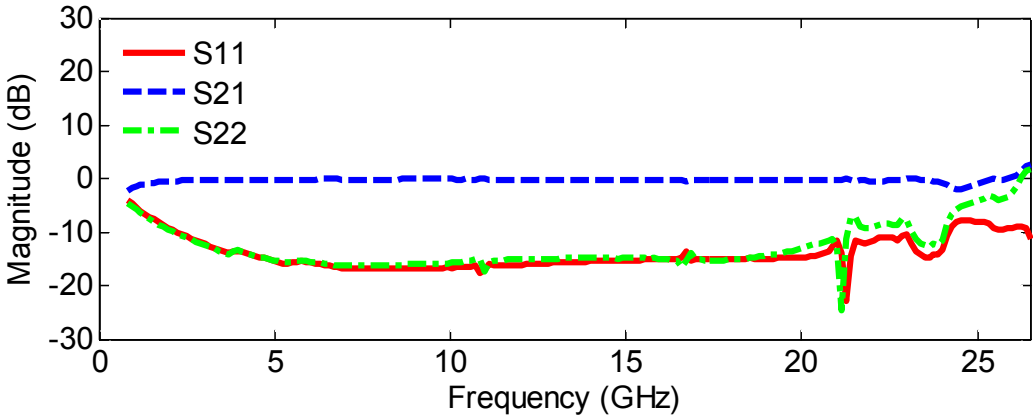
Fig. 3-15. Locations of via defects in each DUT: (a) the open via defects (b) the short via defects



(a) $[S]^{(1)}_{dcon}$

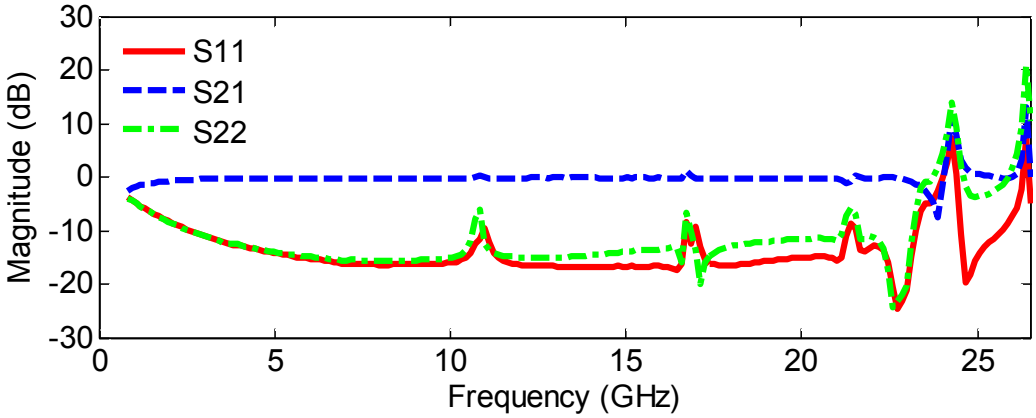


(b) $[S]^{(2)}_{dcon}$

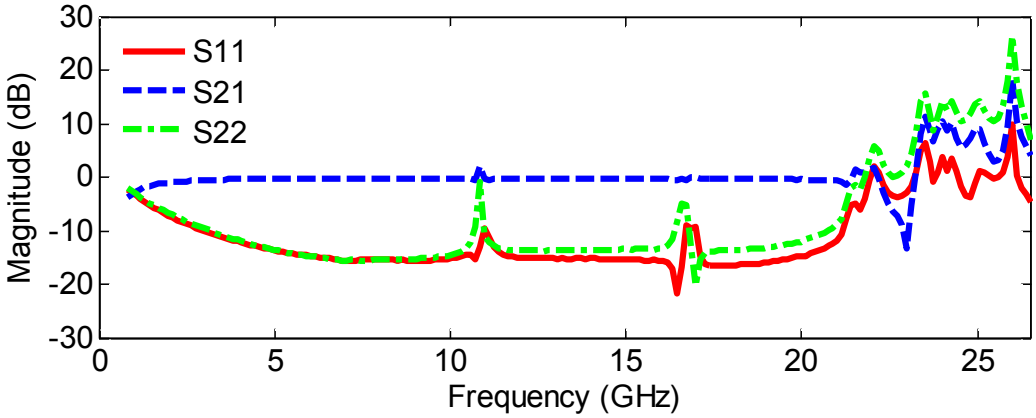


(c) $[S]^{(3)}_{dcon}$

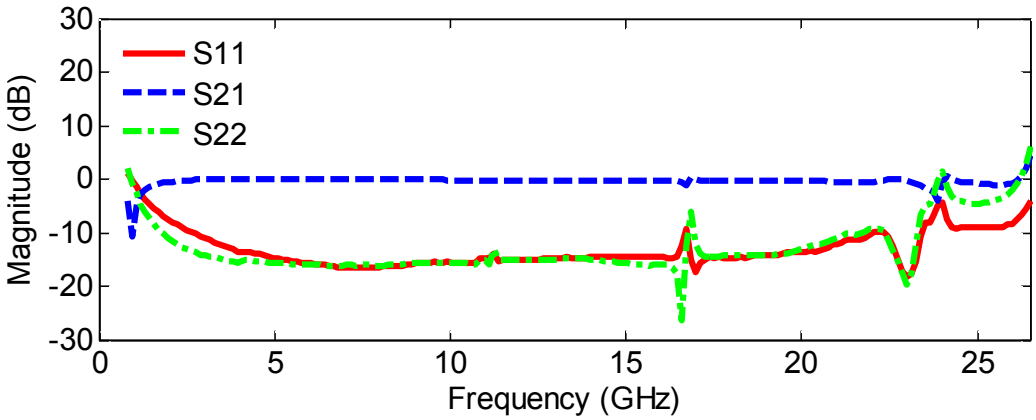
Fig. 3-16. Dielectric contactor characteristics



(d) $[S]^{(4)}_{dcon}$

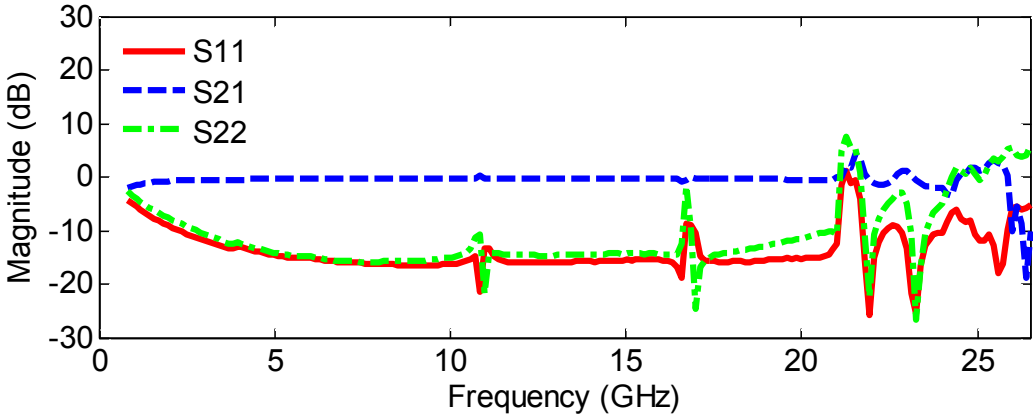


(e) $[S]^{(5)}_{dcon}$

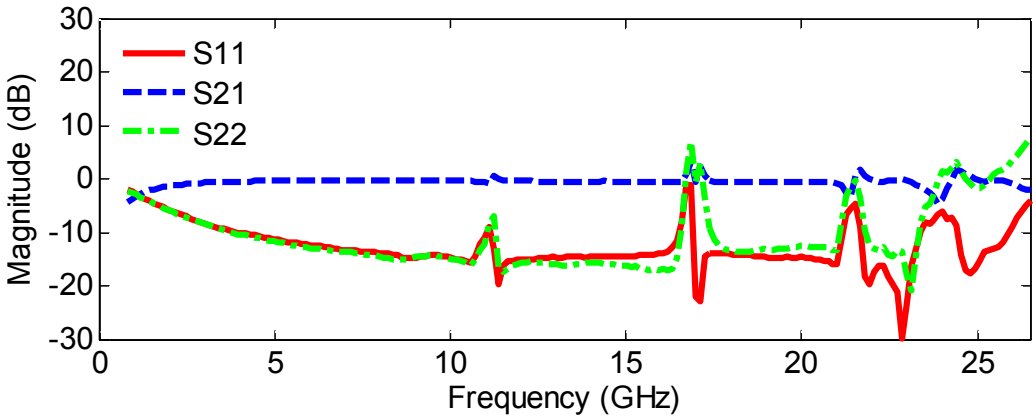


(f) $[S]^{(6)}_{dcon}$

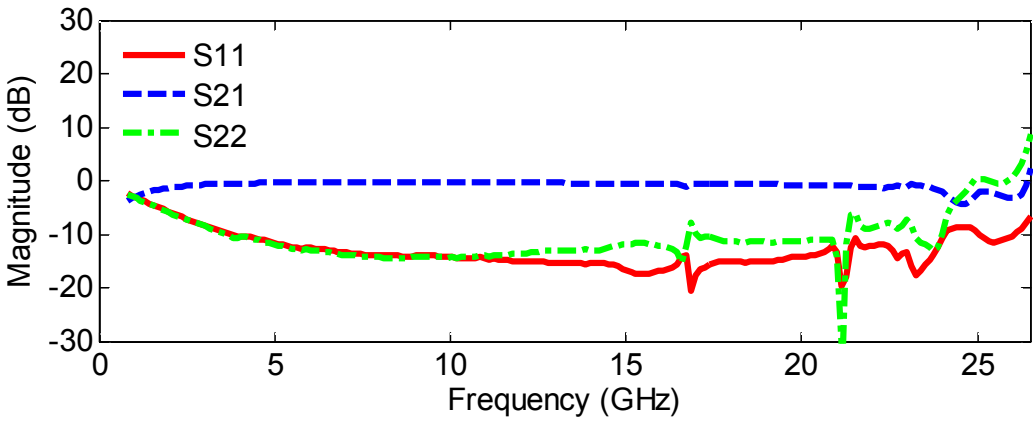
Fig. 3-16. (continued)



(g) $[S]^{(7)}_{dcon}$

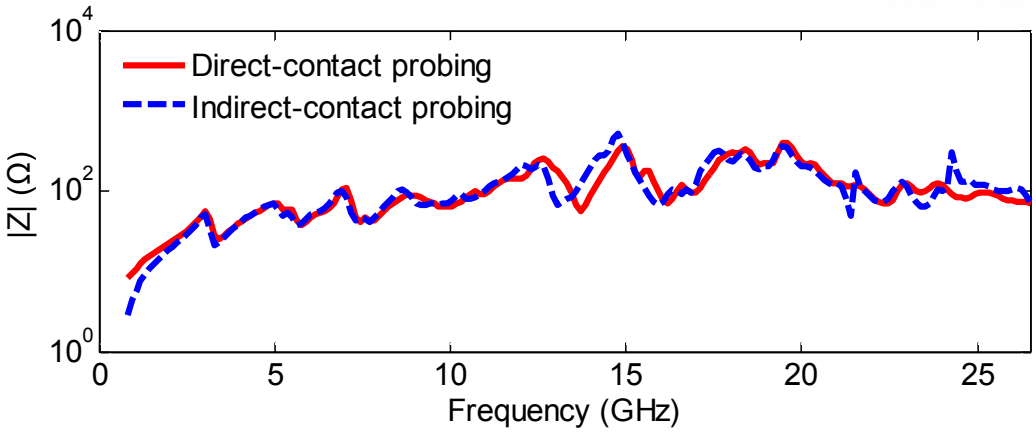


(h) $[S]^{(8)}_{dcon}$

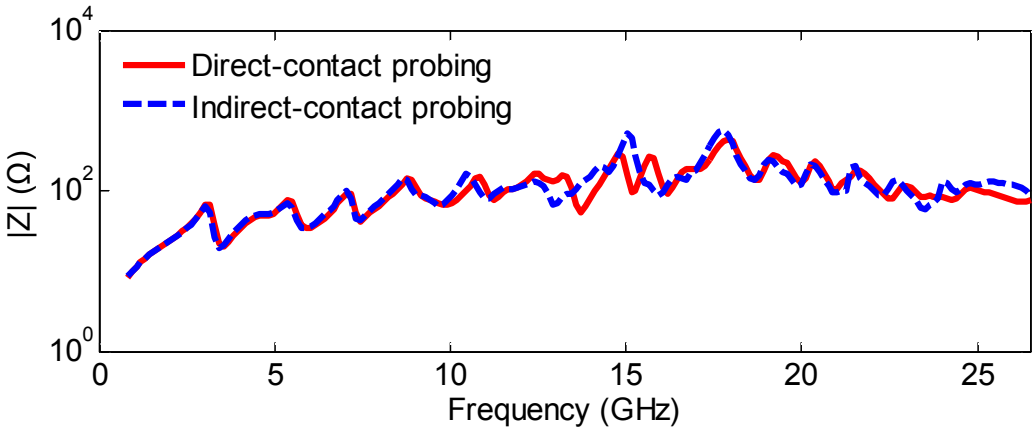


(i) $[S]^{(9)}_{dcon}$

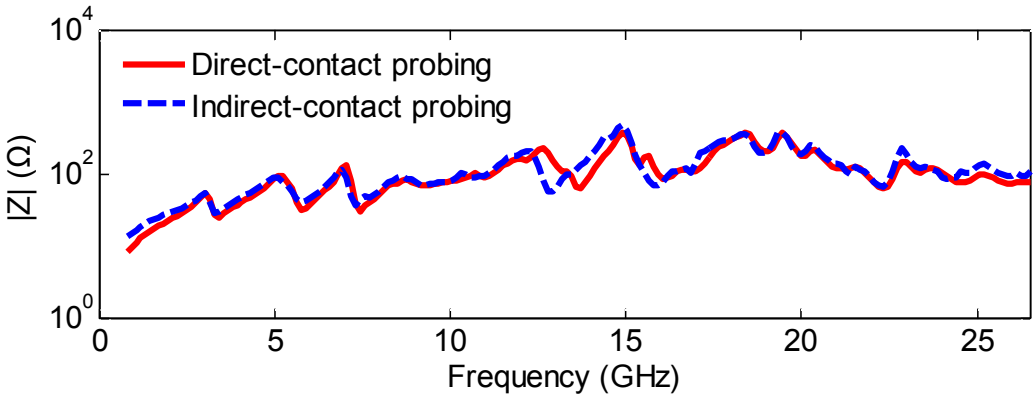
Fig. 3-16. (continued)



(a) via(1)

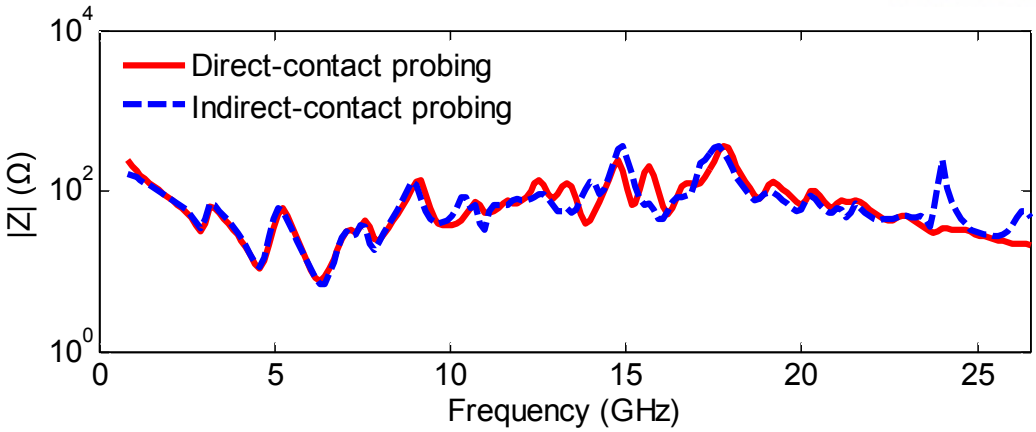


(b) via(2)

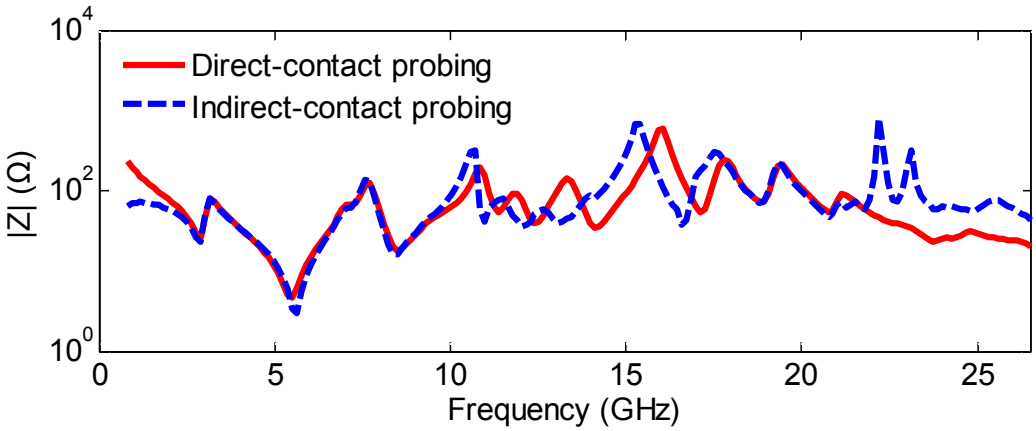


(c) via(3)

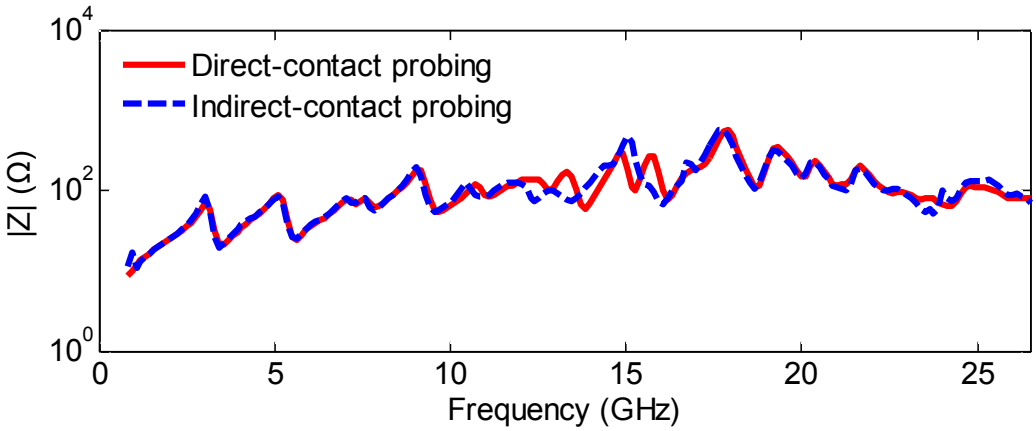
Fig. 3-17. Extracted impedances of the DUT containing open via defects



(d) via(4)

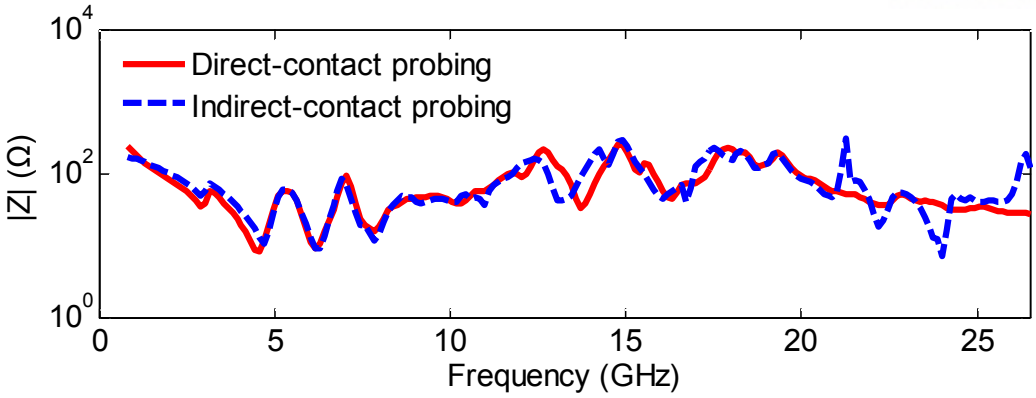


(e) via(5)

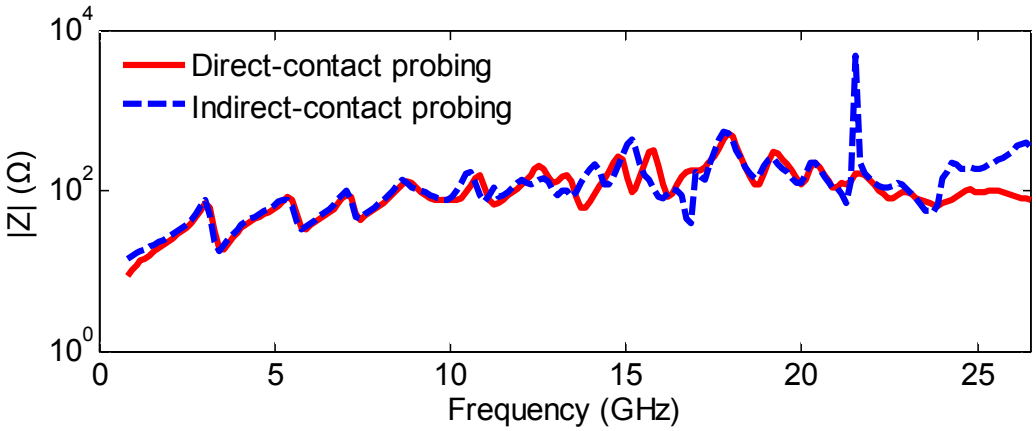


(f) via(6)

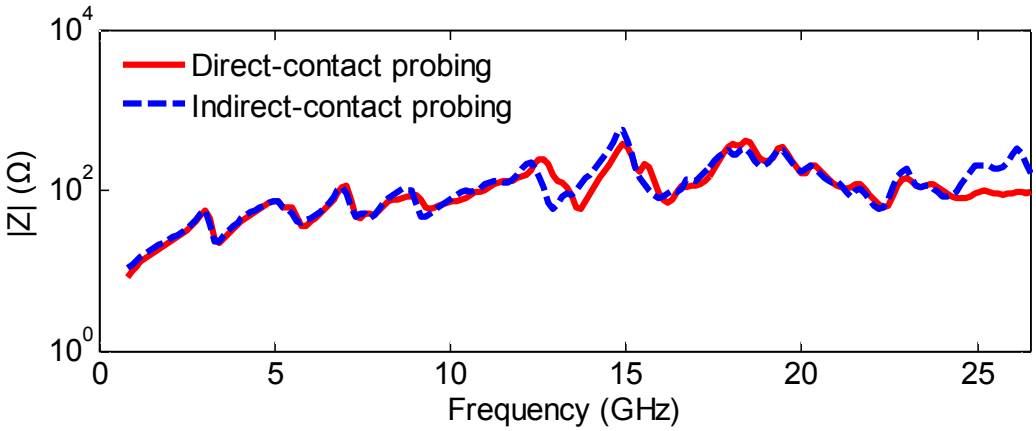
Fig. 3-17. (continued)



(g) via(7)

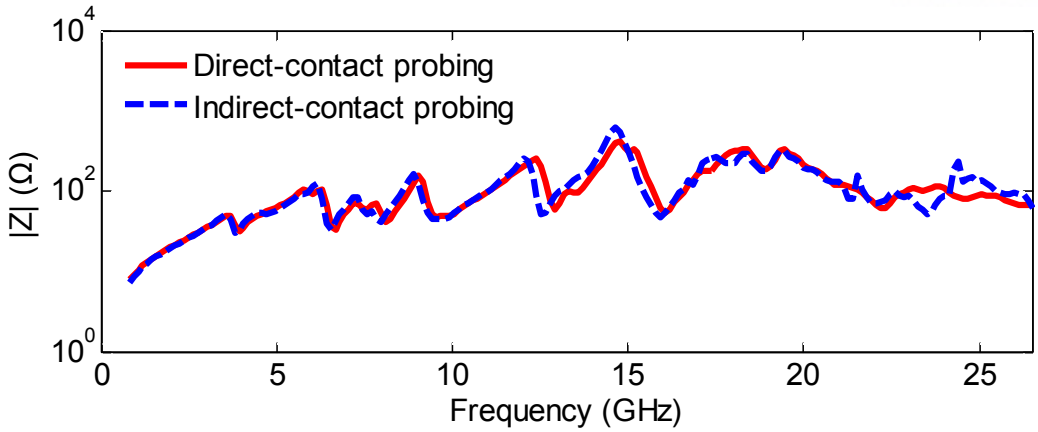


(h) via(8)

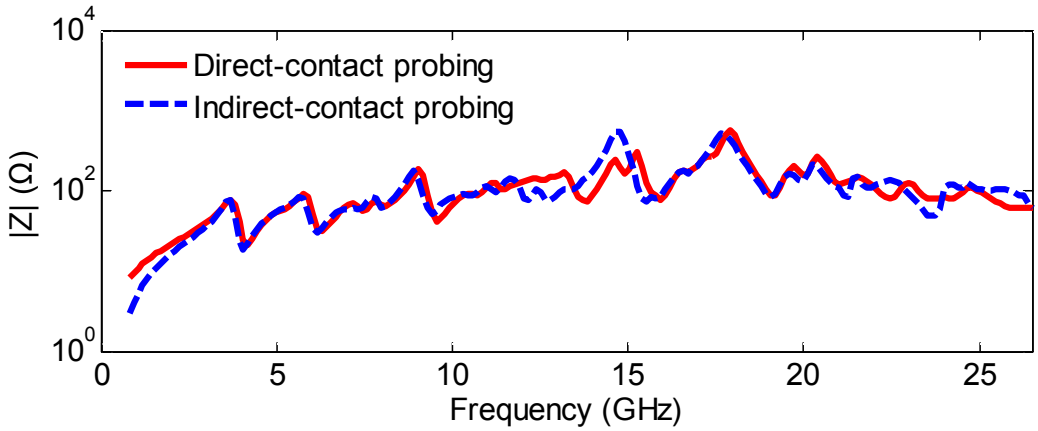


(i) via(9)

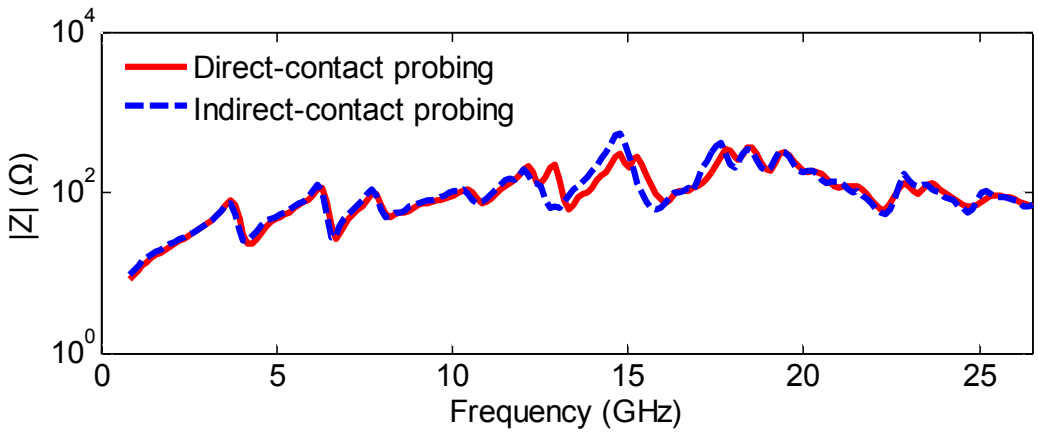
Fig. 3-17. (continued)



(a) via(1)

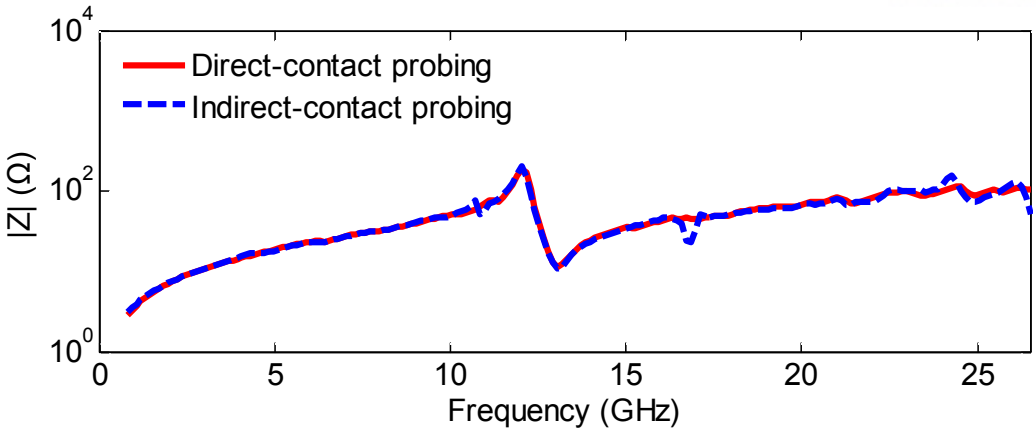


(b) via(2)

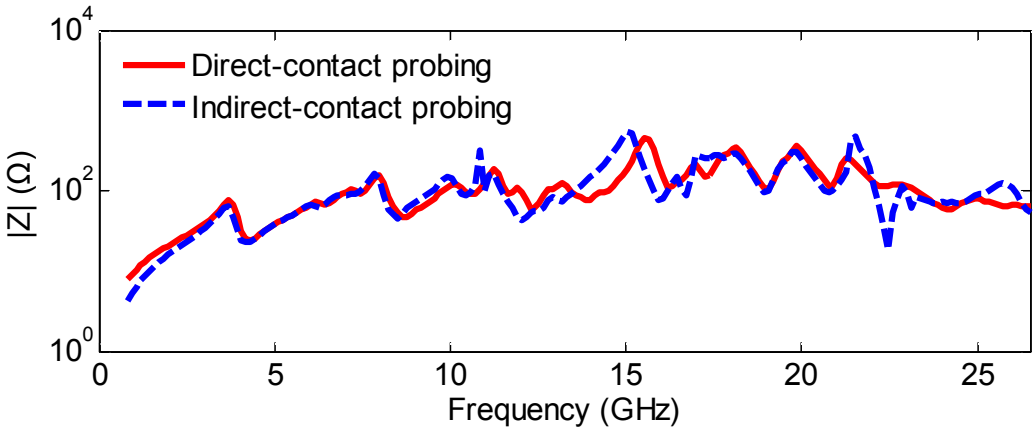


(c) via(3)

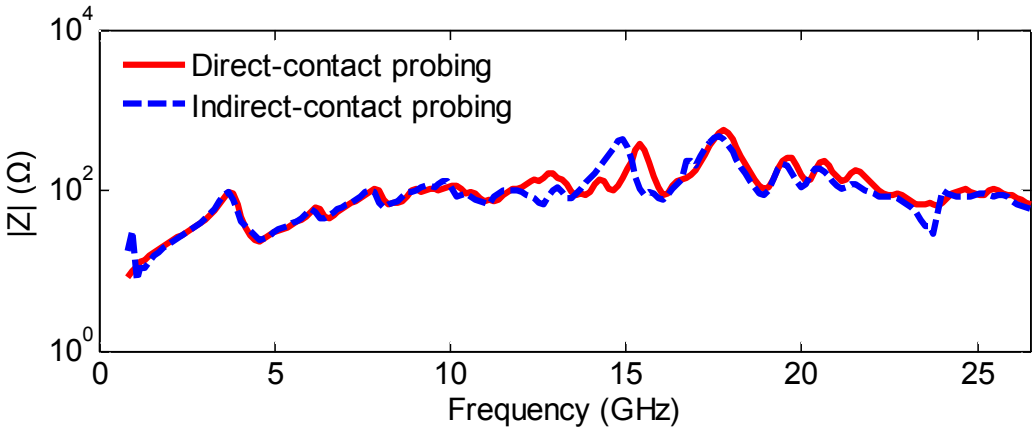
Fig. 3-18. Extracted impedances of another DUT containing short via defects



(d) via(4)

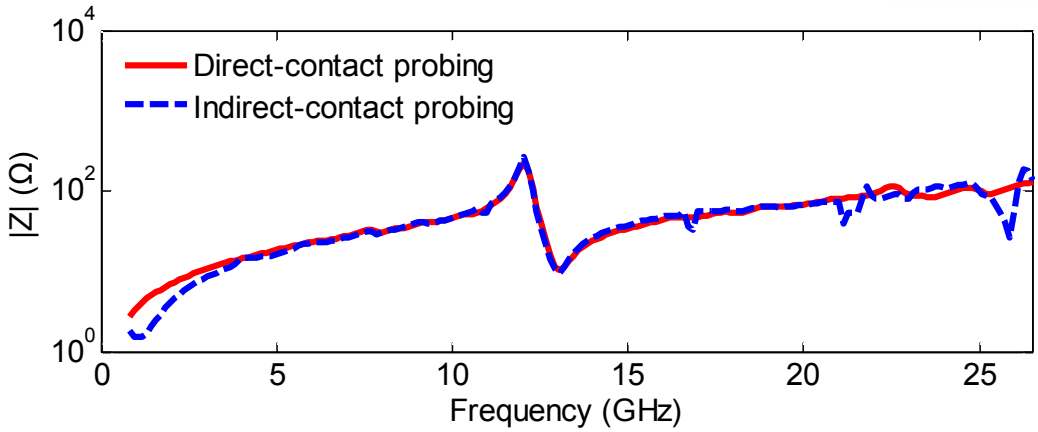


(e) via(5)

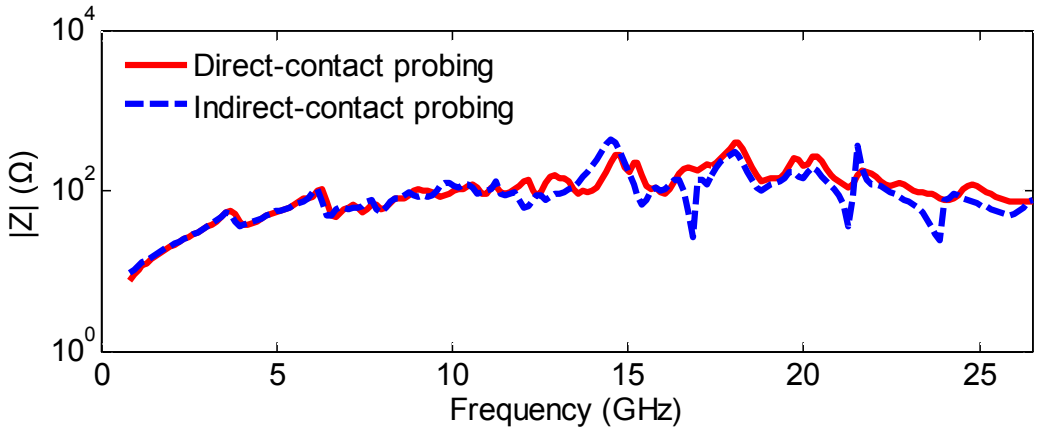


(f) via(6)

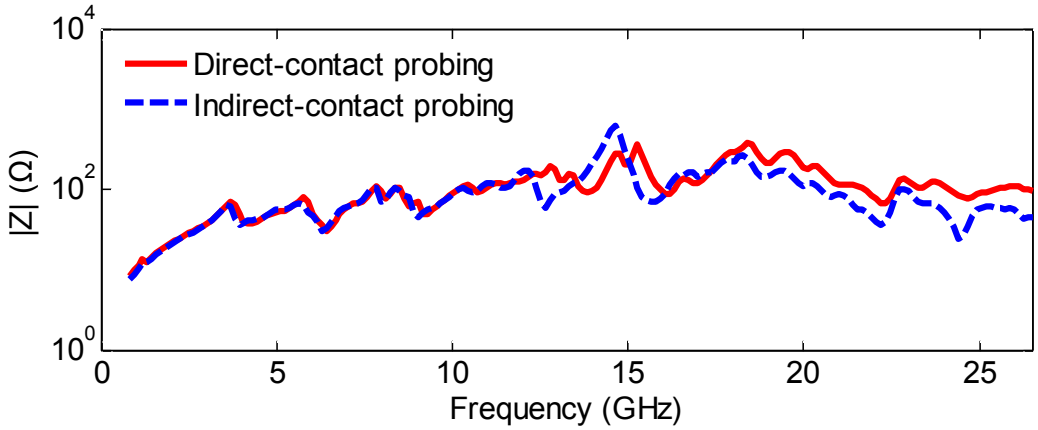
Fig. 3-18. (continued)



(g) via[7]



(h) via[8]



(i) via[9]

Fig. 3-18. (continued)

Chapter IV

Multi-port characterization of vias using indirect contact probing method

The indirect-contact probing method for multi-via test discussed in the previous section is limited to testing each individual via, since the method is based on the one-port extraction presented in Chapter II. In order to characterize the entire characteristics of multiple vias, the proposed method should be able to extract a multi-port network of multiple vias. From the extracted multi-port network, we can identify the inter-via couplings as described in Fig. 1-3(c). To apply general *n*-port network de-embedding, we can model the dielectric contactor and the DUT as series, as shown in Fig. 4-1. Each of them is expressed as a *S*-parameter matrices, where $[S]_{dcon}$ and $[S]_{DUT}$ are *S*-parameter matrices representing the dielectric contactor and the DUT characteristics, respectively. The matrix form of $[S]_{dcon}$ is defined as follows:

$$\begin{bmatrix} S_{\text{dcon I,I}} & S_{\text{dcon I,II}} \\ S_{\text{dcon II,I}} & S_{\text{dcon II,II}} \end{bmatrix} \tag{7}$$

, where $S_{\text{dcon I,II}}$, $S_{\text{dcon II,I}}$, $S_{\text{dcon I,II}}$, and $S_{\text{dcon II,II}}$ are the $n \times n$ sub-matrices of S_{dcon}. The cascaded *S*-parameter of the DUT can be calculated as:

$$[S]_{\text{DUT}} = \left([S]_{\text{dcon II,II}} + [S]_{\text{dcon II,I}} ([S]_m - [S]_{\text{dcon }I,I})^{-1} [S]_{\text{dcon }I,II} \right)^{-1} \tag{3}$$

, where $[S]_{\text{DUT}}$ is the extracted *S*-parameter of the DUT and $[S]_{\text{m}}$ is the indirect-contact measurement of *n*-port on the DUT. Assuming that the cross couplings of pads are negligible, $[S]_{dcon}$ can be obtained from the one-port calibration process. For simulation-based verification, we have extracted a two-port network between

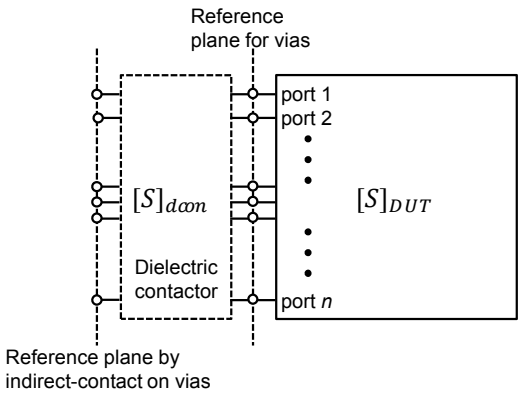
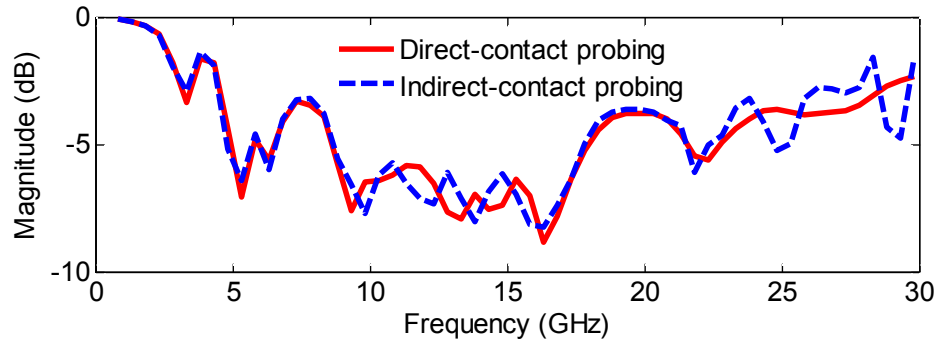
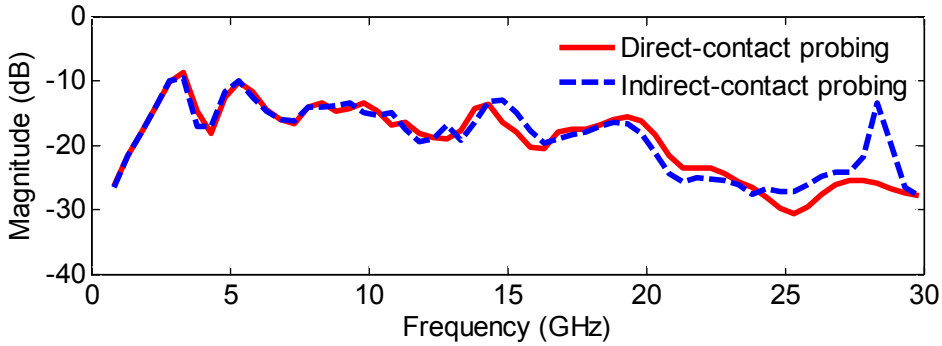


Fig. 4-1. General *n*-port network de-embedding

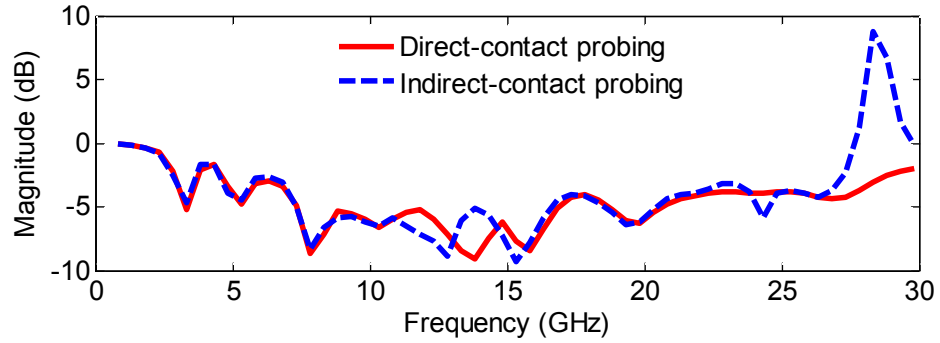
normal via(1) and normal via(2) in Fig. 3-15(a). The extracted s-parameters of the two-port network are shown in Fig. 4-2(a)-(c) and the inter-via coupling in Fig. 4-2(b). The extracted results show a good agreement with those obtained by the direct-contact probing in the frequency range 0.8 GHz to 24 GHz [21].



(a) S_{11}



(b) S_{21}



(c) S_{22}

Fig. 4-2. Extracted $[S]_{DUT}$ representing the scattering matrix of the two-port network between normal via(1) and normal via(2)

Chapter V

Conclusion

In this thesis, the indirect-contact probing method has been introduced to characterize vertical interconnects without damages from the direct contact probing. The key device of the proposed method is the dielectric contactor, which alleviates two issues on low sensitivity and via protection. In addition, the fine vertical control module and sensor electronics are omitted by providing the constant gap of the dielectric contactor. The proposed method has been verified in both cases of a single-pair vias extraction and multi-via testing based on simulations and measurements, successfully detecting all vertical interconnect defects. The proposed method for a single-pair vias has extracted the via impedances in the frequency range from 2 GHz to 18 GHz and for multi-via test from 2.5 GHz to 22 GHz both by measurements. The proposed method for characterizing the multi-port network of vias is also implemented. Based on simulations, the characteristics of the two-port network are successfully extracted to capture the inter-via coupling from 0.8 GHz to 20 GHz.

In reality, the proposed method should diagnose defects by probing all vertical interconnects at one time and be applicable in package and wafer-level. To achieve these, additional works are suggested. Firstly, the probe card design should be considered for fast testing. As described in Fig. 5-1, the probe card includes the dielectric contactor and multiple probe needles sharing the same ground plane. The probe card can be aligned by the parallel control module to cover a low frequency range, where the extraction is very sensitive on a pad alignment. Along with the control module, the vector network analyzer is connected to the probe card. Due to the fact that a multi-port VNA is not available, we can calibrate the DUT based on multiple two-port measurements [22]. Fig. 5-2(a) shows the N-port network of the DUT where the terms are connected. After characterizing a two-port *S*-parameter $[S]_{prob}$ representing the characteristics of the probe card with the dielectric contactor at each port, the impedance Z_{term} at the term can be calculated with the open-end termination on the top of the probe needle as shown in Fig. 5-2(b). After performing a two-port measurement on *i* th port and *j* th port, $[S]^{(i)}_{prob}$ and $[S]^{(j)}_{prob}$ are de-embedded as described in Fig. 5-2(c). VNA ports are normalized to $Z_{i,term}$ and $Z_{j,term}$ corresponding to each port. Based on that, we can fill the 2×2 sub-matrix in N×N scattering matrix of N-port DUT. Executing this procedure ${}_NC_2$ times on all ports, we can obtain the complete scattering matrix. Finally, it is renormalized to all 50 ohms for a standard form.

Secondly, the proposed method can be applied to vertical interconnects in package and wafer-level. Adopting a thin and high permittivity film, we can ensure required capacitive couplings as described

in Fig. 5-3. The probe card design should be also accompanied for a multi-port measurement. Due to micro-scale vertical interconnects, a probe card should be attached to a fine parallel control module. In addition, with the aid of mechanical support, the dielectric contactor can be properly pressed on the DUT without an air gap.

Finally, for better reliable characterization the proposed method should conduct further research. The SOLT calibration method for the probe has lower accuracy at high frequencies. Moreover, performing double calibration on the probe and the dielectric contactor, the accuracy drops even more. To address these issues, the total calibration method on the probe combined with the dielectric contactor is required. Therefore, by supporting calibration algorithm and a calibration kit, we can achieve the accurate calibration. Following the calibration issues, the sensitivity depending on the pad alignment, a thickness and dielectric constant of the dielectric contactor should be obtained. Based on the sensitivity data, we can design the dielectric contactor and its alignment system.

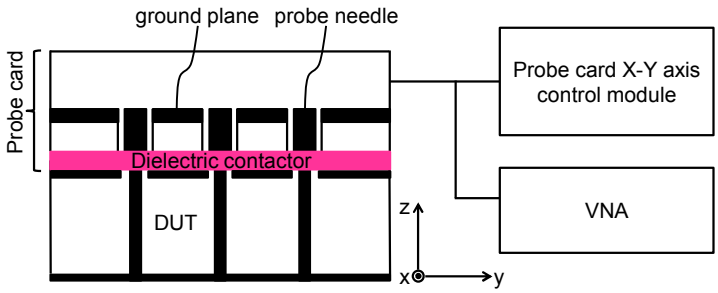
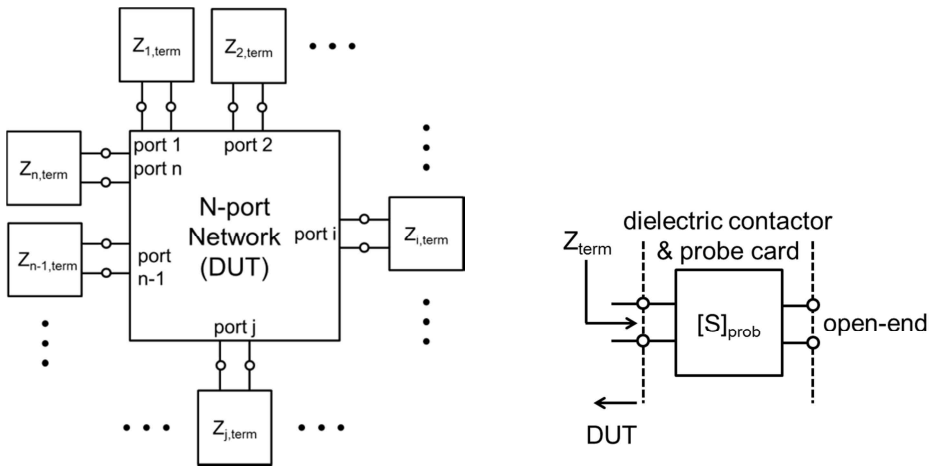
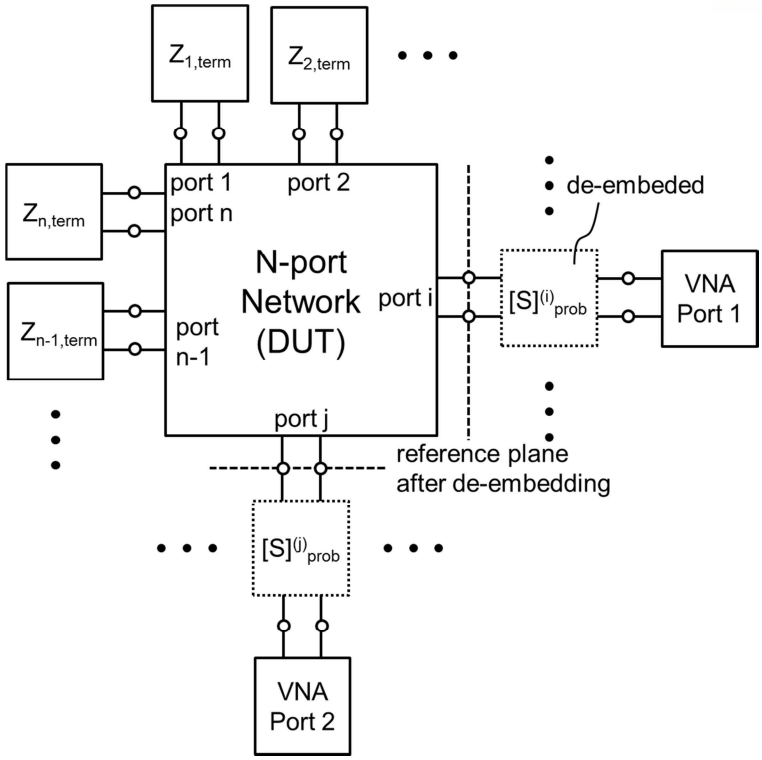


Fig. 5-1. Probe card designed for the indirect contact probing method



(a) (b)

Fig. 5-2. Multi-port indirect contact probing method based on two-port measurements: (a) the terms connected to the DUT (b) the characterization of the term



(c)

Fig. 5-2. (c) the procedure to obtain 2×2 sub-matrix in the complete N×N matrix (continued)

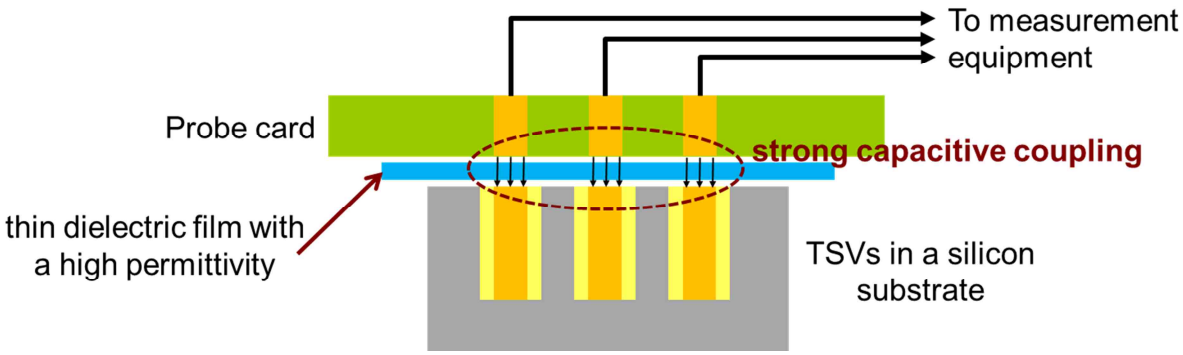


Fig. 5-3. Proposed method required for vertical interconnects in package and wafer-level

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