

On-chip interconnect boosting technique by using of 10-nm double gate-all-around (DGAA) transistor

Jaemin Lee¹, Myunghwan Ryu¹, and Youngmin Kim^{2a)}

¹ School of Electrical and Computer Engineering, UNIST,
UNIST-Gil 50, Ulsan 689–798, Republic of Korea

² Department of Computer Engineering, Kwangwoon University,
Gwangun-ro 20, Nowon-gu, Seoul 139–791, Republic of Korea
a) youngmin@kw.ac.kr

Abstract: Increasing short channel effects (SCEs) hinder further technology downscaling of CMOS transistors. Beyond the 10-nm technology node, the gate-all-around (GAA) FET is considered a promising solution for continuing Moore's law. In this study, we introduce a novel structure for speeding up the interconnect propagation using 10-nm channel length double gate-all around (DGAA) transistors. We propose a boosting structure that can significantly improve the performance of circuits by controlling the two gates of the DGAA independently. The proposed structure demonstrates that the propagation delay can be reduced by up to 30% for short interconnects and 47% for long interconnects. In high-speed, low-power IC designs, the proposed boosting structure gives circuit designers several options in the trade-off between power consumption and performance, which will play an important role in application-specific integration circuits in future GAA-based designs.

Keywords: gate-all-around (GAA), multi-gate transistor, interconnect, repeater, boosting technique, RC delay

Classification: Integrated circuits

References

- [1] Y. Taur and T. Ning: *Modern VLSI Devices* (Cambridge Univ. Press, New York, 2009).
- [2] ITRS 2013 edition, <http://www.itrs.net/>.
- [3] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neiryneck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki and K. Mistry: IEEE

- Symposium on VLSI Technology (2012) 131. DOI:10.1109/VLSIT.2012.6242496
- [4] H. M. Fahad and M. M. Hussain: Sci. Rep. **2** [2] (2012) 6. DOI:10.1038/srep00475
- [5] Y. Cao, T. Sato, M. Orshansky, D. Sylvester and C. Hu: Custom Integrated Circuits Conference, CICC (2000) 201. DOI:10.1109/CICC.2000.852648
- [6] D. Deschacht: Electrical Design of Advanced Packaging and Systems Symposium (2011) 1. DOI:10.1109/EDAPS.2011.6213729
- [7] P. Cocchini: IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **22** (2003) 1613. DOI:10.1109/TCAD.2003.819422
- [8] D. Pamunuwa and H. Tenhunen: 14th International Conference on VLSI Design (2001) 513. DOI:10.1109/ICVD.2001.902709
- [9] A. Nalamalpu, S. Srinivasan and W. P. Burleson: IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **21** (2002) 50. DOI:10.1109/43.974137
- [10] V. Adler and E. G. Friedman: IEEE Trans. Circuits Syst. II, Exp. Briefs **45** (1998) 607. DOI:10.1109/82.673643
- [11] C. Shin, X. Sun and T.-J. K. Liu: IEEE Trans. Electron Dev. **56** (2009) 1538. DOI:10.1109/TED.2009.2020321
- [12] F. Ana and Najeeb-ud-din: Int. J. Electron. Commun. Technol. **2** [4] (2011) 29.
- [13] B. Cheng, B. Maiti, S. Samavedam, J. Grant, B. Taylor, P. Tobin and J. Mogab: IEEE International SOI Conference (2001) 91. DOI:10.1109/SOIC.2001.958000
- [14] I. De, D. Johri, A. Srivastava and C. M. Osburn: Solid-State Electron. **44** (2000) 1077. DOI:10.1016/S0038-1101(99)00323-8
- [15] Sentaurus, ver. H-2013-03, <http://www.synopsys.com/>.
- [16] E. G. Friedman and M. A. El-Moursy: Integration, VLSI J. **38** (2004) 205. DOI:10.1016/j.vlsi.2004.04.001
- [17] Raphael reference manual, ver. H-2013.03, <http://www.synopsys.com/>.

1 Introduction

The scaling limits of CMOS technology make it difficult to follow Moore's law, thus requiring novel device structures to increase gate controllability and suppress short channel effects (SCEs) [1]. In ultra-scaled devices (i.e., below 32-nm), SCEs such as sub-threshold swing (SS) degradation, source/drain leakage current problems, larger drain-induced barrier lowering (DIBL), threshold voltage (V_{th}) roll-off, and V_{th} mismatch caused by random dopant fluctuations (RDF) limit further scaling. The increase in SCEs occurs primarily because of reduced gate controllability. Industry and academia have proposed a number of next-generation transistor candidates [2]. Among these candidates, multi-gate device topologies are considered a leading technology for further scaling. Recently, 22-nm technology has successfully adopted FinFETs, which are an example of multi-gate technology; they are expected to work for channel lengths down to 10 nm [2, 3]. Beyond 10 nm, the gate-all-around (GAA) FET is considered the most promising multi-gate technology. The GAA FET provides theoretically perfect electrostatic control of the channel, which enables further reduction in transistor size while maintaining low leakage currents and makes it highly attractive for low power applications [4]. A DGAA FET can be classified as either a shorted-GAA (SGAA) or an independent-GAA (IGAA) according to the inner gate bias. Circuit designers cannot

change the V_{th} value of the device because V_{th} is set by channel doping (the traditional way) or the applicable gate workfunction. However, the threshold voltage of the transistor can be modulated by controlling the separated gate terminal. Using the IGAA scheme in circuit design, designers can control the V_{th} value of the device, which provides more design options.

As the technology scales down, the obtained gain of active devices degrades because of an increase of interconnect propagation delays. More concerns arise for especially long interconnects [5]. Repeaters, which divide a long interconnect into shorter sections, have been proposed and have successfully resolved the problems by improving the interconnect delay [6, 7, 8, 9, 10]. However, repeaters generate other problems: finding the optimal number and size of the repeaters has been non-trivial and additional power and area is required.

In this study, a novel methodology to boost the signal propagation speed in repeaters using IGAA transistors in which the bias of each gate is controlled separately to obtain significantly better circuit performance is proposed and analyzed.

The remainder of the paper is organized as follows. Section II explains the 3D TCAD structure and the properties of the DGAA. The proposed boosting techniques are presented in Section III. Simulation results regarding performance and power consumption are discussed in Section IV, followed by conclusions in Section V.

2 Double Gate-All-Around (DGAA) transistor

The 3D TCAD structure used in this study is shown in Fig. 1. The nominal physical parameters used in the device simulations are summarized in Table I. The channel length (L_g) is 10 nm and (both inner and outer) gate oxide thickness (t_{ox}) is set to 1 nm. The radius of the silicon channel is 10 nm. The channel region is lightly doped at $1 \times 10^{16} \text{ cm}^{-3}$ (boron for n-type FET and arsenic for p-type FET) to reduce RDF effects and avoid mobility degradation [11], and the source/drain region is doped at $2 \times 10^{19} \text{ cm}^{-3}$ (arsenic for n-type FET and boron for p-type FET). A high-k metal-gate (HKMG) process, with tungsten and HfO_2 as a gate electrode and a gate dielectric, respectively, is used to construct the gate region. The workfunctions for NMOS and PMOS are calibrated to maintain a sufficiently high

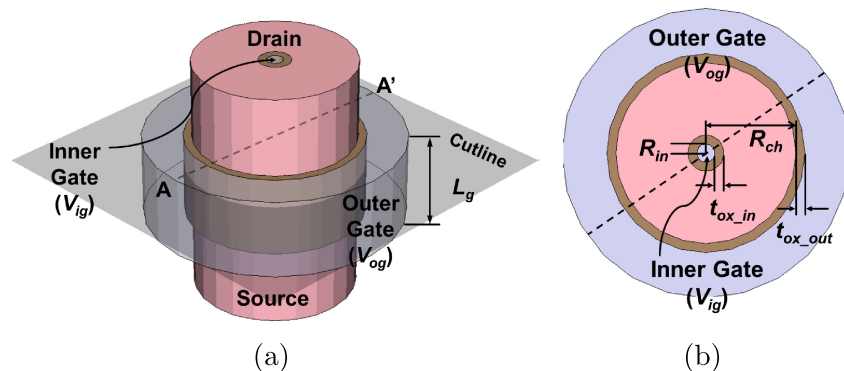


Fig. 1. DGAA FET structure used in device simulations in (a) bird's eye view and (b) cross-sectional view.

Table I. Physical parameters used in the device simulation

Parameters	Value
Channel length (L_g)	10 nm
Inner gate oxide thickness (t_{ox_in})	1 nm
Outer gate oxide thickness (t_{ox_out})	1 nm
Radius of the inner gate electrode (R_{in})	1 nm
Radius of silicon channel (R_{ch})	10 nm
Channel doping concentration	$1 \times 10^{16} \text{ cm}^{-3}$
Source/Drain concentration	$2 \times 10^{19} \text{ cm}^{-3}$
Supply voltage (V_{DD})	0.75 V
Gate material	Tungsten
Gate oxide material	HfO ₂
Workfunction (n-type)	4.5 eV
Workfunction (p-type)	4.8 eV

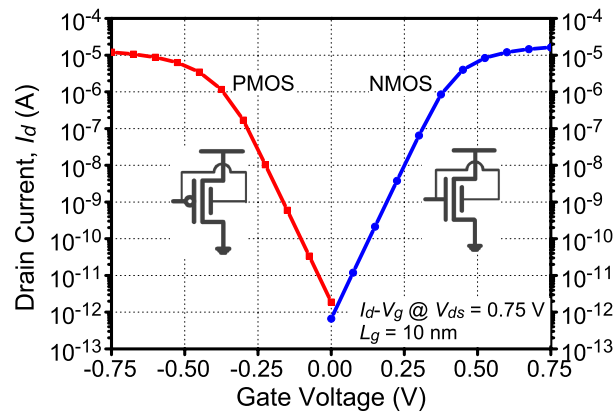


Fig. 2. I–V characteristics of the GAA NMOS and PMOS devices used in this study. The schematics used in the simulations are shown in the figure.

I_{on}/I_{off} ratio [12, 13, 14]. The $I_d - V_g$ curves of both transistors in shorted-gate mode (i.e., SGAA) at $V_{ds} = V_{DD}$ are plotted in Fig. 2. The supply voltage is set to 0.75 V according to the ITRS (International Technology Roadmap for Semiconductors) for 10-nm gate length [2]. The TCAD software, Sentaurus Device [15], is used to perform device-level and mixed-mode (e.g., transient) simulations.

The gate voltage is applied to create a conductive channel between the source and drain to allow current to flow in the transistor. In this study, V_{th} is set by the metal-semiconductor workfunction difference. When the inner gate and outer gate terminal are tied together and biased equally, they function together to induce a conductive channel. However, when the inner gate is biased differently from the outer gate, the metal-semiconductor workfunction will differ between the vicinity of the inner gate and outer gate region. In other words, V_{th} modulation can happen by separating the two gates using IGAA methods. Fig. 3(a) represents the threshold voltage for different inner gate bias (V_{ig}) values in the IGAA FET. As shown, the V_{th} value falls from 0.397 V to 0.214 V when V_{ig} rises from 0 V to 0.75 V. The

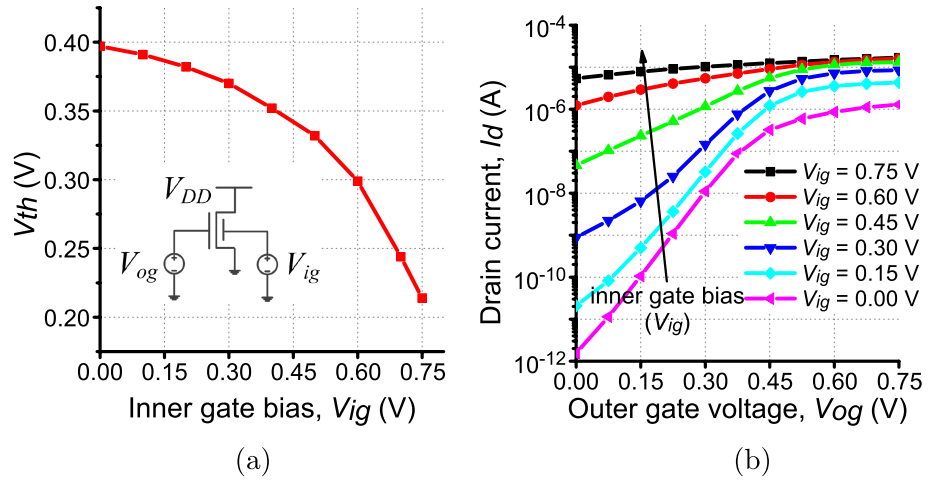


Fig. 3. (a) Threshold voltage modulation by introducing additional inner gate bias and (b) Drain current vs. outer gate voltage for various inner gate bias values. The test circuit used in the simulations is shown in the figure.

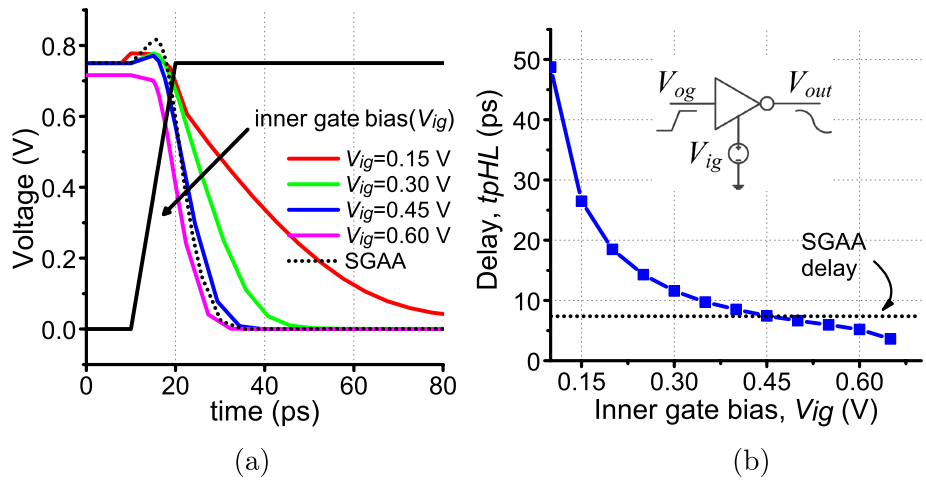


Fig. 4. (a) Transient graph of one IGAA inverter simulated at various inner gate bias values and (b) delay vs. inner gate voltage. The SGAA delay is also plotted as a reference. The circuit for the simulations is shown in the figure.

dynamic threshold voltage change in the IGAA transistors can provide additional options for circuit designers in terms of performance and power optimization according to the requirements of the integrated circuits. Fig. 3(b) shows the drain current (I_d) while increasing the inner gate voltage (V_{ig} in the n-type IGAA). As seen in the figure, the drain current increases dramatically when increasing the outer gate voltage V_{og} when V_{og} remains lower than the threshold voltage (e.g., ≤ 0.4 V). This phenomenon indicates that even though there is a large leakage current penalty, the increased drain current will boost the discharging for NMOS (charging for PMOS) capability of the transistor when V_{ig} is not tied together with V_{og} .

Fig. 4(a) shows the transient graph of single-IGAA inverter simulations for various inner gate (V_{ig}) bias values. As V_{ig} increases, the output decreases earlier in the high-to-low transition. The high-to-low propagation delays are measured for

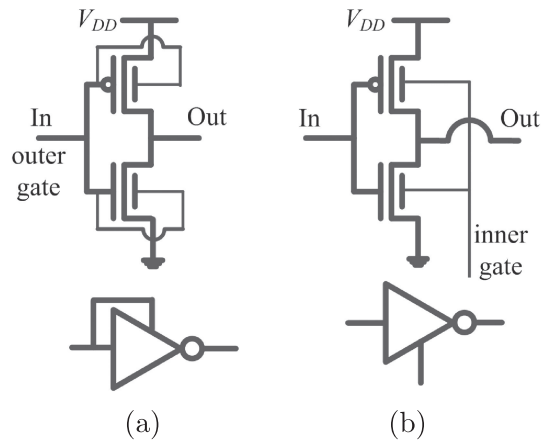


Fig. 5. Schematic and symbol of inverter using (a) SGAA and (b) IGAA.

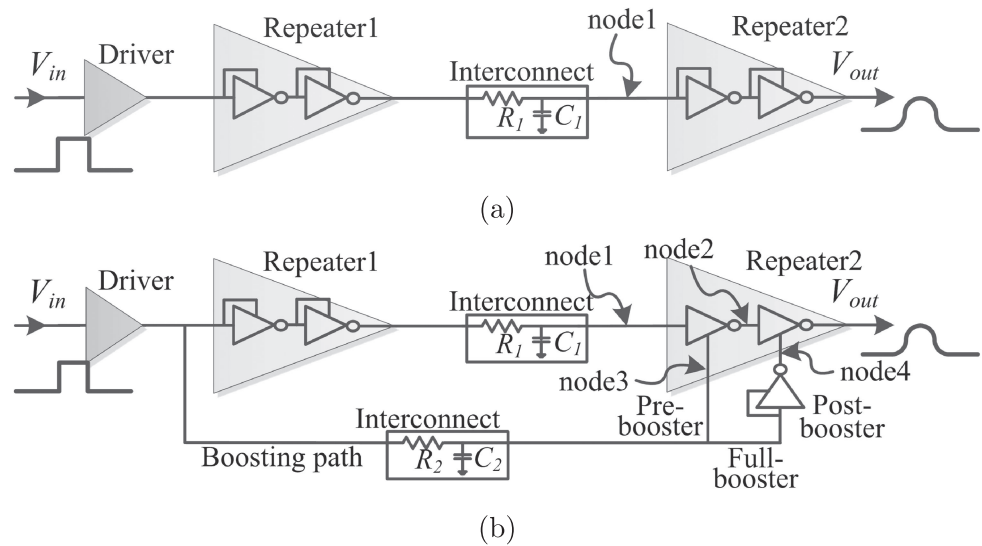


Fig. 6. Architecture of two repeaters in (a) the nominal case and (b) the proposed boosting technique.

increasing inner gate bias values in Fig. 4(b). As shown, the IGAA inverter is faster than SGAA when V_{ig} is larger than approximately 0.45 V. This result shows that the increasing V_{ig} can effectively lower the propagation delay.

3 Interconnect boosting technique

The schematics and symbols of (a) SGAA and (b) IGAA devices are shown in Fig. 5. There are two different gates (inner gate and outer gate) for both SGAA and IGAA. In case of SGAA, the inner gate and the outer gate are connected. The inner gate and outer gate are separated and controlled independently in IGAA.

The foregoing discussion demonstrates that by lowering the V_{th} value of one side of the gate, the signal can propagate through the transistor more quickly, and thus, improve the chip's performance. Particularly, following the input signal on its critical path, a boosting signal that is identical to the original input signal is routed to the inner gate of the IGAA device to lower V_{th} in advance. When distributing the digital signals inside the chip, the most popular design approach for reducing

propagation delay is to introduce intermediate repeaters in the interconnect line [6, 7, 8, 9, 10]. To decrease the interconnect delay in modern IC design, a long interconnect is divided evenly into smaller segments with repeaters inserted between each segment (each repeater is responsible for driving one segment). Thus, the timing transmission is significantly reduced [16].

A traditional two-repeater chain structure using SGAA that is employed regularly in driving a long chain of interconnects is depicted in Fig. 6(a). In the repeaters, two identical inverters are connected in series; each inverter consists of two parallel SGAA devices (for double size). Multiple GAA devices should be connected in parallel to size up the GAA structure because the width of one GAA device is pre-defined by the diameter of the GAA.

The proposed signal boosting technique is illustrated in Fig. 6(b). As shown, we develop a novel configuration that replaces the second repeater (Repeater2) with the IGAA device and keeps the first repeater (Repeater1) as an SGAA type. There are three possible boosting structures: the Pre-booster, in which only the first inverter of Repeater2 is IGAA type and where the inner gates are connected to the boosting path and the second inverter is normal SGAA without a boosting path; the Post-booster, in which only the second inverter of Repeater2 is IGAA type with a boosting path connection through the small SGAA to ensure proper polarity of the signal and the first inverter is normal SGAA type; and the Full-booster, in which both inverters of Repeater2 are IGAA type and the inner gates are connected to the boosting path directly. The driver is strong enough to drive both the repeater and the boosting path. We use five parallel SGAA inverters for the driver.

The operation of the proposed boosting technique is as follows. When the input signal (V_{in}) changes, the signal is propagated both through Repeater1 and the boosting path. When the signal arrives at node1 (the outer gate of the first inverter), the same logic value has already arrived at node3 (the inner gate of the first inverter) and it lowers the threshold voltage of the inverter. Thus, discharging via NMOS (or charging by PMOS) can occur faster than when there is no boosting path. Additionally, the signal with opposite polarity arrives at node4 (the inner gate of the second inverter) earlier than at the input of the second inverter (the outer gate, node2). Thus, when the signal reaches the input of the inverter, the transition can occur significantly faster than when not using the boosting path. The boosting path plays a supporting role and runs parallel to the critical path, or it can be routed in a shorter path. Hence, the length of the interconnect in the boosting path is comparable to the critical path.

4 Simulation results

In this study, segments of interconnect with a specific dimension (60 nm height, 30 nm width and space, and 2.2 dielectric constant assuming 22-nm nodes [2]) are inserted between repeaters. These segments are analyzed using the distributed RC model and the parasitics are extracted in [17]. The extracted resistance and capacitance are $12.2 \Omega/\mu\text{m}$ and $0.15 \text{ fF}/\mu\text{m}$, respectively.

Mixed-mode transient analysis is performed in 3D TCAD [15] to measure the propagation delay between the input signal (V_{in}) and the final output (V_{out}) through

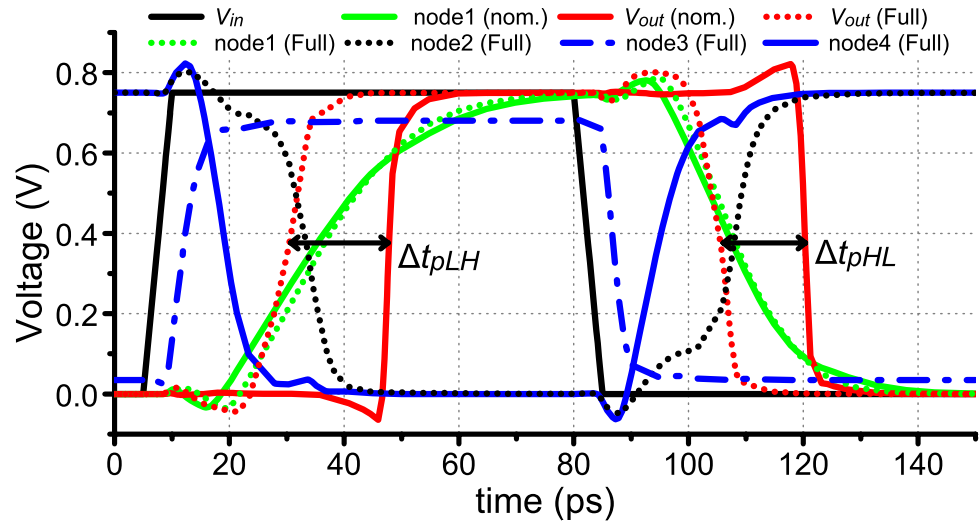


Fig. 7. Transient graph of nominal case and Full-booster.

the two-repeater structure for various interconnect lengths ranging from 1 μm to 10 μm . To evaluate our proposal, we compare the performance of all four repeater structures: SGAA without a boosting path (which is the nominal case), IGAA with a Full-booster (both Pre- and Post-booster paths in Repeater2), Pre-booster only, and Post-booster only.

The results of the transient analysis with mixed-mode TCAD simulations of the nominal case and the Full-booster case when the interconnect length is 5 μm are plotted in Fig. 7. As shown in the graph, V_{out} of the Full-booster rises 8.31 ps (Δt_{pLH}) earlier and falls 8.52 ps (Δt_{pHL}) earlier than the nominal case. As explained in the previous section, in the Full-booster, node4 (blue solid line, the inner gate of the second IGAA inverter) is already low so as to pull-up and start charging the output node before node2 (black dotted line) arrives for the low-to-high transition case. The rise time, however, is slower than that of the nominal case because only one side of the gate is driving the output load, instead of both gates together in the nominal case. The same phenomenon occurs for the high-to-low transition and the falling time.

Normalized average propagation delays (t_p) for a wide range of interconnect lengths are shown in Fig. 8. At short interconnect lengths (i.e., 1 μm), the Pre-booster and the Post-booster can reduce the delay by as much as 15% and 16%, respectively, and the Full-booster reduces it by approximately 30%. When the interconnect becomes longer (i.e., 10 μm), our proposed structure enhances the repeater's speed effectively as demonstrated by the 22%, 36%, and 47% reduction in propagation delay with the Pre-booster, the Post-booster, and the Full-booster technique, respectively.

To investigate the penalty on the driving capability caused by the single-side gate for IGAA in the boosting technique, normalized output slews (i.e., 20%–80% rising and falling time of V_{out}) are also compared as shown in Fig. 9. In case of the Pre-booster, the slew is comparable to that of the nominal case, because the last inverter, which is SGAA type, can recover the transition time of the output. However, high penalties on the slew rate are expected by the Post- and Full-

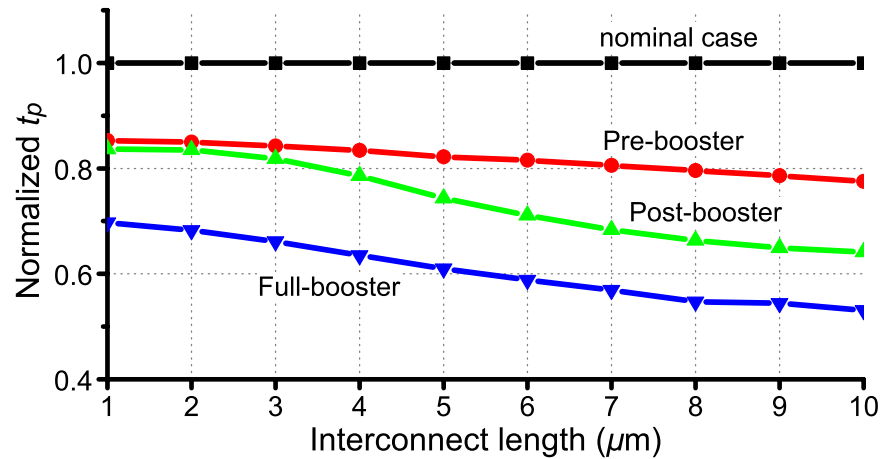


Fig. 8. Normalized average propagation delays (t_p) among various architectures.

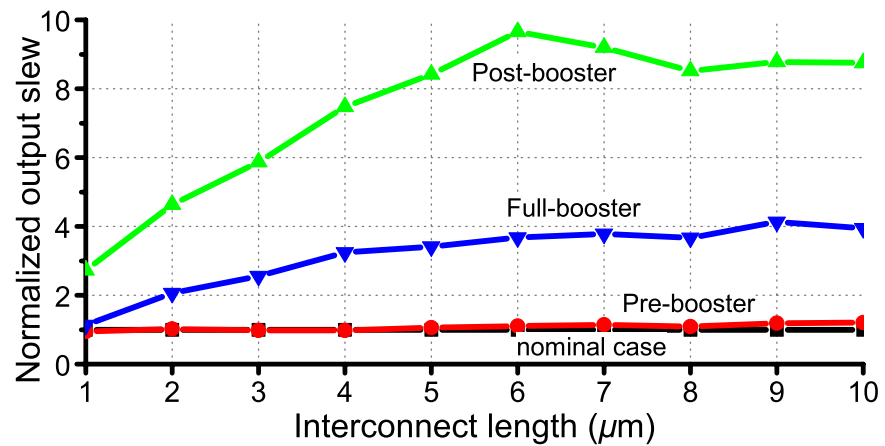


Fig. 9. Normalized output slews among various architectures.

booster because both inverters in the repeater are IGAAAs. For example, the output transition time becomes up to 10× and 4× longer than in the nominal case for the sake of propagation delay improvement in the Post-booster and the Full-booster architecture, respectively.

Normalized dynamic power consumptions for both transitions are compared in various architectures for a wide range of interconnect lengths, as shown in Fig. 10. In case of the Pre-booster, when the interconnect length is short (e.g., less than 4 μm), it consumes less power than the nominal case, because the transition slew (rise and fall time) of the first inverter in Repeater2 becomes slower in the boosting architecture. When the interconnect length is 10 μm , up to 3.5% more power is required than without the boosting path. In case of the Post- and Full-booster, there are similar power consumption penalties for all interconnect lengths because of the additional SGAA inverter and the boosting path. Up to 6% more power is required for the boosting technique when the interconnect length is 10 μm .

Even though the Full-booster is the best choice for maximum signal propagation speeds for long interconnects, the Pre-booster technique provides a good trade-off between performance (delay and slew) and power (or area) overhead.

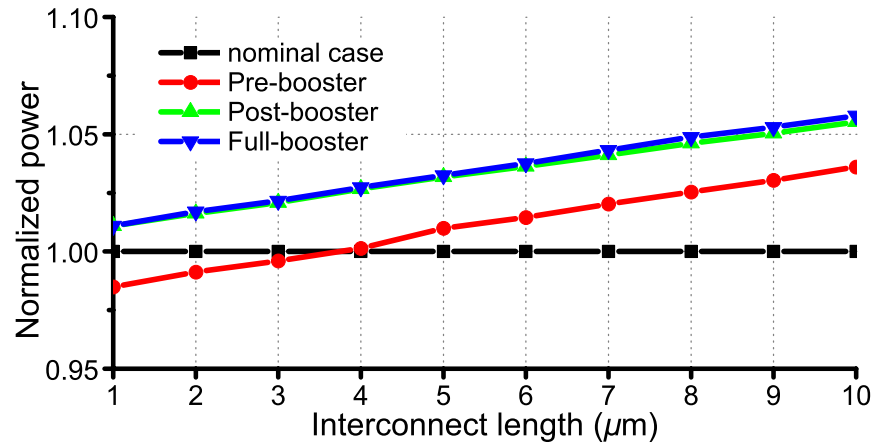


Fig. 10. Normalized average power among various architectures.

The proposed configurations have been proven to be effective solutions for driving the interconnect line in the range of 1–10 μm. To apply these boosting techniques to a longer interconnect line (e.g., longer than 100 μm), we need to assemble a number of the proposed structures in series such that each boosting structure transfers the signal through a shorter length of interconnect (1–10 μm). Clearly, the proposed boosting technique takes up a portion of the area inside the chip to route the boosting path and accommodate the additional inverter; thus, it consumes a certain amount of power. Therefore, depending on the requirements of a given application, circuit designers can select Pre-booster or Full-booster to speed up performance with minimal area (and thus, power) and routing overhead.

For example, the Full-booster technique is a good choice when increasing the propagation delay is the primary concern whereas the Pre-booster provides a reasonable improvement in terms of delay with a small impact on the slew and power consumption.

Simulation results are summarized in Table II. Table II shows the results when the length of the boosting path is the same as the interconnect length between repeaters (i.e., $R_1 = R_2$ and $C_1 = C_2$ in Fig. 6(b)). As shown in the table, additional

Table II. Simulation results (normalized) when the length of the boosting path is the same as the length between repeaters

length (μm)	nominal case			Pre-booster			Post-booster			Full-booster		
	delay	slew	power	delay	slew	power	delay	slew	power	delay	slew	power
1	1.00	1.00	1.00	0.85	0.95	0.98	0.84	2.72	1.01	0.70	1.14	1.01
2	1.00	1.00	1.00	0.85	1.02	0.99	0.83	4.64	1.02	0.68	2.06	1.02
3	1.00	1.00	1.00	0.84	0.98	1.00	0.82	5.87	1.02	0.66	2.56	1.02
4	1.00	1.00	1.00	0.83	0.98	1.00	0.79	7.48	1.03	0.64	3.25	1.03
5	1.00	1.00	1.00	0.82	1.06	1.01	0.74	8.42	1.03	0.61	3.41	1.03
6	1.00	1.00	1.00	0.82	1.11	1.01	0.71	9.65	1.04	0.59	3.68	1.04
7	1.00	1.00	1.00	0.81	1.14	1.02	0.68	9.19	1.04	0.57	3.78	1.04
8	1.00	1.00	1.00	0.80	1.09	1.03	0.66	8.52	1.05	0.55	3.67	1.05
9	1.00	1.00	1.00	0.79	1.19	1.03	0.65	8.78	1.05	0.54	4.13	1.05
10	1.00	1.00	1.00	0.78	1.20	1.04	0.64	8.75	1.06	0.53	3.94	1.06

delay reduction and smaller power penalties can be achieved when the boosting path routed is shorter. For example, when the interconnect length between repeaters is 10 μm , up to 47% speed increase with 6% additional power can be expected. The Pre-booster provides a good trade-off between speed (delay and slew) and power consumption whereas the Post-booster is not recommended because of its significant slew rate and power consumption degradation.

5 Conclusion

This paper introduced a novel methodology for speeding-up signal propagation in the critical path by utilizing 10-nm double-gate GAAs. By taking advantages of independent control of two GAA gates, we developed boosting structures that can significantly improve the IC performance. Without considering the power consumption, propagation delay simulation on a wide range of interconnects with repeaters shows up to a 47% speed increase using the Full-booster structure. Therefore, the proposed technique may play an important role in high speed ICs, especially because critical path delay lowers the overall performance of the chips. However, when prioritizing low power consumption, the Pre-booster, which provides a good trade-off between performance and power, is an alternative solution. In addition, the improvement in the propagation delay when using the proposed boosting technique can lower overall power usage and area of the chip by reducing the number of repeaters required in the interconnect paths.

Acknowledgments

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2014R1A1A2057715).