Effect of inclined quantum wells on macroscopic capacitance-voltage response of Schottky contacts: Cubic inclusions in hexagonal SiC

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Effect of inclined quantum wells on macroscopic capacitance-voltage response of Schottky contacts: Cubic inclusions in hexagonal SiC

K.-B. Park, Y. Ding, and J. P. Pelz[a)]
Department of Physics, The Ohio State University, Columbus, Ohio 43210-1106

M. K. Mikhov, Y. Wang, and B. J. Skromme
Department of Electrical Engineering and Center for Solid-State Electronics Research, Arizona State University, Tempe, Arizona 85287-5706

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Finite-element calculations of Schottky diode capacitance-voltage (*C-V*) curves show that an array of subsurface *inclined* quantum wells (QWs) produce negligible change in shape and slope of *C-V* curves, but significantly reduce the intercept voltage. This is particularly important for hexagonal SiC, in which current- or process-induced cubic inclusions are known to behave as electron QWs. These calculations naturally explain the surprisingly large effect of cubic inclusions on the apparent 4H–SiC Schottky barrier determined by *C-V* measurements, and together with the measured *C-V* data indicate the QW subband energy in the inclusions to be ~0.51 eV below the host 4H–SiC conduction band. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1935757]

We report finite-element calculations and measurements of capacitance-voltage (*C-V*) response of Schottky diodes when the semiconductor substrate has quantum wells (QWs) in an *inclined* geometry with respect to the metal/semiconductor interface, with sufficient density to deplete the host semiconductor of free carriers. In this case, free carriers are concentrated in the QWs, but can move freely toward the metal interface in response to an applied ac or dc voltage. This geometry is particularly relevant for hexagonal SiC, a wide band-gap semiconductor with great promise for applications in high-temperature, high-frequency, and high-power electronic devices. Basal-plane inclusions with local cubic "3C" stacking often form in hexagonal SiC during device operation[1,2] and/or processing[3–5] with an inclined geometry for most SiC surface miscut angles. These cubic inclusions have recently been shown to act as unique "structure-only" QWs (Refs. 6–8) which can deplete the surrounding hexagonal SiC host and strongly impact device performance. Since *C-V* measurements are commonly used for semiconductor characterization, it is important they be properly interpreted when inclusions are present. We find that calculated *C-V* curves for this inclined QW geometry have the usual linear shape (plotted as $1/C^2$ versus applied reverse bias V_r) and the same slope as for equally doped material without QWs, but with a shifted intercept voltage V_{int} that depends strongly on the QW energy depth ΔE_{QW} at the physical depth where the QWs start to accumulate free carriers. Hence, measured *C-V* curves can be used to quantify ΔE_{QW} at this depth, provided the QW spacing can be independently determined. Our calculations provide a natural explanation for the surprisingly large reported effect[4] of "double stacking fault" cubic inclusions on the apparent Schottky barrier height (SBH) determined by *C-V*, even though ~98% of the metal/SiC interface was unaffected by the inclusions.[8] Our measured *C-V* data indicate $\Delta E_{\text{QW}} \cong 0.51$ eV, in good agreement with an independent measurement of ΔE_{QW} close to the metal interface (~0.53 eV).[8]

Finite-element electrostatic modeling was done with the commercial software package FLEXPDE (Ref. 9) using the sample geometry shown in Fig. 1. We define the total electron potential energy in the host semiconductor (4H–SiC) as $\phi_{\text{tot-host}} = \phi(x,y,z) + E_{\text{SB-host}}$, where $E_{\text{SB-host}}$ is a constant equal to the host SBH at the metal interface. The total potential energy in the QWs is therefore $\phi_{\text{tot-QW}} = \phi_{\text{tot-host}} - \Delta E_{\text{QW}} = \phi(x,y,z) + (E_{\text{SB-host}} - \Delta E_{\text{QW}})$. The electrostatic potential energy $\phi(x,y,z)$ is determined by solving the Poisson equation $\nabla^2[\phi/(-q)] = -\rho(x,y,z)/\varepsilon_s\varepsilon_0$, where $\rho(x,y,z)$ is the net charge density inside the semiconductor, q is the elementary charge, ε_0 is the vacuum permittivity, and ε_s is the relative dielectric constant of the semiconductor. With these definitions the metal Fermi level is the reference energy, and $\phi(x,y,0) = 0$ along the metal interface. The net charge density is $\rho(x,y,z) = q[N_d - n_c(x,y,z)]$, where N_d is the donor density and n_c the free electron density. In the host semiconductor, n_c is given by:[10] $n_c \equiv (M_c/4)(2m^* k_B T/\pi\hbar^2)^{3/2} \exp[(E_{F,S} - \phi_{\text{tot-host}})/k_B T]$, where $E_{F,S} = -qV_r$ is the Fermi energy in the semiconductor with an applied reverse bias V_r, M_c is the number of equivalent host conduction-band minima, m^* is the effective electron density-of-states mass in the host, k_B is Boltzmann's

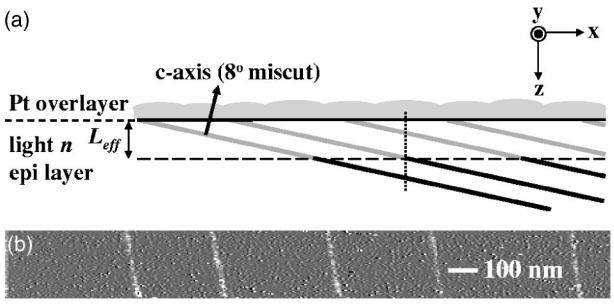

FIG. 1. (a) Schematic cross-sectional view of sample showing the 3C inclusions (gray+black lines) which start to fill with free carriers (electrons) at the depth L_{eff} below the interface, while the surrounding 4H area remains depleted even in the bulk. (b) BEEM image (taken with −1.5 V tip voltage) of a Pt/4H−SiC sample with embedded 3C inclusions. The bright straight lines show reduced SBH where the 3C QW inclusions intersect the metal/SiC interface. (More details are given in Ref. 8.)

[a)]Electronic mail: pelz.2@osu.edu

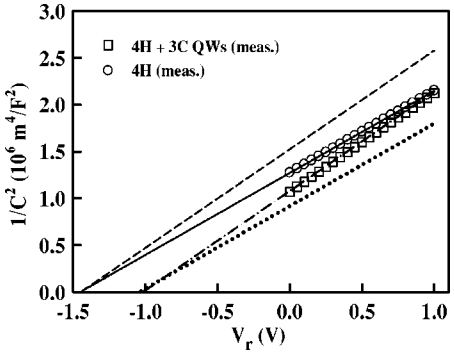

FIG. 2. Top two lines: Calculated *C-V* curves without QWs, with $N_d = 1.4 \times 10^{17}$ cm^{-3} (dashed line) and $N_d = 1.7 \times 10^{17}$ cm^{-3} (solid line), and parameter values from Table I. Changing N_d has little effect on the intercept voltage. Bottom two lines: Calculated *C-V* curves with inclined QWs present, with $\Delta E_{QW} = 0.50$ eV, $s_\perp = 95$ nm, parameters from Table I, and with $N_d = 1.4 \times 10^{17}$ cm^{-3} (dotted-dashed line) and $N_d = 1.7 \times 10^{17}$ cm^{-3} (dotted line). Introducing QWs strongly reduced the intercept voltage, but not the shape or slope of the calculated *C-V* curves. Changing N_d still has little effect on the intercept voltage. (○) Measured *C-V* data from a diode on the wafer periphery without inclusions. (□) Measured *C-V* data from Diode A from the central part of the SiC wafer with inclusions.

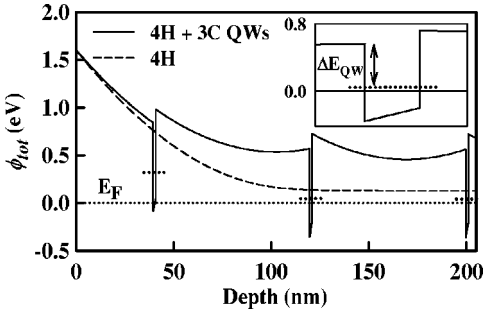

FIG. 3. Calculated electron potential energy profiles for Diode B along the particular path perpendicular to the metal/SiC interface shown as a dotted line in Fig. 1(a). The solid line represents the three-dimensional conduction-band minimum for bulk 4H- and 3C–SiC, while the horizontal dotted lines represent the two-dimensional conduction-band minimum of the QW states, including quantum confinement energy. The overall band bending is decreased with respect to pure 4H–SiC (dashed line) by charging of the QWs deep in the bulk, with a corresponding reduction in *C-V* measured SBH. Inset: Close-up view of QW profile around an inclusion.

constant, and $\hbar$ is the reduced Planck's constant. In the QWs, $n_c \cong \sigma_{QW}/d$, where $\sigma_{QW} \cong (M_c m_t^* k_B T/\pi\hbar^2) \ln[1+\exp\{(E_{F,S}-\phi_{tot\text{-}QW})/k_B T\}]$ is the sheet electron density in a QW,[11] and m_t^* is the QW in-plane effective density-of-states mass, and d is the QW width. The local surface charge density on the metal can be calculated as $\sigma_M(x,y,0) = \varepsilon_S \varepsilon_0 \partial(\phi/(-q))/\partial z|_{z=0}$, and *C-V* curves are calculated by monitoring how the average surface charge density depends on the applied bias. We include the effects of *spontaneous polarization* (SP) in the host semiconductor, which according to theory[12] and recent experiments[13,14] should exist in 4H–SiC, and would produce a strong electric field across any (nonpolar) cubic inclusions that would shift the QW conduction band relative to the 4H–SiC host. Our calculations assume that $E_{SB\text{-}host} > \Delta E_{QW}$, which is true for all cubic inclusions in the SiC system and for most other QW systems as well.

The central result of these calculations is illustrated in Fig. 2. The top two curves are calculated *C-V* curves for a sample *without* QWs, using identical parameters except for somewhat different donor density. As expected, the calculated *C-V* curves are straight lines with a slope that depends on the doping, but with an intercept voltage almost independent of doping.[10] As a check, we analyzed these calculated *C-V* curves in the conventional way,[10] and extracted values for N_d and $E_{SB\text{-}host}$ that are (as expected) identical to the respective parameter values used to calculate the *C-V* curves.

The bottom two curves in Fig. 2 were calculated with the same parameters, but now with inclined QWs with a certain average spacing $s_\perp$ in the bulk and each with the same QW depth ΔE_{QW}. In this case, the two calculated *C-V* curves are still straight lines with the *same respective slopes* as the *C-V* curves without QWs, but with the intercept voltages shifted by essentially the same amount for both curves. This shift depends strongly (almost linearly) on ΔE_{QW}, but depends weakly on $s_\perp$. At first glance, it is surprising that the shape and slope of the *C-V* curves do not change, since the QWs greatly alter the free carrier distribution. But since the QWs are inclined with respect to the sample surface, free carriers in the QWs can quickly respond to an applied ac or dc voltage, producing a *C-V* response that *mimics* a uniform material of the same doping but with a much lower Schottky barrier height. To understand this, we note that in *uniform* material the measured capacitance under reverse bias is determined by the *depletion width L*, which terminates at the physical depth where the host conduction-band minimum approaches $E_{F,S}$ and accumulates sufficient free carriers to screen the fixed donor charge. In contrast, with inclined QWs the measured capacitance is determined by an "effective" depletion width L_{eff} [see Fig. 1(a)], which is approximately equal to the physical depth *where the conduction band of the QWs approach* $E_{F,S}$ and accumulates sufficient carriers to *effectively* screen the fixed donor charge in the surrounding host material.[15] This is illustrated in Fig. 3. Since the QW conduction band has lower energy than that of the host, it reaches $E_{F,S}$ at a shallower depth L_{eff} than for the uniform material, producing a *larger capacitance*, and hence a *smaller intercept voltage*. But the shape of the *C-V* curve remains the same since it is still the host donor density N_d that determines how much L_{eff} must change when V_r is changed. We emphasize that the shifted intercept voltage is *not due to any change in the metal/semiconductor interface*. In fact, the calculated *C-V* curves would be the same even if the QWs happened to terminate just below the metal interface, since no free carriers exist in the QWs (or in the host) close to the metal interface.

We next compare these calculations with measured *C-V* data from regions of a 4H–SiC wafer with subsurface cubic inclusions (which are confirmed to behave as QWs)[8] inclined ~8° to the sample surface. These samples had a 2 μm lightly *n*-type N-doped epilayer (with specified $1-2 \times 10^{17}$ cm^{-3} doping) on a heavily N-doped ($\sim 3 \times 10^{19}$ cm^{-3}) *n*-type Si-face substrate.[4,8] Double stacking fault cubic inclusions formed in the substrate during a 90 min thermal oxidation[4] at 1150 °C, many of which extended through the epilayer to the sample surface [see Fig. 1(a)]. Samples were stripped of their oxide, cleaned and introduced into our UHV chamber.[8] An ~8 nm thick Pt film was then electron-beam evaporated through a shadow mask to form 0.5 mm-diameter Schottky diodes. For comparison, similar Pt Schottky diodes were made on a piece of the same SiC wafer close to the wafer periphery, where no inclusions

TABLE I. The parameter values from the literature (citation in parentheses) used in finite-element electrostatic modeling.

m^* (Ref. 17)	m_t^* (Ref. 7)	ε_s (4H and 3C, Ref. 18)	M_c (Ref. 17)	d (Ref. 7)	SP (Ref. 13)
0.39 m_0	0.36 m_0	9.7	3	1.25 nm	1.1×10^{-2} C/m^2

Note: m_0: Free electron mass. SP: Spontaneous-polarization.

formed.[4] The *C-V* measurements were done *in situ* after Pt deposition.

The open circles in Fig. 2 show measured *C-V* data from the SiC wafer periphery (without inclusions). These data were fit to a straight line (not shown) from which were extracted the SBH $E_{\text{SB-host}} \cong 1.60$ eV and local epifilm doping $N_d \cong \sim 1.7\times10^{17}$ cm^{-3}. The solid line through the open circles is the calculated *C-V* curve based on the measured $E_{\text{SB-host}}$ and N_d, which as expected matches the measurements exactly. Literature values were used for m^*, m_t^*, ε_s, M_c, d, and SP in all calculations here (see Table I). The *C-V* measured Barrier height is consistent with the ~1.54 eV barrier height measured independently on the same diode using ballistic electron emission microscopy (BEEM),[8] after accounting for the expected ~78 meV "image force lowering"[10] of the BEEM-measured barrier height for that doping level.

The open squares in Fig. 2 show *C-V* data measured from a Schottky diode with inclusions (denoted as "Diode A") from a wafer piece close to the wafer center. These data were fit to a straight line (not shown) which was analyzed in the conventional way to estimate the local doping $N_d \cong \sim 1.4\times10^{17}$ cm^{-3} on this part of the wafer. Since the inclined QWs do not change the slope of the *C-V* curves (as discussed above), they can still be used to determine the local epifilm doping. Using this value of N_d and $E_{\text{SB-host}} \cong 1.60$ eV, we then calculated *C-V* curves using various values for ΔE_{QW} and the perpendicular QW spacing $s_\perp$. These calculated *C-V* curves all had the same slope as the measured *C-V* curve, but with shifted intercept voltages which depend strongly on ΔE_{QW} and weakly on $s_\perp$. We note that the measured doping on the sample with inclusions (from the wafer center) is somewhat less than that measured on the sample taken from the SiC wafer periphery. We do not think this difference is significant since variations in doping across a wafer are common, and since the calculations indicate that the *change* in intercept voltage of *C-V* curve due to inclined QWs is nearly independent of doping.

Our modeling suggests that we could use measured *C-V* data to determine the QW energy ΔE_{QW}, provided we have an independent measurement of the average perpendicular separation $s_\perp$ between the QWs. Accordingly, we measured $s_\perp \cong 95$ nm on Diode A by using BEEM to directly image and count individual inclusions [see Fig. 1(b) and Ref. 8], sampling ~10% of the diode diameter along a line perpendicular to the inclusions.[16] Since all parameter values, except ΔE_{QW}, are known from the literature or from direct measurement (see Table I), we varied ΔE_{QW} until the calculated *C-V* curve best fit the measured data, as shown by the calculated dotted-dashed line through the open-square data points in Fig. 2. This *C-V* curve was calculated with the best fit value $\Delta E_{\text{QW}} \cong 0.50$ eV. We also made similar measurements (not shown) on another diode (Diode B), which had ~50 mV smaller intercept voltage in measurement, and also had a slightly smaller measured average inclusion spacing of $s_\perp \cong 79$ nm. In this case, the best fit QW energy depth was $\Delta E_{\text{QW}} \cong 0.52$ eV, close to the best fit value for Diode A. We note that spontaneous polarization in 4H–SiC *was* included in these calculations as noted earlier. For comparison, we made similar calculations assuming zero spontaneous polarization, and found essentially identical best-fit *C-V* curves but with best fit values $\Delta E_{\text{QW}} \cong 0.58$ eV and 0.60 eV for Diodes A and B, respectively.

In summary, finite-element electrostatic modeling shows that the presence of inclined QWs under a Schottky contact with sufficient density to deplete the host semiconductor will result in a *C-V* curve that has the same shape and slope as without the QWs, but with a significantly reduced intercept voltage. These calculations explain the remarkable decrease in the apparent *C-V* determined Schottky barrier observed on 4H–SiC with embedded double stacking fault cubic inclusions. Together with measured *C-V* data, these calculations give an estimate of ~0.51 eV for the QW energy depth of the double stacking fault cubic inclusions in 4H-SiC far from the metal interface, which agrees well with an estimate of ~0.53 eV measured with BEEM at the metal/SiC interface.

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[1] J. P. Bergman, H. Lendenmann, P. A. Nilsson, U. Lindefelt, and P. Skytt, Mater. Sci. Forum **353**, 299 (2001)
[2] J. Q. Liu, M. Skowronski, C. Hallin, R. Söderholm, and H. Lendenmann, Appl. Phys. Lett. **80**, 749 (2002).
[3] R. S. Okojie, M. Zhang, P. Pirouz, S. Tumakha, G. Jessen, and L. J. Brillson, Appl. Phys. Lett. **79**, 3056 (2001); L. J. Brillson, S. Tumakha, G. Jessen, R. S. Okojie, M. Zhang, and P. Pirouz, *ibid.* **81**, 2785 (2002).
[4] B. J. Skromme, K. Palle, C. D. Poweleit, L. R. Bryant, W. M. Vetter, M. Dudley, K. Moore, and T. Gehoski, Mater. Sci. Forum **389**, 455 (2002).
[5] J. Q. Liu, H. J. Chung, T. Kuhr, Q. Li, and M. Skowronski, Appl. Phys. Lett. **80**, 2111 (2002).
[6] S. G. Sridhara, F. H. C. Carlsson, J. P. Bergman, and E. Janzén, Appl. Phys. Lett. **79**, 3944 (2001).
[7] H. Iwata, U. Lindefelt, S. Öberg, and P. Briddon, Mater. Sci. Forum **389**, 439 (2002); Phys. Rev. B **68**, 245309 (2003).
[8] Y. Ding, K.-B. Park, J. P. Pelz, K. C. Palle, M. K. Mikhov, B. J. Skromme, H. Meidia, and S. Mahajan, Phys. Rev. B **69**, 041305(R) (2004).
[9] PDE Solutions, Inc., Antioch, CA.
[10] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, Sons, New York, 1981).
[11] Only the lowest QW subband is considered here because it is known that double stacking fault inclusions in SiC have only one QW bound state below the host conduction-band minimum.
[12] A. Qteish, V. Heine, and R. J. Needs, Phys. Rev. B **45**, 6534 (1992).
[13] S. Bai, R. P. Devaty, W. J. Choyke, U. Kaiser, G. Wagner, and M. F. MacMillan, Appl. Phys. Lett. **83**, 3171 (2003).
[14] A. Fissel, U. Kaiser, B. Schröter, W. Richter, and F. Bechstedt, Appl. Surf. Sci. **184**, 37 (2001).
[15] T. A. Kuhr, J. Q. Liu, H. J. Chung, M. Skowronski, and F. Szmulowicz, J. Appl. Phys. **92**, 5863 (2002).
[16] Considering the 8° miscut, the average perpendicular spacing between inclusions in the bulk is obtained to be $s_\perp \sim 95$ nm (Diode A) and $s_\perp \sim 79$ nm (Diode B).
[17] C. Persson and U. Lindefelt, J. Appl. Phys. **82**, 5496 (1997).
[18] L. Patrick and W. J. Choyke, Phys. Rev. B **2**, 2255 (1970).