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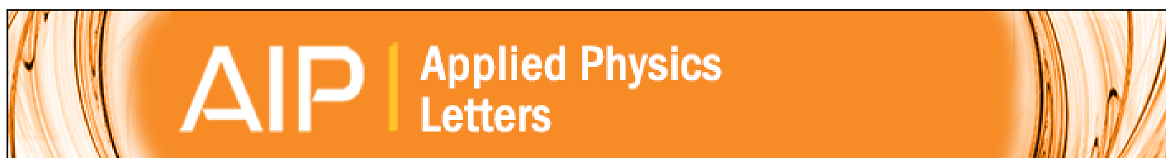

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Direct observation of microscopic change induced by oxygen vacancy drift in amorphous TiO_2 thin films

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To clarify the resistive switching and failure mechanisms in Al/amorphous TiO_2/Al devices we investigate the microscopic change in amorphous titanium oxide films and interface layers after the set process according to film deposition temperatures. For low temperature (<150 °C) samples, the thickness of top interface layer decreased after the set process due to the dissociation of a top interface layer by uniform migration of oxygen vacancies. Meanwhile, for high temperature samples, crystalline TiO phases emerged in the failed state, meaning the formation of conducting paths from the local clustering of oxygen vacancies in nonhomogeneous titanium oxide film. © *2010 American Institute of Physics*. [doi:10.1063/1.3467854]

Recently, there has been an increasing demand for resistance-based nonvolatile memories as several technical and physical limitations have been encountered in the scaling of traditional charge-based memories. Resistance random access memory (RRAM) devices that use binary metal oxides such as NiO,[1] TiO_2,[2] and ZnO[3] have shown outstanding performance with a simple structure and process. However, the driving mechanism of resistive switching phenomena has not yet been completely established. It is generally believed that the microscopic origin of bistable electrical switching in binary oxide thin films is the oxygen vacancy (ion). The type of motion of the oxygen vacancies determines whether the resistive switching mechanism is based on the filamentary conduction model[1,3] or the interface barrier model.[2,4] Several studies have been conducted recently for clearly visualizing direct evidence for the filamentary path. The Ni filament channels in NiO[5] and the Ag bridges in ZnO[3] have been visualized using transmission electron microscopy (TEM) equipped electron energy loss spectroscopy (EELS) and energy dispersive x-ray spectroscopy. More recently, the structural change in conducting nanofilaments in polycrystalline brookite TiO_2 resistive switching memory was directly characterized by high-resolution electron microscopy (HRTEM) equipped with *in situ* current-voltage measurement.[6] However, there have been few papers showing the direct changes in amorphous titanium oxide film during set/reset processes.

In this letter, therefore, we visualize the microscopic changes in the top interface layers and inner amorphous titanium oxide thin films, which occurred when high electric fields were applied, using (HRTEM). The migration of oxygen ions (vacancies), which is the microscopic origin in bipolar resistive switching (BRS) of our Al/amorphous TiO_2 (a-TiO2)/Al devices,[7–9] could be strongly confirmed.

A titanium oxide film on an Al/SiO_2/Si substrate at a deposition rate of 0.45 Å/cycle was deposited by means of plasma-enhanced atomic layer deposition (PEALD) (ASM Genitech MP-1000).[7–9] Various deposition temperatures, ranging from 150 to 250 °C, were selected in order to compare the switching characteristics. The 60-nm-thick aluminum electrodes were deposited at the top and bottom by the thermal evaporation method, and cross-bar array structures were formed using metal shadow masks with line widths of 50 and 500 μm. The sample with the line width of 500 μm was fabricated for the TEM characterizations of the real on/off states. The cross-sectional TEM images of Al/TiO_2/Al samples were examined using 300 kV JEOL JEM 3010. The electrical properties of these samples were measured using a Keithley 4200 semiconductor characterization system in a dc voltage sweep mode.

Figure 1(a) shows the I-V characteristics of Al/TiO_2/Al memory cells at different TiO_2 deposition temperatures of 150, 180, 200, and 250 °C. The PEALD process cycle was 300 cycle. It should be noted that during the dc sweep mode, it easily failed for devices that were fabricated at TiO_2 deposition temperatures of 200 and 250 °C; this is indicated by black arrows in Fig. 1(a). In contrast, devices fabricated at TiO_2 deposition temperatures of 150 and 180 °C clearly showed the reversible behavior, as reported by our previous works.[7–9] The easy breakdown of the devices fabricated at 200 and 250 °C may imply that the state of TiO_2 films is an important factor in determining the reversible BRS properties in our Al/a-TiO_2/Al system. Generally, TiO_2 thin films deposited by the ALD method at temperatures below 200 °C show an amorphous phase, whereas those fabricated at temperatures above 250 °C show a crystalline phase, such as anatase or rutile.[10] The anatase polycrystalline phase in the 250 °C sample was confirmed by observing a cross-sectional TEM image of the film, as shown in the left inset of Fig. 1(a). It is commonly accepted that the electrical conducting paths might be due to the many grain boundaries existing in polycrystalline TiO_2 thin films. Although resistive switching behaviors of the polycrystalline TiO_2 thin films with Al top electrode have been reported,[11] the easy breakdown of our device system may be related with a ultrathin thickness (10–20 nm) and different deposition method of PEALD. However, the TiO_2 thin film fabricated at 200 °C showing the permanent breakdown did not show the crystalline phase even though it was fabricated using a 500-cycle PEALD process, as shown in Fig. 3(a).

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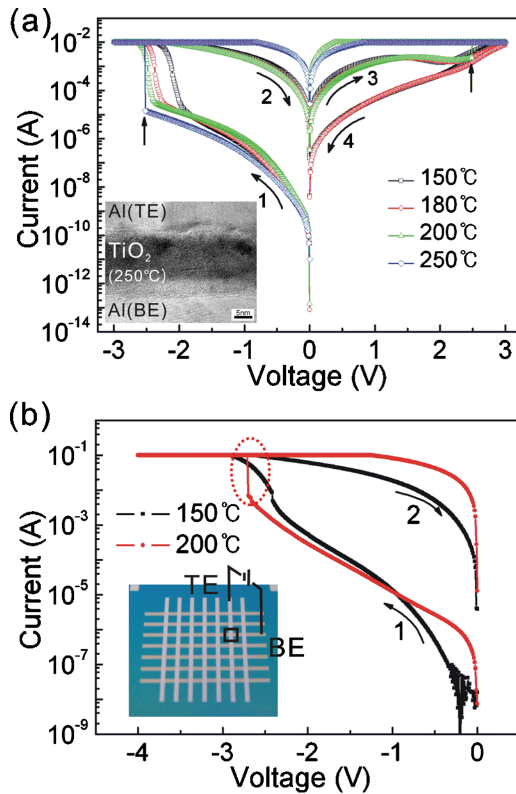

FIG. 1. (Color online) (a) I-V characteristics of $Al/TiO_2/Al$ devices deposited at various temperatures (150, 180, 200, and 250 °C). The HRTEM image of Al/TiO_2(25 °C)/Al stacked structure is shown in the left inset. (b) I-V characteristics of $Al/TiO_2/Al$ devices deposited at 150 and 200 °C measured during negative sweeps. The left inset shows the real photograph of our memory device.

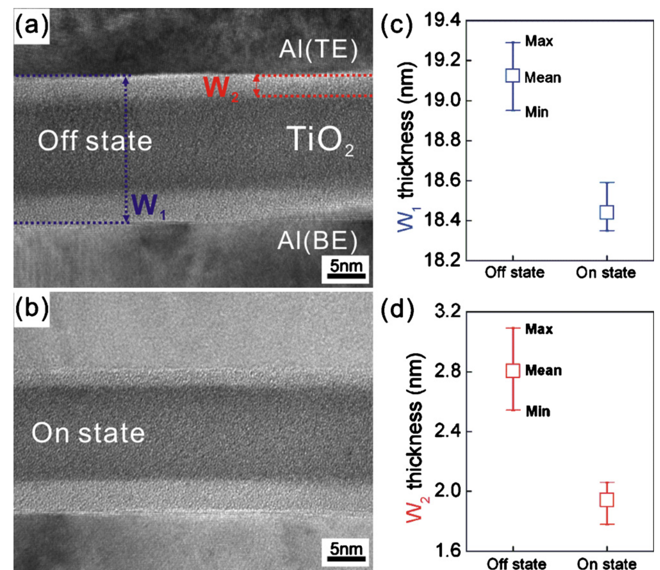

FIG. 2. (Color online) (a) and (b) show the HRTEM images of $Al/TiO_2/Al$ stacks deposited at 150 °C for the off and on state, respectively. W_1 denotes the thickness of the whole layer including both interface layers and W_2 is defined as the thickness of the top interface layer (Al–Ti–O). (c) and (d) present the statistical results of the W_1 and W_2 for the each state, respectively.

In order to further investigate the microscopic origin of the different behaviors according to film deposition temperatures, we compared two different samples at deposition temperatures of 150 and 200 °C. Figure 1(b) shows the I-V characteristic of two $Al/a\text{-}TiO_2/Al$ devices measured at room temperature under the first negative dc voltage sweep. While the I-V curve of the memory cell fabricated at 150 °C exhibited a clear hysteretic behavior when a negative bias was applied to the top Al electrode, the device fabricated at 200 °C showed an abrupt increase, at a negative voltage of −3 V followed by a permanent failed state; this failed state is indicated by the red circle in Fig. 1(b). In this case, reversible resistive switching could not be obtained.

For a clear characterization of the microscopic changes in the interface layers and inner TiO_2 thin films, the HRTEM analysis was separately carried out for each on/off sample. Figures 2(a) and 2(b) show the HRTEM images obtained in the on and off states of the samples fabricated at 150 °C, deposited by a 300 cycle PEALD process. The on state was induced by a negative bias, as shown in Fig. 1(b). In the pristine sample (off state), it was clearly observed that the amorphous TiO_2 thin film with a thickness of ∼13 nm was uniformly stacked on the Al_2O_3/Al substrate. The authors have already reported that the top interface layer was formed by the redox reaction between the Al top electrode and the TiO_2 top domain owing to the strong oxygen affinity of Al.[7,8] It was also demonstrated that the oxygen ions piled up in the top interface region can be mobile by an external voltage bias through EELS elemental mapping using analytical TEM.[7] In Fig. 2, we focus on the top interface layer width [denoted as W_2 in Fig. 2(a)]. The combined thickness of the three layers (bottom interface layer, bulk TiO_2 thin film, and top interface layer) is denoted as W_1. Remarkably, it was observed that both W_1 and W_2 decreased after the set process. Because one HRTEM image could not be used to clearly verify the change in the width of the top interface layer, we measured more than 10 points from three on/off TEM samples in order to obtain statistical data. This is summarized in Figs. 2(c) and 2(d). It is evident that the mean values of both W_1 and W_2 for the off sample are larger than those for the on sample. From the statistical experiments, it can be established that the oxygen ion piled up in the top interface region uniformly drifted into the TiO_{2-x} bulk layer during the set process (negative bias), thereby confirming the dissociation of the Al–Ti–O top interface layer.[7,8] Furthermore, in the image shown in Fig. 2, the microstructural change in the bulk TiO_2 layer was not observed.

In contrast, the device fabricated at 200 °C showed interesting results. The sample was deposited using a 500 cycle PEALD process for the TEM observation in order to more clearly visualize the inner amorphous titanium oxide thin films. Figure 3(b) shows the bright field (BF) images of the on state sample when a negative bias was applied to the top electrode of the samples. In contrast to the image of the sample in the off state, seen in Fig. 3(a), regions of black contrast were remarkably observed; this indicates that the crystalline phase satisfies the diffracted beam condition. The HRTEM image, shown in Fig. 3(c), reveals the crystalline phase with lattice fringes more clearly. Magnified HRTEM images of the regions marked with a red dotted line are shown in Fig. 3(d). The spacing of the fringes corresponds to interplanar spacing of 0.206 nm, as determined from the spacing of the (111) lattice fringes in the silicon substrate. This interplanar spacing is consistent with the (200) planes in a TiO structure (cubic, a=4.177 Å, JCPDS file No. 65–9473), which is the reduced crystalline phase of TiO_2. The permanent electrical path might be originated from this me-

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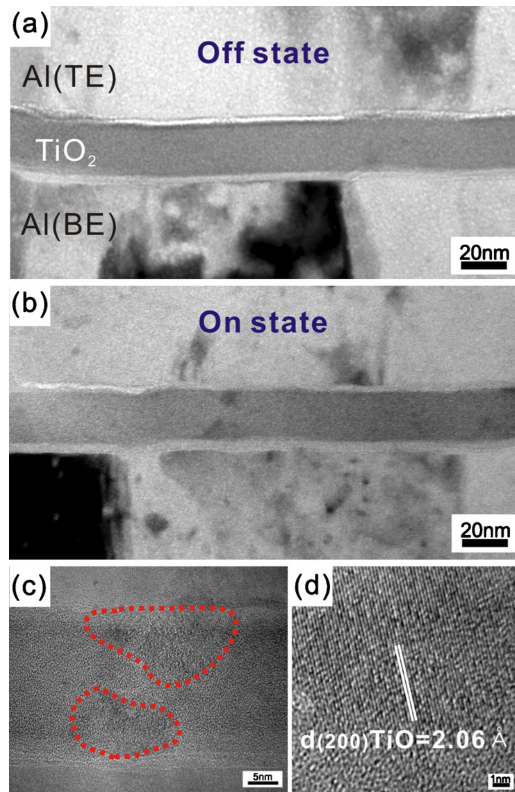

FIG. 3. (Color online) (a) and (b) show the BFTEM images of $Al/TiO_2/Al$ structure deposited at 200 °C for the off and on state, respectively. (c) HRTEM image of the black-contrast region in (b). (d) is the enlarged HRTEM image of region marked with red dot lines of (c).

tallic TiO phase. Moreover, it was another remarkable feature that there was no noticeable change in the top interface layer in the case of 200 °C samples (data not shown here).

These interesting phenomena can be explained by the nonuniform migration of oxygen vacancies in the TiO_2 thin film grown at 200 °C during the set process; the schematics are shown in Fig. 4. The phase and density of the TiO_2 thin films are generally affected by the growth temperature.[10] In our experiment, the TiO_2 films deposited at two different temperatures (150 and 200 °C) had a similar amorphous phase, as observed using the TEM analysis, but showed different I-V characteristics. It can be inferred that although clear lattice fringe images that indicate a polycrystalline phase were not observed in both samples, the TiO_2 thin film fabricated at 200 °C has a nonhomogeneous film due to a relatively high deposition temperature. This nonhomogeneity also induced the irregularity of oxygen vacancies at the inner TiO_2 layer, as shown in Fig. 4(b), when the Al top electrode was deposited. This may cause the local clustering oxygen vacancies in the titanium oxide layer due to nonuniform migration when a negative bias is applied to the top electrode, thereby resulting in the formation of the TiO conducting phase and electrical breakdown. Therefore, amorphous TiO_2 thin films with a homogeneous film density are required in order to retain the stable BRS behavior in our $Al/a\text{-}TiO_2/Al$ RRAM devices.

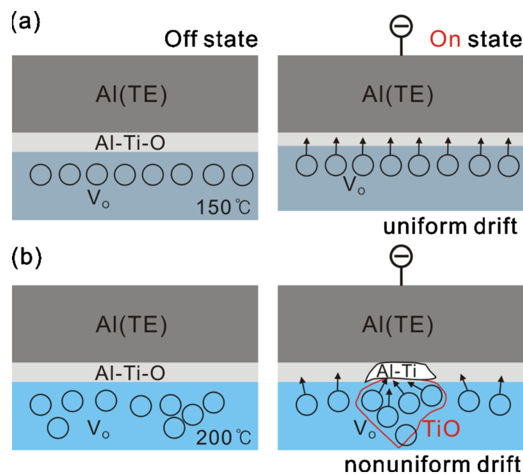

FIG. 4. (Color online) Schematic models showing the difference of the oxygen vacancy drift in amorphous TiO_2 thin films between (a) 150 °C and (b) 200 °C devices.

In summary, we have visualized the microscopic change in amorphous titanium oxide memory devices before and after the set process. On the basis of the HRTEM observation of each on/off sample, it was found that the thickness of the top interface layer (Al–Ti–O) in the 150 °C samples decreased and crystalline TiO structures were formed at the region of bulk TiO_2 in the 200 °C samples after the set process. These results elucidate the microscopic origin of the resistive switching and failure mechanisms in $Al/a\text{-}TiO_2/Al$ RRAM memory devices by providing a direct evidence for the oxygen migration.

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