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# Fabrication of single-electron tunneling transistors with an electrically formed Coulomb island in a silicon-on-insulator nanowire

Dae Hwan Kim,<sup>a)</sup> Suk-Kang Sung, Kyung Rok Kim, Jong Duk Lee, and Byung-Gook Park<sup>b)</sup>

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For the purpose of controllable characteristics, silicon single-electron tunneling transistors with an electrically formed Coulomb island are proposed and fabricated on the basis of the sidewall process technique. The fabricated devices are based on a silicon-on-insulator (SOI) metal–oxide–semiconductor (MOS) field effect transistor with the depletion gate. The key fabrication technique consists of two sidewall process techniques. One is the patterning of a uniform SOI nanowire, and the other is the formation of *n*-doped polysilicon sidewall depletion gates. While the width of a Coulomb island is determined by the width of a SOI nanowire, its length is defined by the separation between two sidewall depletion gates which are formed by a conventional lithographic process combined with the second sidewall process. These sidewall techniques combine the conventional lithography and process technology, and guarantee the compatibility with complementary MOS process technology. Moreover, critical dimension depends not on the lithographical limit but on the controllability of chemical vapor deposition and reactive-ion etching. Very uniform weakly *p*-doped SOI nanowire defined by the sidewall technique effectively suppresses unintentional tunnel junctions formed by the fluctuation of the geometry or dopant in SOI nanowire, and the Coulomb island size dependence of the device characteristics confirms the good controllability. A voltage gain larger than one and the controllability of Coulomb oscillation peak position are also successfully demonstrated, which are essential conditions for the integration of a single-electron tunneling transistor circuit. Further miniaturization and optimization of the proposed device will make room temperature designable single-electron tunneling transistors possible in the foreseeable future.

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## I. INTRODUCTION

Recently, single-electron tunneling phenomena in silicon nanostructures have been extensively studied in terms of future low-power nanoelectronic device applications. In comparison with GaAs heterostructures, the possibility of the integration with the conventional complementary metal–oxide–semiconductor (CMOS) devices is a unique merit of silicon nanostructures.

Up to now, various single-electron tunneling transistors (SETTs) based on silicon-on-insulator (SOI) nanowires have been demonstrated. In the case of highly doped SOI nanowire,<sup>1–4</sup> Coulomb blockade oscillation is attributed to the formation of randomly distributed Coulomb islands separated by tunnel junctions formed by dopant fluctuations, and its dependence on the gate voltage is quite complicated. On the other hand, SETTs based on the undoped SOI nanowire (i.e., weakly *p* doped)<sup>5,6</sup> show relatively controllable characteristics originated from the device geometry due to the exclusion of a dopant fluctuation effect. Therefore, from the viewpoint of reproducibility of device characteristics, the undoped SOI film is a promising material for the implementation of the SETT circuit.

In most SETTs based on the undoped SOI nanowire, tunnel junctions have been defined using lateral patterning by electron-beam lithography.<sup>5,6</sup> However, its low throughput, high cost, and incompatibility with conventional CMOS technology provides a motivation to pursue an alternative nanoscale lithography technique.

As another technique to form tunnel junctions, a depletion or split gate structure has been used in SETTs based on the bulk silicon metal–oxide–semiconductor field effect transistor (MOSFET),<sup>7–9</sup> in which the Coulomb island is incorporated into the inversion channel at the Si/SiO<sub>2</sub> interface and the tunneling conductance is controlled by the depletion gate voltage.

In this article, we present the fabrication method for SETTs based on a weakly *p*-doped SOI MOSFET with depletion gates. In our process, two sidewall process techniques are used. One is the patterning method for the definition of an SOI nanowire. The other is the formation method of two depletion gates with narrow line and space. These techniques combine the conventional lithography, chemical vapor deposition (CVD), and reactive ion etching (RIE), and guarantee the compatibility with CMOS process technology. Very uniform weakly *p*-doped SOI nanowire defined by the sidewall technique effectively suppresses unintended tunnel junctions formed by the fluctuation of the geometry or dop-

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ant in SOI nanowire. A Coulomb island in the inversion channel of the SOI MOSFET is electrically formed by the sidewall depletion gate voltage, and its size is estimated to be smaller than 13.2 nm.

In addition to the idea of device fabrication, we focus on the formation mechanism of the Coulomb island and tunnel junctions in terms of the island size dependence of device characteristics.

## II. EXPERIMENT

The devices were fabricated on  $4 \times 10^{15} \text{ cm}^{-3}$  boron doped (100) SOI wafers prepared by the separation by implanted oxygen technique. The top Si layer is separated from the Si substrate by 400-nm-thick buried oxide. In the fabrication of our SETTs, two sidewall process techniques are used. First is the patterning method for the formation of a SOI nanowire. The thickness of the top Si layer is thinned to 60 nm by thermal oxidation, and the 40-nm-thick  $\text{SiO}_2$  is deposited, and the device region is defined by the conventional photolithography and RIE [Fig. 1(a)]. Then an 80-nm-thick  $\text{Si}_3\text{N}_4$  layer is deposited on the SOI wafer at  $750^\circ\text{C}$  using a low pressure CVD (LPCVD) system and defined by the conventional photolithography and RIE, which covers a part of the device region and a part of the buried oxide region as shown in Fig. 1(b). Then, 35-nm-thick amorphous silicon is deposited at  $550^\circ\text{C}$  using an LPCVD system and annealed at  $800^\circ\text{C}$  for 30 min, so that the edge of  $\text{Si}_3\text{N}_4$  layer is fully covered [Fig. 1(c)]. This amorphous silicon layer is anisotropically etched in  $\text{Cl}_2$  reactive-ion plasma, resulting in the 30-nm-wide amorphous silicon sidewall around the corner of both the  $\text{Si}_3\text{N}_4$  layer and the device region [Fig. 1(d)]. After the selective chemical etching of the  $\text{Si}_3\text{N}_4$  layer in  $\text{H}_3\text{PO}_4$  solution [Fig. 1(e)], 40-nm-thick  $\text{SiO}_2$  layer is anisotropically etched in  $\text{CHF}_3/\text{CF}_4$  reactive-ion plasma using the amorphous silicon sidewall as an etch mask, resulting in 30-nm-wide  $\text{SiO}_2$  wire on the device region, and the silicon surface is exposed except underneath this  $\text{SiO}_2$  wire as shown in Fig. 1(f). Then, the source and drain region are covered with the photoresist by photolithography [Fig. 1(g)], and the top silicon is etched in  $\text{Cl}_2$  reactive-ion plasma using the 30-nm-wide  $\text{SiO}_2$  wire as a hardmask, forming the 30-nm-wide SOI nanowire [Fig. 1(h)]. During this step, the exposed amorphous silicon sidewall is also etched in  $\text{Cl}_2$  plasma, but the  $\text{SiO}_2$  wire is a useful hardmask during the pattern transfer due to a good selectivity between Si and  $\text{SiO}_2$  in  $\text{Cl}_2$  reactive-ion plasma. Adequate chemical etching of the silicon oxide in HF solution enables the preparation of a damage-free surface of SOI nanowire and the lift-off process of the remnant amorphous silicon sidewall [Figs. 1(i)–1(j)]. In reality, there may be amorphous silicon sidewall residue around the source/drain region even after wet etching of the silicon oxide, as shown in Fig. 1(i), but this residue has no influence on the device operation, thus this residue is left out hereinafter in Fig. 1(j).

Figure 2 shows the scanning electron microscope (SEM) image of the SOI nanowire formed by our sidewall patterning technique. Uniform 30-nm-wide SOI wire with no ir-

regularities can be defined by our technique, which eliminates unintended tunnel junctions formed by the fluctuation of the width of SOI wire. The uniformity of nanowire defined by the sidewall patterning technique was better than that of nanowire defined by electron-beam lithography.<sup>10</sup> Although it may depend on the performance of electron-beam lithography facilities, irregularity with the size of electron-beam diameter is an inherent problem regardless of the facilities and may be the origin of unintended tunnel junctions formed by the fluctuation of the geometry.<sup>6,11</sup>

For the electrically formed Si island, two polycrystalline silicon (poly-Si) depletion gates are subsequently formed on the SOI wire, which is our second sidewall process technique. After stripping the remnant oxide on the SOI wire in HF solution, 55-nm-thick  $\text{SiO}_2$  is deposited by a plasma enhanced CVD (PECVD) system and etched in  $\text{CHF}_3/\text{CF}_4$  reactive-ion plasma, forming the oxide spacer around SOI wire. This spacer plays an important role in the step coverage of the poly-Si sidewall which will act as the depletion gate, by substituting a smoothly curvilinear shape for the step-like shape around the SOI wire. Then, 30-nm-thick  $\text{SiO}_2$  is deposited by a PECVD system, and 80-nm-thick  $\text{Si}_3\text{N}_4$  is deposited using the LPCVD system [Fig. 3(a)]. Then, a groove pattern is transferred into the  $\text{Si}_3\text{N}_4$  layer by the lithography and RIE as shown in Fig. 3(b). This nitride groove pattern is designed to overlap with the region which will become the sidewall gate contact pad, as shown in Fig. 3(c). The width of groove  $W_{\text{Grv}}$  is varied from 100 to 250 nm in 50 nm steps in the same wafer by electron-beam lithography using poly(methylmethacrylate) electron-beam resist, but the feature size of this range can be easily obtained by state-of-the-art photolithography. After the formation of the nitride groove, 8-nm-thick oxide is thermally grown in dry  $\text{O}_2$  at  $800^\circ\text{C}$  for damage curing, which forms the gate-oxide-quality control gate oxide. During this step, the control gate oxide becomes thicker locally at the nitride groove region as shown in Fig. 3(d). Then, 35-nm-thick phosphorus doped  $n^+$  poly-Si is deposited using LPCVD, and the sidewall gate contact pad region is covered with the photoresist by photolithography [Fig. 3(c)]. Following etching of the  $n^+$  poly-Si in  $\text{Cl}_2$  reactive-ion plasma forms the poly-Si sidewall depletion gates [Fig. 3(d)], which is eventually connected into the low-resistance poly-Si region, i.e., the sidewall gate contact pad region. After stripping the photoresist, the formation of the additional intergate oxide using the PECVD system is followed by the formation of the poly-Si control gate by the photolithography and RIE in  $\text{Cl}_2$  plasma. The control gate and source/drain regions are doped by  $\text{As}^+$  ion implantation [Fig. 3(e)]. Then, the passivation oxide is deposited using LPCVD, and the contact hole is formed by the photolithography and RIE in  $\text{CHF}_3/\text{CF}_4$  plasma [Fig. 3(c)]. Finally, the formation of an aluminum electrode is performed using Al sputtering, photolithography, and RIE in  $\text{Cl}_2$  plasma, which is compatible with the conventional CMOS process technology. The resultant thickness of SOI wire was 45 nm, and the final width of SOI wire  $W_{\text{CH}}$  shrunk to about 23 nm.

Figure 4 shows the cross section of the fabricated device,

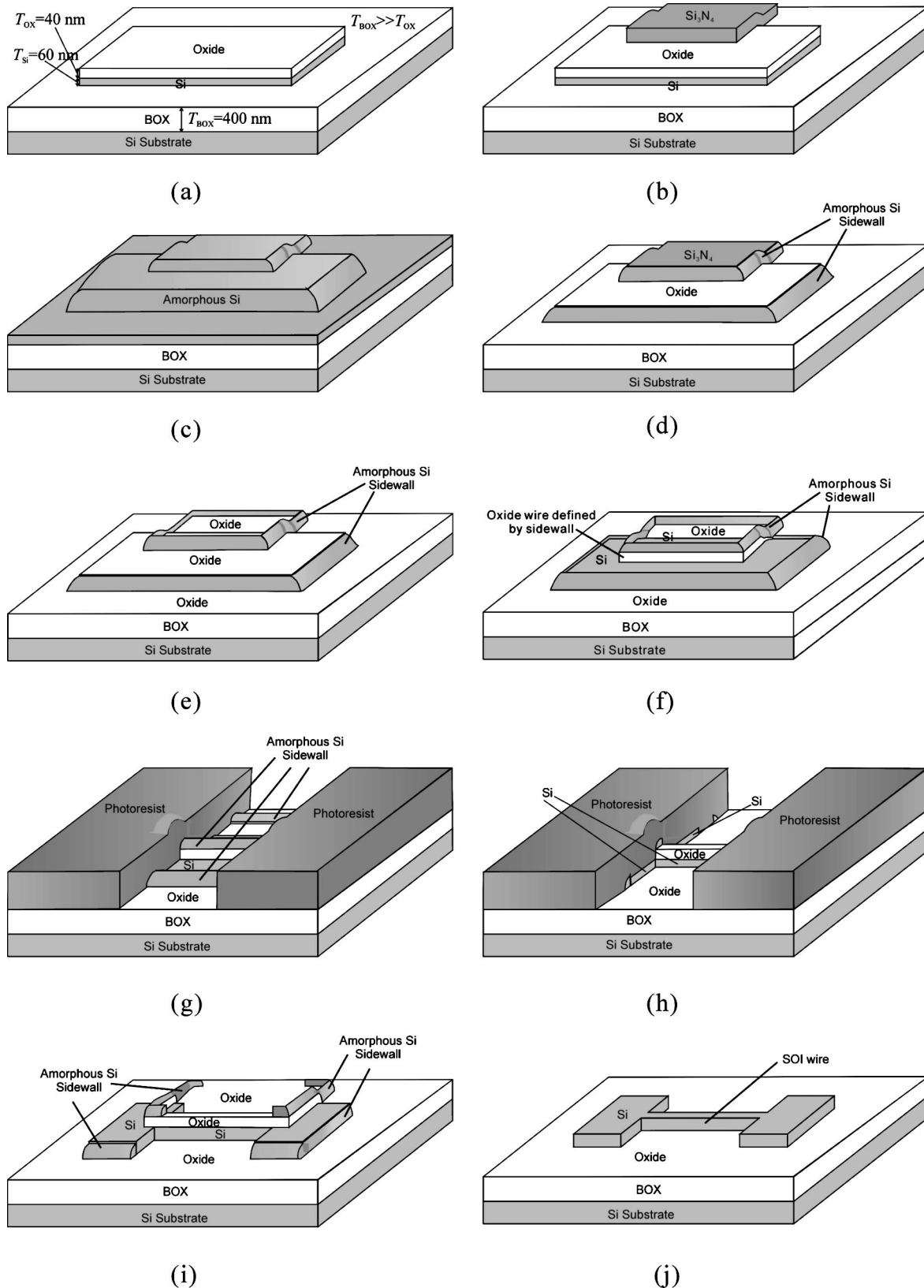


FIG. 1. Key process steps to form SOI nanowire by the sidewall patterning technique. These are just schematics, not to the exact scale. (a) The definition of the device region and the oxide layer. (b) The definition of the  $\text{Si}_3\text{N}_4$  layer overlapped between the device region and the buried oxide region. (c) The deposition of the amorphous silicon layer. (d) The anisotropic etching of the amorphous silicon and the formation of a 30-nm-wide amorphous silicon sidewall around the corner of both the  $\text{Si}_3\text{N}_4$  layer and the device region. (e) The chemical etching of the  $\text{Si}_3\text{N}_4$  layer in  $\text{H}_3\text{PO}_4$  solution. (f) The anisotropic etching of the oxide. The 30-nm-wide pattern is transferred to the oxide layer. (g) The blocking of the source and drain region by the photoresist. (h) The anisotropic etching of silicon and the formation of 30-nm-wide SOI wire. (i) The stripping of the photoresist. (j) The chemical etching of the oxide and the lift-off of the remnant amorphous silicon sidewall.

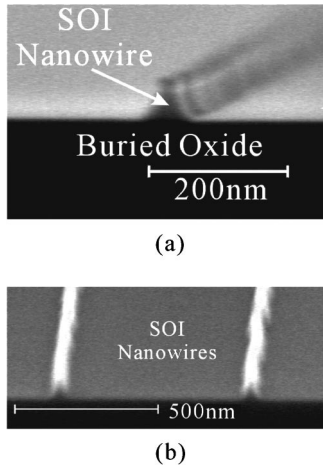


FIG. 2. SEM images of the SOI nanowire formed by the sidewall patterning technique. A good uniformity of SOI wire efficiently prohibits the unintentionally formed tunnel junctions.

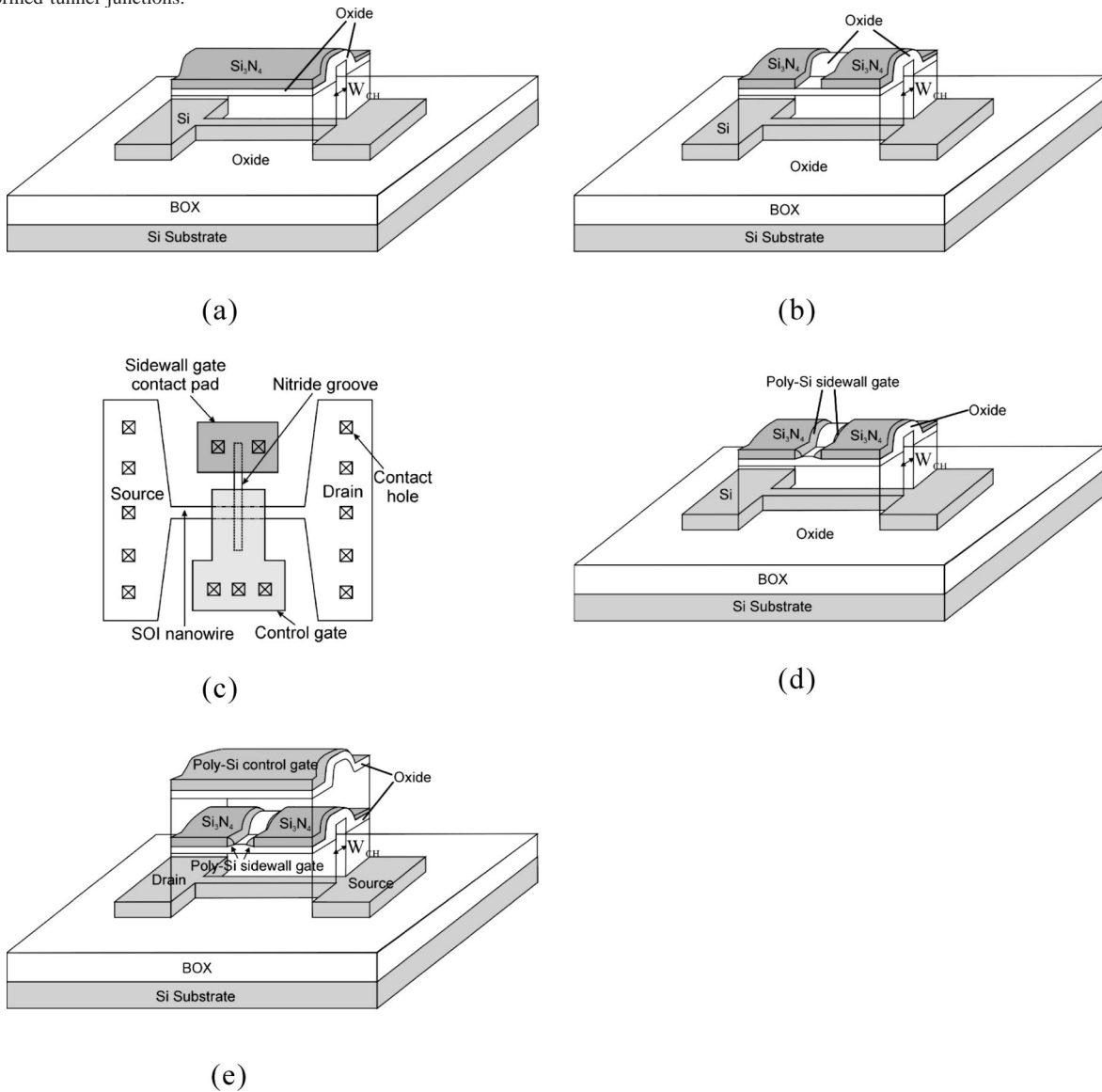


FIG. 3. Key process steps to form two sidewall depletion gates and the top control gate on the SOI nanowire. (a) The deposition of the gate oxide and  $\text{Si}_3\text{N}_4$  layer. (b) The formation of the groove in the  $\text{Si}_3\text{N}_4$  layer, whose width  $W_{\text{Grv}}$  is varied from 100 to 250 nm on the same wafer. (c) The layout of a fabricated SETT. (d) Thermal oxidation and the formation of  $n$ -type doped poly-Si sidewall depletion gates. (e) The deposition of control gate oxide and the formation of the poly-Si control gate.

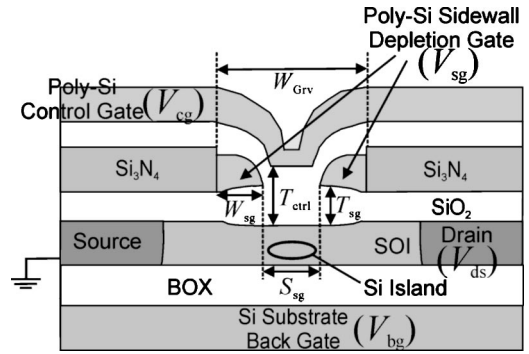


FIG. 4. Schematic diagram of the cross section of a fabricated device, the notation for voltages biasing electrodes, and major geometric parameters. They are:  $T_{\text{ctrl}}=60$  nm,  $T_{\text{sg}}=38$  nm, and  $W_{\text{sg}}=30$  nm,  $L_{\text{CH}}=7$   $\mu\text{m}$ , respectively. The  $S_{\text{sg}}$  is varied from 40 to 190 nm.

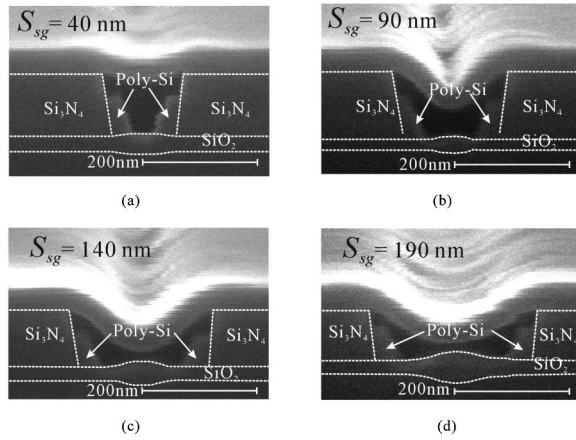


FIG. 5. SEM images of the cross section along the channel length direction of fabricated SETTs having various  $S_{sg}$ 's on the same 4 in. SOI wafer: (a)  $S_{sg}=40$  nm, (b)  $S_{sg}=90$  nm, (c)  $S_{sg}=140$  nm, (d) and  $S_{sg}=190$  nm.

indicating bias electrodes and major geometric parameters. They are:  $T_{ctrl}$  (thickness of the control gate oxide)=60 nm,  $T_{sg}$  (thickness of the sidewall depletion gate oxide)=38 nm,  $W_{sg}$  (width of the sidewall depletion gate)=30 nm, and  $L_{CH}$  (length of SOI wire)=7  $\mu$ m, respectively. The space between two sidewall gates  $S_{sg}$  is 40, 90, 140, and 190 nm, respectively, because  $S_{sg}$  is given by  $W_{Grv} - 2 \times W_{sg}$ . Thus, the length of the Coulomb island shrank to be smaller than the feature size of state-of-the-art lithography, by a conventional lithographic process (electron-beam lithography in this work) combined with a sidewall process technique. In our devices, the effective size of Coulomb island should be smaller than  $S_{sg} \times W_{CH}$ , due to the electric field effect. Figure 5 shows SEM images of the cross section along the channel length direction of fabricated SETTs having various  $S_{sg}$ 's on the same 4 in. SOI wafer.

The operation of the device is as follows: the formation of the inversion layer (i.e., threshold voltage of SOI MOSFET) is controlled by the back gate voltage  $V_{bg}$ , and two tunnel junctions are formed by poly-Si sidewall depletion gate voltage  $V_{sg}$ . The charge of the electrically formed island is controlled by the control gate voltage  $V_{cg}$ .

The salient feature of our process technique can be summarized as follows: Using the combination of conventional lithography and process technology, the size of the Coulomb island and tunnel junctions can be defined beyond the limit of state-of-the-art lithography.

The first idea for the development of the Si island with the capacitance of a few aF is the formation of a SOI nanowire by the sidewall patterning technique. The next idea is the formation of a sidewall depletion gate in the groove with the feature size of state-of-the-art lithography.<sup>12</sup>  $W_{CH}$  and  $W_{sg}$  defined by the sidewall process technique have a good uniformity, which suppresses unintentional tunnel barriers in the SOI wire effectively, as previously described. Moreover, the proposed sidewall technique has the merit in that its scaling limit depends not on the limit of lithography but on the controllability of CVD and RIE.

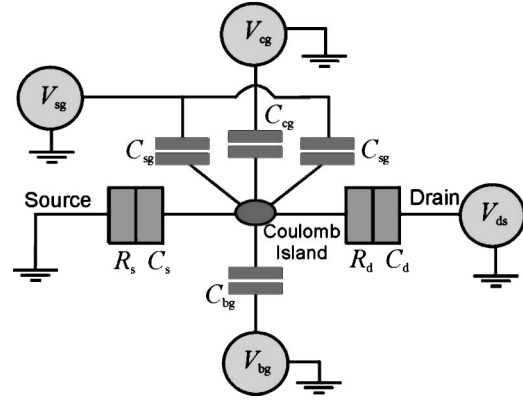


FIG. 6. Equivalent circuit diagram of the fabricated SETTs. The charge of Coulomb island is coupled with five capacitance components. They are: the capacitance between the control gate and island  $C_{cg}$ , the capacitance between the drain electrode and island  $C_d$ , the capacitance between the source electrode and island  $C_s$ , the capacitance between sidewall depletion gate and island  $C_{sg}$ , and the capacitance between the back gate and island  $C_{bg}$ . Tunneling resistances  $R_d$  and  $R_s$  and tunnel junction capacitances  $C_d$  and  $C_s$  are determined by the shape of the potential barrier induced by  $V_{sg}$ .

### III. RESULTS AND DISCUSSION

#### A. Coulomb island size dependence of device characteristics

Figure 6 shows the equivalent circuit diagram of the fabricated SETTs. The charge of the Coulomb island is coupled with five capacitance components. They are: the capacitance between the control gate and island  $C_{cg}$ , the capacitance between the drain and island  $C_d$ , the capacitance between the source and island  $C_s$ , the capacitance between the sidewall depletion gate and island  $C_{sg}$ , and the capacitance between the back gate and island  $C_{bg}$ . Tunneling resistances  $R_d$  and  $R_s$  and tunnel junction capacitances  $C_d$  and  $C_s$  are determined by the shape of the potential barrier induced by  $V_{sg}$ , and the period of Coulomb oscillation in sweeping  $V_{cg}$  ( $\Delta V_{cg}$ ) is determined by  $C_{cg}$ . The total capacitance of an electrically formed Si island  $C_{total}$  will be the summation of  $C_{cg}$ ,  $C_d$ ,  $C_s$ ,  $2C_{sg}$ , and  $C_{bg}$ .

The devices were characterized by a precision semiconductor parameter analyzer HP4155A. Figure 7 shows the drain current  $I_{ds}$  as a function of the control gate voltage  $V_{cg}$  and the size of Coulomb island  $S_{sg}$ . In these  $I_{ds}-V_{cg}$  curves,  $V_{ds}$ ,  $V_{sg}$ , and  $V_{bg}$  are fixed at 10 mV, -0.1 V, and 10 V, respectively. Multiple Coulomb oscillation peaks are clearly observed even at the liquid nitrogen temperature. The period of Coulomb oscillation  $\Delta V_{cg}$  in the  $I_{ds}-V_{cg}$  curve is 675, 210, 123, and 80 mV, respectively, as  $S_{sg}$  is varied from 40 to 190 nm. The clear difference of  $\Delta V_{cg}$  related to  $S_{sg}$  verifies that the oscillation of  $I_{ds}$  stems from single-electron tunneling phenomenon in an electrically formed Coulomb island, and its size is controllable by the process parameter  $S_{sg}$ . This Coulomb oscillation showed reliable single-island characteristics at various temperatures.<sup>13</sup>

The drain current  $I_{ds}$  and the differential conductance as a function of the drain-source voltage  $V_{ds}$  and the size of Coulomb island  $S_{sg}$  is also measured at 15 K as shown in Fig. 8.

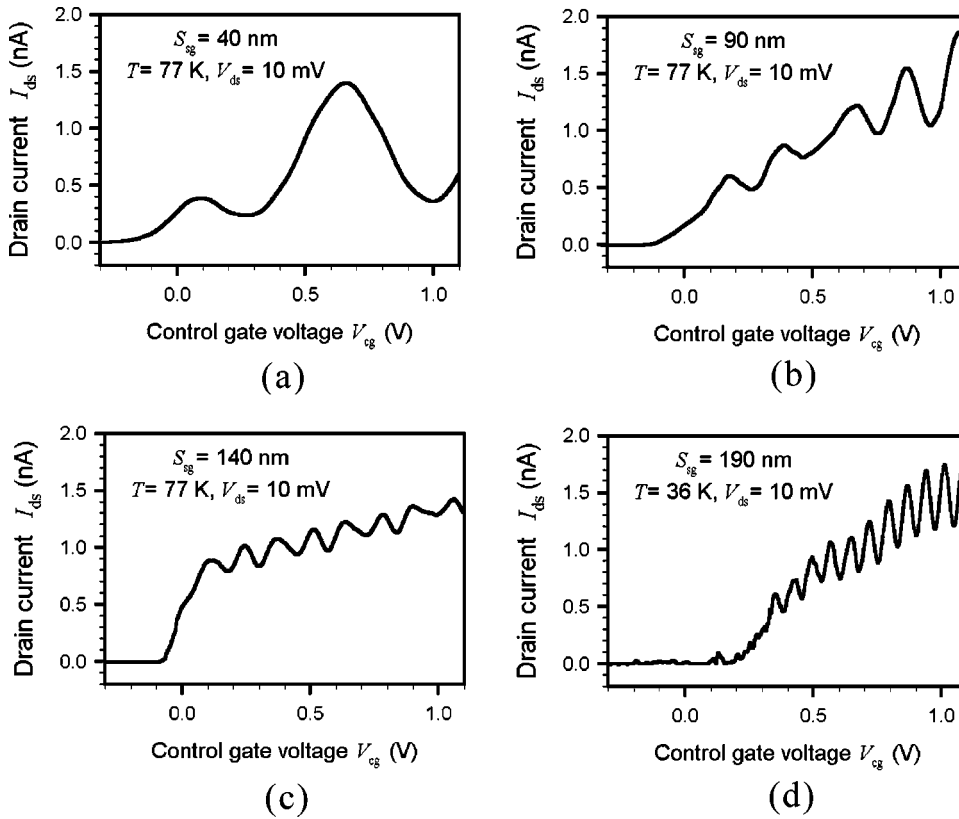


FIG. 7. Drain current  $I_{ds}$  as a function of the control gate voltage  $V_{cg}$  and the size of Coulomb island  $S_{sg}$ . In these  $I_{ds}-V_{cg}$  curves,  $V_{ds}$ ,  $V_{sg}$ , and  $V_{bg}$  were fixed at 10 mV,  $-0.1$  V, and 10 V, respectively. (a)  $S_{sg}=40$  nm, (b)  $S_{sg}=90$  nm, (c)  $S_{sg}=140$  nm, (d) and  $S_{sg}=190$  nm.

These  $I_{ds}-V_{ds}$  curves are acquired, fixing  $V_{sg}$  and  $V_{bg}$  at  $-0.1$  and 10 V, respectively. Nonlinear relation between  $I_{ds}$  and  $V_{ds}$  by Coulomb blockade phenomenon is clearly observed. When measuring  $I_{ds}-V_{ds}$  characteristics,  $V_{cg}$  is chosen to be the value at the valley of the oscillation in  $I_{ds}-V_{cg}$  curve, i.e., the voltage region showing the zero-differential

conductance is the maximum Coulomb gap voltage  $\Delta V_{MAX}$ , which is 104, 76, 59, and 45 mV, respectively, as  $S_{sg}$  is varied from 40 to 190 nm.

The  $S_{sg}$  dependence of device characteristics suggests that our SETTs are based on a clearly artificial formation mechanism of a Coulomb island and tunnel junctions. Moreover,

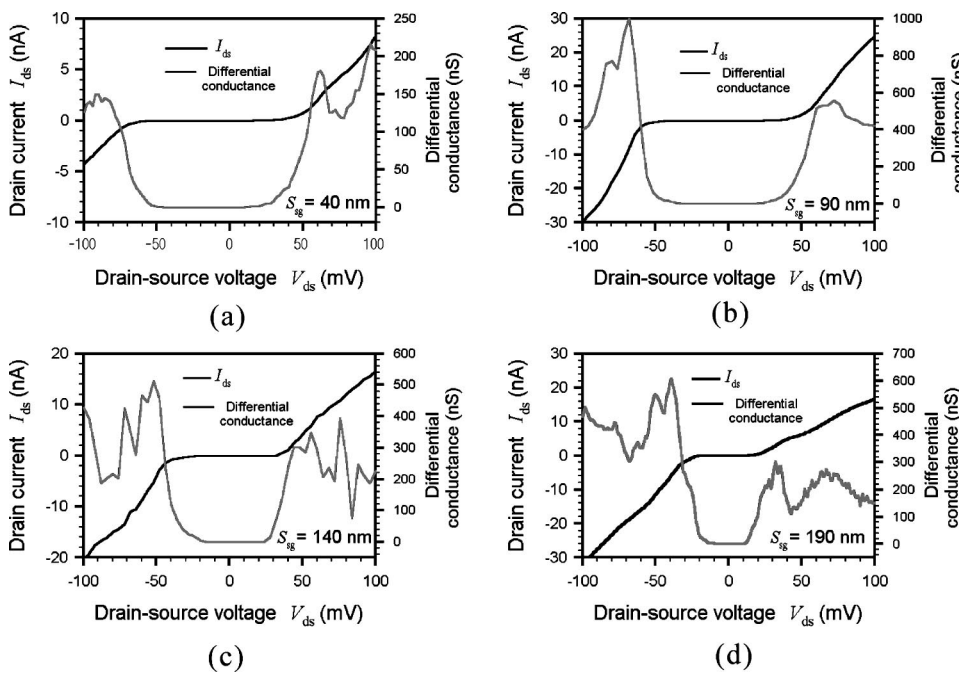


FIG. 8. Drain current  $I_{ds}$  and the differential conductance as a function of the drain-source voltage  $V_{ds}$  and the size of Coulomb island  $S_{sg}$  measured at 15 K. In these  $I_{ds}-V_{ds}$  curves,  $V_{sg}$  and  $V_{bg}$  were fixed at  $-0.1$  and 10 V, respectively.  $V_{cg}$  was chosen to be the value at the valley of the oscillation in the  $I_{ds}-V_{cg}$  curve, i.e., the voltage region showing the zero-differential conductance is the maximum Coulomb gap voltage  $\Delta V_{MAX}$ : (a)  $S_{sg}=40$  nm, (b)  $S_{sg}=90$  nm, (c)  $S_{sg}=140$  nm, and (d)  $S_{sg}=190$  nm.

TABLE I. Summary of the device parameters extracted from the electrical characteristics. They are well controlled by the process parameter  $S_{sg}$ , which is miniaturized to be smaller than the limit of state-of-the-art lithography by the combination of the conventional lithography and process technology. The size of the Coulomb island shrank to 50%–80% of the size of the defined island (i.e.,  $S_{sg} \times W_{CH}$ ) by the device geometry, which is originated from the field effect of sidewall depletion gate bias  $V_{sg}$ . In the case of  $S_{sg} = 40$  nm, the size of the Coulomb island may be about 13.2 nm.

Device parameters	Defined island size $S_{sg}$			
	40 nm	90 nm	140 nm	190 nm
Coulomb oscillation period $\Delta V_{cg}$	675 mV	210 mV	123 mV	80 mV
Coulomb gap voltage at $V_{cg}$ at the valley of $I_{ds}$ oscillation $\Delta V_{MAX}$	104 mV	76 mV	59 mV	45 mV
$C_{cg}$ extracted from $\Delta V_{cg}$ $C_{cg} = \frac{e}{\Delta V_{cg}}$	0.24 aF	0.76 aF	1.30 aF	2.0 aF
$C_{cg}$ estimated from the device geometry (two parallel plate approximation) $C_{cg} = \epsilon_{SiO_2} \times \frac{S_{sg} \times W_{CH}}{T_{ctrl}} \times \alpha$	$0.49\alpha$ aF	$1.17\alpha$ aF	$1.77\alpha$ aF	$2.45\alpha$ aF
Island size shrinkage factor $\alpha$	0.49	0.65	0.73	0.82
$C_d$ extracted from measured $I_{ds}$ contour	1.30 aF	1.34 aF	1.42 aF	1.54 aF
$C_{total}$ extracted from measured $I_{ds}$ contour and $\Delta V_{MAX}$ at constant $V_{sg}$ and $V_{bg}$	2.86 aF	3.44 aF	4.14 aF	5.08 aF
Voltage gain $K_V$	0.185	0.57	0.92	1.3
Island size $2r$ estimated from the self capacitance $C_{self}$ under assumption of spherical Coulomb island in a $SiO_2$ environment $C_{self} = 4\pi\epsilon r$	13.2 nm	15.9 nm	19.1 nm	23.4 nm

the process parameter  $S_{sg}$  can be controlled by the conventional lithography with the feature size of 0.1  $\mu\text{m}$  and process technology such as CVD and RIE, without a special nanoscale lithography method. In addition, it is confirmed by the electrical characteristics that the good uniformity and low doping level of SOI nanowire effectively suppress tunnel junctions unintentionally formed by the fluctuation of the geometry or dopant.

A few device parameters extracted from the electrical characteristics of fabricated SETTs are summarized in Table I. Comparing  $\Delta V_{cg}$  with  $C_{cg}$  estimated from the device geometry,  $C_{cg}$  extracted from  $\Delta V_{cg}$  is about 50%–80% of that calculated from the device geometry, which implies that the size of the Coulomb island shrank to be smaller than the defined island (i.e.,  $S_{sg} \times W_{CH}$ ) by the field effect of  $V_{sg}$ . Thus, the potential barrier by  $V_{sg}$  penetrates into the region of the defined island. However, the  $\Delta V_{cg}$  is seldom varied when sweeping  $V_{cg}$  at a constant  $V_{sg}$  (see Fig. 7), which confirms that the size of the Coulomb island is dominantly controlled by  $S_{sg}$  and  $V_{sg}$  and immune to  $V_{cg}$ , i.e.,  $V_{cg}$  independently controls the potential of the Coulomb island. These characteristics stem from the three-dimensional structure of the poly-Si sidewall depletion gate wrapping the SOI nanowire.

Since the poly-Si control gate fully covers the SOI wire, fringing capacitance exists as an additional component of the effective  $C_{cg}$ . Therefore, the real size is maybe less than 50% of the defined island. As shown in Table I, if we compare the total capacitance of the Coulomb island  $C_{total}$  ex-

tracted from the  $I_{ds}$  contour with the self capacitance of the spherical conducting island in a  $SiO_2$  environment, the island size of SETT with  $S_{sg} = 40$  nm is about 13.2 nm, which is less than a half of  $S_{sg}$ .

## B. Voltage gain and peak position control

The  $I_{ds}$  contour of SETT with  $S_{sg} = 190$  nm at 15 K is shown in Fig. 9, whose shape is a well-known parallelogram, the so called Coulomb diamond. The  $C_{total}$  of the island is 5.08 aF, which corresponds to the charging energy of 15.7 meV and the thermal noise of 188 K. From the slope of contour,  $C_{cg}$ ,  $C_d$ , and  $C_s$  are given to be 2.0, 1.54, and 1.33 aF, respectively.

Of importance is the voltage gain  $K_V$  of SETTs in the viewpoint of the application to a practical integrated circuit. It is given as the ratio  $C_{cg}/C_d$  at a constant current.<sup>14</sup> Low current level and small voltage gain are inherent demerits of SETTs. Up to now, technologically oriented research has been primarily focused on the further miniaturization of the basic component of SETTs, while ignoring the voltage gain. A voltage gain larger than unity has been recently reported and discussed.<sup>15–17</sup> Our device shows  $K_V = 1.3$  as shown in Fig. 9. On the other hand, the  $K_V$  decreases as the island size is smaller (Table I), because the capacitive coupling between the island and the control gate decreases while  $C_d$  and  $C_s$  are nearly invariant. Therefore, both  $S_{sg}$  and  $T_{ctrl}$  should be scaled down for the application of our SETTs to the room temperature operation. In addition,  $K_V$  is expected to in-



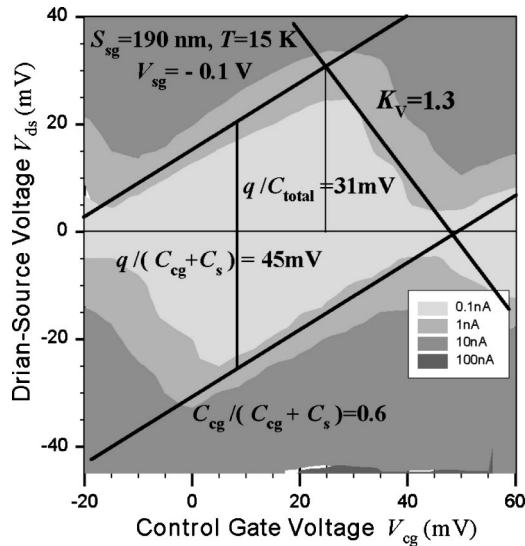


FIG. 9.  $I_{ds}$  contour, i.e., Coulomb diamond of SETT with  $S_{sg} = 190$  nm. The measurement temperature was 15 K and the voltage gain  $K_V$  was 1.3 from the slope of the contour.

crease as the thickness of SOI wire decreases, but the optimization of the concentration of impurities and the thickness of SOI wire is required.

The controllability of the peak position<sup>9,16,18</sup> of Coulomb oscillation is another issue. It is indispensable to most SETT circuits. However, the randomness of background charge makes it difficult to control the position of the oscillation peak. In the case of recently published SETTs, an asymmetric tunnel barrier,<sup>9</sup> additional side gate,<sup>16</sup> or a Si nanocrystal floating gate<sup>18</sup> is used for the peak position control. But these ideas have the demerits of varied current level,<sup>9</sup> large area of device structure,<sup>16</sup> and irreproducible programming characteristics from randomly distributed Si nanocrystals,<sup>18</sup> respectively. In our structure, a sidewall depletion gate can control the position of the oscillation peak, which is originated from the sharing of the island charge between the control gate and sidewall depletion gate as shown in Fig. 6.

Figure 10 shows the  $V_{cg}$  dependence of  $I_{ds}$  as a function of  $V_{sg}$  at 4.2 K for a SETT with  $S_{sg} = 190$  nm. The position of the oscillation peak is well modulated by  $V_{sg}$ . The slight decrease of  $I_{ds}$  at  $V_{sg} = -0.1$  V is attributed to the increase of the potential barrier height by negatively larger  $V_{sg}$ . The position of the oscillation peak in the  $V_{cg}$  axis is modulated by 58 mV, when  $V_{sg}$  is changed by 100 mV while  $V_{ds}$  and  $V_{bg}$  are fixed at 10 mV and 18 V, respectively. Quantitatively, the displacement of the oscillation peak in the  $V_{cg}$  axis ( $\Delta V_{cgd}$ ) by the change of the  $V_{sg}$  ( $\Delta V_{sg}$ ) can be analytically derived from the charge sharing of Coulomb island, which is as follows:

$$\left(1 - \frac{C_{cg}}{C_{total}}\right) \times \Delta V_{cgd} = \frac{2C_{sg}}{C_{total}} \times \Delta V_{sg}. \quad (1)$$

From Eq. (1),  $C_{sg}$  is estimated to be 0.89 aF, assuming  $C_{cg} = 2.0$  aF,  $C_{total} = 5.08$  aF (see Table I),  $\Delta V_{cgd} = 58$  mV, and

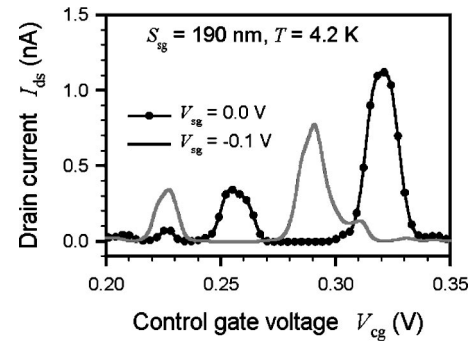


FIG. 10.  $V_{cg}$  dependence of  $I_{ds}$  at 4.2 K as a function of  $V_{sg}$  of SETT with  $S_{sg} = 190$  nm.  $V_{ds}$  and  $V_{bg}$  were fixed at 10 mV and 18 V, respectively. The position of oscillation peak is well controlled by  $V_{sg}$ . The slight decrease of  $I_{ds}$  at  $V_{sg} = -0.1$  V is attributed to the increase of the potential barrier height by negatively larger  $V_{sg}$ .

$\Delta V_{sg} = 100$  mV. The  $C_{sg}$  is estimated from the device geometry by the simple formula as follows:

$$C_{sg} = \epsilon_{SiO_2} \times \frac{W_{sg} \times W_{CH}}{T_{sg}} = 0.63 \text{ aF}. \quad (2)$$

This discrepancy means that Eq. (2) underestimates  $C_{sg}$  by neglecting the fringing capacitance component due to the poly-Si sidewall depletion gate wrapping SOI nanowire, as in the case of  $C_{cg}$ . But the error is larger in the case of the calculation of  $C_{sg}$ , because the sidewall depletion gate more closely covers the SOI wire than the control gate.

Finally, from the viewpoint of the SETT circuit, the resistance issue should be discussed. In our SETTs, the cross section of both the SOI nanowire and the sidewall depletion gate is so small that their resistances should be lowered. In the case of the SOI wire, its length should be decreased by the integration of many SETTs because the maximum limit of the cross section of the SOI nanowire manifests itself, in terms of the operation temperature and the theoretical premise about the resistance quantum (tunneling resistance  $\geq 26$  k $\Omega$ ). Because the sidewall depletion gate is made of highly  $n$ -doped poly-Si, its resistance issue is less conspicuous. The cross section of the sidewall depletion gate is correlated with both the resistance and the capacitance of electrically induced tunnel junction as is the case in that of the SOI wire, thus, there still exists its maximum boundary. To optimize the resistance issue, the nitride grooves of many integrated SETTs should be efficiently arranged, and the self-aligned doping technique by the ion implantation is necessary.

The properties of our SETTs are summarized as follows. First, scaling down of the size of Coulomb island is easier in comparison with SETTs relying on a special nanoscale lithography, in that the dimension of critical parameters (i.e.,  $W_{CH}$ ,  $S_{sg}$ , and  $W_{sg}$ ) depends on the controllability of CVD and RIE.

Second, the formation of the Coulomb island beyond the feature size of state-of-the-art lithography is possible, by the combination of the conventional lithography and process technology, which guarantees the compatibility with CMOS technology.

Third, the control of the position of the Coulomb oscillation peak is possible without additional gate electrode, since the poly-Si sidewall depletion gates play two major roles in the formation of tunnel junctions and the control of peak position. Thus, our device provides a variety of possibilities in the integrated SETT circuit application.

#### IV. CONCLUSIONS

We have developed a fabrication method for SETTs, based on a lightly *p*-doped SOI MOSFET with the depletion gate by using the combination of conventional lithography and process technology. The key fabrication method consists of two sidewall process techniques, which are the patterning of a uniform SOI nanowire and the formation of *n*-doped poly-Si sidewall depletion gates. The feature of our technology is that the scaling limit is not influenced by the limit of lithography but by the controllability of CVD and RIE.

Critical device parameters are controlled by the device geometry design, and single-electron tunneling phenomena in an electrically defined single island having various sizes are clearly observed at 77 K. A voltage gain larger than one and the controllability of Coulomb oscillation peak position are also successfully demonstrated, which are essential conditions for the practical integration of SETTs. Further miniaturization and optimization of our SETTs will make it possible to develop controllable and reproducible SETTs operating at room temperature.

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