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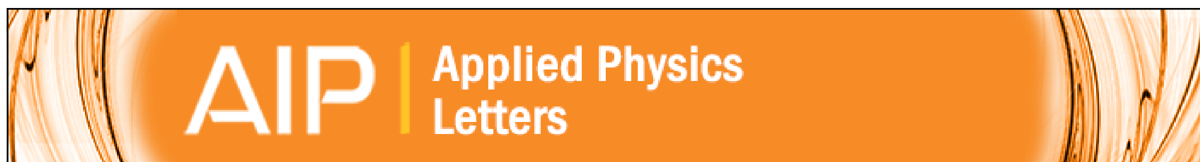

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Determination of energy levels of surface states in GaAs metal–semiconductor field-effect transistor using deep-level transient spectroscopy

Kyoung Jin Choi and Jong-Lam Lee[a)]
Department of Materials Science and Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Kyungbuk 790-784, Korea

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The energy levels of surface states at the surface of GaAs were determined through capacitance deep-level transient spectroscopy of GaAs metal–semiconductor field-effect transistor with large gate periphery. Two types of hole-like traps are observed in the spectra. These originate from the surface states at the ungated regions between gate and source/drain electrodes. The activation energies of both surface states are determined to be 0.65 ± 0.07 and 0.88 ± 0.04 eV, which agree well with the energy levels of As_{Ga}^{+} and As_{Ga}^{++} within band gap of GaAs, responsible for the Fermi level pinning at the surface. © *1999 American Institute of Physics.* [S0003-6951(99)00808-6]

Surfaces of compound semiconductors are very active for the chemisorption of the impurities, the oxygen atom, and the metallic elements, even in relatively small quantities on the clean surface. The oxygen atoms chemisorbed at the clean surface of GaAs can induce point defects through dissipation of the heat of condensation, resulting in the formation of point defects on the surface, such as the vacancies and the antisites.[1] Such surface states play a role in pinning the Fermi level at the energy levels which are positioned at the near center of band gap of GaAs.

The surface states act as recombination centers for free carriers, leading to the undesirable electrical properties, such as the transconductance dispersion,[2] the hysteresis in current–voltage *(I–V)* characteristics,[3] and the low breakdown voltage behavior[4] in metal–semiconductor field-effect transistors (MESFETs). The understanding on the nature of the surface states could be a key to solve the problems. However, only a few works were reported on this. The As antisites, As_{Ga}^{+} and As_{Ga}^{++} have been defined as the surface states, the energy levels of which were measured to be 0.65 and 0.9 eV apart below the conduction band edge using electron paramagnetic resonance measurements.[5]

The deep-level transient spectroscopy (DLTS) is a promising tool in obtaining information about traps in semiconductors, such as the activation energy, the capture cross section and the density of traps. In the DLTS measurement of MESFET under a negative bias, electrons emitted from gate could be captured by the trap at the surface exposed between gate and source/drain electrodes, exhibiting trap signals for such surface states. Thus, one could obtain the information for the surface states if MESFETs with large gate periphery are examined using DLTS. No works have been, however, conducted on this.

In the present work, GaAs MESFETs with large gate periphery were used to observe the surface states using capacitance DLTS technique. From this, the activation energy of each surface state was determined. The characteristics of traps in the MESFETs were examined by changing both sampling time in capacitance transient and magnitude of reverse bias. The results will be used to propose the energy levels of surface states within the band gap of GaAs.

Figure 1 shows the schematic cross-sectional diagram of GaAs MESFET used in this study. The layer structure was prepared by molecular beam epitaxy on semiinsulating GaAs wafer. The structure consists of a 1-μm-thick undoped GaAs buffer layer on the substrate, a thin active layer doped to $3\times10^{17}/cm^3$, a thick active layer doped to $5\times10^{16}/cm^3$, and finally an undoped GaAs layer for surface passivation. Top layer of undoped GaAs has the role of protecting the active channel layer from surface defects caused by oxygen chemisorption.[6] MESFETs with a total gate width of 21.16 mm having 92 fingers with a width of 230 μm were fabricated on the substrate. Gate-to-source and gate-to-drain spacings were 0.5 and 1.1 μm, respectively. The MESFETs were loaded in a variable-temperature cryostat, and capacitance DLTS measurements were made using a 1 MHz capacitance meter, a pulse generator, and a temperature controller. The temperature of the device was cooled down below 90 K using liquid nitrogen and heated until 400 K.

I–V characteristics of the GaAs MESFET were mea-

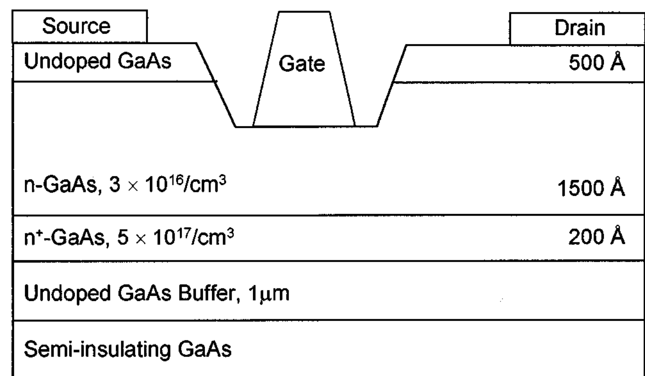

FIG. 1. Schematic cross-sectional diagram of the GaAs MESFET used in DLTS measurement.

a)Author to whom correspondence should be addressed. Electronic mail: jllee@vision.postech.ac.kr

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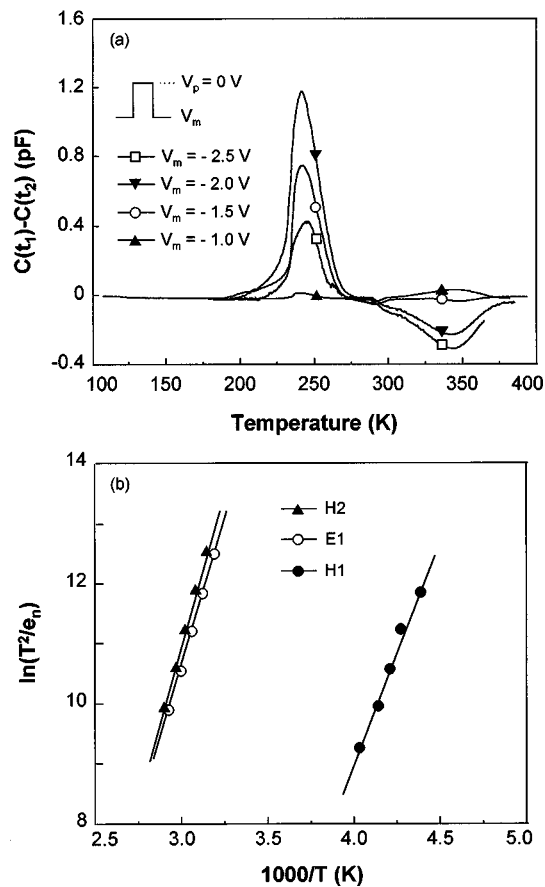

FIG. 2. (a) Capacitance DLTS spectra of GaAs MESFET with multifinger gate (total gate width =21.16 mm). (b) The temperature dependence of H1, H2, and E1 traps.

sured by pulse signal with a period of 0.1 ms. The pinch-off voltage is measured to be −2.1 V. The maximum drain current, measured at $V_{gs}=+0.5$ V, is 5.9 A and its density is 279 mA/mm. The saturated drain current and its density are evaluated to be 5.0 A and 236 mA/mm, respectively. Figure 2(a) displays the DLTS spectra of the MESFET. The reverse bias (V_m) applying to the gate was changed in the range of −1.0–−2.5 V with a step of 0.5 V, keeping a constant pulse bias (V_p) of 0 V. The DLTS signal corresponds to the difference between capacitances measured at different sampling times. The capacitance at a sampling time t_2, $C(t_2)$, was subtracted from that at an initial sampling time t_1, $C(t_1)$. Thus, the positive signal in DLTS spectrum corresponds to a hole trap, and the negative one is an electron trap. Two types of hole trap-like signals are observed at 250 K (labeled as H1) and 340 K (labeled as H2) when the MESFET was measured at $t_1=50$ ms and $t_2=200$ ms. The height of H1 peak is increased as V_m is decreased from −1.0 to −2.0 V. Meanwhile, the H2 peak disappears and an electron trap appears at 340 K (labeled as E1) when the V_m is lower than −1.5 V. Note that the hole-like peaks begin to be observed at the reverse bias of −1.0 V which is higher than the pinch-off voltage of the device, −2.1 V. This supports that the hole trap-like signals observed are related to the surface states at the ungated regions rather than to the hole traps at the interface of active layer with substrate.

The temperature dependence of H1, H2, and E1 are shown in Fig. 2(b). The activation energies and the capture cross sections for these traps determined are summarized in Table I. Note that the height of H1 peak is decreased at reverse biases smaller than −2.5 V. This is due to the increase of depletion layer width in the undoped GaAs buffer layer, via the decrease of $C(t_1)$ at reverse biases lower than the pinch-off voltage of −2.1 V.

TABLE I. Activation energies and the capture cross sections for H1, H2, and E1.

Type of trap	Activation energy (eV)	Capture cross section (cm^2)
H1	0.65±0.07	9.2×10^{-13}
H2	0.88±0.04	7.6×10^{-14}
E1	0.84±0.01	4.0×10^{-14}

There are a number of types of electron traps in GaAs. The EL2 trap, commonly observed in GaAs, acts as a role in producing the semi-insulating property of GaAs. The activation energy of EL2 was reported to be in the range of 0.80 ±0.06 eV.[7] Thus, the E1 peak in Fig. 2 is believed to be EL2 because its activation energy, 0.84±0.01 eV, agrees well with that of EL2.

The two types of hole trap-like signals in Fig. 2 originate from surface states produced on the surface of GaAs between gate and source/drain. When the reverse bias is applied to the gate, a high electric field is concentrated at edges of the gate toward source and drain. Thus, electrons are emitted from the gate electrode onto the ungated surface of device. Some electrons are swept away into the ohmic contacts, but remaining is captured by the surface states, leading to the increase of depletion layer width under the ungated regions. The increase of the depletion layer width results in the positive capacitance transient, namely hole trap-like signal in DLTS spectra.

The peak height of H1 trap changes with the period of t_1, as shown in Fig. 3. The increase of t_1 leads to the shift of the peak to lower temperatures. The height of EL2 peak is independent of the peak temperature, which is consistent with the results previously reported.[8] But, the height of H1 peak is abruptly increased with the peak temperature, namely, the temperature dependence of electron density in the H1 trap. This can be explained by the temperature dependence of the thermal emission current from the gate edge to the ungated regions in the DLTS measurement.

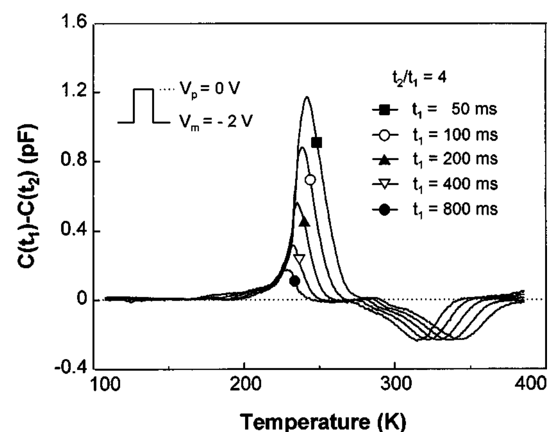

FIG. 3. Temperature dependence of the peak heights of H1 and E1 traps. The value of t_2 was set to be $4t_1$ at the constants of V_p and V_m.

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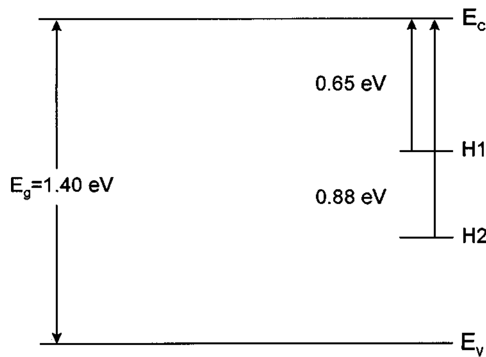

FIG. 4. Energy levels of surface states within the band gap of GaAs, determined using DLTS measurements.

The temperature dependence of thermal emission current from metal to semiconductor is expressed as in Eq. (1);[9]

$$J_{m\rightarrow s} \propto \frac{A^*T}{k} \exp\left(\frac{-q\phi_{Bn}}{kT}\right), \quad (1)$$

where A^* is the Richardson constant, k, the Boltzmann constant, T, the temperature, ϕ_{Bn}, the barrier height for electrons. The ratio of thermal emission current at 277 K ($t_1 = 800$ ms) to that at 243 K ($t_1 = 50$ ms) is calculated to be 0.065. This means that the current produced by electrons from the gate edge increases with temperature, resulting in the drastic decrease of the peak height for the surface trap H1, as shown in Fig. 3. Consequently, the hole trap-like signals observed in Figs. 2 and 3 are due to surface states at the ungated regions between gate and source/drain electrodes, acting as trapping sites for electrons emitted from gate edge during the reverse bias.

The activation energies of H1 and H2 traps obtained are directly related to the energy levels of surface states within band gap of GaAs. Figure 4 displays the energy levels for the surface states of H1 and H2. The energy levels of H1 and H2 are 0.65 and 0.88 eV apart below the conduction band edge, respectively, plotted in Fig. 4. These energy levels agree well with those of arsenic antisite responsible for Fermi level pinning at the surface of GaAs, namely, 0.65 eV for As_{Ga}^{+} and 0.90 eV for As_{Ga}^{++} apart below the conduction band edge.[5]

In conclusion, two kinds of hole trap-like signals with activation energies of 0.65 ± 0.07 and 0.88 ± 0.04 eV and one kind of electron trap signal with that of 0.84 ± 0.01 eV were observed in capacitance DLTS measurements on GaAs MESFETs with large gate periphery. The peak height of the hole trap-like signal (H1) was abruptly decreased with peak temperature. This is due to the fact that the current produced by electrons from the gate edge is increased with temperature. This provides evidence that the hole trap-like signals originate from the surface states at the ungated regions between gate and source/drain electrodes. The activation energies of both surface states agree well with energy levels of As_{Ga}^{+} and As_{Ga}^{++} within band gap of GaAs, causing the Fermi level pinning[5] at the surface.

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