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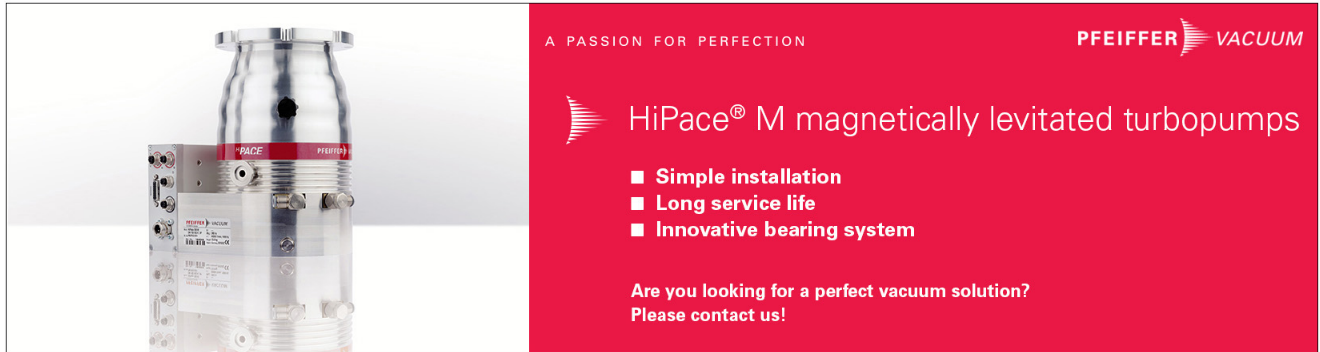

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Surface states on n-type $Al_{0.24}Ga_{0.76}As$ characterized by deep-level transient spectroscopy

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Surface states on n-type $Al_{0.24}Ga_{0.76}As$ were studied using capacitance deep-level transient spectroscopy (DLTS). Two types of hole-like traps (labeled as H1 and H2 in this work) were observed in a $Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As$ pseudomorphic high-electron-mobility transistor with a multifinger gate. But, no hole-like traps were observed in the fat field-effect transistor (FATFET) having a negligible ratio of the ungated surface to the total area between the source and the drain. This provides evidence that the hole-like trap peaks in the DLTS spectra originated from surface states at the ungated $Al_{0.24}Ga_{0.76}As$ regions exposed between gate and source/drain electrodes. The activation energies for both surface states were determined to be 0.50 ± 0.03 and 0.81 ± 0.01 eV. The comparison of activation energies of the two surface states with the Schottky barrier height 0.66 ± 0.01 eV suggests that H1 and H2 are deeply related to the Fermi energy pinning levels at the $Al_{0.24}Ga_{0.76}As$ surface. © *2001 American Vacuum Society.* [DOI: 10.1116/1.1368679]

I. INTRODUCTION

Surfaces of compound semiconductors are very active for the chemisorption of impurities, oxygen atoms, and metallic elements, even in relatively small quantities on the clean surface. Oxygen atoms chemisorbed at the clean surface of GaAs can induce point defects through the dissipation of the heat of condensation, resulting in the formation of point defects below the surface, such as vacancies and antisites.[1]

Surface states act as recombination centers for free carriers, leading to undesirable electrical properties, such as transconductance dispersion,[2,3] hysteresis in current–voltage ($I-V$) characteristics,[4] reduction of free carriers in the channel,[5] and low breakdown voltage behavior[6] in field-effect transistors (FETs). The magnitude of transconductance dispersion depending on surface leakage current from the gate[4] could be reduced after surface passivation with Si_3N_4.[7] A reduction in the charge density was observed after the removal of the n-type GaAs layer between gate and source/drain electrodes. The gate-to-drain breakdown voltage was increased after the surface treatment of GaAs by $(NH_4)_2S_x$ solution.[8]

Deep-level transient spectroscopy (DLTS) is an effective tool in obtaining information about traps in semiconductors, such as the activation energy, the capture cross section, and the density of traps.[9] In DLTS measurements of FETs, anomalously large hole-like signals were frequently observed.[10–13] Blight *et al.*[10] observed hole-like signals using conductance DLTS technique and attributed their origin to surface states between gate and source/drain electrodes. The fingerprint of the hole-like signal was provided by observing the temperature and filling pulse time dependence on the change of the peak height of the hole-like signal.[11,12] In Magno *et al.*'s work,[13] current and capacitance DLTS measurements were performed on AlGaAs/GaAs high electron mobility transistors (HEMTs) before and after the accelerated lifetime stress. After the accelerated lifetime stress, hole-like signals were detected by current DLTS measurements, but no minority-carrier signals were observed in capacitance DLTS spectra.

The Fermi level pinning at the surfaces of compound semiconductors has attracted much attention because of its academic and technological importance. The barrier height of an ideal metal/semiconductor contact is determined by both metal work function and the electron affinity of semiconductor. However, the barrier height at the interface of metal with a III–V semiconductor is virtually independent of the metal work function, because the Fermi level is pinned at the surface of GaAs by two types of surface states with activation energies of 0.65 and 0.9 eV below the conduction band edge. The possible origins for these surface states were attributed to the As antisites, As_{Ga}^{+} and As_{Ga}^{++} using electron paramagnetic resonance measurements.[14] In spite of important applications of $Al_xGa_{1-x}As$, such as HEMTs, heterojunction bipolar transistors, and laser diodes, no works on detailed information on surface states, such as their activation energies and capture cross sections, have been conducted yet.

In the present work, $Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As$ pseudomorphic HEMTs (PHEMTs) with different surface geometries were fabricated to find the surface states on n-type $Al_{0.24}Ga_{0.76}As$ using capacitance DLTS technique. The characteristics of traps in the PHEMTs were examined by changing both the sampling times in capacitance transient and magnitudes of the reverse and the filling pulse voltage. The results were compared with the Schottky characteristics of $Ti/Al_{0.24}Ga_{0.76}As$. From these results, it is proposed that surface states are responsible for the Fermi energy pinning at the $Al_{0.24}Ga_{0.76}As$ surface.

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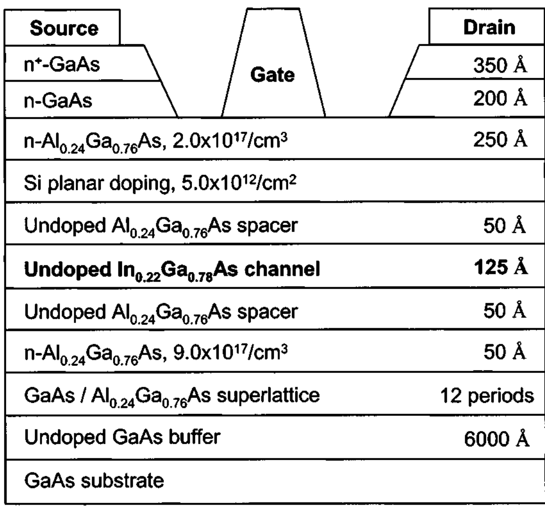
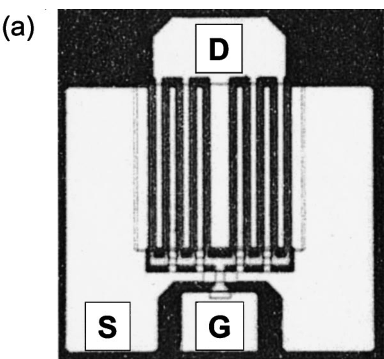


FIG. 1. Schematic cross-sectional diagram of the $Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As$ PHEMT fabricated in this work.

II. DEVICE FABRICATION AND MEASUREMENTS

The layer structure of a PHEMT was prepared by molecular-beam epitaxy on a semi-insulating GaAs substrate, as shown in Fig. 1. Details on the epitaxial structure are described elsewhere.[3] In order to investigate surface states on the ungated surface through DLTS spectra, two types of PHEMTs were fabricated on the same substrate. Top views of devices used are displayed in Fig. 2. One is a 2.5 mm wide PHEMT with ten fingers each of a gate width of 250 μm (multifinger-gate PHEMT). The gate length (L_g) was 0.8 μm, and gate-to-source (L_{gs}) and gate-to-drain (L_{gd}) separations were 1.0 and 1.5 μm, having an appreciable ungated surface with respect to the gate length. The other is a 150 μm wide PHEMT with a single finger (FATFET). L_g was 100 μm with 2 μm interelectrode spacings, having negligible ungated surface with respect to the gate length.

(a)



(b)

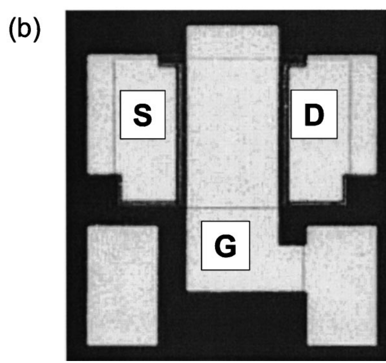


FIG. 2. Top views of two types of devices, (a) multifinger-gate PHEMT and (b) FATFET.

The active region was isolated by the mesa etching with H_3PO_4:H_2O_2:H_2O etchant. Ohmic metal, Au/Ge/Ni, was deposited by an electron-beam evaporator, followed by rapid thermal annealing at 380 °C for 10 s.[15] The typical value of specific contact resistivity was about $2\times10^{-6}\,\Omega\,\text{cm}^2$. The single recess structure was adopted for the gate region. A selective etching solution with a solution of 50% citric acid/H_2O_2 (1.5:1) was used to remove the 550-Å-thick GaAs cap layer.[16] The selectivity or the ratio of the etching rate of GaAs to AlGaAs was 143, and the etching rate of GaAs was 110 Å/s. Samples were dipped into the solution for 20 s, corresponding to the etching depth of 2200 Å for GaAs. Thus, even after the formation of the gate, the surface of *n*-type $Al_{0.24}Ga_{0.76}As$ at the vicinity of the gate edge is exposed to the air because lateral etching proceeds toward source and drain electrodes during etching, as shown in Fig. 1. The 0.5-μm-thick Ti/Pt/Au gate was then deposited on the top of the *n*-type $Al_{0.24}Ga_{0.76}As$ Schottky layer. Source pads were connected by a plated-gold airbridge with a thickness of 2.0 μm. Thinning the backside of the wafer to 100 μm, gold was deposited to reduce thermal resistance. All chips were mounted into ceramic packages before electrical measurements.

The devices were loaded into a variable-temperature cryostat and capacitance DLTS measurements were made using a 1 MHz capacitance meter, a pulse generator, and a temperature controller. The temperature of the device was cooled down below 90 K using liquid nitrogen and heated until 400 K.

III. EXPERIMENTAL RESULTS

The Schottky barrier height, ϕ_{Bn}, and the ideality factor, *n*, of the FATFET, were evaluated using Eqs. (1) and (2):[17]

$$\phi_{Bn}=\frac{kT}{q}\ln\left(\frac{A^*T^2}{J_s}\right), \tag{1}$$

$$n=\frac{q}{kT}\,\frac{\partial V}{\partial(\ln J_s)}, \tag{2}$$

where J_s is the reverse saturation current density of the Schottky diode, and A^* is taken to be 10.03 $\text{A/cm}^2/\text{K}^2$ in this work.[18] Using the earlier equations, ϕ_{Bn} and n were determined to be 0.66±0.01 eV and 1.6±0.04 eV, respectively.

From current–voltage characteristics of the multifinger-gate PHEMT, the pinch-off voltage was determined to be −0.8 V. The maximum drain current, measured at $V_{gs}=+0.8\,\text{V}$, is 0.76 A, and its density is 304 mA/mm. The saturated drain current and its density were evaluated to be 0.3 A and 120 mA/mm, respectively.

Figure 3 displays the DLTS spectra of the multifinger-gate PHEMT. The negative voltage (V_m) applied to the gate

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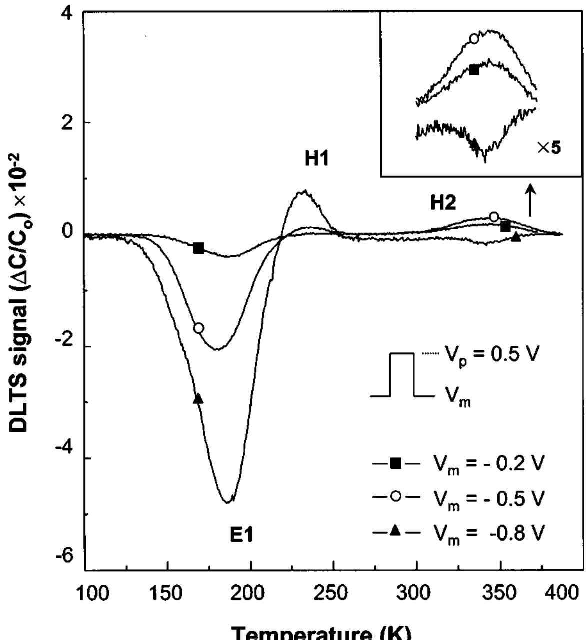

FIG. 3. Capacitance DLTS spectra of the $Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As$ PHEMT with the multifinger gate at V_m in the range of -0.2 to -0.8 V and a constant V_p of 0.5 V.

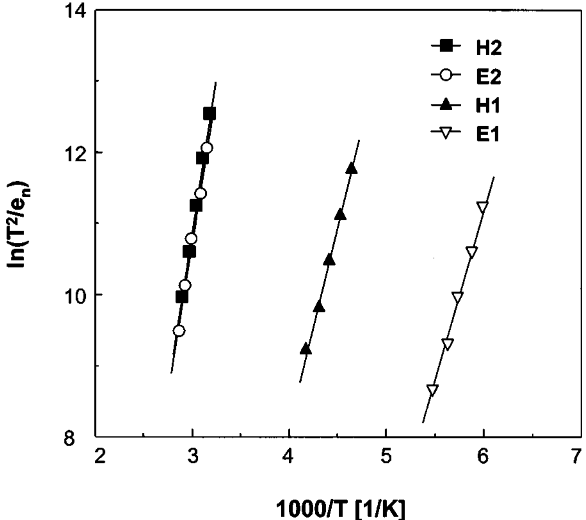

FIG. 4. Arrhenius plots for H1, H2, E1, and E2 traps, observed in the DLTS spectra.

was changed in the range of -0.2 to -0.8 V, keeping the filling pulse voltage (V_p) to be 0.5 V. Capacitance difference at two sampling times, namely $C(t_1)-C(t_2)$, was measured and normalized with the initial capacitance value C_0 at $t=0$, which is used as the DLTS signal in the plot. Thus, a positive signal in DLTS spectrum corresponds to a hole trap, and a negative one is an electron trap. Two types of hole-like signals were observed at 240 K (labeled as H1) and 340 K (labeled as H2), and two electron traps were observed at 190 K (labeled as E1) and 340 K (labeled as E2). As V_m was decreased from -0.2 to -0.8 V, heights of H1 and E1 were increased, but the H2 peak disappeared and a weak E2 peak was observed. The temperature dependencies of H1, H2, E1, and E2 are plotted in Fig. 4. The activation energies and the capture cross sections for these traps determined are summarized in Table I.

When $Al_xGa_{1-x}As\,(x>0.23)$ is doped with *n*-type dopants, *DX* centers, known as the complex of the substitutional donor atom with an unknown lattice defect, are generated. The E1 peak in Fig. 3 is believed to be due to *DX* centers because its activation energy, 0.42 ± 0.01 eV, agrees well with the previously reported value of *DX* center, 0.43 eV.[14,19] The EL2 trap, commonly observed in GaAs, acts as a role in producing the semi-insulating property of GaAs. The origin of EL2 is thought to be the As_{Ga}-related defect. Thus, it is reasonable that EL2 can exist in the AlGaAs layer. Indeed, in the previous DLTS studies on *n*-type AlGaAs performed by Yamanaka *et al.*, the ME7 peak was attributed to EL2.[20] The activation energy of EL2 reported was in the range of 0.80 ± 0.06 eV.[21] Thus, the E2 peak in Fig. 3 is believed to be EL2 because its activation energy, 0.76 ± 0.04 eV, agrees well with that of EL2.

In order to find the origin of hole-like signals, DLTS measurements were performed on the FATFET. Two electron signals corresponding to *DX* center and EL2 were only observed as shown in Fig. 5. In other words, no hole-like signals were observed. The gate area of the FATFET is 7.5 times larger than that of the multifinger-gate one, namely larger C_0 value in the FATFET. However, the ungated surface area of the FATFET is only 0.16 in comparison with that of the multifinger-gate one. Thus, if we assume that the hole-like signal is caused by surface states existing at the ungated surface, the calculated magnitude of the hole-like signal in the FATFET corresponds to 0.021 against the multifinger-gate PHEMT. This value is too small to be observed by DLTS measurements, which explains the disappearances of hole-like signals in the FATFET. This suggests that the hole-like signals originate from the surface states existing at the ungated $Al_{0.24}Ga_{0.76}As$ region between gate and source/drain electrodes.

IV. DISCUSSION

The hole-like signals were attributed to surface states existing on the ungated surface between gate and source/drain electrodes, because the height of the hole-like signal depends on the area of ungated surface region with respect to the gate area. This is consistent with Blight *et al.*'s works.[10] In their work, the height of the hole-like signal was proportional to the ratio of the ungated surface between gate and source/

TABLE I. Activation energies and the capture cross sections for H1, H2, E1, and E2 traps.

Type of trap	Activation energy (eV)	Capture cross section (cm^2)
H1	0.50 ± 0.03	2.4×10^{-14}
H2	0.81 ± 0.01	3.4×10^{-13}
E1	0.42 ± 0.01	1.5×10^{-14}
E2	0.76 ± 0.04	2.7×10^{-14}

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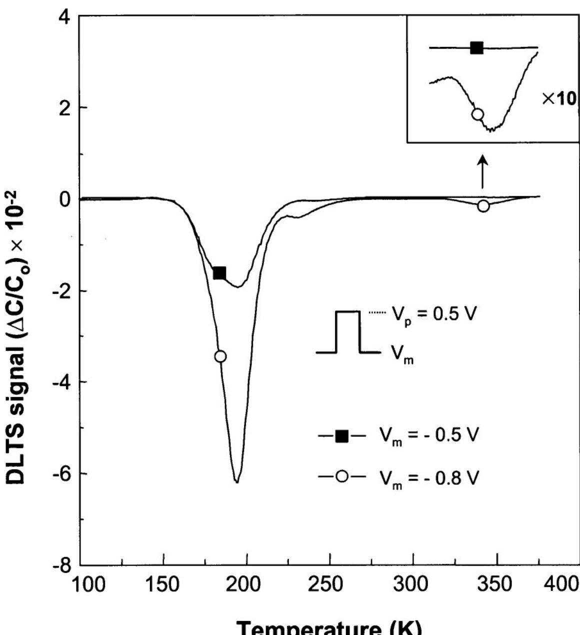

FIG. 5. Capacitance DLTS spectra of a FATFET fabricated on the same epitaxial layer as the multifinger-gate device as shown in Fig. 1.

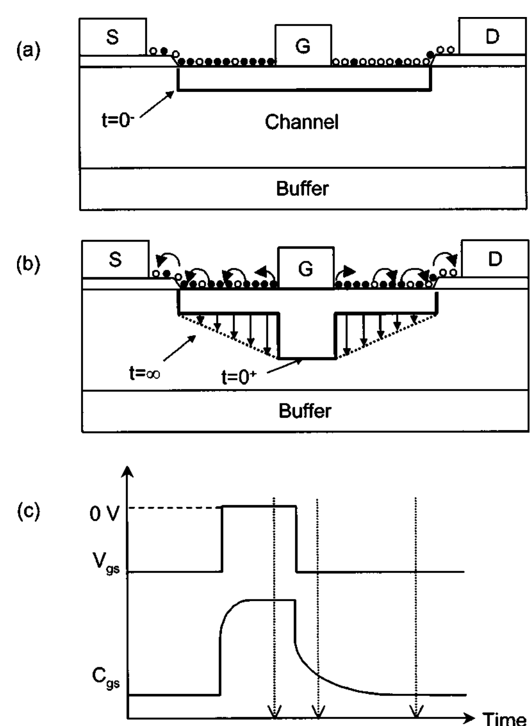

FIG. 6. Evolution of the hole-like signal due to surface states in the DLTS measurement of MESFET; (a) at zero bias to gate, (b) at reverse bias to gate, and (c) change of capacitance with time.

drain electrodes to the gated area. Namely, they could find hole-like signals in a short-gate FET ($L_g = 1\ \mu$m and $L_{gs} = L_{gd} = 2\ \mu$m) and even in a FATFET with an appreciable ungated surface with respect to the gate length ($L_g = 100\ \mu$m and $L_{gs} = L_{gd} = 10\ \mu$m). However, in a FATFET with a negligible ungated surface ($L_g = 300\ \mu$m and $L_{gs} = L_{gd} = 2\ \mu$m), no hole-like signals were observed. Similarly, we could observe hole-like signals in short-gate FETs ($L_g = 0.8\ \mu$m, $L_{gs} = 1.0$, $L_{gd} = 1.5\ \mu$m) and hole-like signals disappeared in the FATFET ($L_g = 100\ \mu$m and $L_{gs} = L_{gd} = 2\ \mu$m).

An experimental model for the hole-like signal due to surface states is shown in Fig. 6.[10] Due to the Fermi level pinning at the surface of $Al_xGa_{1-x}As$, the depletion layer width is approximately constant from the source to the drain at the gate voltage of zero, as in Fig. 6(a). Figure 6(b) shows the shapes of both depletion region edges under the gate and ungated surface between gate and source/drain electrodes when a reverse voltage is applied to the gate. Immediately after the application of a reverse bias, or $t = 0^+$, the depletion region edge under the gate quickly reaches to the steady state, drawn as the solid line in Fig. 6(b). At the same time, electrons begin to be injected from the gate edge into the ungated surface region. Some electrons are captured by surface states and the others are swept into the ohmic contacts through the channel. Electrons in surface states are drifted towards ohmic contacts through the surface by the repetition of trapping and detrapping. As a result, the charge state of surface trap changes to negative, leading to the increase of depletion width to maintain the charge balance with positive charges in the depletion region, drawn as a broken line in Fig. 6(b). Consequently, the evolution of positive capacitance transient is observed for the surface trap on the ungated region, displayed in Fig. 6(c). If the filling pulse voltage is applied again to the gate, electrons are begin to be emitted from surface states. As a result, the depletion region under the ungated surface is decreased and finally takes the shape of Fig. 6(a).

As stated in the previous paragraph, DLTS signals by surface states are caused by electron capture, injected from the gate during the reverse bias. Thus, if it is assumed that the concentration of injected electrons from the gate is much lower than that of surface states, electron injection might be the determining step in the generation of the hole-like signal. In order to investigate this effect, DLTS measurements were performed as a function of the period of t_1, as displayed in Fig. 7. The increase of t_1 leads to the shift of peaks to lower temperatures. Also, the height of H1 peak was abruptly decreased. It is known that a large activation energy of thermal capture cross section may result in the strong dependency of peak height.[22] Namely, the peak height decrease for decreased temperature. However, the decreasing rate is normally much smaller than that of hole-like signals observed in this study. This effect was clearly explained by the temperature dependency of electron injection from the gate into the ungated surface.[11,12] The thermionic emission current from metal to semiconductor is expressed by Eq. (3):[17]

$$J_{m\rightarrow s} \propto \frac{A^*T}{k}\exp\left(-\frac{q\phi_{Bn}}{kT}\right), \tag{3}$$

where A^* is the Richardson constant, k is the Boltzmann constant, and T is the temperature. The ratio of thermal emission current at 214 K ($t_1 = 800$ ms) to that at 238 K (t_1

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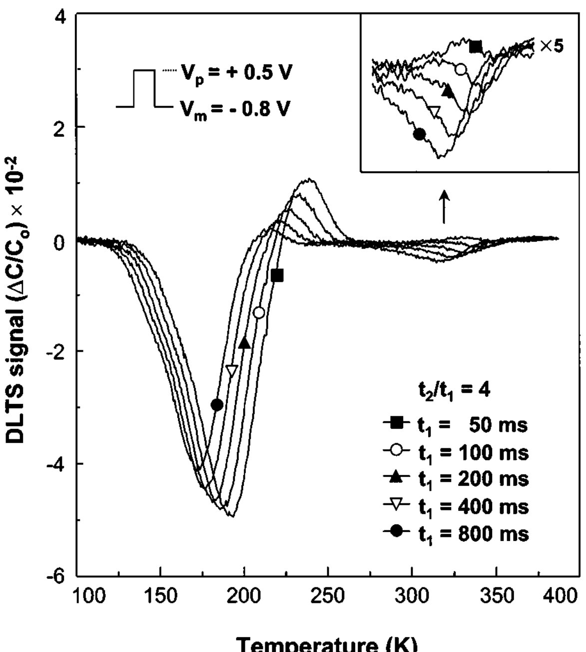

FIG. 7. Temperature dependence of DLTS peaks. The value of t_2 was set to be $4t_1$ at the constants of V_p and V_m.

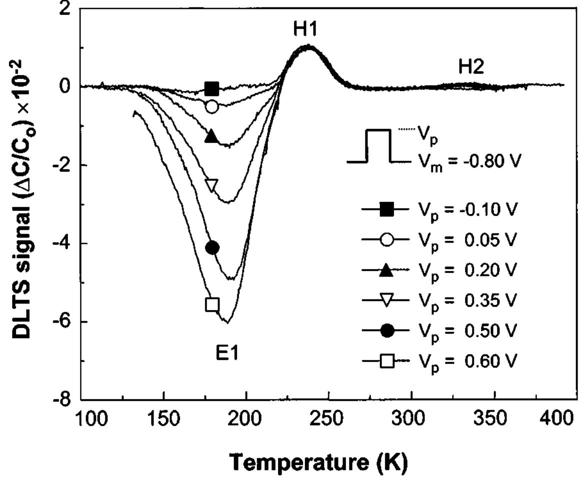

FIG. 8. DLTS spectra in AlGaAs/InGaAs PHEMT as a function of filling pulse voltages.

$=50$ ms) is calculated to be 0.018. This means that the number of electrons emitted from the gate edge decreases at the lower temperature, resulting in the drastic decrease of the peak height of H1 trap, as shown in Fig. 7.

The change in polarity of the 340 K peak with changes in the rate window could be explained by the rapid decrease of H2. The DLTS peak at 340 K is composed of H2 and E2, which were overlapped with each other. Consequently, the rapid decrease of H2 results in the increase of E2, because bulk electron traps are generally independent of the rate windows. For the change in polarity of H2 with the rate window, one can suspect that the capacitance transient is not exponential or the time between pulses may not be long enough. In order to check whether or not the transient is exponential, we directly measured the capacitance transient at $V_p=0.5$ V, $V_m=-0.8$ V, and $T=312$ K. From the linearity of the logarithmic capacitance with time evolution, the capacitance transient was found to be exponential. Also, in our DLTS measurements, the ratio of sampling times, t_2/t_1, was kept to be 4, where t_1 was changed from 50 to 800 ms. In other words, the rate window $(t_2-t_1)/\ln(t_2/t_1)$ was changed from 108 to 1731 ms, where the time between pulses was 3200 ms. This rules out the possibility that the time between pulses is not long enough.

Hole-like signals have been sometimes attributed to other origins than surface states between gate and source/drain electrodes.[23,24] Thus, it is worth while to check other possible origins for the surface states observed in this study. First, a positive DLTS signal was observed only near pinchoff biases in a GaAs metal–semiconductor FET (MESFET), which was attributed to hole traps existing at the interface of grown layer/substrate.[23] In this work, however, the hole-like peaks H1 and H2 begin to be observed at the reverse bias of -0.2 V which is higher than the pinchoff voltage of the device, -0.6 V. This means that the hole-like signals observed are not related to bulk hole traps existing at the interface of grown layer/substrate. Second, a positive DLTS signal was observed in an AlGaSb Schottky diode when the bias condition was forward ($V_p=0.6$ V, $V_m=-0.5$ V) and then disappeared when V_m is negative (-0.1 V).[24] This was explained by the hole capture at the electron trap. In this work, we have performed DLTS measurements as a function of V_p as shown in Fig. 8. V_p was changed from $+0.6$ to -0.1 V with a constant reverse voltage of -0.8 V. The H1 peak was independent of V_p and was observed even at V_p of -0.1 V, although the hole injection was not expected at such a bias condition. These results suggest that H1 is not the result of hole capture at an electron trap.

The ideality factor of our device ($n=1.6$) was measured to be rather high. This might be explained by the presence of an interfacial layer between metal and semiconductor.[25] The surface of $Al_xGa_{1-x}As$ is extremely reactive, especially at a high aluminum concentration. Thus, a thin oxide layer between metal and semiconductor is inevitable, unless the metal–semiconductor contacts are fabricated *in situ* in an ultrahigh vacuum. Indeed, ideality factors of *in situ* epitaxial Al on $Al_xGa_{1-x}As\,(0\leqslant x\leqslant 1)$ were less than 1.03, which means near-ideal Schottky diodes.[18] However, ideality factors of metal-$Al_xGa_{1-x}As$ contacts, exposed to air during device fabrication, were in the range of 1.15–1.3.[26,27] Furthermore, ideality factors were increased up to 1.68 after annealing at 300 °C.[27] The devices used in this work were annealed at 300 °C for 10 h for the enhancement of thermal stability. This could be a reason for such a high ideality factor in our devices.

Oxygen atoms in the air are known to actively react with the fresh surface of GaAs, and in turn, cause local migration of the host atoms to produce point defects at the surface.[25,26] It was observed that the Ga–O bond is stronger than that of As–O and that Ga atoms preferentially migrate towards the surface leaving vacancies behind in the subsurface region.

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This behavior can convert the subsurface layer into an As-enriched one. Namely, the excess elemental As could promote the creation of donor-type As_{Ga} defects at the subsurface of GaAs[28,29] through a reaction with Ga vacancies given by

$$V_{Ga}+As_{As}\rightarrow As_{Ga}+V_{As}. \quad (4)$$

This reaction is highly probable since the formation energy of As_{Ga} antisite defects is much lower than that of the vacancies.[30] There are two donor levels within the band gap of GaAs, responsible for Fermi level pinning at the surface of GaAs, namely, 0.65 eV for As_{Ga}^{+} and 0.90 eV for As_{Ga}^{++} apart below the conduction band edge.[1,14] The barrier heights of metal-GaAs Schottky contacts are about 0.8 eV, irrespective of the types of metals. Thus, it was suggested that both As_{Ga} antisites play a role to pinning the Fermi level on the surface of GaAs.

Surface oxides are more easily formed on $Al_xGa_{1-x}As$ than on GaAs, because the Al–O bond is stronger than the Ga–O one. This means that Al_2O_3 is the most favorable oxide in the *n*-type $Al_xGa_{1-x}As$ surface, leading to outdiffusion of Al atoms to the surface of $Al_xGa_{1-x}As$ to form Al_2O_3. Therefore, two types of As_{Al} donor defects, similar to the reaction expressed in Eq. (4), could be produced at the subsurface of $Al_{0.24}Ga_{0.76}As$:

$$V_{Al}+As_{As}\rightarrow As_{Al}+V_{As}. \quad (5)$$

The clean surface of $Al_xGa_{1-x}As$ is inevitably exposed to air during device fabrication processes, resulting in the formation of native defect on the surface of $Al_xGa_{1-x}As$. Considering the surface reaction on $Al_{0.24}Ga_{0.76}As$ is similar to that on GaAs, two types of donor, As_{Al}^{+} and As_{Al}^{++}, could be produced at the surface of $Al_{0.24}Ga_{0.76}As$.

The activation energies of H1 and H2 are directly related to the energy levels of surface states within the band gap of *n*-type $Al_{0.24}Ga_{0.76}As$. The energy levels of H1 and H2 are 0.50 and 0.81 eV below the conduction band edge, respectively. The Schottky barrier height of 0.66 eV lies between the energy levels of surface state H1 and H2. From this, H1 and H2 can be attributed to the Fermi energy pinning levels in AlGaAs surface. And the possible origins of H1 and H2 are related to the energy levels of As_{Al}^{+} and As_{Al}^{++}. Comparing the energy levels of H1 and H2 traps with those of As_{Ga}^{+} and As_{Ga}^{++}, it is suggested that energy levels of As_{Al}^{+} and As_{Al}^{++} are more near from the conduction band edge than As_{Ga}^{+} and As_{Ga}^{++}, respectively.

V. SUMMARY

$Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As$ PHEMTs with different surface geometry were studied, in order to observe surface states on *n*-type $Al_{0.24}Ga_{0.76}As$ using capacitance DLTS technique. Two kinds of hole-like signals with activation energies of 0.50±0.03 eV (H1) and 0.81±0.01 eV (H2), and *DX* center and EL2 signals with those of 0.42±0.01 eV and 0.76 ±0.04 eV were observed in capacitance DLTS measurements on multifinger-gate PHEMT. However, no hole-like signals were observed in the DLTS spectra of the FATFET, which has a negligible ratio of the ungated surface to the total area between the source and the drain. From this, the hole-like signals were attributed to surface states at the ungated $Al_{0.24}Ga_{0.76}As$ regions exposed between gate and source/drain electrodes. The peak heights of hole-like signals, H1 and H2, were abruptly decreased with the decrease of peak temperature, which was explained by the decrease of electrons injected from the gate into the ungated surface due to decreased temperature. The Schottky barrier height of 0.66 eV lies between the energy levels of surface state H1 and H2. From this, H1 and H2 could be attributed to the Fermi energy pinning levels in AlGaAs surface. Taking into account the stronger Al–O bond than any other bonds, the possible origins of H1 and H2 were attributed to As_{Al}^{+} and As_{Al}^{++}.

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