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High-yield TiO_2 nanowire synthesis and single nanowire field-effect transistor fabrication

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We report a facile method for synthesizing single-crystal rutile TiO_2 nanowires using atmospheric-pressure, chemical vapor deposition with Ti and TiO as precursors. The synthesis is found to depend critically on the predeposition of a layer of metallic Ti on the Ni catalysts layer. The omission of this step seems previously to have impeded the efficient synthesis of titania nanowires. Single-nanowire field-effect transistors showed the TiO_2 nanowires to be *n*-type semiconductors with conductance activation energy of ~58 meV.
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One-dimensional (1D) nanostructures of metal oxide semiconductors are currently the subject of intense research both in order to discover fundamental sciences at the nanoscale as well as for their potential in electronic and optoelectronic device applications such as nanolasers,[1] solar cells,[2] and nanosensors.[3] In particular, TiO_2 nanostructures have received considerable attention as attractive building blocks as gas sensors, photovoltaic cells, and photocatalysis cells.[4–6] In addition to their attractive physicochemical properties, TiO_2 materials have distinct real-world advantages including low toxicity and environmental safety. A number of wet-chemical methods, such as the sol-gel process,[7] hydrothermal synthesis,[8] and electrochemical synthesis,[9] have been recently developed for producing TiO_2 nanostructures. Wet-chemical syntheses may, however, introduce contaminants; they are difficult to integrate with conventional wafer processing. Although a few reports exist on the synthesis of TiO_2 nanowires by catalyst-assisted vapor-phase synthesis,[10–12] in which a Ni or Au thin layer was used as catalyst material, finding reliable conditions under which high-quality TiO_2 nanowires are produced efficiently remains a challenge.

Once synthesized, it becomes important to evaluate the electronic properties of TiO_2 nanowires in nanoscale devices. Crucial parameters for electrical performance, such as the carrier concentration, mobility, and bandgap, strongly depend on the details of the growth. Among the various options for carrying out such measurements, the field-effect transistor (FET) is a good candidate device for characterizing nanowires. Recently, FETs made of various metal oxide nanowires, such as ZnO (Ref. 13) and SnO_2 (Ref. 14), have been shown to function as gas sensors, switching devices, and in several other applications. However, no report has yet appeared on an FET based on TiO_2 nanowires except for some preliminary results on Co-doped TiO_2 nanowires[8] synthesized in AAO templates. Here, we report on the fabrication of FETs using TiO_2 nanowires.

Single-crystalline TiO_2 nanowires were grown by atmospheric-pressure chemical vapor deposition (APCVD). Briefly, single crystal (100) Si wafers covered with a 200 nm thick SiO_2 layer were overcoated with a 50 nm thick Ti layer using e-beam vapor deposition. A ~2 nm Ni thin film was then coated onto the Ti layer. Fine meshed TiO (0.5 g) (99.95%, Aldrich) was loaded at the center of a 5 cm long quartz boat. The $Ni/Ti/SiO_2$ substrate assembly was placed in the quartz boat approximately 5 mm from the TiO powder. The quartz boat was placed in a quartz tube furnace and heated over a 10 min period to a temperature in the range of 850–950 °C in air and then kept at that temperature for an additional 10 min. High purity Ar carrier gas (99.999%) was introduced with a flow rate of 200 SCCM (SCCM denotes cubic centimeter per minute at STP) at the growth temperature for 2 h. High yields of good-quality TiO_2 nanowires were only obtained when the entire procedure was conducted at atmospheric pressure. The structures and morphologies were examined using scanning electron microscopy (SEM) (FEI Sirion) and high-resolution electron microscopy (HRTEM) (FEI Tecnai G2 F30 S-Twin).

Figure 1(a) shows a low magnification SEM image of products grown on a $Ni/Ti/SiO_2$ substrate, patterned using conventional photolithography. Large quantities of long nanowires with well-defined shapes and random orientations are observed to grow only on the surface covered by Ni/Ti. The majority of the nanowires grown were straight and retained the nearly spherical catalyst particle from which it grew at one tip [inset to Fig. 1(a)] reminiscent of nanowires grown by vapor-liquid-solid (VLS) synthesis.[15] The lengths of most of the nanowires fell in the range of 10–30 μm, with a mean diameter of ~48 nm and a narrow distribution width ~ ± 11 nm [Fig. 1(b)]. Energy dispersive x-ray spectroscopy measurements show that, while the catalyst particle consists of Ni, Ti, and O atoms, the nanowire consists only of Ti and O. Moreover, the nanowires were single crystals as shown by the clear and regular lattice fringes [Fig. 1(c)]. Selected area electron diffraction indicted lattice constants $a=0.473$ nm and $c=0.310$ nm, corresponding to the (101) and (110) planes of rutile TiO_2, respectively. This suggests that this nanowire grew along the [110] crystallographic direction.

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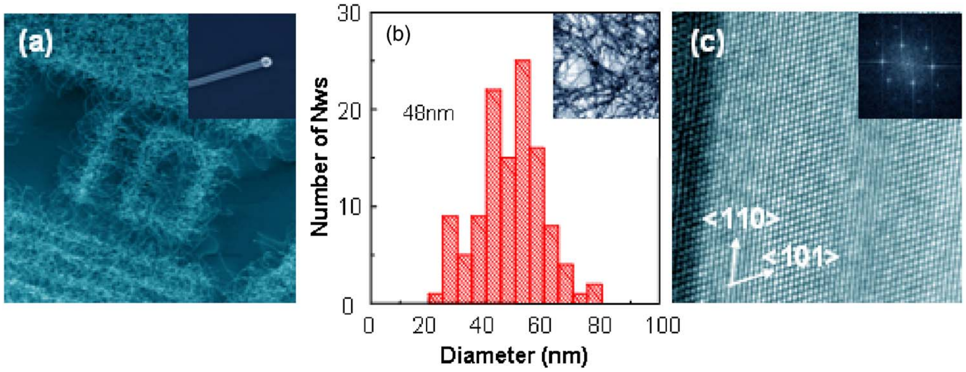

FIG. 1. (Color online) (a) Low magnification SEM image of large-scale TiO_2 nanowires formed on a patterned $Ni/Ti/SiO_2$ substrate. (Inset) High-magnification SEM image of a single TiO_2 nanowire. (b) Nanowire diameter distribution determined by low-magnification TEM imaging (inset) of as-grown (at 950 °C) TiO_2 nanowires. (c) HRTEM image of a single nanowire.

Although the presence of a small catalyst particle implies a VLS growth mechanism, a number of observations suggest that the mechanism differs somewhat from the VLS process as it is normally understood. These aspects, which are currently being investigated and will be the subject of a separate publication, include: (i) an unusual interface region which contains a significant amount of Ti metal and (ii) the need to precoat the substrate with Ti metal. Indeed, no nanowires grew in the absence of this pre-coating procedure [Fig. 2(a)]. Additionally, nanowire growth was optimal only when a certain range of Ti metal thicknesses was used. Figure 2 shows that a 5 nm Ti overcoat is not sufficient; 20 nm Ti results in very good growth while 500 nm of Ti [Fig. 2(d)] results in the growth of rather irregular structures that for the most part do not resemble nanowires and might, in fact, not have involved the catalyst at all. Unlike traditional VLS, it appears (and this is being currently verified) that the nanowire growth is external to the catalyst droplet with much of the Ti metal precursor being provided by metal present at the interface region between the catalyst particle.

The FETs based on single TiO_2 nanowire were fabricated by transferring the nanowires onto a thermally grown silicon dioxide layer on a *p*-type silicon wafer substrate which served as the back gate. The source and drain electrodes were fabricated using conventional photolithography with the Ti/Al/Au (10/100/200 nm) electrodes deposited using e-beam evaporator. The fully fabricated samples were annealed for 1 min by rapid thermal annealing under nitrogen atmosphere from 200 to 500 °C and the electrical transport measurements (I_{sd} versus V_{sd}) were carried out at room temperature. Experience shows that such rapid annealing does not oxidize the aluminum layer, although the Ti might convert to an oxide. As a result, the Ohmic nature of the contacts is not compromised as the linear currents versus voltage characteristics [Fig. 3(a)], in fact, suggests. (Although one cannot eliminate the possibility that Ohmic junction resistances are present.) The dramatic decrease in the resistance after annealing to 300 °C and above is likely due to the formation of oxygen vacancies. The resistance dropped to values as low as 18 MΩ in samples annealed to 500 °C. For samples annealed to 500 °C the nanowire resistance (V_{sd}=10 V) increases approximately linearly with the nanowire cross-sectional area [Fig. 3(b)], implying rather uniform electrical materials characteristics for the nanowires, more or less, independent of their diameters over the range.

Figure 4(a) shows I_{sd}-V_{sd} curves for the gate bias (V_g) of samples annealed at 500 °C. The increase (decrease) in conductance with increasingly positive (negative) V_g indicates the nanowires to be *n*-type. The measured I_{sd} dependence on temperature (at a constant value V_{sd}=10 V) is shown in Fig. 4(b). It follows the expected activated conductance relationship,

$$I_{ds} = I_0 \exp\left(\frac{-E_E}{k_B T}\right). \tag{1}$$

Plotting the logarithm of the current versus the inverse absolute temperature [Fig. 4(b), inset] produces a straight line

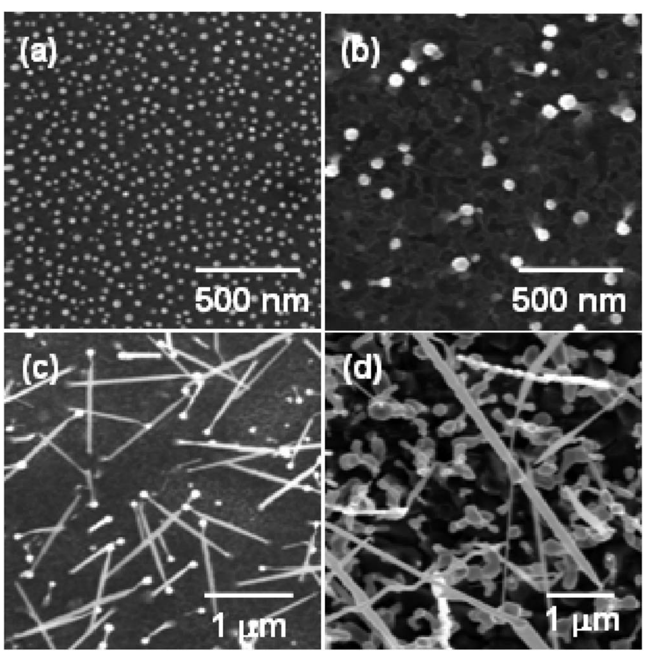

FIG. 2. SEM images of TiO_2 nanowires produced by varying the thickness of Ti layer predeposited on the SiO_2 substrate. (a) $Ni(2\ nm)/SiO_2/Si$, (b) $Ni(2\ nm)/Ti(5\ nm)/SiO_2/Si$, (c) $Ni(2\ nm)/Ti(20\ nm)/SiO_2/Si$, and (d) $Ni(2\ nm)/Ti(500\ nm)/SiO_2/Si$.

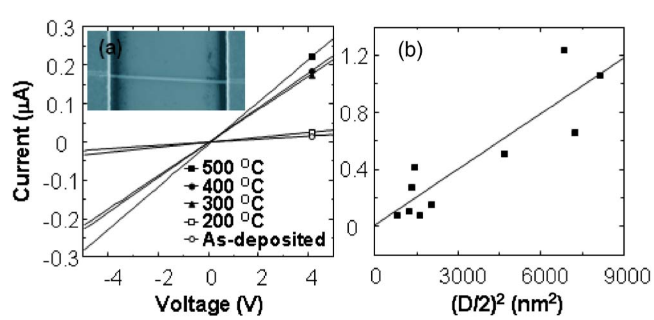

FIG. 3. (Color online) (a) Current-voltage of single TiO_2 nanowires configured as FETs measured at room temperature after the device was annealed to the temperatures indicated. (b) The nanowire resistance as a function of the square of the radius of the nanowire, for nanowires annealed to 500 °C.

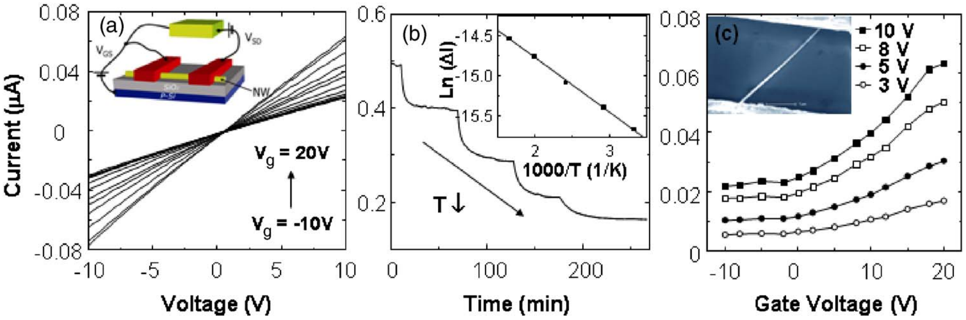

FIG. 4. (Color online) (a) Gate voltage dependence of I_{sd} vs V_{sd} of a single TiO_2 nanowire configured as a back-gated FET. (b) Current measured through a TiO_2 nanowire (at constant source-drain voltage) as a function of temperature. Inset: Ln current vs inverse temperature. (c) I_{sd} vs V_G for a TiO_2 nanowire for various values of V_{sd}. All *I-V* curves were obtained at an ambient pressure under 5×10^{-6} Torr.

corresponding to an activation energy value of 58.3 meV, consistent with published values for bulk rutile TiO_2.[16] The transfer characteristics of the TiO_2 nanowire FET were also examined and shown in Fig. 4(c). From the linear region of the curve, the threshold gate voltage (V_{th}) and the transconductance ($g_m = dI_{ds}/dV_g$) are determined to be -5 V and 1.70 nS, respectively. The value of the field-effect mobility μ_e of the device was estimated using the expression,[14]

$$\mu_e = g_m \frac{L^2}{CV_{ds}}, \tag{2}$$

where L (4.0 μm) is the nanowire device's channel length, and C is the capacitance of the back gate, approximately 56 aF/μm using the expression for the capacitance of a cylinder resting on a dielectric-covered plane,

$$C = \frac{2\pi\varepsilon\varepsilon_0 L}{\cosh^{-1}[(2h+r)/r]}. \tag{3}$$

The relative dielectric constant (ε) of SiO_2 was assumed to be 2.5, and h is the thickness of the layer. Using these formulas we estimated the mobility to be $\sim 0.2\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$, consistent with values reported for single-crystalline TiO_2 films.[17] Finally, an on/off ratio of approximately 3 was obtained by changing the gate voltage from -20 to $+10$ V; the saturation transconductance was found to be ~ 3 nS. This low on/off ratio compared with the threshold voltage may result from the presence of contact resistances that are not insignificant compared to the resistance of the nanowire. The electron concentration in the nanowire was calculated to be $\sim 4.5\times10^{17}\ \text{cm}^{-3}$, lower than values reported for TiO_2 films.[18] This implies that the oxygen vacancy concentration is relatively low.

In summary, we report a facile synthesis of good-quality single crystalline, rutile TiO_2 nanowires using APCVD. Most nanowires were observed to have a nickel nanoparticle at one tip. The synthesis is found to depend critically on the predeposition of a layer of metallic Ti on the substrate prior to the deposition of the Ni catalysts layer. Single-nanowire FETs showed the TiO_2 nanowire to be *n*-type semiconductor with a gate-bias-induced on/off ratio ~ 3. The FETs produced possess properties already suitable for applications as sensors.

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