ISOLATING POWER AMPLIFIERS FOR PARALLEL TRANSMIT MRI

A Dissertation

by

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ABSTRACT

A radio frequency parallel transmitter was developed for magnetic resonance imaging. Eight channels of vector modulation and isolating power amplifiers were constructed so that the performance of different amplifier architectures could be investigated. An eight channel system was implemented and tested using both quantitative bench measurements and imaging experiments. The imaging experiments were performed on three separate MR systems at 3T, 4.7T, and 7T at different sites using both B_1 shimming and fast modulation techniques.

The modulation system implemented is based on vector modulators in order to simplify integration with existing MRI systems. Current Source and Low Output Impedance amplifiers were built and compared in terms of theory of operation, their ability to isolate array coils, and the amount of power they can deliver to a coil. The current source amplifiers function by introducing a high impedance in series with the coil which is series resonant. In contrast, the low output impedance amplifiers present a low impedance to the coil which has a matching network that forms a parallel resonant tank. Both are able to provide isolation, with the current source amplifiers producing in excess of 30dB of isolation and low output impedance amplifiers providing approximately 12.5dB in practical situations. The current source amplifiers can only produce approximately 10A (or between 150W and 300W) of output power because they are not power matched. In contrast, the low output impedance amplifiers can produce roughly 1kW (the device rating) because they are power matched. Ultimately, there is no single best architecture of power amplifiers at this time. Standard amplifiers are useful when only one or two transmit channels are needed and broad-bandedness is valuable. Current source amplifiers are best suited to situations where very high channel counts are needed because of their high isolation. Low output impedance amplifiers are most useful with moderate channel counts because they provide some isolation at moderately high powers.

DEDICATION

Whatever you do, work at it with all your heart, as working for the Lord, not for human masters…

~Colossians 3:23~

ACKNOWLEDGEMENTS

I would like to thank all of the various people who were involved with and helped me complete this work. I must start with my parents, as with most things in life. They raised me with a love of knowledge, a willingness for hard work, and the shear bullheaded stubbornness that life demands at times. My brother and sister, Eric and Anya, who's pushing, goading, taunting, and willingness to remind my parents that yes, higher education can take time, was also of immense value. There were so many others who moved through my life at an early age, shaping me that I can hardly do them justice here in a few short words.

My now wife, Liz, has been supportive and tolerant through a difficult process. Her love and willingness to stand by me and support me has been a boon to my heart and soul. My many friends, many of whom have listened to my jokes and complaints about the process and problem of getting this done. Their commiseration and retorts lifted my spirits during low times.

There was no shortage of lab-mates who's help and knowledge must be acknowledged. Ke Feng, who I worked with at the start of my graduate work and always held a practical "make it work" stance. John Bosshard, who's tenure in the lab continues to overlap mine, held a mentality of theoretical perfection and elegance. Katie Moody, who has eaten with me at Pizza House at 1AM more times than is completely seemly, and built the other half of the system that is described here. Stephen Ogier, who suffered my desire to make everything just a little smaller, but helped push this work through. Jon-Fredrik Nielson, Doug Noll, and the various students at the University of Michigan that I subjected to late nights at the scanner made this whole effort both possible and valuable.

Dr. Steve Wright, who advised and pushed me through-out this process. His experience and insights helped make this project possible. He created a lab and environment in which I and others could do work that is rarely, if ever, possible at any other lab in the world. Without his years of effort there is, without a doubt, no way I would have completed this work. Dr. Mary McDougall, who has been intimately involved with this project and advised Katie in her work. Her joint lab brought skills and expertise that we would not have otherwise had, and made this work feasible.

I cannot, in a span of a few words, truly express the value that so many people have added to my life, and in consequence my work. I have made note of just a few that have come to mind as having especially marked this part of my life. There is no doubt that I have forgotten, neglected, or missed many who have impacted my work to this point. Please do not think less of me for this, if I were to simply write a few words for each person then this volume would double in length.

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CHAPTER 1
INTRODUCTION

Magnetic Resonance Imaging (MRI) has developed from its roots in Nuclear Magnetic Resonance (NMR)[1], [2]. Lauterbur first demonstrated the ability to spatially localize using a modified NMR system in 1973[3]. From there it has developed into an imaging technique marked by flexibility. Contrast can be developed from such diverse mechanisms as material properties (T_1 and T_2), water concentration, fluid flow[4], diffusion[5], [6], material stiffness[7], blood oxygenation[8], and many others. Achieving the possibilities of MRI has consistently brought us to odds with the very physics of the NMR phenomenon. Development of new techniques and hardware has made good on many promises, and opened the doors to yet new possibilities.

MRI has seen major advancements from its beginnings as a modified version of NMR. The development of imaging specific routines and hardware has moved MRI from being able to distinguish between a few test tubes to being one of the premier medical imaging modalities. These advancements occurred across the board, on the software/pulse sequence side it includes (but is hardly limited to) new pulse sequences that provide faster imaging[9], new contrast mechanisms[4], [6], [8], and an ever evolving panoply of specialized sequences[10]. The hardware has seen similar revolutions, with larger, stronger, better magnets[11], new coil designs[12], receive arrays for better SNR[13]–[15] and faster imaging[16], [17], and now transmit arrays[18]–[20].

One of the major revolutions was the use of multiple, independent receiver channels. The basic concept occurred relatively early in the development of MRI[21], [22], and was quickly recognized as a power technique. It has allowed higher SNR, higher speed, and higher resolution imaging, and in many ways shaped the design of the RF system, coil design, and pulse sequence design. The use of parallel receivers has become nearly ubiquitous, with commercial systems being widely available. The transmit system has not, however, seen this type of revolution. The development of the birdcage coil, with a nearly uniform B_1 field at 1.5T, and acceptable results even at 3T, has made one and two channel transmit systems sufficient for most uses. The push to ever higher main magnet field strengths, from 1.5T to 3T and now on to 7T, and the desire for ever faster imaging has brought interest to what was once esoteric. Parallel techniques for transmit are being developed that allow uniform excitations at ever higher fields, accelerated imaging from reduced excitation windows, and correction schemes for difficult artifacts. Parallel receive has paved the way for parallel transmit, with much of the mathematical and theoretical framework translating directly between the two techniques. Unfortunately, the implementation of parallel transmit hardware does not benefit as directly. The RF transmit hardware architecture has needed to be developed nearly from the ground up in order to facilitate parallel excitation techniques.

Part of that development has been new methods of ensuring independent operation of the array coil elements. Coil structures[23], networks[24], active feedback[25], [26], and amplifier architectures[27], [28] have all been explored as methods of isolating the arrays. This work has specifically focused on transmit amplifiers that provide isolation to the coils they are connected to. Much of the work focused on testing current source amplifiers and low output impedance amplifiers in order to obtain quantitative comparisons between the architectures. Comparisons were made on the mechanism of isolation, the amount of isolation obtainable, and the peak power level obtainable from the different architectures.

1.1 Parallel MRI

Multiple independent RF coils were conceived of early in the development of MRI. Using a set of smaller surface coils can increase SNR compared to using a single, large surface coil. Array receivers can also increase the imaging time by reducing the number of unique phase encode steps needed in a sequence. This two uses are not a binary choice, but can be used together. Parallel receivers can also be combined with techniques like Echo Planer Imaging (EPI)[29] and spiral k-space trajectories[30]. Realizing these benefits required the development of extensive mathematical frameworks that make designing the pulse sequences possible. Two landmark developments were the Simultaneous Acquisition of Spatial Harmonics (SMASH)[17] and SENSitivity Encoding (SENSE)[16] techniques. These techniques have made possible the design and use of accelerated receive sequences, and so opened the door for widespread adoption.

Parallel transmit MRI has followed a similar, but somewhat divergent development path. Uniform transmit patterns can be readily obtained using birdcage coils at 1.5T and below. Even at 3T the error is typically acceptable, even with whole-body systems. Additionally, transmit has not historically been the time limiting factor, so there has historically little drive to develop parallel transmit. The development of 7T whole body systems and increasingly sensitive imaging techniques has changed this and given new motivation to investigating parallel transmit. Uniform transmit fields are no longer achievable with single coils at 7T, and full-wave effects must be contended with[31], [32]. Additionally, susceptibility artifacts render some techniques impractical or impossible to use in all the desired ways. Finally, faster imaging can be obtained by reducing the Field-of-View (FOV) of an image and retaining the same spatial resolution. All of these things can be corrected or made practical with parallel transmit. The frameworks for parallel receive systems have been extended and modified for parallel transmit hardware. What is lacking is widely available multi-channel transmit systems.

1.2 Array Coil Coupling

Parallel MRI has largely been predicated on the assumption of independent channels. This means not only that the receiver/transmitter hardware is controllable on a per channel basis, but also that the coil arrays should be independent[33], [34]. Independent array elements mean that power is not transferred between them, which would seem to be a given a first glance, but is actually a complicated condition to enforce.

Independence is accomplished commonly achieved with a combination of geometric (inductive) decoupling and the use of low input preamplifiers. The amplifiers and coil matching network combine to prevent induced currents, and the geometric decoupling results in zero net flux through overlapped elements. These highly effective techniques have become the mainstays of receive coil design. While the geometric, inductive, and capacitive decoupling techniques translate directly to transmit arrays, the low input preamplifiers do not. Receive coils do not need any currents to flow on them, as the preamplifiers are sensitive to the induced voltage. Transmit arrays are different in that they *must* produce magnetic fields of substantial strength, which requires large currents. So, any decoupling technique for transmit arrays must prevent undesired currents from being induced by other channels, but must create or allow the desired currents.

1.3 Dissertation Organization

This dissertation describes the implementation and testing of an eight channel RF transmit system for MRI, incorporating a vector modulation system and isolating power amplifiers. A comparison has been made between different isolating amplifier architectures, and parallel transmit imaging has been performed. Following this introduction is a chapter of background to establish a framework to understand parallel transmit and isolating amplifiers. An overview of MRI is presented, with a look at the basic imaging sequence and structure of the acquired data. This is followed by background on parallel MRI and a theory of coupled arrays. A brief discussion of the different power amplifier architectures is included, as well as information regarding modulation systems. Chapter 3 describes the vector modulators and their operation. An architectural overview is presented, along with a development of the circuits used. Additional testing and performance data is included to demonstrate the capabilities of the vector modulation system. This is followed by a treatment of the isolating power amplifiers. The current source and low output impedance amplifier architectures are described with information regarding their design method of functionality. Testing information is included, and comparisons are shown for their ability to isolate arrays as well as deliver power to the coil. The fifth chapter concerns the parallel transmit system as a whole. This covers the overall architecture of the system, including interconnection and interaction between the different subsystems. Examples and uses are shown from three different MR systems and different field strengths, as well as both B_1 shimming and fast modulation techniques. Finally, chapter 6 concludes the main body with a review of the prior material, some conclusions that can be drawn from the testing and work done, as well as considerations of possible future work.

CHAPTER 2
BACKGROUND

2.1 Magnetic Resonance Imaging

The physical phenomenon of Nuclear Magnetic Resonance (NMR) was first described by Bloch and Purcell in 1946[1], [2]. This found its first application in the NMR spectroscopy, where compounds are analyzed based on their resonant frequencies. This was modified into the tomographic imaging technique known as Magnetic Resonance Imaging (MRI) by Lauterbur in 1973[3]. He was able to localize where signals were generated in space by breaking with known good NMR practice and introducing a linear magnetic field gradient. The Larmor relationship that is fundamental to NMR made this possible, as it relates the resonant frequency of a material to the magnetic field by:

$$\omega = \gamma B_0 \tag{2.1}$$

Where ω is the resonant frequency in rad/sec, γ is the gyromagnetic ratio of the nuclei in question measured in rad/T, and B_0 is the applied magnetic field in Tesla. The linear variation in B_0 that Lauterbur used made it possible to localize signals in one spatial dimension. Repeatedly rotating the direction of that gradient relative to the sample and gathering data makes a back projection reconstruction possible, producing an image. The development of Fourier encoding was a landmark development for MRI[35], and is the basis for most modern MRI techniques.

2.1.1 Basic Imaging Sequences and Gradient Encoding

The imaging sequence, or waveforms and timing of the system used to collect MR information, controls most of the aspects of an MR image. Two foundational sequences are the Spin Echo (SE) and the Gradient Recalled Echo (GRE). Many of the imaging techniques used can be seen as modifications of these two sequences. The sequences having timing, strength, and patterns for the RF transmit pulses, three orthogonal gradients, and RF receive. The RF transmit pulses are delivered at the resonate frequency of the nuclei (or spins), typically ^{1}H corresponding to the hydrogen in water, and will tip the spins into the transverse plane. The nuclei are normally aligned with the main magnetic field (typically z-directed), and the RF pulse will excite them so that they process in the XY plane. The magnetic field gradients generate time varying, z-directed magnetic fields that have a spatial dependency in one direction. The gradients are orthogonal from each other, so we can write them as:

$$G_x = \frac{\delta B_z}{\delta z}, \quad G_y = \frac{\delta B_z}{\delta y}, \quad G_z = \frac{\delta B_z}{\delta z} \tag{2.2}$$

We often discuss the Slice Select Gradient (G_{SS}), Phase Encode Gradient (G_{PE}), and the Frequency Encode Gradient (G_{RO}), which are the logical gradient channel that map to the spatial gradient channels. These logical gradients can be thought of as an arbitrary rotation of the spatial gradients (or vice versa). Finally,

the RF receive indicates the time during which RF data is gathered by the system. Normally, this occurs during the echo, or the time during which the spins in the sample are rephasing. A basic Spin Echo sequence, based on the spin echo technique first described by Hahn[36], is shown in Figure 2.1. This shows a single repetition, and would repeated a number of times equal to the number of data points in the phase encoded direction. The number of points in the second dimension is set by the number of samples recorded during the echo.

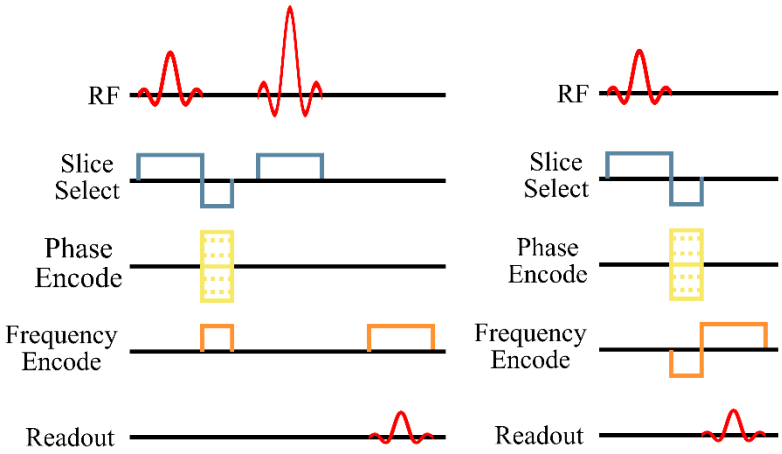


Figure 2.1: The basic Spin Echo and Gradient Echo pulse sequences.

The RF excitation pulses of a typical sequence are on the order of a few milliseconds. While this amount of time cannot be ignored in terms of dephasing of the spins, it is not sufficient to create substantial degradation of the image quality. Each repetition will be substantially longer, in some cases multiple seconds. This is because the spins must be allowed to relax back fully or there will be a cumulative signal loss.

2.1.2 k-Space

The data used to form an MR image is not gathered in a manner that can be directly displayed. It is, instead, gathered in the what is known as *k*-space[37], [38], which is a Fourier domain. The image must then be reconstructed using a 2D inverse Fourier transform, or equivalent. The data is gathered so that one direction corresponds to Frequency Encode, and the other is Phase Encode. This can be expanded to a 3D case, but we will not do so at this point as the fundamentals do not change but the notation and representation become more complex. The basic structure and notation of *k*-space is shown in Figure 2.2

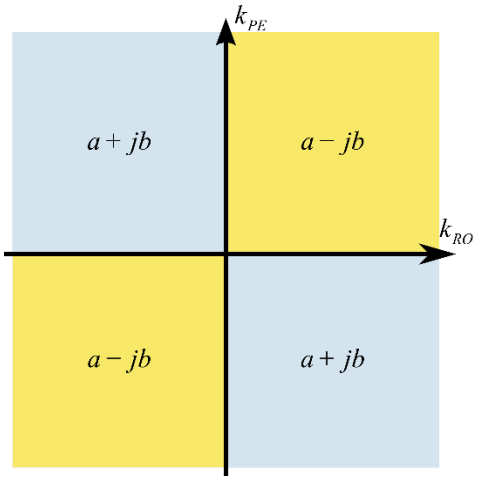


Figure 2.2: The primary directions in *k*-space are notated a k_{PE} and k_{RO}. *k*-space follows a conjugate symmetric pattern.

The gradients and RF transmit pulses can be thought of the observer through *k*-space. The time integral of the gradient determines the distance and direction which the observer moves through the space. This *k*-space trajectory is important for how data is gathered, as the observation point moves across lines of *k*-space in a raster scan fashion. So we can define the spatial frequency (or location in *k*-space) as the point (k_{RO}, k_{PE}) which are given by:

$$\begin{aligned} k_{RO} &= \gamma G_{RO} m \Delta t \\ k_{PE} &= \gamma n \int G_{PE}\, dt \end{aligned} \tag{2.3}$$

The point number is given by (m, n) and Δt is the dwell time of the sampling. So the spatial position and spatial frequency must be related by a Fourier transform. While we are assuming a simple pulse sequence for this formulation, other k-space trajectories (e.g. spirals) have been used for various reasons. Also, this has been defined in terms of the receive space, but is equally applicable to the excitation.[39]

2.2 Multi-Channel MRI

The initial MRI systems inherited many things from their NMR predecessors. One of those was the use of a single RF transmit channel, and a single RF receive channel, similar to what is shown in Figure 2.3 [12]. This configuration has proved to be very robust for the small samples of NMR, but the transition to MRI quickly made its limitations obvious. A steady progression to multi-channel MRI systems has occurred since the first experiments by Lauterbur [3].

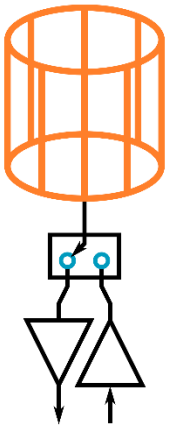


Figure 2.3: The single channel transmit/receive system. It has proven robust for small regions of interest.

Multi-channel RF systems were of interest even from early in the development of MRI. Their advantages became obvious quickly, allowing for improved SNR and faster imaging times[13], [15], [21], [22]. The focus at this point was on multi-channel receivers only, with the transmit system remaining single channel. The initial development was to have a relatively limited number of coils, in part due to the need to have the coils operate independently. Two or three surface coils can easily be geometrically decoupled, but beyond that a different technique is needed. Low input impedance preamplifiers were ultimately the enabling technology for large receive arrays.

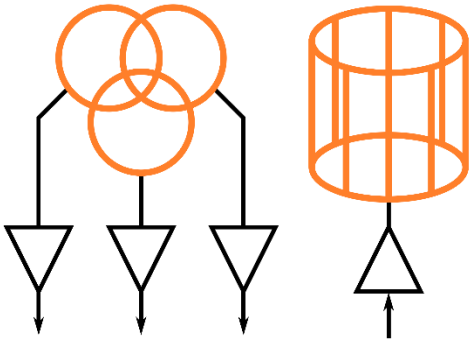


Figure 2.4: Multi-channel receiver with single channel transmit.

The low input impedance preamplifier is designed specifically to prevent coupling between array elements for MRI. They are used to create a high impedance node on the coils, thereby minimizing induced currents. The amplifiers are sensitive to voltage, so they are still able to pick up the NMR signal that is induced in them. This technique has proved to be so effective and beneficial that multi-channel receive systems have become commonplace in clinical settings. Systems with 96 receive channels or more are readily available,

and can be put to good use. But still, the transmit system has remained single channel (or more recently dual channel). Interest in multi-channel transmit systems has begun to grow recently.

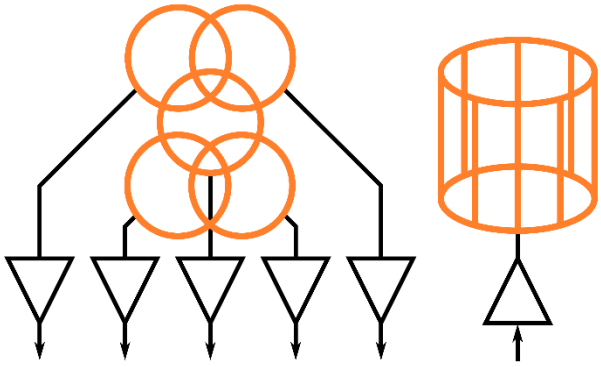


Figure 2.5: Highly parallel receiver with single channel transmit.

2.2.1 Multi-Channel Transmit

Interest in multi-channel transmit systems is being driven by two primary trends. The first is the increase in main magnet field strength. The imaging field has increased in strength from fractions of a Tesla to 1T, 1.5T, 3T, and now 7T for whole body MRI systems. The corresponding increased operating frequency and decreased wavelength has introduced substantial problems obtaining a uniform excitation by introducing full-wave effects. [31], [32], [40], [41] At the same time, interest has increased in using 2D and 3D excitation pulses. These pulses elongate the transmit time the point that it can adversely impact the SNR of the final image. Multi-channel transmit systems offer ways to correct the non-uniformities seen at high field strength, and accelerate multi-dimensional RF pulses. This is very much analogous to what multi-channel systems achieved for receivers.

The development of multi-channel transmitters and receivers share a similarity beyond just their basic application. They both require an enabling technology to allow large scale arrays to be practical. Receive arrays found that technology in low input impedance preamplifiers, which limited problems related to array coupling. Transmit arrays must still overcome this hurdle. To understand why this is necessary, the details of preventing it, we must examine the coupling phenomenon itself.

2.2.2 Coupling in Arrays

When a single coil is used a very simple model and accurately represent the behavior (Figure 2.6). The coil itself is characterized by a small resistance and some inductance. These result directly from the structure of the coil, and are intrinsic to a given design. It is supplied by a voltage generated with an internal resistance (for now we can consider this to be 50Ω). In the receive case this generator would be replaced with a passive load. A matching network sits between these two parts to ensure maximum power transfer between them.

There is some terminal voltage across the inputs to the coil, V_1, that will generate a current on the coil of I_1. This current is what actually generates the B_1^+ field that we need from a transmit coil, and in the same way an EMF is induced in a receive coil by the B_1^- field.

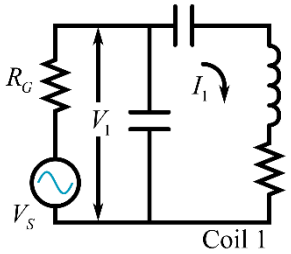


Figure 2.6: Network representation of a single coil. It is characterized by some resistance and inductance, and matched with a basic capacitive L network. The transmitter will produce some voltage at the matching network terminals, I_1, and has some internal impedance R_G.

Introducing a second coil complicates this model as the field from one is likely to interact with the other. One model for this interaction is that the coils act like a loosely coupled transformer. This model is shown in Figure 2.7 where the coupling constant M is a generalized coupling constant that can be complex.

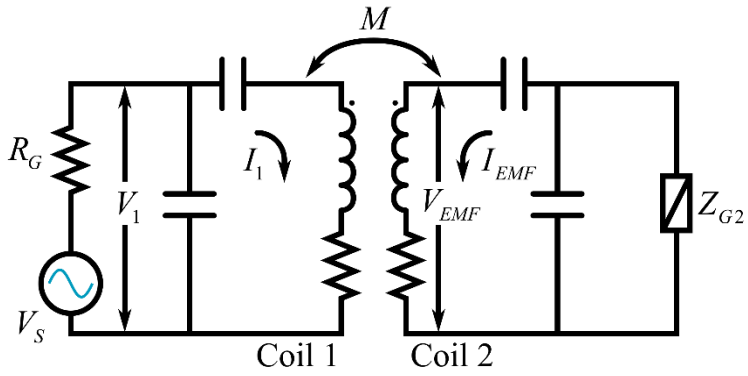


Figure 2.7: Network representation of coupled coils. The generalized coupling constant M indicates the flux coupling between elements, with I_1 inducing an EMF on coil 2, V_{EMF}. This EMF will result in an induced current, I_{EMF}, that depends on both the EMF and the load impedance Z_{G2}. The load of coil 2 is shown to be passive here, but the same basic principles are followed for an active load (i.e. and amplifier).

What we see is that the current, I_1 will induce an EMF on coil two. This EMF presents as a voltage that will induce some current, though the magnitude of the current will also be dependent on the load impedance and the design of the matching network. The isolating preamplifiers modify the matching network and load impedance create a high impedance node across the coil structure terminals.

2.3 Power Amplifiers

The design goals for the matching network is the other major factor in amplifier performance, aside from the class of operation. These overarching design goals, or what we are optimizing for, are what we call the amplifier "architecture". We will focus on three different architectures that can be viewed as having slightly different design goals: 1) the standard power amplifier, optimized only for peak power, 2) the current source amplifier, optimized only for isolation, And 3) the low output impedance amplifier, which attempts to optimize for both power and isolation.

2.3.1 Standard Power Amplifiers

Standard power amplifiers are the most commonly used power amplifier design. Their goal is to deliver maximum power to a well-defined load (e.g. the transmit coil for NMR/MRI). The matching networks accomplish this by transforming the load impedance, typically 50Ω, into the impedance that is optimal for power output for the amplifier, as shown in Figure 2.8(a).[42], [43] This type of amplifier is seen in single and dual channel systems, and is fundamentally the same as the amplifiers used in many communications and RADAR systems. It is worth remembering that power is conserved by the matching network while impedance, and consequently voltages and currents, are transformed. The result is that the maximum possible current on the coil is obtained for a given input power. Finally, in a practical situation there will be some mismatch at the coil that results in reflected power. Isolators are typically used to absorb this reflected power and prevent damage or performance variation of the amplifiers.

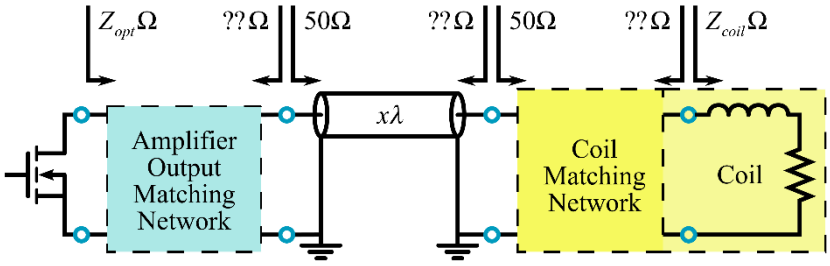


Figure 2.8: The matching network for a standard power amplifier. It is characterized by presenting the optimal load to the active device. The coil will see some impedance, but it is not well controlled.

2.3.2 Current Source Amplifiers

The current source amplifier, in contrast to the stand power amp, is designed to present a high impedance to any induced EMF at the expense of not being power matched.[44], [45] In essence, a single element matching network is used to remove any reactance due to parasitic output capacitance, leaving only the resistance of the MOSFET drain. The resistance very high (on the order of kilo-ohms). The coil is series resonated and connected directly to the amplifier so that there are no other current paths except through the amplifier output. Effectively, the amplifier has a low impedance load, and the coil has a high impedance load (shown

in Figure 2.9(a)). The result is that coupling to the coil produces an EMF but the induced current is minimized, reducing the effective coupling. The downside is that the matching networks used do not result in power match for the amplifier, reducing the maximum current on the coil to the rating of the active device in the amplifier.

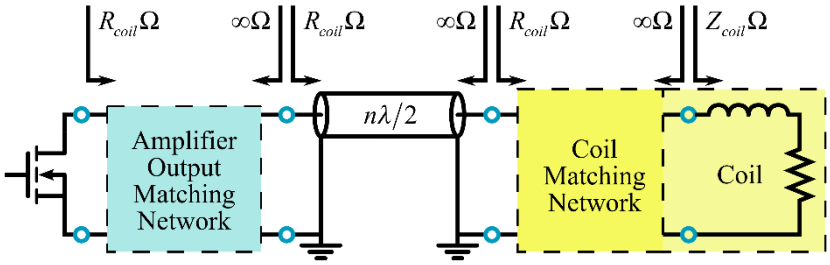


Figure 2.9: The matching network for a current source amplifier. It is characterized by presenting a high impedance to the coil. The active device does not see an optimal match, so the output is limited to the current rating of the device.

2.3.3 Low Output Impedance Amplifiers

The low output impedance amplifier[28] design attempts to obtain both a high output power and isolation. This is achieved in a manner analogous to the low input impedance pre-amplifier, where the amplifier matching network optimizes performance and presents a low impedance to the coil.[13] The design is such that the MOSFET sees an optimal load for power, and the coil port sees a low impedance, shown in Figure 2.10(a). The coil's matching network is designed to form a tuned tank across the coil element, preventing induced currents. The design of the coil matching network is identical to those used with low input impedance preamplifiers, and has previously well described.[46] This allows the amplifier to obtain the same peak power output as the standard power amplifier and simultaneously decouple the array coil.

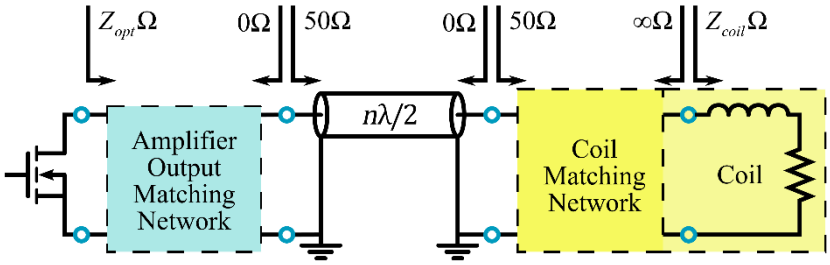


Figure 2.10: The matching network for a low output impedance power amplifier. It is characterized by presenting the optimal load to the active device and a low impedance to the coil.

2.3.4 Feedback Based Decoupling

We have previously mentioned feedback systems in the context of linearizing amplifiers. They can also have applications in correcting coupling between array elements. This is accomplished by measuring the current on each element, comparing it against the desired waveform, and correcting the input, as in Figure 2.11. While this works, it requires a very high bandwidth feedback system.[47] Combined with resonant systems it tends to lead to instability. An iterative approach can reduce some of the problems associate with this, but may still drive the output of the amplifiers to a minimum in some cases. Finally, it should be noted that feedback systems can be implemented with any architecture and class of amplifiers, so should not be interpreted as mutually exclusive to the above isolating amplifiers.

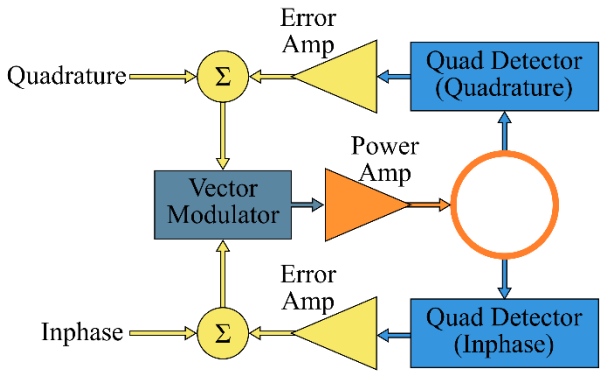


Figure 2.11: The block diagram of a polar feedback system. It samples the output of the amplifier and converts it into baseband I and Q terms. These are amplified and summed with the input I and Q terms to remove any error. If the sampling is done on the coil, then coupling will also be removed.

2.4 RF Modulators

Modulation is, in simple terms, applying a time varying envelope to a constant RF signal. This envelope may be in amplitude, phase, or both. The most basic method of modulating involves using a mixer to combine two signals. Mixers essentially apply a time-domain multiplication between the two signals. In the frequency domain this appears as sums and differences of the two frequencies and all of their harmonics. This multiplying effect is obtained with a non-linear device, often a diode or similar solid state junction. Better performance is obtained with a more refined system than a simple diode mixer. We can break these into three techniques: Multi-stage mixing, direct modulation/single stage mixing, and Direct Digital Synthesizers.

2.4.1 Multi-Stage Modulation

A multi-stage, or heterodyne modulation system, uses multiple mixing stages to achieve the final output RF. This has the advantage of only requiring relatively low frequencies to be synthesized, and at no point is the center frequency directly generated. This is good because every mixer will allow some amount of the Local

Oscillator (LO) the feedthrough to the output. It also allows the Intermediate Frequencies (IFs) to be selected based on minimizing interference and filtering capabilities.

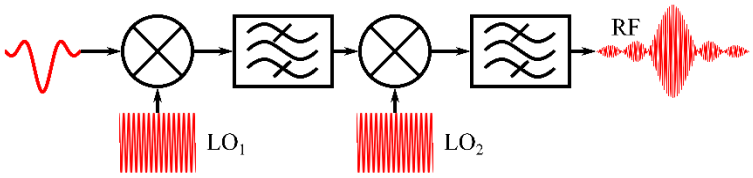


Figure 2.12: A heterodyne modulation system. Multiple mixing stages are used to bring the modulated waveform up to the desired output frequency.

2.4.2 Direct Modulation

2.4.2.1 Cartesian Modulation

The direct modulation scheme is conceptually simple and elegant. It uses a single RF frequency synthesizer, with no IF stages that must be phase locked/controlled. One approach to this is a Cartesian modulation scheme where the amplitude and phase are directly controlled, as shown in Figure 2.13. The amplitude would be controlled by either a variable attenuator or a Variable Gain Amplifier (VGA). Phase would be modulated using a variable phase shifter. While there is a conceptual elegance to this system, it is rarely implemented. High quality, linear, controllable phase shifters that work well in the 10's to 100's of MHz are difficult to build, expensive and hard to find.

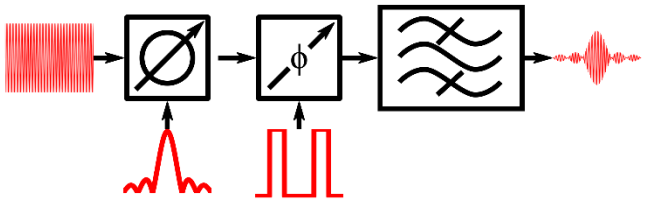


Figure 2.13: The basic Cartesian direct modulation system.

2.4.2.2 Vector Modulation

Vector modulation is based on a linear combination of a sine and cosine wave that allows for homodyne modulation. The two waves are modulated in amplitude, but not applied phase. The modulated sine and cosine waves are summed to produce a single phase and amplitude modulated output. To see how this works we can consider two waves defined by $A\sin\omega t$ and $B\cos\omega t$ then we can show that $A\sin\omega t + B\cos\omega t = C\cos\omega t + \varphi$ That is to say, a sinusoid of arbitrary phase and magnitude can be constructed by summing a sine and cosine wave of different magnitudes, directly phase shifting the wave is not necessary. We will start by looking at $C\cos\omega t$ to see how this works:

$$\begin{aligned} C\cos\omega t-\phi &= C\left(\cos\omega t\cos\phi+\sin\omega t\sin\phi\right) \\ &= C\cos\omega t\cos\phi+C\sin\omega t\sin\phi \\ &= \left(C\cos\phi\right)\cos\omega t+\left(C\sin\phi\right)\sin\omega t \end{aligned} \tag{2.4}$$

From this we compare $B\cos(x)+A\sin(x)$ with the right hand side of the above equation and we can see that

$$A = C\cos\phi \tag{2.5}$$

$$B = C\sin\phi \tag{2.6}$$

From this we are able to find the magnitude (C) and phase shift (φ) of the final waveform as follows:

$$\begin{aligned} A^2+B^2 &= C^2\cos\omega t^2+C^2\sin\omega t^2 \\ &= C^2\left(\cos\omega t^2+\sin\omega t^2\right) \\ &= C^2 \end{aligned} \tag{2.7}$$

because $\cos\omega t^2+\sin\omega t^2=1$. So we finally have that the magnitude C is found by:

$$C = \sqrt{A^2+B^2} \tag{2.8}$$

The phase shift φ can be found by dividing equation (2.5) by equation (2.6) so we have:

$$\frac{C\sin\phi}{C\cos\phi}=\frac{B}{A}\Rightarrow\tan\phi=\frac{B}{A}\Rightarrow\phi=\tan^{-1}\frac{B}{A} \tag{2.9}$$

There are two mixers, who take in IF signals that corresponding I and Q (or in the notation above A and B). LO is passed through a 90° hybrid to produce the sine and cosine feeds for the two mixer's LO ports. The RF out of the mixer is passed through a summer, or power combiner. This is basic architecture is shown in Figure 2.14. The output can be modulated in both phase and amplitude using Equations (2.8) and (2.9) to calculate values for I and Q. An important point is that I and Q can both be baseband signals (sub 100kHz for MRI). That is, neither signal must contain phase information in and of itself. It is possible to set them to be DC values and a static phase and amplitude shift would be applied to the LO signal. While this simplified implementation can be made to work, it is far from ideal. A number of refinements would be made for a real world implementation. Examples might be improved mixer architectures (e.g. doubly balanced mixers, AGC to normalize the input LO levels, or a buffer amplifier to drive output). This is in addition to things like matching networks and the complexities inherent in implementing each of these blocks. While it is possible to build a vector modulator from components, it is not a simple task.

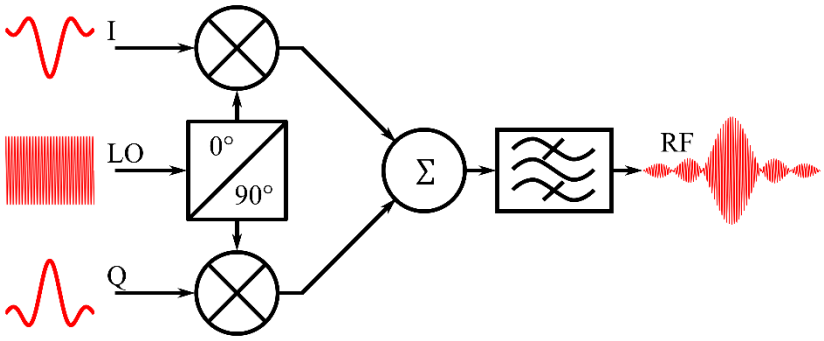


Figure 2.14: A simple vector modulator implementation.

2.4.3 Direct Digital Synthesis

The Direct Digital Synthesizer, or DDS, has only begun to see significant use at high frequencies relatively recently.

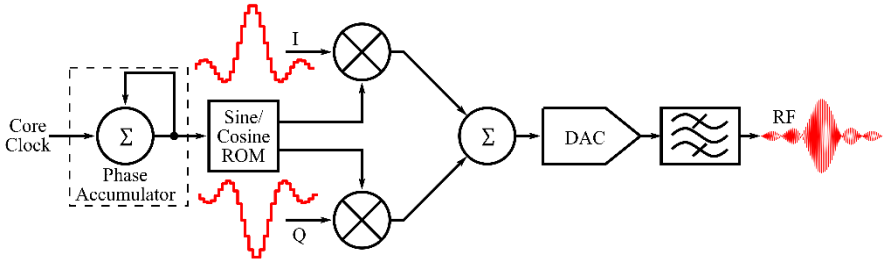


Figure 2.15: The basic DDS system generates a sine wave in the digital domain. A cosine wave can easily be generated at the same time, and these can then be modulated in much the same way as a vector modulator works. Finally, the fully modulated signal is converted to analog by a high speed converter.

Recently, DDS based modulation systems have been constructed. These systems produce fully modulated RF using a point-skipping Numerically Controlled Oscillator (NCO) in conjunction with lower frequency Digital-to-Analog Converters (DACs). Highly integrated DDS chips have become commercially available reducing the cost and size of modulation systems, but this architecture introduces additional complexities in the design of add-on multi-channel systems. Each modulator directly generates its own RF, so the center frequency must set to match the receivers or a phase ramp will be introduced. Obtaining this information from the MRI system requires tightly coupled subsystems, which complicates the design of the transmitter.

CHAPTER 3
MULTI-CHANNEL MODULATORS

The basic operation and theory of vector modulation has been discussed in Section 2.4.2.2. A multi-channel vector modulator system was created for the parallel transmit system to provide an easy to integrate, scalable solution to adding transmit channels to an existing MRI scanner.

3.1 Architectural Overview

The vector modulators system can be divided into two main sections: The digital and low-frequency analog on the Frontend Board, and the RF Board. The Frontend Board provides the connection to the controller, power connection, and input signal conditioning. A single PCB is allocated to this, with female header receptacles to connect to the RF Board. The RF portion of the vector modulators has a main board that implements the core functionality (modulators, step attenuators, RF switches, etc.) and a set of pluggable modules with filters and preamplifiers. The board also has all of the RF connections for the LO and modulated RF signals. A high level block diagram showing he major functional parts of the modulators is shown in Figure 3.1

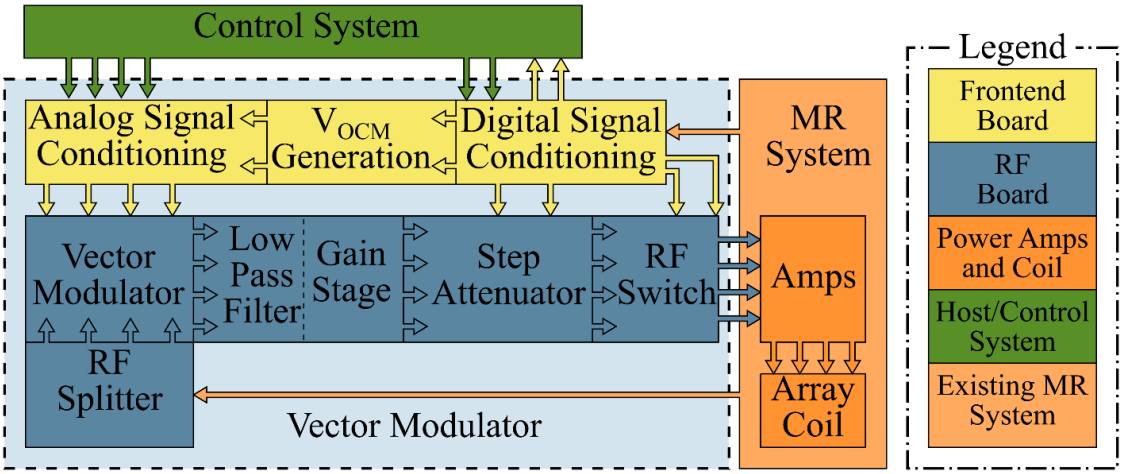


Figure 3.1: Block diagram of the modulators and connections. The Front End Board and RF board physically separate the high and low frequency signals. Input connections (with the exception of LO) are passed through the Front End Board. RF outputs and the LO connection are made directly on the RF Board.

3.1.1 Frontend Board

The frontend is contained on a single two layer PCB shown in Figure 3.2. It handles signal conditioning and interfaces to the control system and, power supplies, and other parts of the system, as shown in Figure 3.3.

The circuit was designed to interface to a control system based around the National Instruments PXI-7853R card. The main interface connector uses the pinouts for the PXI-7853R connector, and the analog and digital signal condition assumes the voltages and drive levels that these cards produce. The board has three major functional blocks: 1) the digital signal conditioning; 2) analog signal conditioning; 3) V_{OCM} generation. In addition there are a number of connectors for interfacing to ports on the RMIO connector that are not directly used by the modulators.

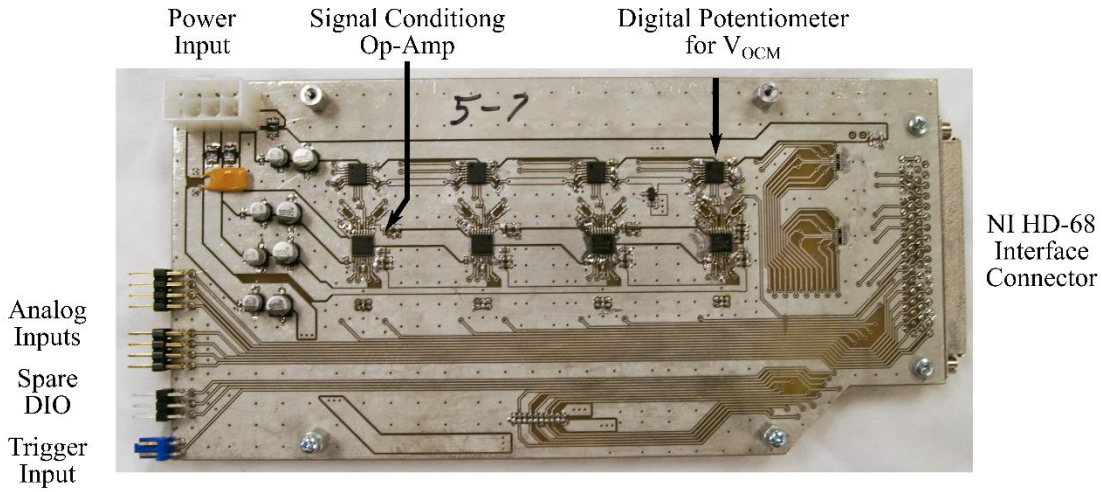


Figure 3.2: The frontend board for modulators. This board has been designed for use with the NI PXI-7853R boards, so the main interface connector on the right edge is an HD-68 connector. Power input is top left through a Mini Fit Jr. connector, and additional connections are on the left edge.

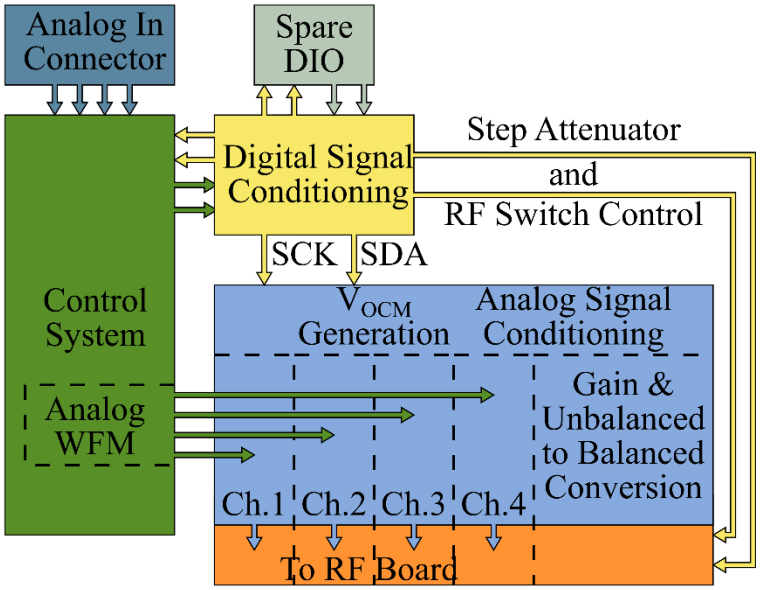


Figure 3.3: Block Diagram of the frontend. This circuitry handles the interface and signal conditioning can be divided into three major functional blocks.

3.1.1.1 Digital Signal Conditioning

The primary purpose of the interface board is to connect to and condition the output from the controller (a National Instruments PXI-7853R in this case). There is a basic level of conditioning/protection for the digital lines to prevent over voltage and damage from Electro Static Discharge(ESD). A set of shunt, reverse biased Zener diodes are used to clamp the lines voltages at 3.3V. There are also shunt capacitors, series resistors, and pull down resistors on most lines to mitigate transient spike. The exception is that the lines used to implement an I^2C interface do not have the diodes or pull down resistors since they must be pulled up to 3.3V to function properly A single channel of the protection circuit is shown in Figure 3.4.The capacitor shown is a shunt capacitance to ground that is part of an array.

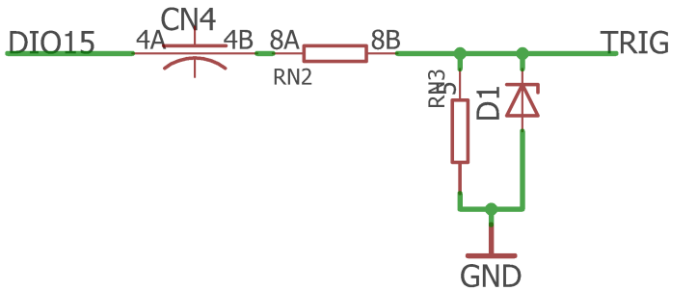


Figure 3.4: The over-voltage/ESD protection circuit. The design uses an RC network with diode to reduce the likelihood of damage to the system.

3.1.1.2 Analog Signal Conditioning

A ±10V single ended signal is generated by the PXI-7853R, but the vector modulator IC input range is 0-1V differential signal with 0.5V common mode, as shown in Figure 3.5. The primary analog signal condition is based around a fully differential op-amp (Texas Instruments THS4522) that includes a common mode offset voltage (V_{OCM}) control. A single channel, as implemented, is shown in Figure 3.6 with a more conceptual schematic provided in Figure 3.7. A digitally controlled potentiometer circuit is used to generate V_{OCM} so that any error can be calibrated out in hardware by the control system. A simple resistive divider to achieve the desired gain for the op-amps, but the resistors R_F and R_G are 1% tolerance to minimize the need to manual gain adjustment. R_T is a drain resistor that prevents any DC offset at the input of the op-amp, but the design assumes that no significant DC bias will be on present.

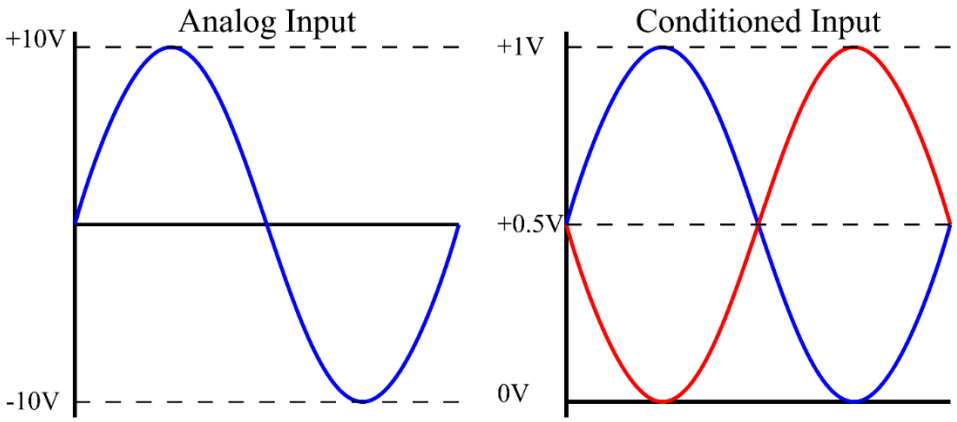


Figure 3.5: Simple example of the expected analog waveform input and conditioning.

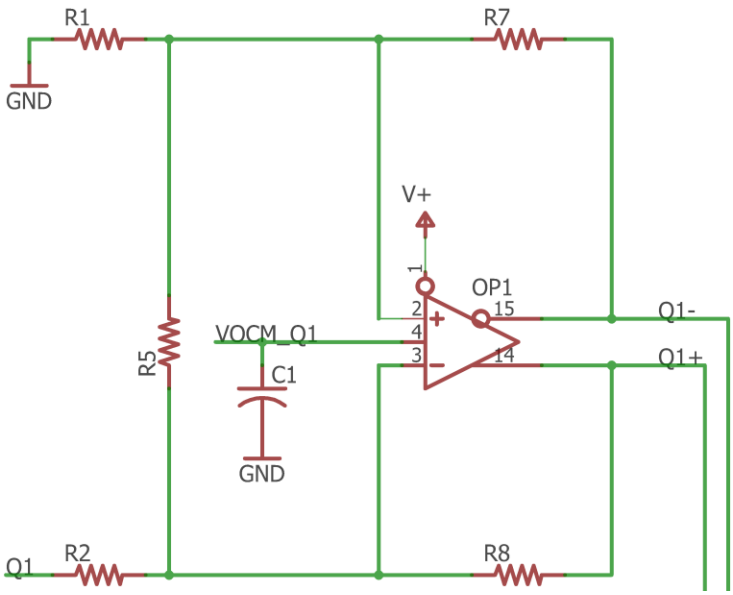


Figure 3.6: The op-amp circuit used to condition one of the analog inputs.

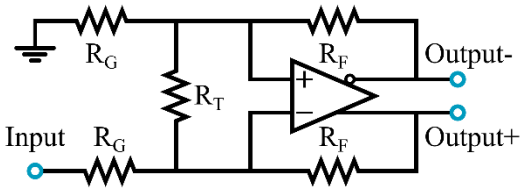


Figure 3.7: A fully differential op-amp circuit to convert a single ended feed to differential.

3.1.1.3 V_{OCM} Generation

The vector modulator IC requires differential inputs with a common mode voltage, called V_{OCM}, for the baseband I and Q inputs. A nominal offset of 0.5V is needed, with an absolute max of 0.6V and min of 0.4V. This is generated in two stages: a high stability reference voltage of 1.25V is created, then a voltage divider made up of two fixed resistors and a digital potentiometer. The potentiometer is used to trim the offset voltage, while the fixed resistors ensure that the voltage never exceeds the limits of the vector modulator. A single voltage reference is located on each board, but there is a separate voltage divider for each of the I and Q signals.

The 1.25V reference is generated using a TI REF2912 series voltage reference. It is a simple bandgap reference that only needs a capacitor to stabilize (shown in Figure 3.8), and is accurate to 100ppm/degree C. This provides a good, stable starting point for generating V_{OCM} without require the precise adjustment of a voltage regulator. This voltage is the input to the voltage divider, which is based around the Microchip MCP4651 digital potentiometer is shown in Figure 3.9). These are two channel devices with an

I²C interface, so one chip is used for each modulator channel. The device is a 10kΩ pot with 8 bit resolution, yielding a voltage resolution of approximately 78μV.

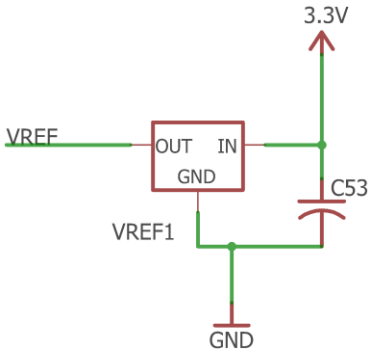


Figure 3.8: The TI REF2912 requires only a stabilizing capacitor to function.

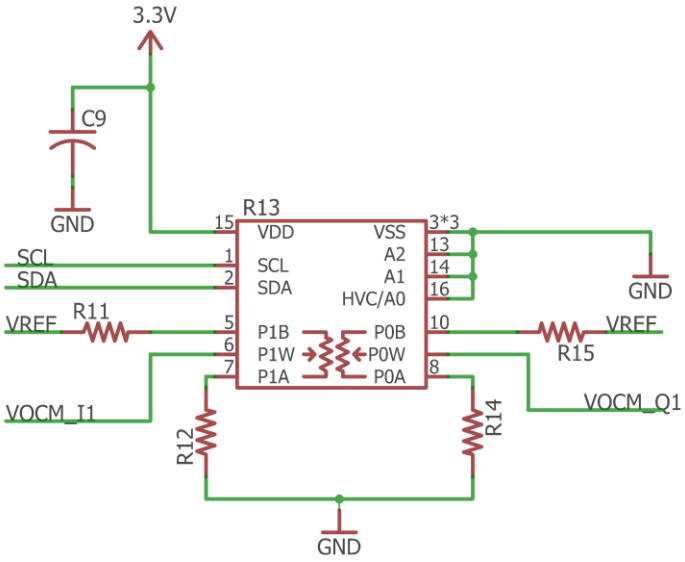


Figure 3.9: The digital potentiometer circuit allows adjustment of V_{OCM} for I and Q separately for each channel. The resistor values were selected so that the max and min values are 0.6V and 0.4V respectively.

3.1.2 RF Circuitry

The RF board uses the output of the frontend board and a Local Oscillator (LO) signal to generate the fully modulated output. A number of condition steps are added in addition to the modulation stage in order to reduce noise and spurious signals, increase the usable dynamic range, and achieve a signal level suitable for transmission to the next sub system. This is shown in block diagram form in Figure 3.10, with a photograph of a physical example in Figure 3.11. The high level operation is that the LO input split to feed all four channels on the board. The vector modulator itself is at the start of each channel. It is followed by a passive

low pass filter to remove mixing products and a preamplifier to bring the signal up to a slightly higher power. A digital step attenuator does bulk scaling of the output to ensure that the dynamic range of the system is well utilized, and finally a digitally controlled RF switch is used to minimize any feedthrough when the modulator should not be producing output.

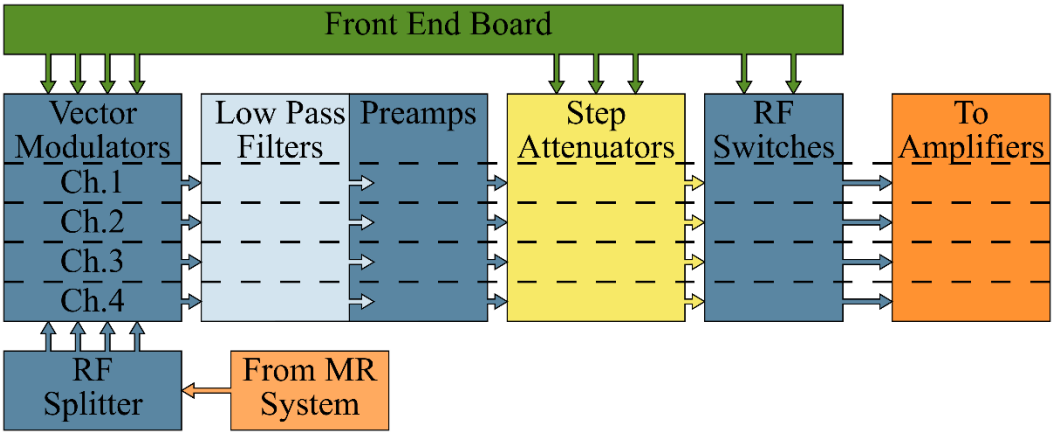


Figure 3.10: The RF board can be divided into the functional sections shown.

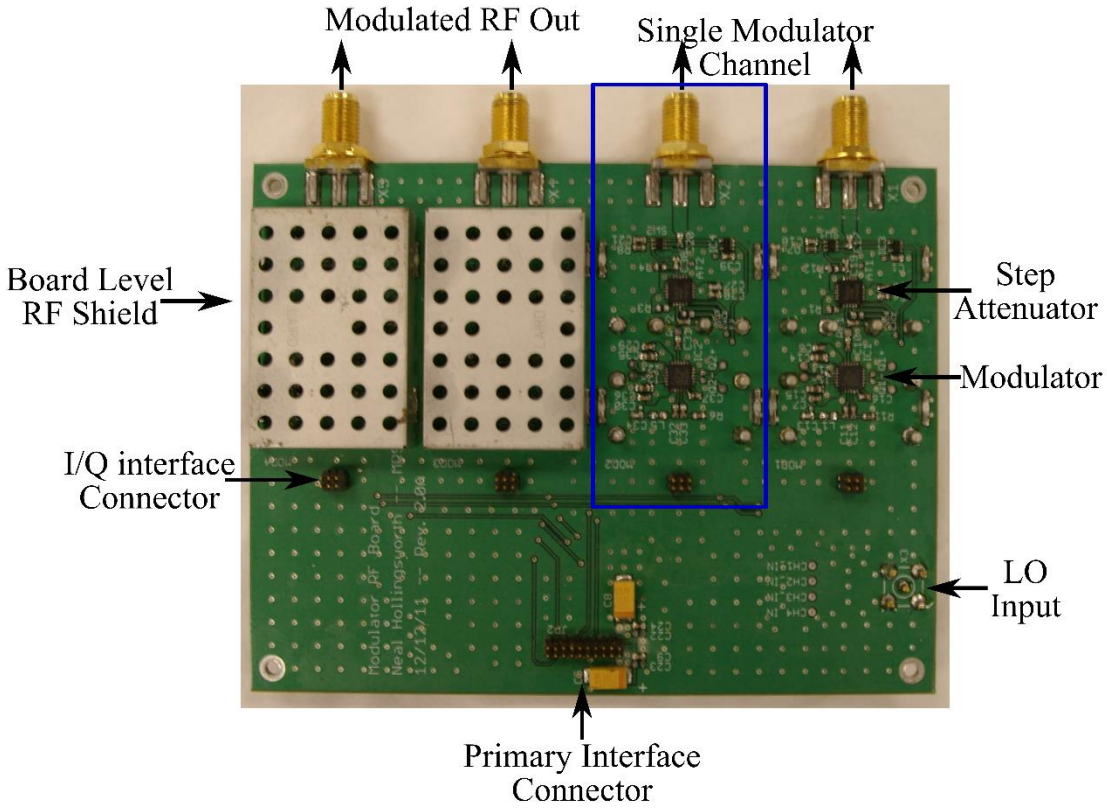


Figure 3.11: PCB containing the RF section of the modulator.

3.1.2.1 Vector Modulator

The modulator is based around the Linear Technologies LT5598 vector modulator IC which integrates a broadband power splitter/phase shifter, doubly balanced mixers, power combiner and some RF amplification into a single chip. The primary inputs are the LO inputs (LOP and LOM) and the I and Q inputs (BBPI, BBMI, BBPQ, and BBMQ). Some matching has been used on the LO port to improve the return loss in the frequency ranges this system is expected to be used (from around 50MHz to around 300MHz). The I and Q inputs are low frequency and present few problems, however they do have a non-positive input impedance that must be taken into account if a sensitive system is used to supply the waveforms. The op-amp used for signal condition serves to buffer the rest of the system from this impedance.

The I and Q inputs are baseband inputs, so a signal from DC up to hundreds of MHz could be used to modulate LO. For our purposes only a low frequency input is used, so no effort is made to improve the matching at higher frequencies, however the input bandwidth is sufficient to modulate some off-resonance on the order of tens of kilo-hertz if need be.

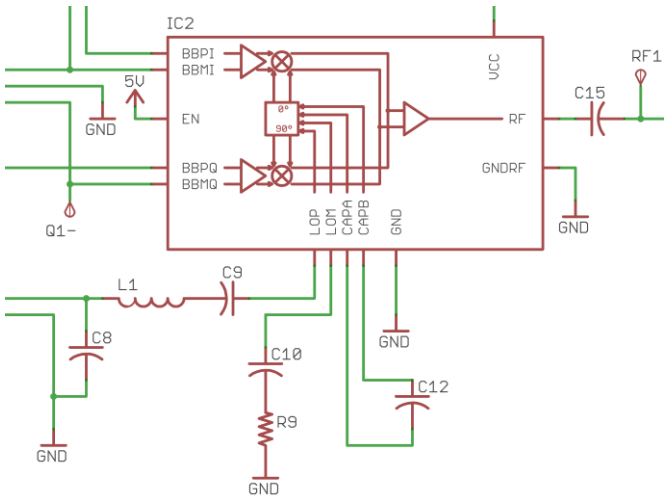


Figure 3.12: The Linear Technologies LT5598 circuit. This forms the primary functional block of the vector modulators.

3.1.2.2 Filter and Preamp

Following the vector modulator stage is a low pass filter and preamplifier located on a pluggable daughter board. The filter has been implemented using discreet components, seen in Figure 3.13, so that it could be tuned to the desired frequency (e.g. 130MHz, 210MHz, 310MHz) so that most of the higher mixing products would be attenuated. This is the only network that needs to be retuned so that the modulator can be used at different frequencies, which is why it is included on a daughter board. After the filter there is a gain stage that is based around the MiniCircuits PSA-545+ monolithic LNA, the circuit is shown in Figure 3.14. It boosts

the level to a point that some attenuation should be needed prior to the next gain stage, allowing the bulk power for a given channel.

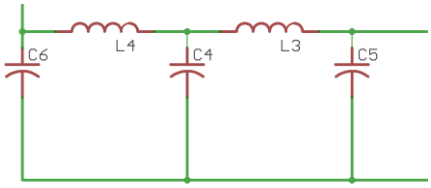


Figure 3.13: A five element, low pass filter. This is designed to remove the higher order mixing products.

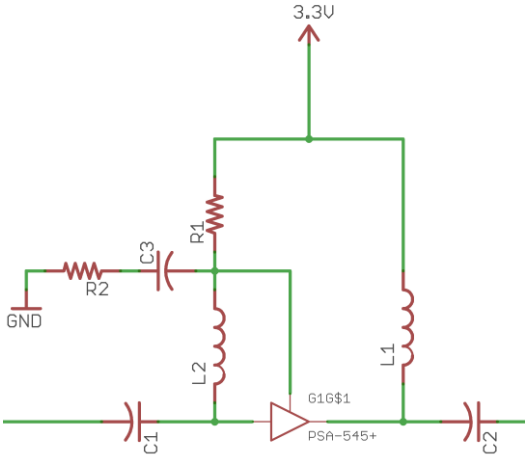


Figure 3.14: A gain stage based around the Minicircuits PSA-545+ monolithic LNA.

3.1.2.3 Digital Step Attenuator and Switch

A variable attenuator is included at the output to allow for bulk changes in the amplitude of the RF. This allows for better utilization of the dynamic range of the system. The step attenuator also allows us to effectively increase the resolution of the modulators. For example, if an RF pulse has low peak amplitude, or if part of a longer pulse train has low peak amplitude, then the attenuation can be increase and the baseband waveforms scaled accordingly. This allows the output of the control system and vector modulator IC to be higher, and the effective resolution to be improved. The minimum output will be controlled by the noise floor of the vector modulator, and by doing this we can operate further above the noise floor when running low amplitude pulses. The attenuator used is the Peregrine Semi PE4302, a 31.5dB attenuator with 0.5dB resolution, the circuit is shown in Figure 3.15. The device is programmed through SPI to reduce the number of signal traces, and it is configured to default to maximum attenuation to reduce the risk during startup or communications failure.

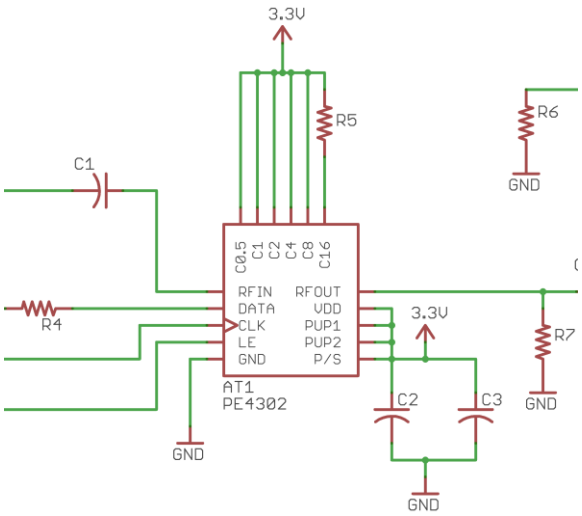


Figure 3.15: The Peregrine Semi PE4302 digital step attenuator circuit. It allows a default attenuation setting to be loaded, and gives a buffered serial interface for setting the attenuation.

The final device on the RF board is an RF switch used to blank the output of the modulators, circuit shown in Figure 3.16. The nature of the vector modulation scheme used puts LO directly on the Larmor frequency so any feedthrough through the modulator can impact the image. This is mostly a problem during long, low average power pulse trains (e.g. 2D RF excitations). The switch allows us to terminate the input to the amplifier chain in 50Ω when the magnitude of the pulse drops below a minimum amplitude. The RF switch takes approximately 75nS to fully cycle (on-off-on) so it should only be used if the pulse waveform drops below the noise floor for longer than this period.

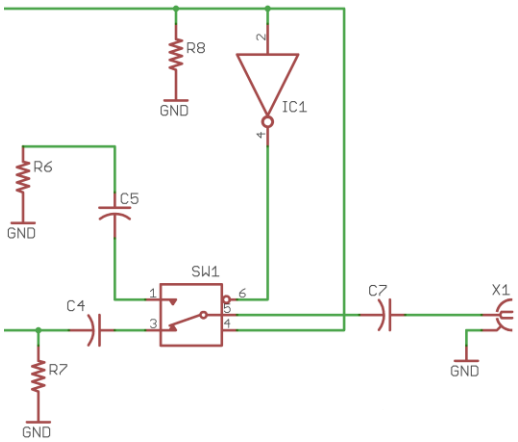


Figure 3.16: The MASWSS0115 solid state RF switch circuit. It is used to blank the output of the modulators. A 50Ω termination is connected to one of the inputs, and the modulator signal is routed to the other, with the common port being the output of the modulator board. This provides a 50Ω termination to the next gain stage independent of the state of the switch.*Support Hardware*

The modulators require some support hardware to function correctly. A set of DC power supplies are needed to provide the desired voltages and RF band pass filters are used to further attenuate any out of band noise or mixing products.

3.1.3.1 Power Supplies

The EOS VLT130-3100-S2, A commercial Switch Mode Power Supply (SMPS) with three output voltages, +3.3V, +5V, and +12V is used as the primary power supply. The +12V rail is not needed for the modulators, but may be useful for other equipment in the transmit system. It is also important that these supplies require active air cooling, with fans that provide at least 32CFM air flow. The second supply is a HengFu HF25W-SL-3.3 floating output supply, configured for negative voltage

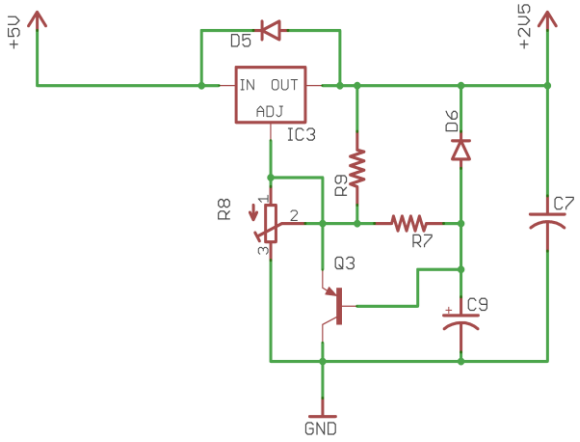


Figure 3.17: The +2.5V regulator circuit. It is designed around the SPX-117 and includes short circuit protection and soft-start.

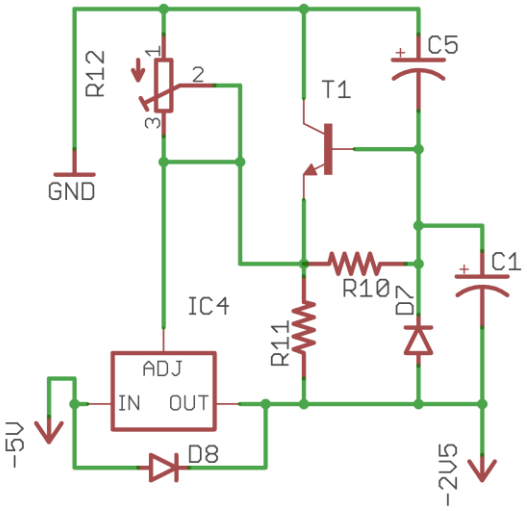


Figure 3.18: The -2.5V regulator circuit. It is designed around the LM337 and includes short circuit protection and soft-start.

In addition to these SMPSs there is a PCB with two voltage regulators that also has the Mini-Fit Jr. power connectors normally used. The two regulators supply the ±2.5V needed by the frontend board, the circuits are shown in Figure 3.17 and Figure 3.18.

3.1.3.2 Filters

The RF output of the modulators should be filtered to remove any out of band noise or higher order mixing products. A simple low pass filter is included on the modulators, but this is only included to reduce high frequency noise to minimize the potential for problems with the on-board preamplifier. A narrower band-pass filter can improve performance by further attenuating any out-of-band noise. For the 128MHz system a bank of MiniCircuits BPF-A127+ filters are used.

3.2 Testing

3.2.1 Primary Setup

The modulators require some basic setup for almost all testing. The major parts are the power supply, the LO source, the control system, and the trigger. The power supply is the one used in actual operation. It consists of two commercial DC switch mode supplies (SMPS and an in-house designed voltage regulator board. The SMPSs need to have constant air flow, so they are mounted in a 19in. rack case with two 32CFM fans. Again, this is how they would be set up for regular use. The LO source will typically be the Signal Forge RF generator set to 128.07MHz center frequency with 30dB of attenuation at the output and the level set to -2dBm with zero offset. The control system is the National Instruments PXI-7853R running custom control software. Our regular software set (that is, what would be used for imaging) will be used. An Agilent 33220A function generator set to pulse mode supplies the trigger. Pulse width and frequency are set on a per experiment basis. This setup will be used for all testing, except where otherwise noted.

3.2.2 LO Feedthrough and Dynamic Range

3.2.2.1 Test Overview

All mixer based systems suffer from LO feedthrough, where signal on the LO port is passed through the device unchanged. Feedthrough in the modulator will significantly contribute to raising the noise floor and limiting the dynamic range. It can also cause artifacts in the image when a long excitation pulse with low average power is used. In this case the tip angle imparted by the LO leakage can be significant relative to the desired excitation pattern. There are techniques that we can use to minimize this problem, but it is important to quantify it first.

3.2.2.2 Test Setup

Measuring the feedthrough will use most of the basic test setup described above. The output of the modulators is monitored with the LeCroy Oscilloscope. It is set to use the smallest V/div that captures the waveform and 1Gsamp/sec, with the input terminated in 50Ω. Port two is connected to the trigger line, and this is displayed as well as triggered off of. The modulators are setup so that all unused outputs are terminated in 50Ω. The calibration constants are set to be neutral (multiply values of one and add values of zero) with zero attenuation and no linearization applied. Three separate conditions are tested. The first is a hard pulse of maximum amplitude, the second is a zero amplitude pulse with the RF switch on, and the third is a zero amplitude pulse with RF switch off. The waveforms are saved to be processed after the data is gathered.

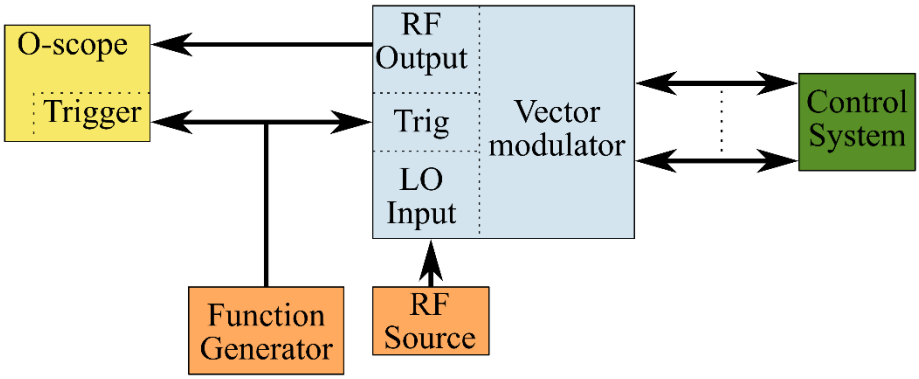


Figure 3.19: Test setup for measuring LO feedthrough of the modulators

The same test was then run using one of the old revision (HPMX-2005 based) modulator boards that was removed from the University of Michigan system. All of the setup and waveforms were the same, with the exception of the DC power supplies due to different requirements of the two boards. The board was not adjusted for this test, so should be representative of the performance it had while in the Michigan system. This includes any drift that occurred over the time it was installed there.

Finally, the new modulator cards were adjusted for best performance, and the test run again. The adjustment is done in two stages: setting V_{OCM} and setting the I and Q add calibration constants. V_{OCM} is adjusted by using the o-scope to measure the value and changing the potentiometer settings until it was 0.5V. The high impedance scope probe can be used to measure the output of the op-amps with a zero waveform file being loaded by the control system. The I and Q calibration constants are, again, adjusted by looking at the output when playing a zero waveform file. The values are changed in small increments to minimize the magnitude of the output.

3.2.2.3 Data

The base LO feedthrough level is first found by calculating the power (in dBm) of the zero amplitude wave with the RF switch on. Example code used to calculated this is found in Appendix L-2. The average LO feedthrough level was -40.23dBm, with a maximum of -34.47. This is the minimum feedthrough level, and can only be scaled linearly by adjusting the attenuation of the modulator. Next the maximum output power is found in the same way, but using the waveform of peak amplitude. In this case the average value was 14.3dBm with a minimum of 14.07dBm. The average dynamic range of the modulators was 54.55dB and the minimum was 48.97dB, which was calculated as the between the feedthrough and max power level. Fine adjustments were made to board one and then retested. The potentiometers and I/Q add calibration values were adjusted following the described procedure. The resulting values are shown in Table 3.1. Calculations for the old modulator boards were done in the same way. The average dynamic range is 40.40dB, which is

significantly reduced from the new revision modulators. It's worth noting that the best performance was 44.25dB, and this is about than 4dB less than the worst performing channel on the new boards.

Channel	Potentiometer		Add Cal	
	I	Q	I	Q
1.1	187	187	0.006	0.003
1.2	189	183	0.0025	-0.005
1.3	189	183	0.0025	0.0175
1.4	187	182	0.0025	-0.0075
2.1	174	162	0.015	0.005
2.2	200	167	0.01	-0.005
2.3	189	197	-0.005	0.0075
2.4	180	171	-0.01	0.005

Table 3.1: Calibration constants for the new modulators to maximize the dynamic range.

Channel	Min(dBm)	Max(dBm)	Dynamic Range(dB)
1.1	-44.06	14.15	58.21
1.2	-44.84	14.23	59.07
1.3	-41.88	14.45	56.33
1.4	-44.83	14.14	58.97
2.1	-45.00	14.23	59.23
2.2	-43.41	13.96	57.37
2.3	-43.80	14.37	58.17
2.4	-42.52	14.25	56.78
Avg	-43.79	14.23	58.02

Table 3.2: Dynamic range of the modulators after calibration as been completed.

Channel	Min(dBm)	Max(dBm)	Dynamic Range(dB)
1.1	-29.65	12.99	42.63
1.2	-25.40	13.03	38.44
1.3	-21.91	13.41	35.31
1.4	-31.18	13.07	44.25
2.1	-29.77	13.91	43.68
2.2	-24.07	13.65	37.72
2.3	-30.02	13.47	43.50
2.4	-24.76	12.90	37.66
Avg	-27.10	13.30	40.40

Table 3.3: Dynamic range of the old modulators.

3.2.3 Amplitude Linearity

3.2.3.1 Test Overview

Modulators can exhibit non-linear output across both the power and phase spectrum. The magnitude envelope out of the modulators may not increase as the output magnitude swings from minimum to maximum. It may also be the case that if a single magnitude is selected and the phase rotated through 360° that the output magnitude will be non-constant.

3.2.3.2 Test Setup

The test setup for basic power linearity is the primary setup, with the output of the channel under test being recorded by the LeCroy oscilloscope. Each waveform is captured at 1Gsample/sec, with a record length of 500kSamples. The V/div are set to the minimum that does not clip the waveform. A set of waveforms is generated for each channel using the 'wf_aramp_gen.m' and 'wf_pramp_gen.m' Matlab scripts shown in Appendix L-3. Each channel has an amplitude ramp with 0°, 45°, and 90° applied phase shift as well as phase ramps at 1, 5, and 10 amplitude. Figure 3.20 shows an amplitude ramp waveform, and Figure 3.21 shows a phase ramp waveform. All channels except the one being tested have zero amplitude and phase waveforms. The calibration constants in Table 3.1 applied for this test.

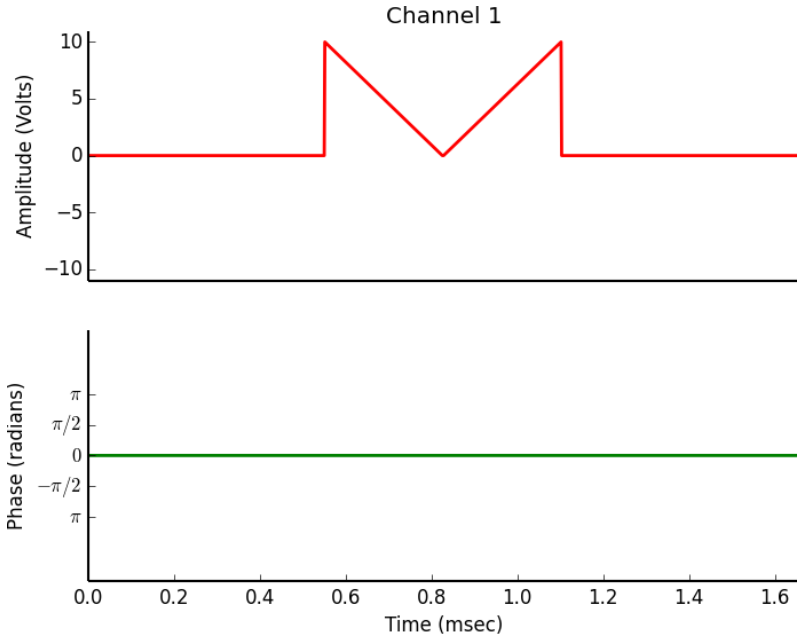


Figure 3.20: Amplitude ramp waveform with zero applied phase shift.

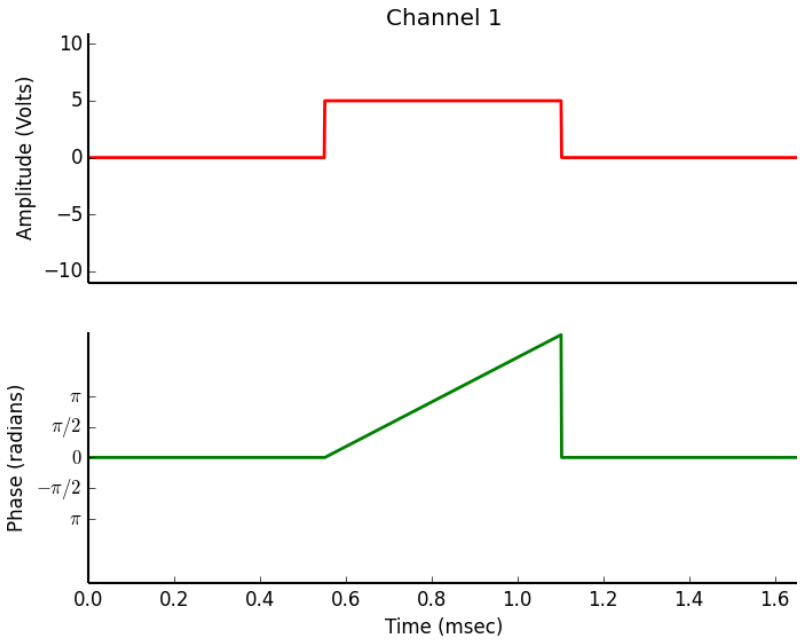


Figure 3.21: Phase ramp waveform with half-scale (+5V) magnitude

3.2.3.3 Data

The waveforms acquired with the oscilloscope need to be converted into envelopes, aligned and trimmed, decimated, and then compared to the desired waveforms from the *.aap files. These procedures are done in the error_calc*.m files. There is a separate .m file for each of the data sets (amplitude ramps at 0°, 45°, and 90° and the phase ramps at 1,5 and 10 magnitude) that only differ in the file names they read and write. The file for the 10 magnitude phase ramp is shown in Appendix L-4.

Once the waveforms are read in they are converted to an envelope. The magnitude of the Hilbert transform of the data gives a basic envelope, but it still needs to be filtered. In this case a 5th order Chebyshev filter with 0.5dB of passband ripple is designed. The cutoff frequency is located at 20kHz, which removes most residual RF and high frequency noise from the signal, but does not significantly degrade the edges of the waveform. An edge finding algorithm is then run over the data and returns the first and last edge (code for this is also shown in Appendix L-5). These edges mark the start and end of the waveform, which are then used to trim the data. The waveform from the .aap file is also trimmed to remove any zero padding. Data from the o-scope is sampled at a much higher rate than the waveform is defined, which can complicate direct comparison of the two. Instead, the captured data is decimated to have the same number of points as the .aap file waveform. This requires some hand adjustment because the decimation algorithm in Matlab does not always produce usable data points at the ends of the data, and may also not produce the desired number of data points. Finally, both the data and the .aap file are normalized to simplify extracting an error term. Both are normalized to their peak amplitude.

At this point the captured waveforms and the .aap file can be compared. The error in the magnitude is found at each point by simple subtraction. The root-mean-square error (RMSE) is then found for each of the files. Table 3.4 shows the RMSE terms for the amplitude ramp waveforms, and Table 3.5 shows the same, but for the phase ramp waveforms.

Channel	Error		
	0°	45°	90°
1.1	0.0565	0.0438	0.0859
1.2	0.0678	0.0584	0.0928
1.3	0.0657	0.0558	0.0950
1.4	0.0585	0.0465	0.0826
2.1	0.0639	0.0481	0.0916
2.2	0.0639	0.0451	0.0861
2.3	0.0674	0.0569	0.0968
2.4	0.0684	0.0533	0.0969
avg	0.0640	0.0510	0.0910

Table 3.4: Root Mean Square Error of an amplitude ramp waveform at different phase shifts.

Channel	Error		
	1	5	10
1.1	0.1389	0.1850	0.1238
1.2	0.1458	0.2153	0.1378
1.3	0.1605	0.2031	0.1172
1.4	0.1187	0.1725	0.1155
2.1	0.1383	0.1830	0.1190
2.2	0.1442	0.1965	0.1329
2.3	0.1446	0.2048	0.1248
2.4	0.1492	0.1802	0.1120
avg	0.1425	0.1926	0.1229

Table 3.5: Root Mean Square Error of a phase ramp waveform at different amplitude shifts.

The tables show that there is some significant non-linearities. Looking at the plot of the amplitude waveforms (and example shown Figure 3.22) indicates that the problem may be exaggerated due to gain compression near the maximum amplitude. The gain of the modulator also clearly varies with the phase in Figure 3.23.

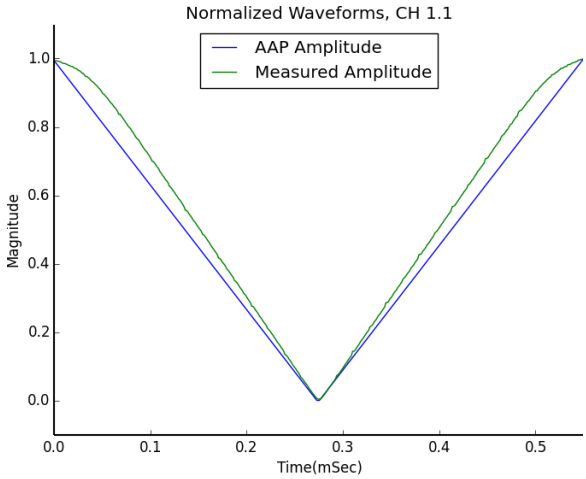


Figure 3.22: Channel 1.1 amplitude ramp waveform envelope compared to the desired amplitude.

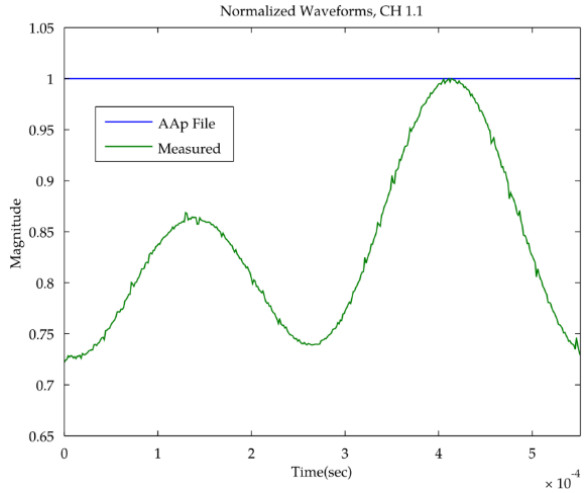


Figure 3.23: Channel 1.1 phase ramp waveform envelope compared to the desired amplitude.

3.2.4 Phase Linearity

3.2.4.1 Test Overview and Setup

The variation in phase with changing power levels was also measured. A S_{21} measurement through the modulators is used to evaluate the variation in phase at different output amplitudes. The HP4395A network analyzer was setup to measure S_{21} with a zero span sweep, and an RF output level that is nominally -32dBm. There is a loss of approximately 7dB in the test head, making the input level to the modulators roughly -39dBm. This is not critical, but should be within the linear range of the modulators and high enough to make measurements stable. The modulators were set to play back a constant amplitude CW pulse at different amplitudes. Measurements were made at amplitudes of 10, 8, 4, 2, 1, 0.5, 0.25 and 0.1. The S_{21}

measurements were recorded as phase shift and gain. The measurements have been made using a single channel, operated at 128MHz. The files all had zero phase shift, and were simple CW pulses. At higher output levels there is not much variation in the phase, however below an amplitude of one the phase begins to drift significantly.

3.2.4.2 Data

Data was gathered for channel one of one of the boards. The phase appears to be very constant at higher amplitudes, but begins to drift significantly below an amplitude of about 0.5, as shown in Table 3.6. Part of this is due to the nature of the modulation scheme vs. the measurement scheme. The waveforms are specified on the I/Q plane, which is a Cartesian grid. In contrast, the measurements are made as phase and amplitude, which is a polar grid. The result is that constant resolution in I/Q is not constant resolution in phase/amplitude. Phase resolution will be lost at low amplitude levels.

Amplitude	Gain(dB)	Phase(degrees)
10	25.27	114.95
8	23.80	114.55
6	21.65	114.15
4	18.15	113.65
2	10.92	113.05
1	2.28	112.3
0.5	-5.95	111.0
0.25	-12.65	108.5
0.1	-20.1	102.8

Table 3.6:Modulator Gain and Phase at different amplitude settings.

3.3 Discussion

The vector modulators are a compact, easy to integrate solution for adding additional channels to a transmit system. Testing showed that they are capable, but exhibit some non-linearities and imbalance between the I/Q channels, especially at lower frequencies. It is unclear why this is the case, as the data sheet indicates that performance should be good. This appears to be an implementation problem, and is not a theoretical limit of the modulators. A linearization system can improve the performance of the modulators. This has been implemented as a look-up table based prediction method in the control software. An alternative would be to use a real-time Cartesian feedback technique. This may be a difficult system to implement, but should be possible.

Additional work on the controls system would see other performance benefits. One would be better dynamic control of the step attenuators. This could be used to implement resolution improvements at low power levels, and avoid the highly non-linear regions near zero amplitude. Substantial modification to the

linearization and waveform preprocessing would be needed, but there are no fundamental limitations preventing this method from being implemented.

CHAPTER 4
RF POWER AMPLIFIERS

4.1 Current Source Amplifiers

The B_1^+ of transmit coils is generated by the current on the element. The phase and amplitude of this field correspond to the phase and amplitude of the current on the element. Parallel transmit systems need to be able to control the amplitude and phase on each element independently, which is achieved by decoupling the elements. Parallel receive systems typically accomplish decoupling with a combination of preamplifier and capacitive or inductive decoupling methods. This suppresses the current induced in the coil, preventing cross-talk. This works well because the receive system is sensitive to the induced EMF. Preamplifier decoupling is not suitable for parallel transmit systems because they require currents of high amplitude to generate the desired B_1^+ field.

One such drive/decoupling mechanism is the RF current source[45], [48] which is a modified version of the classical RF amplifier, as seen in Section 2.3.2. The current source amplifier takes advantage of the fact that FETs behave as controlled current sources. Their drain to source resistance appears very high, on the order of kilo-ohms, when they are operated in the saturation region (see Appendix B). The RF current source concept is similar to the principle of the antennafier element[49] and active integrated antennas[50]–[53] where studies have shown that integrating the antenna to the active device results in the feed network of antenna arrays becomes less sensitive to the effects of mutual impedance than equivalent passive arrays driven by classical RF amplifiers due to the unidirectional nature of the active devices.[54] The design of this network directly trades an optimal power match for higher isolation. Looking at the formulation of the matching network will help us understand this.

4.1.1 Matching Network Overview

A simplified circuit schematic of the RF current source is shown in Figure 4.1. As mentioned before, the RF power MOSFET is a RF voltage controlled RF current source. Comparing Figure 4.1 and Figure B-7 the RF current source is implemented by replacing the optimal load resistance of the classical RF amplifier by an RF coil that is tuned to series resonance at the Larmor frequency such that it presents a low resistance load to the MOSFET. If the output capacitance (C_{os}) is not compensated for by a conjugate match it forms a parallel path for current, reducing the amplitude of the current driven through the RF coil. For improved RF current source performance, C_{os} is tuned out using a parallel inductor such that the RF current driven through the RF coil is maximized.

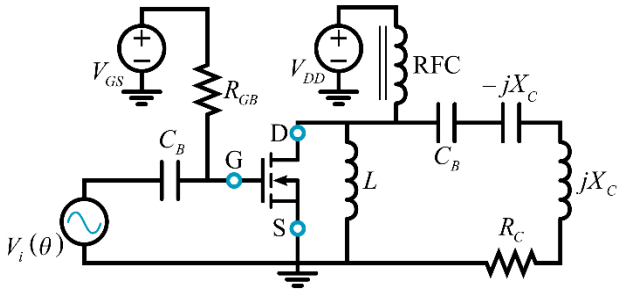


Figure 4.1: The basic current source amplifier replaces the optimal load with a series tuned, low resistance coil element. The inductor L is tuned to resonate with C_{os} so that there is only one path for the coupled current.

This introduces some difficulty if the coil is to be used as a transmit/receive coil. The coil matching network used with current source amplifiers does not lend itself to receive systems. It is possible to integrate a matching network with the T/R switch, so that the coil is appropriately tuned for the two cases, but a simpler approach is to use a second receive only coil.

4.1.2 Analysis of the Current Source Network

The amplifier matching network is made up of a single inductive element resonated with the output capacitance so that:

$$L = \frac{1}{\omega^2 C_{OS}} \tag{4.1}$$

This results in a high impedance load for the coil. The exact impedance will be impacted by the Q of the resonate circuit, which tends to increase with lower values of C_{OS} since this increases the value of the inductor L. This design does not attempt to transform the low impedance of the tuned coil, so the MOSFET will not have an optimal load resistance. Therefore, the same RF current amplitude, I_0, driven into the RF coil will result in a voltage drop, V_0, that is significantly reduced compared to the optimal load resistance in a classical amplifier design. This reduces the V_{DS} swing which results in a load line that no longer spans the saturation region of the MOSFET DC characteristic curve shown in Appendix B-1. In fact, the lower the RF coil resistance, the closer the load line is to a vertical line as shown in Figure 4.2.

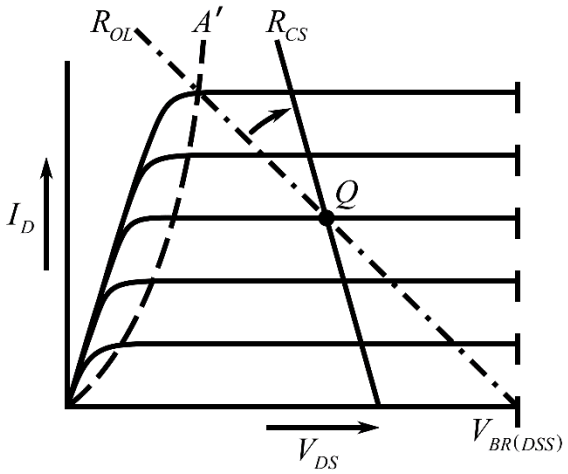


Figure 4.2: The current source amplifier has a lower load resistance than is optimal. This corresponds to a steeper load-line, meaning that for a given swing in output current there is a smaller swing in drain-source voltage.

The induced current (i.e. magnitude of the coupling) will be reduced by the high impedance of the MOSFET. This can be seen by looking at the amplifier with the coil, and replacing the MOSFET with a hybrid pi model (seen in Figure 4.3(a)).

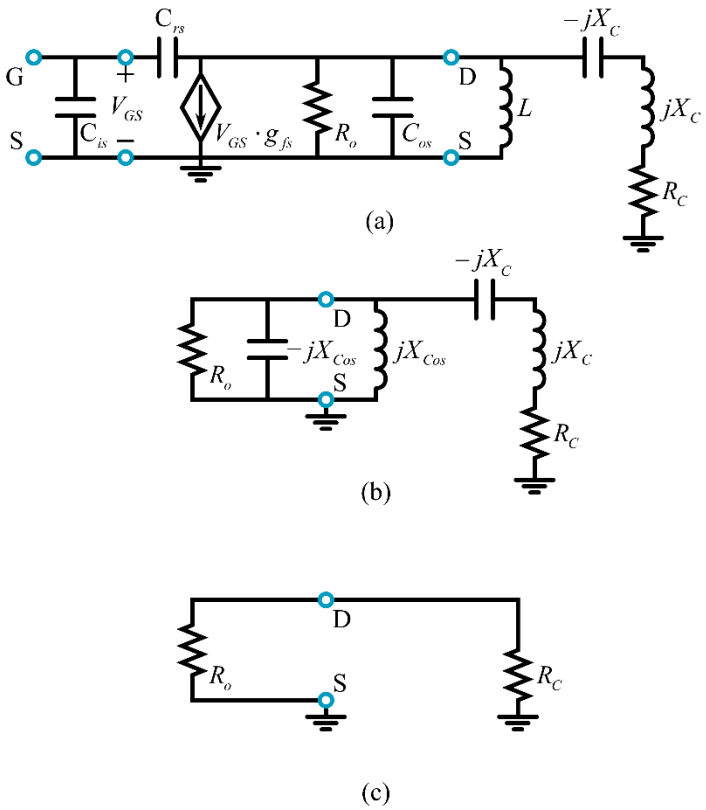


Figure 4.3: The MOSFET is replaced by the hybrid pi model , and the coil is represented by a lumped element RCL circuit(a). The coil is tuned so that the L and C elements resonate. We are only concerned about the output of the MOSFET at this point, so ignore the gate and associated components. The current source can be replaced with an open circuit, and the inductor L is tuned to resonate with the output capacitance C_{os} (b). Removing the resonate sections we are left with two series resistances, as per (c).

The we can reduce the circuit to only passive devices at the output of the amplifier, as in Figure 4.3(b). Further, there are two resonate circuits: the MOSFET output has a tuned tank that will be high impedance, and the coil has a series resonate circuit. This reduces the circuit to the R_o and R_C in series (Figure 4.3(c)). Coupling in to this circuit would manifest and an EMF induced on the coil element, that is a series voltage source. We have previously seen that R_o is a large value, so this will result in a relatively small induced current. This is the fundamental way that current source amplifiers reduce coupling.

If we consider the standard amplifier case we know that the coil is conjugate load matched to a 50Ω system. So based on this, we can see that an induced EMF (V_{EMF}) will produce a current on the coil (I_{50}) defined by:

$$I_{50} = \frac{V_{EMF}}{Z_C + Z_C^*} = \frac{V_{EMF}}{2R_C} \tag{4.2}$$

Similarly, the current source will have an induced current, I_{CS}, of:

$$I_{CS} = \frac{V_{EMF}}{R_o + R_C} \tag{4.3}$$

Dividing (4.3) by (4.2) allows us to calculate the ratio of currents for the two cases.

$$\frac{I_{CS}}{I_{50}} = \frac{\frac{V_{EMF}}{2R_C}}{\frac{V_{EMF}}{R_o + R_C}} = \frac{2R_C}{R_o + R_C} \tag{4.4}$$

We know that $R_o \gg R_C$, so then $I_{CS} / I_{50} \ll 1$. That is to say, the current source amplifier will significantly reduce the current coupled into a coil.

If we consider the active case and do not hold the output of the MOSFET at zero, then we see that the total voltage across the MOSFET terminals is the vector sum of $V_{DS}(\theta)$ and $V_{EMF}(\theta + \phi)$. Examining the characteristic curves in Figure 4.2 shows that variation in the drain-source voltage will have negligible impact on the output current, I_O. This means that I_O is completely controlled by the input voltage, so the coil is decoupled from all other coils.

4.1.3 ARF545FL Current Source

Current source amplifiers were implemented based around the ARF475FL from MicroSemi. The device is a 1kW, 150V, 10A LDMOS device. The device is a push-pull NMOS device, as opposed to the single ended structure that has been discussed thus far. A schematic of this circuit is included in Appendix K-4. The amplifier is biased as a class AB linear system, with a quiescent current of approximately 200mA (100mA per active device). The input matching is constructed using a lattice balun to produce the balanced feed needed for a push-pull amplifier. The matching network consists mostly of shunt capacitors with a series inductor. There are shunt resistors on the recommendation of the spec sheet in order to improve the stability of the amplifier.

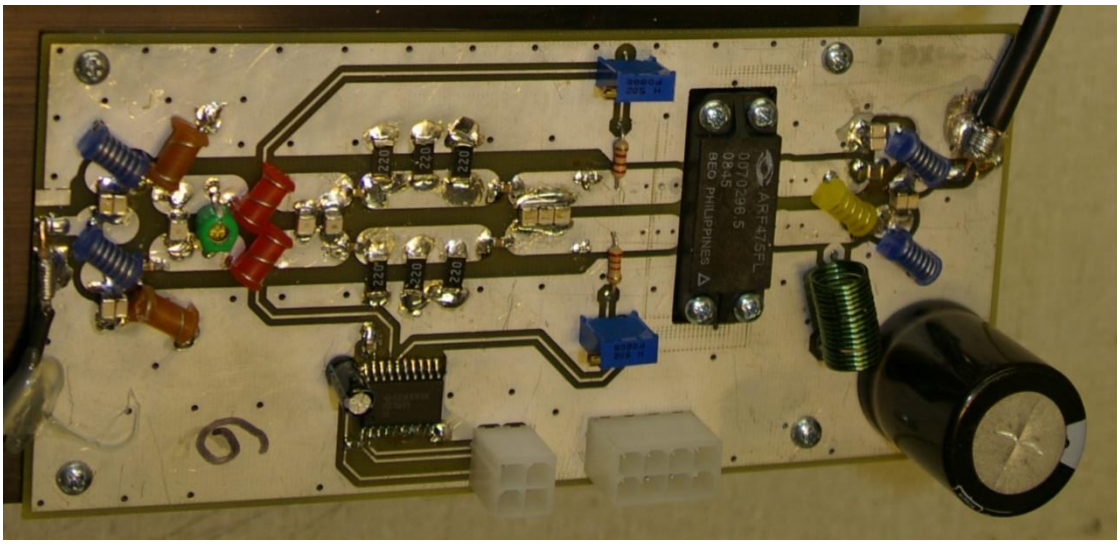


Figure 4.4: Amplifier module based on the ARF475FL. The input is on the left of the image, with output on the right. The output matching network is comprised of a single inductor (yellow on right). Power, gate, and drain bias are supplied through the white connectors at center bottom.

The amplifier supply lines need to be bypassed with large electrolytic capacitors, and isolated with RF chokes. If this is not done, then the amplifiers will become unstable at high power due to RF coupling into the DC supply lines.

4.1.3.1 Input Lattice Balun

The input to the amplifier starts with a lattice balun, the basic structure is shown in Figure 4.5. This is a lumped element circuit that is designed to convert the unbalanced input to the balanced signal needed to drive the push-pull device. Many different balun structures exist and are used, this particular design has two advantages: it uses lumped elements, so can be compact at lower frequencies, and it the need for ferrites that can exhibit non-linearity at high power.

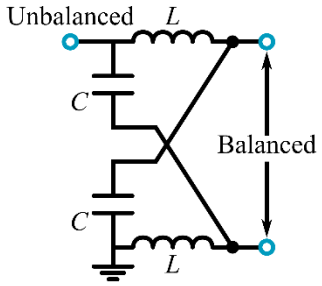


Figure 4.5: The basic lumped element lattice balun. The component values can be calculated to give a conversion from one impedance to another, and are deterministic. No ferrites are needed and the $\lambda/4$ section is constructed with lumped elements. This makes for a compact circuit that can easily handle high powers.

The component value can be found based on the following equations:

$$C = \frac{1}{\omega Z_C}$$
$$L = \frac{Z_C}{\omega} \tag{4.5}$$

Where $Z_C = \sqrt{R_{Unbalanced} R_{Balanced}}$ and $\omega = 2\pi f$.

4.1.3.2 Input Matching Network

The input matching network for this amplifier is somewhat non-standard. In addition to a multi-stage LC network there are shunt resistors included, as seen in Figure 4.6. These resistors reduce the gain of the amplifier, but substantially improve the stability. The device used has sufficiently high gain that this is a superior design to a true lossless network. Aside from this, the network is reasonably typical. It uses a cascaded series of capacitors and inductors in a balanced network. A mica compression capacitor is included to tune the input. Note that good quality components must be used for this network. Coil Craft air core inductors and ATC RF capacitors with an NP0 thermal constant are recommended.

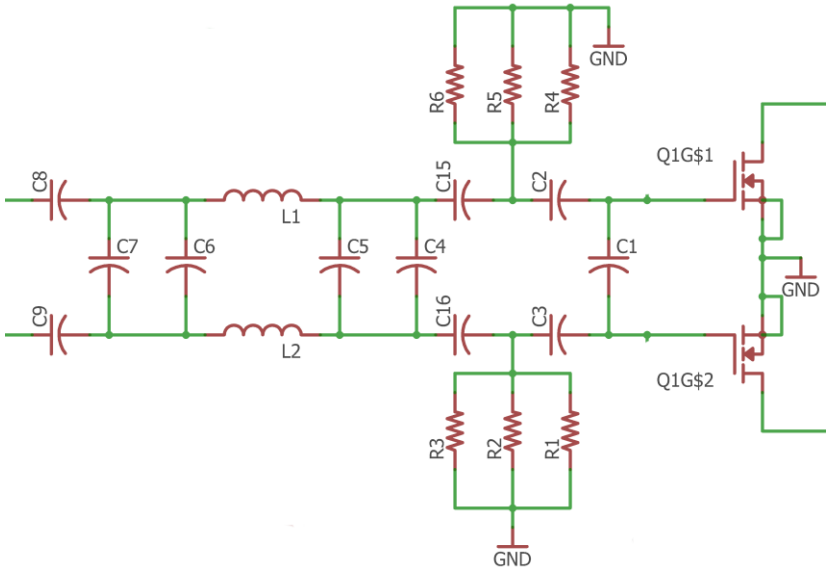


Figure 4.6: The input matching network for the Current Source amplifier.

4.1.3.3 Current Source Biasing

Correctly setting the bias point for the gate and drain of the amplifier is important to ensure proper operation. The drain voltage is relatively straight forward, primarily needing a high current (10A+) power supply that operates at 150V. The supply should be over-speced by 25%-50% to account for the efficiency of the amplifier and allow some headroom to prevent edge case problems. Additionally, because of the high RF

powers involved there needs to be adequate bypassing and decoupling on the DC bias line. This is accomplished with a combination of shunt capacitance and series inductance. The initial element should be a high value RF choke or near resonant inductor. This will provide significant RF blocking. Following this with a set of shunt capacitors that are ceramic and have either X7R or NP0/C0G dielectrics will substantially reduce the RF coupling. It is generally a good idea to include multiple capacitors at a few different values (e.g. a capacitor of 1nF and one of 2200pF). This can then be followed by an additional single turn ferrite core inductor, then another set of shut capacitors. Finally, there should be a high valued shunt electrolytic capacitor. These amplifiers are extremely high power, and sensitive to correct bypassing and isolation of the supplies, so it is not recommended to attempt using a less isolation.

The gate bias is substantially more sensitive, and must be adjusted with the amplifier powered on. A simplified circuit for doing this is shown in Figure 4.7. In this case, the adjustment is done based on the quiescent current through the drain. This sets the operating point, and establishes the class of operation for the amplifier (see Appendix D). A high power linear amplifier will typically be operated in class AB, which corresponds to some small amount of quiescent current. In this case, we use 100mA quiescent current per device (200mA total for an amplifier). This corresponds to 30W of power statically dissipated in the device, which is a non-trivial amount of power. When setting the bias point this needs to be considered, and the amplifier should not be held on (even with no input signal) for extended periods of time. During normal operation the amplifier should not exceed 10% duty cycle or 100mSec continuous on time to prevent damage. This is because of the high powers that are dissipated in the device itself, even in class AB operation.

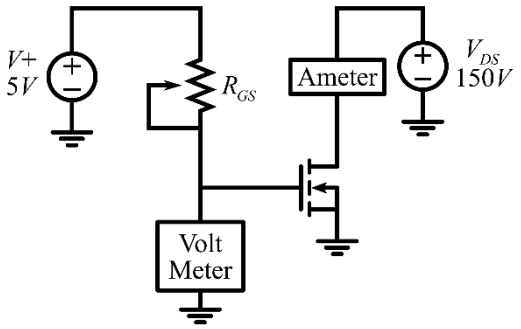


Figure 4.7: The basic circuit diagram for setting the bias point of an amplifier. The matching networks and bypassing components have been left off for clarity, but should be in place for setting the operating point. The volt meter measuring the gate voltage is not strictly needed, but is useful for ensuring correct operation. The ammeter reading is used to actually set the operating point. The potentiometer is adjusted until the desired quiescent current is obtained (between 100mA and 200mA in this case). Higher quiescent currents will produce more linear results, but have lower efficiency.

4.2 Low Output Impedance Amplifiers

The operation of the low output impedance amplifier is, as discussed in Chapter 2.3.3, directly analogous to the operation of the low input impedance preamplifier. The amplifiers present a near short to the coil, and the coil matching network acts as a high impedance node across the coil terminals. This prevents induced currents, and so coupling mitigated. From here we can see that there are two simultaneous requirements for amplifier output matching network: 1) that the matching network transforms a 50Ω load into the optimal impedance for the active device. 2) That the network transforms the drain-source impedance of the device into a small, pure real impedance. With these two conditions in mind we can formulate a matching network for the amplifier.

4.2.1 Matching Network Overview

Recalling the hybrid-pi model from Appendix B-2 will help make the matching network design clearer. The output is modeled as a voltage controlled current source paralleled by a resistance (R_O) and capacitance (C_{OS}). Varying the Drain-to-Source Voltage (V_{DS}) changes the value of this capacitance, but a class A/B linear amplifier operates at a fixed so we will treat it as a simple fixed value that we can expect to be around 100pF. The output resistance of a MOSFET is typically on the order of a few kilo-ohms. This leads to an output impedance of the device that will typically have a very small real component with some amount of reactance.

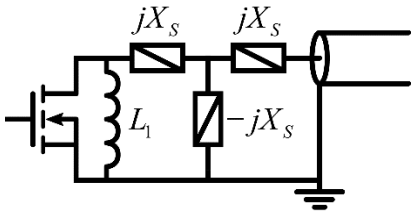


Figure 4.8: Simplified output matching network for the LOI amplifier. L_1 is selected to resonate with the output capacitance of the device, and the Tee network is used to provide a match, as well as form a series resonate circuit.

The basic matching network is built of four components, as shown in Figure 4.8: a shunt inductor (L_1) that cancels C_{OS} , then a reactive Tee-network (labeled X_S and $-X_S$)with the shunt and series elements are series resonant. This combination allows us to achieve both conditions at once, matching for power and a low impedance load for the coil. Fortunately, the values for all of these elements can be directly calculated and shown to provide the desired performance.

4.2.2 Matching Network Calculations

Selecting the value of L_1 is reasonably straightforward, as it simply resonates with C_{OS} , this removes the reactance from the output impedance. The Tee-network can be either high-pass (series capacitor, shunt

inductor) or low-pass (series inductor, shunt capacitor). Both configurations are valid, but one may result in component values that are impractical in the real world, such as a very small inductance. The value of the series elements is found based on the optimal load resistance (R_{OL}) and the system impedance (50Ω):

$$R_{OL} = \frac{1}{50\omega^2 C^2} = 50\omega^2 L^2 \tag{4.6}$$

The shunt element is then selected to resonate with the series element. These conditions will produce both a power match and a low impedance load for the coil.

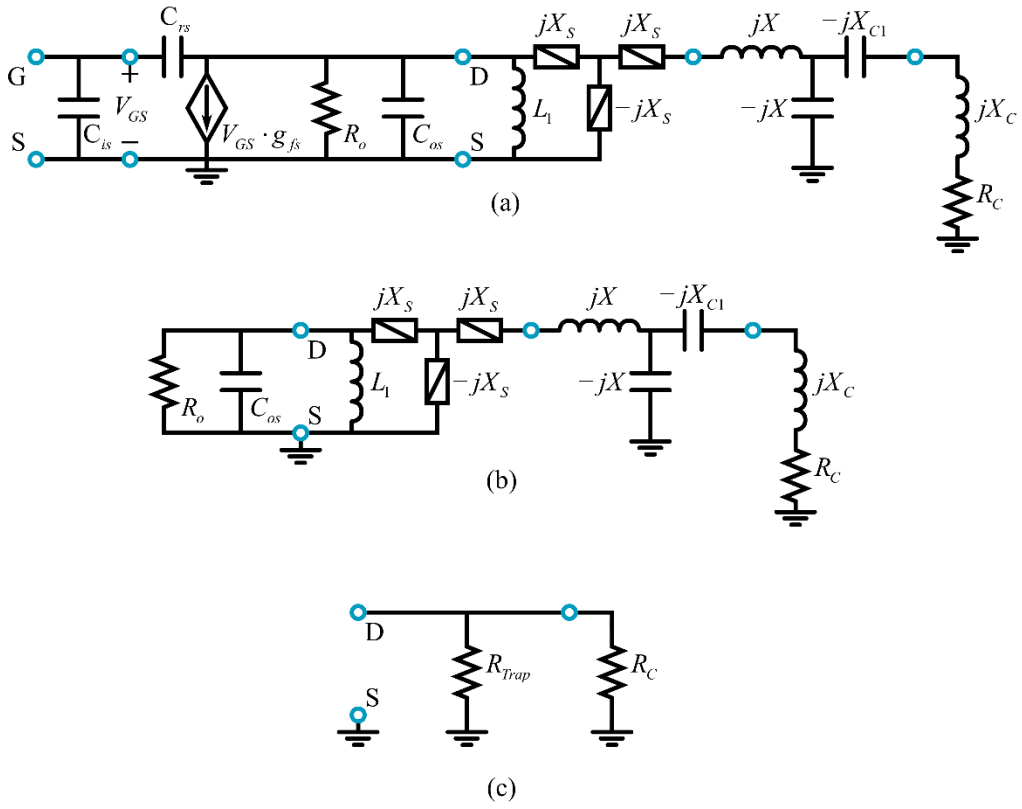


Figure 4.9: Matching network, with the device replaced by the hybrid-Pi model. The complete model is shown in (a), a this time we are not concerned with the input matching at this point in time. This allows us to reduce the model to what is seen in (b). Further, the voltage controlled current source is high impedance, so can be treated as an open circuit. Finally, accounting for the resonant circuits that are built into the design yields an approximate circuit shown in (c), where the coil is simply loaded with a high impedance tank R_{Trap}

These calculations can be derived based on the hybrid-pi model. Combining the hybrid-pi model with the output matching network, we have the circuit shown in Figure 4.9(a). We are only considering the output at the moment, so the input matching/biasing networks are not shown and we can remove the Gate

side components. The feedback capacitance C_{rs} should be negligible in a well designed MOSFET, so we can also ignore that. Further, a current source has infinite impedance, so can be replaced with an open-circuit when evaluating a circuit. Because of this our analysis can proceed using a simple circuit made only of passive devices, as shown in Figure 4.9(b). L_1 is designed to resonate with C_{OS} so a high impedance tank circuit is formed. This allows us to remove C_{OS} and L_1 and replace them with an open circuit, so the load the coil sees (Z_{OUT}) is given by:

$$Z_{OUT} = -jX_S \,||\, (R_o + jX_S) + jX_S = \frac{X_S^2}{R_o} \tag{4.7}$$

This shows that large values of R_o will result in a low impedance being presented to the coil. Similarly the load seen by the MOSFET (Z_L) for a 50Ω system can be found as:

$$\begin{aligned} Z_L &= j\omega L_1 \,||\, \left(jX_S - jX_S \,||\, (jX_S + 50) \right) \\ &= \left(\frac{50}{X_S^2} + \frac{1}{j\omega L_1} \right)^{-1} \end{aligned} \tag{4.8}$$

The optimum load impedance for the MOSFET (Z_{OL}) may be considered to be the optimum load resistance in parallel with parasitic output capacitance (C_{OS}) so that:

$$Z_{OL} = R_{OL} \,||\, C_{OS} = \frac{1}{R_{OL} - j\omega C_{OS}} \tag{4.9}$$

In order to achieve the highest output power possible for the MOSFET we want to have the load impedance equal to the optimal load for the MOSFET ($Z_L = Z_{OL}$). Substituting (4.8) and (4.9) into this, and resonating the output capacitance (i.e. $\omega L_1 = 1/\omega C_{os}$) we have:

$$\begin{aligned} Z_{OL} &= Z_L \Rightarrow \\ \frac{1}{\frac{1}{R_{OL}} - j\omega C_{OS}} &= \frac{1}{\frac{50}{X_S^2} - \frac{j}{\omega L_1}} \\ R_{OL} &= \frac{X_S^2}{50} \end{aligned} \tag{4.10}$$

Maintaining these conditions will result in an amplifier capable of producing the maximum rated power of the active device, and also a low impedance load for the coil. It is worth seeing how this is implemented in a real world configuration, as there are some practical concerns to be managed.

4.2.3 Coil Matching Network

Proper operation of the amplifier depends on a suitably designed coil, so we will briefly examine the coil matching network. The coil needs satisfy two primary conditions: 1) the coil must be matched to 50Ω and 2) the coil's matching network must form a trap when connected to the amplifier. The first condition is necessary to prevent reflected power at the coil port as well as presenting the optimal load to the coil. The

second condition is the mechanism by which the isolation is actually achieved. A three element matching network can be used which both matches the coil to 50Ω and forms a high impedance tank, shown in Figure 4.10. In practice, this network produces component values that cannot be realized, but other networks that achieve the same goals have been described.[55]

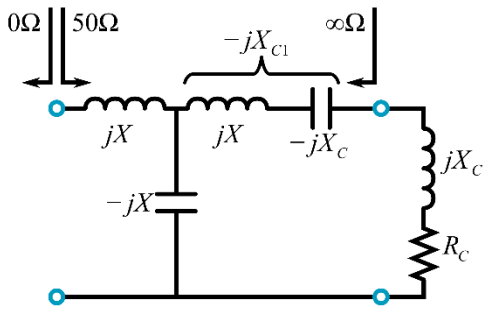


Figure 4.10: The basic matching network for a LOI coil. This is identical to the network used with low input impedance preamplifiers. The matching network forms a high impedance tank across the coil, preventing current from being induced.

4.2.4 Output Matching Network for the ARF475FL

An example design using the ARF475FL (Microsemi PPG) for 3T will serve to demonstrate the above calculations. This device is rated for 1kW output power at 128MHz as a pulse amplifier, so is suitable for use in MRI. ARF475FL is a common source push-pull pair with two NMOS devices in a single package, as shown in Figure 4.11. The design equations that have been formulated are for a single ended device, and push-pull, so they cannot be directly applied. Fortunately, a straight forward to conversion can be used transform a single ended network design into a balanced design.[56] This allows us to design one half of the matching network with the device matched to 25Ω instead of 50Ω. This difference accounts for the conversion from balanced to unbalanced in the matching network.

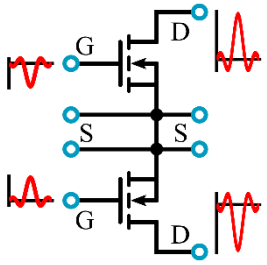


Figure 4.11: The ARF475FL is a push-pull device. This means there are two separate NMOS devices in the package. The source pins are bonded together, so a common-source amplifier architecture is needed for this device.

The data sheet for the MOSFET specifies the optimum load impedance at 120 MHz (a negligible difference from 128MHz) as $10-j20\Omega$ measured between the drains of the two devices, so it has a single-ended impedance of $5-j10\Omega$. The value of L_1 is found as shown in Figure 4.12, which resonates it with C_{os}. So L_1 is found to be 15.5nH, and the impedance will now be $25+j0\Omega$. This tells us that R_{OL} is 25Ω, which is needed for calculating the component values in the T-network. Substituting R_{OL} and the 25Ω system impedance into equation (4.6) allowing us to calculate values for C and L as:

$$R_{OL}=\frac{1}{25\omega^2C^2}=25\omega^2L^2 \tag{4.11}$$

$$C=\sqrt{\frac{1}{25\omega^2R_{OL}}}=\sqrt{\frac{1}{25\left(2\pi128\cdot10^6\right)^2}}=49.7\,pF \tag{4.12}$$

$$L=\sqrt{\frac{R_{OL}}{25\omega^2}}=\sqrt{\frac{25}{25\left(2\pi128\cdot10^6\right)^2}}=1.25nH \tag{4.13}$$

We will select the element to be a 49.7pF capacitor since an inductor of 1.25nH is difficult to obtain. The shunt element is and inductor that resonates with this having a value of:

$$\omega=\frac{1}{\sqrt{LC}}\Rightarrow L=\frac{1}{\omega^2C}=\frac{1}{\left(2\pi128\cdot10^6\right)^2\,49.7\cdot10^{-12}}=31nH \tag{4.14}$$

Plotting this on the Smith chart shown in Figure 4.13 shows that the Tee-network brings us to the desired 25Ω.

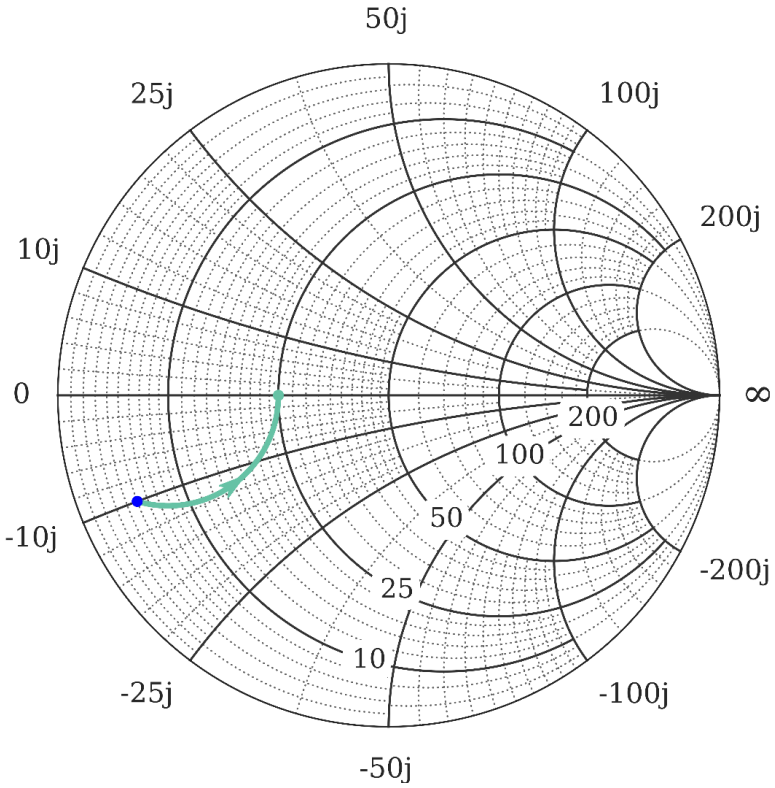


Figure 4.12: Smith chart showing the impedance transform from adding $L_1 = 15.5nH$.

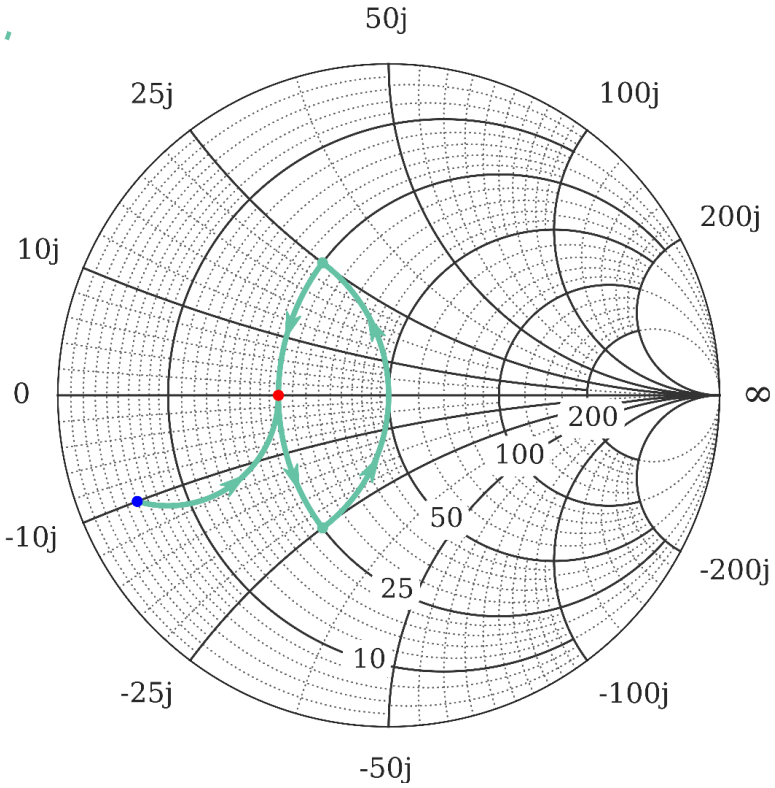


Figure 4.13: Smith Chart showing the transit of the full LOI matching network. This network is for the single-ended case and will be modified for the push-pull amplifier.

The calculations are completed, so the design can be converted to a balanced network. The shunt inductors are doubled in value, and the series elements replicated in the other branch. The conversion takes advantage of the virtual ground between the two halves of the circuit, which is why the inductor value is doubled (shunt capacitances would be halved.) The full matching network is shown in Figure 4.14. The final component values will be $L_1 = 31nH$, $C = 50pF$, and $L = 31nH$.

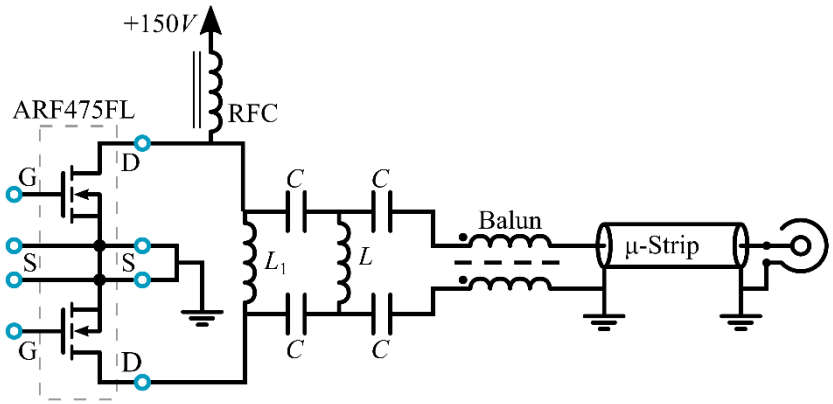


Figure 4.14: Matching network for the ARF475FL LOI amplifier.

Figure 4.15: An LOI amplifier module based on the ARF475FL. Input on left, output on right. This module include a thermal sensor on the MOSFET package, and a biasing network to switch the PIN diode TR switch.

4.2.5 Input Matching Network

The input matching network for the LOI amplifier is shown in Figure 4.16. It is, in many ways, very similar to the one used with the current source amplifier. Some variations were made that result in a different realization of the network. First, the lattice balun was replaced with a Transmission Line Transformer (TLT) balun, the construction of this element is shown in Figure 4.17.

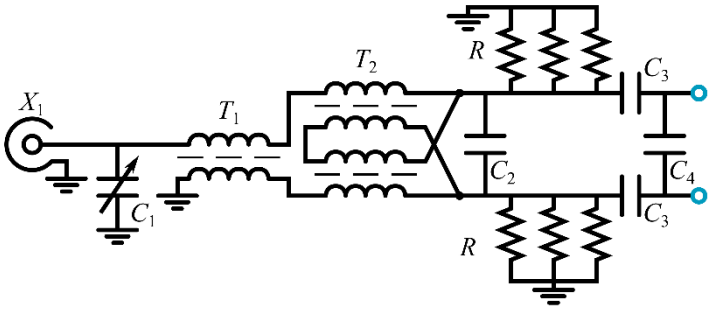


Figure 4.16: The input matching network for the LOI amplifier. C_1 is an poly-film trimmer capacitor for final adjustment of the network. T_1 is a TLT balun, and T_2 is a 4:1 TLT. C_2 is used to compensate for leakage in the TLT, followed by the resistors R that are used to produce a "center tap" for the TLT and stabilize the amplifier. C_3 act primarily as DC blocking capacitors, and C_4 is used to resonate the gate series gate impedance of the MOSFET.

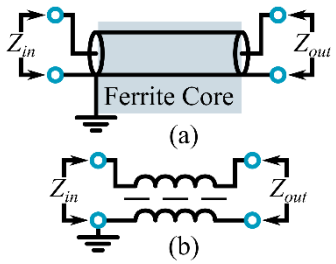


Figure 4.17: The TLT 1:1 balun. The physical layout is shown in (a), while the schematic representation is shown in (b).

The design is based on Guanella's 1:1 TLT balun, with the ferrite presenting a high-impedance to external shield currents as shown in Figure 4.17. RG-188 50Ω coax is used for the transmission line in this device, both for electrical performance and in order to physically fit into the ferrite. The limiting factor on this is that the ferrite must not saturate due to the RF power level. This is why the balun is separated from the 4:1 TLT that follows, which is substantially more sensitive. This also uses a binocular ferrite and 25Ω coax cable (Beldon 83305 PTFE dielectric, shielded hookup wire is an adequate substitute) connected as shown in Figure 4.18. These two TLT devices reduce the number of lumped element components needed, and are largely insensitive to frequency, so require no tuning or adjustment.

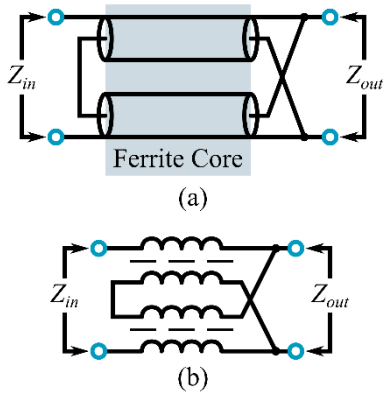


Figure 4.18: the 4:1 Transmission Line Transformer. The design is based on Guanella's 4:1 balun, but it is configured to operate in a balanced form on both sides (a balbal, perhaps). Z_{in} will be a factor of four higher than Z_{out} for this design. Note that the "in" and "out" designations are somewhat arbitrary. The physical connections are shown in (a) with a circuit representation shown in (b). This construction can also be used as a balun, but may suffer from saturation of the ferrite if a sufficiently large core is not used.

The exact positioning of and construction of the TLT devices will alter impedance of the circuit. Additionally, there is some manufacturing variability in PCB itself that can lead to the need for tuning the input matching. This may lead to some adjustments to the exact values of the capacitors in the matching network, and

trimming with the variable capacitor. Capacitors C_2 and C_4 are especially sensitive to position and manufacturing tolerances, and their value may need to be adjusted on each amplifier.

4.2.6 LOI Biasing

The gate bias of the LOI amplifiers is set in the same basic manner as with the current source amplifiers (see section 4.1.3.3 for more details). The network itself is somewhat altered and improved, as stability of the amplifier was found to be difficult to achieve. One additional RC components were added to damp the RF on the bias line, as well as a series inductor to decouple the input. All of the capacitors must be good quality devices, with a dielectric of at least X7R and NP0 or C0G preferred. Lower quality dielectrics do not perform well at RF frequencies and will reduce the efficacy of the circuit.

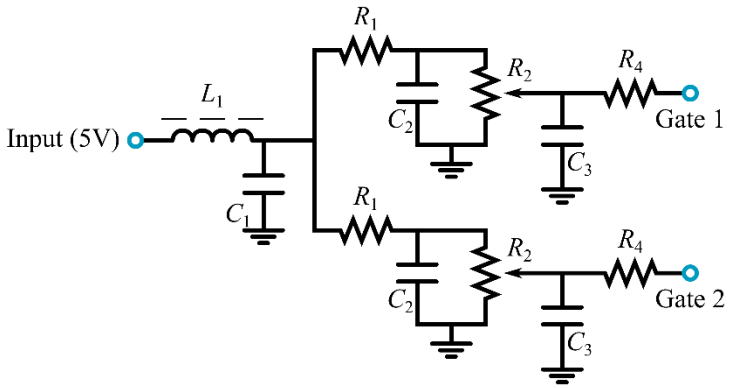


Figure 4.19: The gate bias network used for the LOI amplifier. L_1 is a decoupling inductor built from this (#32AWG) magnet wire wrapped 10 times around three 1/8inch ferrite cores. This was added to counteract instability seen in the amplifiers during high power operation. The shunt capacitors are X7R or better bypassing capacitors. The series resistors are used to damp the RF entering the bias line. The actual bias voltage is adjusted with R_2 and is set for each device independently.

The drain bias line has man of the same requirements as that of the current source amplifier. In this case, more care needs to be taken due to the higher RF powers involved. Both bypassing capacitors and decoupling inductors are used in order to adequately suppress the RF power on the DC line, as shown in Figure 4.20. Inductor L_1 is hand wound magnet wire on a 3/8inch non-magnetic core with 20 turns. This device should be close to self resonance, but should still appear inductive. The near self resonance increases the impedance of the inductor to the RF. The shunt capacitors are high quality ceramic devices, at a small an large value. This is followed by a second inductor that is only a single turn around a ferrite core. This is bypassed with a small resistor, which helps to suppress any resonance at subharmonic frequencies. A second pair of shunt capacitors is included, one is a ceramic capacitor of high value to reduce the remaining high frequency content. The second is a large electrolytic capacitor that substantially reduces the low frequency harmonics. This is necessary to prevent sub-harmonic oscillations around 10-12MHz.

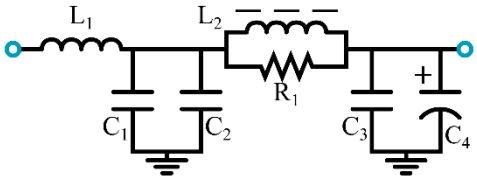


Figure 4.20: The bypassing and isolation circuit used for the LOI amplifiers. The first inductor is wound to be near self resonance at 128MHz. Two ceramic bypassing capacitors are then placed, followed by a single turn of wire around a large ferrite core. This is paralleled with a small resistance to suppress any resonance that might occur in it. Finally, another pair of bypassing capacitors. The polarized capacitor is a 1000uF electrolytic capacitor that reduces the propensity for sub-harmonic oscillations.

4.2.7 PIN Diode Bias Network

The amplifier has a built in network for biasing the PIN diode in the T/R switch. The network connects directly to the output of the power amplifier, so high isolation is needed to prevent RF from leaking back into PIN diode driver lines and circuits. The first step to produce this isolation is to use a tuned tank built from a high power, high quality ATC series C capacitor and a hand wound inductor mounted over this. The inductor is deformed until the tank resonates, and high impedances (between 5kΩ and 10kΩ) can be achieved. A $\lambda/4$ coax cable is used to connect this tank to the input connector to the amplifier. The connector has a built in bypassing capacitor (high valued shunt capacitor) which looks like a short to RF. This short is transformed to an open at the far end of the cable, thereby increasing the rejection of RF onto the line. This circuit is shown in Figure 4.21Inadequate isolation on the bias connections will lead to an unstable amplifier, and possibly damaging equipment, so this cannot be ignored.

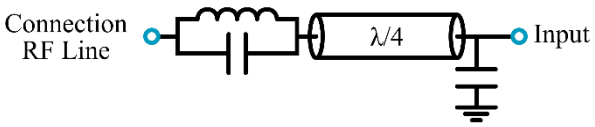


Figure 4.21: Bias line connection in amplifier. The inductor and capacitor resonate at the center frequency of the system, and shunt capacitor should be an RF short.

4.2.8 LOI Amplifier Output Tuning

The computed values for the matching network will be close to what is needed, but manufacturing tolerances mean that tuning the amplifier will result in better performance. Additionally, there will be some amount of parasitics and phase delay due to the circuit board that needs to be compensated for. There are too many degrees of freedom in the network to simply vary the values of all components, so a systematic method of measuring and tuning the amplifier is needed. Establishing a tuning method first requires a detailed understanding of the circuit.

4.2.8.1 Tuning Method Overview

The output matching network in Figure 4.14 has the matching network previously designed, as well as a balun and a section of transmission line. The balun then converts the 25Ω balanced impedance to 50Ω unbalanced, while the transmission line is microstrip on the board and an output connector. This delay line is not needed from a matching network perspective, but is needed to allow for physical connections. The phase delay it introduces must also be accounted for when tuning the network. Tuning will involve measuring the phase delay, adjusting the Tee network to have a minimum impedance, and finally connecting the amplifier to a test coil and setting L_1 to maximize isolation. The series capacitors need to be the same value, so would be difficult to tune. The tuning process is greatly simplified and still achieves good results when limiting tuning to the shunt elements.

4.2.8.2 Tuning Process

With this basic strategy in mind, the first step is to measure the delay of the microstrip and output connector because any phase delay will affect the measured values of later components and propagate error into the tuning procedure. This is done by taking a S_{11} measurement in the form of $|\Gamma|-\theta$ looking into the board with the balun detached from the microstrip. This will vary depending on the exact board layout and construction, so will need to be measured during fabrication, for our example board the phase delay was found to be 23°.

Next, the Tee network is installed. The calculated value of the shunt inductor is 31nH, however a tunable inductor of approximately that value should be used. The balun should also be fully connected at this point. The S_{11} is repeated and L adjusted to obtain a $|\Gamma|-\theta$ that corresponds to a short circuit phase shifted by the previously measured amount (in our case $|\Gamma|=0.995$ and $\theta=157°$). The Tee network should be fully tuned at this point, so the MOSFET and L_1 can be populated. L_1 is also a tunable inductor that will be adjusted in the next step.

L_1 should be adjusted to resonate with C_{os} , but direct measurements of the output of the amplifier are difficult to make safely, so an indirect technique is used. The isolation provided by the amplifier is a good indicator of whether or not L_1 is correctly tuned because the Tee-network is tuned. This measurement involves connecting the amplifier to a tuned coil with electrical length between the matching network and the coil of $n\lambda/2$. This is achieved by using a cable that is $n\lambda/2$ shortened to compensate for the electrical length on the amplifier board. The isolation measurement is made as a $|S_{21}|$ measurement through a pair of decoupled pickup loops are then position near the coil. The amplifier drain is biased and L_1 is adjusted until maximum decoupling (minimum $|S_{21}|$)is seen. This is indicated by a “dog-ear” in the $|S_{21}|$ curve at the frequency of interest, as shown in Figure 4.22.

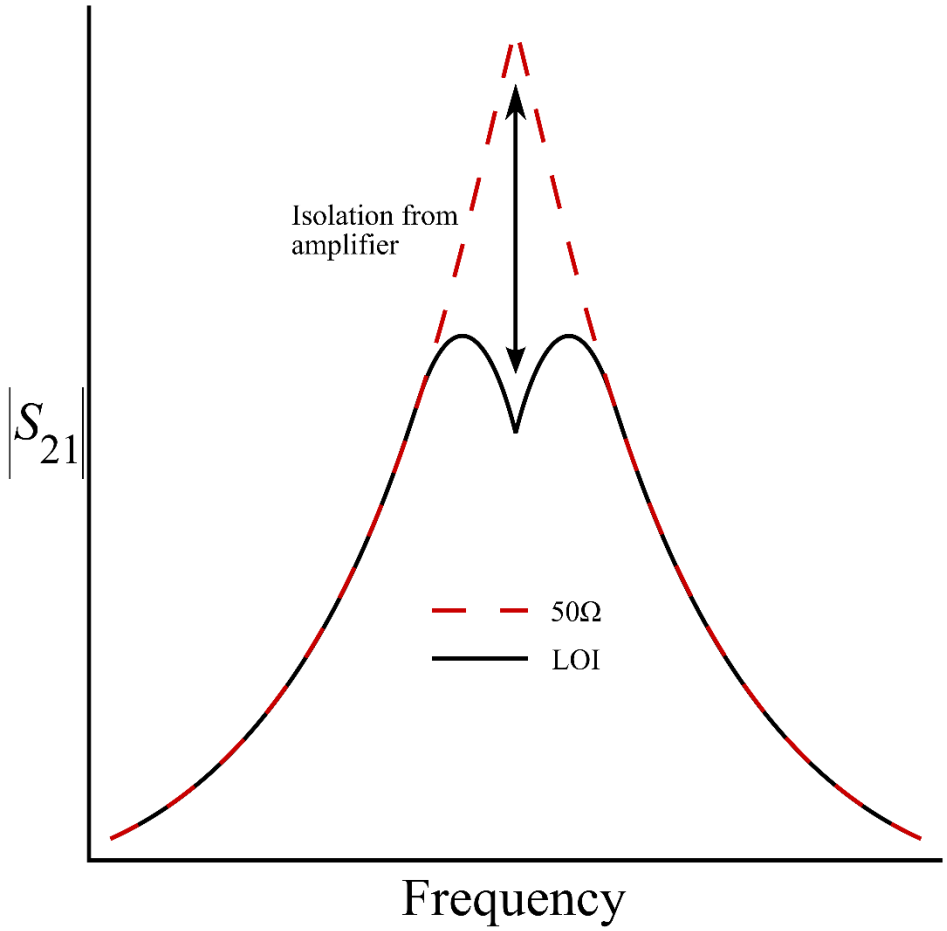


Figure 4.22: Isolation is maximized by minimizing $|S_{21}|$. This appears as a dip, or "dog-ear", in the $|S_{21}|$ when the isolating amplifier attached. The difference between the $|S_{21}|$ with the amplifier and a 50Ω termination is the isolation the amplifier provides.

The matching network should be fully tuned after this process, which can be validated with bench measurements. The power output, gain, and isolation can and should be measured.

4.3 Testing and Comparison of Amplifier Architectures

Evaluation of the amplifiers is equally important as understanding their operation. By both measuring the performance in test fixtures and imaging we can better understand their relative merits. An understanding of the test fixtures is important prior to discussing the actual results.

4.3.1 Amplifier Measurement

The primary (but by no means only) validation of the LOI involves measuring the power delivered to the load, and the isolation provided by the amplifier. Conceptually, both of the measurements are fairly straight forward. Accurate results require some care and knowledge of the measurement systems to be used.

4.3.1.1 Isolation Measurement Technique

Directly measuring the isolation provided by an amplifier is difficult, so instead we measure it as $|S_{21}|$ between two pickup loops positioned over a tuned coil. Two measurements are needed in order to extract decoupling: 1st is when the coil is connected to the amp, 2nd with the coil connected to a 50Ω termination. The coil must be correctly tuned for an LOI amplifier, and should be connected as it would be in normal operation.

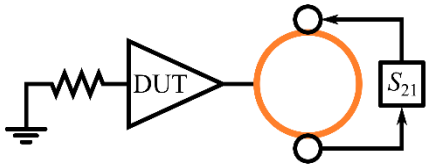


Figure 4.23: The basic measurement setup of isolation. It involves a $|S_{21}|$ measure through isolated pickup loops placed near the coil.

The amplifier is also setup for normal operation, but the input is terminated in 50Ω and the gate bias line grounded to prevent any possibility of high power being transmitted. Two separate pickup loops are positioned near the coil so that they are isolated from each other, and are connected to the network analyzer for the $|S_{21}|$ measurement. For the second measurement the amplifier is replaced with a 50Ω, but everything else remains the same. It is important that the pickup loops not be moved between these two measurements, or the results are invalid. The difference between these two values (in dB) is the amount of decoupling provided by the amplifier.

4.3.1.2 Power Measurement Technique

For the standard amplifier and Low output impedance amplifier it is relatively straightforward to measure the power delivered to the load. And thru-line power meter can be used, with a tuned coil acting as the load. It is important to allow the pulses to run repeatedly since they are pulse amps and this can skew the measured power low. Measuring the output of the current source amplifier requires a calibrated pickup loop. A basic calibration can be accomplished by positioning the pickup loop over a coil that is excited by a standard amplifier. The pickup loop reading can be taken with an oscilloscope, while power measurements are made with a thru-line power meter, as in Figure 4.24. A lookup table is made by taking measurements at a number of different power levels. The pickup loop and calibration table can then be used for power measurements

of the current source amplifier. This requires that the calibration fixture and the test fixture be as close to identical as possible.

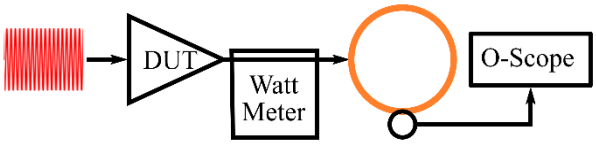


Figure 4.24: The amplifier power measurement using a watt meter and o-scope. For the standard and LOI amplifiers the thru line watt meter will provide accurate results. For the current source amplifier a calibrated pickup loop is needed. Basic calibration can be accomplished at using this setup to generate a lookup table. Care must be take in the location of the pickup loop to achieve accurate results.

4.3.2 Amplifier Performance Comparison

The standard and low output impedance power amplifiers, which are power matched, were capable of delivering significantly more power to the coil than the current source amplifier. Across multiple devices and measurements the power from the standard and LOI amps was consistently between 950W and 1050W. There was some variation in performance and measurements, but this is expected. While slightly higher powers are possible, they are not recommended due to device non-linearity and increased power dissipation in the device. The current source architecture performed consistent with the expectations, measuring at roughly 10A on the coil. Similarly, the current source was able to produce the highest amount of decoupling, followed by the low output impedance amplifier. The standard amplifier (when used with an isolator) produced 0dB of isolation, as per how we defined the measurement.

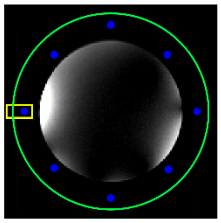
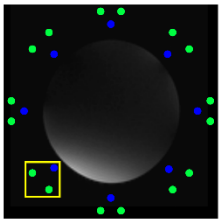
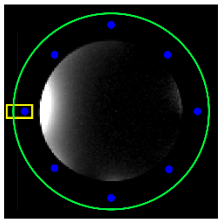
	Standard Amp	**CS Amp**	**LOI Amp**
Max Power	1kW (device Rating)	150W (device current rating)	1kW (device Rating)
Isolation	0dB	30+dB	14+dB
Single Channel Excitation			

Figure 4.25: Basic performance of the different types of amplifiers. The isolation of the standard amplifier is defined as zero as, as it is the reference point. The power output of the current source is limited by the device current rating, and is ultimately a product of this and the coil impedance. Each image is overlaid with a basic display of the coil used. Blue is the current path of the imaging element, and green is the return/shield path. The active element is boxed in yellow.

4.3.3 LOI Amplifier Imaging Tests

The amplifiers were used in a multi-channel transmit system as well to observe the real world effects they have. One of the most visible effects of couple is the transmit pattern of an element becoming less localized. To see an example we used an eight channel, partially decoupled rung array constructed for use with LOI amplifiers.[57] A single channel of the coil was excited and all other channels were connected to in one of two ways: first, they were connected to 50Ω terminators to simulate the use of isolators; second they were connected to LOI amplifiers with no other changes made. Images were taken under both conditions show that the LOI amplifiers help suppress the effects of coupling, especially in the region near the elements that are opposite the excited element. A similar experiment was done using the current source amplifiers. In this case a different coil structure was used because of the vastly different performance of the amplifiers. What we see is that it is fairly easy to eliminate coupling between the nearest neighbor elements (which is typically the strongest coupling). For elements that are more removed, this is less practical, so the isolating amplifiers are useful in mitigating coupling between the other pairs of elements.

As a basic demonstration of the isolating amplifiers we also used a B_1 shimming technique to synthesize a more uniform excitation. Each of the eight channels of a transmit system using the low output impedance amplifiers was used, with a set of complex weights adjusting the phase and magnitude between channels. The isolated and stable channels allow the signals to combine in a simple, linear fashion and synthesize a nearly uniform excitation seen in Figure 4.26.

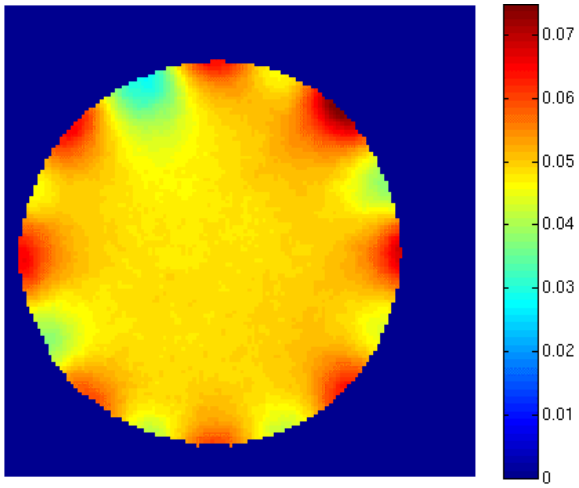


Figure 4.26: The eight transmit channels were combined using B_1 shimming. This generates a synthetic birdcage mode so a uniform excitation is obtained. Nonlinear behavior, temporal instability, or even significant coupling between channels would have degraded the quality of the excitation.

4.4 Discussion

Power amplifiers are one of the major units in the transmit subsystem for NMR and MRI systems. The basic designs and classes of operation have been able to benefit from work done for communications systems and the development of newer solid state components. The improvements in MOSFET technology has allowed the exploration of higher efficiency and more specialized amplifier designs. Much of these improvements have manifested in different biasing points and new matching networks.

Experience with parallel receive systems has shown the value in multi-channel systems. This is beginning to be translated to transmit systems as well. We have also seen that being able to decouple an array coil using the attached amplifier is a useful technique. This helps to mitigate the effects of mutual coupling in arrays.

The standard power amplifier, current source amplifier, and low output impedance amplifier have markedly different strengths and weaknesses in terms of performance. Consideration of these characteristics makes it possible to better asses which architecture is best suited for a particular application, as well as being to understand possible avenues for improvement.

We have focused on linear class amplifiers, but there is on-going work with Current mode class-D (CMCD) amplifiers that may be able to increase the power output as compared to linear current source amplifiers, but this comes at the cost of significantly higher complexity.[58], [59] There may also be applications for techniques like feedback in both linearization and effectively decoupling arrays.[25], [60]

Current source amplifiers allow for intrinsic isolation of the array by using a single current path and having a very high impedance presented to induced power. This is very effective in limiting the coupling between elements, but reduces the power generated by the amplifier.

Low output impedance amplifiers are something of a compromise. They are narrow band and can only achieve around 1kW to 2kW peak power, but they also provide around 14dB of isolation. This makes them useful in situations where neither the standard power amplifier, nor the current source excel.

The designs also all used a commercially available MOSFET device that was designed for use in standard power amplifiers. It is reasonable to believe that effort is put into adapting the MOSFET designs to be best suited to isolating amplifiers would yield improved performance. Finally, these designs could be considered "first generation" amplifier designs. The current source and low output impedance amplifier designs are based on relatively simple models of the active device. Performance gains could be expected if a more complete model were used, at the cost of more complicated design procedure.

4.4.1 Selection of Amplifier Architecture

The architectures discussed above each have different benefits. At this time, there is no single clear choice that is best for all situations. Instead, the different amplifiers might be considered for different applications. The selection between architectures is summarized in Figure 4.27.

Standard power amplifiers are still the best option when broad band or very high powers are needed. This tends to be the operating mode of NMR systems and one or two channel MRI systems. The standard amplifier becomes less desirable as the channel count goes up relative to the imaging volume.

Current source amplifiers are limited in the amount of power they can produce to a few hundred watts, but can isolate an array to -30dB or better. This makes them useful for arrays with a large number of channels as compared to the volume of interest (e.g. a 32-channel head array). These arrays will tend to have high intrinsic coupling between elements that is hard to compensate for in other ways, and each individual channel will not require large amounts of power.

The low output impedance amplifiers can obtain powers at the kilowatt level (the rating of the device used), but also provides up to 14dB of isolation for the array. This makes the LOI amp well suited to cases where a moderate number of channels is needed for a given volume (e.g. an eight channel head array). Higher density arrays will tend to have higher coupling between elements that the LOI cannot adequately compensate for, as well as lower power requirements. At the other end, low channel count arrays may require higher power levels than can be obtained from a small number of LOI amplifiers and inter-element coupling is less of a problem.

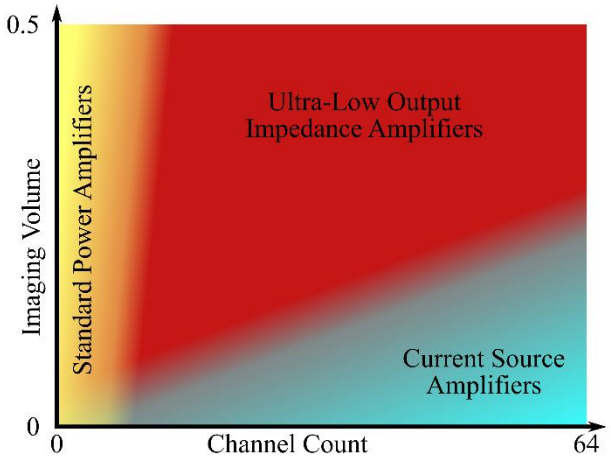


Figure 4.27: The amplifier architectures examined have different strengths and weaknesses. This makes them practical in different scenarios. Generally, in very low channel count situations a standard amplifier is a good choice. When the number of channels vs. imaging volume is low (e.g. an eight channel whole head array) then low output impedance amplifiers are a good choice. Current source amplifiers are well suited to situations where there are a large number of channels in a small region.

CHAPTER 5
PARALLEL TRANSMIT SYSTEM

5.1 System Overview

The parallel transmit system provides eight, independently modulated channels. Each channel can produce at least 300W peak output power into a coil. At the same, the power amplifiers provide moderate decoupling, simplifying the design of the array coil. The modulators can control both amplitude and phase dynamically, so full fast modulation is possible.

5.2 System Architecture

The transmit system is made of four main subsystem: the modulators, the power amplifiers, the coil, and the control system. The high level connections are shown in Figure 5.1.

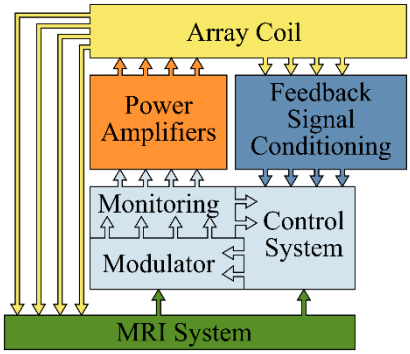


Figure 5.1: The major system subdivisions in block diagram form. These are: the modulators, power amplifiers, and the array coil. In addition, there is a feedback system for monitoring the performance. Further, the modulators are built of a set of subsystems.

The modulators and power amplifiers have been previously discussed in Chapter 3 and Chapter 4. The control system and coil were primarily the work of Katie Moody[61]. A brief description of each, with a focus on the system level aspects will follow.

5.2.1 Modulators

The vector modulators have been designed to simplify interfacing with an existing MR system. It is a homodyne modulation system with the input waveforms supplied at baseband as an I/Q pair for each channel. This makes full modulation possible, while bulk phase shifts, phase locking, and frequency setting can be managed by a single high stability RF source (e.g. the frequency synthesizer in a MRI system). The modulation waveforms can be low frequency, less than 200kHz analog signals. Additionally, the modulators are capable of B_1 shimming in a straight forward manner since the modulation waveforms may be true DC.

Digital control signals can set the attenuation, output blanking, and offset nulling voltages for each channel as shown in Figure 5.2.

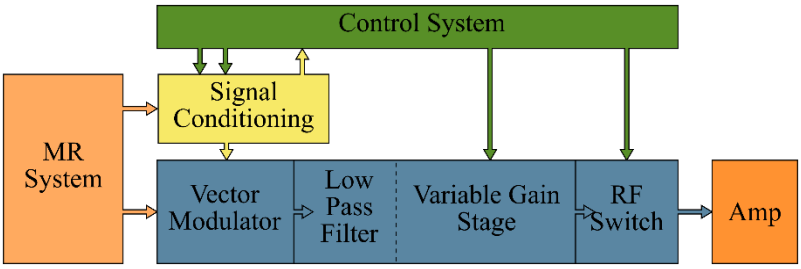


Figure 5.2: Modulator block diagram showing major functional elements and connections.

5.2.2 Amplifiers

The amplifier chain is a multi-stage system that takes the low power output of the modulators and increases it to at least 300W peak output. Additionally, the amplifiers add roughly 12dB of isolation to the coil. The LOI amplifiers that make the final stage also have integrated PIN diode drivers to control the T/R switches. There is additional blanking between the medium power stage and the final stage to minimize leaked noise. Figure 5.3 shows the overall functional structure and connections of the amplifier chain. The amplifiers have been designed to operate in a pulsed mode, with duty cycles of under 10% and maximum on times under 100mSec.

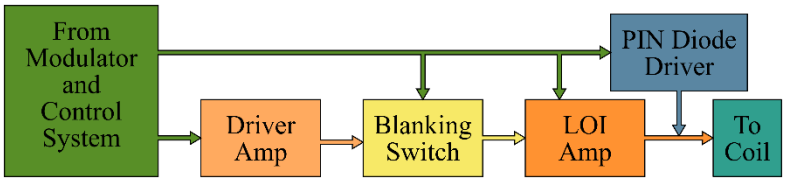


Figure 5.3: The amplifier chain's major blocks and connections.

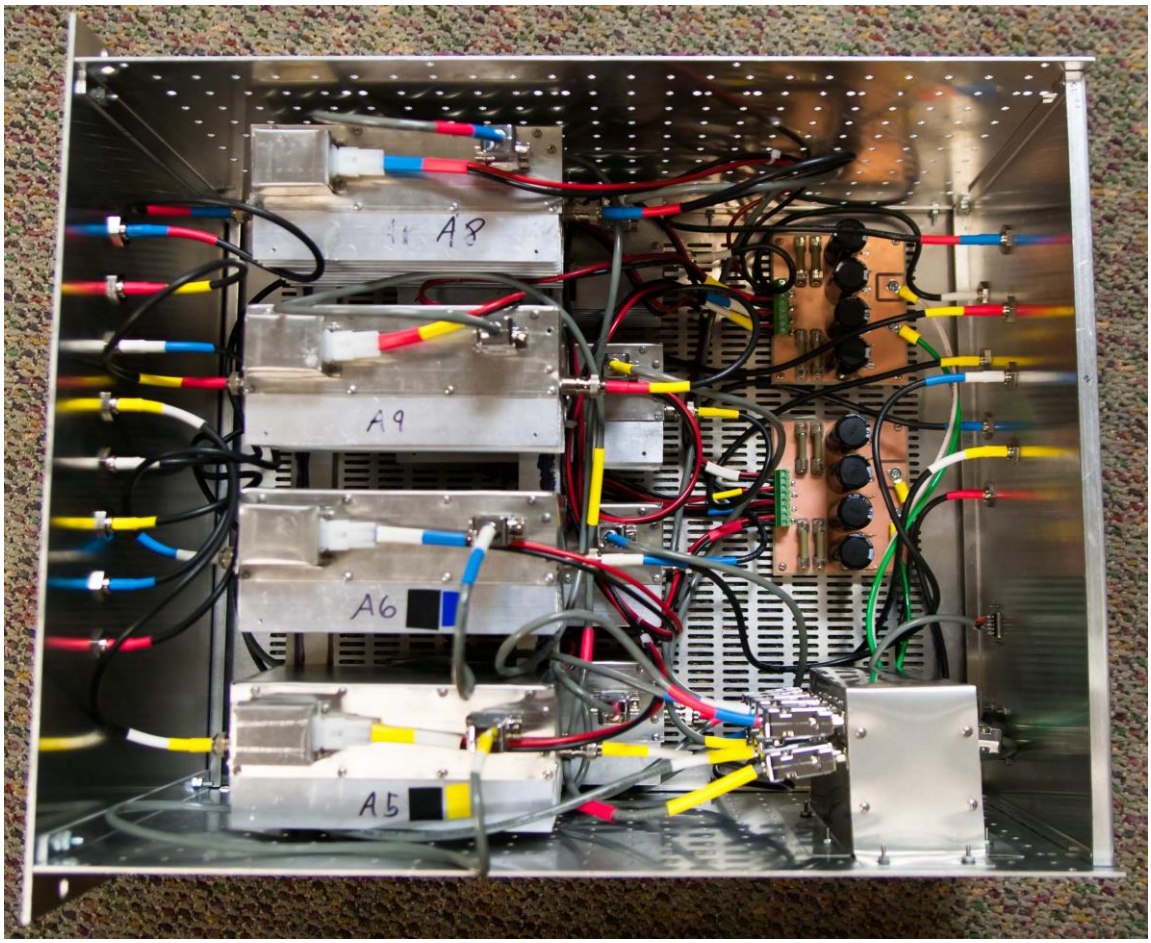


Figure 5.4: Rack unit with eight LOI amplifier modules. Inputs are on the right, outputs on the left. Module on the lower right contains the PIN diode drivers and gate biasing circuits. Copper boards are the 150V power distribution boards.

5.2.3 Control System

The control system was developed by Katie Moody, based on National Instruments hardware and programmed in the Labview environment. The primary functions of this subsystem are to produce the analog modulation waveforms and the digital control signals shown in Figure 5.5. The control system is configured to support up to eight transmit channels, with multi-slice, linearization, and some feedback based safety interlocks. The waveforms are generated at ±10V, 16 bits, and locked to a 40MHz backplane clock in the NI chassis.

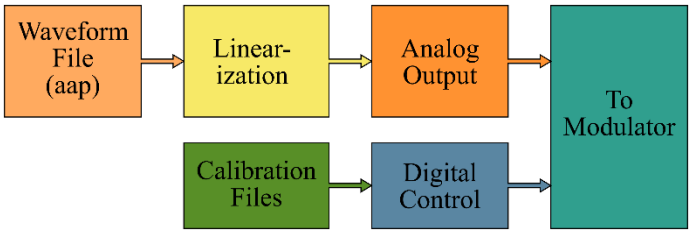


Figure 5.5: Basic functions of the control system.

5.2.4 Array Coil

The primary coil for use with this system is a fully shielded eight channel head array with rung elements[57]. It has integrated TR switched and low input impedance preamplifiers so that it can operate as a transmit/receive coil, as shown in Figure 5.6. Capacitive decoupling of nearest neighbor elements is used to supplement the isolation obtained from the amplifiers. Again, this is the work of Katie Moody.

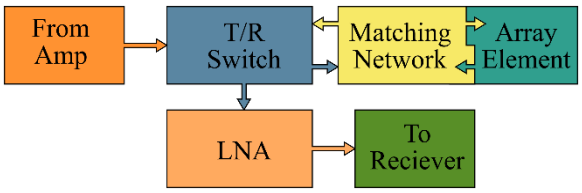


Figure 5.6: The major sub-units of the array coil.

5.3 Installation with a 3T GE MRI Scanner

The parallel transmitter was installed at the University of Michigan, Ann Arbor on two separate scanners. In both cases they were 3T whole body MRI systems from General Electric. Integration required that the parallel transmitter could be disconnected and removed from the magnet room completely, with the system returned to stock configuration. This must be done at the end of any set of parallel transmit experiments so that the system could be used for volunteer studies.

5.3.1 Location of Major Components

The modulators, control system, power supplies, and driver amplifiers are located in the equipment room of the MR suite. This is for a few reasons: first, most of those units have components that are sensitive to magnetic fields, so would not function in the magnet room proper. Second, this minimized the amount of equipment that would need to be located in the magnet room (and potentially moved on a regular basis.) Third is the availability of high power AC connections for the DC power supplies, which are not generally available in either the control room or the magnet room. Finally, the needed connections from the MR system are located on units in the equipment room.

The power amplifiers are located in the magnet room near the rear of the magnet. This minimizes the cable runs for high power RF and the losses associated with it. It does mean that a number of feedthroughs into the magnet room must be available. These include the RF feedthrough for each channel, a D-Sub filtered feedthrough for the low voltage/low power supplies and the digital control lines, and finally a pair of high voltage/high power filtered feedthroughs for the amplifier supplies.

5.3.2 Connections to the MR System

Two signals are needed from the scanner: a digital trigger/transmit window and the on-resonance RF pulse. The RF line is taken from the system directly before the main power amplifier (with the input to amplifier being terminated in 50Ω). The digital trigger used is the transmit gate signal. The choice of trigger signal is somewhat system dependent, as a programmable line or some other line may be used. The transmit gate signal is a reasonable choice in most cases, as it will typically transition states at the beginning and end of the RF transmit window.

5.3.3 Software/Sequence Modifications

The primary modification needed is to the RF transmit pulse. The parallel transmitter expects an RF hard pulse at the excitation desired frequency with an amplitude of approximately -30dBm. It is best to hard-code this configuration into the pulse sequence when possible, but the GE systems generally require that amplitudes are checked in a number of control panels.

5.4 Parallel Transmitter on 4.7T Varian System

Four channel transmit experiments were also done on the 4.7T, 40cm Varian system in the MRSL. A detailed operation manual is located in Appendix A that covers the connections and software setup for this experiment. Again, the isolating amplifiers were built for use at 128MHz, so a set of 100W, 100MHz amplifiers were used that are part of the 64 channel T/R SEA system[19], [62], [63].

5.5 Parallel Transmitter on 7T Phillips System

Some additional testing was done using on a 7T Phillips scanner at the University of Texas, Southwestern. The full system was not used, as the transmit amplifiers were not designed for operation at 300MHz. Instead, the modulators and control system were used with the scanners power amplifiers and a two channel coil.

5.6 Imaging with the Parallel Transmitter

Imaging experiments to test the parallel transmit system were performed at three different sites and field strengths. The pulse design and sequences were primarily done by Jon-Fredrick Nielson at the U of M, and Will Grissom at Vanderbilt, working at UTSW AIRC and at the MRSL of Texas A&M.

5.6.1 B_1 Mapping

Mapping the excitation profile is necessary for any parallel transmit technique. This involves generating an excitation with each individual channel and extracting the amplitude (often in B_1) and phase. Many techniques have been devised for this, but the Bloch-Siegert B_1 mapping technique[64] has some significant advantages. One of the primary ones is that it performs well even if the excitation is highly non-uniform, and does not suffer from significant signal loss in low tip regions. An example of the magnitude B_1 maps is shown in Figure 5.7 for the eight channel head array used at 3T.

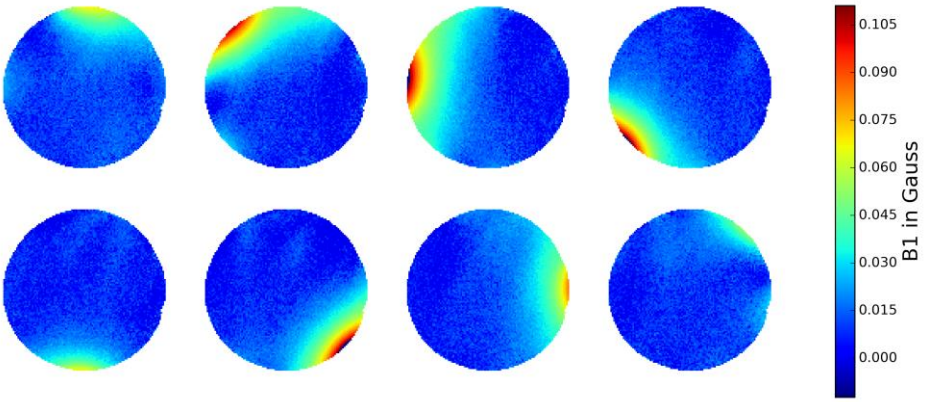


Figure 5.7: B_1 maps of the eight channel transmit system at 3T.

The B_1 maps are clearly no uniform, in that no individual coil is capable of exciting the complete phantom. This is expected, and is not considered a problem. The excitations are also generally localized over their respective coils, which is an indicator that there is not significant coupling between elements. The reduced coupling is valuable for both B_1 shimming, and controlling SAR in Transmit SENSE excitations.

5.6.2 Uniform Excitations at 3T

One of the simplest examples of parallel transmit is to synthesize a uniform excitation from a non-uniform set of coils. A demonstration of what this can achieve is shown in Figure 5.8, which was generated from the array with the B_1 maps shown in Figure 5.7. This shows a marked improvement in the uniformity, and the ability to achieve substantial excitation in the center of the imaging volume.

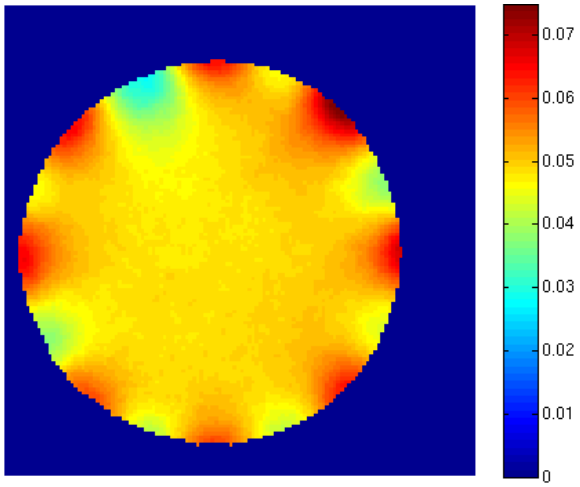


Figure 5.8: Synthetic birdcage generated from the eight channel array.

This excitation is essentially a B_1 shimming experiment. Each channel transmitted a sinc pulse, but was phased and amplitude shifted to emulate a birdcage. The results match what would be expected with a birdcage, including the high signal regions near the elements. Some error is seen as low signal areas between elements (especially left of the top element). This is likely a fundamental limitation of the B_1 shimming technique. Because the patterns from each element are not precisely like that of a birdcage, a perfect birdcage mode cannot be produced. A more refined coil and weighting scheme may improve the performance, but this clearly demonstrates the benefits of B_1 shimming.

5.6.3 Parallel Excitation at 4.7T

A four channel excitation system was configured for use with the 4.7T Varian MR scanner in the MRSL. The target excitation was a uniform square inside of a cylindrical phantom filled with distilled water. An accelerated excitation was generated utilizing the Shiner-La Roux[65]–[67] design process. A unipolar EPI excitation was used to avoid *k*-space location inaccuracies due to mistuning of system parameters. Simulated and experimental data is shown in Figure 5.9

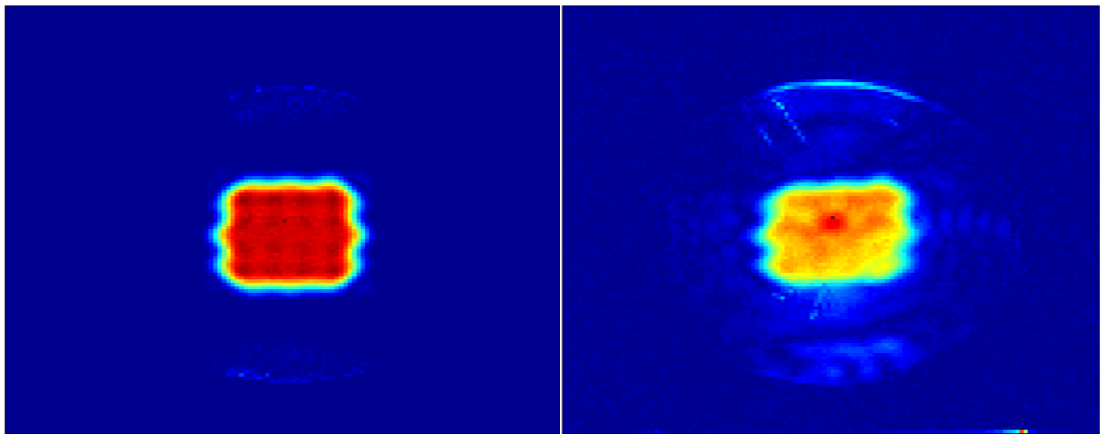


Figure 5.9: The predicted (left) and the measured (right) excitation. The excitation was generated using a four channel coil, with acceleration factor of 2. The desired excitation as a uniform square inside of a cylindrical phantom.

This experiment is an excellent demonstration of both the suitability of the modulator system, and the difficulties of parallel transmit. The system was able to generate an accelerated RF pulse that excites the desired pattern. Further improvement of the excitation would rely on refining both transmit system, and the calibrations of the gradients. The EPI excitation used has not yet been well calibrated on our system, so may be suffering from errors in the gradient waveforms or other problems.

5.6.4 Parallel Excitation at 7T

The experiments done at 7T were preliminary work to validate that the modulators could function at those frequencies and we could install the transmit hardware on the Phillips system. The coil used was a commercial quadrature birdcage coil for the human head(Nova Medical, Inc. Wilmington, MA) and the phantom was a spherical homogenous test unit. The pulse sequence was intended to generate a uniform excitation. A spokes excitation pulse[68] was used to synthesize the uniform excitation, and the coil was operated in three different modes. The first was a simple circularly polarized (CP) mode, in which the two channels were fed the same waveform with equal magnitude and 90° phase shift. The second was the Phillips multi transmit method, which is similar to CP but does not have the fixed phase/amplitude relationship. Finally, a fully parallel excitation was done using the vector modulator system. A set of data was taken using varying numbers of spokes in the *k*-space trajectory and mapping the tip angles generated, shown in Figure 5.10.

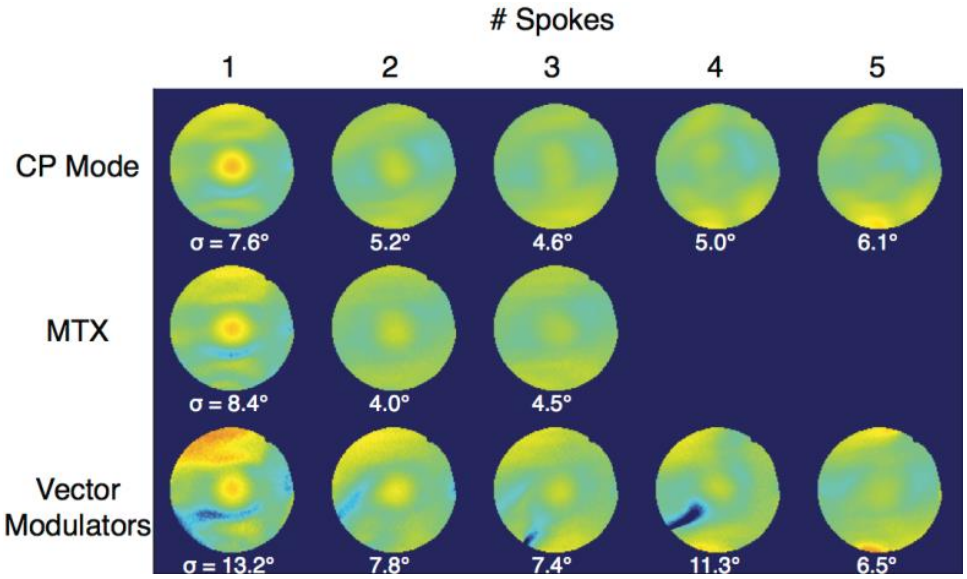


Figure 5.10: The tip-angle maps of 7T spokes excitations. The first row used the transmit in circularly polarized mode. The second row was the Phillips MulTx system (B_1 shimming). The third row used the vector modulators to generate independent waveforms on each channel.

Generally, the uniformity of the excitation increased with higher numbers of spokes, as expected. At high spokes counts the quality decreased, which seems to be an over fitting problem. One oddity is the signal null that appears when using the vector modulators with a four spoke excitation. It is unclear why this occurred, but it was not a transient effect. These results are only preliminary, and represent a minimal investment of personnel time and equipment time. Improvements to the performance should easily be possible with more effort.

5.7 Discussion

A parallel transmit system has been constructed and installed at the University of Michigan, Ann Arbor. This included an eight channel modulation system and isolation power amplifiers, along with a control system and head coil. The amplifiers can produce up to 300+W to the array coil, and generate a substantial B_1. A basic B_1 shimming technique was able to synthesize a birdcage, confirming that B_1 in the center of the imaging region on the order of 0.05 Gauss is obtainable.

Further testing of the modulators and control system was done at 4.7T and 7T as preliminary work. This demonstrates the flexibility of the control and modulation unit, as well as showing some more advanced capabilities of the system. The work at 7T was an unfunded, exploratory experiment, and so did not produce high quality results. Further effort would be needed in terms of calibrating the parallel transmitter at 7T, confirming the pulse sequence and design, and general debugging. Additionally, a higher channel system would potentially improve the results.

At 4.7T the results are of good quality. Standard power amplifiers were used with a geometrically and capacitively decoupled loop array and accelerated excitations were achieved. Additional work to increase the channel count, and potentially construct isolating power amplifiers would improve the capabilities of the system. Further tuning and adjustment of the MR systems gradient amplifiers and eddy current compensation may also prove beneficial. Introducing a *k*-space trajectory mapping[69] step to the sequence design may indicate if the gradients are introducing error, and potentially provide a way to reduce that error.

CHAPTER 6
CONCLUSIONS

An eight channel parallel transmit was constructed using vector modulators and low output impedance amplifiers. The modular nature of the system made it possible to also run experiments using standard and current source amplifiers. Integration with multiple commercial MR systems was possible, and straight forward, because of the minimal number of connections needed (only a single RF line and a single digital trigger are needed from the MR system).

The vector modulators proved to be capable of complex excitation pulses. They were demonstrated at 3T, 4.7T, and 7T. Linearization to correct for imbalances in I/Q proved to be necessary, and problematic at lower frequencies. This should not be a fundamental limitation, but there appears to be some implementation problem. Contact with Linear Technologies has not resolved the issue yet.

Multiple amplifier architectures were constructed and tested. The standard amplifiers acted as a baseline, with the performance of the current source and low output impedance amplifiers measured relative to it. The current source amplifiers proved to be highly capable of decoupling the array coil. It was even possible to use an eight element loop array with no additional decoupling. The nature of the matching network did, however, make it difficult to use the coil for transmit/receive which produced some limitations. A transmit only/receive only pair of coils is one method of circumventing this problem. The current source amplifiers are fundamentally limited in the amount of current they could transmit to the coil. This limited the effective B_1 they could produce.

The low output impedance amplifiers were able to produce some isolation, though substantially less than the current source amplifiers. This made a partially decoupled rung array possible. Further, the matching network is identical to that needed for low input impedance preamplifiers. This made it trivial to use the array as a transmit/receive array. The low output impedance amplifiers were also able to produce high levels of output power. They matched the standard amplifier for output levels when considered in the narrow band case.

This system can be seen as nearly first generation technology, so many improvements could be expected. The nonlinearities of the vector modulators should be resolvable, making them practical for use at all current MRI field strengths. The control system could be more highly integrated, reducing cost and size so that high channel count systems are possible. It may also be possible to implement feedback into the control system, or amplifiers, in order to obtain better linearity and better isolation.

The amplifiers were built around a commercially available LDMOS device that has not be optimized for isolating amplifier designs. It may be possible to adjust the fabrication of the device to achieve a higher Q trap across the drain, improving isolation. A higher current/lower voltage FET would be better suited for

the current source design, or perhaps a matched pair to increase current handling. Both amplifier designs are based on a simple model of the MOSFET. A better model of the FET may allow for improved performance by taking into account additional parasitics and feedback. Moving the amplifiers onto the coil should produce improved results, but there are some difficulties in this approach. Thermal control, high currents and voltages, and the need for nonmagnetic and non-ferrite parts substantially increase the difficulty of the design.

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APPENDIX A
PARALLEL TRANSMIT ON THE 40CM VARIAN

A-1 Overview

The Varian system will supply the RF hard pulse, and two trigger lines that control the coil tuning, amplifier blanking, and baseband waveform generation. A pair of PIN diode drivers are needed to tune/detune coils, and an RF switch is needed to route the hard pulse correctly. The basic system setup is shown in Figure A-1.

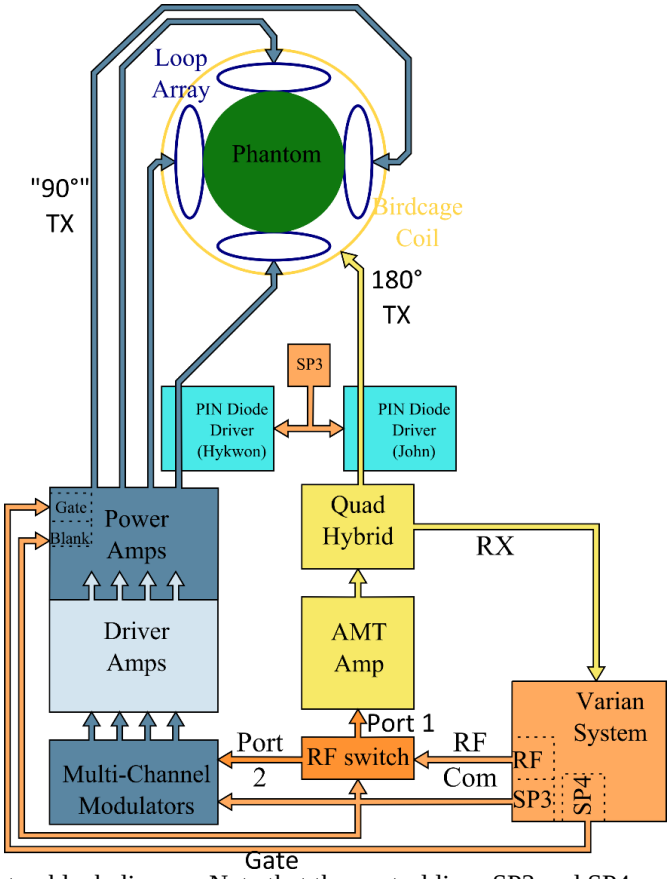


Figure A-1: System setup block diagram.Note that the control lines SP3 and SP4 need to be added to most pulse sequences.

A-1.1 Brief Order of Operations

● Control Line Connections

PIN Diode drivers connected to Spare 3

Modulator trigger port and $\overline{\text{unblank}}$ port connected to Spare 3.

RF switch connected to Spare 3

Amplifier Gate port connected to Spare 4

- RF Connections

  Varian RF connected to RF Common port on switch.

  AMT amplifier connected to Port 1 on RF switch

  Modulator RF in connected to port 2 on RF switch

  Output of modulators connected to input of 64-channel driver amplifiers

  Output of 100W amplifiers connected to transmit array

  Bias-Tee inline with coil 1 of transmit array

  PIN diode driver output connected to DC port of Bias-Tee

  Birdcage coil connected to the magnet leg through PIN diode driver and jumper cable

- B_1 Mapping

  Power on the Varian and pTx system

  Set the scaling factor for the pTx system

  Shim, you should be able to get a line-width below 20Hz

  Load the “Sgbs_multx” sequence on the Varaian

  Set gsp1=0, gsp2=2.9644, and tspulse =0.007312

  Obtain images with all the bs#.aap and bsconj#.aap RF files, saving the images as “bs_coil#_1” and “bs_coil#_2” respectively

  Load the “Sgpm_multx” sequence

  Obtain images with all the sinc_ch#.aap files, saving the images as “phs_coil#”

  Obtain a second image with sinc_ch#.aap, setting TE 1mSec longer, save as “phs_coil#_te7”

  Process with loadb1_bs_2

- Pulse Generation

  Configure the xsense_tamu_2 script

  run the script (need b1_bs.mat and other Matlab scripts)

  upload the gradient and RF waveform files

- Running a Multx sequence

  load the correct aap file on the ptx host sytem

  load the “Ssems_multx” sequence

  set gsp1, gsp2, and tspulse

  rename the gradient waveforms to blipwill.GRD and trapwill.GRD if needed

  Click scan, pray it works

A-2 Triggers and RF Connections

The parallel transmit system currently uses two digital triggers derived from the Varian. The first is the playback trigger. Spare 3 on the back of the Varian console is used for this purpose Currently, that signal is routed through the "Spare 1" port on the magnet leg (labeled "TX GATE" on the front of the magnet leg). It is then routed to both PIN diode drivers, the modulator trigger port, and the port on the 64-channel system (located on the back of the power supply/signal distribution box).

The RF cable is taken from the input to the AMT amplifier (after the power splitter/power detector) and connected to the RF common port on the switch. Then, RF port 1 is connected to the input to the AMT amplifier, and RF port 2 is routed to the input to the parallel transmit modulators. It is important that the modulators and amplifiers are connected in that order, failure to do so will result in the RF being routed to the incorrect subsystem during the pulse sequence. The RF switch is controlled by the Spare 3 digital signal, again taken from the opto-isolater port.

The RF out of the multi-channel modulators is routed through both stages of the 64-channel transmitter amplifiers. **The channel 3 power amplifier appears to be bad, so do not use this one.** The output of the modulator goes into the first stage amplifiers, which are cascaded with the second stage 100W power amps. These are then connected to the transmit array directly through the RF ports on the penetration panel. Note that the inputs and outputs of all the unused power amps in that bank are terminated in 50Ω.

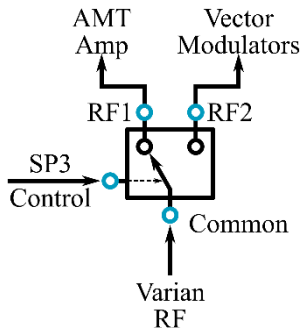


Figure A-2: Transmit RF connections routed through switch. The control is handled by the Spare digital line 3 from the Varian system. RF common on the switch is connected to the output of the Varian modulator (the input to the AMT amplifier). Port 1 of the switch is connected to the input of the AMT amplifier, and port two routes to the vector modulators.

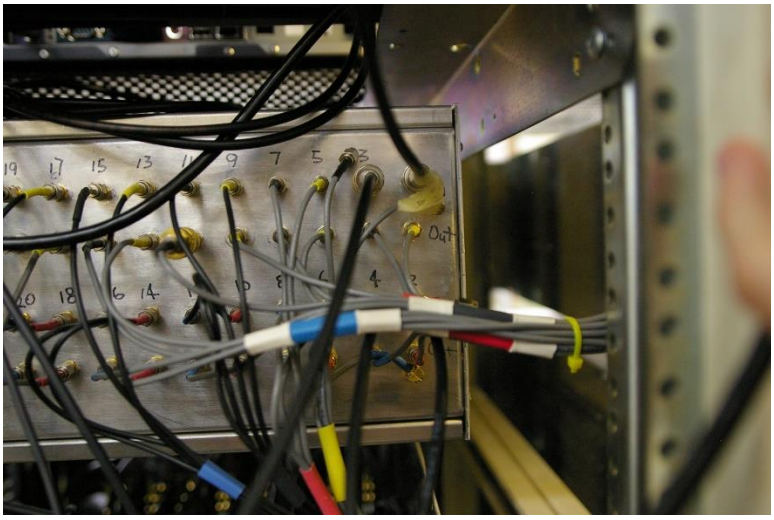


Figure A-3: The four outputs of the vector modulator are routed to the amplifiers. Note that the odd channels are the first two rows (inputs on top) even channels are the bottom two rows (inputs on 3rd row down).

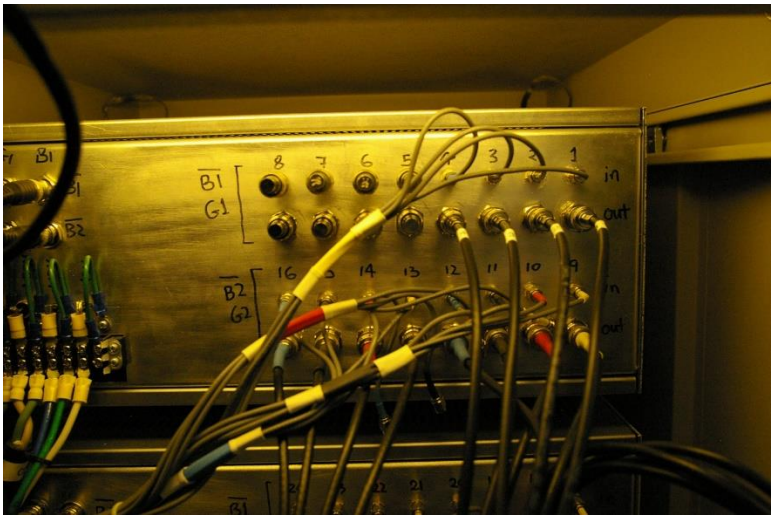


Figure A-4: The inputs and outputs to channels 5-8 are terminated in 50ohms.The outputs of channels 1-4 are routed to the transmit array coil.

A-3 Coils and PIN Diode Drivers

Two RF coils are used, the first is the four element loop transmit array, the second is the 20cm quad birdcage John built. The loop array is loaded into the birdcage on a cradle that centers it in two directions. The coils imaging region is approximately centered front-to-back when the front edge of the array former is 7cm in from the front of the birdcage former. The birdcage is centered in the magnet when its front edge is approximately 70cm from the inside wall of the shield room.

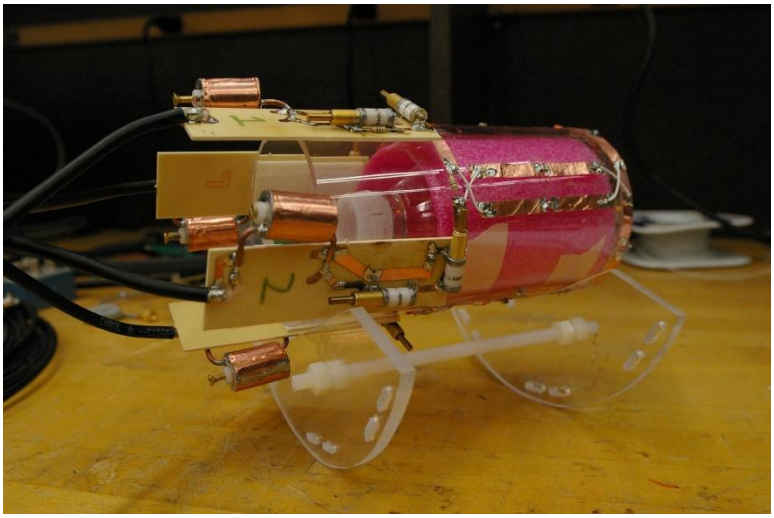


Figure A-5: Four channel transmit array. RF connections exit left. The array sits in the acrylic cradle so that it is correctly centered in the 20cm birdcage coil.

The birdcage connects to the magnet leg through the quad-hybrid ports. The correct cables need to be used to maintain the quadrature phase relationship. A pair of matched cables are zip-tied in the shield room that are used between the coil and the penetration panel. We typically connect the coil to these cables through a pair of bulk-head BNCs that are mounted in a small aluminum plate. The plate is the slipped between the wall and the metal of the shield room, though this is probably not strictly necessary. There is a second set of matched cables that normally runs from the penetration panel to the magnet leg, but because we are using John's PIN diode driver this is altered somewhat. The red (0°) port of the quad-hybrid is connected to the RF input of the diode driver through the cable that is taped to that port. The red cable that runs to the penetration panel then connects to the output of the diode driver. Zip-tied to the input cable of the diode driver is a second short RF cable that is marked yellow. This connects to the yellow (90°) port on the quad-hybrid and jumpers to the yellow cable that is connected to the penetration panel. Use only these cables so that the quadrature phase relationship is maintained. Also note that the color code is consistent and correct for this coil.

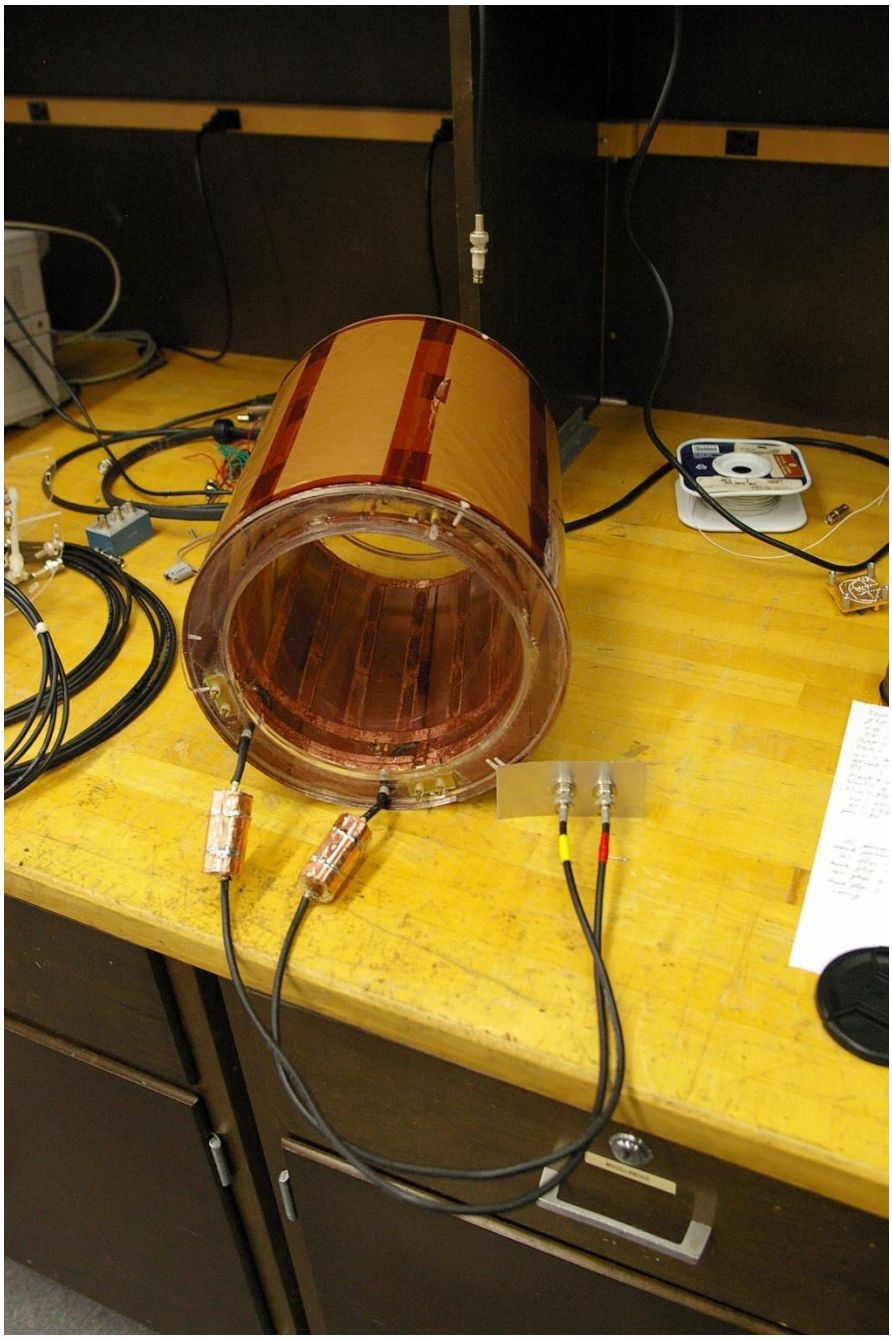


Figure A-6: The 20cm birdcage. Note the RF cables are color coded correctly for connection to the quad-hybrid. Also, the aluminum plate with bulkhead connectors can be used to ground the cable shields to the magnet at the end of the bore

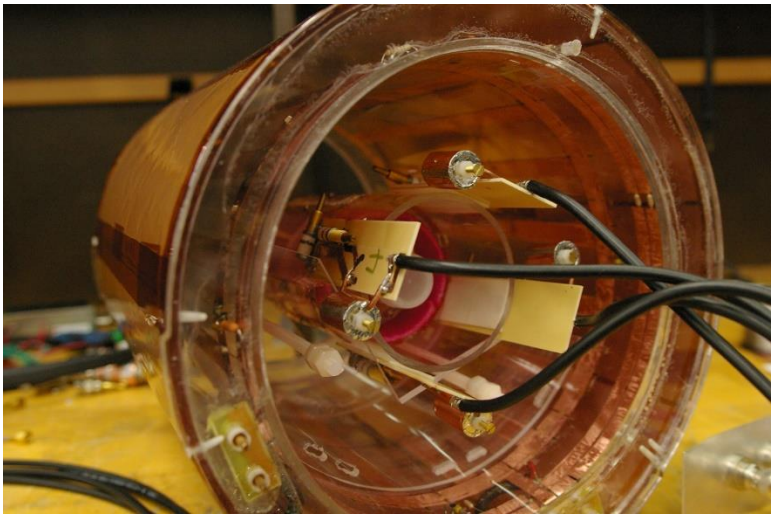


Figure A-7: The transmit array positioned in the 20cm birdcage. Note that the front of the array former is approximately 7cm from the front of the birdcage. Also, the RF cables exit the magnet bore into the shield room.

The array coil connects directly to the BNC connectors on the penetration panel. There is a sleeved bundle of four RG-58 cables that has been made to connect from the penetration panel to the power amplifiers in the 64-channel transmit system. Channels 2-4 connect directly to the output of the power amplifiers through these cables. Channel 1 needs to have its bias-Tee inline, so the cable from the power amplifier connects to the port labeled “TX”. The “coil” port is then jumpered to the penetration panel. DC is sourced from the output of Hykwon's PIN Diode driver.

Both PIN diode drivers are controlled by the Spare 3 line from the console. That line is currently routed through the Spare 1 port of the magnet leg (which is labeled “TX GATE” on the front of the magnet leg). John's diode driver should be set in the “system” position for tuning and normal operation. The other driver should be set to 'Coil “OFF” for high input' and “system controlled”. Note that the labeling on this is reverse for this coil, so it will actually be tuned when the control signal is high. If the diode drivers are correctly configured and connected the LED on John's will be off and on Hykwon's will be on when the digital line is low (when the system is idle). This corresponds to the birdcage being tuned and the array being detuned. The LEDs will blink to the other state when the system is running a multx sequence.

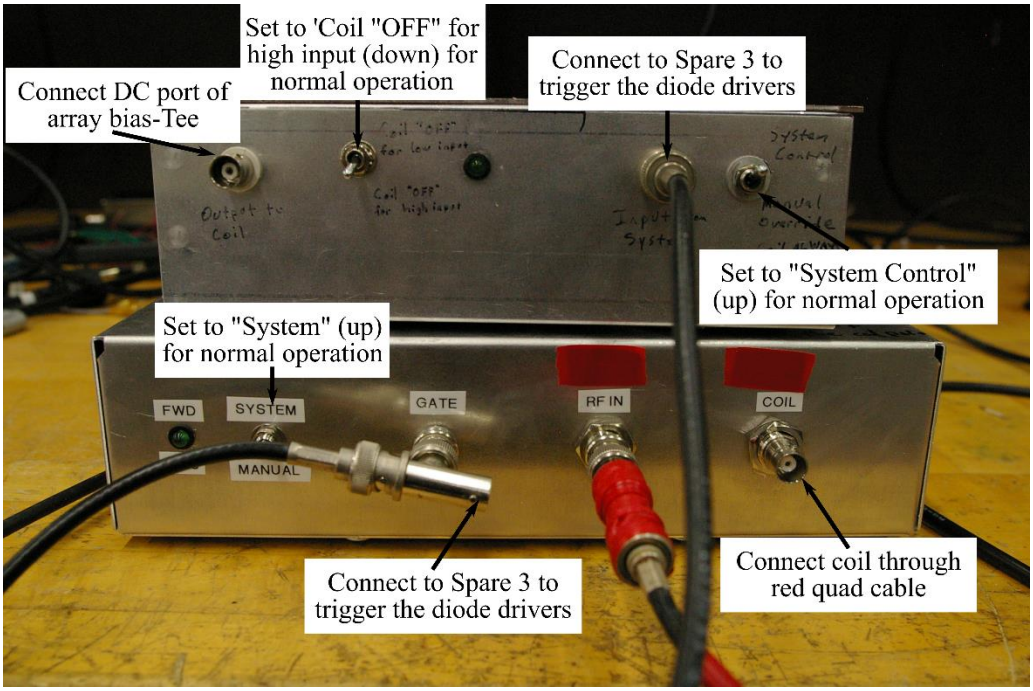


Figure A-8: The two PIN diode drivers. Top is the driver for the array, bottom is the driver for the 20cm birdcage.

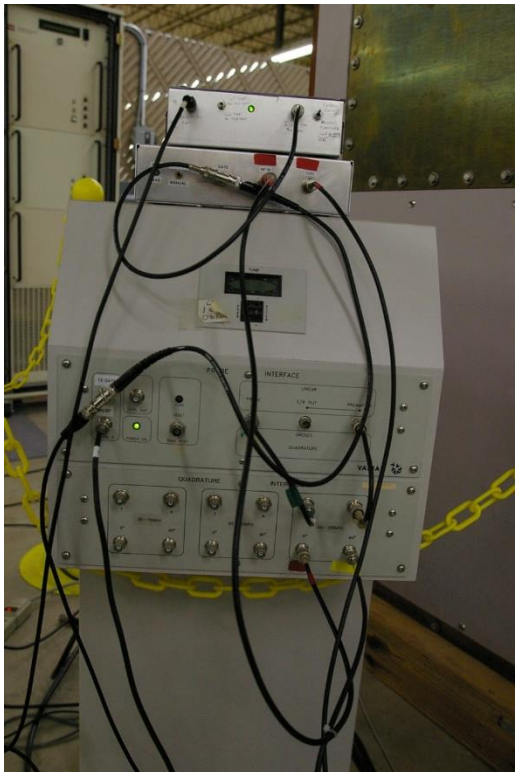


Figure A-9: Diode drivers located on top of the magnet leg. Note that the LED on the top driver is lit, while the bottom driver is not. Also note that the diode driver for the birdcage is connected after the quad-hybrid.

A-4 Powering on the pTx System

The NI chassis must be powered on before powering on the host control system. If the computer is powered first then it will not identify and enumerate the cards in the chassis, so the system will not function correctly.

Once all connections are made then the transmit system can be powered on. First, the modulators should be plugged in and powered on (switch above the AC inlet). Then the low voltage DC supplies in the 64 channel system can be powered on (top, then bottom rocker switches on the power supply unit). The seven segment display will flash various characters for a few seconds, then should settle out to '00', this normally displays the duty cycle the system is being operated at. If it does not settle to 00 in a few seconds then there is a problem and you should not proceed power on the system until it is resolved. The 3-phase AC cut-off should then be turned on. This will power the 50V DC supplies for the output amplifiers. The bottom (channels 1-32) rocker switch on the 50V supply rack should then be flipped to the on position. All indicators on the bottom three 50V supplies should now be lit and show good.

The Varian is powered in the normal way. Note that both of the shim supplies need to be turned on in order for all of the shim channels to work (which is important for obtaining good results).

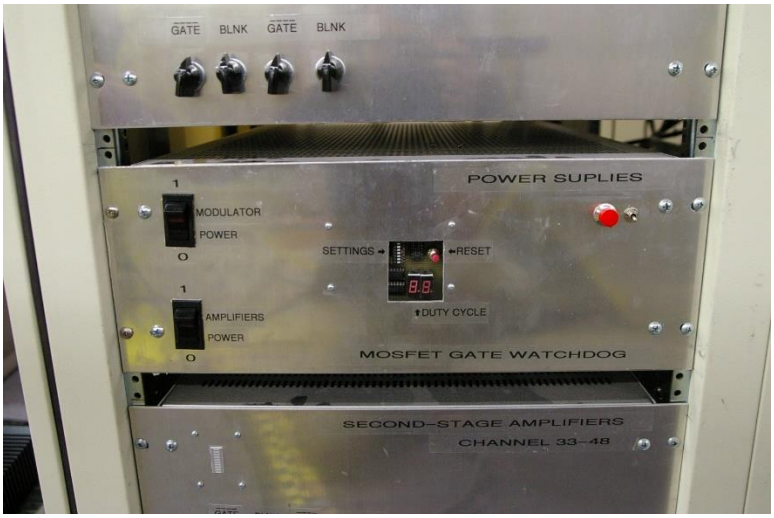


Figure A-10: Low voltage DC supplies for the 64 channel transmitter. Turn on the rocker switch labeld "MODULATOR POWER" first, then the one labeled "AMPLIFIERS POWER". Duty cycle monitor in center should settle to 00 before continuing.

Figure A-11: Cut-off for 3-phase AC for the 50V supplies at top. The bottom cut-off powers the 40cm equipment, do NOT power this off. Located on fence behind the 40cm magnet.

Figure A-12: The front of the 50V supply rack for the power amplifiers. Only the bottom three supplies are needed. The lower rocker switch needs to be turned on after the 3-phase power. At this point all three LEDs on the bottom three supplies should light.

A-5 Configuring the Parallel Transmit System

Start LabView 2011 click "Open" and navigate to the "March Software UMICH" folder located on the desktop. Open the "Feb 2013 Software.lvproj" file. Once this has loaded, double click the "Tx Transmit System Host.vi" entry in the project explorer. A window called "Resolve Load Conflict" will pop up. Select "Load With Selected" and the host software will load (hopefully correctly).

Now, the scaling factors for each of the channels will need to be set as follows:

Channel	Value
1	0.75
2	0.55
3	0.75
4	0.75

Table A-1: Scaling factors for modulators. Note that the little box to the left of the scaling factors should be set to zero.

The attenuation factors are set at:

Channel	Attenuation
1	21
2	20
3	20
4	20
5	19
6	20.5
7	15
8	20

Table A-2: Attenuation settings for modulators.

Calibration factors are all set to 1 for multiply and 0 for add. The PXI-7853R card should be in slot 3, connected to the modulator to be used. At this point, the modulators should be powered on and the software started (the "run" arrow at the top left of the interface), the waveform selected, and played out. It is not ready for playback until all three for the green indicators are lit. For long RF pulses this can take 10s of seconds. The software will wait for a trigger, and will play out the loaded waveform once each time it gets a trigger. If a different waveform file needs to be loaded then first quite the software, then restart it, select the desired waveform and click "play waveform" again.

A-6 B_1 Mapping

We obtain magnitude B_1 maps by using a Bloch-Siegert method. Eight images are required for this. Phase is extracted from a set of four gradient echo images, with channel one being used as a phase reference. The RF waveforms and are stored in the "b1mapping" folder on the desktop of the parallel transmit host computer. They can also be regenerated with the 'genbsfermi_2' and 'sinc_gen' MatLab scripts. The files are as follow:

File Name	Description	Generation Script
bs1.aap	CH.1 Fermi pulse, forward phase ramp	genbsfermi.m
bsconj1.aap	CH.1 Fermi pulse, reverse phase ramp	genbsfermi.m
bs2.aap	CH.2 Fermi pulse, forward phase ramp	genbsfermi.m
bsconj2.aap	CH.2 Fermi pulse, reverse phase ramp	genbsfermi.m
bs3.aap	CH.3 Fermi pulse, forward phase ramp	genbsfermi.m

Table A-3: Naming of B_1 mapping files.

File Name	Description	Generation Script
bsconj3.aap	CH.3 Fermi pulse, reverse phase ramp	genbsfermi.m
bs4.aap	CH.4 Fermi pulse, forward phase ramp	genbsfermi.m
bsconj4.aap	CH.4 Fermi pulse, reverse phase ramp	genbsfermi.m
sinc_ch1.aap	CH.1 sinc for phase mapping	sinc_gen.m
sinc_ch2.aap	CH.2 sinc for phase mapping	sinc_gen.m
sinc_ch3.aap	CH.3 sinc for phase mapping	sinc_gen.m
sinc_ch4.aap	CH.4 sinc for phase mapping	sinc_gen.m

Table A-3: Continued

The images for the Bloch-Siegert B_1 mapping are obtained using the 'Sgbs_multx' sequence (Sgems Bloch-Siegert for multi-transmit). To setup the sequence, first load Sgems, then set the sequence file with seqfil = 'Sgbs_multx'. Then ensure that 'tspulse' and and 'gsp2' are in the variable tree (query the values). If they are not, add them with create('tspulse') and create('gsp2'). The imaging parameters should be set as follows:

Parameter	Value
Tspulse	0.007312 sec
gsp2	2.9644 Gauss
TR	1000/3000 mSec
TE	14 mSec
Matrix size	128X128
Slice Thickness	2mm
RF coil	quad20cm
Pulse time	2000uSec
Pulse Pattern	Sinc
Pulse power	54dB
Flip angle	90
Spectral width	50000
Acquisition time	2.56 mSec
Receiver gain	30dB
Tped	0.002Sec

Table A-4: Parameters for Bloch-Siegert mapping.

When setting 'tspulse' you may get the error “tspulse set to it's maximum 5e-6” or similar. If this happens, then first remove it from the tree with delete('tspulse') then recreate it with create('tspulse') and try to set it again. Also, the Bloch-Siegert method is not very sensitive to the magnitude of the obtained images, so the tip angle and repetition time can be adjusted to suit. With distilled water, a 90° tip and 3second TR gives good results, reducing TR to 1second introduces an error on the order of 5% or less.

The scaling factors for each channel should be set at their normal operating range. Eight images will be collected using each of the Fermi pulses provided. Typically, these will be saved as “bs_coil#_1” for the forward phase ramp and “bs_coil#_2” for the conjugated phase. The maps should be checked to confirm that the magnitude of B_1 did not exceed what the method is sensitive to. The “bs_map” function can be used to compute and view each channels map, it is called as “bs_map(forward, reverse);” and will display the generated B_1 map. Forward is the image obtained with the “bs#.aap” pulse, reverse is the image obtained with the “bsconj#.aap” pulse.

Phase maps are obtained from four images taken using the “Sgpm_multx” sequence (Sgems Phase Mapping for multi-transmit)with the four “sinc_ch#.aap” files. To setup the sequence, first load Sgems, then set the sequence file with seqfil = 'Sgpm_multx'. No additional parameters need to be created for this sequence, as it is a standard gradient echo but using the parallel transmitter. The imaging parameters should be set as follows:

Parameter	Value
TR	1000/3000 mSec
TE	6 mSec
Matrix size	128X128
Slice Thickness	2mm
RF coil	quad20cm
Pulse time	3000uSec
Pulse Pattern	Sinc
Pulse power	54dB
Flip angle	90
Spectral width	50000
Acquisition time	2.56 mSec
Receiver gain	30dB
Tped	0.002Sec

Table A-5: Parameters for Phase Mapping.

Note that the RF power and pattern are hardcoded to the correct values, but for best results the system should be told that it is a sinc. Again, the phase information is what we care about, so the repetition time can be adjusted to obtain the data faster, but there may be some nominal degradation in quality. The images will typically be save as “phs_coil#”. A fifth image should be obtained, transmitting on channel 2 with a TE of 7mSec. This should be named “phs_coil2_te7” and is used to obtain the B_0 map. If different TE values are used, there should be a separation of 1mSec between the two in order to correctly obtain the B_0 map.

B_1 / B_0 maps are generated using the “loadb1_bs_2” script. The images just obtained should be downloaded into a folder named “b1” in the same directory as the script. The “lookuptab_fermi_4ms4kHz.mat' file should also be in the directory. Adjust any file name/size parameters in the script and run it. The “b1_bs.mat” file should be generated, which is needed for generating parallel transmit pulses.

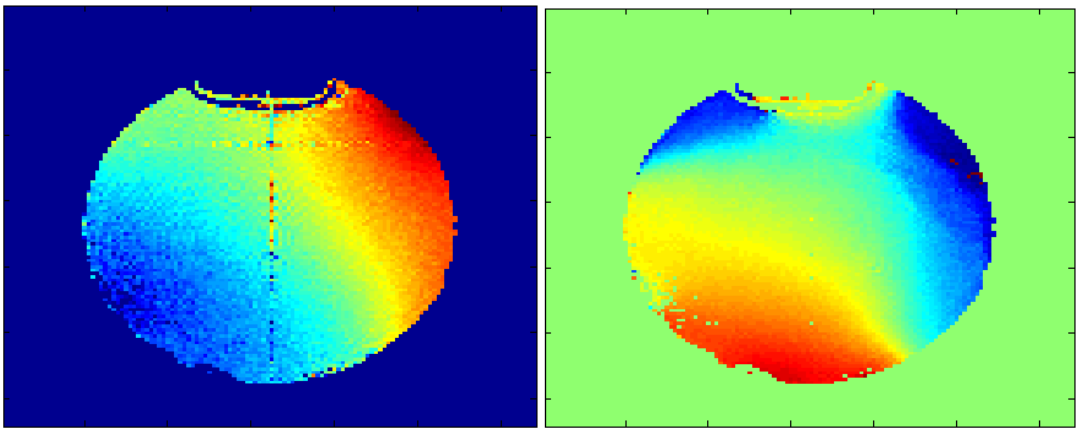


Figure A-13: An example of the B_1 maps that should result from the Bloch-Siegert method. Amplitude (Left) and corresponding phase map (Right). These can be displayed by calling imagesc(abs(b1(:,:,#))) and imagesc(angle(b1(:,:,#))) where # is the desired channel.

A-7 Generating the Parallel Transmit Pulse and Gradients

The “xsense_tamu_2” script is used to generate the RF and gradient waveforms for a 2D excitation. The script will write out the gradient and RF waveforms needed, and will print out both the time and gradient magnitudes. The expected print out will be similar to the following:

Designing echo-planar trajectory...
building system matrix
Warn: fatrix2_setup_dim 77: 1d odim full omask, >1d idim: transpose may not work
Warn: fatrix2_setup_dim 77: 1d odim full omask, >1d idim: transpose may not work
building penalty matrices

designing pulses

Uploading trapwill.GRD, blipwill.GRD, rfwill.RF to inova2

gsp1 = 0.6991

gsp2 = 1.4774

tspulse = 0.0193440000

detected 8 channels

The relevant information are the values for gsp1, gsp2, and tspulse. These are the settings that need to be entered into at the console for those variables. The gradient waveform files will be uploaded to the inova2 console under Neal's account. The default is to name them “blipwill.GRDacc” and “trapwill.GRDacc”. The RF waveforms will be written out to an AAP file with the default name of “acc_square.aap”. The AAP file needs to be loaded onto the parallel transmitter host computer. All of these will be found in the pTx folder.

A-8 Configuring the Varian for 2D RF Pulses

The current sequence being used for parallel transmit 2D RF pulses is the “Ssems_multx” sequence. Configuring it requires that the Ssems sequence is first loaded. Then confirm that the gsp1, gsp2, and tspulse variables exist and set them to the values obtained from the pulse generation script. The sequence can be setup normally, otherwise. Note that parameters that normally control the RF 90° pulse do not change the sequence. The pattern is coded to be a hard pulse and the power is fixed at 40dB. Typically, it's a good idea to set the time and pattern to match the 180, but it should not change the results.

A-9 Current Results

The current results from the square excitation with a flyback EPI is shown below on the left, with the same image that was obtained when Will was here on the right.

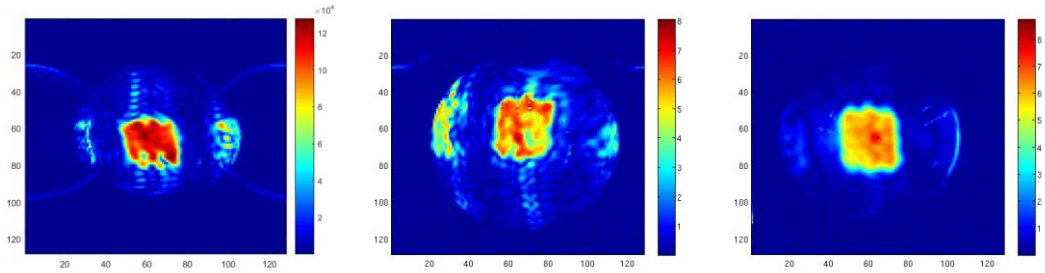


Figure A-14: Examples of the square excitation. Left is the most recent. Note that the FOV is oversized causing excitation foldover. Middle is an older excitation. Right is what we obtained when Will was here.

There appear to be a few changes in the setup since Will was here, and I have been unable to track them down so far. First is the fact that the scaling constants in the control system are significantly different than

what we saw previously. I expected the constants to be 0.75, 0.5, 0.75, 0.75 but needed to set them to 0.75, 0.5, 0.4, 0.375. I am unsure what caused this change. The coil was damaged at some point, so the tuning and decoupling have probably changed, but I didn't not expect it to be that significant. It's possible that the wrong linearization files were loaded, though I don't know why that would be the case. It also may be that I've simply set something up incorrectly, but I'm unsure of what.

The second thing to note is that the pattern I obtained appears to be flipped or transposed relative to what Will obtained. I'm not sure why this happened. I did make some alterations to the pulse sequences because I found some timing errors. Also, I needed to change the sequence used for Bloch-Siegert mapping to obtain good results. This caused some changes to the orientation of the data that I may not have correctly accounted for.

Overall, the results are close, but clearly worse than what we obtained last time Will was down. Clearly, more work needs to be done to correct these problems.

A-10 Setting Up MatLab

After installing MatLab a working C++ compiler will also be needed. The best freely available option is the Microsoft Windows SDK 7.1 available at http://www.microsoft.com/en-us/download/details.aspx?id=8279 . The SP1 will also be needed from http://www.microsoft.com/en-us/download/details.aspx?id=4422 . I believe this will have a working compiler, but there may be another needed hotfix.

A number of toolboxes and scripts are needed in order to run Will's pulse design routines. First you will need to download and install Fessler's Image Reconstruction Toolbox (IRT) from http://web.eecs.umich.edu/~fessler/code/index.html. Unzip it into an install directory, add the IRT top directory to MatLab's path (do not add sub directories) and run the "setup" command in MatLab. This should install IRT correctly, but needs to be done every time MatLab is loaded, can be added to startup script. Finally, the 'C:\IRT\mri\mri_exp_mult_mex.c' file needs to be compiled by calling mex on it from the MatLab console.

You will also need the files in the ptx_files.zip/matlab_files directory. This contains the various scripts and functions that are needed to do the design. Unzip this folder to the working directory.

The epi folder contains scripts that are called by the RF design script. @fastRF is a MatLab method needed by other scripts. rf_tools is a set of scripts developed by John Pauly (I think) for RF design. A few of the files in the rf_tools/mex5 need to be recompiled and moved up to the rf_tools folder: abrx.c, b2a.c, b2rf.c, cabc2rd.c

blochsim_optcont_mex_b1.c is a Bloch simulator written for Matlab. The blochsim_optcont_mex_b1.mexa64 and blochsim_optcont_mex_b1.mexw64 are the compiled Linux and Windows port, respectively. The Windows port requires the "pthreads_win32" (https://www.sourceware.org/pthreads-win32/) library and dll to function correctly. The lib and dll should be placed in the same directory as blochsim_optcont_mex_b1. It has also been modified to do the dynamic

array allocation using malloc and free. This change was needed because the original version used a non-standard behavior of the GCC compiler, but MatLab doesn't easily work with GCC on Windows, and needs Visual Studio to function correctly. The unaltered file is in the "original" subfolder, while the windows version is in the main directory.

The bs_map.m is a function that will generate and display the magnitude B_1 map using the Bloch-Siegert method. Forward and inverse 2D transforms with correct shifts are handled by the ft2.m and ift2.m convenience functions.

The actual B_1, B_0 and mask are generated by the loadb1_bs_2.m function. lookuptab_fermi_4ms4kHz.mat is data needed to generate the B_1 maps, it is also made when the genbsfermi_2 script is run. The RF data that Will's scripts generates can be converted to our AAP format using the rf2aap_ptx.m function. The gradient waveforms (and RF) are converted to the Varian format using the will2varian2.m function.

Replace the FID files in the b1 directory with those obtained when gathering the B_1 mapping data. The B1mapping folder contains the RF waveforms in AAP format needed to perform B_1 mapping

APPENDIX B
MOSFET CHARACTERISTICS

B-1 DC Characteristics

A basic curve tracing circuit, shown in Figure B-1 can be used to measure the DC characteristics of a MOSFET. The MOSFET is connected in a "common source" configuration, with the source terminal grounded. Variable DC voltage sources, V_{GG} and V_{DD}, are connected to the gate and drain terminals of the MOSFET, respectively. The ammeter A_D and voltmeters V_G and V_D are used to measure the drain current (I_D) gate voltage (V_{GS}) and drain voltage (V_{DS}) respectively.

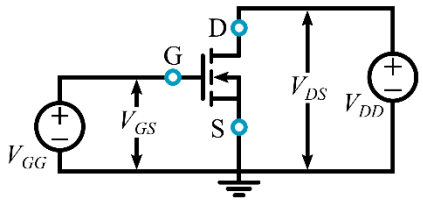


Figure B-1: The schematic of a basic curve tracer circuit. It is used to determine the DC characteristics of the MOSFET.

This test circuit can be used to generate the "transfer curve" of the MOSFET which shows the how the drain current changes as the gate voltage is varied. The measurement is made by setting V_{DD} to be a constant voltage that is relatively large (on the order 10's of volts). V_{GG} is then varied from zero to some positive value of a few volts while recording V_{GS} and I_D. A plot of I_D against V_{GS} results in the characteristic curve of Figure B-2. The transfer curve can be divided into four major regions based on the relation of I_D to V_G. In the first region, where $V_{GS} < V_T$, I_D is zero. Next, we see a small quadratic increase in I_D relative to V_{GS} when $V_T < V_{GS} < (V_{GS} - V_T) < V_L$. This is followed by region where I_D increases linearly when $V_L < (V_{GS} - V_T) < V_U$. Finally, I_D begins to saturate when $V_{GS} > V_U$. The forward transconductance of the MOSFET, which governs its ability to amplify, is commonly defined for the linear region of the transfer curve as:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \tag{B.1}$$

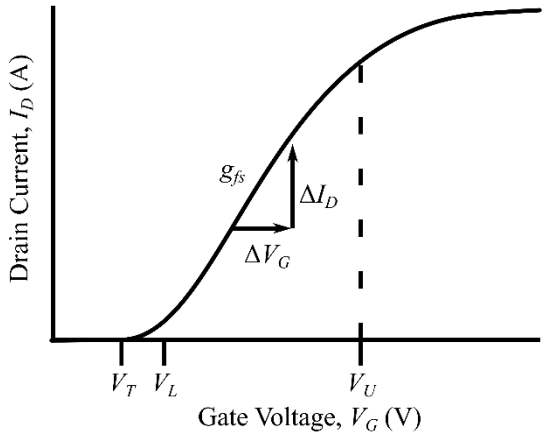


Figure B-2: Transfer curve of MOSFET. It shows the Drain current flow for any applied gate voltage.

The RF behavior of the MOSFET is based on the periodic traversal of the transfer curve corresponding to the periodic swing of the gate voltage. The transfer curve is used to define the quiescent (or operating) point of the RF amplifier based on this periodic traversal. The same basic test system can be used to generate a set of I-V curves that relate the drain current to the drain voltage at fixed gate voltages. In this case, V_G is fixed at some voltage and V_D varied from zero to V_{DD}, while measuring V_{DS} and I_D. This is repeated for different values of V_G between zero and V_{GS}. The result in characteristic curves can be plotted as shown in Figure B-2.

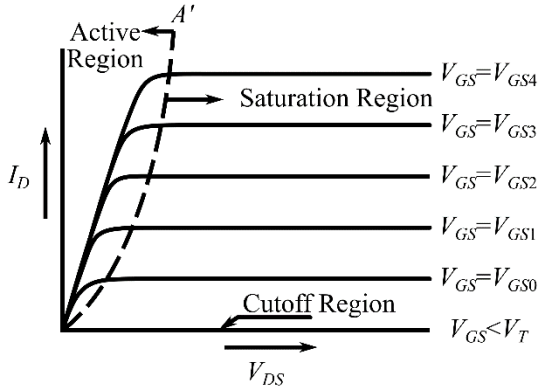


Figure B-3: I-V curves of the MOSFET. Each curve corresponds to a specific setting of V_{GS}. The three regions of operation are shown.

Three distinct regions of operation, marked in Figure B-3, are defined as follows:

- In the "cutoff" region, when $V_{GS} < V_T$, I_D is zero. This region is symbolically represented in Figure B-4(a).

- In the "active" region, when $V_{GS} > V_T$ and $V_{DS} < V_{DSat}$, I_D increases linearly as V_{DS}. The projection of OA' on the abscissa in Figure B-3represents the range of V_{DSat} over the range of V_G. This is symbolically represented as a series resistor, $r_{DS(on)}$, in the drain-source path seen in Figure B-4(b).
- In the "saturation" region, when $V_{GS} > V_T$ and $V_{DS} > V_{DSat}$, I_D changes negligibly with V_D. The MOSFET behaves as a true current source in this region, shown symbolically in Figure B-4(c).

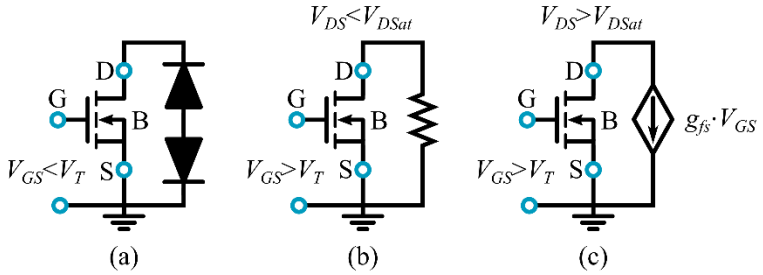


Figure B-4: Symbolic representation of the three MOSFET states.

These measurements, and the resulting curves, define the basic operation of a MOSFET. They are vital to the understanding of how a MOSFET functions as an amplifier, but are not sufficient to understand its behavior at RF frequencies, so we will take an expanded view of the parameters of a MOSFET.

B-2 RF Characteristics

The structure of the MOSFET results in the formation of parasitic capacitances that are not significant at low frequencies but have significant effect on the MOSFET response at RF. The capacitances occur between the various nodes that are isolated by insulating regions, and are shown diagrammatically in Figure B-5. The interface of the drain and substrate forms a diode that is reverse biased, resulting in a junction capacitance C_{DS}. C_{DS} depends on the applied reverse voltage across the diode. The gate metallization partially overlaps the diffused N-type regions of the gate and drain, giving rise to C_{GS} and C_{GD}. These are not voltage dependent because they are not junction capacitances.

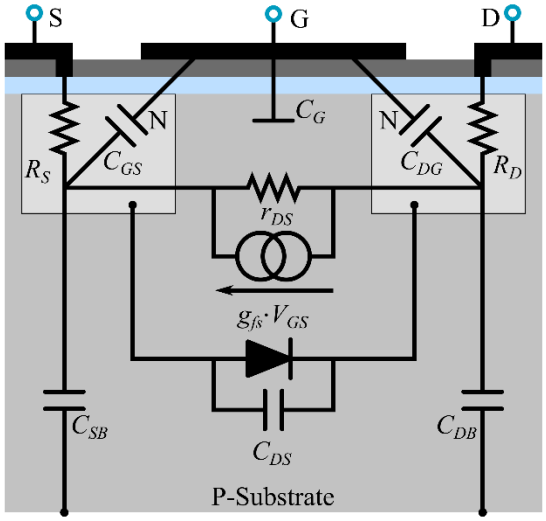


Figure B-5: Parasitic capacitances of the MOSFET. C_{GS} and C_{DG} are the parasitic capacitances formed due to overlap of the gate metallization over the source and drain regions respectively. C_{DS} is the drain-source capacitance formed due to the reverse biased diode at the drain-substrate interface.

Typically, a MOSFET datasheet does not specify C_{GS}, C_{DG}, and C_{DS}. Instead, values of the output capacitance, C_{os}, input capacitance, C_{is}, and feedback capacitance, C_{rs}, which are hybrids of the previously mentioned capacitances. These two sets of values are related as follow:

- C_{os} is measured with V_{GG} set to ground potential and is given by:

$$C_{os} = C_{DS} + C_{GD} \tag{B.2}$$

  C_{os} appears as a capacitance across the output terminals of the MOSFET. Since the internal resistance of the MOSFET current source is very high, the output impedance of the MOSFET is essentially the output capacitance.

- C_{is} is measured with the drain shorted to the sourced terminal and appears across the input terminals of the MOSFET. C_{is} is given by:

$$C_{is} = C_{GS} + C_{GD} \tag{B.3}$$

  C_{is} does not vary significantly with the applied gate voltage. The effect of C_{is} is to reduce the input impedance of the MOSFET. This makes matching to a 50Ω generator more difficult.

- C_{rs} is the feedback capacitance and is the same as C_{GD}. Through proper layout of the MOSFET, this capacitance is minimized.

MOSFET behavior In saturation can be represented with a hybrid-pi model, which uses a relatively simple circuit model[70]. The most basic form represents the MOSFET as an open circuit between Gate and Source, and a voltage controlled current source between Drain and source. The input voltage node (V_{GS}) modulates the output current as $V_{GS} \cdot g_{fs}$. The parasitics can be included as lumped element capacitors between nodes

of the device, as show in Figure B-6. The increased complexity of additional elements improve the model's accuracy, but the inherently non-linear operation of the MOSFET in large signal operation makes it difficult to completely model its behavior.

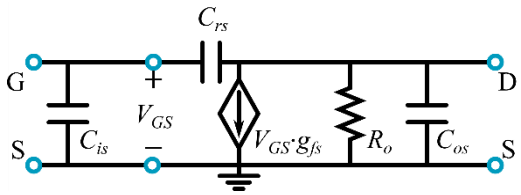


Figure B-6: The hybrid-pi model of a MOSFET. It provides a basic circuit level description of the behavior of MOSFET devices that can be helpful to understand amplifier behavior.

It is important to remember that most elements of this model will be modulated by the bias point, and the value of V_{DS} and I_{DQ} can have especially strong influences on C_{os} and g_{fs} respectively. Further, C_{OS} is a function of the drain-source voltage. So, for a given operating point (a pair of gate and drain DC bias voltages) we can model the device with a fairly simple circuit.

Combining the DC and RF characteristics will allow us to being considering amplifier design. One of the first major questions is how the quiescent point of the amplifier should be selected, and what impacts it has on performance. This is, essentially, a question of what "class" an amplifier should be.

B-3 Mechanism of RF Power Amplification

The principle of operation of a MOSFET RF amplifier can be analyzed on the basis of the DC characteristics of the MOSFET. A class A amplifier will be analyzed in this section for simplicity, other linear class amplifiers can be analyzed similarly. Switch mode class amplifiers operate on the same fundamental principles, but the analysis proceeds somewhat differently because of their highly non-linear operation.

The analysis will proceed from a basic common source RF amplifier, as shown in Figure B-7 with symbols defined in Table B-1.

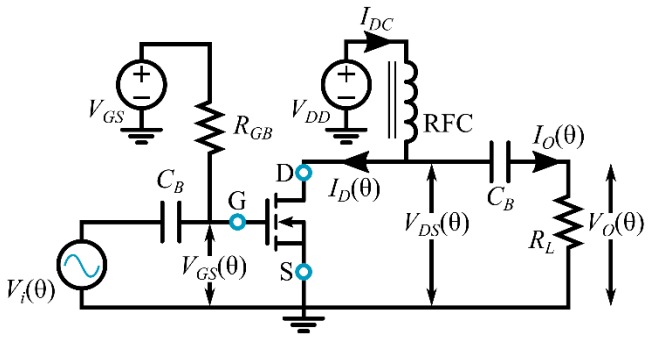


Figure B-7: Schematic of the basic RF amplifier. The parasitic output capacitances described in Section B-2 are ignored here. In reality, the parasitic capacitances are compensated for and the load resistance represented by R_L is a virtual load resistance.

Symbol	Definition
C_b	DC block capacitor
I_{DC}	DC quiescent current drawn by MOSFET
$I_d(\theta)$	Time varying drain current
$I_o(\theta)$	Time varying load current
R_{GB}	Gate bias resistor
R_L	Load resistor
RFC	RF choke
V_{GG}	Gate DC supply voltage
V_{DD}	Drain DC supply voltage
$V_{GS}(\theta)$	Time varying gate-source voltage
$V_{DS}(\theta)$	Time varying drain-source voltage
$V_i(\theta)$	Time varying input voltage
$V_o(\theta)$	Time varying output voltage

Table B-1: Symbols used in RF amplifier design and their definitions.

The RF source produces a sinusoidal voltage $V_i(\theta)$ such that:

$$V_i(\theta) = V_{im}\sin(\theta) \tag{B.4}$$

Where V_{im} is the peak voltage of the input. This combines with the DC gate bias to result in a gate-source voltage that is:

$$V_{GS}(\theta) = V_{GG} - V_{im}\sin(\theta) \tag{B.5}$$

For class A operation $V_{im} < (V_{GS} - V_T)$ hence $V_{GS}(\theta) > V_T$ for $t > 0$ so the entire voltage waveform presented to the gate lies in the linear region of the transfer curve. The amplified output of the device is found as the multiplication of equation (B.5) with the transconductance g_{fs} (defined in equation (B.1):

$$I_{DS}(\theta) = I_{DQ} - I_{om}\sin(\theta) \tag{B.6}$$

The quiescent current I_{DQ} flows through the RF choke and the RF current $I_{om}\sin(\theta)$ flows through the blocking capacitor into the load, R_L. Here, I_{om} is the peak current of the output RF wave. This creates a voltage drop of $V_o(\theta)$ across it, given by:

$$V_o(\theta) = R_L I_{om}\sin(\theta) = V_{om}\sin(\theta) \tag{B.7}$$

Similar to previously, V_{om} defines the peak voltage of the output RF wave. This results in power dissipated is R_L defined as the output power P_o, found as:

$$P_o = \frac{I_{om}^2}{2R_L} = \frac{V_{om}^2}{2R_L} \tag{B.8}$$

From equation (B.7), it is clear that instantaneous drain-source voltage $V_{DS}(\theta)$ must be:

$$V_{DS}(\theta) = V_{DD} + V_{om}\sin(\theta) \tag{B.9}$$

The amplification processes described in by these equations is illustrated in Figure B-8. From Figure B-8 (c) and Figure B-8 (f), it can be seen that the drain current is minimum at maximum voltage across the drain-source terminals and vice versa.

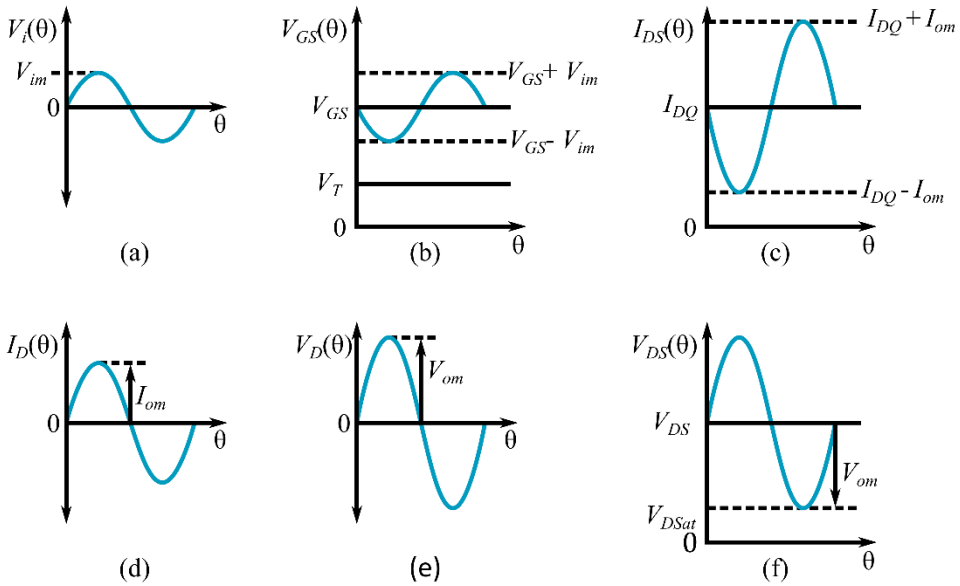


Figure B-8: Waveform diagram of Class A amplifier. Figures (a) through (f) are pictorial representations of equations (B.4) through (B.9) except equation (B.8).

Equation (B.8) implies that the output power varies linearly as the amplitude of the output voltage swing. Further, V_{om} itself varies linearly as R_L so equation (B.8) implies that when the MOSFET behaves as a current source, with a larger load resistance resulting in greater output power. This behavior is bounded by the fact that the drain-source voltage must remain larger than the drain saturation voltage at all times, that is $V_{DS}(\theta) > V_{DSat}$. From this we see that equation (B.9) imposes an upper bound on the peak output voltage of:

$$V_{om} \le V_{DD} - V_{DSat} \tag{B.10}$$

Initial assessment of equation (B.9) would seem to indicate that that V_{DD} could be increased arbitrarily to accommodate the condition imposed by equation (B.10). However the avalanche breakdown voltage, $V_{BR(DSS)}$, of the reverse biased diode formed by the drain-substrate interface imposes an upper bound on V_{DD} as:

$$V_{DD} \le V_{BR(DSS)} - V_{om} \tag{B.11}$$

From equation (B.8) and the conditions (B.10) and (B.11), the optimum value of R_L can be calculated as:

$$R_L = \frac{(V_{DD} - V_{DSat})^2}{2P_o} \tag{B.12}$$

This analysis indicates that the MOSFET may be described as a high resistance current driver. The RF operation of the amplifier is shown overlaid on the DC characteristic curves of the MOSFET in Figure B-9. The line DD' represents the variation of the drain current and voltage, I_D and V_{DS}, with the sinusoidal variation of the gate voltage above the threshold voltage. DD' is a straight line because I_D and V_{DS} are 180° out of phase for a pure resistive load. A pure reactive load would cause DD' to be a perfect circle, while for the mixed loads found in most practical situations DD' would become an ellipse. This is caused by the phase shift in the current to voltage relationship that is caused by reactive impedances.

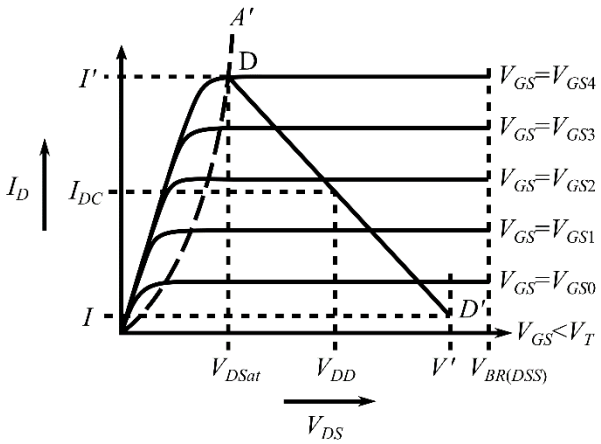


Figure B-9: The output swing of a MOSFET amplifier. DD' is the locus of V_{DS} and I_{DS} during RF operation of the MOSFET. V_{DS} swing is represented by VV'. The I_{DS} swing is represented by II'. The lower limit for the V_{DS} swing is V_{DSat}. I_D swings about I_{DQ}, the quiescent current.

APPENDIX C
DIODE CHARACTERISTICS

The diode is one of the foundational components, especially in RF circuits. Its intrinsic non-linear behavior makes it useful in both switching and mixing functions, as well as protection circuits and some bias networks. A thorough understanding of diode behavior is needed to appreciate how it functions in different circuits, as well as the functionality of different types of diodes. A cursory look at the ideal diode is a suitable starting place, followed by the typical p-n junction diode, the Schottky diode, and finally the PIN diode.

C-1 Ideal Diode

The ideal diode exhibits infinite forward conductance, with zero reverse conductance. The schematic symbol and a basic DC measurement circuit is shown in Figure C-1. The diode is biased with a voltage source, ranging from a negative voltage up to some positive voltage while recording the current through the diode. This relationship forms the diode I-V curve, which is fundamental to the behavior of a diode. An example of an ideal diode curve is shown in Figure C-2.

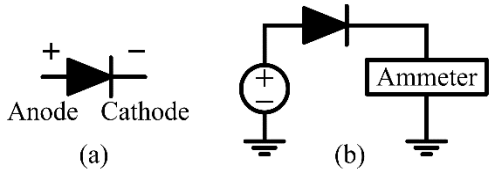


Figure C-1: The diode symbol and measurement circuit.

The behavior of a diode is non-ohmic, in that the relationship between voltage and current is not linear. For an ideal diode it can be described as follows:

$$\begin{aligned} I_{diode} &= 0 \quad : V_{diode} < V_T \\ I_{diode} &= \infty \quad : V_{diode} > V_T \end{aligned} \tag{C.1}$$

This is clearly non-physical behavior, but is interesting as it provides an idea of why one would use a diode. If a small signal is applied, and a large DC bias, then a diode will act as a switch. As long as the sum of the signal and bias remains below V_T the switch is off, if they are above then the switch is on. If the bias is also a signal then a type of multiplier or mixer is formed. While diodes do not have the idealized transfer function shown here, they are still useful for these applications.

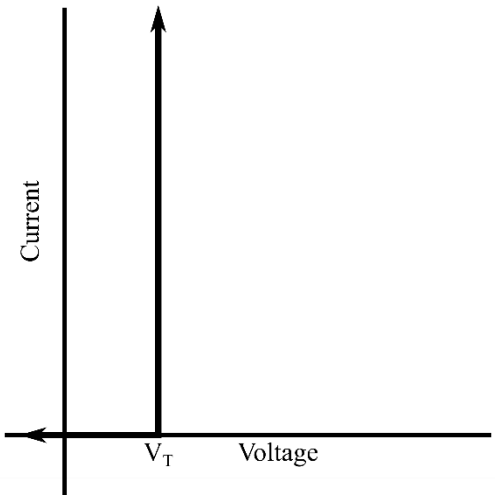


Figure C-2: The ideal diode I-V curve. It is characterized by no current flowing until the device is forward biased to at least its turn-on voltage (V_T) following this the diode does not require any additional potential to generate a higher current. That is, the current vs. voltage becomes a vertical line.

C-2 P-N Junction Diode

The p-n junction diode is one of the most common type of diodes or rectifiers. Their physical structure is basically what is implied, as section of p-type semiconductor is attached to n-type semiconductor. This basic structure is shown in Figure C-3. There are a number of construction methods for the p-n diode, that result in similar performance and structures. We will not consider the details of construction, as semiconductor manufacture is a highly specialized field.

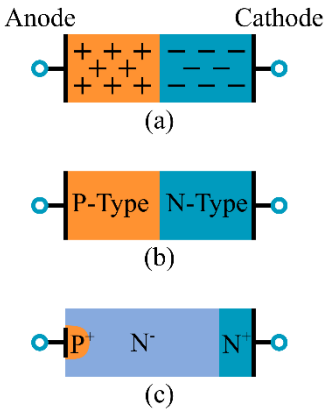


Figure C-3: The p-n junction diode. The charge carrier (holes for positive and electrons for negative) can be thought of as being distributed as shown in (a). This corresponds to a physical construction like that of (b) with the p-type and n-type semiconductors essentially identical and connected uniformly. A more realistic construction is what is shown in (c). In this case, a heavily doped p-type region (P^+) is diffused into a lightly doped n-type (N^-) region. A heavily doped n-type region is diffused into the N^- substrate at the opposite end. Note that the anode metallization does not extend beyond the P^+ region.

For a p-n junction there are two distinct charge carriers, the negatively charged electron and the positively charged "virtual particle" the hole. These two particles will annihilate or recombine when they come into contact with each other, leaving a neutrally charged semiconductor lattice. In an unbiased diode the charge carriers near the junction will tend to annihilate, leaving a depletion region where there are no free carriers. When the junction is forward biased additional charge carriers are added to the crystal, resulting in a thinning of the depletion region. At some point the depletion region collapses, and conduction through the diode becomes high. This is the turn-on voltage of the diode. Conversely, reverse biasing the junction will lead to the depletion region widening as fewer carriers are available. This simple analysis leads to the I-V curve shown in Figure C-2, but the actual availability of carriers follows a statistical distribution, as seen in Figure C-4.

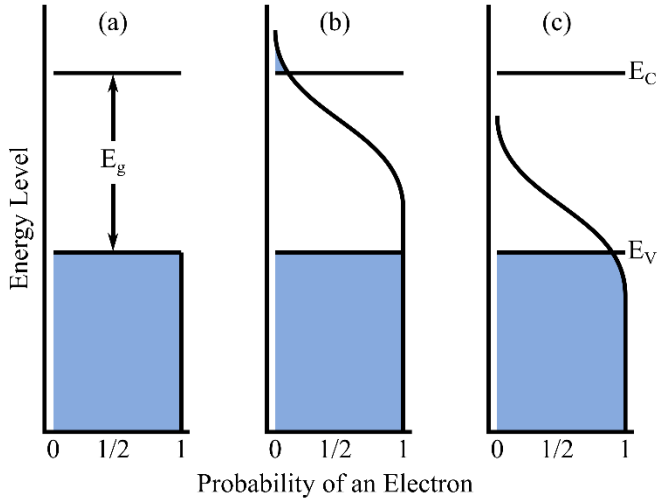


Figure C-4: Energy Band distribution of electrons in a semiconductor. A simplistic view of the behavior of semiconductors leads to (a), where electrons are either in the conduction band (above E_C) or in the valance band (below E_V). The bias voltage will push the electrons into one state or the other based on the gap energy (E_g). A more realistic model has the probability of an electron at any given energy level following a Fermi-Dirac distribution. This leads to some number of electrons being available for conduction at bias points in an n-type semiconductor, as shown in (b). Similarly, the p-type semiconductor will always have some likelihood of a free hole, as shown in (c).

The availability of electrons and holes for conduction is dependent on their being at an energy level that allows them to move through the crystal lattice of the semiconductor. That is to say, the electrons must be in the conduction band and not the valence band for it to be free to conduct. Conversely, there must be a lack of an electron in the valence band for there to be a free hole. The distribution of electrons across all energy levels follows a Fermi-Dirac distribution, which is defined by:

$$f_e(E) = \frac{1}{e^{E-E_F/kT}+1} \tag{C.2}$$

This defines the probability of an electron being at a given energy level ($f_e(E)$) where the energy level is E , k is the Boltzmann constant, T is the temperature in Kelvin, and E_F is the Fermi energy which is the energy level where $f_e(E) = 0.5$. The model shown remains a simplification and incomplete model, but begins to give an idea of where the actual behavior of a diode comes from. The result is that the I-V curve of a p-n diode is more complex than the ideal diode, shown in Figure C-5.

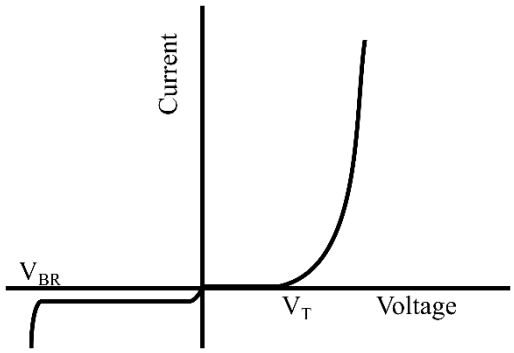


Figure C-5: The I-V curve of a p-n junction diode. After the turn-on voltage the diode does not conduct perfectly, but will move through a "square law" region into high conductance. Additionally, there is some small reverse current when the diode is reverse biased. At a large reverse bias voltage the device will fail and begin to conduct.

The Shockley diode equation can be used to model the general behavior of the I-V curve, though it does not account for some processes, such as photon generated carriers or reverse breakdown voltage. The equation relates the diode current (I_D) to voltage (V_D) by:

$$I_D = I_S\left(e^{V_D/nV_T} - 1\right) \tag{C.3}$$

I_S is the reverse bias saturation current, n is the ideality factor that ranges from 1 to 2 and accounts for carrier recombination in the depletion region, and V_T is the thermal voltage of the device that is found as kT/q. In this case k is Boltzmann's constant, T is the junction temperature in Kelvin, and q is the electron charge.

Until this point the low frequency behavior of the diode has been considered. At higher frequencies the performance is altered due to the details of the device physics. Specifically, there are two important energy storage mechanisms that occur in a p-n junction diode: junction capacitance, C_J , and the diffusion capacitance C_D. The carriers (electrons and holes) in the p and n regions are associated with a "space charge", and so contribute to this capacitance. An approximation of the junction capacitance can be found by assuming that the junction acts as a parallel plate capacitor:

$$C_J\left(V_D\right) = \frac{A_J \kappa \epsilon_0}{W\left(V_D\right)} \tag{C.4}$$

Here, A_J is the cross sectional area of the depletion region, κ is the relative permittivity of the semiconductor, ϵ_0 is the permittivity of free space, and $W(V_D)$ is the width of the depletion region as a function of the applied voltage. In general, the charge in a diode does no accumulate directly at the edges of the depletion region, and the doping is not uniform. This leads to a more complicated equation for the junction capacitance, but follows the same basic concept.

The drift capacitance is associated with the minority carriers that are injected in to the depletion region under forward bias. These carriers will persist for some amount of time, even as the bias changes, governed by the transit time τ_T. This is a function of the semiconductor lattice purity and channel length. The result is charge storage under the forward bias condition that is given by:

$$C_D = \frac{I_D \tau_T}{V_{th}} \tag{C.5}$$

This contributes to a finite forward to reverse, and reverse to forward recovery times. As the bias on the diode switches the stored charge must be depleted to either allow current to begin to flow or cease flowing. In the extreme, the diode will not act as a rectifier for high voltages at all.

C-3 Schottky Diode

The Schottky diode is structured significantly differently than a standard junction diode since there is no semiconductor junction to speak of. Instead, a metal Schottky barrier is made that noise to a lightly doped n-type semiconductor. A point-contact diode is one variation of this in which a fine wire is held in mechanical contact with the semiconductor crystal, as shown in Figure C-6(b). This “cat’s whisker” wire has an extremely low junction capacitance owing to its very small area. Additionally, the turn on voltage of the diode is very low. In some cases the diodes can be operated in a “zero bias” mode, where it is effectively turned on with no forward bias voltage. Finally, these diodes have extremely fast recovery time because a depletion region does not form in the same way as with a p-n junction. This has historically made the point-contact diode extremely useful for RF detectors, though it has lost popularity in recent years.

Schottky diodes are similar, but have substantially larger barrier areas. This improves their power handling capabilities relative to the point-contact diode, but does increase the junction capacitance somewhat. They retain a very low turn on voltage, so they are useful for protection circuits and passive switches. A comparison of the I-V characteristics with those of a p-n junction can be seen in Figure C-7.

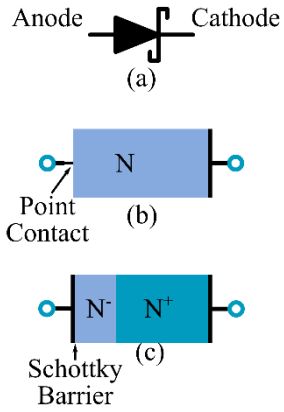


Figure C-6: The Schottky barrier junction diode. A typical schematic symbol is shown in (a). The original solid-state diode design was a point-contact diode, where a thin metal wire was place in contact with a semiconductor crystal (b). The point contact forms a p-type diffusion region, and the result is a diode with extremely low junction capacitance, low turn on voltage, but poor power handling capabilities. Schottky diodes modify this design by metalizing most of the face of an epitaxial grown N^- layer (b). The resulting junction has higher capacitance than a point contact diode, but retains the low turn on voltage and improves on the current handling.

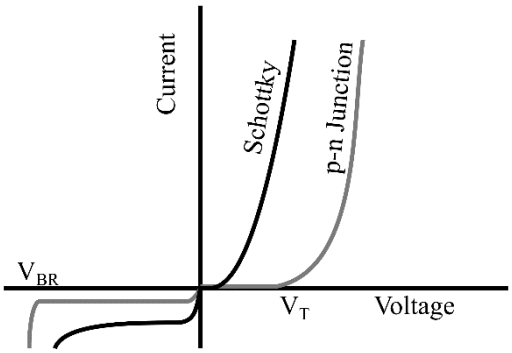


Figure C-7: The I-V curve of a Schottky diode. The turn on voltage is substantially lower than a typical p-n junction diode, but there is higher reverse bias current and a lower breakdown voltage. Schottky diodes are typically preferred when a low forward voltage or fast switching time is needed.

The Schottky diode equation is a modification of equation (C.3) that accounts for some of the physical differences of the two structures. The two major change are the inclusion of an ohmic voltage drop due the contact and semiconductor resistance R_S, so the I-V curve can be modeled by:

$$I_D = I_S\left(e^{V_D - I_D R_S / nV_T} - 1\right) \tag{C.6}$$

Additionally, the Schottky diodes does not have junction capacitance to speak of. There are no minority carriers in the device, as all majority carriers are collected by the metal interface, so there is no charge storage associated with the forward bias current of the diode. This characteristic is what allow for the fast switching times of the diode, and will make it possible to rectify high frequency signals. The point-diode

additionally minimizes the junction capacitance my minimizing the junction area using the cat's whisker contact. A standard Schottky diode still has junction capacitance associated with the ohmic contact region.

C-4 PIN Diode

The PIN diode can be thought of as a logical inverse of the Schottky diode. They are constructed with a large, undoped or lightly doped intrinsic region between the p-type and n-type regions, as shown in Figure C-8. This increases the effective width of the depletion region, and generally slows the diode recovery time down. Interestingly enough this also makes them extremely useful for RF applications. A forward bias current applied to the PIN junction causes it to behave as a resistive element, as opposed to a rectifier, since the intrinsic region will not deplete fully at high frequencies. By adjusting the bias current the resistance of the device can be modulated from nearly infinite, since the PIN junction has very low junction capacitance, to nearly a short at large forward currents. So the PIN diode also sees use in switching elements and limiters, but is inherently an active device.

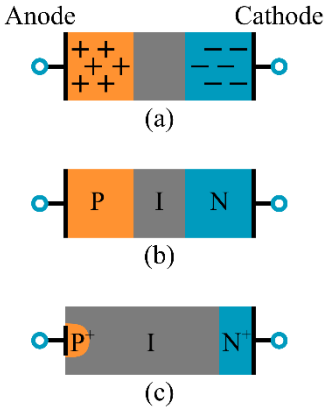


Figure C-8: The PIN diode structure. The design is very similar to a standard p-n junction diode, but includes a large intrinsic region between the p and n doped diffusion regions. The result is a very wide depletion region, as shown in (a). The conceptual and realized structures, (b) and (c), mirror those of the p-n junction.

At low frequencies the PIN diode functions in the same way as a p-n diode, though with a substantially larger depletion region. This is neither terribly useful, nor interesting, functionality. In contrast, the PIN diode at high frequencies begins to act as a current controlled resistor. The diode is designed to have low junction capacitance so that it is a high impedance to RF when it is reverse biased. In contrast the diffusion capacitance is extremely high. This leads to significant charge storage in the forward bias state that is achieved primarily due to the long carrier transit times associated with a wide depletion (intrinsic) region. The stored charge in the forward bias condition is found as:

$$I_D = {dQ}/{dt} + {Q}/{\tau_{eff}} \tag{C.7}$$

Where τ_{eff} is the effective carrier life time in the intrinsic region. For a DC bias this simplifies to:

$$Q = I_D \tau_{eff} \tag{C.8}$$

Based on this charge storage and the physical parameters of the intrinsic layer we can find the resistance that the junction has for RF in the forward biased state:

$$R_J = \frac{W^2}{\left(\mu_n + \mu_p\right) Q} \tag{C.9}$$

Where μ_n and μ_p are the electron and hole mobility respectively. This behavior only occurs for frequencies that are above the transit time of the intrinsic region. The charge storage is assumed to be controlled only by the low frequency or DC bias. The result is that at high frequency the PIN diode can be approximated by a series resistance and inductance when it is forward biased. This remains true as long as the stored charge is not substantially depeleated by the RF waveoform, so:

$$Q >> \frac{I_{RF}}{2\pi f} \tag{C.10}$$

In the reverse bias case there is no diffusion capacitance because no charge has been injected into the intrinsic region. Instead, the capacitance of the device is dominated by the junction capacitance that was defined in equation (C.4). The width of the depletion region in this equation would be extremely large because of the intrinsic region, which substantially reduces the junction capacitance of the PIN diode. C_J will decrease slightly as additional reverse bias is applied until the "punch-through" voltage is reached. This is the voltage at which all free carriers have been removed from the intrinsic region, which is largely based on the purity of the intrinsic region semiconductor. Beyond the punch-through voltage there will not be substantial changes to the capacitance of the junction. This behavior is valid for frequencies above the dielectric relaxation frequency of the intrinsic region:

$$f > \frac{1}{2\pi\rho\kappa\epsilon_0} \tag{C.11}$$

With ρ being the resistivity of the semiconductor. The resistivity (purity) of the semiconductor strongly influence the lowest frequency that the diode will operate as desired. Below the cutoff frequency (which for a good diode is typically around a few MHz to a few tens of MHz) the reverse bias voltage should exceed the peak RF voltage.

APPENDIX D
CLASSES OF AMPLIFIER OPERATION

An amplifiers class of operation is determined by the amount of a sinusoidal input that results in conduction at the output of the amplifier. This is controlled by the quiescent point of the amplifier, which is a function of the DC gate and drain voltages. Generally, a higher bias voltage at the gate leads to a more linear amplifier. The basic linear classes of operation for amplifiers are referred to as A, AB, B, and C. This is in order from the highest bias to the lowest bias as shown in Figure D-1. We will consider each of these classes briefly to see how they are biased, and some of the ramifications of selecting a given class.

D-1 Linear Classes

Class A operation is obtained when the gate bias is set to roughly the middle of the linear region on the transfer curve of the MOSFET. This corresponds to $V_{GS} = V_{GS(A)}$ in Figure B-3, and results in the quiescent current $I_{DQ} = I_{DQ(A)}$ that is a large constant current of the order of a few amps for a high power device. This translate to a lower efficiency for the amplifier (approximately 25%) and substantially increased power dissipation even when no signal is being amplified. However, application of an RF input voltage (Figure D-2(a)) whose amplitude is less than $V_{GS(A)} - V_T$ ensures that the MOSFET never goes into the cut off region. This gives a conduction angle of 360° and the highest degree of linearity.

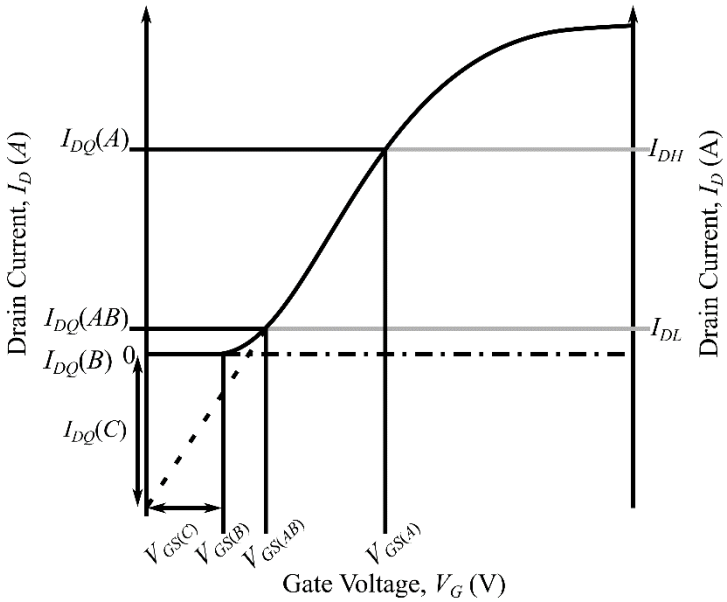


Figure D-1: Transfer curve with gate bias points for linear amplification.

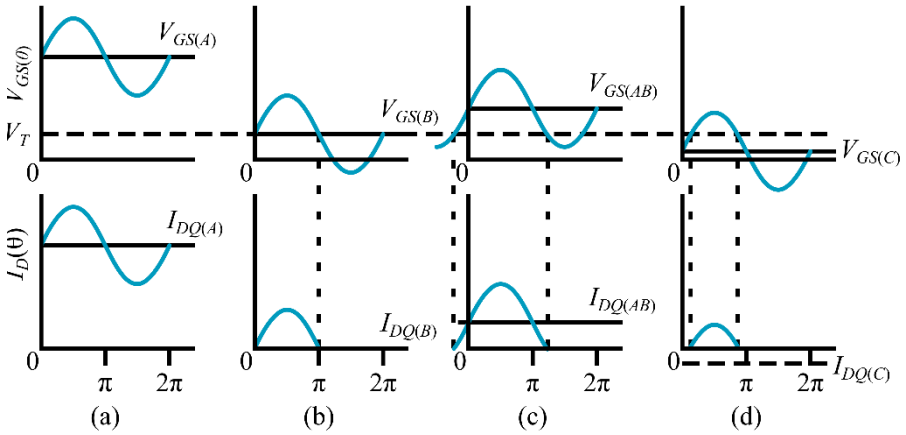


Figure D-2: Conduction of different classes of amplifiers. Upper half of the figure represents input RF voltage and lower half represents output current. The bias points of Class A (a); Class B (b); Class AB (c) and Class C (d) amplifiers are shown.

Class B operation occurs at a lower bias point when $V_{GS} = V_{GS(B)} = V_T$. Because the DC gate voltage is at the turn on voltage there is static current through the drain, that is to say $I_{DQ(B)} = 0A$. For this configuration V_{GS} is less than V_T for half the sinusoidal cycle as shown in Figure D-2(b), so the MOSFET is ON for only the positive half of the input voltage sinusoid (a conduction angle of 180°). The complete sinusoidal waveform on the output is obtained either by the use of a push-pull configuration in case of a broadband amplifier or by a tuned output network in case of a narrow-band amplifier. The result is lower linearity than a class A amplifier, but an much higher efficiency of around 78%.

Class AB is a compromise between these two, where $V_{GS(B)} < \left(V_{GS} = V_{GS(AB)}\right) < V_{GS(A)}$. The result is a non-zero quiescent current, $I_{DQ(AB)}$, that is lower than seen with a class A amplifier. Usually, $V_{GS(AB)}$ is set at the beginning of the linear portion of the transfer curve, so the resulting output is more linear than class C. This gives conduction angle is between 180° and 360°, as shown in Figure D-2(c) and an efficiency that is typically around 50%.

Class C amplifiers have the lowest bias point of the basic classes at $0 < V_{GS(C)} < V_T$ with $I_{DQ(C)}$, which is shown to be negative in both Figure D-1 and Figure D-2(d). However, in practice, $I_{DQ(C)} = 0A$ because it is below the threshold voltage of the device. The conduction angle for a class C amplifier usually is between 90° and 180°. The theoretical efficiency approaches 100%, though this can never be realized and a realistic efficiency is typically slightly better than class B. In exchange for the higher efficiency, the low conduction angle contributes to a loss of linearity.

In addition to these is are the class G and H amplifiers that modulate the drain voltage V_{DS}. Class G amplifiers use multiple supply rails of different voltages that are switched based on the amplitude of the signal. This reduces the amount of power dissipated in the device by using a lower V_{DS} when the envelope allows. Class G extends this idea by modulating V_{DS} as well as V_{GS} further improving the efficiency of the design. In general, the gate bias point could be set to match any of the previous classes of operation, though

class AB is perhaps the most commonly used. The gains in efficiency seen with class G and H come at the cost of higher design complexity and some loss of linearity. Additionally, some of the device parasitics will now vary along with the signal level, potentially adding complexity to the matching network design.

Linear class amplifiers represent the classical amplifier design, but are by no means the only option. Non-linear switching amplifiers have been developed, and in recent years have started to see applications in RF amplifier designs.

D-2 Switch Mode Amplifiers

Switch mode amplifiers are designed to operate with the output MOSFET in either the ON or OFF state, which is substantially different from the linear devices discussed until now. This significantly reduces the amount of power dissipated in the MOSFET since there is either no current flowing through it or minimal voltage dropped across the internal resistance. The final output is obtained by using a tuned output circuit that acts as a reconstruction filter, removing the higher order harmonics caused by switching. A diagram showing the basic operation of a class D amplifier is shown in Figure D-3. This group of amplifiers, which also includes classes E, F, and S, is highly efficient compared to linear class amplifiers. Increased efficiency is achieved at a cost to linearity and complexity. Only relatively recently have these designs become viable for RF amplifiers, and their design and use are an area of active research. Further details about the circuit and specific characteristics of each class of switching mode amplifiers may be found in current literature.[71] Because of the complexity, and relative scarcity of use in the RF domain, we will focus on linear class amplifiers.

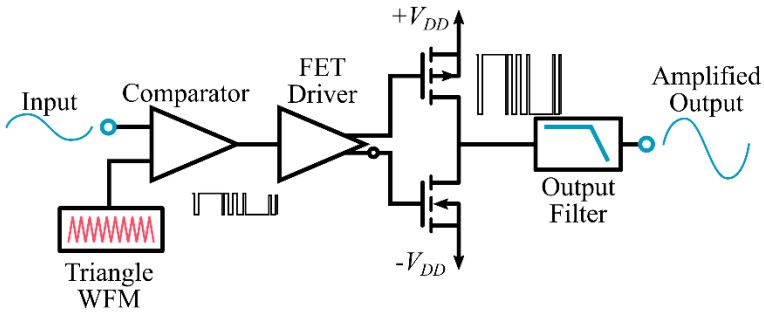


Figure D-3: The basic class-D amplifier operates in a switched mode. The input is converted into pulses that are used to drive the output FETs. This signal is then filtered to obtain an amplified version of the input.

APPENDIX E
RF SWITCHES AND PIN DIODE DRIVERS

E-1 Transmit/Receive Switch

In our application the coil is used in a transmit/receive mode, so must be alternately connected to the RF transmit chain during the excitation and to the receive system during the echo(s). The NMR receiver is a high sensitivity system, so a high degree of isolation between the transmit and receive port is needed. This both limits the amount of noise injected into the signal, and protects the Low Noise Amplifier (LNA) from damage. Both active and passive T/R switches exist and can be used, so a brief discussion of both will be made.

E-1.1 Passive T/R Switch

The basic passive T/R switch takes advantage of the non-linear properties of diodes in order to isolate and switch between the two ports. A pair of back-to-back Schottky diodes is put in series with the transmit port, and a pair of shunt back-to-back Schottky diodes is placed just before the receive port. These are separated by a $\lambda/4$ line. This circuit is shown in Figure E-1

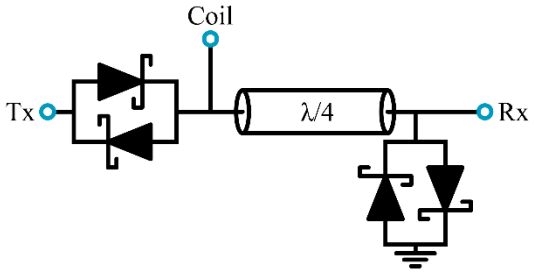


Figure E-1: The basic passive T/R Switch. Schottky diodes are used due to their fast recovery time, o the order of nSec, as opposed to the mSec that p-n diodes will often exhibit.

The switch is a “single pole, double throw” type, so has two operating modes. The first is when the transmit port is connected to the coil. In this mode, the high voltages of transmitter turns on the all of the diodes. This allows power to flow from the transmit port to the coil. The shunt diodes appear as a short, which is transformed to an open by the $\lambda/4$ section. This is shown in Figure E-2(a). When the transmitter is not producing high voltages then all of the diodes are unbiased and appear as open circuits, as in Figure E-2(b). The result is that the voltage induced by the spins can appear at the receive port. The transmitter is effectively disconnected by the series open circuit the diodes form.

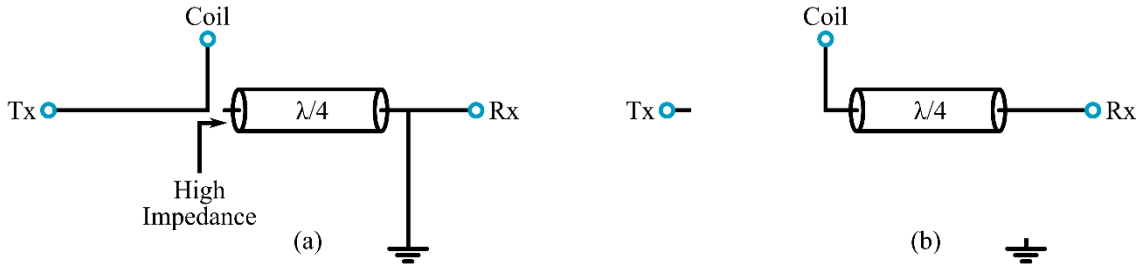


Figure E-2: The two operating states of a passive T/R switch. During transmit the diodes are biased on, producing the circuit in (a). At all other times the diodes are biased off as shown in (b).

While this technique works reasonably well there are two factors that limit the performance that can be obtained. First is that the circuit may not be reliable under very high powers. Diodes that switch quickly and handle large powers well are hard to obtain, so they are prone to failure during high power transmit pulses. The second is due to the non-zero turn-on voltage of the diodes. The desired behavior is that the transmit pulse instantly turns the diodes on and they act as perfect shorts. However, the diodes have some small but finite turn on voltage that will clip the lower power portions of the transmit pulse, as shown in Figure E-3. For simple excitations this should be a negligible effect, and could be compensated for. For 2D and 3D excitation, which a substantial portion of the RF envelope is at low powers, this can introduce much more significant distortions in the excitation.

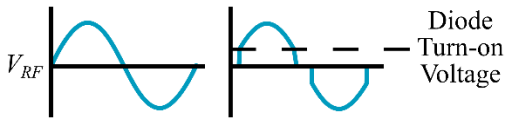


Figure E-3: The turn on voltage of the diodes has a clipping effect on the RF waveform. The result is a distortion of the desired excitation that is most pronounced when the average voltage of the RF signal is low. This is more like to be the case with multi-dimensional excitation.

E-1.2 Active T/R Switch

Active T/R switches use the same basic structure as the passive version, but exchange the Schottky diodes for PIN diodes that are biased for one state or the other. This has the advantage of being better able to handle high power transmit pulses and not clipping the low power signals. The tradeoff is that the PIN diodes used in the active switch must be driven into either a forward or reverse bias state to effectively switch the signal path without substantial distortion. The typical arrangement uses a forward bias current during transmit, and a reverse bias voltage during receive. Both of these should be large enough that the RF signals do not drive the diodes out of bias. Device physics and the power levels will dictate the needed level, but in general the bias does not actually need to be the magnitude of the RF signals.

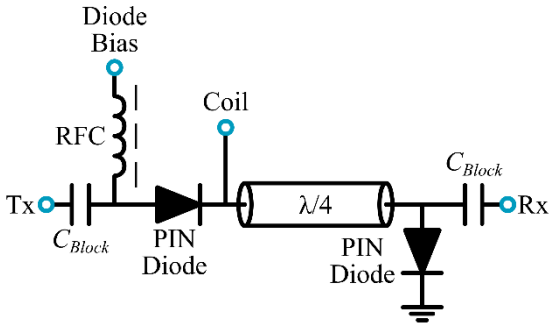


Figure E-4: The basic active T/R switch. It has a structure that is essentially the same as the passive circuit, but uses single PIN diodes, and requires a DC bias line in order to switch states.

E-1.3 Active T/R Switch Design

The switch design we use is based on a combination of the active and passive designs, with a lumped element phase shifter. The primary switch is a PIN diode design, with the addition of shut back-to-back diodes just before the receive port, as seen in Figure E-5. This adds a "clipper" type limiter to the output that reduces the chances of a failure that damages the receive chain. Microsemi UM9145 PIN diodes are used for the primary devices, and are biased to ~200mA forward for transmit and -48V reverse for receive. A 100mA forward bias should be sufficient to obtain a series resistance of around 0.2Ω, a heavier 200mA bias is set to allow for any variation in component values.

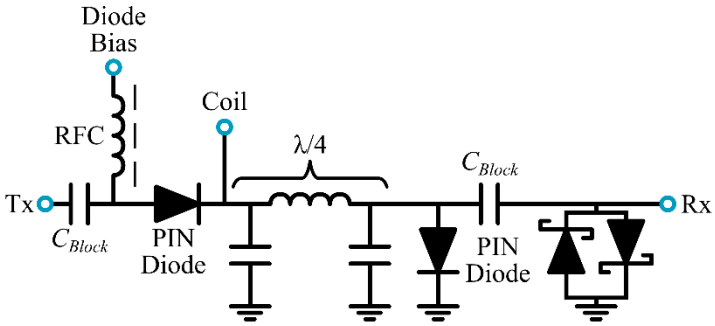


Figure E-5: The T/R switch implemented. The back-to-back Schottky diodes help to ensure a high level of isolation between the transmit and receive port. They also provide a passive fail-safe to prevent damage to the LNA. The lumped-element $\lambda/4$ quarter wave section is a more compact solution than a cable section.

One detail that has to be accounted for is the parasitic capacitances around the phase shifter. There is likely to be a few pF of stray capacitance, particularly on the receive side of the phase shifter. This is due to the mounting and land pads for the components. Some tuning in situ of an example board is needed to ensure the best isolation is obtained.

E-2 PIN Diode Driver

The active T/R switch design shown above requires a drive circuit that can bias the PIN diodes correctly. A bias supply of 200mA forward and -48V reverse is needed with an interface to a logic level signal. UM9415 PIN diodes themselves have approximately 0.75V forward drop, and upwards of 5pF junction capacitance when reverse biased. A totem-pole driver circuit is a relatively simple method of generating the bias for the diodes, shown in Figure E-6.

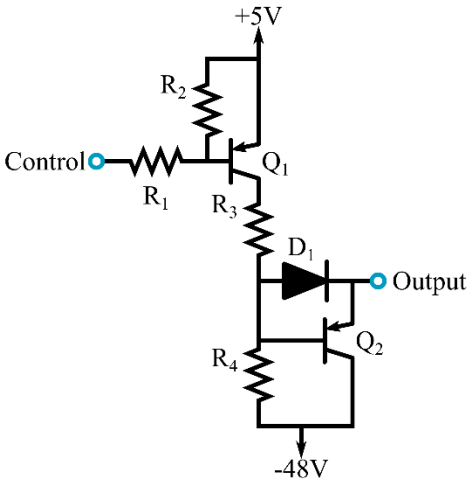


Figure E-6: A simple totem-pole driver circuit. A pair of PNP transistors can be used, with appropriate boot-strapping resistors in place. The top transistor is conducting when the PIN diode is forward biased, while the bottom conducts when the diode is reverse biased.

This circuit is designed to be controlled by a 5V logic signal, with a "high" control signal causing the diode to be reverse biased. R_1 and R_2 are set to be 150Ω and 300Ω respectively so that when the control signal is low Q_1 is biased to be on. This allows current to flow through R_3 and D_1. R_3 is selected to produce the desired current (200mA), so it is a 15Ω resistor. When the control signal is high, the Q_1 does not conduct, D_1 now allows Q_2 to enter the on state, so the output of the driver is the negative 48V. R_4 is a 3.9kΩ drain resistor that prevents charge accumulation at the base of Q_2.

Improved performance of the diode driver can be obtained with a slightly more complicated circuit. Additionally, a self-diagnostic circuit can be included that is used to ensure proper switching of the unit. Examples of these improvements can be seen in White[72] and Brorsson[73]

E-3 PIN Diode Blanking Switch

A slightly different application of the PIN diode switch is to use it as an inter-stage blanking switch for the amplifier chain. In this application the switch sits between the driver amplifier output and the final amplifier stage input. This switch is configured with a single series PIN diode, but uses a nearly identical driver design.

The two sub-circuits are integrated on a single PCB to save space and reduce cabling requirements. The diode driver section is identical to that shown in Section E-2, so will not be repeated here. The RF switch itself is somewhat different, so deserves some examination. The RF switch section, shown in Figure E-7, uses only a series diode but requires an additional DC current path through a RF choke. The result is that a lower isolation through the switch is obtained, but a simpler broad-band circuit is created.

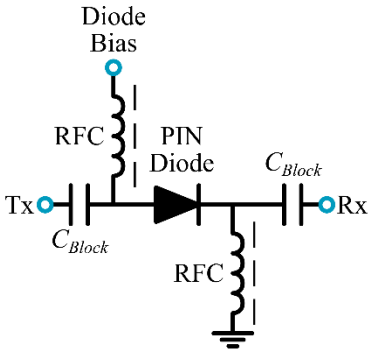


Figure E-7: The switch sub-circuit of the PIN diode blanking switch. A single series diode is used, with no tuned sections. The result is lower isolation, but smaller circuit.

APPENDIX F
MIXERS AND MODULATION

F-1 Mixer Theory

The RF mixer is one of the core technologies used in both transmit and receive systems. At its simplest, a mixer allows frequencies to be translated. While this may seem to be a trivial function, it is both highly useful and fraught with difficulty for the unwary designer. Real world mixers are not so neat and tidy as a simple translation in frequency. Appreciating the power of problems of mixing requires some look at the foundations of mixers and their implementations.

F-1.1 Ideal Mixer

The ideal mixer is a three port device that translates the input (IF) frequency to another frequency (RF) that is either the sum or difference of the local oscillator (LO) frequency. This is shown in Figure F-1, where an up-converting mixer would produce the $IF + LO$ product and a down converting mixer would produce the $IF - LO$ product. While this is the desired product.

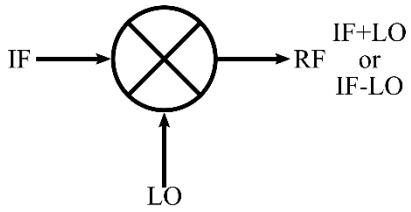


Figure F-1: The ideal mixer.

Mathematically, the mixer can be seen as the producing the product of two sinusoids (IF and LO). So, if we define these two signals as:

$$\begin{aligned} V_{IF}(t) &= V_{IF,max}\sin\left(2\pi f_{IF}t\right) \\ V_{LO}(t) &= V_{LO,max}\sin\left(2\pi f_{LO}t\right) \end{aligned} \tag{F.1}$$

Knowing that the product of two sinusoids is given by:

$$\sin(x)\sin(y) = \frac{1}{2}\left[\cos(x-y) - \cos(x+y)\right] \tag{F.2}$$

We can see that the mixer product would be give by:

$$V_{IF}\cdot V_{LO} = \frac{V_{IF,max}V_{LO,max}}{2}\left[\cos\left(2\pi\left[f_{IF} - f_{LO}\right]t\right) - \cos\left(2\pi\left[f_{IF} + f_{LO}\right]t\right)\right] \tag{F.3}$$

So, we see that the resulting output is the sum and difference of the frequencies of the LO and IF inputs. A appropriate filter can be used to select for the desired frequency, producing either the up-converted or down-converted product. Of course, the ideal mixer cannot be realized, and additional mixing products will always be introduced. The exact products and their strength will depend on the implementation, so it's worth considering a few of the common mixer designs.

F-1.2 Single Diode Mixer

The most basic implementation of a mixer is a single diode, as shown in Figure F-2. The assumption is made that the magnitude of the IF voltage is substantially smaller than that of the LO voltage. In this way the diode is biased by the LO voltage and not the IF. The resulting output spectrum is a sum of products of the two input spectrums.

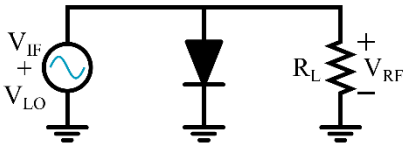


Figure F-2: The basic single diode mixer.

An ideal diode, with an I-V curve that has infinite slope above the turn on voltage, would act as a simple switch. The LO signal would drive the switch into and out of conduction so that the frequency content could be seen as the Fourier series of a square wave, which is:

$$F(t) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(n\pi t f) \tag{F.4}$$

Importantly, this is made up of *only the odd terms*. Combining this with equation (F.3) we see that the frequency spectrum will contain the sums and differences of the IF frequency and all odd harmonics of the LO frequency, that is:

$$f_{RF} = nf_{LO} \pm f_{IF} \quad : \text{n is only odd integers} \tag{F.5}$$

Realistic diodes do not produce this, since their slope is finite. Instead, they operate in a square law regime, which is to say that the resulting frequency content of the LO an IF are no longer simply the odd harmonics. Additionally, the IF frequency can no longer be ignored as it traverses the transfer function of the diode, so we have:

$$f_{RF} = nf_{LO} \pm mf_{IF} \quad : \text{n,m ALL integers} \tag{F.6}$$

The resulting output is far from the ideal single frequency output. Instead, it has many spurs, some of which will fall near the desired product. The result is that high quality filters are needed to obtain only the desired products. This situation is shown in Figure F-3

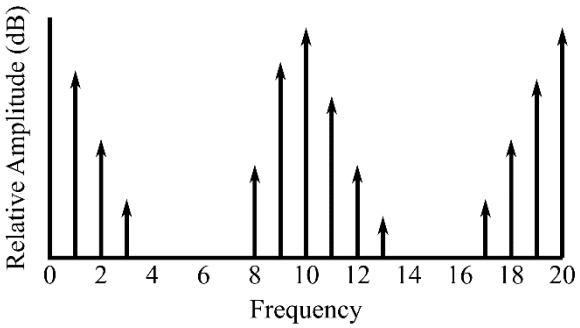


Figure F-3: Spectral output of a single diode mixer.

A second concern is the need to obtain a combined IF and LO signal. These two signals will typically be at very different frequencies, so there is a need for additional circuitry to combine them into the feed to the diode.

F-1.3 Balanced Mixer

An improvement on the single diode design is the balanced mixer. This design takes advantage of the behavior of a quadrature hybrid to simultaneously generate isolated IF and LO ports, as well as produce a balanced drive for the mixer. Of course, a balanced mixer must use two diodes in order to function correctly.

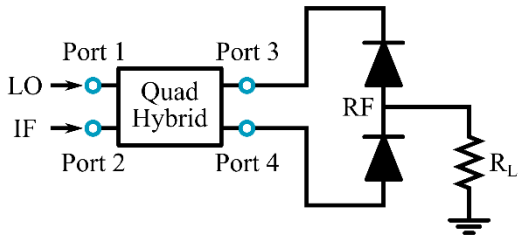


Figure F-4: A simplified balanced mixer.

This has the additional advantage of reducing the magnitude of the even harmonics of the LO signal. So, we simplify the spectral content to:

$$f_{RF} = nf_{LO} \pm mf_{IF} \quad : \text{n odd, m all} \tag{F.7}$$

So the spectrum is reduced by roughly 50%, with power being put into the remaining products. This yields an output that has fewer spurs, and a mixer with lower conversion loss. Overall, the single balanced mixer is a substantial improvement over the simple single diode mixer, but yet further gains can be had.

F-1.4 Doubly Balanced Mixer

The single balanced mixer uses two diodes with balanced drive signals, and consequently solves many problems associated with the single diode mixer. The doubly balanced mixer expands on this idea by adding a balanced output. The resulting structure is essentially a ring diode mixer with two quad hybrids, as shown in Figure F-5. This structure has the advantage of suppressing the even harmonics of both inputs, further reducing the spurs found in the spectrum. The result is an output spectrum with the frequency content of:

$$f_{RF} = nf_{LO} \pm mf_{IF} \quad \text{:n,m odd} \tag{F.8}$$

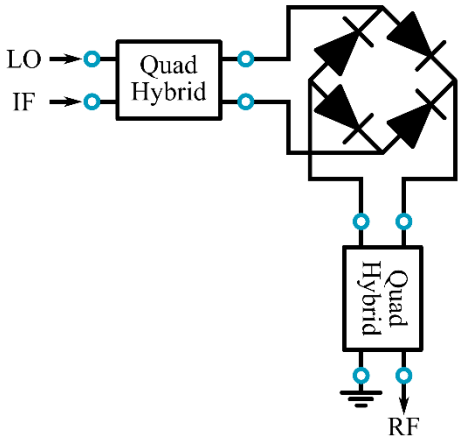


Figure F-5: Doubly balanced mixer.

This further reduces the conversion loss of the mixer. The result is that the spectrum has 75% of the frequency spurs removed compared to the single diode mixer, and substantially improved loss measurements for a passive device. Further improvements can be made using a “doubly double balanced mixer”, also known as a “triply balanced mixer”, which is simply an expansion on the same concept. Additionally, most integrated circuit mixers do not use diodes, since a pn junction diode is not effective at RF. Instead, a diode mixer uses Schottky diodes, and an IC mixer will often use a FET based design like the Gilbert cell shown in Figure F-6. The fundamental concepts transfer, though the exact implementation is different.

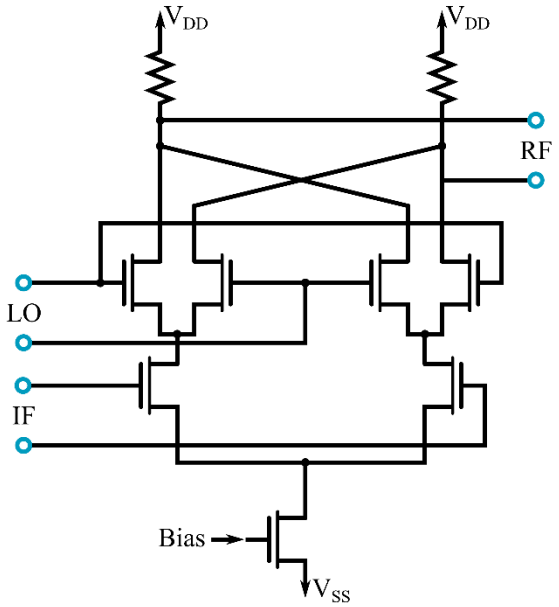


Figure F-6: A simplified Gilbert Cell mixer. The design uses CMOS process to generate a doubly balanced mixer that is suitable for integration onto an IC. The general behavior is similar to the ring-diode based design, though the exact performance will very. This design removes the need to use a Schottky diode, making it more suitable for integration.

F-2 RF Modulation Principles

In the simplest terms, modulation is the variation of some parameter over time. The MR transmit system is primarily concerned with modulating the amplitude and phase of the RF. Again, this appears to be a trivial task, but the complexity inherent in it quickly becomes apparent when implementing a real world system.

F-2.1 Amplitude Modulation

Amplitude modulation is one of the foundational modulation techniques which varies the RF envelope magnitude with time. The result is an RF waveform defined by

$$RF(t) = V_{env}(t)\sin(2\pi t) \tag{F.9}$$

Where $V_{env}(t)$ is the time varying envelope of the signal. An simple example of amplitude modulation is shown in Figure F-7. One interesting point to note is that a negative amplitude envelope will result in a 180° phase shift.

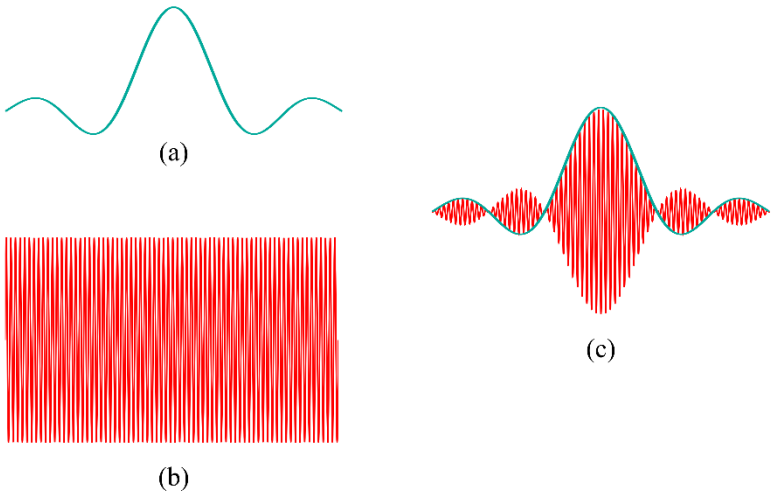


Figure F-7: A simple example of amplitude modulation. The desired envelope (a) is shown at "baseband". The base RF is a simple sinusoid of constant envelope amplitude (b). The result of amplitude modulation is shown in (c) with the envelope overlaid on the resulting RF. Note that a negative envelope translates to a 180° phase shift.

A complementary view of this is the frequency domain of these signals. The RF will, ideally, be a delta function at the center frequency (this is, of course, some spread but we will ignore that here). The baseband envelope will have some finite frequency content. For the shown waveform, a truncated sinc, the frequency would be roughly a rectangular frequency spectrum. The modulated waveform will have a spectrum that is the spread of the baseband waveform centered on the RF waveform frequency.

F-2.2 Phase Modulation

The second modulation scheme used in MRI is phase modulation. The basic concept is the same as a for amplitude modulation, thought in this case the modulation is a phase shift from nominal at each time point. Typically the phase shift would not be cumulative, so that the signal can be described by:

$$RF(t) = V_0 \sin\left(2\pi t + \phi(t)\right) \tag{F.10}$$

One way to think of a sine wave is that it move through phase in a linear fashion. That is, for a given frequency that phase changes with time as:

$$\phi(t) = \phi_0 + 360\, ft \tag{F.11}$$

This assumes that the phase is measured in degrees, frequency in hertz, and time in seconds. So, the sinusoid will form a linear ramp in when comparing phase vs. time, while it is clearly non-linear in amplitude vs time. These basic concepts are shown in Figure F-8.

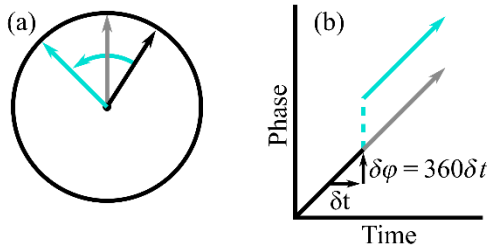


Figure F-8: Phase advancement over time of a sinusoid. A polar representation of phase advancement is shown in (a) where the black arrow is the initial phase, the gray arrow is the expected phase at the next time step, and the blue arrow is the realized phase if the time point is advanced in phase. A plot of the phase vs. time of a sinusoid is shown in (b). The colors coordinate with those in (a), however now we see that a phase step is propagated to all following time points.

F-2.3 Phase and Amplitude Modulation

Generally, for MRI both the phase and amplitude need to be modulated simultaneously. For an RF waveform the phase and amplitude are orthogonal, so this does not present any theoretical problem, but constructing an effective modulator does pose some difficulties. A naive approach is to simply cascade a variable attenuator and variable phase shifter to achieve the desired modulation. This can be thought of as a Cartesian modulation scheme. It is possible to construct such a device, but is relatively expensive and difficult. A voltage controlled attenuator can be constructed with PIN diode circuit.

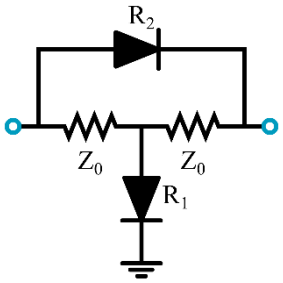


Figure F-9: Variable attenuator using PIN diodes. PIN diodes act as current controlled resistors at RF, so can be used in a bypassed Tee-network to construct an attenuator. A match at both ports can be obtained by maintain the correct ratio between R_1 and R_2. Bias and drive circuitry is not shown for simplicity.

A phase shifter can also be constructed using PIN diodes, but unlike the attenuator they are not continuously variable. The design will use switched elements in order to adjust the phase by some amount. One example implementation is a loaded-line phase shifter. In this design there are a series of phase-shifting blocks that can be switched in an out. Each block is built from two susceptances that are spaced by $\lambda/4$.

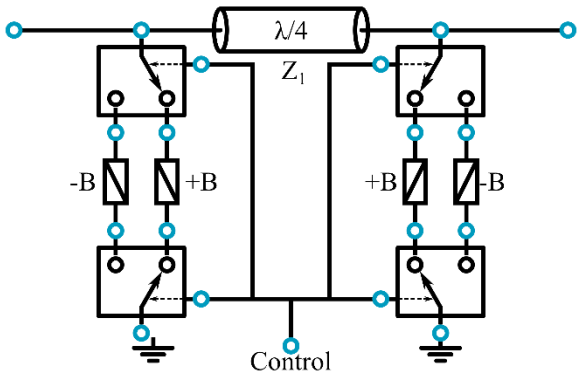


Figure F-10: Single cell of a loaded-line phase shifter. The switches would be formed using a solid state device (e.g. PIN diode), while the susceptances and impedance of the $\lambda/4$ section are based on the desired phase shift.

There are a few problems with these solutions. The first is linearity of the attenuator. Generally, a PIN diode attenuator will not be inherently linear relative to the control input. This adds complexity to the design. The phase shift network will typically be very large, especially at MR frequency of tens to hundreds of MHz. Finally, there is substantial complexity that is not shown in the example circuits due to the driving requirements of the PIN didoes. Many diodes would need to be controlled, and for the attenuator they need a specific current ratio. Ultimately, this is a very difficult system to implement. Alternative modulation systems can be constructed using the mixers shown in section F-1.

APPENDIX G
MATCHING NETWORK BASICS

The matching network design, along with biasing, make up the core of RF amplifier design. Matching networks are used to transform impedances and generally attempt to minimize power loss and reflection. Amplifiers will also not achieve their desired performance if they are not properly matched. This could manifest as low output power, or oscillation in some cases. The design of matching networks has been extensively covered in existing RF and microwave literature,[42], [74]–[77] so we will not attempt to fully describe it here. Instead, we will offer an overview that highlights some important features.

G-1 Overview of Matching Networks

The fundamental purpose of a matching network is to transform the impedance of a device or system from one value to another, as shown in Figure G-1. This may be to minimize reflected power, obtain the minimum noise figure for a pre-amplifier, obtain maximum power output for a power amplifier, or some other condition.

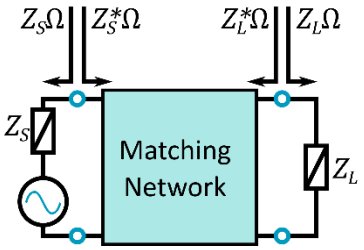


Figure G-1: The basic conjugate matching network will transform a load impedance (Z_L) to the complex conjugate of the source impedance (Z_S). This conjugate match will typically minimize the power reflected from the load.

We can consider matching networks to be passive and lossless for now, as this is a reasonable approximation of their behavior. While the passivity of the network is absolute (they do not generate power, only transform it), real networks are lossy as all components will dissipate some amount of power. Good quality, high Q reactive components will limit this problem and the use of resistive elements should generally be avoided.

The use of reactive elements in the matching network means that it will exhibit a frequency dependent response. A design frequency is used, and the network will have some bandwidth over which an acceptable match is obtained. A common "acceptable match" is to have a Voltage Standing Wave Ratio (VSWR) of 1.5:1, which translates to a Return Loss (RL) of 14dB. Based on the bandwidth we can divide matching networks into either narrow band (10% bandwidth or less) or broadband (above 10% bandwidth).

Narrow band designs can be useful for MRI, which is interested in ^{1}H almost exclusively. NMR, on the other hand, virtually dictates the use of broadbanded systems.

G-2 Narrow-Band Matching Networks

MRI is typically concerned with ^{1}H, and specially water, which has a very narrow bandwidth. An excitation pulse would not be expected to exceed roughly 200kHz, which on a 128MHz system corresponds to a bandwidth of approximately 0.15%. This is well below 10% bandwidth, making it practical to use narrowband matching techniques. The simplest versions use two or three lumped element capacitors and/or inductors. These are arranged in one of the networks shown in Figure G-2.

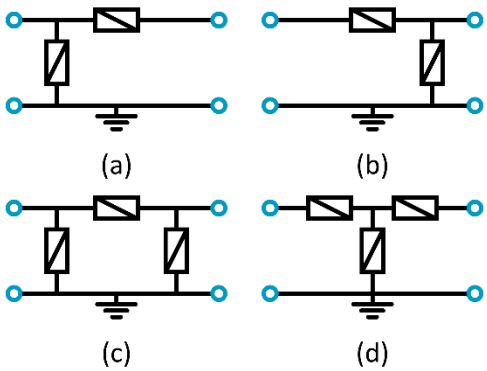


Figure G-2: The elemental matching network structures. The L-networks (a) and (b) are able to match only some impedances. The Pi and Tee networks (c) and (d) are able to match all impedances. The different structures, and whether a given element is capacitive or inductive, will yield different component values. This may make some options difficult to implement.

Each of these L, Tee and Pi networks may be high-pass (series capacitor, shunt inductor) or low-pass (series inductor, shunt capacitor), and in some particular cases may use only capacitive or inductive elements. Many design techniques can be used for selecting component values, but one helpful tool is the Smith chart, shown in Figure G-3.[78]–[80] This graphical tool can be used for both visualizing and designing matching networks, and is used extensively in RF circuit design and analysis.

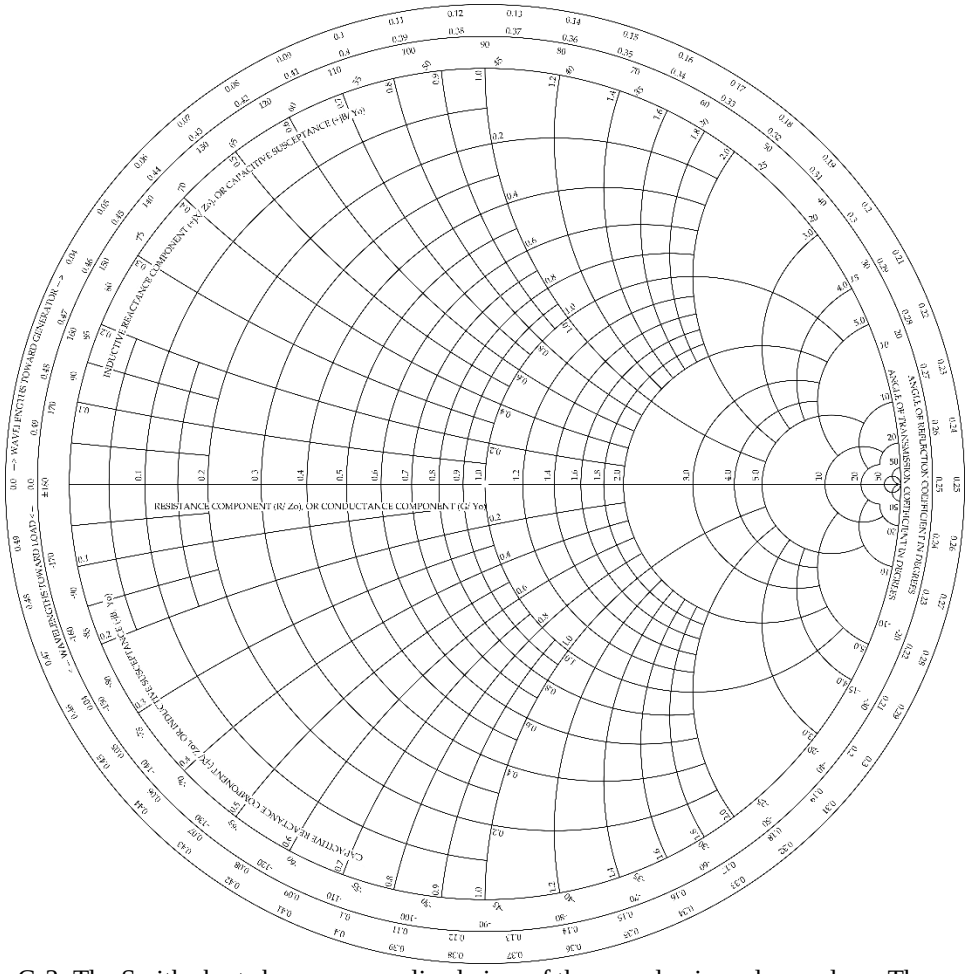


Figure G-3: The Smith chart shows a normalized view of the complex impedance plane. The contours represent constant resistance and constant reactances. Elements of a matching network will "move" a point on this plane in predictable ways, making it useful for design as well as displaying information.

In addition to lumped elements, transmission line can be used to match by attaching appropriately sized stubs, either shorted or open. While this technique can be limited for MRI and NMR due to the lower frequencies (and consequently longer transmission line) it has seen application as a way to replace lumped elements.[19], [62] One advantage to this method is that well designed microstrip stubs can mitigate problems with coupling between the input and output of an amplifier. This can occur due to flux coupling between inductors, and may lead to oscillation of the amplifiers.

Ultimately, these techniques will only be able to produce a relatively narrow bandwidth. For MRI, where only one frequency is of concern, this has the benefit of rejecting out of band noise. When additional nuclei are of interest, which is the case with NMR a narrow band solution becomes impractical. In this case, we need to consider a broadband design.

G-3 Broadband Matching Networks

Amplifiers for NMR have the additional complication that they need to be able to excite multiple different species, with each specie at a different frequency. If we consider the low band of a 400MHz system, then the exciter need to used on nuclei ranging ^{15}N(40.5MHz)to ^{31}P(162MHz) which equates to a bandwidth of 200%. While different amplifiers tuned for each frequency are possible, this quickly becomes large, expensive and impractical. A better solution is to use a single amplifier which has been designed to operate at all the relevant frequencies, that is to say a broadband amplifier. While conceptually simple, the actual design of a broadband matching network can be quite complex.

Unfortunately, even a cursory look at this topic far exceeds what can be covered here. In lieu of a poor treatment here, there are many resources available covering topics like tapered transmission lines,[42], [81] multi-section matching techniques,[56], [82] numerical design techniques,[83] the fundamental limits of broadband systems.[84], [85]

APPENDIX H
S-PARAMETERS

The basic performance of RF networks is often described using some network parameter set, with scattering parameters, or *s*-parameters, being one of the more common. Essentially, these parameters describe how power incident on a given port generates power on other ports. They are in common enough use that it is worth understanding their basic formulation, application, and pit falls when dealing with power amplifiers and array coils.

H-1 Overview of *s*-Parameters

S-parameters relate the power incident on some port to the power leaving some other port. The simplest case is of the single port device, shown in Figure H-1. In this case the power leaving the port (b) is related to the power incident on the port (a) by the value of S_{11} as:

$$b = aS_{11} \tag{H.1}$$

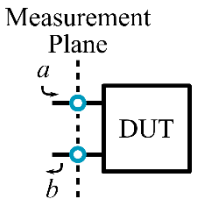


Figure H-1: The basic S11 measurement. The power entering the port is notated as a, leaving b, and they are related by the value of S_{11}. All of these values can be complex, that is have both amplitude and phase. Finally, these measurements are taken and definition is valid only at the measurement plane as shown.

The notation of *s*-parameters is that the first number in the subscript is the port being measured at, and the second is the port being excited. So S_{21} is the measurement of power leaving port 2 with power incident on port 1, as shown in Figure H-2.

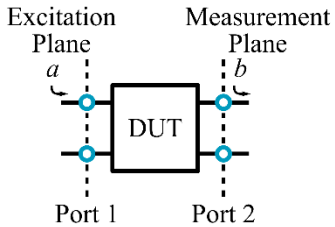


Figure H-2: The basic S_{21} measurement. Note that in this case the excitation occurs on a separate port from the measurement.

This leads to a full definition of the 2-port *s*-parameters as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{H.2}$$

There are a few important but implicit properties of *s*-parameters. First is they are a linear measurement. It is assumed that the behavior of the device does not change based on input power. Second is that they are a black-box measurement. That is to say, they are defined at the measurement planes and give no direct information about what occurs within the device under test. Both of these have important implications for amplifier and array coil measurements.

H-2 *s*-Parameters and Amplifiers

Amplifier performance is typically measured using *s*-parameters, but his presents some difficulties and introduces some problems to the measurements. The gain, measured as S_{21}, assumes that the amplifier is linear, but high power amplifiers are known to never be truly linear. The degree of error varies based on the class of operation of the amplifier. Over the input power range the gain of the amplifier will actually change. All amplifiers will experience gain compression at higher powers where the magnitude of the gain decreases. Gain may also drop off at lower power for less linear classes of operation. This manifests as harmonics appearing in the output of the amplifier.

This can make it difficult to actually measure the output power using a network analyzer, as the harmonics will actually interfere with the measurement of the primary frequency. Further, a network analyzer will no indicate if harmonics are present. All measurements of the power amplifier with a network analyzer must be validated with a time-domain o-scope measurement or another measurement that does not assume linearity.

H-3 *s*-Parameters and Arrays

The *s*-parameter measurements are only valid, and only contain information about the power passing into and out of the DUT. No information is given about the voltages and currents present inside of the DUT. What this means is that S_{21} between two elements does not necessarily provide an accurate view of coupling that we care about. Instead, it only tells about the *port* coupling. No information is provided about the currents present on the individual elements. This information must be extracted using some other method (e.g. pickup loops measuring the field produced by the element.)

APPENDIX I
B_1 MAPPING

A brief discussion of Bloch-Siegert B_1 mapping, and Double Angle Method (DAM) tip angle measurement is included. The topic of measuring B_1 /tip angle is important and well discussed in literature[64], [86]–[88], what is included here is a brief overview.

I-1 Double Angle Method

The Double Angle Method takes advantage of a linear approximation of the signal equation, which is approximately correct when tip angles are small. Two images are taken with approximate tip angles of α and 2α with all other parameters held the same. Additionally, a long TR should be used so that full relaxation is achieved between repetitions. So then we have

$$\begin{aligned} I_1 &\propto M_0 \sin(\alpha) \\ I_2 &\propto M_0 \sin(2\alpha) \end{aligned} \tag{I.1}$$

Where I_1 and I_2 are the acquired image intensities. Using the relationship $\sin(2\alpha) = 2\sin(\alpha)\cos(\alpha)$ we can reduce equation (I.1) to

$$\alpha = \arccos\left(\frac{S_2}{2S_1}\right) \tag{I.2}$$

Thus, by acquire two image of roughly 20° and 40° we can compute the tip angle at all points in the image. This method was used to validate the B_1 pattern obtained from the four channel transmit array in the MRSL. An example tip angle map is shown in Figure I-1. An example implementation that generated the shown figure is in section I-2.

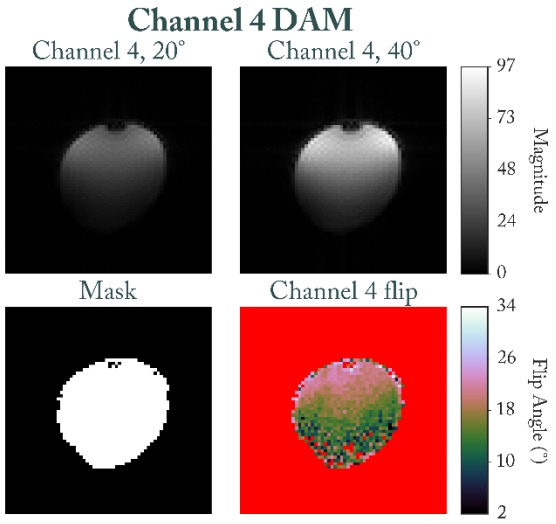


Figure I-1: Tip angle map computed using the DAM. The two images used are shown in the top row. A mask is generated to remove noise caused by low signal level (bottom right) and the flip angle map is shown at bottom left. Red indicates invalid regions.

I-2 A Python Implementation of the DAM

```
import numpy as np
import numpy.ma as ma

import matplotlib.pyplot as plt
import matplotlib.font_manager as fm
from matplotlib import ticker
from matplotlib.gridspec import GridSpec

from nmrglue import varian

import utils as ut
import filters as filt

#**************************************************************************
*****
#Import images and construct DAM flip angle map
#**************************************************************************
*****


#import the "20 degree" tip image
dat_20_dic, dat_20 = varian.read('bc_20deg.fid')
dat_20_im = ut.recon(dat_20)

#import the "40 degree" tip image
dat_40_dic, dat_40 = varian.read('bc_40deg.fid')
dat_40_im = ut.recon(dat_40)

#generate the mask based on the magnitude image
mask = filt.mask(dat_40_im, np.mean(np.abs(dat_40_im))*0.8)

#construct a masked flip-angle array
```

```
fa_im = ma.masked_array(np.arccos(np.abs(dat_40_im) / (2 *
np.abs(dat_20_im))),
                        mask)
fa_im.mask = np.invert(fa_im.mask)

#**************************************************************************
*****
#Configure plotting options to make it a little prettier
#**************************************************************************
*****

#configure a color map with an "error" color
colormap = plt.cm.cubehelix
colormap.set_bad('r', alpha = 1)

#a better ticker?
tick_loc = ticker.LinearLocator(numticks=5)
formatter = ticker.FormatStrFormatter('%d')

#better font?
fontpath = 'C://Windows//Fonts//'
heading = fm.FontProperties(fname=fontpath+'ACaslonPro-Bold.otf').copy()
heading.set_size(20)

heading2 = fm.FontProperties(fname=fontpath+'ACaslonPro-
Regular.otf').copy()
heading2.set_size(16)

heading3 = fm.FontProperties(fname=fontpath+'ACaslonPro-
Regular.otf').copy()
heading3.set_size(12)

#Set up the axis grid
gs = GridSpec(100, 100, bottom=0.1, left=0.1, right=0.9, top=0.9)

#**************************************************************************
*****
#Generate the figure and save it out.
#**************************************************************************
*****
fig = plt.figure(frameon=False, facecolor='white', figsize=[6,5], dpi=90)

fig.suptitle('Birdcage DAM', fontsize = 'large', fontproperties=heading)

ax20 = fig.add_subplot(gs[3:48,0:45])
ax20.set_axis_off()
plot20 = ax20.imshow(np.abs(dat_20_im), cmap='gray', aspect=1)
ax20.set_title('Birdcage, 20°', fontproperties=heading2)
ax20.set_anchor('SE')

#cbar20 = plt.colorbar(bc_20plot)
#cbar20.set_label('Magnitude', rotation=270, labelpad=20)

ax40 = fig.add_subplot(gs[3:48,50:95])
ax40.set_axis_off()
plot40 = ax40.imshow(np.abs(dat_40_im), cmap='gray', aspect=1)
ax40.set_title('Birdcage, 40°', fontproperties=heading2)
ax40.set_anchor('SW')
```

```
#colorbar for top row
cbar_ax = fig.add_subplot(gs[3:48, 90:95])
cbar40 = plt.colorbar(plot40, ax=ax40, cax=cbar_ax)
cbar40.set_label('Magnitude', rotation=270, labelpad=20,
                 fontproperties=heading3)
cbar40.locator = tick_loc
cbar40.formatter = formatter
cbar40.ax.set_yticklabels(cbar40.ax.get_yticklabels(),
fontproperties=heading3)
cbar40.update_ticks()

clims = plot40.get_clim()
plot20.set_clim(clims)

maskax = fig.add_subplot(gs[55:100,0:45])
maskax.set_axis_off()
maskplot = maskax.imshow(mask, cmap='gray', aspect=1)
maskax.set_title('Mask', fontproperties=heading2)
maskax.set_anchor('SE')

faax = fig.add_subplot(gs[55:100, 50:95])
faax.set_axis_off()
faplot = faax.imshow(fa_im*180/np.pi, cmap=colormap, aspect=1)
faax.set_title('Birdcage flip', fontproperties=heading2)
faax.set_anchor('SW')

#colorbar for top row
cbar2_ax = fig.add_subplot(gs[55:100, 90:95])
cbarfa = plt.colorbar(faplot, ax=faax, cax=cbar2_ax)
cbarfa.set_label('Flip Angle (°)', rotation=270, labelpad=20,
                 fontproperties=heading3)
cbarfa.locator = tick_loc
cbarfa.formatter = formatter
cbarfa.ax.set_yticklabels(cbarfa.ax.get_yticklabels(),
fontproperties=heading3)
cbarfa.update_ticks()

fig.savefig('pngs/bc_dam_2040.png', pad_inches=0)

plt.show()
```

I-3 Bloch-Siegert B_1 Mapping

The Bloch Siegert B_1 mapping technique takes advantage of the Bloch-Siegert phase shift induced by off resonance RF[89]. It is a phase shift based method that uses a quasi-uniform excitation to achieve the needed signal level to acquire the B_1 map. After the initial excitation an off-resonance RF pulse is used to induce a phase shift without causing additional excitation. The phase shift is dependent on the magnitude of B_1, so that a B_1 map can be generated. The method does require a modified pulse sequence as shown in Figure I-2.

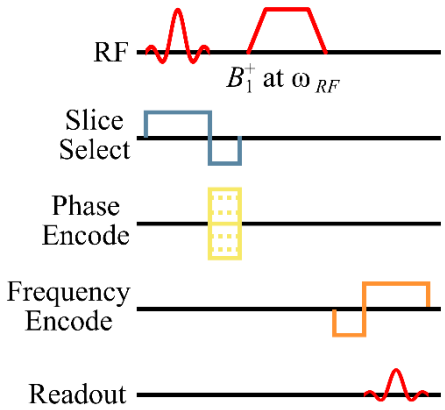


Figure I-2: Bloch-Siegert B_1 mapping sequence. This version is based on a GRE sequence. A similar modification can be made to a SE sequence.

The off resonate pulse will be at ω_{RF} offset from the center frequency around 4kHz. Any background phase can be removed by taking the difference between these two images. The phase shift induced by the BS pulse is found as:

$$\phi_{BS} = \int_0^T \frac{\left(\gamma B_1(t)\right)^2}{2\omega_{RF}(t)}\,dt = B_{1,peak}^2 \int_0^T \frac{\left(\gamma B_{1,normalized}(t)\right)^2}{2\omega_{RF}(t)}\,dt = B_{1,peak}^2 \times K_{BS} \tag{I.3}$$

Where K_{BS} is measured in rad/G^2/mSec, $B_{1,peak}$ is the peak magnitude of the B_1 field, and $B_{1,normalized}$ is the normalized B_1 waveform. K_{BS} can be found as:

$$K_{BS} = \int_0^T \frac{\left(\gamma B_{1,normalized}(t)\right)^2}{2\omega_{RF}(t)}\,dt \tag{I.4}$$

The BS pulse is typically shaped, with the Fermi pulse being a reasonable choice. This pulse can be defined as

$$RF(t) = \frac{e^{j2\pi\omega_{RF}t}}{1+e^{(|t|-\mu)/k}} \tag{I.5}$$

Where $RF(t)$ is the RF envelope, μ and k are shaping factors, ω_{RF} is the off resonance in Hz, and t is the time in seconds, centered on 0. Reasonable values are $\omega_{RF} = 4kHz$, $\mu = 1.5\times10^{-3}$, $k = 2.5\times10^{-4}$, and a pulse length of 4mSec. It's a good idea to apodize the envelope with a Hamming window, or similar. The result of the Bloch-Siegert B_1 mapping is a magnitude B_1 map, like the one shown in Figure I-3.

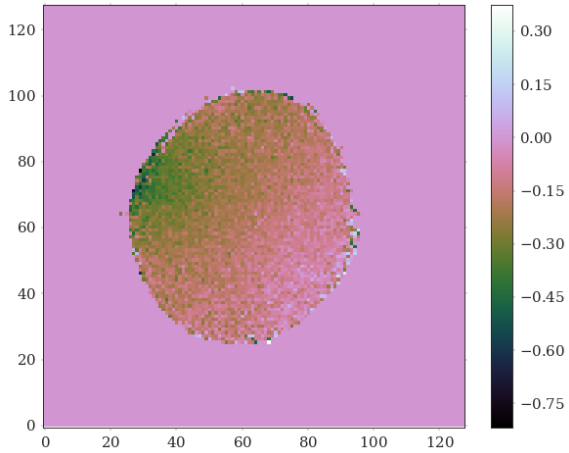


Figure I-3: Bloch-Siegert magnitude B_1 map. The phase of the B_1 must be obtained from a set of GRE by taking the difference of the phase with a single reference coil (e.g. subtracting the phase of coil 1 from all others). This is then added to the magnitude B_1 map from the Bloch-Siegert method.

I-4 Python Implementation of Bloch-Siegert B_1 Mapping

The design of a Fermi pulse can be done using a function such as this:

```
    def fermi(T, dt, wRF, mu, k):
        """
        Designs a Fermi pulse apodized with a Hamming window.

        The function implemented is rf(t)=exp(2*j*pi*wRF*t)/(1+exp((|t|-mu)/k).

        Parameters
        ----------
        T : float
            The total length of the RF pulse in seconds.
        dt : float
            The dwell time of each point, inverse of sampling rate.
        wRF : float
            The off-resonance of the pulse in rad/Sec.
        mu : float
            The first shaping factor of the Fermi function.
        k : float
            The second shaping factor of the Fermi function.

        Returns
        -------
        rf : 1D array
            The envelope of the RF pulse.
        """
        npoints = T / dt  # Compute the number of points
        t = np.linspace(-(T / 2), T / 2, npoints)  # Calculate the time points
        # This is the actual Fermi function
        rf = np.exp(1j * 2 * np.pi * wRF * t) / (1 + np.exp((np.abs(t) - mu) /
    k))
        # Apodize with a Hamming window
        rf = np.hamming(len(rf)) * rf
        # Retur the final waveform
        return rf
```

This generates a Fermi pulse windowed with a hamming window. The calculation of the value K_{BS} can be accomplished using a numerical integration routine. So, a simple version is to use a trapezoid integration, as in this function.

```
    def kBSCalc(wfm, dt, wRF):
        """
        Computes the value of K_BS for Bloch-Siegert B1 mapping.

        The waveform wfm with off-resonance wRF and dwell time dt is
    numerically
        integrated using the trapazoid rule to obtain K_BS.

        Parameters
        ----------
        wfm : array of floats
            The RF pulse.
        dt : float
            The dwell time of each point, inverse of sampling rate.
        wRF : float
            The off-resonance of the pulse in Hz.

        Returns
        -------
        K_BS : float
            The phase accmulation metric in rad/G^2.
        """
        temp = wfm / np.max(wfm)  # Normalize the waveform
        # Precompute the internal function of the integral
        temp = ((2 * np.pi * 42.576 * temp) ** 2) * 10 / (2 * wRF)
        # Integrate and return the value
        return sp.integrate.trapz(temp, dx=dt)
```

APPENDIX J
MODULATOR INTERFACE CONNECTORS

J-1 Modulator Board Connectors

J-1.1 Primary I/O

The main interface connector is through a male HD-68 connector. This aggregates digital and analog I/O using the pin-out of the National Instruments (NI) PXI-7853R connector.

Pin Number	Name	Description of Use
1,35	+5V	+5V supplied by PXI-7853R, not used
2-9,14-34,56,58,61,64,67	GND	Tied to board ground plane
10	DIO8	Control for RF switch 1 (SW1)
11	DIO10	Control for RF switch 3 (SW3)
12	DIO12	Spare Line (DIO12)
13	DIO14	Spare Line (DIO14)
36	DIO0	Clock for I^2C (SCL)
37	DIO1	Data for I^2C (SDA)
38	DIO2	Data for attenuator 1 (SD1)
39	DIO3	Data for attenuator 2 (SD2)
40	DIO4	Data for attenuator 3 (SD3)
41	DIO5	Data for attenuator 4 (SD4)
42	DIO6	Clock for attenuators (CLK)
43	DIO7	Latch for attenuators (LE)
44	DIO9	Control for RF switch 2(SW2)
45	DIO11	Control for RF switch 4 (SW4)
46	DIO13	Spare Line (DIO13)
47	DIO15	Trigger line (TRIG)
48	AO7+	Quadrature waveform for Ch.4 (Q4)
49	AO6+	In-phase waveform for Ch.4 (I4)
50	AO5+	Quadrature waveform for Ch.3 (Q3)
51	AO4+	In-phase waveform for Ch.3 (I3)
52	AO3+	Quadrature waveform for Ch.2 (Q2)
53	AO2+	In-phase waveform for Ch.2 (I2)
54	AO1+	Quadrature waveform for Ch.1 (Q1)
55	AO0+	In-phase waveform for Ch.1 (I1)
57	AI7+	Analog Input 8
59	AI6+	Analog Input 7
60	AI5+	Analog Input 6
62	AI4+	Analog Input 5
63	AI3+	Analog Input 4
65	AI2+	Analog Input 3
66	AI1+	Analog Input 2
68	AI0+	Analog Input 1

Table J-1: Pin number, name, and description for the main interface connector.

Pins 1 and 35 are the +5V supply from the PXI-7853R cards. These pins are connected together, but are not used as supplies in the system. All of the ground pins are connected directly to the main ground plane. If possible, it would be desirable to use a split ground/star ground topology to isolate the analog and digital signals, however this was not done on the current revision of the interface board. Pins 10, 11, 44, and 45 control the RF switches for the different channels. These switches are active low, that is, the modulator channel is connected to output by a logic low on these lines. Pins 36 and 37 are SCL and SDA, which are the clock and data lines for the I^2C bus. These lines must be pulled up to the +3.3V line through resistors (approximately 4.7kΩ, but this depends on the devices connected.) Pins 37-41 are the serial data lines for the step attenuators. Each line corresponds to a separate channel. See the Peregrine Semi data sheet for timing. Pins 42 and 43 are the clock and latch lines for the step attenuators. Pin 47 is the trigger line, this should be connected to a digital line for the MRI system that transitions high when waveform playback should begin. Pins 48-55 are the analog waveform lines. They are paired to supply the I and Q channels for each physical channel. These should be operated from +10V to -10V. The remaining digital lines are not dedicated to any specific use. They are brought out to connectors for later use. The analog input lines are also brought to connectors, but they are expected to be used for feedback and monitoring.

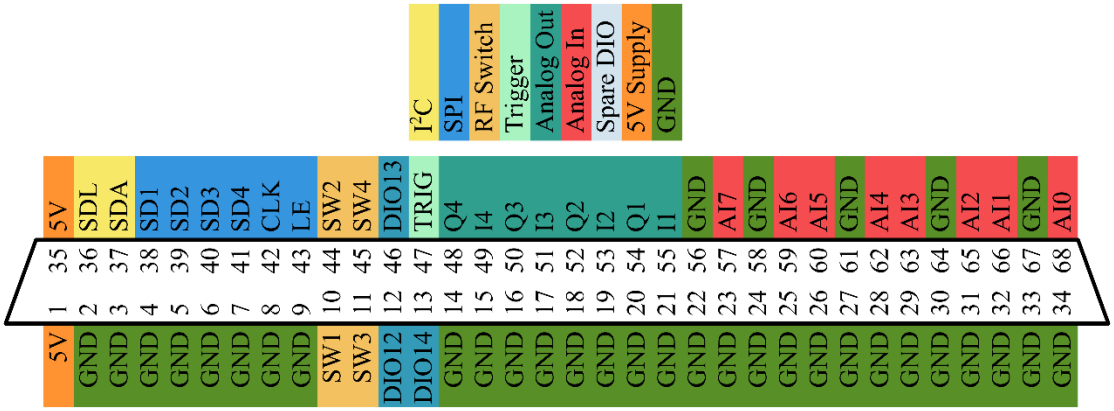


Figure J-1: Pinout for the NI HD-68 connector. This connector corrisponds to the RMIO-68 cable connecting the PXI-7853R card to the modulators.

J-1.2 Outward I/O

Only a subsection of the digital and analog I/O lines are actively used by the vector modulators. The remaining lines are passed through to a set of connectors on the rear edge of the board. These are spread over three connectors, two having the analogue input lines and the third having the digital I/O lines.

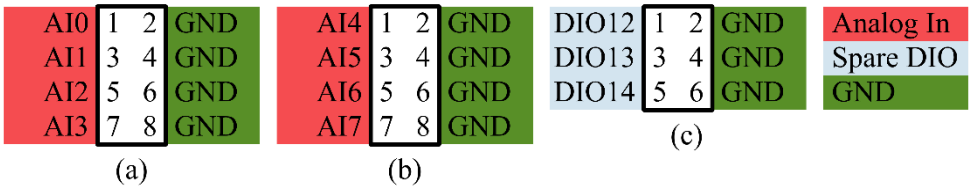


Figure J-2: Pinouts for the spare I/O connectors. The two analog connections are shown in (a) and (b), and the digital connections shown in (c).

J-1.3 RF I/O

A single SMB connection is used to bring in the local oscillator. The level at this connector should be approximately -32dBm. The outputs are four SMA connectors, with a peak possible power level of 14dBm.

J-1.4 Power Connections

Power is supplied to the vector modulator through an 8-pin Mini-Fit Jr. connector.

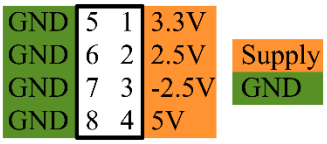


Figure J-3: Pinout for power connector.

J-1.5 Board-to-Board Connections

There are five connectors between the front-end and RF boards. Each of these is a 50mil pitch header connector. The primary connector is a 20 pin connector that carries the power and digital signals. Pins 19 and 20 are the supply lines (+3.3V and +5V respectively). The RF switch controls are on pins 13-14, corresponding to channels one through four. These switches are active low and will work with either 5V or 3.3V logic. The data lines for the step attenuators are on lines seven through ten. Note that pins seven and eight are for channels one and two, and ten and nine for channels three and four in that order. The latch enable and data clock lines for the attenuators are on pins three and four. The attenuator control lines can also be used with either 5V or 3.3V logic. All of the remaining pins are ground.

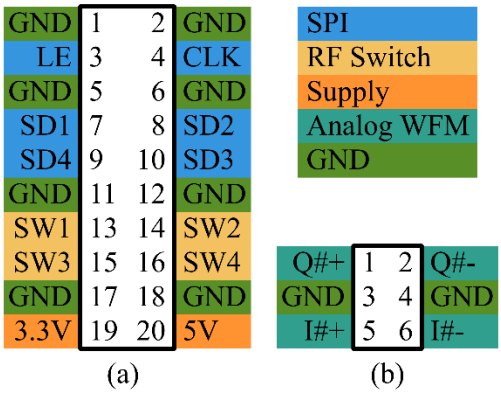


Figure J-4: Board-to-board connector pinouts. The I/Q waveform connectors are showin in (a), there is one for each modulator channel. The main digital and power connnector is shown in (b), there is one per board.

Pin Number	Name	Description
1	Q+	Quadrature waveform +
2	Q-	Quadrature waveform -
5	I+	In-phase waveform +
6	I-	In-phase waveform -
3,4	GND	Tied to board ground plane

Table J-2: Pin number, name, and description for the channel board-to-board connector

Pin Number	Name	Description
3	LE	Latch for attenuators
4	CLK	Clock for attenuators
7	SD1	Data for attenuator 1
8	SD2	Data for attenuator 2
9	SD4	Data for attenuator 4
10	SD3	Data for attenuator 3
13	SW1	Control for RF switch 1
14	SW2	Control for RF switch 2
15	SW3	Control for RF switch 3
16	SW4	Control for RF switch 4
19	+3.3V	+3.3V power supply
20	+5V	+5V power supply
1,2,5,6,11,17,18	GND	Tied to board ground plane

Table J-3: Pin number, name, and description for the primary board-to-board connector

Each channel also has its own six pin connector that carries the analog waveforms. Pins one and two carry Q+ and Q- signals and pins five and six carry I- and I+. The modulator expects to see a differential signal that swings from 0V to 1V, with a common mode voltage of 0.5V. It is important that the common mode voltage does not exceed 0.6V or the modulator IC may be damaged. Pins three and four are ground pins.

J-2 Voltage Regulator Board Connections

All of the DC power for the modulators is routed through this board so the lines can be collected into standard power connectors. Molex's Mini-Fit Jr. line of connectors is used for internal DC power connections.

J-2.1 Screw Terminal (Power Input)

The input to the voltage regulator board is through a ten position euro terminal block. The modulators do not require all of these voltages, but other parts of the system do. Collecting all of the voltage rails onto a single board simplifies the wiring harness.

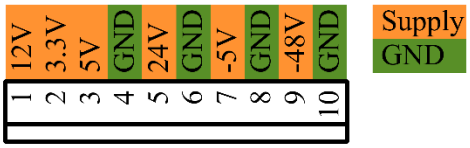


Figure J-5: Screw terminal connections for the DC regulator board.

J-2.2 Mini-Fit Jr and Spare Power. Connectors

The regulator board has two each of three different size Mini-Fit Jr. Connectors. The four pin connectors are intended to supply the driver amplifier stage, the size pin connectors have legacy voltages and supply the power amplifiers, and the eight pin connectors are for the modulators.

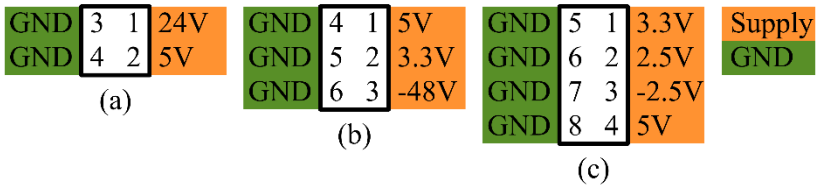


Figure J-6: Mini-Fit Jr. Supply connectors. The 4 pin legacy connector (a), six pin amplifier connector (b), and eight pin modulator connector (c).

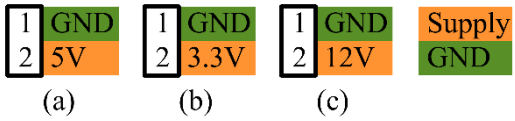


Figure J-7: The supply board spare two pin connectors. The three most commonly used voltages are included

APPENDIX K
SCHEMATICS AND BOMS

The schematics for the major PCBS and Bills of Material (BOMS) are included in this appendix.

K-1 Modulator RF Board Schematics and BOM

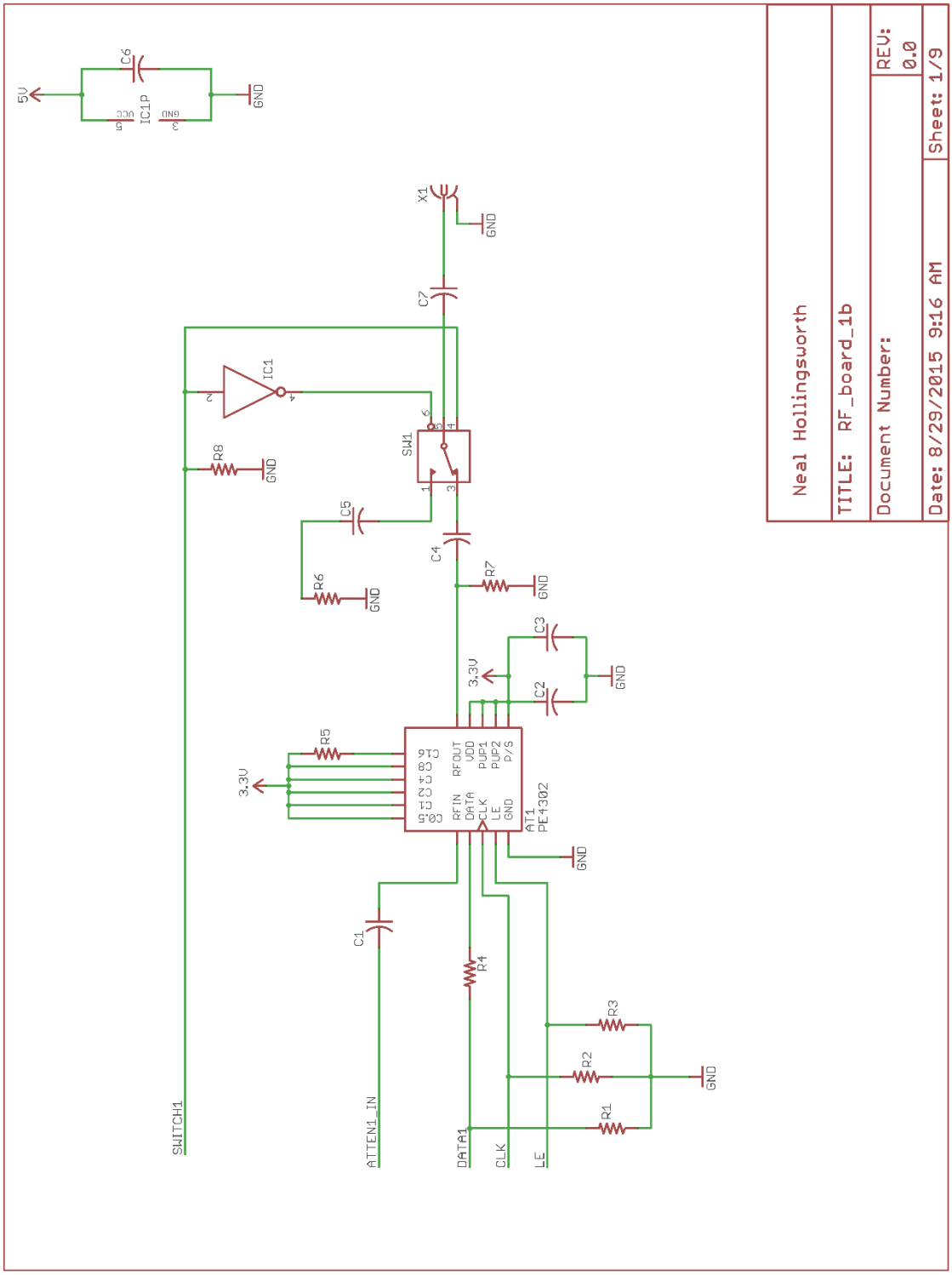


Figure K-1: Modulator RF board schematics.

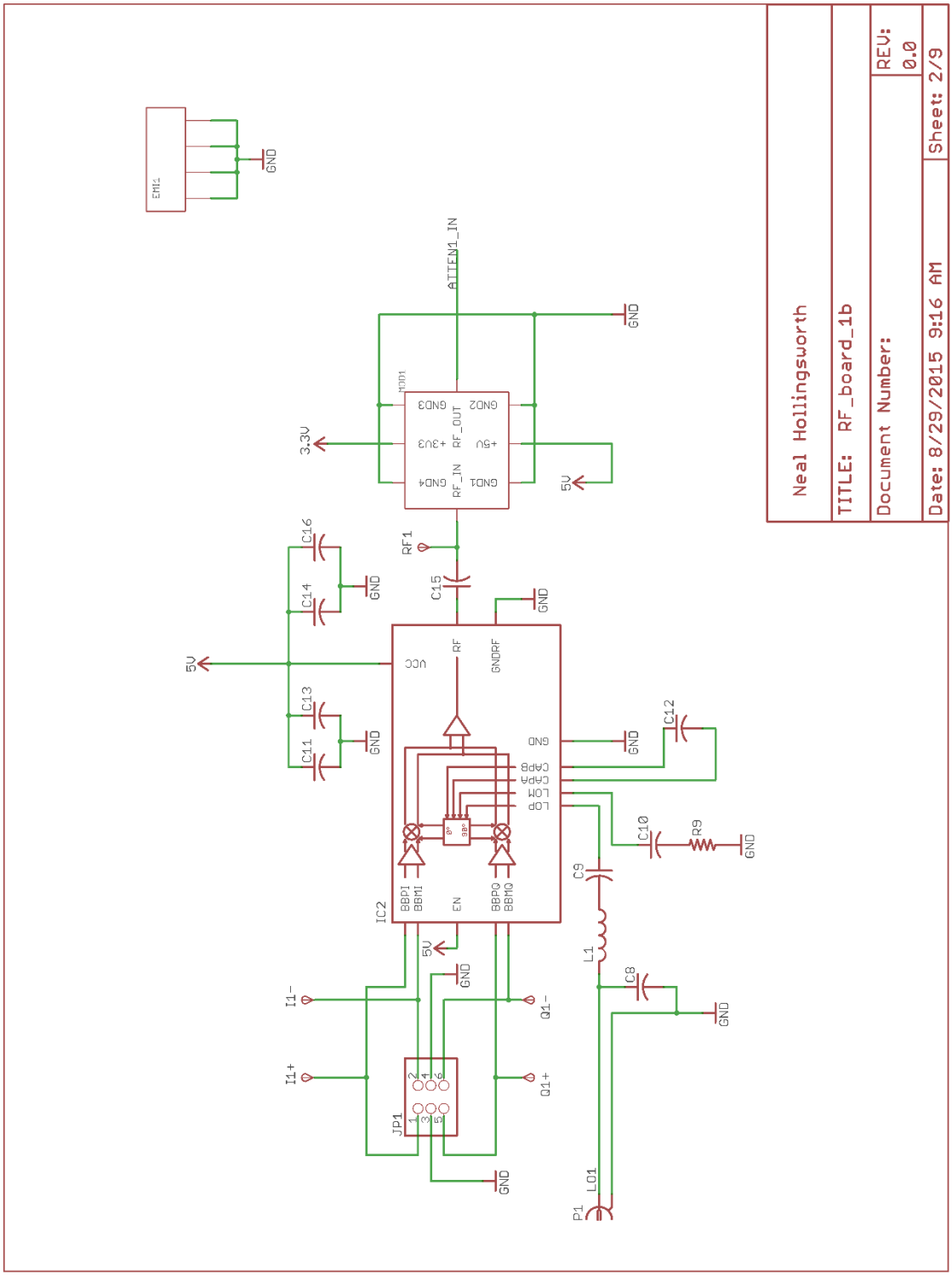


Figure K-1 : Continued

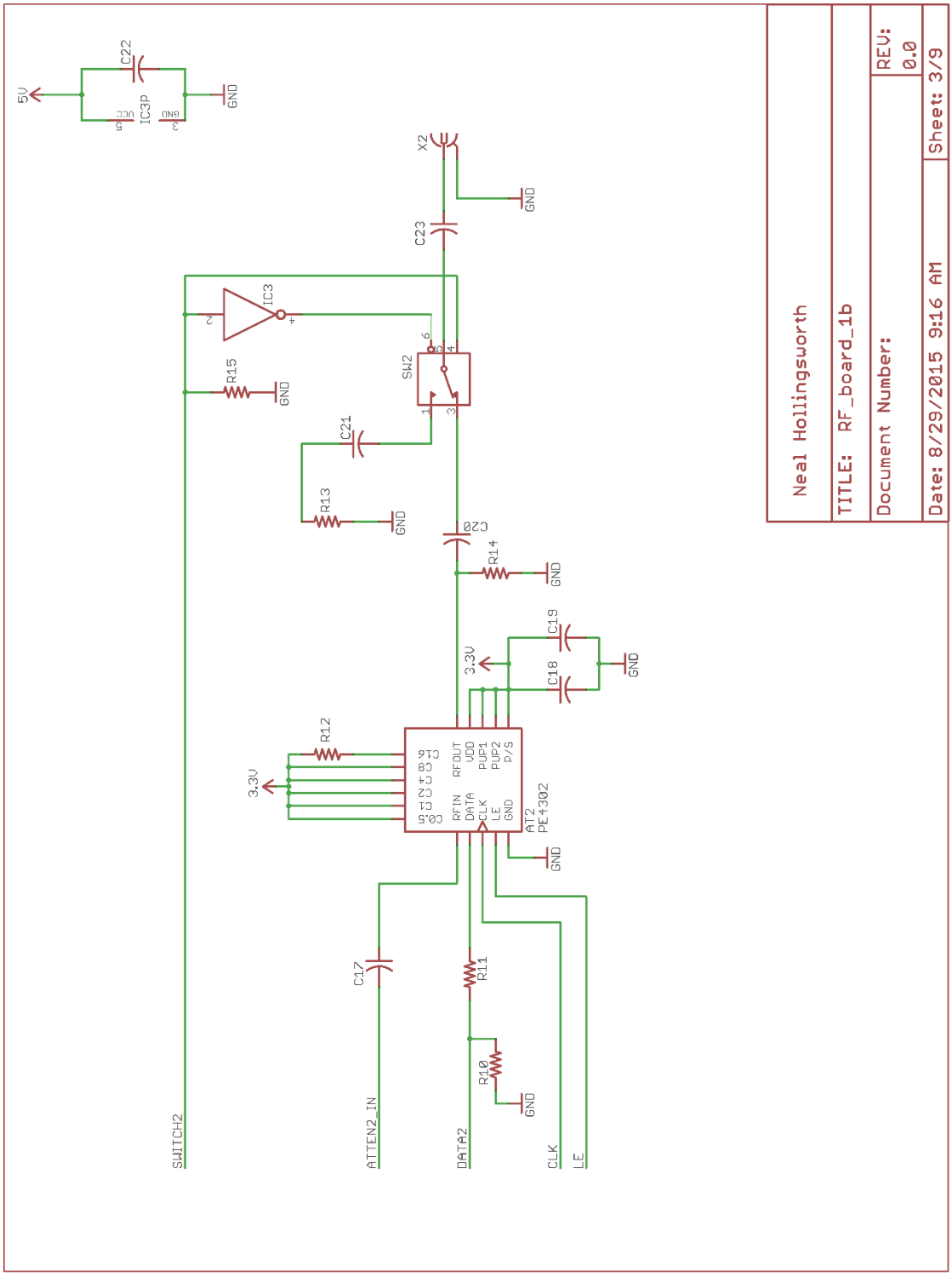


Figure K-1 : Continued

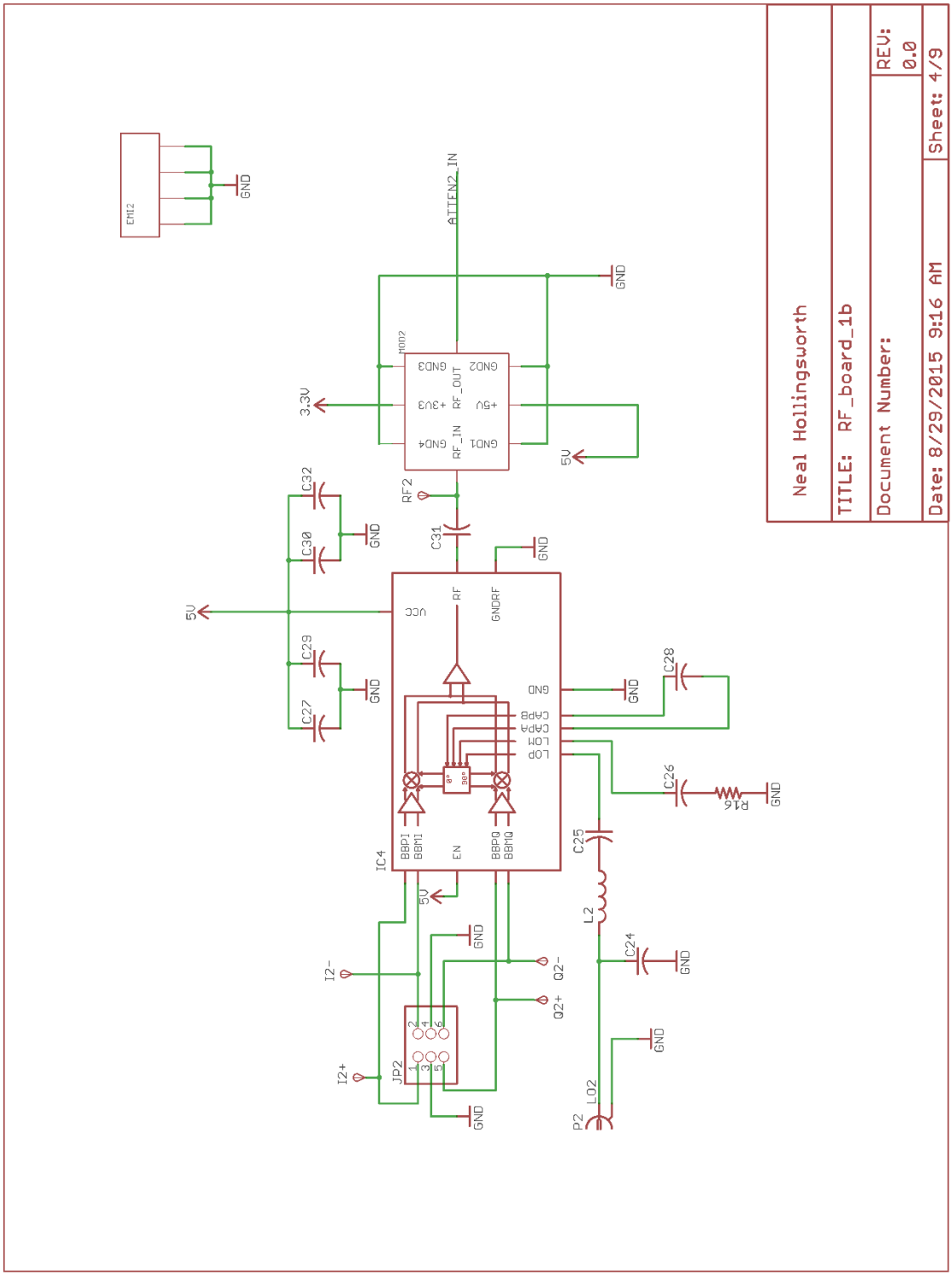


Figure K-1 : Continued

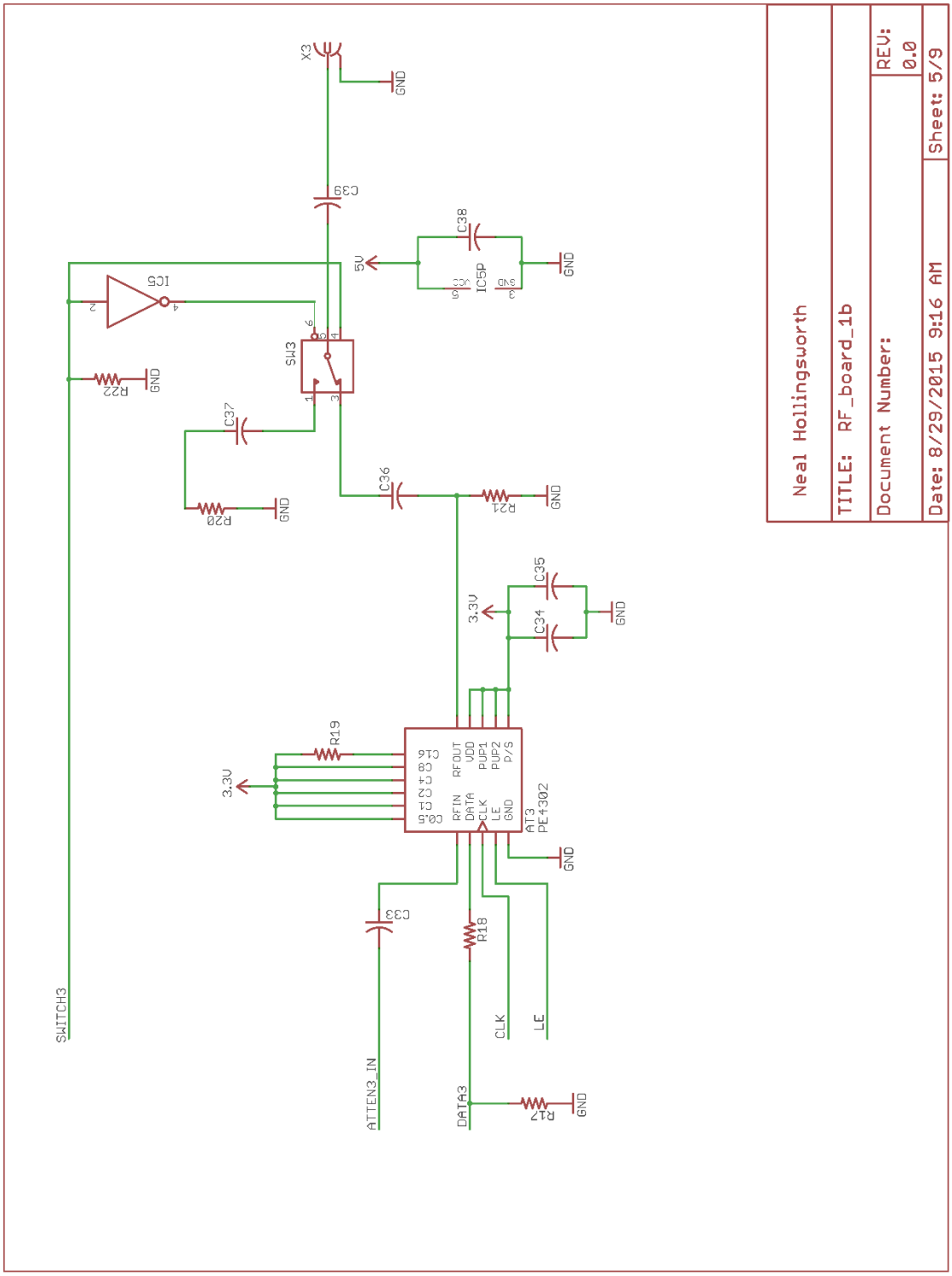


Figure K-1 : Continued

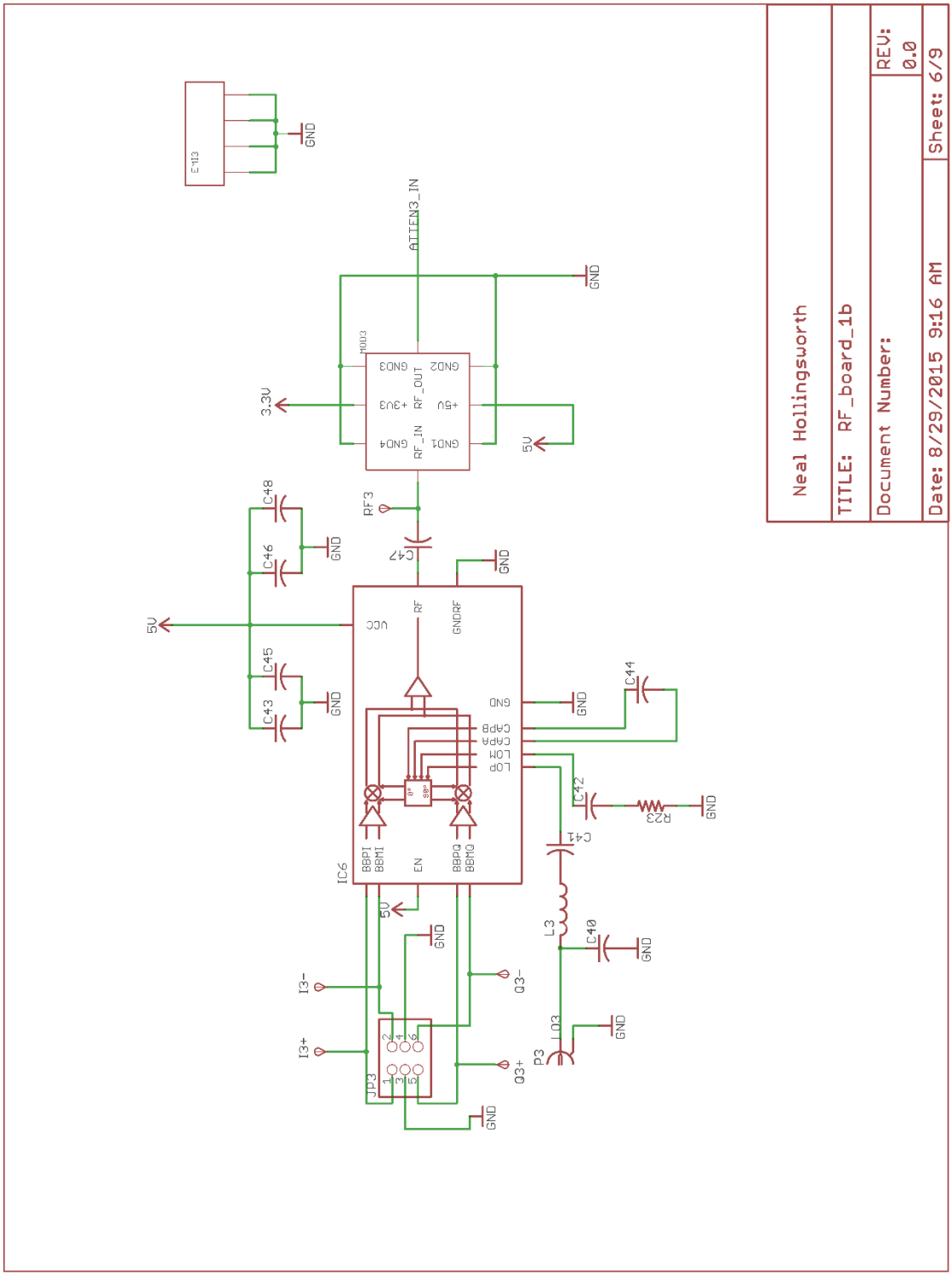


Figure K-1 : Continued

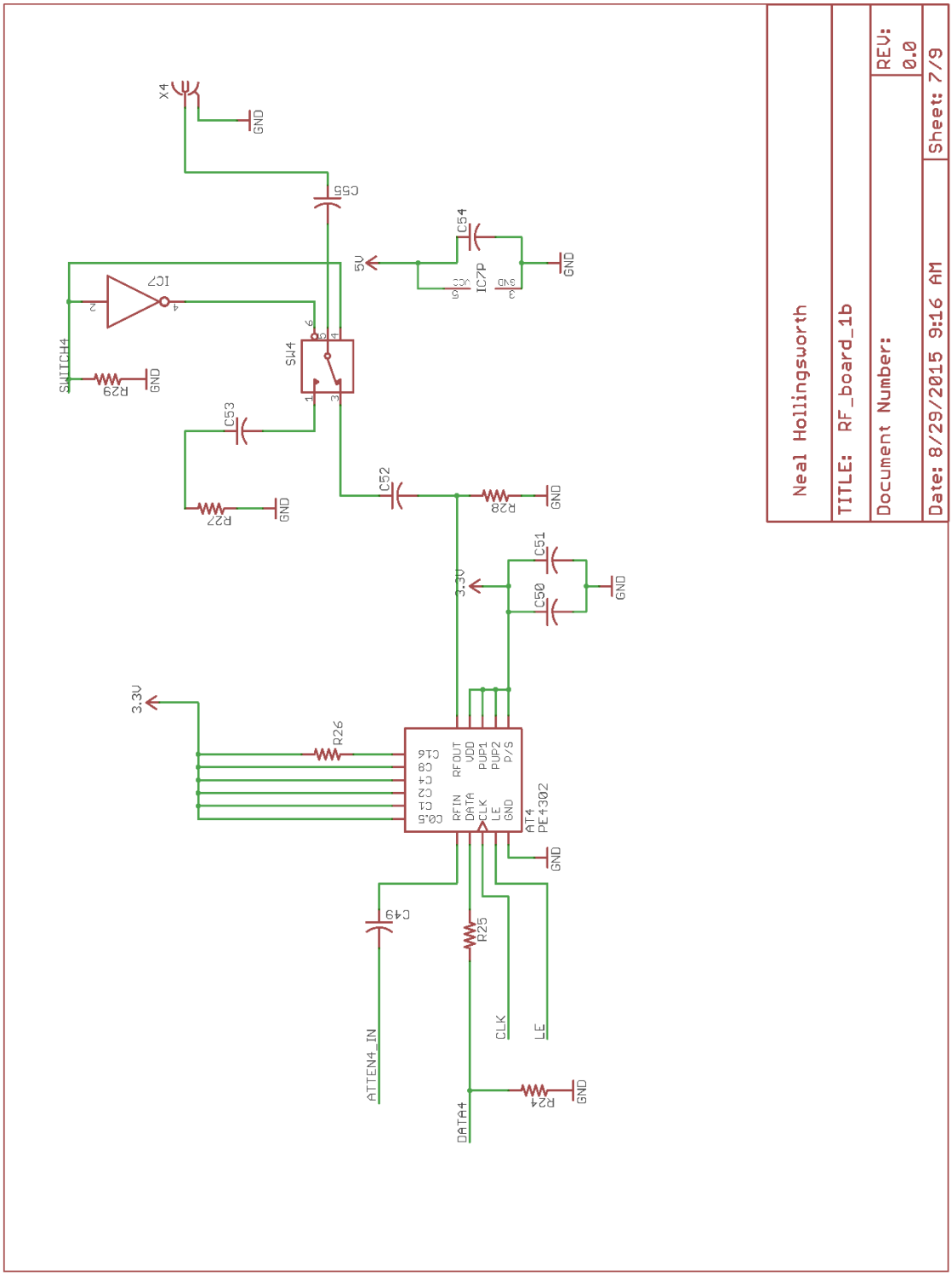


Figure K-1 : Continued

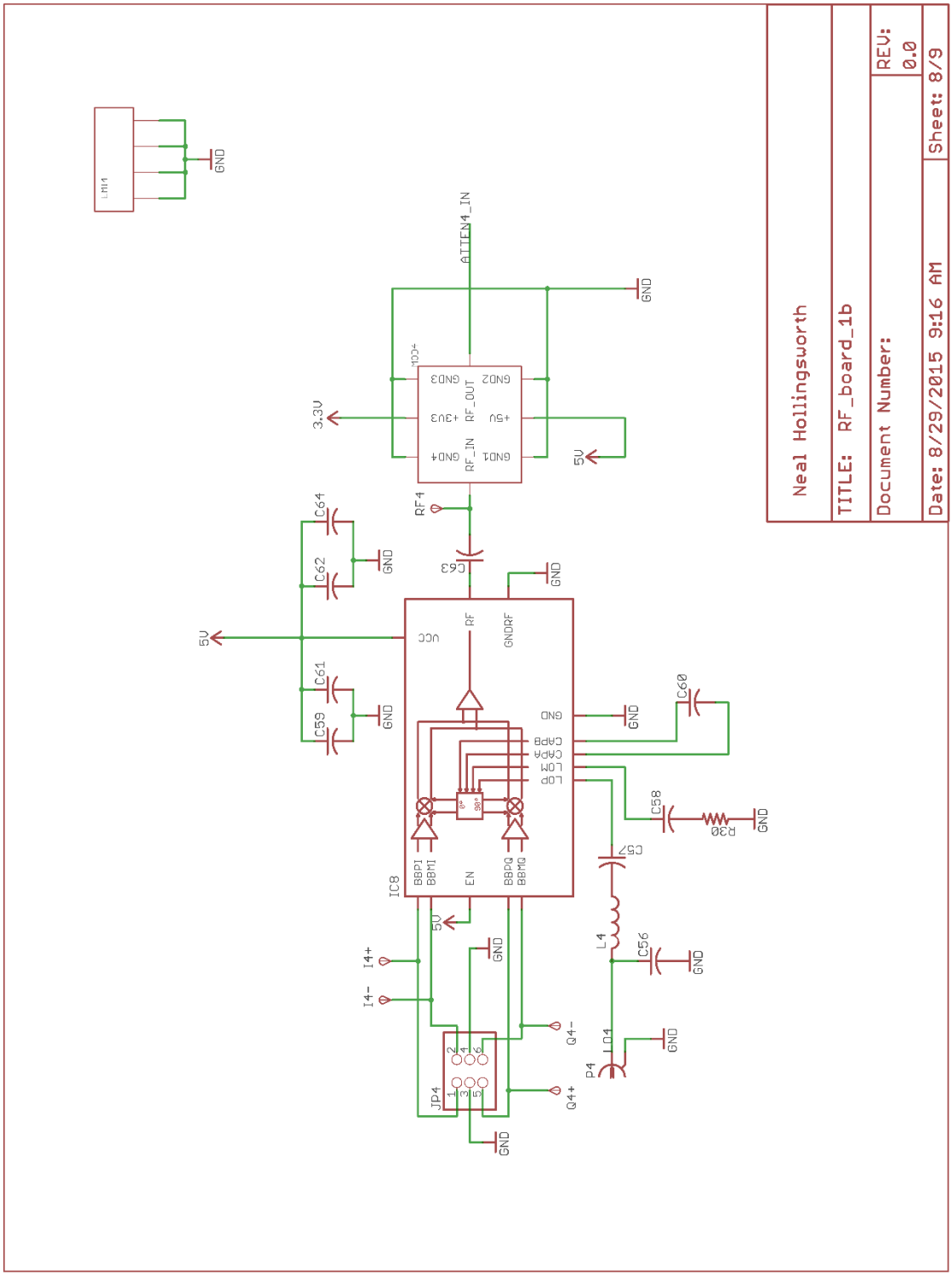


Figure K-1 : Continued

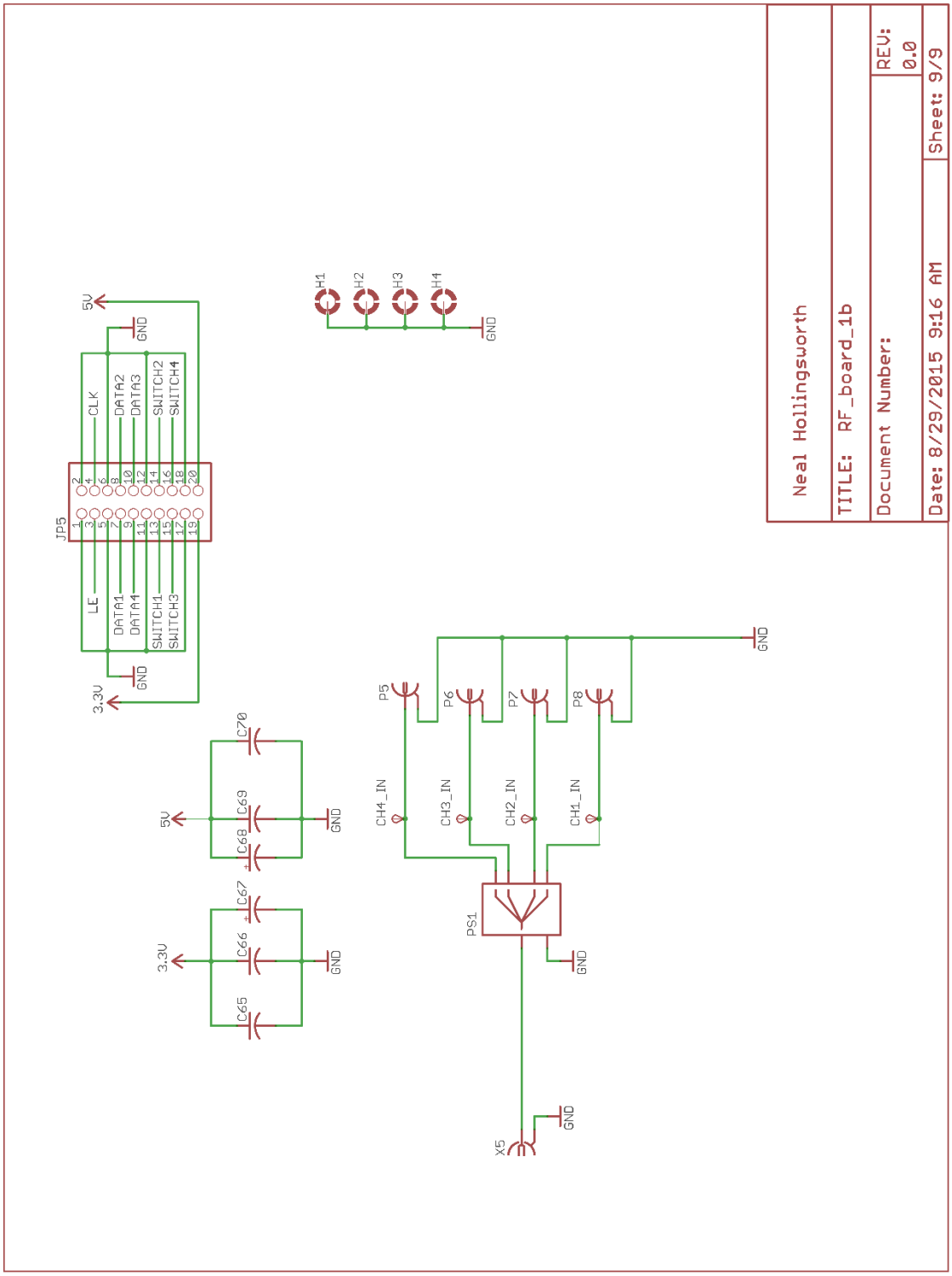


Figure K-1 : Continued

Qty	Value	Parts	Notes
6	0.1uF	C3, C19, C35, C51, C66, C70	
4	100pF	C2, C18, C34, C50	
8	10KΩ	R4, R5, R11, R12, R18, R19, R25, R26	
10	15KΩ	R7, R10, R14, R15, R17, R21, R22, R24, R28, R29	
4	15pF	C8, C24, C40, C56	
8	1nF	C13, C14, C29, C30, C45, C46, C61, C62	
22	2200pF	C1, C6, C9, C10, C15, C17, C22, C25, C26, C31, C33, C38, C41, C42, C47, C49, C54, C57, C58, C63, C65, C69	Supply bypassing capacitors
2	22uF	C67, C68	Tantalum bypassing capcitors
12	39pF	C4, C5, C7, C20, C21, C23, C36, C37, C39, C52, C53, C55	
4	4.7kΩ	R1, R2, R3, R8	
8	4.7uF	C11, C16, C27, C32, C43, C48, C59, C64	
4	470nF	C12, C28, C44, C60	
8	51.1Ω	R6, R9, R13, R16, R20, R23, R27, R30	RF Termination, near 50Ω is Good Enough
4	56nH	L1, L2, L3, L4	
4	74AHC1G04DCK	IC1, IC3, IC5, IC7	
4	BMIS105_EZ	EMI1, EMI2, EMI3, EMI4	Board level shielding
1	BU-SMB-VEM	X5	SMB Input Connector
4	LT5598UF	IC2, IC4, IC6, IC8	RF Modulator
4	MASWSS0115	SW1, SW2, SW3, SW4	RF Switch
4	PE4302	AT1, AT2, AT3, AT4	Digital Step Attenuator
1	PINHD-2X10/127F	JP5	Board -to-Board Connector
4	PINHD-2X3/127F	JP1, JP2, JP3, JP4	Board -to-Board Connector
1	SCA-4-10+	PS1	Power Splitter
4	SMA-73251-1290	X1, X2, X3, X4	SMA Output Connectors

Table K-1: Bill of Materials for modulator RF Board.

K-2 Modulator Frontend Board Schematics and BOM

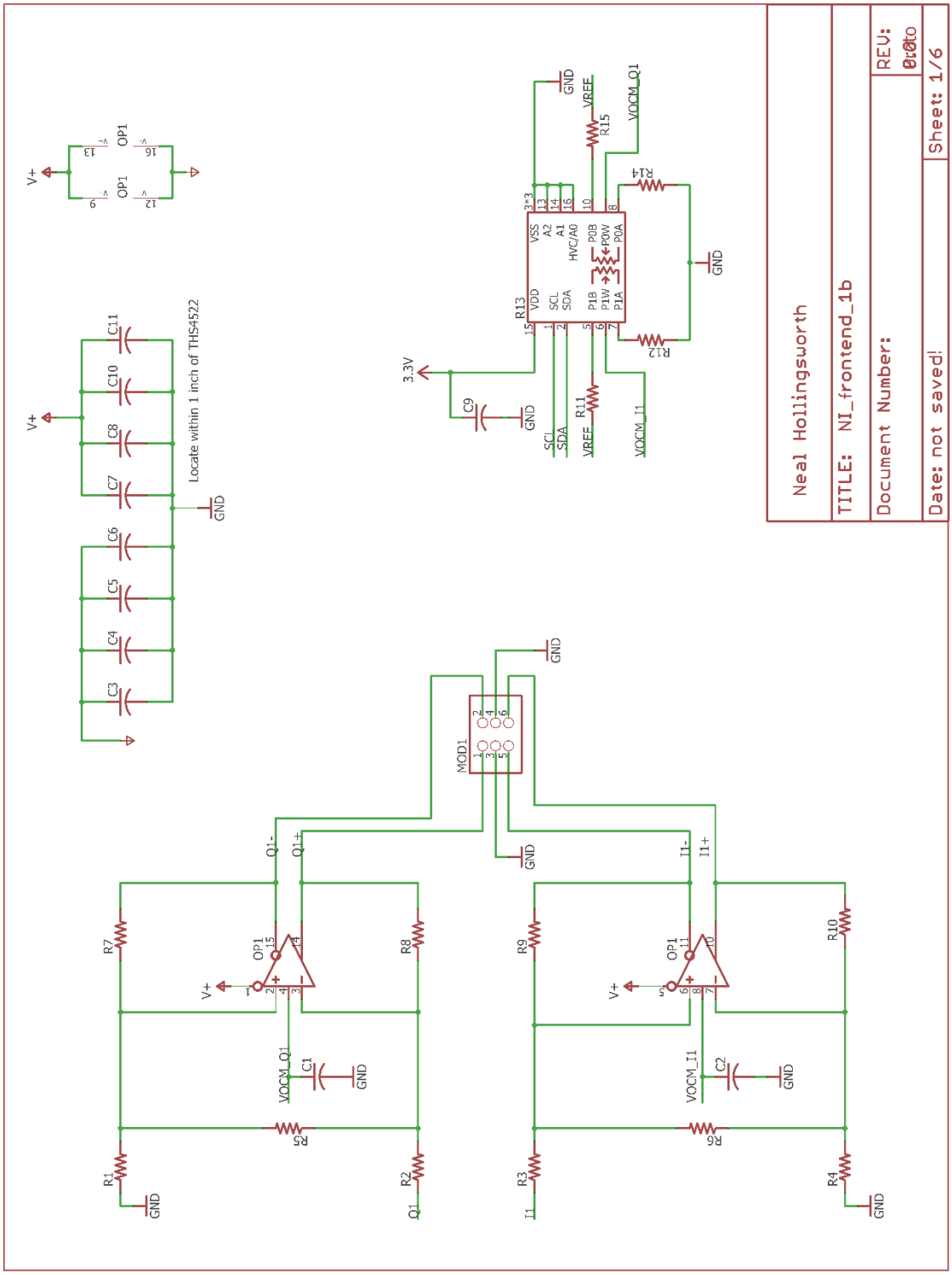


Figure K-2: NI frontend schematics.

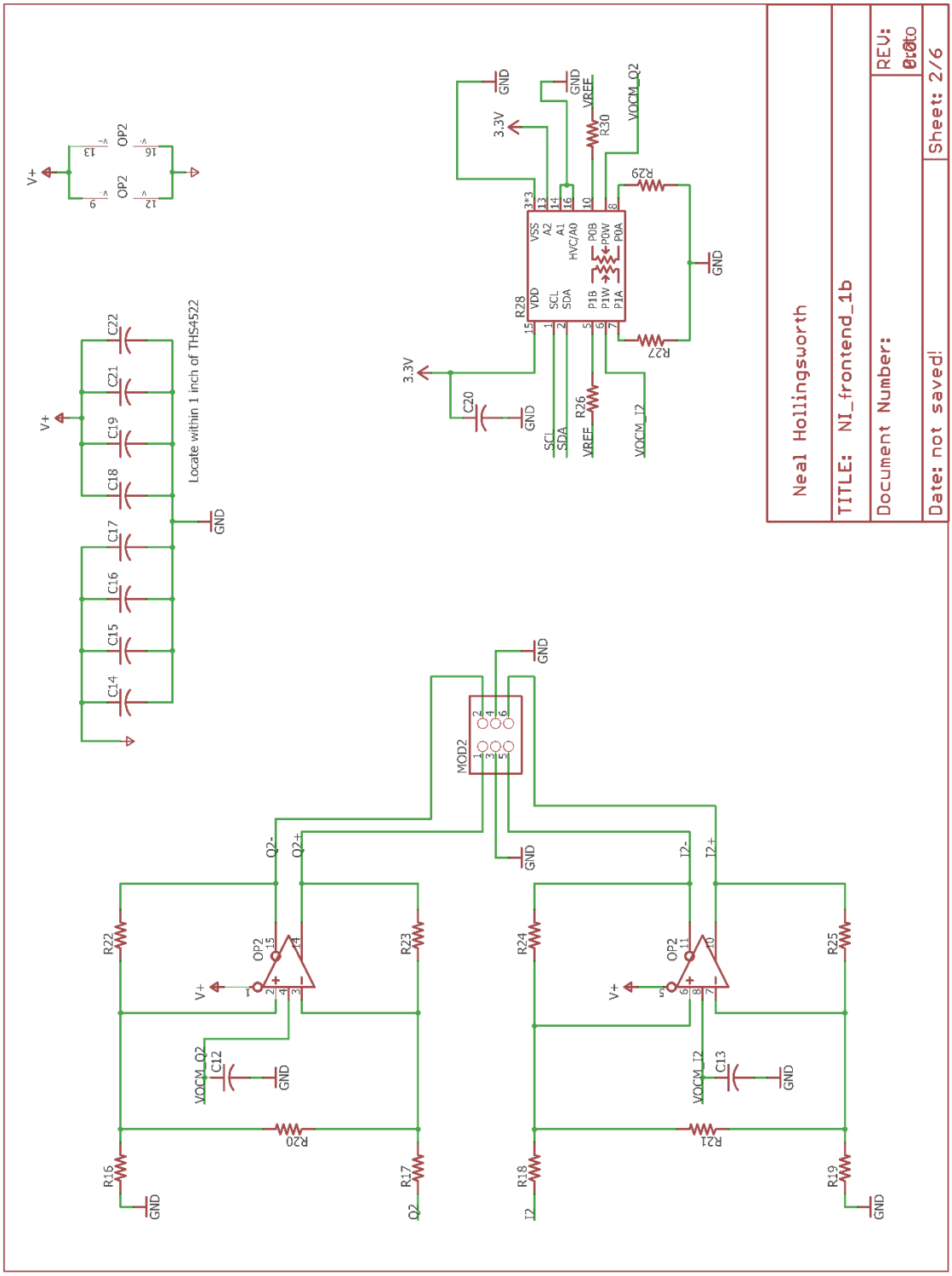


Figure K-2: Continued

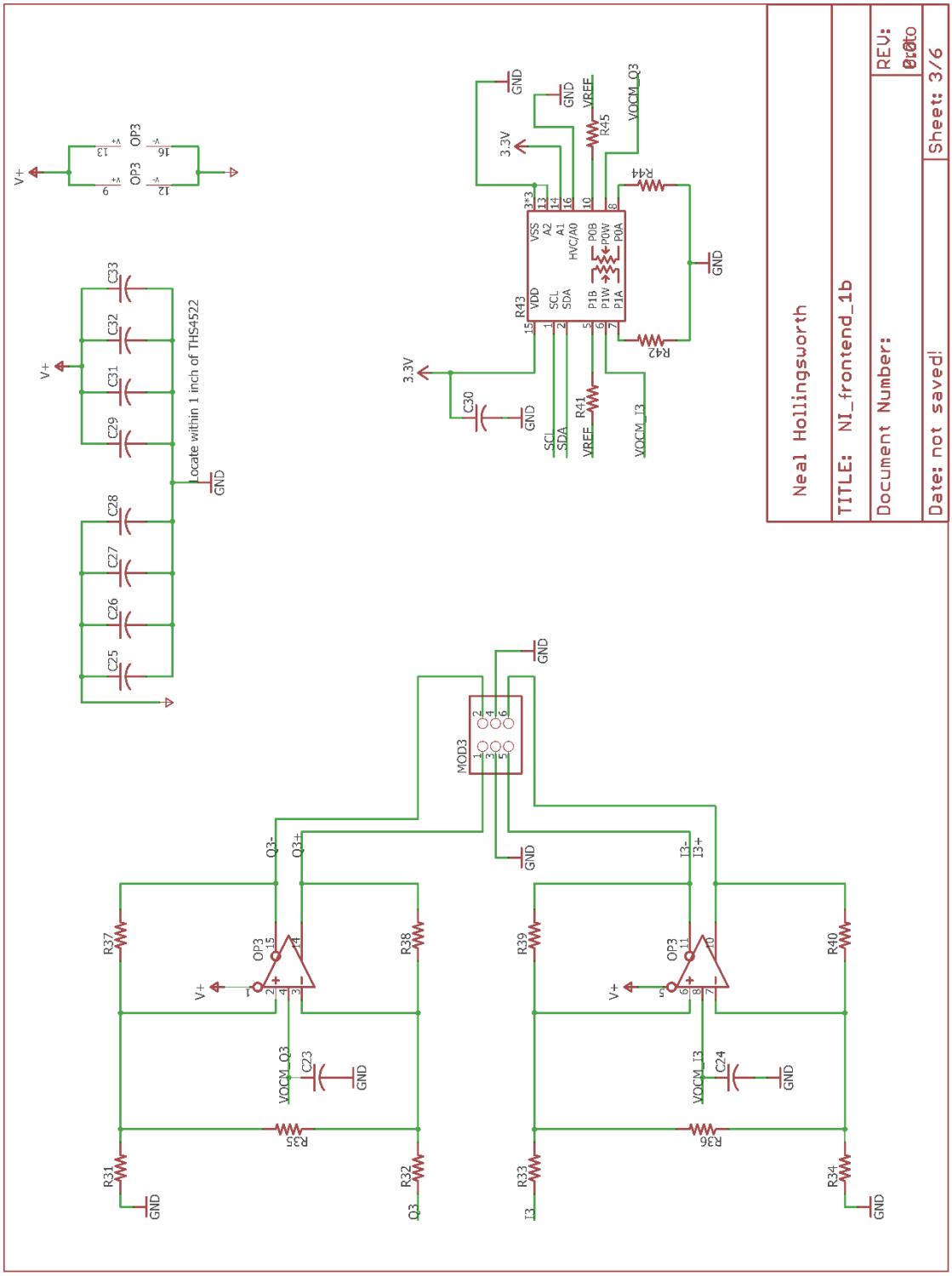


Figure K-2: Continued

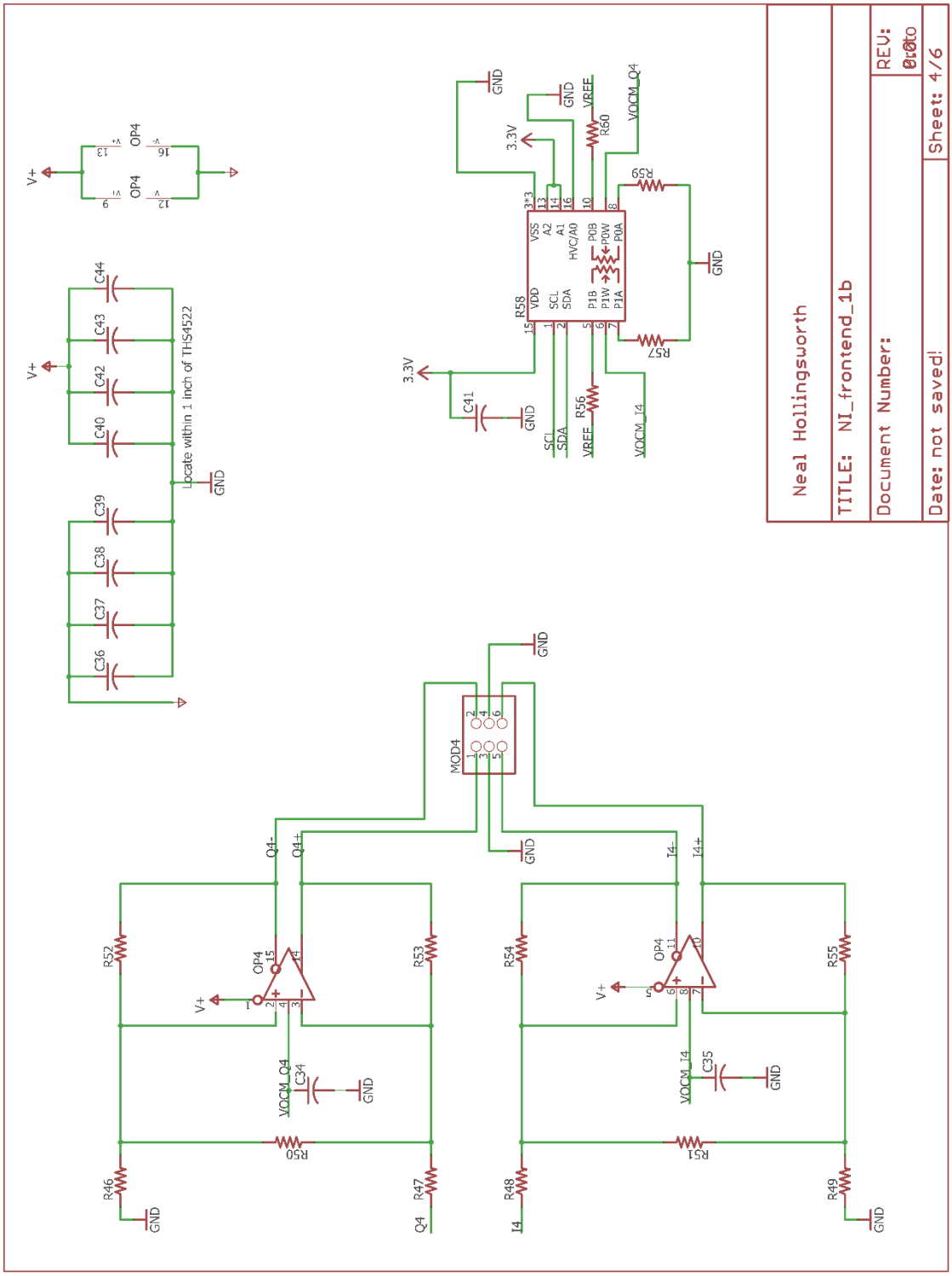


Figure K-2: Continued

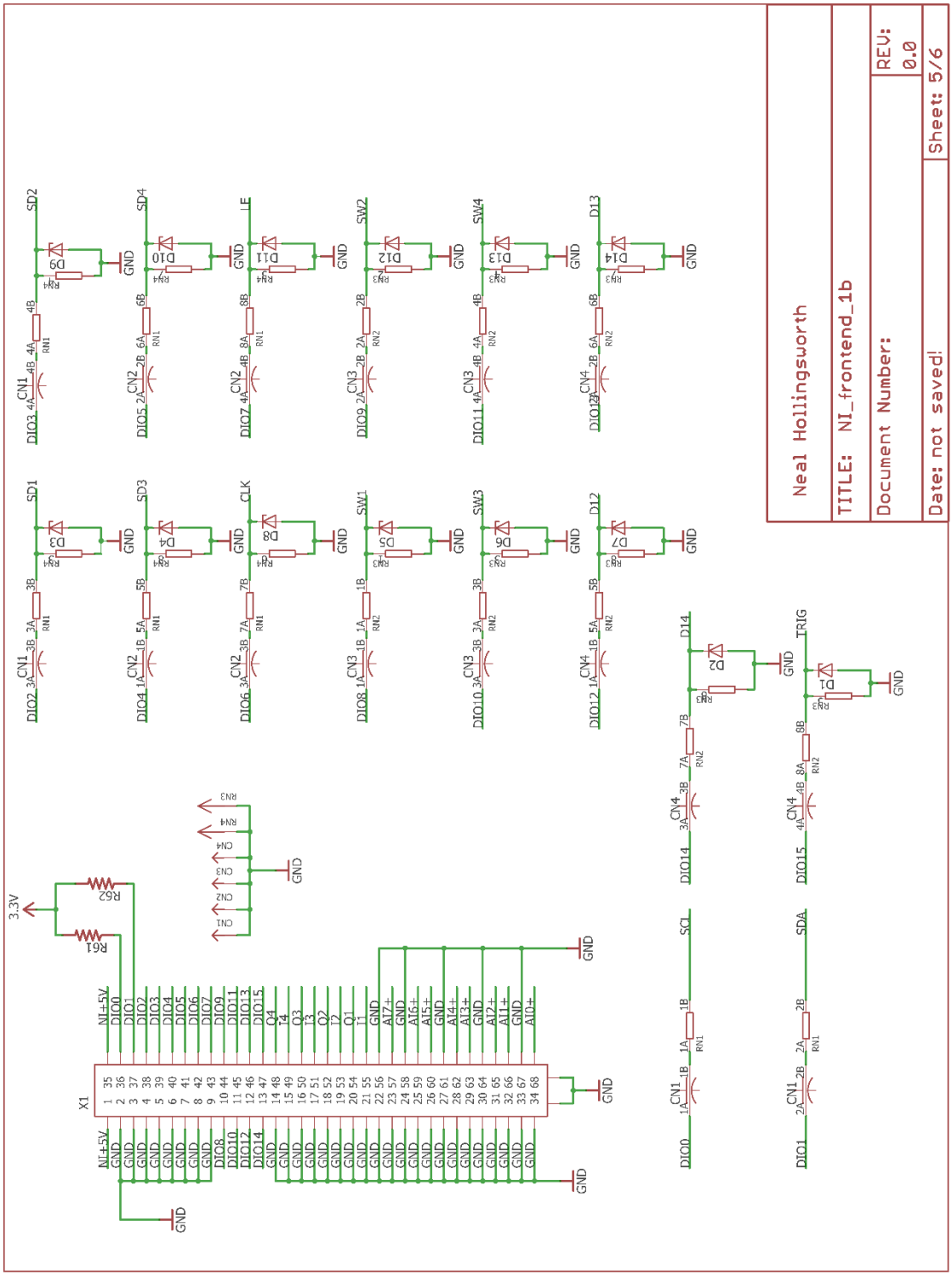


Figure K-2: Continued

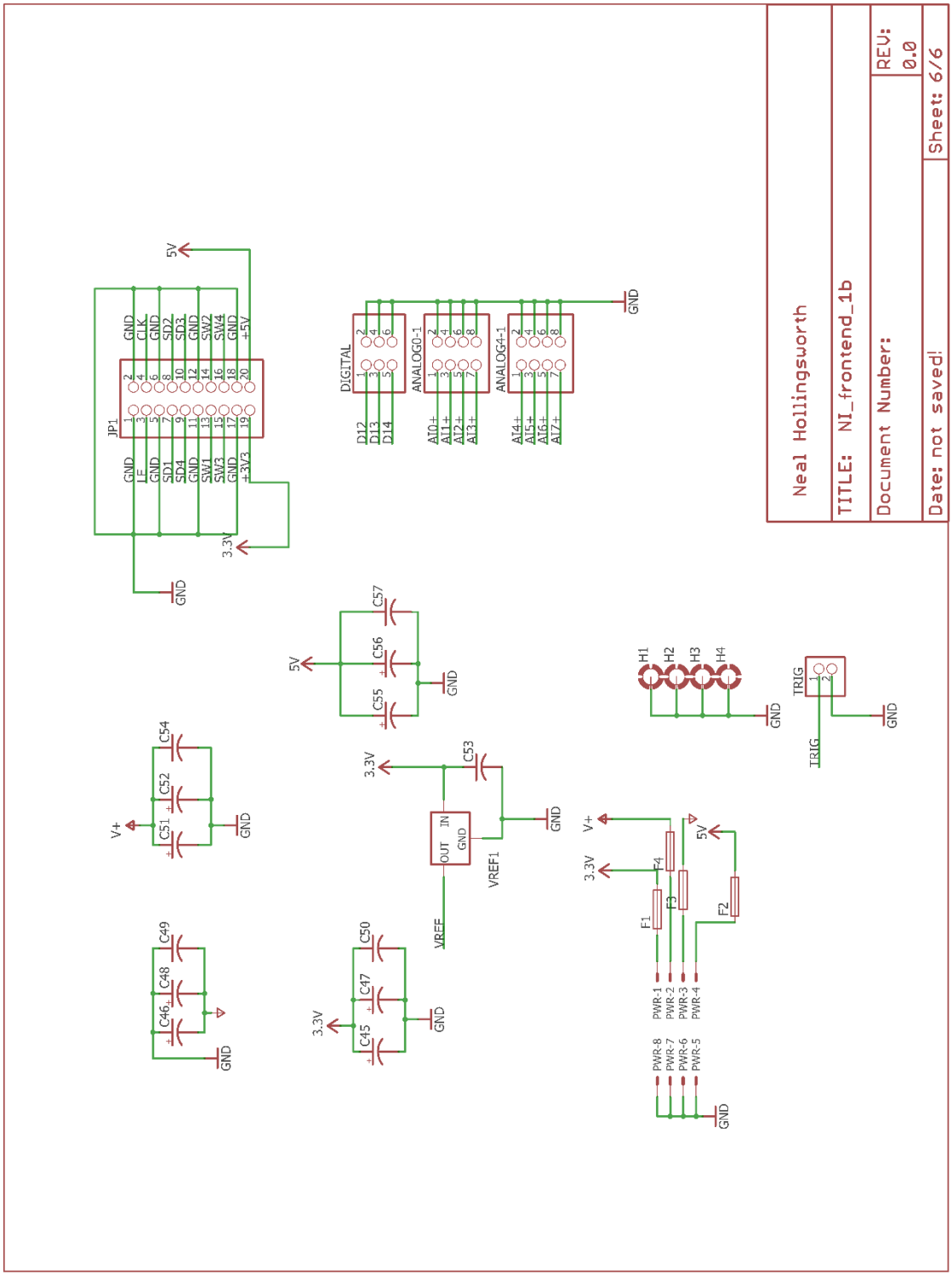


Figure K-2: Continued

Qty	Value	Parts	Description
2	PINHD-2X4/90	ANALOG0-1, ANALOG4-1	PIN HEADER
32	0.1uF	C1, C2, C3, C4, C7, C8, C9, C12, C13, C14, C15, C18, C19, C20, C23, C24, C25, C26, C29, C30, C31, C34, C35, C36, C37, C40, C41, C42, C49, C50, C54, C57	CAPACITOR, American symbol
1	0.47uF	C53	CAPACITOR, American symbol
1	1.25V Voltage Reference	VREF1	REF29* series 2% voltage reference
4	100pF Capacitor Array	CN1, CN2, CN3, CN4	PANASONIC 4 element capacitor array
4	10KΩ Resistor Array	R13, R28, R43, R58	Microchip Dual Digital Potemtiometer
2	10kΩ Resistor Array	RN3, RN4	CTS eight element bussed resistor array
8	10kΩ	R11, R15, R26, R30, R41, R45, R56, R60	RESISTOR, American symbol
16	10uF	C5, C6, C10, C11, C16, C17, C21, C22, C27, C28, C32, C33, C38, C39, C43, C44	CAPACITOR, American symbol
4	10uF	C47, C48, C52, C56	POLARIZED CAPACITOR, American symbol
2	1210L005 Fuse	F3, F4	LITTLEFUSE
1	1210L050 Fuse	F1	LITTLEFUSE
4	1uF	C45, C46, C51, C55	POLARIZED CAPACITOR, American symbol
8	2.1kΩ	R5, R6, R20, R21, R35, R36, R50, R51	RESISTOR, American symbol
24	20kΩ	R1, R2, R3, R4, R12, R14, R16, R17, R18, R19, R27, R29, R31, R32, R33, R34, R42, R44, R46, R47, R48, R49, R57, R59	RESISTOR, American symbol
2	220Ω Resistor Array	RN1, RN2	CTS Resistor Arry
16	2kΩ	R7, R8, R9, R10, R22, R23, R24, R25, R37, R38, R39, R40, R52, R53, R54, R55	RESISTOR, American symbol
1	30R110 Fuse	F2	LITTLEFUSE
2	4.7kΩ	R61, R62	RESISTOR, American symbol

Table K-2: Bill of Materials for the Modulator Frontend Board.

Qty	Value	Parts	Description
14	4.98V Zener Diode	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14	Z-Diode
1	5566-8A	PWR	Mini FIT connector 8 pol
1	HDM68	X1	HD68 connector
1	PINHD-1X2/90	TRIG	PIN HEADER
1	PINHD-2X10/127F	JP1	PIN HEADER
4	PINHD-2X3/127F	MOD1, MOD2, MOD3, MOD4	PIN HEADER
1	PINHD-2X3/90	DIGITAL	PIN HEADER
4	THS4522	OP1, OP2, OP3, OP4	THS4522 dual fully differential op amp.

Table K-2: Continued

K-3 Filter/Gain Block Schematic and BOM

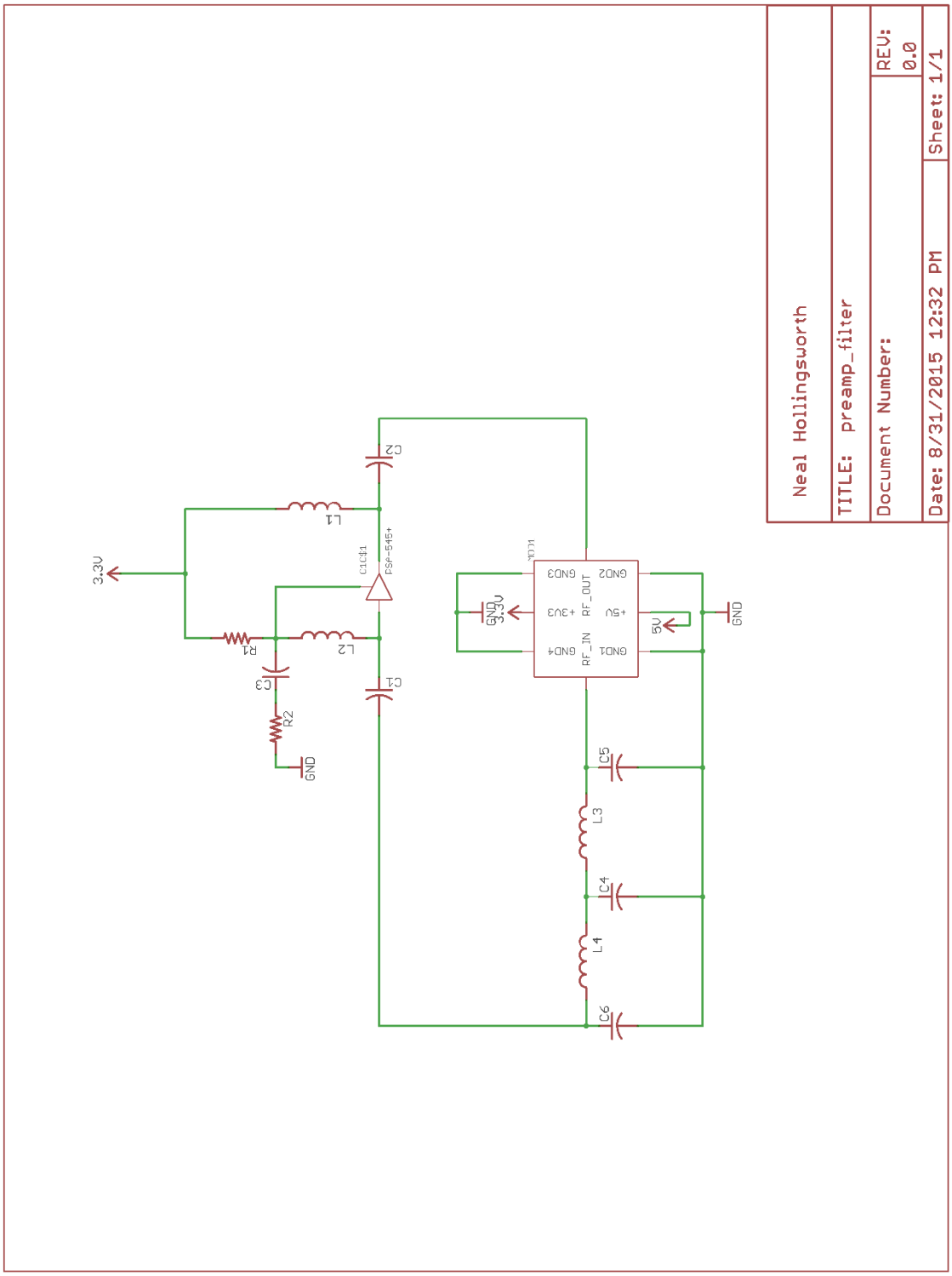


Figure K-3: Modulator preamplifier and filter schematic.

Qty	Value	Parts	Description
1	10pF	C3	CAPACITOR, American symbol
1	150ohm	L1	INDUCTOR, American symbol
1	180nH	L2	INDUCTOR, American symbol
2	2200pF	C1, C2	CAPACITOR, American symbol
1	442Ω	R1	RESISTOR, American symbol
1	50Ω	R2	RESISTOR, American symbol
2	51pF	C5, C6	CAPACITOR, American symbol
2	68nH	L3, L4	INDUCTOR, American symbol
1	75pF	C4	CAPACITOR, American symbol
1	PSA-545+	G1	Low noise MMIC amplifier. NF = 0.8dB gain = 20dB IP20=1dBm

Table K-3: Bill of Materials for a 128MHz filter/gain block daughter board.

K-4 Current Source Amplifier Schematics and BOM

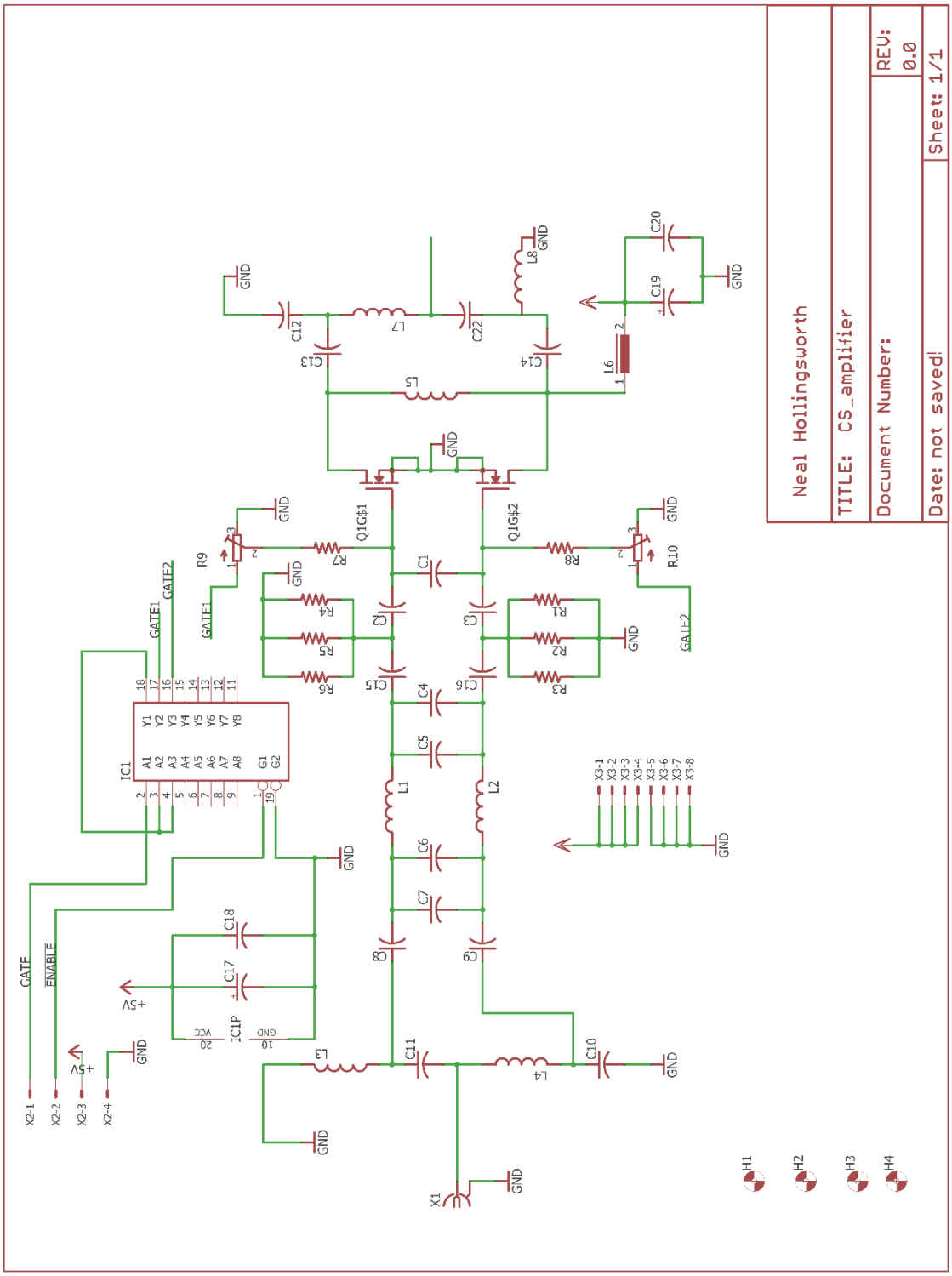


Figure K-4: Current Source amplifier schematic.

Qty	Value	Parts	Description
2		R9, R10	Trimm resistor
1		L6	Speicherdrossel (bis typ. 250kHz)
1	1000uF	C19	POLARIZED CAPACITOR, American symbol
2	100pF	C6, C7	CAPACITOR, American symbol
7	10nF	C2, C3, C8, C9, C15, C16, C20	CAPACITOR, American symbol
2	182pF	C4, C5	CAPACITOR, American symbol
2	2.2K	R7, R8	RESISTOR, American symbol
2	21nH	L1, L2	
2	2200pF	C13, C14	CAPACITOR, American symbol
1	2200pF	C18	CAPACITOR, American symbol
6	22R	R1, R2, R3, R4, R5, R6	RESISTOR, American symbol
1	22uF	C17	POLARIZED CAPACITOR, American symbol
4	25pF	C10, C11, C12, C22	CAPACITOR, American symbol
4	31nH	L3, L4, L7, L8	
1	37.5nH	L5	
1	5566-4A	X2	Mini FIT connector 4 pol
1	5566-8A	X3	Mini FIT connector 8 pol
1	74LS541DW	IC1	Octal BUFFER and LINE DRIVER, 3-state
1	750pF	C1	CAPACITOR, American symbol
1	ARF475FL	Q1	
1	SMA-142-0701-801/806	X1	SMA 50 Ohm End Launch Jack Receptacle - Round Contact

Table K-4: Bill of Materials for the Current Source Amplifiers.

K-5 LOI Amplifier Schematics and BOM

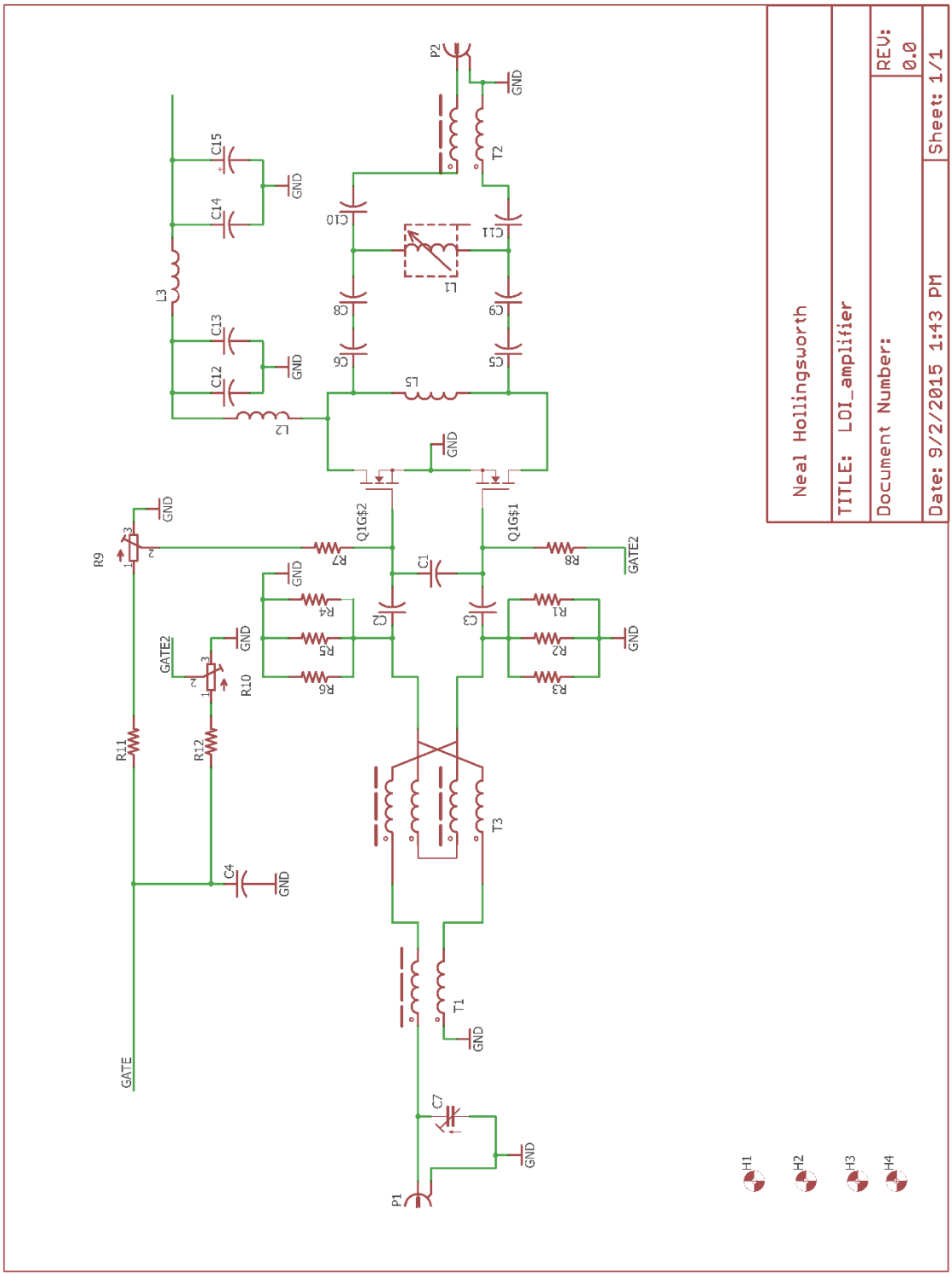


Figure K-5: Low Output Impedance amplifier schematic.

Qty	Value	Parts	Description
1		L1	
1		C7	Trimm capacitor
4		C8, C9, C10, C11	CAPACITOR, American symbol
2		L2, L3	INDUCTOR, American symbol
2		R9, R10	Trimm resistor
1	1000uF	C15	POLARIZED CAPACITOR, American symbol
3	10nF	C2, C3, C4	CAPACITOR, American symbol
2	1k	R11, R12	RESISTOR, American symbol
2	2.2K	R7, R8	RESISTOR, American symbol
2	2200pF	C5, C6	CAPACITOR, American symbol
6	22R	R1, R2, R3, R4, R5, R6	RESISTOR, American symbol
1	37.5nH	L5	Coilcraft Midi Spring Air Core Inductors
3	4.7nF	C12, C13, C14	CAPACITOR, American symbol
1	4:1TRANSFORMER	T3	
1	750pF	C1	CAPACITOR, American symbol
1	ARF475FL	Q1	
2	BALUN	T1, T2	

Table K-5: Bill of Materials for the Low Output Impedance Amplifier.

K-6 Voltage Regulator Board Schematics and BOM

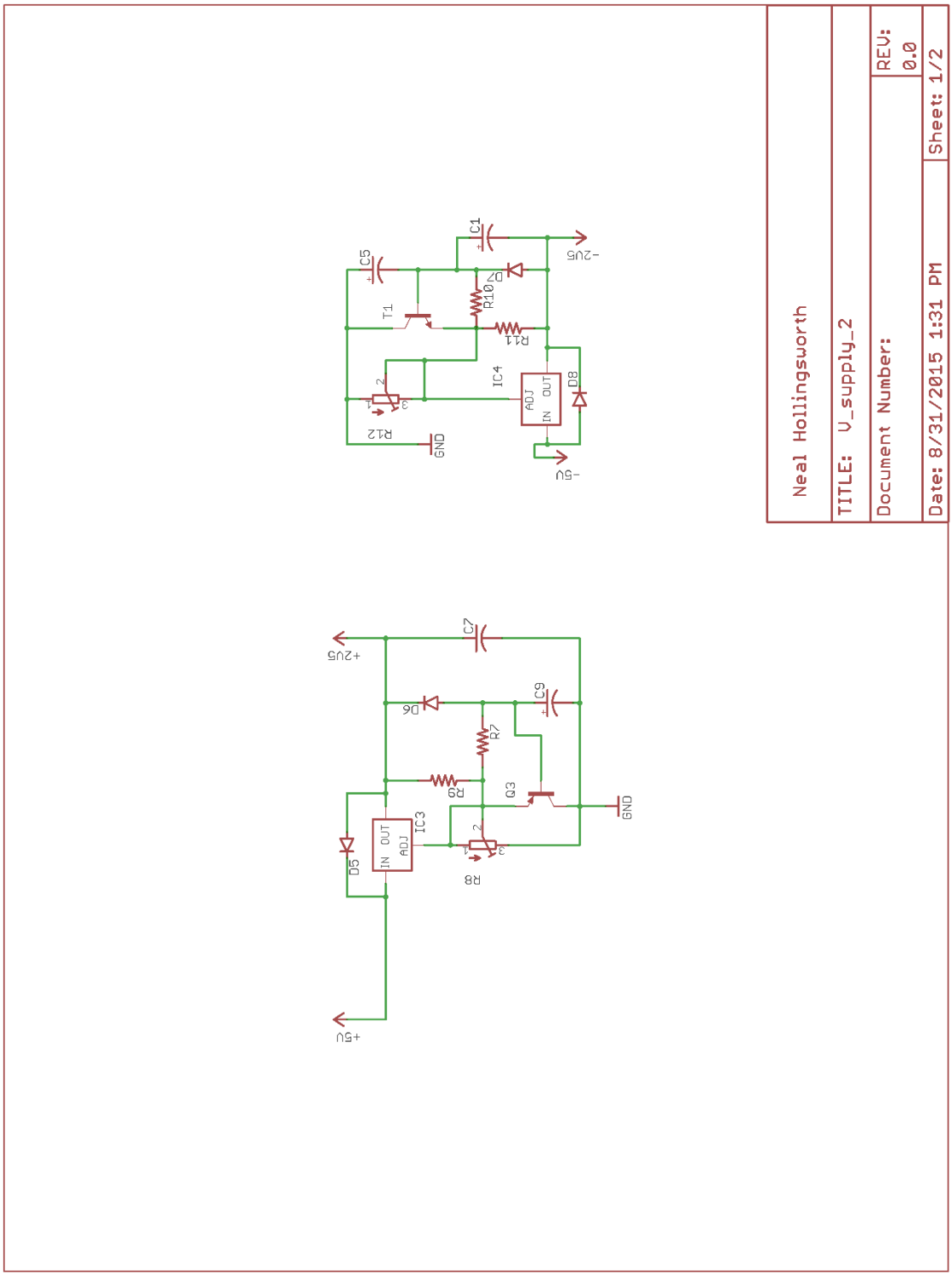


Figure K-6: Modulator voltage regulator schematics.

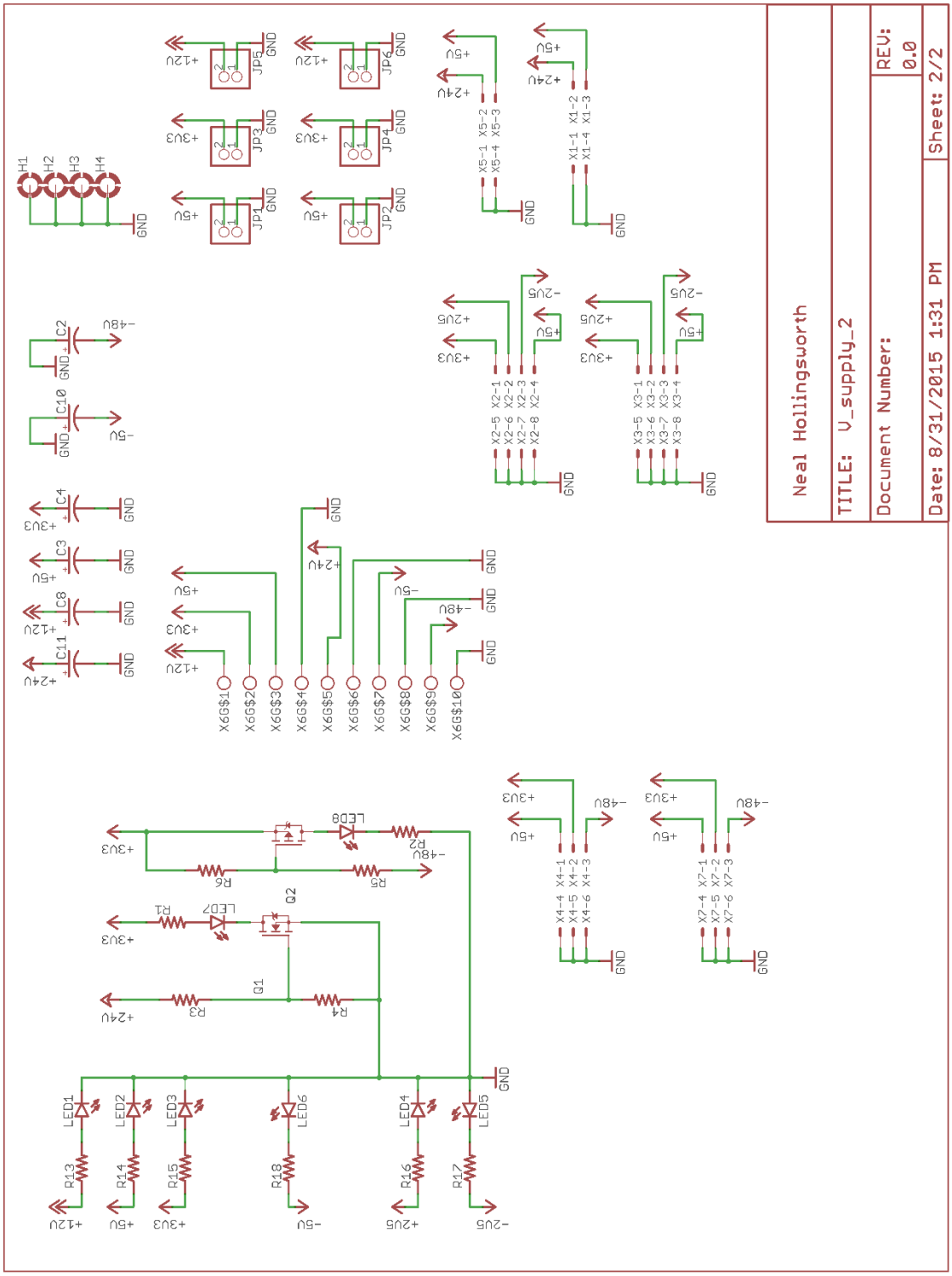


Figure K-6: Continued

Qty	Value	Parts	Description
8		LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8	LED
1		IC4	VOLTAGE REGULATOR
6		JP1, JP2, JP3, JP4, JP5, JP6	PIN HEADER
2	100uF	C5, C9	POLARIZED CAPACITOR, American symbol
1	10uF	C7	CAPACITOR, American symbol
1	10uF	C1	POLARIZED CAPACITOR, American symbol
2	121Ω	R9, R11	RESISTOR, American symbol
2	15Ω	R16, R17	RESISTOR, American symbol
2	150Ω	R14, R18	RESISTOR, American symbol
4	1N4148DO35-7	D5, D6, D7, D8	DIODE
1	22KΩ	R6	RESISTOR, American symbol
3	22uF	C3, C4, C8	POLARIZED CAPACITOR, American symbol
3	22uF	C2, C10, C11	POLARIZED CAPACITOR, American symbol
1	2N2907	Q3	
1	2N7002K	Q1	2N7002K N-Channel Enhancement Mode FET
1	330KΩ	R5	RESISTOR, American symbol
1	330KΩ	R3	RESISTOR, American symbol
2	50KΩ	R7, R10	RESISTOR, American symbol
1	51KΩ	R4	RESISTOR, American symbol
2	5566-4A	X1, X5	Mini FIT connector 4 pol
2	5566-6A	X4, X7	Mini FIT connector 6 pol
2	5566-8A	X2, X3	Mini FIT connector 8 pol
3	56Ω	R1, R2, R15	RESISTOR, American symbol
1	560Ω	R13	RESISTOR, American symbol
2	5kΩ	R8, R12	Trimm resistor
1	BC337TO92/S	T1	NPN TRANSISTOR
1	BSS84	Q2	BSS84 P-channel Enhancement FET -0.13A,-50V, Rds(on)=10ohm
1	LD117ASTR	IC3	Low drop fixed and adjustable positive voltage regulators 1 A
1	W237-10	X6	

Table K-6: Bill of Materials for Voltage Regulator Board.

K-7 T/R Switch and Preamp Schematics and BOMs

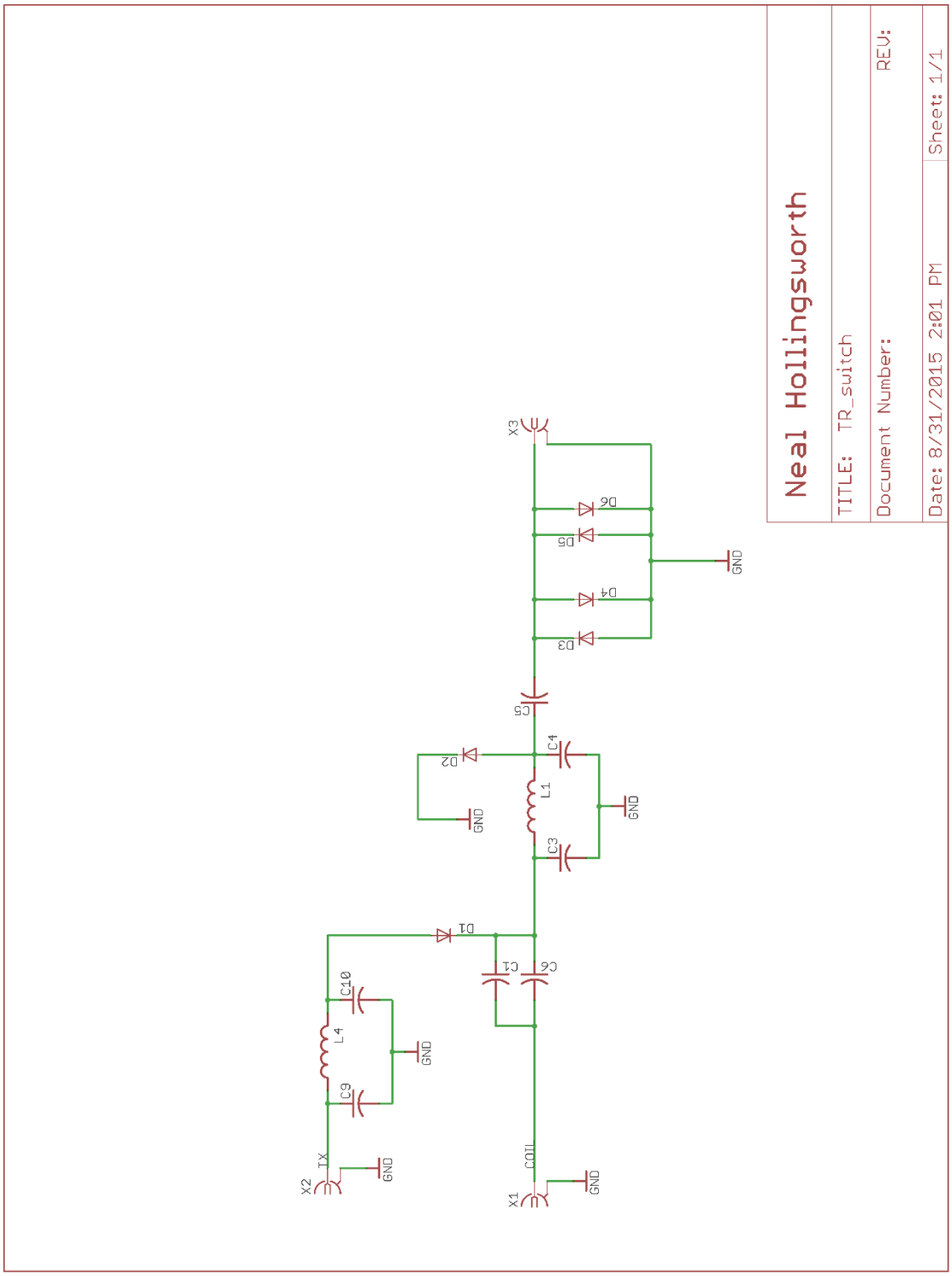


Figure K-7: T/R switch schematic.

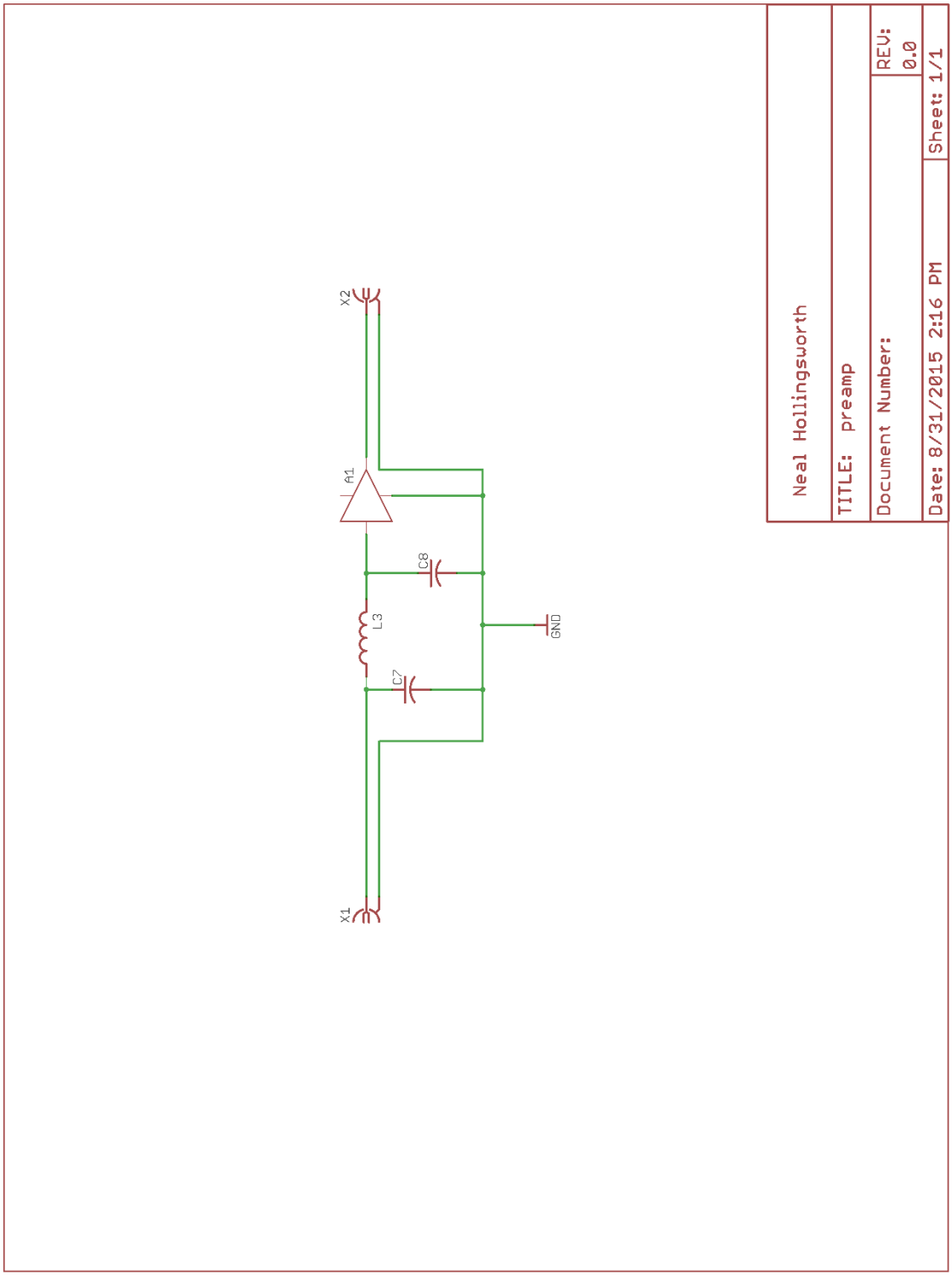


Figure K-8: Preamplifier schematics.

Qty	Value	Parts	Description
1		L4	
2		C9, C10	CAPACITOR, American symbol
2	UM9415	D1, D2	PIN DIODE
4	UM9188	D3, D4, D5, D6	PIN DIODE, Passive
3	2200pF	C1, C5, C6	CAPACITOR, American symbol
2	25pF	C3, C4	CAPACITOR, American symbol
1	62nH	L1	
3		X1, X2, X3	SMA 50 Ohm End Launch Jack Receptacle - Round Contact

Table K-7: Bill of Materials for the T/R Switch.

Qty	Value	Parts	Description
1		L3	
2		C7, C8	CAPACITOR, American symbol
1		A1	
2	SMA-142-0701-801/806	X1, X2	SMA 50 Ohm End Launch Jack Receptacle - Round Contact

Table K-8: Bill of Materials for Preamp.

K-8 PIN Diode Driver Module Schematic and BOM

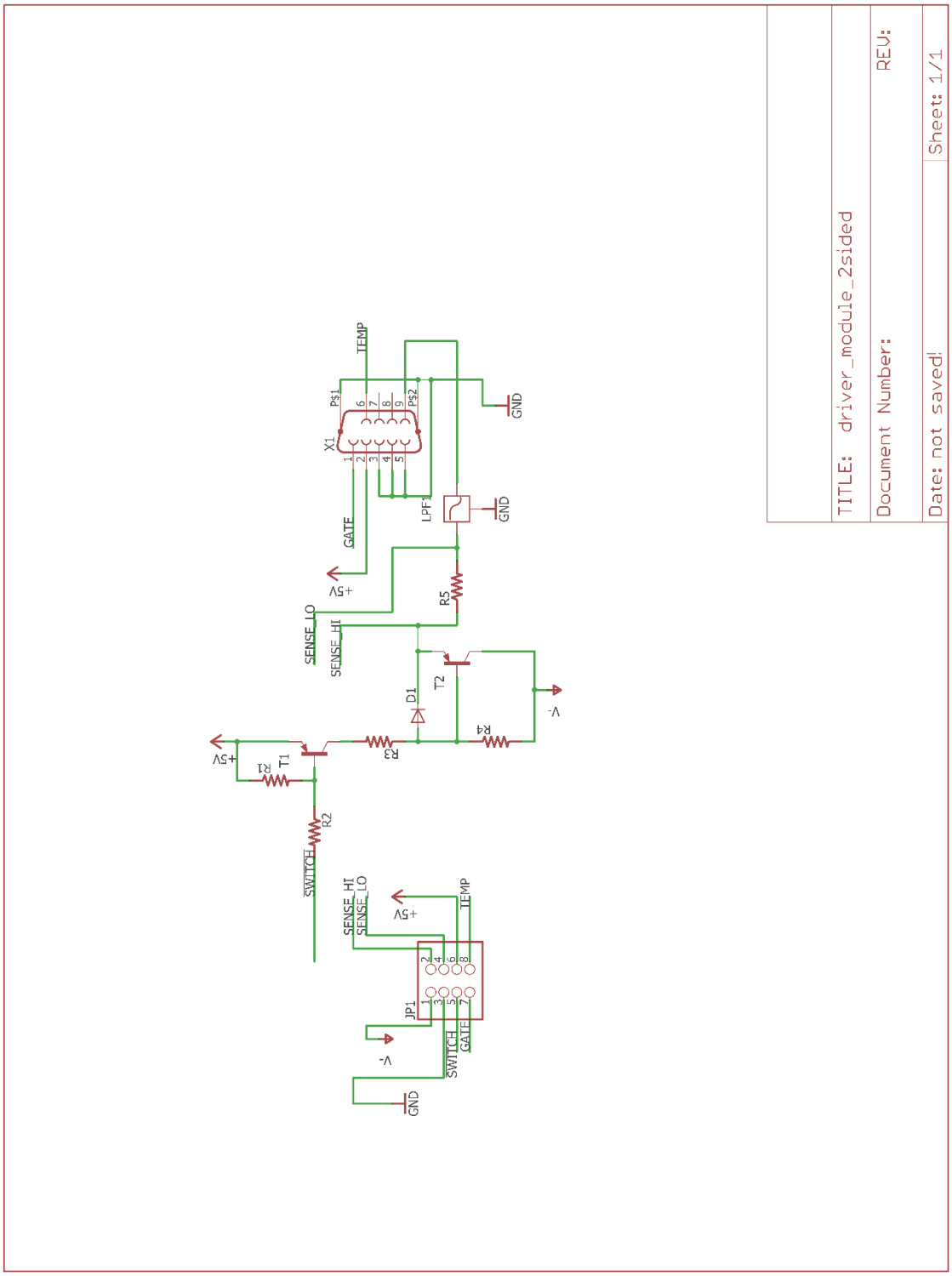


Figure K-9: PIN diode driver schematic.

Qty	Value	Parts	Description
2		T1, T2	PNP Transistror
1		LPF1	TDK Low Pass Filter
1		X1	SUB-D
1		JP1	PIN HEADER
1	0.1Ω	R5	RESISTOR, American symbol
1	15Ω	R3	RESISTOR, American symbol
1	150Ω	R2	RESISTOR, American symbol
1	1N4007	D1	DIODE
1	3.9kΩ	R4	RESISTOR, American symbol
1	300Ω	R1	RESISTOR, American symbol

Table K-9: Bill of Materials for the PIN diode driver.

K-9 Blanking Switch Schematic and BOM

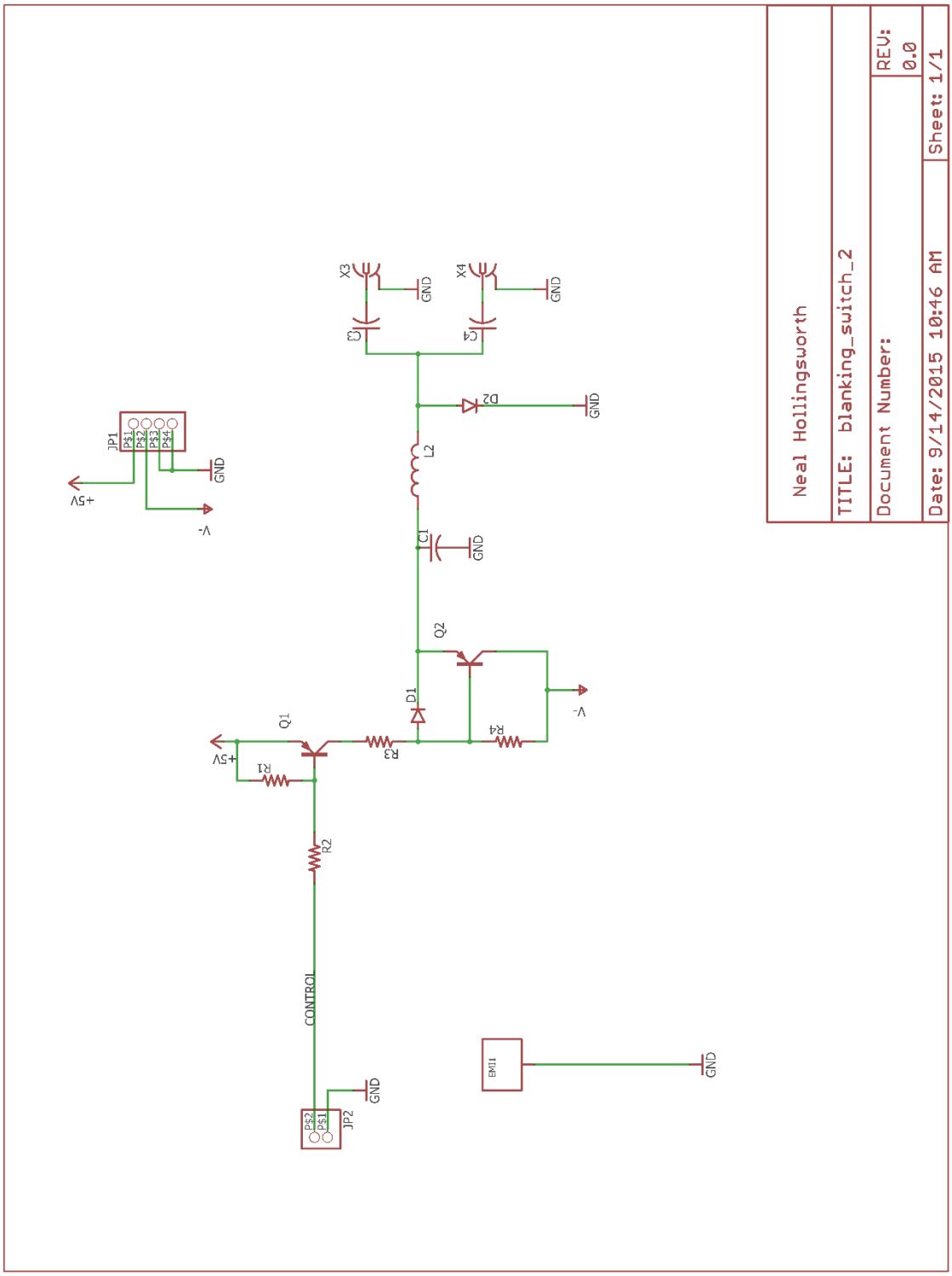


Figure K-10: RF blanking switch schematic.

APPENDIX L
CODE FOR MODULATOR TESTING

L-1 Read and Plot Data from the LeCroy O-Scope

```
function [data] = lecroy_plot1(file)
%lecroy_plot1 reads in a binary wfm file from the lecroy
%wavejet, extracts the data from channel one and plots it
%against time. It returns the data from channel 1.

%read the wfm file
[data nfo]= readLeCroyWaveJetWfm(file);
%extract the data from channel 1
data = data(:,1);

%generate the time points based on the data file header
timevec=[0:nfo.dx:(length(data)-1)*nfo.dx];
%plot the data vs time
plot(timevec,data);

end
```

L-2 Dynamic Range Calculation

```
%{
File name: drange_board1.m
Date:7/27/2012
Author: Neal Hollingsworth
Description:
    This script imports the waveforms and calculates the
dynamic range for all channels of the new modulator card
one. The output is the minimum and maximum output levels
and the dynamic range calculated as the difference.
%}
clear all;close all;

%import the minimum output data for channel 1
[data10]=lecroy_plot1('LOLT0013.WFM');
%calculate the average RMS voltage of the output
Vrms10=sqrt(mean(data10.^2));
%calculate the power from the RMS voltage. 0.224 is the
%magnitude of a 0dBm wave
dbm10=20*log10(Vrms10/0.224)

%import the maximum output data for channel 1
[data11]=lecroy_plot1('LOLT0014.WFM');
%calculate the average RMS voltage of the output
Vrms11=sqrt(mean(data11.^2));
%calculate the power from the RMS voltage. 0.224 is the
%magnitude of a 0dBm wave
dbm11=20*log10(Vrms11/0.224)
%calculate the dynamic range for channel 1
d_range1 = dbm11-dbm10
```

L-3 Ramp Waveform Generation

```
%{
File name: wf_aramp_gen.m
Date:8/8/2012
Author: Neal Hollingsworth
Description:
    This script reads generatees the amplitude ramp
waveforms for all channels at 0, 45 and 90 degrees phase
shift. It writes them out in tab delimited aap files.
```

```
%}
clear all; close all;
time_points=(0:0.00125:0.5)';

%generate a ramp from max to min amplitude that is 200
%points long. This is roughly half the time length that the
%LeCroy scope can digitize at full speed.
half_ramp = linspace(10,0,200)';
%make the double ramp, forcing the center point to zero
ramp = [half_ramp;0;flipud(half_ramp)];
%pad the file out with zeros
pad = zeros(401,1);
wf=[pad;ramp;pad];
%construct the last line in the file with the update rate
%marked as 55ticks
append_row = [55,zeros(1,15)];
%build the full waveform file for each of the four channels
wf_block1 = [wf,zeros(length(wf),15);append_row];
wf_block2 = [zeros(length(wf),2),wf,...
             zeros(length(wf),13);append_row];
wf_block3 = [zeros(length(wf),4),wf,...
             zeros(length(wf),11);append_row];
wf_block4 = [zeros(length(wf),6),wf,...
             zeros(length(wf),9);append_row];

%write out an aap file for each of the four channels
dlmwrite('aramp_ch1.aap',wf_block1,...
    'delimiter','\t','newline','pc');
dlmwrite('aramp_ch2.aap',wf_block2,...
    'delimiter','\t','newline','pc');
dlmwrite('aramp_ch3.aap',wf_block3,...
    'delimiter','\t','newline','pc');
dlmwrite('aramp_ch4.aap',wf_block4,...
    'delimiter','\t','newline','pc');

%rebuild the waveform blocks with a 90 degree phase shift
%the phase shift is introduced as zeros(length(wf,1)+pi/2
wf_block5 = [wf,zeros(length(wf),1)...
             +pi/2,zeros(length(wf),14);append_row];
wf_block6 = [zeros(length(wf),2),wf,zeros(length(wf),1)...
             +pi/2,zeros(length(wf),12);append_row];
wf_block7 = [zeros(length(wf),4),wf,zeros(length(wf),1)...
             +pi/2,zeros(length(wf),10);append_row];
wf_block8 = [zeros(length(wf),6),wf,zeros(length(wf),1)...
             +pi/2,zeros(length(wf),8);append_row];

%write out an aap file for each of the four channels
dlmwrite('aramp_ch1_90d.aap',wf_block5,...
        'delimiter','\t','newline','pc');
dlmwrite('aramp_ch2_90d.aap',wf_block6,...
        'delimiter','\t','newline','pc');
dlmwrite('aramp_ch3_90d.aap',wf_block7,...
        'delimiter','\t','newline','pc');
dlmwrite('aramp_ch4_90d.aap',wf_block8,...
        'delimiter','\t','newline','pc');

%rebuild the waveform blocks with a 90 degree phase shift
%the phase shift is introduced as zeros(length(wf,1)+pi/4
wf_block9 = [wf,zeros(length(wf),1)+pi/4,...
             zeros(length(wf),14);append_row];
wf_block10 = [zeros(length(wf),2),wf,zeros(length(wf),1)...
             +pi/4,zeros(length(wf),12);append_row];
wf_block11 = [zeros(length(wf),4),wf,zeros(length(wf),1)...
             +pi/4,zeros(length(wf),10);append_row];
wf_block12 = [zeros(length(wf),6),wf,zeros(length(wf),1)...
             +pi/4,zeros(length(wf),8);append_row];
```

```
%write out an aap file for each of the four channels
dlmwrite('aramp_ch1_45d.aap',wf_block9,...
    'delimiter','\t','newline','pc');
dlmwrite('aramp_ch2_45d.aap',wf_block10,...
    'delimiter','\t','newline','pc');
dlmwrite('aramp_ch3_45d.aap',wf_block11,...
    'delimiter','\t','newline','pc');
dlmwrite('aramp_ch4_45d.aap',wf_block12,....
    'delimiter','\t','newline','pc');



%{
File name: wf_pramp_gen.m
Date:8/8/2012
Author: Neal Hollingsworth
Description:
    This script reads generatees the phase ramp
waveforms for all channels at 10, 5 and 1 amplitude. It
writes them out in tab delimited aap files.
%}
time_points=(0:0.00125:0.5)';

%generate a ramp from max to min amplitude that is 401
%points long. This is roughly the time length that the
%LeCroy scope can digitize at full speed.
pramp = [pad;linspace(0,2*pi,401)';pad];
%pad the file out with zeros
pad = zeros(401,1);
wf=[pad;zeros(401,1)+10;pad];
%construct the last line in the file with the update rate
%marked as 55ticks
append_row = [55,zeros(1,15)];
%build the full waveform file for each of the four channels
wf_block1 = [wf,pramp,zeros(length(wf),14);append_row];
wf_block2 = [zeros(length(wf),2),wf,...
            pramp,zeros(length(wf),12);append_row];
wf_block3 = [zeros(length(wf),4),wf,...
            pramp,zeros(length(wf),10);append_row];
wf_block4 = [zeros(length(wf),6),wf,...
            pramp,zeros(length(wf),8);append_row];
%write out an aap file for each of the four channels
dlmwrite('pramp_10A_ch1.aap',wf_block1,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_10A_ch2.aap',wf_block2,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_10A_ch3.aap',wf_block3,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_10A_ch4.aap',wf_block4,...
    'delimiter','\t','newline','pc');
%rebuild the waveform file using a 5 amplitude
wf=[pad;zeros(401,1)+5;pad];
wf_block5 = [wf,pramp,zeros(length(wf),14);append_row];
wf_block6 = [zeros(length(wf),2),wf,pramp,...
            zeros(length(wf),12);append_row];
wf_block7 = [zeros(length(wf),4),wf,pramp,...
            zeros(length(wf),10);append_row];
wf_block8 = [zeros(length(wf),6),wf,pramp,...
            zeros(length(wf),8);append_row];
%write out an aap file for each of the four channels
dlmwrite('pramp_5A_ch1.aap',wf_block5,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_5A_ch2.aap',wf_block6,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_5A_ch3.aap',wf_block7,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_5A_ch4.aap',wf_block8,...
```

```
    'delimiter','\t','newline','pc');
%rebuild the waveform file using a 1 amplitude
wf=[pad;zeros(401,1)+1;pad];
wf_block9 = [wf,pramp,zeros(length(wf),14);append_row];
wf_block10 = [zeros(length(wf),2),wf,pramp,...
            zeros(length(wf),12);append_row];
wf_block11 = [zeros(length(wf),4),wf,pramp,...
            zeros(length(wf),10);append_row];
wf_block12 = [zeros(length(wf),6),wf,pramp,...
            zeros(length(wf),8);append_row];
%write out an aap file for each of the four channels
dlmwrite('pramp_1A_ch1.aap',wf_block9,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_1A_ch2.aap',wf_block10,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_1A_ch3.aap',wf_block11,...
    'delimiter','\t','newline','pc');
dlmwrite('pramp_1A_ch4.aap',wf_block12,...
    'delimiter','\t','newline','pc');
```

L-4 Error Calc

```
clear all;
close all;
scrsz = get(0,'ScreenSize');


[prmp1_data] = readLeCroyWaveJetWfm('prmp1001.wfm');

step = 1/1E9;
times=0:step:step*(length(prmp1_data)-1);
xlimits=[0 times(end)];
ylimits=[-5 5];

prmp_1=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp1_data(:,1));
xlim(xlimits);
title('Modulator 1.1 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch11_prmp_10a.svg',prmp_1);

[prmp2_data] = readLeCroyWaveJetWfm('prmp1002.wfm');

prmp_2=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp2_data(:,1));
xlim(xlimits);
title('Modulator 1.2 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch12_prmp_10a.svg',prmp_2);

[prmp3_data] = readLeCroyWaveJetWfm('prmp1003.wfm');

prmp_3=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp3_data(:,1));
xlim(xlimits);
title('Modulator 1.3 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch13_prmp_10a.svg',prmp_3);

[prmp4_data] = readLeCroyWaveJetWfm('prmp1004.wfm');

prmp_4=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp4_data(:,1));
xlim(xlimits);
title('Modulator 1.4 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch14_prmp_10a.svg',prmp_4);
```

```
[prmp5_data] = readLeCroyWaveJetWfm('prmp1005.wfm');

prmp_5=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp5_data(:,1));
xlim(xlimits);
title('Modulator 2.1 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch21_prmp_10a.svg',prmp_5);

[prmp6_data] = readLeCroyWaveJetWfm('prmp1006.wfm');

prmp_6=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp6_data(:,1));
xlim(xlimits);
title('Modulator 2.2 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch22_prmp_10a.svg',prmp_6);

[prmp7_data] = readLeCroyWaveJetWfm('prmp1007.wfm');

prmp_7=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp7_data(:,1));
xlim(xlimits);
title('Modulator 2.3 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch23_prmp_10a.svg',prmp_7);

[prmp8_data] = readLeCroyWaveJetWfm('prmp1008.wfm');

prmp_8=figure('Position',[50 (scrsz(4)/2)-100 scrsz(3) scrsz(4)/2]);
plot(times,prmp8_data(:,1));
xlim(xlimits);
title('Modulator 2.4 phase ramp with 10 amplitude');
xlabel('Time(sec)');ylabel('Amplitude(V)');
plot2svg('svgs\ch24_prmp_10a.svg',prmp_8);
```

L-5 Edge Finding

```
function [low_edge,high_edge] = wfmedges(wfm)
%wfmedges is used to find the first and last edges in a
%waveform. The edge command returns a vector with each edge
%marked with a 1 and all other elements 0. This vector is
%then ittereated over to find the first and last position
%with an edge. It is assumed that the first edge will appear
%in the first half of the data and the last edge in the last
%half.
    edges=edge(wfm);

    low_edge=0;
    high_edge=0;
    for i=1:(length(edges)/2)
        if(edges(i)==1)&&(low_edge==0)
            low_edge=i;
        end
        if(edges(i+250000)==1)
            high_edge=250000+i;
        end
    end
end
```

APPENDIX M
CONFIGURATION AND USE OF THE ULTRAVIEW DIGITIZER

M-1 Software Setup

M-1.1 Software:

The software used for this was obtained from the Ultraview website www.ultraviewcorp.com/downloads.php in the "16-Bit PCIe Data Acquisition Boards" section. The specific pacakage is "AD16-250x4_231213_071714_64bit_Software.zip". Initial testing was done with the "LabVIEW_Acquire_data_x64.exe" under "AD16-250x4_231213_071714_64bit_Software\ complete_daq_utilities\ LabView_2012_64_bit". This requires the LabVIEW 2012 runtime to be installed, as well as drivers for the Ultraview card.

M-1.2 Software Modifications:

The LabVIEW Vis must be modified to enable the segmented capture options. This is done it the "Ultraview PCIe DAQ" LabView project found under "250x4_231213_071714_64bit_Software\ src\ LabVIEW_2012_64-bit". From the project explorer, open the PCIe DAQ.lvlib>Top Level Vis>SetupandControl.vi. Right click on the "Capture Count" control and select "Advanced>Enabled State>Enabled". Repeat this for the "Capture Depth" and save the VI.

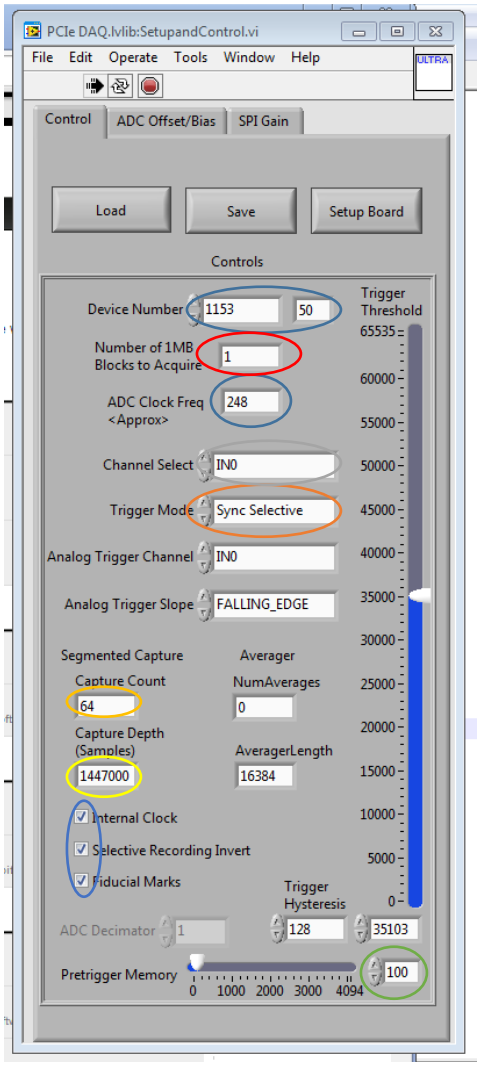
The SetupandControl.VI and ReadandGraph.VI must be recompiled. First, the build specifications must be modified. In the Project Explorer, under "Build Specifications", double click to open "SetupandControl". The destination directory needs to be changed to match the location of AD16-250x4_231213_071714_64bit_Software\ complete_daq_utilities\ LabView_2012_64_bit\ build on the current system (e.g. the initial setting was for C:\ Users\ Joel\ AD16-250x4_231213_071714_64bit_Software\ complete_daq_utilities\ LabView_2012_64_bit\ build and we changed it to C:\ Users\ Katie\ AD16-250x4_231213_071714_64bit_Software\ complete_daq_utilities\ LabView_2012_64_bit\ build). This should be repeated for the ReadandGraph build specification.

Following these modifications, right click on the two build specifications and select Build. The updated files should be correctly located, and "LabVIEW_Acquire_data_x64.exe" can be used as previously mentioned.

M-1.3 Software Configuration:

The card needs to be correctly configured after starting the acquisition program. The software should auto-detect the card and show Device number 1153-50 with an ADC clock of 250MHz (note that it appears to display 248MHz in single channel mode, but this is incorrect). The Trigger Mode should be set to Sync Selective, which may display as <5>, Internal Clock, Selective Recording Invert, and Fiducial Marks need

to be checked. These are the basic operating settings. I also set the “Pretrigger Memory” to 100 to avoid any possible problems with data edges.

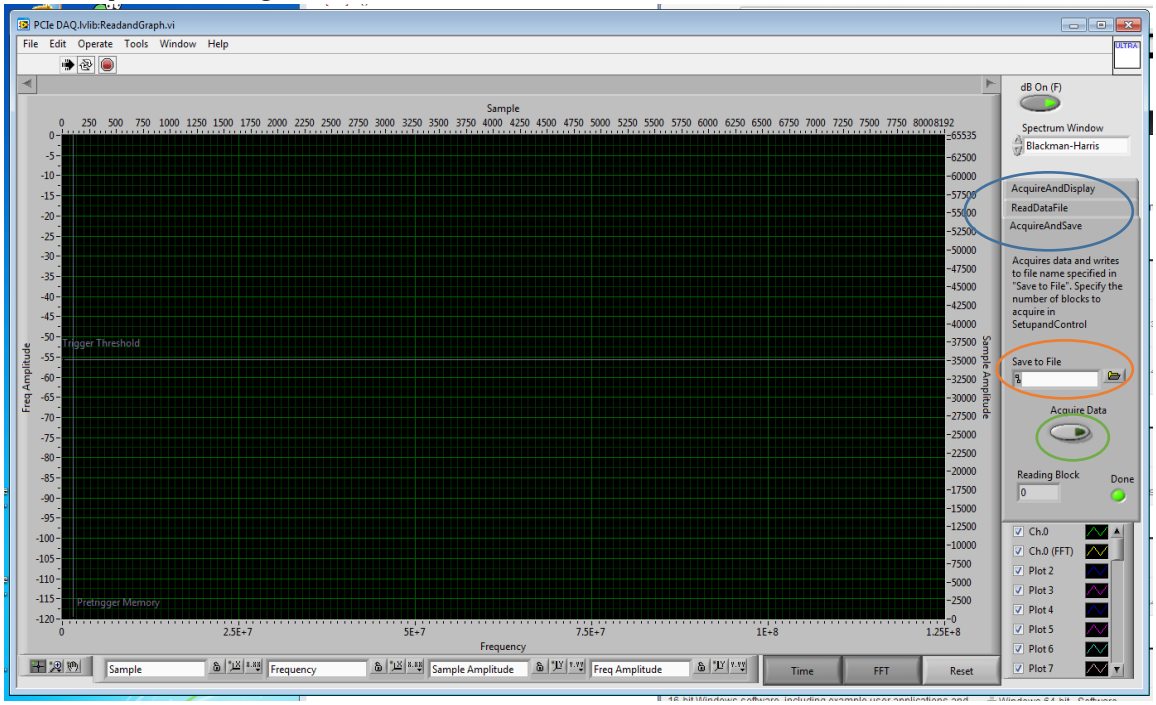


1. Device number should read 1153-50 and clock frequency either 250 or 248
2. Trigger mode should be set to “Sync Selective”, note that this may show as “<5>”
4. All three check boxes should be selected
5. 100 points of pretrigger memory help us avoid any edge effects in the data
6. Select the desired channels for the experiment
7. Capture count is set to the number of phase encode lines to be acquired
8. Capture depth must be calculated to be the number of samples needed for each line of data
9. Finally, the number of 1MB blocks must be set to accommodate the data being captured

Figure M-1: Configuration panel of the Ultraview software.

The card must also be configured for the specifics of the experiment being run, the Channel Select, Capture Count, Capture Depth, and Number of 1MB Blocks to Acquire need to be selected. The Capture Count corresponds to the number of phase encode lines desired, Capture Depth is the number of samples of the 250MHz ADC that should be taken for each channel at each trigger. The Channel Select should correspond to the receiver channels in use. Finally, the number of 1MB blocks must equal or exceed the amount of memory needed to store all of the data for the experiment. Example calculations will be provided later.

Clicking Setup Board will now configure the board for the experiment. In the other open window, on the right hand side, the AcquireAndSave tab should be selected and a file given. The "Acquire Data" button can then be clicked, and the system will wait for triggers and collect the number of captures and 1MB blocks requested, writing them out to the file.



1 Select the "AcquireandSave" tab from the different operating modes

2 Select and name a file to save the data into.

3 Click the "Acquire Data" button to arm the system for capturing data.

Figure M-2: Configuration of the data acquisition window.

M-1.4 File Format

The file format is a binary file of unsigned shorts (16-bit integers). In single channel mode, the data is contiguous for all samples. In multi-channel mode the data is interleaved between channels. Fiducials are written into the data as a set of min,min+1, max, max-1 values directly into the data. The fiducial is only written once per trigger, not once per channel used. A single channel data file will look as follows:

Fiducial								Data					
0		1		65535		65534		Point 1		Point 1		Point 1	
LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB

Figure M-3: Structure of file with data from a single channel.

While a multi channel data set will be

Fiducial								Ch. 0		Ch. 1		Ch.3	
0		1		65535		65534		Point 1		Point 1		Point 1	
LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB

Figure M-4: Structure of a file with data from multiple channels.

M-2 Imaging Experiment – 64x64 with Ringdown Digitization

M-2.1 Scanner Setup

The sequence used is a modified version of Ssems where the phase encoding occurs directly before the acquisition window. This allows the ringdown after the 180 to be digitized. To load it, first load sems and calibrate the RF on the desired coil. Then load Ssems, then set seqfil = 'Ssems_rxg3'. This also has the command to trigger the rxg line 4.5mSec before the acquisition starts. Finally, the receive gain my need to be adjusted for the Ultraview card. In this experiment, it was set to 30dB which appears to result in the maximum signal level out of the magnet leg. Configuration of the sequence is otherwise normal.

M-2.2 Ultraview to Scanner Connections

The rxg line from the Varian is passed through a voltage divider to bring the 5V logic down to 2.5V, which is what the Ultraview card requires. The output of the divider is connected to the trigger cable labeled 'TR'. RF is taken from the output of the magnet leg where it is at roughly 20MHz. This signal magnitude should be checked, but is expected to be much smaller than the +/-375mV that the Ultraview can take. For this setup we included the HP bench top amplifier to bring the signal to a better level for the digitizer. This is known to not be optimal. We only digitized a signal channel, so passed it into the IN0 line, which is the first analog input channel.

M-2.3 Sampling and Memory Configuration

The image has 64 PE lines, so the Ultraview card is set for 64 captures. An acquisition time of 1.28mSec was set, and there is 4.5mSec prior to that which must be sampled for the phase correction. This leads to a total sampling window of 5.78mSec. The sampling clock is 250MHz, so we need $FS\left(delay + tramp + tpe + tacq\right) = \left(250 \cdot 10^6\right) 0.00578 = 1,445,000$ samples, plus 100 pretrigger samples and 100 trailing samples, for a total capture depth of 1,445,200 samples. The total number of samples will then

be $1,445,200 \cdot 64 = 92,480,000$ with each sample being 16 bits. So we can calculate an approximate number of 1MB blocks to record as $92,480,000 \cdot 2/2^{20} = 176.42 \rightarrow 177$.

M-3 Processing

Processing the data can be divided into a few major steps: 1) reading in and formatting the data 2) obtaining the phase correction values 3) obtaining the correctly sized image data 4) phase correcting the data 5) reconstructing the image.

M-3.1 Formatting the Data

The data file, as previously mentioned, is written as a binary set of little-endian 16-bit unsigned integers. Fiducials are embedded into this, and need to be found in order for the data to be reshaped correctly. The (naive) approach used was to simply find all points taking the max value of an unsigned short (65,535). The data is then reformed into an array that is 64x1,445,000 points, where each line is taken from the 100^{th} point after the fiducial to the $1,445,00^{th}$ point. This forms the total, raw, data set.

M-3.2 Computing the Phase Correction Value

The phase correction value will use the first 100,000 points of each line of data, since this is in the ringdown before phase encoding is done. The first step is to Fourier transform these data points and take only two hundred points from around the spectrum of the carrier frequency. Specifically, we use the points in the range of 42,000+/-100. This data is then transformed back into the time domain. We then select a point (100 in this case) to use to calculate the correction factor by dividing that point by its absolute value, and conjugating. The resulting vector is the phase correction factor that will be applied to each line of the image data.

M-3.3 Obtaining the Desired Image Data

Here again we use a naive approach that simply discards much of the data. We first obtain only the data from during the acquisition window. That corresponds to the data beginning 4.5mSec after the trigger with this pulse sequence. So, the image data begins at point $\left(250 \cdot 10^6\right)0.0045 = 1,125,000$ and should run to the end of the data for each line. We can confirm this is correct based on the record length, which should be $\left(250 \cdot 10^6\right)0.00128 = 320,000$ for the acquisition window. This data is Fourier transformed along the time dimension only, yielding a spectrum for each phase encode line. We then select the 64 points surrounding the center frequency, which is found at $\left(320000 + \left((20/125)320000\right)\right)/2 = 185,600$. The result is the Fourier transformed back to give a 64x64 matrix that represents k-space (i.e. the time domain data at baseband).

M-3.4 Applying the Phase Correction

The phase correction data can be directly multiplied by k-space to generate the needed off-set. That is, each point in the phase correction vector is simply multiplied by the corresponding row in the k-space data.

M-3.5 Reconstruction

At this point, a simple 2D FFT reconstruction can be used in order to obtain the image as usual.

M-3.6 Resulting Image

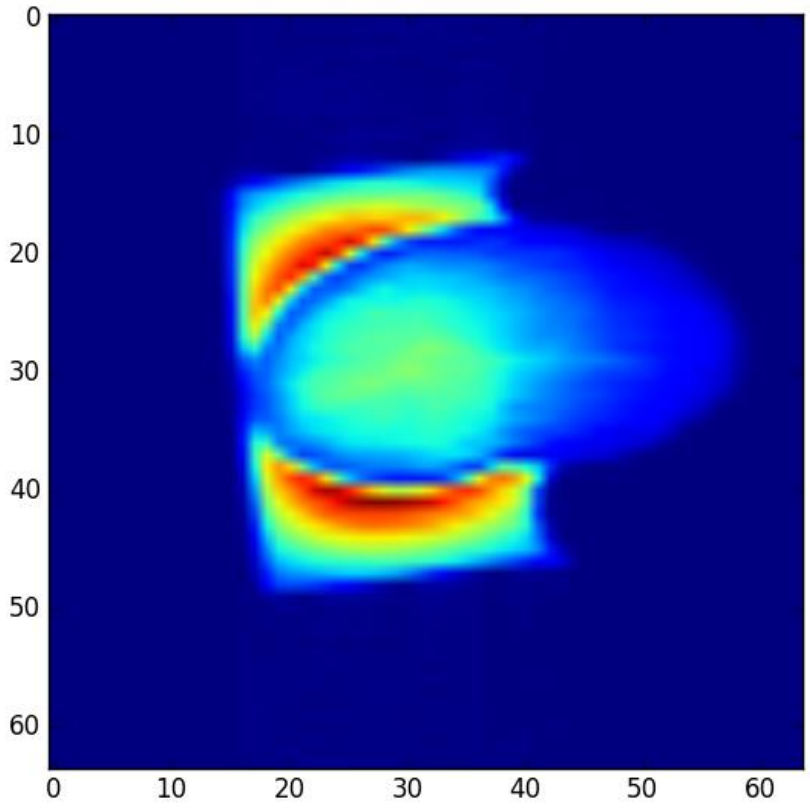


Figure M-5: Initial image obtained with the Ultraview receiver.

M-4 Imaging Parameters

Parameter	Value	Note
Sequence	Ssems_rxg3	Load Ssems with macro first
Matrix Size	64x64	
TR	500mSec	
TE	30mSec	
FOV	180mmx180mm	
Slice Thickness	3mm	
Delay	1mSec	Delay from RXG to PE blip

Table M-1: Imaging parameters for the example Ultraview data capture.

Parameter	Value	Note
RF coil	Quad20cm	
Pulse length	4000uSec	
Pattern	Sinc	
Tpwr1	47dB	
Tpwr2	53dB	
Spectral Width	50,000Hz	
Acquisition Time	1.28mSec	
Receiver Gain	30dB	Above 30dB doesn't change output of magnet leg (I think?)
Tped	3mSec	PE blip time
Tramp	0.5mSec	Ramp time of gradients
Delay	1mSec	Delay from RXG to PE blip

Table M-1: Continued

M-5 Imaging Experiment – 128x128 with Ringdown Digitization

M-5.1 Setup

The setup for this experiment is fundamentally the same as the previous one. The main difference being that the scanner was set to a 128x128 image. This gives an acquisition window of 2.58mSec, which changes the capture depth, number of captures, and number of blocks. The number of captures is set to 128 to match the number of phase encode lines. The capture depth is now 1,765,200 and the number of 1Mb blocks is 431. Beyond this, all configuration is the same. The only changes in the processing script are to set the correct values for the changes noted here.

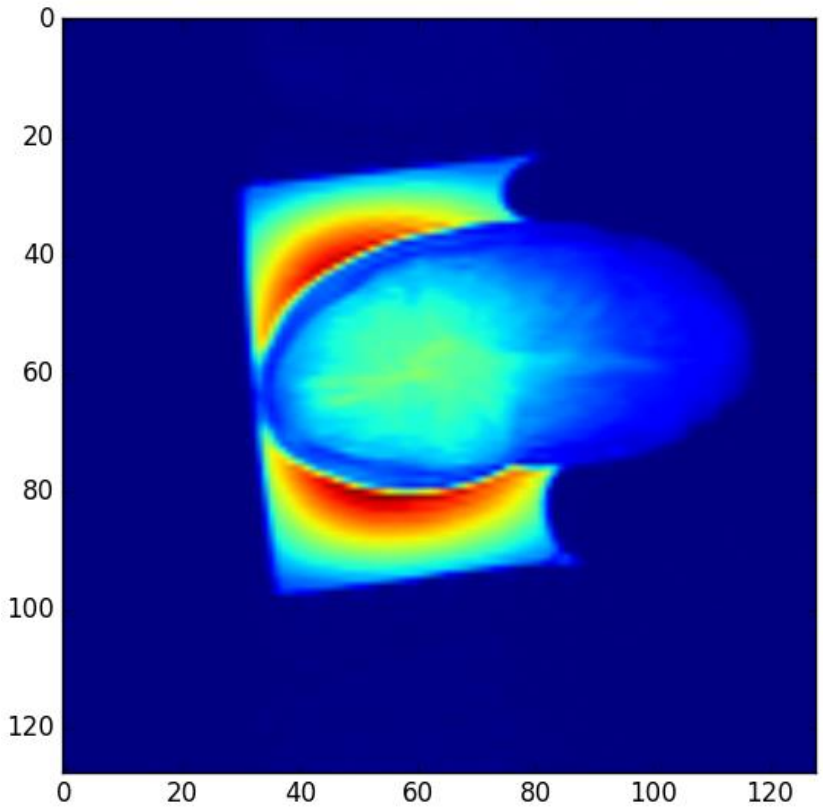


Figure M-6: Higher resolution image from the Ultraview receiver.

The results are as expected, an image with no phase noise at the higher resolution.

M-6 Imaging Experiment – 128x128 4 Channel with Ringdown Digitization

M-6.1 Setup

We want to test the ability to digitize and reconstruct an image from all four channels of the card. However, we do not have a four channel receive only array that is convenient for this test. Instead, we have taken the output of the magnet leg, as before, split it four ways, and connected each of the digitizer card inputs to one of these ports. This puts the same signal on each channel, with the exception of each line having a slightly different phase shift and minor differences in magnitude.

The Ultraview software is then setup to record from all four channels, and the number of 1mB blocks is quadrupled. In all other respects the setup is the same as for the previous (128x128 resolution) experiment. It is worth noting that this yields a file size of around 1.7GB on disk.

M-6.2 Processing

The large file size created some issues with processing the data. We originally would just read all of the data into memory and process from there. However, this was problematic due to memory limitations. The code was altered to load data from only a single channel at a time. This was still much more memory intensive than expected, using around 12GB of system memory. This is problematic, as it limits which computers we can use to process a data set, and it also limits the total resolution we can have. Above 128x128 images will quickly cause us to run out of memory. There is no reason to think this a fundamental limitation, and is most likely due to poor coding practices. At present, I have not run a memory profiler to locate the main problem with this technique.

It is also worth noting that the format of the fiducial markers creates some difficulty in processing the data. Each fiducial is four data points long, however the method currently used to read in the data only takes every 4^{th} point. This means that each channel has a single point fiducial, and each is different. The method used (looking for each of the possible values as a marker) is probably a sub-optimal way of parsing the data, but it does work.

M-6.3 Images

The shown images are reconstructed from the Ultraview data. Each image is a different channel. As expected, they are nearly identical. Slight variation in magnitude and noise is expected, but no structural differences are evident.

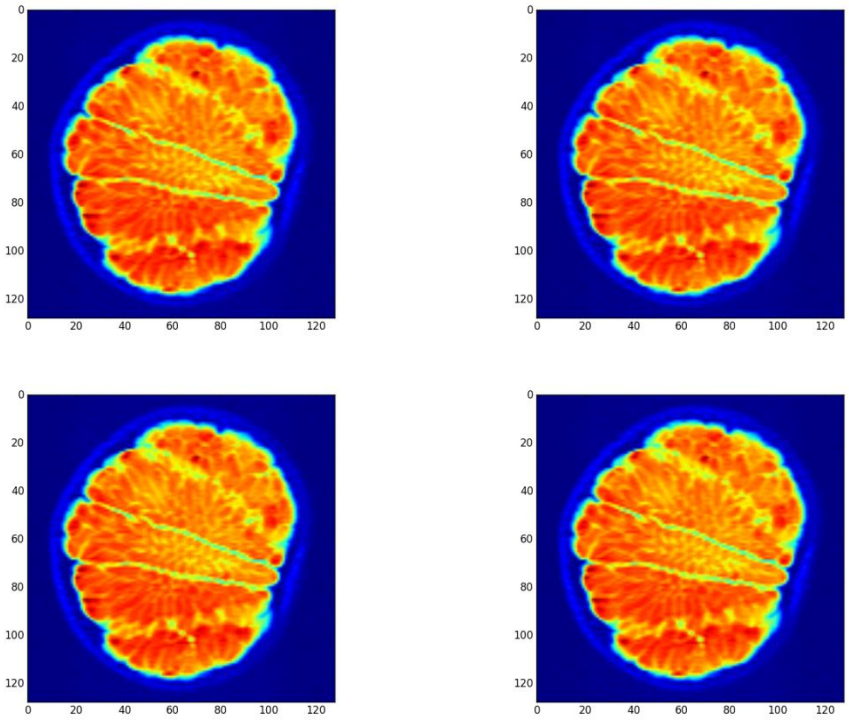


Figure M-7: Multi-channel data capture with Ultraview receiver.

M-7 Memory/Location Calculations

M-7.1 Points in Acquisition Window

AP : Number of acquisition points

FS : Sampling frequency, in Hz

t_{acq} : Acquisition time, in seconds

$$AP = FS * t_{acq} \tag{M.1}$$

M-7.2 Capture Depth

CD : Capture Depth, in number of samples per channel

FS : Sampling Frequency, in Hz (250MHz for internal Clock)

t_{delay} : Delay during which the ringdown will be digitized, in seconds (1mSec for Ssems_rxg3)

t_{ramp} : Delay for gradient ramps, in seconds (default is 0.5msec)

t_{pe} : Phase encode gradient length, in seconds (normally 3mSec, but may change)

t_{acq} : Acquisition time, in seconds

$$CD = FS * \left(t_{delay} + t_{ramp} + t_{pe} + t_{acq} \right) + 200 \tag{M.2}$$

NOTE: The constant 200 points is added to the sample window, and cut during processing. This must simply match the processing used (the example shown uses 100 before and after the data)

M-7.3 Number of 1MB Blocks

NB : Number of 1MB Blocks needed

CD : Capture depth

NP : Number of Phase encode steps

NC : Number of channels used

$$NB = ceil\left(\frac{CD * 2 * NP * NC}{2^{20}}\right) \tag{M.3}$$

NOTE: the value 2^{20} is the number of bytes in a 1MB, *ceil* indicates that the value should always be rounded up to the next integer value

M-7.4 Carrier Location in Spectrum

F_{loc} : Index of the carrier frequency

AP : Number of points in the acquisition/spectrum

FC : Carrier frequency

FN : Nyquist frequency of the data

$$F_{loc} = \frac{\mathrm{AP} + \left(\left(\frac{\mathrm{F_c}}{\mathrm{F_N}}\right) * \mathrm{AP}\right)}{2} \tag{M.4}$$

NOTE: This yields the positive frequency point (i.e. the frequency above the mid-point of the spectrum). The Nyquist frequency is simply the sampling rate, in Hz, divided by 2. The units of the carrier and Nyquist frequency must be the same, but can be Hz, kHz, MHz, or something else. This is used for finding the carrier frequency in both the phase correction data, and the echo itself.

M-8 Processing Code, Single Channel(Python)

```
import struct

import numpy as np
import matplotlib.pyplot as plt
from numpy.fft import fft, fftshift, fft2, ifft, ifftshift

# This function finds every point in data with the max value that an unsigned
# short can take. This is a naive approach to finding the fiducials in the data
def findFiducials(data):
    return [i for i in range(len(data)) if data[i]==65535]

# This loads the data saved by the Ultraview card. It does not reshape the data
# and simply returns an array off all the data points as unsigned shorts.
def loadData(fileName):
    data = []
    test = []
```

```
    with open(fileName, 'rb') as f:
        data = f.read()
        test = struct.unpack('<'+str(int(len(data)/2))+'H', data)
    return np.asarray(test)

#**************************************************************************
# Begin the processing code here
#**************************************************************************

# Read in the complete data set
data = loadData('test5.dat')

# Find the max value points, which we assume are the fiducials
markers = findFiducials(data)

# Reshape and section the data to only contain the data that we actually want
# in a 64x1,445,100 array
raw = []
for i in range(len(markers)):
    raw.append(data[markers[i]+100:markers[i]+1445100])

# Segment out the data for phase correction, and the actual acquistion period
phaseBlocks = np.asarray(raw)[:,:100000]
rawIM = np.asarray(raw)[:,0.0045*250000000:]

# FT the phase correction data, select only the 200 points around the carrier
# frequency, then IFT that back into the time domain.
phaseSpect = ifftshift(ifft(ifftshift(phaseBlocks)))
phaseSpect = phaseSpect[:,42000-100:42000+100]
phaseDat = fftshift(fft(fftshift(phaseSpect)))
# Compute the phase correction constant from the 100th point. Conjugating makes
# sure the phase shift is in the right direction. The reshape lets us just
# multiply this by the k-space data later.
shifts = (phaseDat[:,100]/np.abs(phaseDat[:,100])).conjugate().reshape((64,1))

# FT the phase image data, select only the 200 points around the carrier
# frequency, then IFT that back into the time domain.
temp = fftshift(fft(fftshift(rawIM)))
kspace = temp[:,185600-32:185600+32]
kspace = ifftshift(ifft(ifftshift(kspace)))
# Apply the phase correction
corrected = kspace*shifts
# Reconstruct the image
im = fftshift(fft2(fftshift(corrected)))
# Display the magnitude image
plt.imshow(np.abs(im))
plt.show()
```

M-9 Processing Code, Memory Efficient(Python)

```
"""
.. py:module::Ultraview
Ultraview Module
================

This module is designed to import and process data from the Ultraview card.
Current functions reading in the data, finding the fiducials, and computing
phase correction values. The module can also be run in a script mode by editing
the values in the second half of the file to process the desired data file.

"""

import struct
from mmap import mmap

import numpy as np
```

```
import matplotlib.pyplot as plt
from numpy.fft import fft, fftshift, fft2, ifft, ifftshift
from memory_profiler import profile
import h5py

def makeHeader():
    head = dict()
    head['File'] = 'test9.dat'  # File to be processed
    head['Sequence'] = 'Ssems_rxg3'
    head['channelCount'] = 4

    head['IF'] = 20e6          # Frequency of the sampled data
    IF = 20e6
    head['FS'] = 250e6         # Frequency of the sampling clock
    FS = 250e6
    head['NFreq'] = FS/2       # Nyquist frequency of the receiver
    NFreq = FS/2

    head['Tacq'] = 0.00512   # Acquisition time in seconds
    Tacq = 0.00512
    head['NPE'] = 256          # Number of phase encode steps
    head['NFE'] = 256          # Number of frequency encode steps
    head['preTrigger'] = 100 # Number of pretrigger samples
    preTrigger = 100

    head['ringDown'] = 0.001 # Delay for phase correction data in seconds
    ringDown = 0.001
    head['Tpe'] = 0.003     # Length of phase encode blip in seconds
    Tpe = 0.003
    head['Tramp'] = 0.0005  # Length of gradient ramp in seconds
    Tramp = 0.0005

    head['pCorLength'] = 100000 # Number of points used for phase correction
    head['pCorOffset'] = 100    # Offset of the point used for phase correction
    head['AcqLength'] = int(FS*Tacq)  # Length of the echo, w/o phase correction data
    AcqLength = int(FS*Tacq)

    head['preData'] = int((Tpe+Tramp+ringDown)*FS + preTrigger) # Length of data before
echo
    head['kspaceLoc'] = int((AcqLength + ((IF/NFreq)*AcqLength))/2) # Echo location in
spectrum
    head['recordLength'] = int((ringDown+Tpe+Tramp+Tacq)*FS +preTrigger)
    return head

def createAttribs(HDFile, **kwargs):
    """
    Creates a set of root directory attributes in an HDF5 file from a dict.
    """

    # If File is a string, make an HDF5 file with that name, else it's a file
    # object, and just use that.
    if isinstance(HDFile, str):
        hf = h5py.File(File, 'w')
    else:
        hf = HDFile

    for key, val in kwargs.items():
        hf.attrs[key] = val

def rawToHDF5(HDFile, File, **kwargs):

    # Convert the kwargs to something more useful
    IF = kwargs['IF']
    FS = kwargs['FS']
    NFreq = kwargs['NFreq']
    Tacq = kwargs['Tacq']
    NPE = kwargs['NPE']
```

```
    NFE = kwargs['NFE']
    preTrigger = kwargs['preTrigger']
    ringDown = kwargs['ringDown']
    Tpe = kwargs['Tpe']
    Tramp = kwargs['Tramp']

    recordLength = kwargs['recordLength']
    channelCount = kwargs['channelCount']
    pCorLength = kwargs['pCorLength']
    pCorOffset = kwargs['pCorOffset']
    AcqLength = kwargs['AcqLength']
    preData = kwargs['preData']
    kspaceLoc = kwargs['kspaceLoc']

    # First we create the HDF file object
    with h5py.File(HDFile, 'w') as hf:
        for c in np.arange(channelCount):
            # We create a group for each channel
            ch = hf.create_group('Channel '+str(c))
            # Data set for the raw echo data
            dset = ch.create_dataset('Echo', (NPE, AcqLength), dtype=np.uint16)
            # Data set for the raw phase correction data
            pcor = ch.create_dataset('pCor', (NPE, pCorLength), dtype=np.uint16)

            # Find our markers and shifts and add them each to a data set
            markers = findFiducialsFile(File)
            shifts = np.zeros((NPE,1), dtype=np.complex)
            ch.create_dataset('markers', data=markers)
            ch.create_dataset('shifts', data=shifts)

            # Open the raw data file and memmory map it
            with open(File, 'r+b') as f:
                file = mmap(f.fileno(), 0)
                # preallocate for kspace
                kspace = np.zeros((NPE,NFE), dtype=np.complex)

                # Go through the markers for each PE line
                for i, m in enumerate(markers):
                    # Pull in a single phase correction line
                    dat = readBlock(file, m+pCorOffset*channelCount,
                                    pCorLength, ChannelCount=channelCount,
                                    Channel=c)
                    # put the data into the hdf
                    pcor[i,:] = dat
                    shifts[i] = computePhaseShift(dat)
                    raw = readBlock(file, m+(8*preData), AcqLength,
                                    ChannelCount=channelCount, Channel=c)
                    dset[i, :] = raw
                    temp = fftshift(fft(fftshift(raw)))
                    kspace[i,:] = temp[kspaceLoc-NFE/2:kspaceLoc+NFE/2]
                    del raw,temp
                    hf.flush()

            kspace = ifftshift(ifft(ifftshift(kspace)))
            kspace = kspace*shifts
            im = fftshift(fft2(fftshift(kspace)))
            ch.create_dataset('kspace', data=kspace)
            ch.create_dataset('image', data=im)

        createAttribs(hf, kwargs)
    return hf

def findFiducialsFile(FileName, MMap=True, Verbose=False, Skip=True):
    """
    Finds the location of fiducials in a data file.

    Searches through a data file and checks each four point block to see if it
```

```
    matches the fiducial pattern. The fiducial pattern is
    (0, 1, 65,535, 65,534). Memory mapped access to the file can be used by
    setting the MMap flag. The function will print found markers if Verbose is
    True. The Skip flag will attempt to guess the position of the next marker,
    speeding up the search for large data sets.

    Parameters
    ----------
    FileName : string
        Full name of the file to be searched.
    MMap : bool, optional
        Enables memory mapped access to the file. May fail with large files on
        32-bit systems.
    Verbose : bool, optional
        Enables printing the found marker and it's location in the file.
    Skip : bool, optional
        Enables fast seeking that will seek to a point in the file that is the
        difference of the last two found markers, less 1000, ahead of the
        current position.

    Returns
    -------
    markers : list of ints
        A list containing the locations immediately after each fiducial marker.
    """
    markers = []
    with open(FileName, 'r+b') as f:
        # If we have the space, use memory mapping
        if MMap:
            file = mmap(f.fileno(), 0)
        else:
            file = f
        # pull the first block to test
        data = file.read(8)

        # select how much it prints output
        if Verbose:
            while data:
                # Decode to four uint16
                block = struct.unpack('<4H', data)
                # Check against the fiducial pattern
                if block == (0, 1, 65535, 65534):
                    # Add it to the list if it matches
                    markers.append(file.tell())
                    print("Found marker " + str(len(markers)) + " at " +
                          str(file.tell()))
                    # Guess where the next marker will be to speed things up
                    if len(markers)>1 and Skip:
                        file.seek(markers[-1] - markers[-2] - 1000, 1)
                # Move to the next block
                data = file.read(8)
        else:
            while data:
                block = struct.unpack('<4H', data)
                if block == (0, 1, 65535, 65534):
                    markers.append(file.tell())
                    if len(markers)>1 and Skip:
                        file.seek(markers[-1] - markers[-2] - 1000, 1)
                data = file.read(8)
    return markers

def readBlock(File, Start, Points, ChannelCount=4, Channel=0):
    """
    Reads a block of data for a single channel.

    Reads a block of data of length Points, begining from position Start, from
    the file object File. Note that File may also be a memory mapped file, but
```

```
    should not be the name of a file. ChannelCount is used to determine what
    subset of data to take, and Channel will select the data corresponding to
    the desired channel. Note that the first channel is defined as '0'

    Parameters
    ----------
    File : File object
        Handle to the file from which to read data.
    Start : Int
        Location from which to start extracting data from the file. This should
        not include an offset associated with the channel number
    Points : Int
        Number of data points (uint16, not bytes) to be read.
    ChannelCount : Int
        Number of channels of data in the file. Should be 1, 2, or 4
    Channel : Int
        Channel for which the data will be read. Should be 0, 1, 2, or 3.

    Returns
    -------
    block : array of uint16
        Array of the data which has been read in.
    """
    File.seek(Start)
    # Multiply by 2 because each point is 2 bytes, and ChannelCount because
    # the desired channel is sectioned out later
    raw = File.read(Points * 2 * ChannelCount)
    # convert to uint16's
    block = struct.unpack('<'+str(int(len(raw)/2))+'H', raw)
    # Only return data for the relevant channel
    return block[Channel::ChannelCount]

def computePhaseShift(Data, Carrier=20e6, FS=250e6, Width=200):
    """
    Uses the supplied data to compute a phase correction factor.

    The Data supplied is Fourier transformed, and the carrier frequency found
    in the spectrum based on the supplied Carrier and FS (sampling frequency).
    THe length of the data used to find the phase shift is set by Width. This
    data is sectioned out of the spectrum, converted to time domain, then the
    center point is divided by the absolute value of itself. This is the
    returned value. The correction is applied by  directly multiplying it with
    the kspace data it corresponds to.

    Parameters
    ----------
    Data : 1d array
        The data that will be used to find the phase shift for a single channel
    Carrier : float
        Frequency that the data is at. Must have the same units as FS
    FS : float
        Frequency that the data was sampled at. Must have the same units as
        Carrier
    Width : int
        The number of points to be used in computing the correction factor. It
        must be an even value.
    Returns
    -------
    Shift : complex
        The returned value is a complex number of unit magnitude. It should be
        multiplied by the complex, baseband, kspace data in order to implement
        the phase correction.
    """
    center = (len(Data) + ((Carrier/(FS/2))*len(Data)))/2

    # FT the phase correction data, take a number of points equal to width
    # around the carrier frequency, then IFT that back into the time domain.
```

```
    spect = ifftshift(ifft(ifftshift(Data)))
    spect = spect[center-(Width/2):center+(Width/2)]
    td = fftshift(fft(fftshift(spect)))
    # Compute the phase correction constant from the center point. The reshape
    # lets us just multiply this by the k-space data later.
    return td[round(Width/2)]/np.abs(td[round(Width/2)])

@profile
def doit():
    File = 'test9.dat'  # File to be processed
    IF = 20e6           # Frequency of the sampled data
    FS = 250e6          # Frequency of the sampling clock
    NFreq = FS/2        # Nyquist frequency of the receiver
    Acq = 0.00512    # Acquisition time in seconds
    NP = 256          # Number of phase encode steps
    NF = 256          # Number of frequency encode steps
    Pretrigger = 100 # Number of pretrigger samples
    RingDown = 0.001 # Delay for phase correction data in seconds
    tpe = 0.003      # Length of phase encode blip in seconds
    tramp = 0.0005  # Length of gradient ramp in seconds

    pCorLength = 100000 # Number of points used for phase correction
    pCorOffset = 100    # Offset of the point used for phase correction
    AcqLength = int(FS*Acq)  # Length of the echo, w/o phase correction data
    preData = int((tpe+tramp+RingDown)*FS + Pretrigger) # Length of data before echo
    kspaceLoc = int((AcqLength + ((IF/NFreq)*AcqLength))/2) # Echo location in spectrum

    markers = findFiducialsFile(File)
    shifts = np.zeros((NP,1), dtype=np.complex)

    with open(File, 'r+b') as f:
        file = mmap(f.fileno(), 0)
        kspace = np.zeros((256,256), dtype=np.complex)

        for i, m in enumerate(markers):
            dat = readBlock(file, m+800, 100000, ChannelCount=4, Channel=1)
            shifts[i] = computePhaseShift(dat)
            raw = readBlock(file, m+(8*preData), AcqLength, ChannelCount=4, Channel=1)
            temp = fftshift(fft(fftshift(raw)))
            kspace[i,:] = temp[kspaceLoc-NF/2:kspaceLoc+NF/2]
            del raw,temp

    kspace = ifftshift(ifft(ifftshift(kspace)))
    kspace = kspace*shifts
    im = fftshift(fft2(fftshift(kspace)))
    plt.imshow(np.abs(im))
    plt.show()

#*****************************************************************************
# Begin the processing code here
#*****************************************************************************
if __name__ == "__main__":
    doit()
```