AN 8 BIT, 100MS/s PIPELINE ADC WITH PARTIAL POSITIVE FEEDBACK

AMPLIFIER FOR COGNITIVE RADIO APPLICATIONS

A Thesis

by

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ABSTRACT

This thesis focuses on designing a low power Pipeline Analog to Digital Converter (ADC) for use in a Cognitive radio network. The Pipeline ADC architecture is one of the most suitable ADC architectures for applications requiring moderate to high operating speeds and resolution while consuming low power. The designed ADC introduces a Partial Positive Feedback amplifier which yields high gain with minimal power consumption without a need for a common mode feedback. A multiplexer–based Multiplying Digital to Analog Converter (MDAC) is also introduced. The multiplexer–based MDAC mitigates the capacitor mismatch effect encountered in the conventional MDAC. Clocked bootstrapped switches are designed to maintain constant on-resistance desired in switches.

With a power supply of 2.4V, the Pipeline ADC consumed a total power of 8.2mW and achieved a Signal-to-Noise-and-Distortion Ratio (SNDR) of 48.08 dB which corresponds to an Effective Number of Bits (ENOB) of 7.69 bits at the Nyquist frequency. A Differential Non-Linearity error (DNL) of less than ± 1 LSB ensuring that all codes corresponding to an 8 bit ADC are available. The Partial Positive Feedback amplifier used achieved an open loop gain of 51 dB while consuming 1.8mA of current. The designed Pipeline ADC achieved a Figure of Merit (FoM) of 0.38 pJ/conversion step.

ACKNOWLEDGEMENTS

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1   INTRODUCTION

The recent increase in the number of wireless communication devices, as well as the fixed allocation of communication channels to licensed users has led to over-crowdedness and inefficient utilization of the Radio Frequency (RF) spectrum. There is the need for a dynamic approach of spectrum allocation to ensure a more efficient utilization of the RF spectrum. The concept of cognitive radio has been proposed as an approach for efficient spectrum utilization.

A cognitive radio network refers to a communication system equipped with the capability to sense the RF spectrum, identify vacant communication channels and dynamically adjust its operating parameters to transmit within the available channel without affecting the Quality of Service (QoS) of the licensed user. Its main objective is to improve spectrum-usage efficiency [1]. In the operation of any cognitive radio network, the sensed spectrum needs to be digitized by an Analog to Digital Converter (ADC) before subsequent processing can take place.

An ADC refers to a system that converts an analog signal into a digital signal. ADC architectures, notably the Flash ADC, Successive Approximation Register (SAR) ADC and the Pipeline ADC have evolved over the years, each offering one advantage over the other. High speed of operation while resolving a high number of bits with little power consumption are the desirable features in any ADC.

The Pipeline ADC architecture is suitable for applications requiring medium-high resolutions while operating at sampling rates in the order of MS/s [2]. For higher resolution, the Pipeline architecture requires a significantly reduced number of comparators making it even more attractive than the Flash, despite the ability of the Flash to operate at higher speed. The SAR ADC has the capability of operating at similar resolutions to the Pipeline architecture but limited to medium speed applications.

Due to the continuous nature of the Cognitive radio network, reducing the power consumption of the ADC is very important to ensure that the Cognitive radio network can operate with as minimal power consumption as possible. The pipeline architecture offers the best trade-off between high operating speed, resolution and power consumption [3].

In this thesis, various types of ADCs are reviewed along with the advantages and disadvantages of each. An in-depth review of the Pipeline ADC is presented highlighting techniques that have been used in previous designs. The designed Pipeline ADC with a proposed Partial Positive Feedback Amplifier which consumes very little power while achieving high gain is presented.

1.1 Thesis Organization

This thesis is organized into six chapters: Chapter one introduces the problem. In Chapter two, the Successive Approximation Register (SAR) ADC and the Flash ADC architectures are reviewed. The factors limiting the achievable ADC resolution are highlighted. The chapter also outlines the most popular figure of merit by which ADCs are compared. Chapter three gives an in-depth analysis of the Pipeline ADC, outlining all the design requirements of the major building blocks. In Chapter four, power consumption of the Pipeline ADC and techniques to reduce it are reviewed. Chapter five presents the designed 8 bits 100MS/s Pipeline ADC, describing all building blocks and innovations. The simulation results of the designed converter is presented in this chapter. The thesis is concluded in Chapter 6 with a summary of the major techniques used and results obtained.

2 OVERVIEW

In this chapter, the SAR and Flash ADCs are reviewed and the limiting factors to the achievable ADC resolution is outlined. The most popular figure of merit by which ADCs are compared is also presented.

2.1 ADC Architectures

The main factors that affect the choice of a particular architecture are power consumption, resolution and speed of operation. Ideally, a low power consumption while resolving more bits at a high sampling rate is desired. Unfortunately, there are tradeoffs between each of these and hence several architectures have over the years evolved to achieve the optimal performance.

The ADC architectures focused on in this section are the Successive Approximation Register (SAR) and the Flash ADC. The advantages and disadvantages of each is reviewed. A table of comparison summarizing the tradeoffs between the various ADC architectures is shown in Table 2.1.

Table 2.1 Comparison of ADC Topologies

Architecture	Speed	Power	Resolution
Flash	High	High	Low
SAR	Low-Medium	Low	Medium-High
Pipeline	Medium-High	Medium	Medium-High

2.1.1 *Flash ADC*

The Flash ADC architecture is shown in Figure 2.1. It deploys the use of fixed reference voltages, usually generated by a resistive ladder to digitize an analog input signal by comparing it with each of the fixed references. The number of references generated is dependent on the resolution of the ADC according to the relation $2^N - 1$; where N is the resolution of the Flash ADC. For example, a 10 bit Flash ADC would require $2^{10} - 1 = 1023$ reference values. Each reference value corresponds to one unique comparator. Therefore, for a 10 bit resolution, the Flash ADC would require 1023 comparators. Each comparator is biased to compare the input voltage to a unique reference voltage [4]. The decision taken by all comparators is collectively known as a Thermometer code. A Digital Encoder is subsequently needed to convert the Thermometer code to the N-bit binary code which is to be read out.
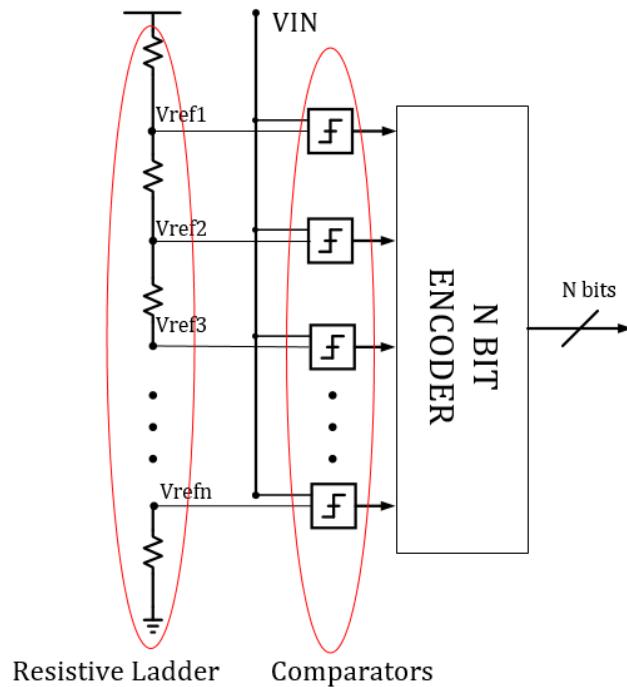
Figure 2.1: Flash ADC architecture

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As the number of references increases, the resolution increases and subsequently the accuracy of conversion increases. However, the comparator count and hence power consumption of the Flash ADC increases exponentially with resolution. This constraint puts a limitation on the maximum number of bits practically realizable with the Flash ADC. As previously stated, to resolve 10 bits a Flash ADC would require 1023 comparators. This would consume an excessive amount of power and makes the Flash topology unsuitable for high resolutions.

A major advantage of the Flash topology lies in its speed. The Flash ADC is a very attractive choice for analog to digital conversion in high speed applications like radar detection, wide band radio receivers and optical communication links [5]. The latency of the Flash architecture is limited to one clock cycle (i.e., the *n*-bit binary code is available exactly one clock cycle after sampling the input), making it the fastest ADC available.

2.1.2   *Successive Approximation Register (SAR) Architecture*

The block diagram of the SAR ADC is shown in Figure 2.2. It consists of a Sample and Hold (S/H), a single comparator, an *N* bit Digital to Analog Converter (DAC), an *N* bit register and a digital control logic. In its operation, the analog input voltage is first sampled by a Sample and Hold circuit operating at the Nyquist rate. The digital control logic determines the value of each bit based on the output of the comparator. It initially sets the most significant bit (*MSB*) to '1' and all other bits to '0'. This digital word is applied to the DAC, which generates an analog signal which is at the mid-point of the full scale input voltage (*Vfull-scale/2).* If the sampled input voltage happens to be greater than *Vfull-scale/2*, the *MSB* of the *N*-bit register
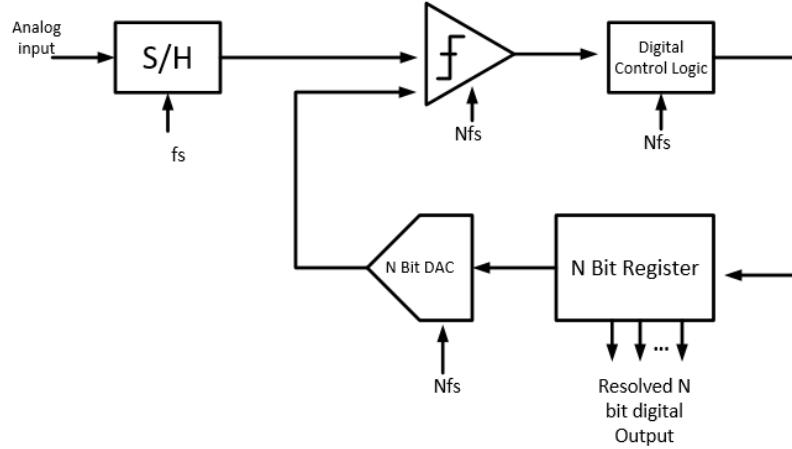
Figure 2.2: Block diagram of the SAR ADC [6]

remains at '1', otherwise it changes to '0'. This is repeated successively until all *N* bits are resolved, each time resetting the current bit to be resolved in the *N*-bit register to '1' and all other bits yet to be resolved to '0'. In all, *N* iterations of the algorithm are performed to resolve all *N* bits. The operation of a 4 bit SAR ADC is shown in Figure 2.3.
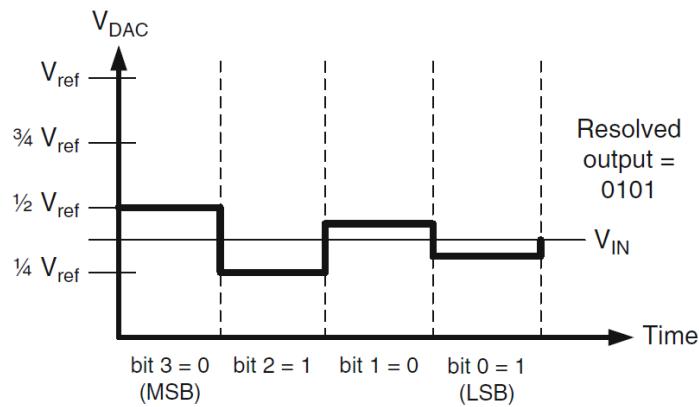
Figure 2.3: Operation of a 4 bit SAR ADC, Reprinted from [2].

The MSB is initially set to 1 and all other bits set to 0. The digital word is applied to the DAC which generates an analog voltage of $0.5V_{ref}$ with which the comparator compares the input voltage. Since the input voltage is less than the initial reference, the output of the comparator is low and the *MSB* is changed to 0 by the digital control logic. This completes the first step in the approximation sequence. The sequence is repeated 4 times till all 4 bits are resolved. The major advantage of the SAR ADC architecture is the reduced number of analog components used, most notably a single comparator regardless of the number of bits to be resolved. As analog components consume the most power, this advantage helps in reducing power consumption, as well as area.

The design of the SAR logic, DAC and comparator however proves to be very challenging. For the ADC to operate effectively at Nyquist sampling rate of *fs*, each of the above mentioned components must operate at *N.fs* ; where *N* is the number of bits and *fs* is the sampling rate [2]. For instance, to operate at a sampling rate of 500MHz with a resolution of 10 bits, each component would be required to operate at 5GHz which proves quite challenging. This limits the realizable speed of the SAR architecture to low-to-medium speed applications. However, it is very suitable for medium to high accuracy applications.

2.2 ADC Resolution Limiting Factor

The Effective Number of Bits (ENOB) achievable by an ADC is limited by the Signal to Noise and Distortion Ratio (SNDR) as shown below;

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad [7] \qquad\qquad (2.1)$$

The Signal to Noise and distortion Ratio is the ratio of the signal power to the summation of the power of all noise sources and total distortion. From (2.1), it is

evident that the effective resolution of the ADC is dependent on the signal amplitude, linearity of the ADC and the total noise. Ideal ENOB is only obtained with zero electronic noise and no distortion which is practically not achievable. Hence to achieve a high ENOB, a highly linear and low noise ADC design is required.
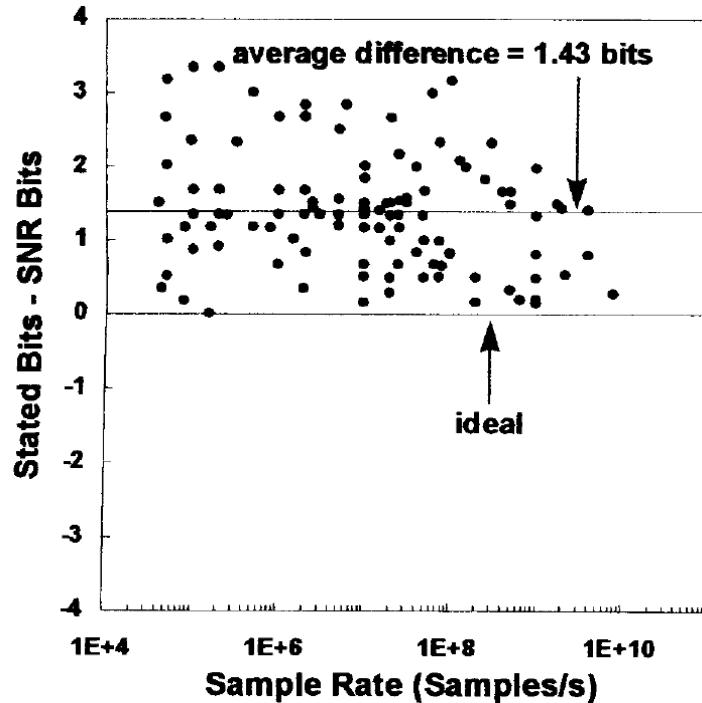
Figure 2.4: Effect of noise and distortion on ENOB, Reprinted from [7]

Figure 2.4 shows the difference between the actual bits designed for and the effective bits obtained due to degradation by noise across a range of frequencies. Ideally, this difference should be zero. This is however practically not possible to attain. An average difference of 1.43 bits is observed across all sampling frequencies.

2.3 Figure of Merit

The Figure of Merit (FoM) provides a basis for comparing the performance of various ADCs. The most popular Figure of Merit by which ADCs are compared is given by;

$$FoMp = \frac{Power}{2^{ENOB}.\ f_s} \quad (\text{pJ/conv. bit}) \ [8] \tag{2.2}$$

To normalize (2.2) with respect to the supply voltage, a new Figure of Merit is given by;

$$iFoM = \frac{Current}{2^{ENOB}.\ f_s} \quad (\text{pA/conv. bit}) \tag{2.3}$$

3 PIPELINE ADC ARCHITECTURE OVERVIEW

The Pipeline ADC architecture is presented in this chapter. The various building blocks are analyzed and the effects of non-idealities on the performance of the ADC is evaluated.

3.1 Pipelined ADC Introduction

Pipeline architectures mainly resolve medium-to-high resolutions (8 – 14 bits) while operating at medium-to-high sampling rates (a few MHz to hundreds of MHz). The generic block diagram of the Pipeline ADC is shown in Figure 3.1. It consists of a number of identical stages, each resolving n number of bits cascaded to resolve a total of N bits. Each stage consists of a sub–ADC (usually a Flash), S/H, DAC, summer and an operational amplifier.
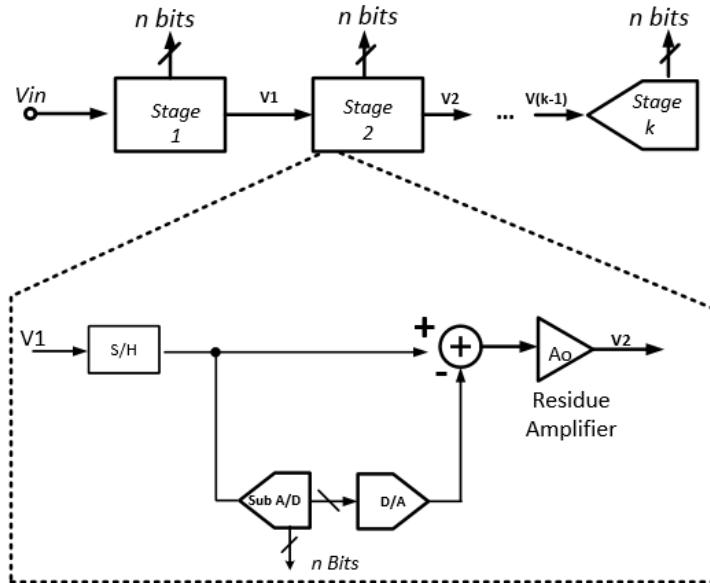
Figure 3.1: Block diagram of a Pipeline ADC

The Sub–ADC resolves *n* bits in each stage as shown in Figure 3.1. The resolved digital bits are converted back into an analog signal and compared with the sampled input signal. The difference, known as the residue, is amplified by the operational amplifier and fed to the next stage. The residue is amplified to full scale in order to maximize the dynamic range of the ADC. The amplification factor is 2^n ; where *n* is the number of bits resolved in a stage. The functions of the S/H, DAC, summer and operational amplifier are all combined in one switched capacitor network known as Multiplying Digital to Analog Converter (MDAC). Due to the reduced number of bits resolved per stage, the comparator count for the Pipeline architecture is significantly reduced as compared to the Flash architecture. For medium to high resolutions (8 – 14 bits), the Pipeline architecture shows considerable power savings over the Flash architecture.

The resolution of the Pipeline ADC is typically comparable to that of the SAR. However, the Pipeline architecture is more favored for higher sampling rates since it does not require components operating *N. fs*, unlike the SAR which requires multiple components operating at *N. fs*. Precision requirements for each of the components decrease along the Pipeline making design of subsequent stages simpler [9]. Latency is however more pronounced in the Pipeline structure than it is in the SAR or Flash architectures. The digital word in the pipelined architecture is obtained after *n* clock-cycles; where *n* is the number of stages, whereas in the Flash, it only takes one clock cycle to obtain the digital data.
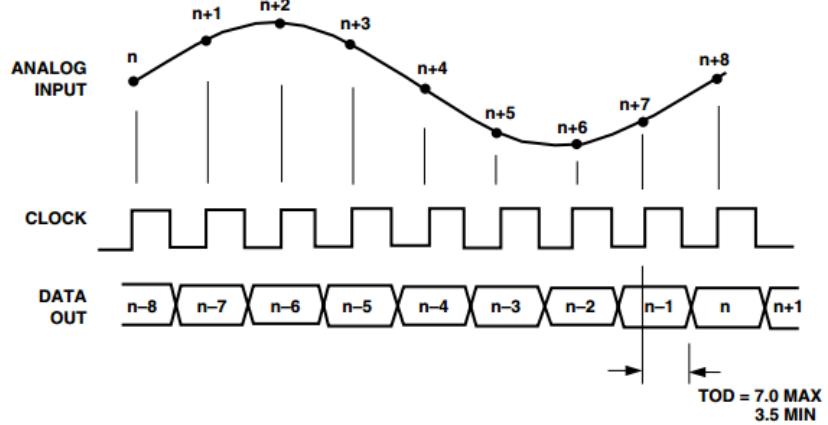
Figure 3.2: 7 clock cycle latency of a Pipelined ADC, Reprinted from [10]

Figure 3.2 shows the timing diagram of a 7 stage Pipeline ADC. The digital word in this Pipeline structure would be obtained after 7 clock cycles as shown.

3.2   Multiplying Digital to Analog Converter (MDAC)

As stated in the previous section, the functions of the S/H, DAC, summer and operational amplifier can be combined into one switched capacitor network known as the MDAC. The MDAC and Sub–ADC make up each Pipeline stage as shown in Figure 3.3.

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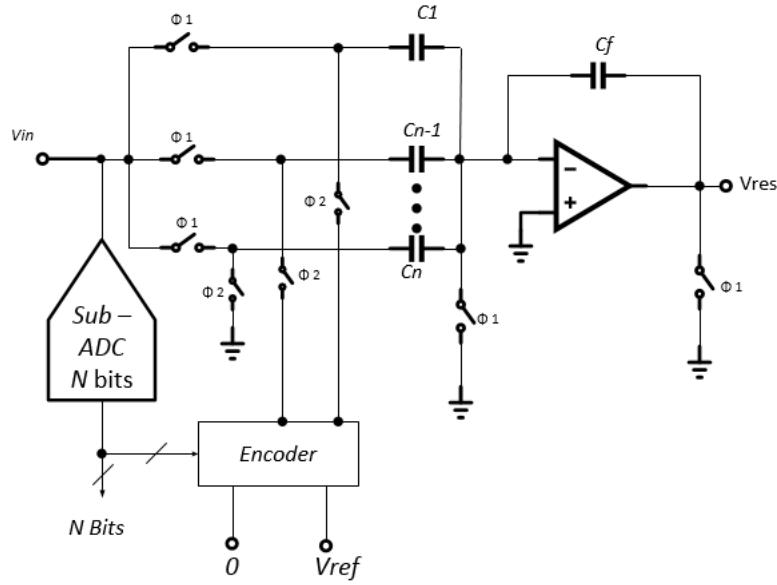
Figure 3.3: Conventional N-Bit MDAC

The operation of the MDAC is as follows: In the first phase (Φ1), the input voltage is sampled onto all sampling capacitors ($C1$-Cn). Bottom plate sampling is done to reduce signal dependent charge injection on sampling capacitors [11] . At the same time, the Sub–ADC would have resolved the n bits for that particular stage. The charge Q_1 accumulated in Φ1 on the sampling capacitors (C_1 to C_n) in Figure 3.3 is given by:

$$Q_1 = \sum_{1}^{2^n} C_i \cdot V_{in} \qquad (3.1)$$

where V_{in} is the input voltage, C_i is the ith sampling capacitor, n is the number of bits. In the second phase (Φ2) the comparator output (thermometer code) is converted into analog voltage (0 or $Vref$) and is subtracted from the initial input voltage sampled on each of the sampling capacitors and the resulting voltage is amplified at the output. The $2^n th$ (Cn) capacitor is however always grounded in the

second phase. The charge Q_2 accumulated in Φ2 on the sampling capacitors (C_1 to C_n) in Figure 3.3 is given by:

$$Q_2 = \sum_1^{2^n - 1} (C_i \, b. V_{full-scale}) + V_{Out} C_f \tag{3.2}$$

where b is the thermometer code, $V_{full-scale}$ is the full-scale input voltage, V_{out} is the residue voltage. Applying the law of conservation of charges, V_{Out} could be expressed as:

$$\frac{\sum_1^{2^n} C_i \, . V_{in}}{C_f} - \frac{\sum_1^{2^n - 1} C_i . b. V_{fullscale}}{C_f} \tag{3.3}$$
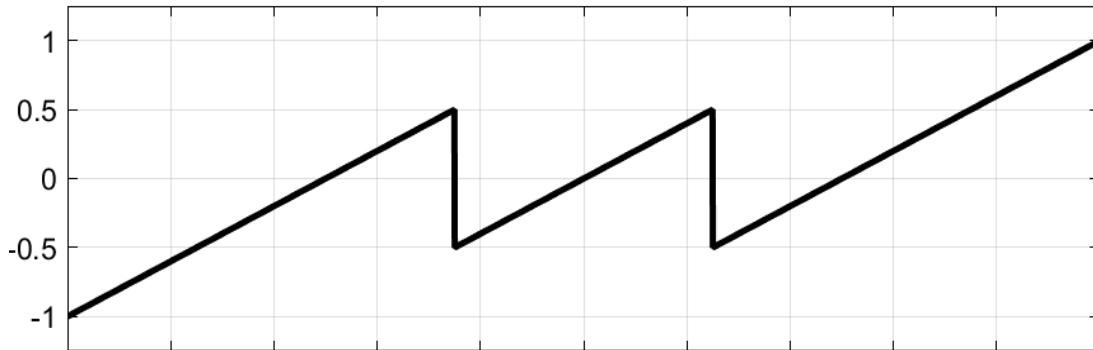
Figure 3.4: Ideal residue curve of a 1.5 bit MDAC with 1V input full scale voltage.

Figure 3.4 shows the ideal residue curve of a 1.5 bit MDAC with an input full-scale voltage of 1V.

3.3 Operational Amplifier (Op-amp) DC Gain Requirement

Equation (3.3) was derived based on the assumption that the operational amplifier used in the MDAC has infinite gain and bandwidth. With finite gain, the equation becomes:

$$V_{out} = \left[\left(\frac{1}{1 + \frac{1}{A\beta}} \right) . \frac{\sum_1^{2^n} C_i}{C_f} \; V_{in} \right] - \left[\frac{\sum_1^{2^n-1} C_i . b . V_{full-scale}}{C_f} \right] \tag{3.4}$$

where A is the open loop gain, β is the feedback factor. The direct transfer function from the input to the output is:

$$V_{out} = \left(\frac{1}{1 + \frac{1}{A\beta}} \right) . \frac{\sum_1^{2^n} C_i}{C_f} \; V_{in} \tag{3.5}$$

A finite gain error of $\frac{1}{A\beta}$ is introduced. This error alters the residue transfer curve from the ideal curve as shown in Figure 3.5 resulting in missing codes in the entire pipeline structure and subsequently leading to harmonic distortion. Consequently, the accuracy and linearity of the Pipeline ADC is limited. To avoid this, the op-amp needs to be designed with a gain high enough to reduce the gain error.
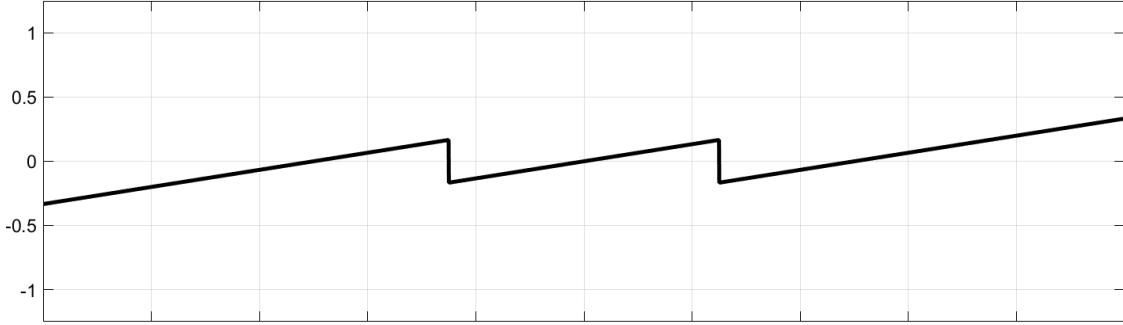
Figure 3.5: Effect of gain error on 1.5 bit residue curve.

To avoid any missing codes, the maximum gain error (Δ_{max}) should be less than the least significant bit (LSB) of the data converter. The maximum gain error occurs when the input voltage is maximum [12] (i.e. $V_{in} = V_{full-scale}$). Hence for Δ_{max}, (3.5) can be re-written as:

$$V_{out} = \left(\frac{1}{1 + \frac{1}{A\beta}}\right) \cdot \frac{\sum_1^{2^n} C_i}{C_f} V_{full-scale} \tag{3.6}$$

The maximum gain error is given by;

$$\Delta_{max} = \frac{V_{full-scale}}{A\beta} \tag{3.7}$$

The LSB of any data converter is given by:

$$LSB = \frac{V_{full-scale}}{2^N} \tag{3.8}$$

Since Δ_{max} should be kept below an LSB of the data converter, the minimum open loop gain (A_{min}) required is given by:

$$A_{min} = \frac{2^N}{\beta} \tag{3.9}$$

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Clearly, a large DC gain is required in the MDAC circuit. As technology scales, achieving large DC gain from op-amps becomes very challenging. Several analog techniques such as gain boosting [13], multi-stage op-amps [14] or longer channel devices have been used to help increase op-amp gain. These techniques however result in either increased power consumption (gain boosting), reduction in speed of the ADC (multi-stage) or a general increase in design complexity.

3.4 Op-amp Gain Bandwidth Product (GBW) Requirement

Equation (3.4) was obtained with the assumption that the only limitation to realizing the ideal transfer function was finite gain of the op-amp. However, the finite gain bandwidth product of the operational amplifier introduces settling errors which affect the transfer curve. So far, we have assumed that the op-amp has infinite bandwidth and hence no settling errors are encountered. Modelling the Op-amp as a first order system, the transfer function close to the unity gain frequency is given by [11]:

$$A(s) = \frac{GBW}{s} \tag{3.10}$$

where $A(s)$ is the open loop is gain and GBW is the unity gain frequency. The closed loop transfer function is given as:

$$H(s) = \frac{A(s)}{1 + \beta A(s)} \tag{3.11}$$

The step response during the second phase of operation, Φ_2 in time domain is:

$$h(t) = \frac{1}{\beta}\left(1 - e^{-\frac{t}{\zeta}}\right) \tag{3.12}$$

where $\zeta = 1/\beta GBW$. The op-amp must settle to $(N - n)$ bits of accuracy within half of the clock period (t = T/2) for proper operation of the circuit. To ensure this, the condition below should be satisfied [12]:

$$e^{-\frac{t}{\zeta}} < \frac{1}{2^{N-n}} \qquad (3.13)$$

From (3.13), we can derive the minimum GBW as:

$$\text{GBW (Hz)} > \frac{2\left(\ln 2^{-(N-n)}\right).f_s}{2\pi\beta} \qquad (3.14)$$

where f_s the sampling frequency, n is the number of bits resolved in the preceding stage(s) and β is the feedback factor.

3.5   Operational Amplifier Topologies

From the previous section, it is evident that the gain and bandwidth of the operational amplifier are very important in ensuring good performance of the ADC. Several ADC architectures with the capability of yielding high gain and bandwidth with minimal amount of power have been used in various designs of Pipeline ADCs. Table 3.1 shows a comparison of the performance of some operational amplifiers.

Table 3.1: Comparison of Op-amp topologies

Architecture	Gain	Gain Bandwidth Product	Power	Output Swing
Single Stage	Low	High	Low	High
Telescopic Cascode	High	High	Medium	Low
Folded Cascode	High	High	Medium	Low
Two Stage	High	Low	Medium	Low

3.6 Thermal Noise Requirement

As seen from the residue equation, the transfer function of the MDAC circuit is dependent on capacitor ratio. The question however is how to determine the minimum value of the sampling capacitor? Op-amp gain bandwidth product and thermal noise set the maximum and minimum limitations on the capacitor size. The sampling capacitor should be small enough to be driven by the Op-amp without burning excessive amount of power. The minimum size is however determined by the sampling thermal noise.

Ideally all capacitors are known to be noiseless elements. However, due to noisy components such as resistors and op-amps, capacitors end up absorbing some noise produced by these elements. Consider the RC model shown in Figure 3.6 [15], where the thermal noise contribution (V_N^2) can be expressed as:

$$V_N^2 = \int_0^\infty [V_{N1}^2(f) + V_{N2}^2(f)] \cdot |H_1(f)|^2 \, df \tag{3.15}$$

$$= \int_0^\infty [4KTR_1 + 4KTR_2] \cdot |\frac{1}{1 + j2\pi f.(R_1 + R_2)C_1}|^2 df$$

Simplifying (3.15), noise can be expressed as:

$$V_N^2 = \frac{KT}{C_1} \tag{3.16}$$

where K is the Boltzmann constant, T is the absolute temperature.
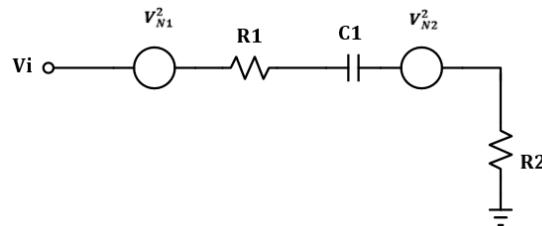
Figure 3.6: RC model with noise sources

From (3.16), it is evident that increasing the capacitor size reduces the thermal noise power. Thus capacitor size introduces a power – accuracy trade-off. The larger the capacitor size, the more power consumed by the op-amp whereas smaller capacitor sizes produce higher thermal noise resulting in reduced accuracy. Thermal noise power should be kept below the quantization noise floor. Quantization noise is given by:

$$Quantization\ noise = \frac{\Delta^2}{12}$$

(3.17)

where Δ is the LSB. To keep the thermal noise contribution below the quantization noise floor, the condition below should be satisfied;

$$C_1 > \frac{12\ KT}{V_{FS}^2} \cdot 2^{2N}$$

(3.18)

where C_1 represents the sampling capacitance.

3.7 Capacitor Mismatch

Recalling the transfer function of the residue from (3.3):

$$V_{Out} = \frac{\sum_1^{2^n} C_i \cdot V_{in}}{C_f} - \frac{\sum_1^{2^n - 1} C_i \cdot b \cdot V_{fullscale}}{C_f}$$

(3.19)

It can be observed that the transfer function is dependent on matching between each of the sampling capacitors, C_i, as well as feedback capacitor, C_f. Mismatches among sampling capacitors or between sampling capacitors and feedback capacitor will cause distortion in the generated residue curve as shown in Figure 3.7, which would result in harmonic distortion.
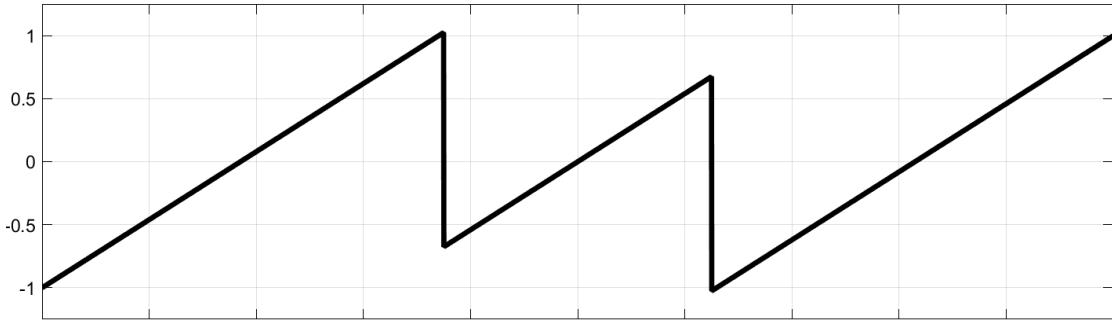
Figure 3.7: Effect of capacitor mismatch on the residue curve of the 1.5 bit MDAC

The relative mismatch between two capacitors varies inversely as the square root of the area of the capacitor as shown below [2]:

$$\text{Capacitor mismatch} \propto \frac{1}{\sqrt{\text{capacitor area}}} \qquad (3.20)$$

In addition to reducing the thermal noise power, large capacitor sizes help reduce capacitor mismatch which results in less harmonic distortion, hence improving linearity. This however comes at the expense of increased capacitor area and more current to drive the capacitor. Improved capacitor matching in layout can be achieved with certain good layout techniques like common centroid approach and use of dummy capacitors [16]. Digital calibration techniques to compensate for capacitor mismatches are also being actively researched into.

3.8 Sub–ADC Design

As previously stated, each stage of the Pipeline architecture consists of a Sub–ADC which is implemented using the Flash architecture. To reduce the complexity of each Sub–ADC, the number of bits resolved per stage by the Sub-ADC is minimized. The main components of the Sub-ADC are the comparator, binary encoder and a resistive ladder.

A comparator basically generates a low or high logic output depending on the comparison between an analog input voltage and a reference voltage. In an ideal comparator with infinite gain, the comparator produces a high logic output for inputs greater than the reference voltage and a low logic output when the input is lower than the reference voltage [17] [18]. Low comparator offsets with low power consumption while resolving bits in the shortest possible time is desired. In [19], different comparator topologies used in Pipeline ADCs are analyzed.

The binary encoder is needed to convert the comparator outputs (thermometer code) to binary code so that the designed bits can be read out. The resistive ladder generates the reference voltages required for comparison. The choice of resistance values is particularly important. Large resistor values result in reduced power consumed by the resistor ladder at the expense of increased kickback noise, which disturbs the reference voltages. Reducing the resistor values would result in increased power consumption but less disturbance to the reference voltages.

3.9 Frontend Sample and Hold

Analog input during the sampling phase is usually sampled by both the MDAC and the Sub-ADC. Due to mismatch in the signal path between the input voltage and each of the two circuits (i.e. The MDAC and the Sub-ADC), there is a sampling mismatch in the voltage sampled by both circuits. Consider Figure 3.8: Different instantaneous voltages sampled by Sub-ADC and *MDAC*. The MDAC samples the voltage *V2 (t)* while the comparator makes a decision with *V1 (t)* as the input voltage. This introduces a voltage error (*Ve*), known as aperture error which is given by:

$$V_e = 2\pi f_{in} V_{ref} (\Delta t) \tag{3.21}$$

where f_{in} represents the signal frequency, Δt is the timing mismatch, V_{ref} is the peak value of the sinusoidal input voltage.
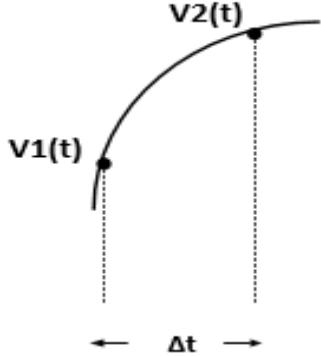
Figure 3.8: Different instantaneous voltages sampled by Sub-ADC and MDAC

The MDAC and Sub–ADC circuits sample very different voltages at very high input frequencies yielding high aperture errors. To eliminate this error, a front-end sample and hold amplifier is placed at the input of the first stage. This discretizes the input signal at the first stage, making it independent of frequency, which allows the MDAC and Sub–ADC sample the same input voltage.

The sample and hold amplifier consumes a large amount of power and area. It also introduces additional noise and distortion in the ADC making it undesirable in most applications. A number of sample and hold-less ADC techniques have been developed to eliminate the need for the front-end sample and hold. A time constant matching technique is used in [20] to eliminate the voltage error resulting from sampling mismatch thereby eliminating the need for a sample and hold. This is discussed in detail in the next chapter.

4 PIPELINE POWER EFFICIENCY

This chapter outlines the major factors that contribute to power consumption in general switched capacitor networks and in the Pipeline ADC architecture. Various power conservation techniques are reviewed outlining their effects on the ADC design.

4.1 Power Consumption in Switched Capacitor Networks

Power consumption in switched capacitor networks can be derived as:

$$P \propto KT \cdot DR \cdot \left(\frac{V_{gs} - V_{th}}{V_{DD}}\right) \cdot f_s \tag{4.1}$$

where P is the power, K is the Boltzmann constant, T is the absolute temperature, f_s is the sampling rate, $V_{gs} - V_{th}$ is the overdrive voltage of the input transistors of the amplifier and V_{DD} is the supply voltage [21]. From (4.1), the power consumption in switched capacitor networks can be said to be directly dependent on the sampling rate and thermal energy, and inversely dependent on the supply voltage. As indicated in (3.14), the gain bandwidth product of the amplifier increases as the sampling frequency increases. The gain bandwidth product (GBW) of the amplifier can be approximated as:

$$GBW = \frac{g_m}{C_L} \tag{4.2}$$

where g_m is the transconductance of the input transistors of the amplifier and C_L is the load capacitance. For higher gain bandwidth product, the transconductance of the input transistors of the amplifier would have to be increased. An increase in the

transconductance (gm) would require increasing the over-drive voltage of the input transistors of the amplifier as shown below:

$$gm = \mu_{p,n} C_{ox} \left(\frac{W}{L}\right)(V_{gs} - V_{th}) \tag{4.3}$$

where $\mu_{p,n}$ is the mobility of the nmos or pmos input transistors, C_{ox} is the capacitance of the oxide, $\frac{W}{L}$ is the dimensions of the input transistors, $V_{gs} - V_{th}$ is the overdrive voltage.

4.2 Power Consumption in Pipeline ADC

As explained in the previous section, the power consumption in general switched capacitor networks is highly dependent on the sampling rate. In the Pipeline ADC however, the power consumption is not only constrained by sampling frequency. The number of bits resolved per stage and thermal noise place major limitations on the power consumption of a Pipeline ADC.

Choice of the per-stage resolution directly impacts the power consumption. Consider an 8 bit Pipeline ADC resolving 2 bits per stage. (i.e. 2-2-2-2). Each sub-ADC in each stage would be composed of 3 comparators, amounting to 12 comparators in all along with 3 amplifiers. Comparing such an ADC to another 8 bit Pipeline resolving 4 bits per stage; this structure yields 15 comparators per stage amounting to a total of 30 comparators along with an operational amplifier. Clearly, resolving 2 bits per stage proves more power efficient than resolving 4 bits per stage. It should however be noted that a 2 bit per stage resolution has more latency and would suffer more from the effects of op-amp non-idealities than a 4 bits resolved per stage. Hence, power consumption is not the sole consideration but a key one in the choice of number of resolutions per stage.

As previously discussed, the sampling process introduces thermal noise given by $\frac{KT}{C}$ which affects accuracy in the Pipeline structure and should be ideally kept below the quantization noise floor. To minimize the thermal noise power, the sampling capacitor size should be increased. Increasing the sampling size would however require more current to drive the capacitor, increasing the overall power consumed.

Finally, the presence of a front-end sample and hold amplifier considerably increases the power consumption. The sample and hold amplifier is known to be one of the most power hungry component of the Pipeline ADC. This is due to the usually large bandwidth required by the sample and hold network (typically multiples of the input frequency).

4.3   Power Reduction Techniques

Operating Pipeline ADCs at high sampling rates while resolving a high number of bits is desirable. However, a number of techniques to help reduce the power consumption have to be incorporated in the Pipeline structure to make its operation more efficient. The general Pipeline power reduction techniques in the literature have been reviewed.

4.3.1   *Sample and Hold-less Approach*

The sample and hold amplifier is a major power consuming component in the Pipeline structure. It is not a required component but plays a role in ensuring that both the sub-ADC and MDAC sampling network sample the same input voltage especially at high frequencies of input voltage. The use of the sample and hold amplifier can be eliminated if the signal path to the input of both the MDAC network and the sub-ADC network is matched such that there is no timing mismatch between

the two circuits. To achieve this, the R-C time constants in both paths should be perfectly matched. [20] achieves this by using the same input sampling switch for both the MDAC and the sub-ADC network as shown in Figure 4.1. To reduce the timing mismatch and hence aperture error, the following condition should be satisfied:

$$\frac{2C_1 + C_{p1}}{2C_2 + C_{p2}} = \frac{\frac{1}{gm}}{R_2} \tag{4.4}$$

where C_{p1} and C_{p2} are the parasitic capacitances at the nodes N1 and N2, R_2 is the resistance of the switch S2 and gm is the transconductance of the comparator's pre-amplifier in Figure 4.1.
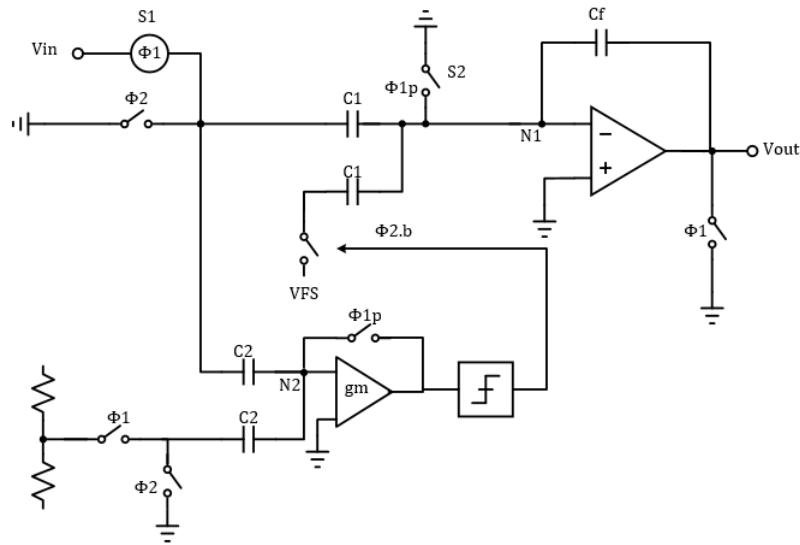
Figure 4.1: Same input sampling switch for time constant matching[20]

By meeting the condition in (4.4), the aperture error introduced as a result of the absence of a front end sample and hold amplifier can be reduced to less than an LSB of the full scale voltage. Perfect matching of these parameters is difficult, however,

due to transistor second order effects such as channel length modulation. This approach is also not the most power efficient solution. It uses a separate set of capacitors in Φ2 for MDAC sampling of the full scale voltage, which reduces the feedback factor. A reduced feedback factor would require an increase in GBW to maintain the same conversion speed as shown below;

$$GBW \; = \; \frac{1}{\beta.\zeta}$$

(4.5)

where ζ is the time constant and β is the feedback factor. Also, due to the comparators and MDAC network sharing the same sampling switch, there is kickback noise coupled from the latches to the MDAC network (from node N2 to node N1 in Figure 4.1). To reduce the effect of kickback noise, a pre-amplifier is used to scale the noise generated by the square of the gain of the pre-amplifier. However, the use of the pre-amplifier results in extra power consumption.

To make this approach more power efficient, [21] uses the same sampling capacitor in the MDAC structure to sample both input voltage and the full scale voltage, while using separate input sampling switches for the sub-ADC and the MDAC network as shown in Figure 4.2.
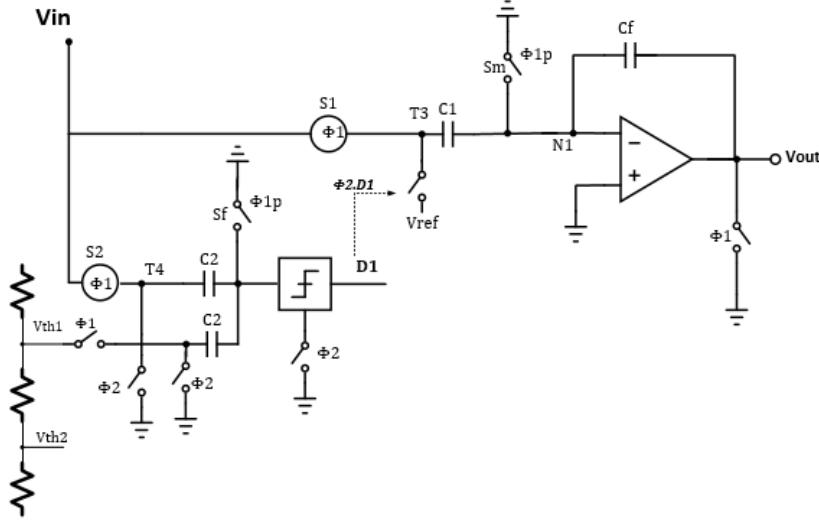
Figure 4.2: Separate input sampling switches for time constant matching[21]

For matching, the following conditions need to be satisfied:

$$\frac{C_1 + C_{p1}}{2C_2 + C_{p2}} = \frac{R_{sf}}{R_{sm}} \tag{4.6}$$

$$\frac{C_1 + C_{p3}}{C_2 + C_{p4}} = \frac{R_{s2}}{R_{s1}} \tag{4.7}$$

where R_{s1} and R_{s2} are the on-resistance of the input sampling switches (S1 and S2), R_{sf} and R_{sm} are the on-resistances of the switches Sf and Sm, C_{p3} and C_{p4} are the parasitic capacitances at the nodes T3 and T4 as shown in Figure 4.2. With this approach, the matching requirements become even more stringent as two nodes in the signal path needs to be matched as opposed to just one node in [20].This is however a more power efficient approach. Since the same capacitor is used in the MDAC network for sampling both the input voltage (in $\Phi1$) and the full scale voltage (in $\Phi2$), the feedback factor is not altered. There is also no problem of kickback noise

from the latch to the MDAC since different input sampling switches are used hence no pre-amplifier is required which saves extra power.

4.3.2   *Stage Scaling and Optimized Stage Resolution*

Traditionally, all stages of the Pipeline ADC are made to be identical (same capacitors and Op-amps). This is however not an ideal solution for power conservation. Consider the pipeline structure in Figure 4.3 which resolves 1 bit per stage with each stage being exactly identical.
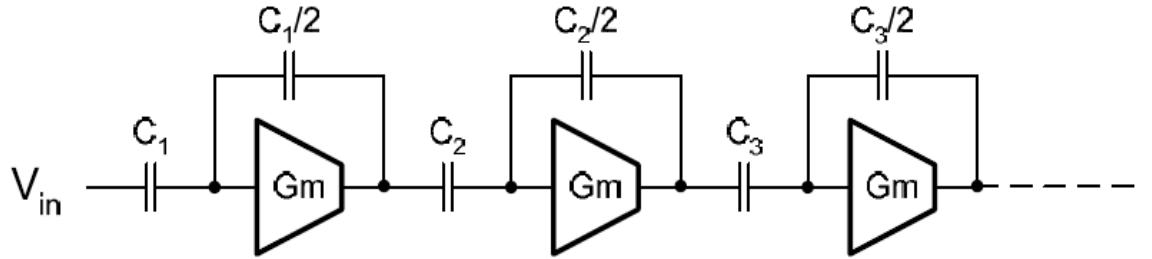
Figure 4.3: Pipeline structure resolving 1 bit per stage, Reprinted from [22]

Given that $C_1 = C_2 = C_3$; the total input referred noise power is given as:

$$N_{total} = KT \left[\frac{1}{C_1} + \frac{1}{4C_1} + \frac{1}{16C_1} + \cdots \right] \tag{4.8}$$

From (4.8), the noise contribution from subsequent stages in the Pipeline queue becomes insignificant. Even though this approach reduces the total noise power, it is very power consuming. Since all capacitors are of the same size, all op-amps will require the same transconductance to supply sufficient current to drive the capacitors. However, if capacitors are scaled from one stage to another by the stage gain of the preceding stage (i.e. $C_1 = 4C_2 = 16C_3$, for a stage gain of 2), the total input referred noise current becomes:

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$$N_{total} = KT \left[\frac{1}{C_1} + \frac{1}{C_1} + \frac{1}{C_1} + \cdots \right] \qquad (4.9)$$

From (4.9), every stage contributes the same amount of noise. Hence, the total noise contribution is increased as compared to using identical capacitor sizes. However, the current required to drive capacitors of subsequent stages in the queue reduces by a factor of the gain of the preceding stage. This reduces the transconductance of the op-amps of these stages and consequently reduces the overall power consumption.

In addition to stage scaling, good choice of the per-stage resolution also helps to reduce power consumption. [23] resolves 2.5 bits per stage for the first 4 stages and 2 bits in the last stage of a 12 bit pipeline ADC. With this choice of resolution per stage, the number of stages and hence amplifiers used in the pipeline structure is reduced. As the operational amplifier is the major power consuming component of the pipeline architecture, reduction in amplifier count greatly reduces the power consumption.

4.3.3   *Open Loop Amplifier Approach*

Closed loop operation has conventionally been used in Pipeline ADCs. The closed loop approach has the advantage of providing a precise gain tolerant temperature and process variation. Consider the closed loop amplifier circuit shown in Figure 4.4, the gain is given by:

$$A_{CL} = \frac{C_s}{C_f} \left(\frac{1}{1 + A\beta} \right) \qquad (4.10)$$

where A_{CL} is the closed loop gain, β is the feedback factor and A is the open loop gain.
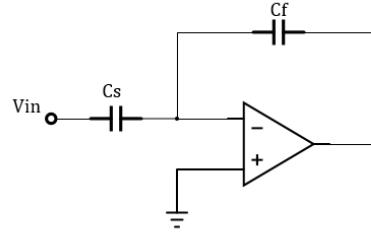
Figure 4.4: Closed loop amplifier

With a large open loop gain, the gain is entirely dependent on the capacitor ratio $\frac{C_S}{C_f}$ which ensures high precision. A large amount of power is consequently required to provide the desired loop gain for successful closed loop operation. To avoid the excessive power required in the closed loop approach, [24] uses an operational amplifier in open loop instead of the conventional closed loop structure in the first stage of a 12 bit Pipeline ADC.
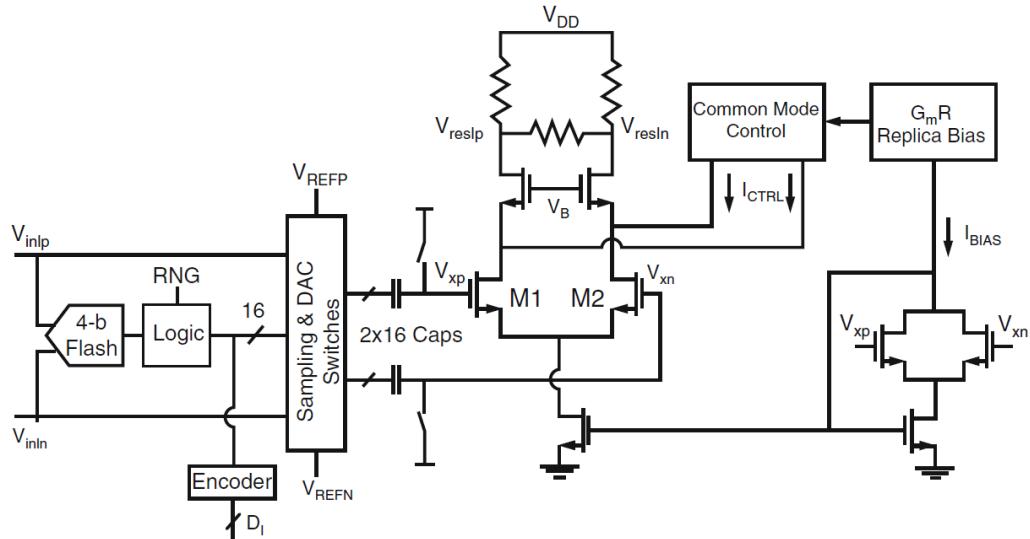
Figure 4.5: 4-bit MDAC using an amplifier in open loop, Reprinted from [24]

The open loop amplifier was designed to achieve a desired gain of 8, given by $g_{m1}R_O$; where g_{m1} denotes the transconductance of the input transistors and R_O is the output impedance of the amplifier. Power savings of about 60% was realized with this approach as opposed to the closed loop approach [24].

A major disadvantage of this approach is that the gain is set by the transconductance, gm, and the output impedance of the amplifier all of which are process dependent. As a result, the gain is susceptible to process and temperature variations and precision cannot be attained. The open loop approach also introduces more harmonic distortion than the closed loop approach. The total harmonic distortion for any system is as shown below:

$$THD = \sqrt{HD_2^2 + HD_3^2 + HD_4^2 + \cdots} \tag{4.11}$$

where HD_2 , HD_3 , HD_4 are the second, third and fourth order distortion components. With feedback, each of the distortion components is scaled down by the square of the loop gain as shown below:

$$THD = \sqrt{\frac{HD_2^2}{(1+AB)^2} + \frac{HD_3^2}{(1+AB)^2} + \frac{HD_4^2}{(1+AB)^2} + \cdots} \tag{4.12}$$

In [24], some calibration techniques are used to correct for the nonlinearity introduced due to the amplifier operating in open loop.

4.3.4   *Capacitive Charge Pump Based MDAC*

In [2], a capacitive charge pump technique is used to obtain a gain of 2 for a 1.5-bit pipeline stage instead of using an op-amp in feedback to obtain the same gain. Capacitive charge pumps basically operate as a switched capacitor network in two phases. They attain voltage gain by sampling an input voltage on multiple capacitors in one phase and subsequently connecting all the capacitors in series in the next

phase to generate a voltage which is the sum of the voltages initially sampled on each capacitor. Figure 4.6 shows the implementation of the capacitive charge pump idea to obtain a pipelined stage gain of 2 for the 1.5-bit MDAC in [2].
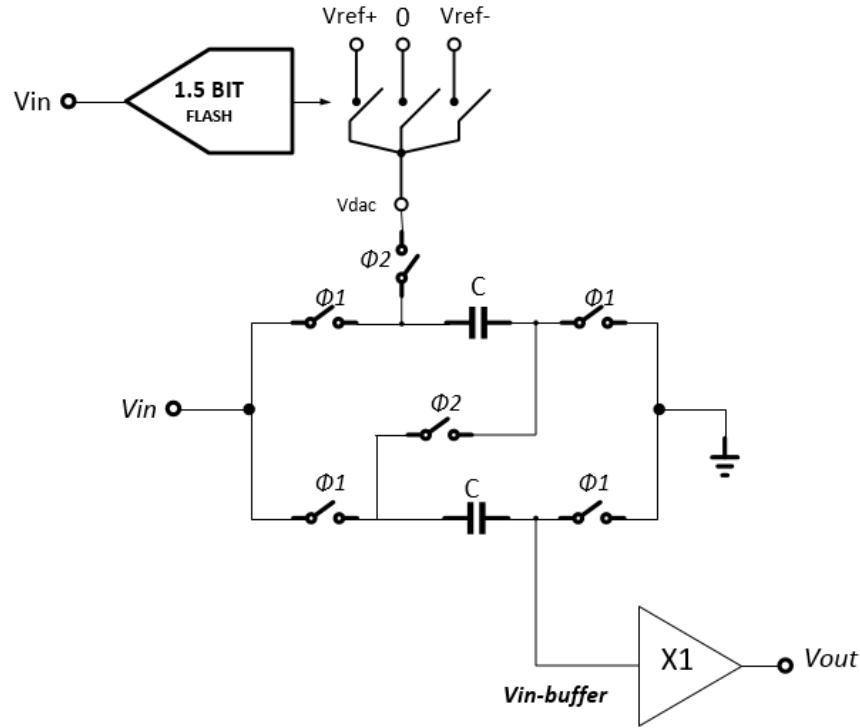
Figure 4.6: Capacitive Charge Pump based MDAC [2]

In the first phase ($\Phi1$) the input voltage (V_{in}) is sampled onto the capacitors. The charge held across the capacitors is given by:

$$Q_1 = 2(V_{in})C \tag{4.13}$$

In phase two ($\Phi2$) an analog voltage (V_{dac}) is subtracted from the initial input voltage sampled on the capacitors in the first phase. The charge held across the capacitors is given by:

$$Q_2 = (V_{dac} - V_{out})C \qquad (4.14)$$

where V_{out} is the output voltage. According to the law of conservation of charges, the charges in both phases should be equal.

$$2(V_{in})C = (V_{dac} - V_{out})C \qquad (4.15)$$

V_{out} is subsequently be expressed as:

$$V_{out} = -(2V_{in} - V_{dac}) \qquad (4.16)$$

A buffer with a gain of 1 is connected at the output to eliminate charge sharing between capacitors from one pipeline stage to another. This technique results in considerable power savings as the only active block used is the buffer.

5   THE DESIGNED 8 BIT PIPELINE ADC

This chapter presents the designed 8 bit, 100MS/s Pipeline ADC. A partial – positive feedback amplifier which achieves high gain with very little power consumption is used in the design of the residue amplifier. The ADC is designed in 40nm CMOS process and achieves an ENOB of 7.69 bits at the Nyquist frequency while consuming 8.2mW of power.

5.1   Design Considerations

The main design considerations for the designed Pipeline ADC are discussed in this section.

1. Fully Differential architecture over Single-Ended architecture.
Even though the fully differential architecture requires twice as much components as the single-ended version, the fully differential architecture holds a number of design advantages over the single-ended version;
a. Increase in dynamic range of the data converter.
 The signal-to-noise ratio (SNR) of a data converter is given by the ratio of the signal power to the noise power. For a fully differential data converter, the signal power is quadrupled while the noise power is doubled. This results in a 3 dB SNR improvement over the single ended version [25].

b. Improved linearity.
With very good matching in a fully differential circuit, all even order harmonics can be cancelled due to the differential operation of the circuit. The major harmonic component now becomes the 3rd order harmonic.
c. Improved supply noise rejection.

Another benefit of the fully differential architecture is its ability to reject all common mode signals. Due to the existence of both digital and analog circuitry in data converters, a lot of noise is generated mainly from switching of digital circuitry and power supply. In the fully differential architecture, the noise generated is treated as common mode signals and is cancelled by the common mode rejection ratio of the circuitry. Fully differential circuits however in addition to increased component count, also require common mode feedback circuits (for operational amplifiers) which consumes extra power and increases design complexity. However, in this work, the amplifier used requires no common-mode feedback, resulting in extra power savings as compared to other fully differential designs.

2. Per Stage Resolution.

The two factors that were considered in choosing the number of resolutions to be resolved per stage are power consumption and latency. Resolving a large number of bits per stage reduces the latency, but increases the power consumption as the number of comparators increases exponentially with an increase in resolution. On the other hand, a small number of bits per stage increases the latency of the data converter. For optimum performance, the ADC designed in this work resolves 3 bits in the first 2 stages and 2 bits in the last stage. Hence, only 2 residue amplifiers and 17 comparators are required.

3. Choice of Sampling Capacitor.

The major source of noise in data converters is the KT/C noise. Re-calling (3.17), the minimum size of sampling capacitor required to keep the thermal noise below the quantization noise floor is $\frac{12\ KT}{V_{FS}^2}$. 2^{2N} . In addition to thermal noise consideration, the parasitic capacitances of the technology is also taken into account in selecting the

capacitor size. The sampling capacitor in addition to limiting thermal noise should also be considerably larger than the parasitic capacitances.

4. Pipeline Stage Scaling.

As previously discussed, stage scaling is one of the techniques used to reduce power consumption. In this work however, stage scaling was not used. Scaling the sampling capacitor in subsequent stages makes it comparable to parasitics, thus becoming highly unreliable. The major noise contribution stage in this design is the first stage since noise from subsequent stages is divided by the square of the gain from previous stages. However, the power saving advantage due to stage scaling is sacrificed.

5.2   Topology of the Designed Pipeline ADC

The topology of the designed Pipeline ADC is shown in Figure 5.1. It consists of 3 stages with the first two stages resolving 3 bits while the last stage resolves 2 bits, achieving a total of 8 bits. The choice of the resolution per stage provides optimum performance in terms of both power and latency as supported by [26].
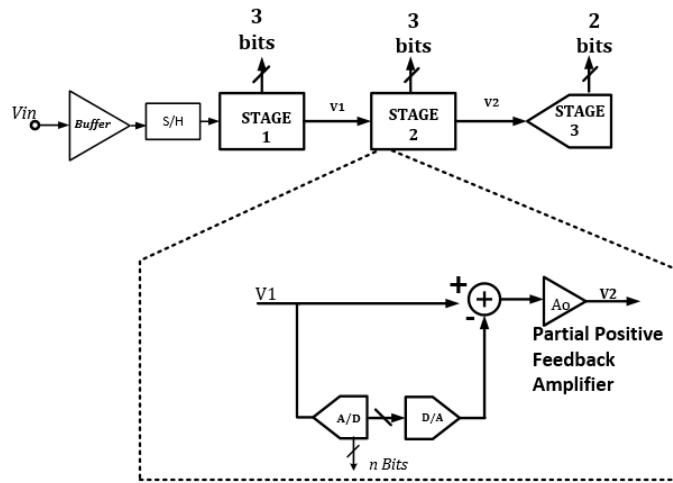

Figure 5.1: Block diagram of the designed Pipeline ADC

A total of 17 comparators are used, which is a significant reduction compared to the Flash ADC which would require 255 comparators for the same resolution. A dedicated sample and hold circuit is placed before the first stage to avoid distortion to the input signal. A buffer is used to drive the capacitor of the sample and hold amplifier. The MDAC used is modified from the conventional topology to eliminate the problem of mismatch between sampling capacitors. A partial – positive feedback amplifier is used in the MDAC network. This operational amplifier yields larger open loop gain with minimal power consumption as compared to the conventional folded cascode amplifier which is used in most designs. It also does not require the use of a common – mode feedback circuitry, providing extra savings in power.

5.2.1   *Sub–ADC Comparator*

The dynamic comparator shown in Figure 5.2 is used for the comparator design due to its smaller latch regeneration time and low power consumption. The comparator operates in two modes; regenerative mode and the reset mode. When the clock is low (reset mode), both output nodes are equal and held by the cross-coupled inverters at V_{DD}. When the clock goes high (regenerative mode), the difference in voltage at the gate of the input transistors will cause one branch to draw more current than the other. This results in one of the nodes at the drain of the input transistors being discharged faster than the other. The two inverters connected back to back form a positive feedback which ensures that one output is pulled towards V_{DD} while the other is pulled down to ground.

Transistors MKB1 and MKB2 are included to reduce kick-back noise which affects the reference voltages generated by the resistor ladder. Without transistors MKB1 and MKB2, the drain nodes of the input transistors are held at V_{DD} just before the comparator enters the regenerative mode. When the comparator enters regenerative mode, the drain nodes are quickly discharged through the clocked NMOS transistors (Mclk) resulting in kick-back noise to the input and reference

voltages [27]. With MKB1 and MKB2, the drains of the input transistors are disconnected from the circuit when the clock is low and hence there is no pre-charge of drain nodes, eliminating the kickback noise.
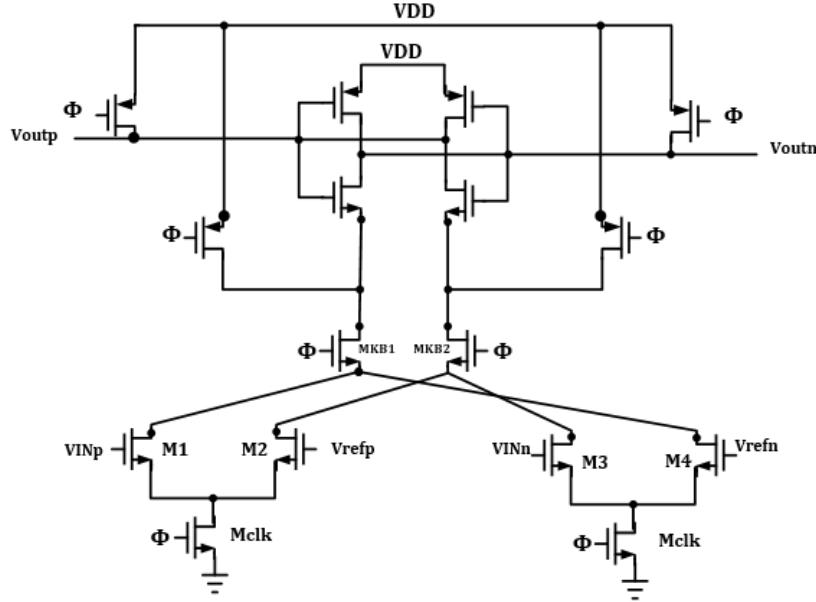

Figure 5.2:Dynamic Comparator with kickback noise reduction[27]

5.2.2   *Multiplexer Based Thermometer to Binary Decoder*

Each Sub–ADC consists of $(2^n - 1)$ comparators, each of which produces either a high output in the case of the input voltage being higher than the reference voltage, or a low output when the reference is higher than the input voltage. The output pattern of the comparators is thus known as a thermometer code. To convert this format to binary, a $(2^n - 1)$–to-n decoder is required. The Multiplexer Based Thermometer to Binary Decoder idea presented by [28] is used in obtaining the thermometer to binary conversion and is explained in this section.

For an N – bit Flash ADC, the most significant bit (MSB) of the binary code is always the same as the thermometer output at the level (2^{N-1}). To find the next most significant bit (MSB – 1), the thermometer codes are fed as inputs to a set of 2:1 multiplexers, with the MSB acting as the control bit for the multiplexers. The output of the $(2^{N-2})th$ multiplexer is selected as the (MSB – 1). The outputs of all the other multiplexers are again fed in as inputs to another set of multiplexers with the (MSB – 1) acting as the control bit. This is continued repeatedly until only one 2:1 multiplexer remains. The output of the last remaining multiplexer is known as the Least Significant Bit (LSB). Figure 5.3 shows a 3 bit multiplexer based encoder.
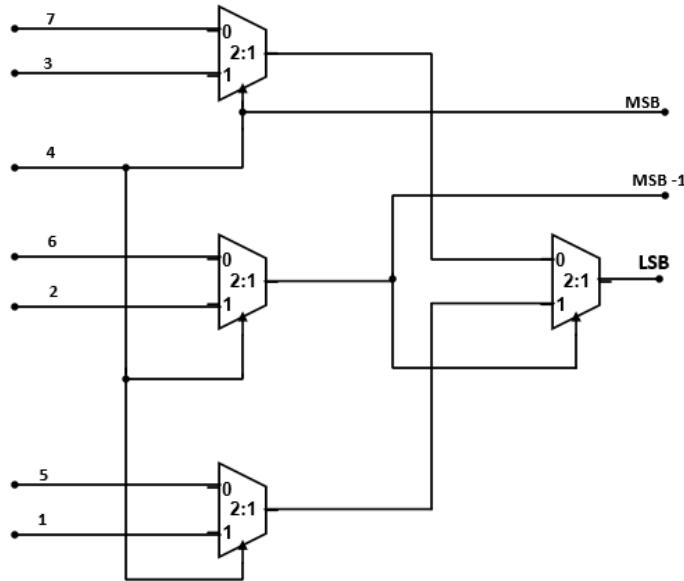

Figure 5.3: Multiplexer based Encoder for a 3 bit Flash ADC [28]

5.2.3   *Operational Amplifier*

As previously discussed in Section 3.3, achieving the gain and bandwidth requirements of the operational amplifier are vital in minimizing gain and settling errors in the Pipeline structure, which introduce distortion in the generated residue

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curve. Due to the typically high gain and bandwidths required, the operational amplifiers used in the Pipeline ADC architecture are the most power consuming component.

Conventionally, the folded cascode amplifier is mostly used due to its ability to yield high gain with fairly large bandwidths as well. However, due to technology scaling, the intrinsic output impedance of transistors have been reduced and hence more power is required to achieve the desired gain. Fully differential folded cascode structures also require common mode feedback circuits which result in extra power consumption. In [29] the single stage amplifier shown in Figure 5.4 is used to reduce the power consumed by the amplifier since it eliminates the need for a common mode feedback circuit.
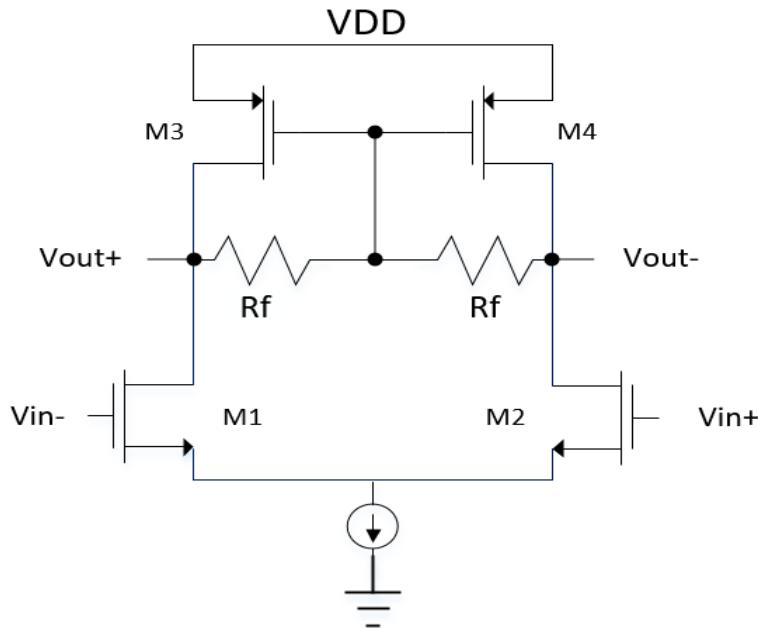

Figure 5.4: Conventional Single Stage Amplifier

The gain of this circuit is approximately given by:

$$A_o = g_{m1}R_f \qquad (5.1)$$

where g_m is the transconductance of the input transistor and A_o is the gain of the amplifier. The maximum achievable gain of this amplifier is limited by the size of the resistor R_F and the transconductance of the input transistor, M_1 as shown in (5.1). The single stage amplifier used in [29] achieved a gain of 20 dB while consuming 4.8mA of current.
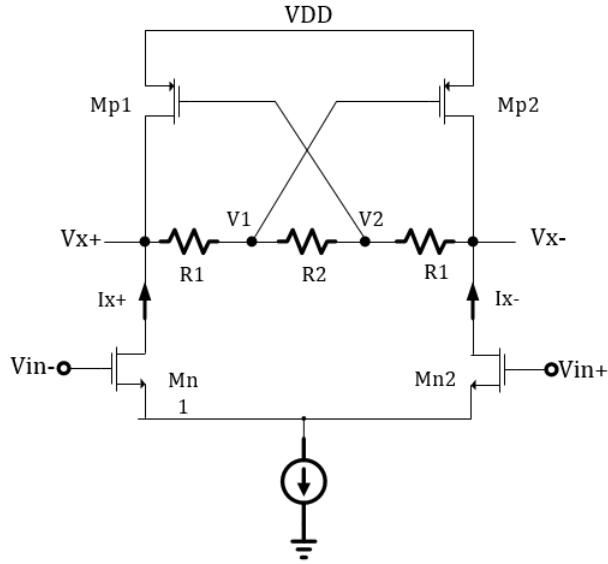

Figure 5.5: Proposed Partial Positive Feedback Amplifier

In this work, the Partial Positive feedback amplifier shown in Figure 5.5 is used to obtain high gain, with little power consumption. In addition to eliminating the need for a common mode feedback, which reduces the overall power consumption as compared to conventional fully differential folded cascode or 2 stage amplifiers, it provides additional degree of freedom for obtaining increased gain. The circuit operates mainly on the principle of current re-use. Through the resistor R_2, as shown in Figure 5.5, Alternating Current (AC) flows through the PMOS transistors (Mp1 and Mp2) unlike in Figure 5.4 where the gates of the PMOS transistors are held at virtual ground (AC ground) and hence no AC current flows

through. The flow of current through the PMOS transistors introduces both negative and positive impedance components to the total impedance seen from the output, V_x. By matching these two components as closely as possible, the total impedance seen at the output is increased and subsequently gain is increased.

From Figure 5.5 the current I_x can be expressed as:

$$I_x = \frac{2V_X}{2R_1 + R_2} + gm_pV_2 + (g_{dsp} + g_{dsn})V_X \tag{5.2}$$

The voltage V_2 is given by:

$$V_2 = \frac{-V_X \cdot R_2}{2R_1 + R_2} \tag{5.3}$$

Substituting (5.3) into (5.2), I_x can be expressed as:

$$I_x = \frac{2V_X}{2R_1 + R_2} - gm_p(\frac{V_X \cdot R_2}{2R_1 + R_2}) + (g_{dsp} + g_{dsn})V_X \tag{5.4}$$

The total impedance seen at the node V_x , is given by:

$$Z_x = \frac{1}{g_{dsp} + g_{dsn} + \dfrac{2}{2R_1 + R_2} - \dfrac{gm_pR_2}{2R_1 + R_2}} \tag{5.5}$$

where Z_x is the impedance seen at the node V_x in Figure 5.5. The gain is given by g_mR_x, where g_m is the transconductance of the input transistors and R_x is the output impedance. For a fixed g_m, the gain is maximum if the condition below is satisfied.

$$g_{dsp} + g_{dsn} + \frac{2}{2R_1 + R_2} = \frac{gm_pR_2}{2R_1 + R_2} \tag{5.6}$$

By satisfying (5.6), high gain values can be obtained without having to use large resistor sizes or increasing the transconductance of input transistors which results

in more power consumption as is the case in Figure 5.4. Due to the dependence of (5.6) on process-dependent parameters (g_{dsp}, g_{dsn}, gm_p), perfect cancellation is extremely difficult. To obtain high gain values, the Maximum Gain Condition (MGC) should be as minimal as possible as shown below:

$$MGC: g_{dsp} + g_{dsn} + \frac{2}{2R_1 + R_2} - \frac{gm_p R_2}{2R_1 + R_2} = 0 \qquad (5.7)$$

The expression for the gain is given by:

$$Gain = \frac{gm_n}{g_{dsp} + g_{dsn} + \frac{2}{2R_1 + R_2} - \frac{gm_p R_2}{2R_1 + R_2}} \qquad (5.8)$$

For a fixed load capacitor, the transconductance of the input transistors (gm_n) and hence the minimum amount of current required is determined by the *GBW* requirement of the application. The *GBW* of the operational amplifier is approximately given by:

$$GBW = \frac{gm_n}{C_L + C_P} \qquad (5.9)$$

where C_L is the load capacitance and C_P is the sum of all parasitic capacitances connected at the output of the operational amplifier. The resistors are tuned until (5.7) is as minimal as possible without affecting the operating conditions of the operational amplifier. This is done for fixed values of g_{dsp}, g_{dsn} and gm_p which are already determined by the desired operating point of the output. The resistor ratios are varied to obtain the optimum resistor ratio that yields the minimum value of

(5.7). As shown in Figure 5.6, for all resistor values, a resistor ratio of 1 gives the minimum value of (5.7). Hence the ratio of R_1 to R_2 is chosen to be 1 in this work.
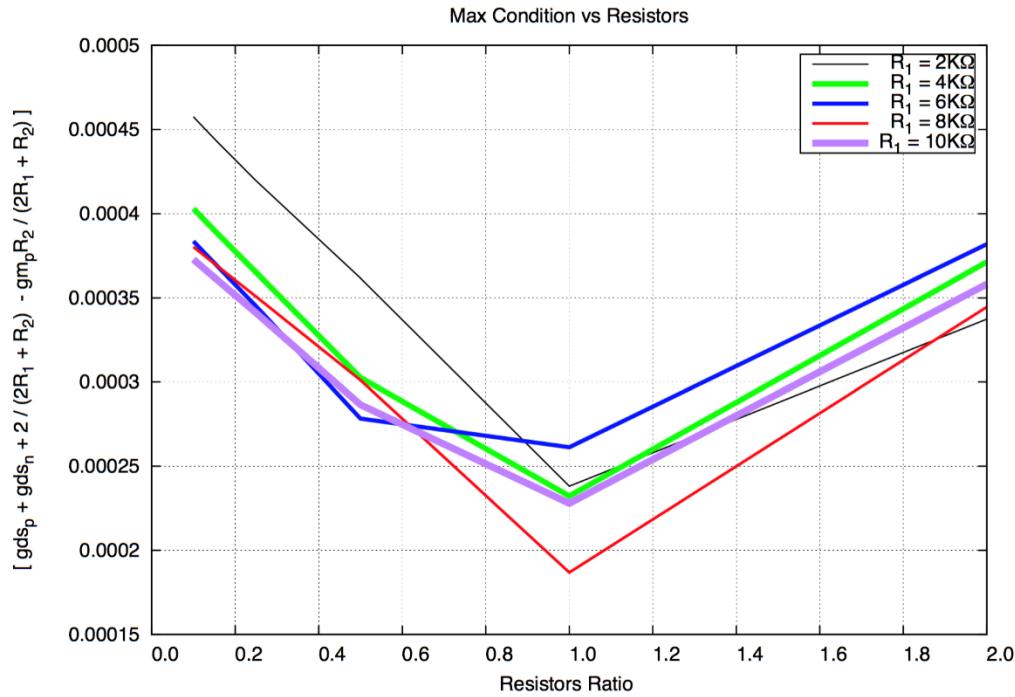

Figure 5.6: Maximum gain condition against varying resistor ratio.

With R_1 and R_2 equal, (5.7) can be re-written as:

$$MGC: g_{dsp} + \ g_{dsn} + \frac{2}{3R} - \frac{gm_p}{3} = 0 \qquad (5.10)$$

After fixing the resistor ratio, the absolute value of the resistors is determined. The resistors are varied to obtain the minimum value of (5.10) as shown in Figure 5.7.
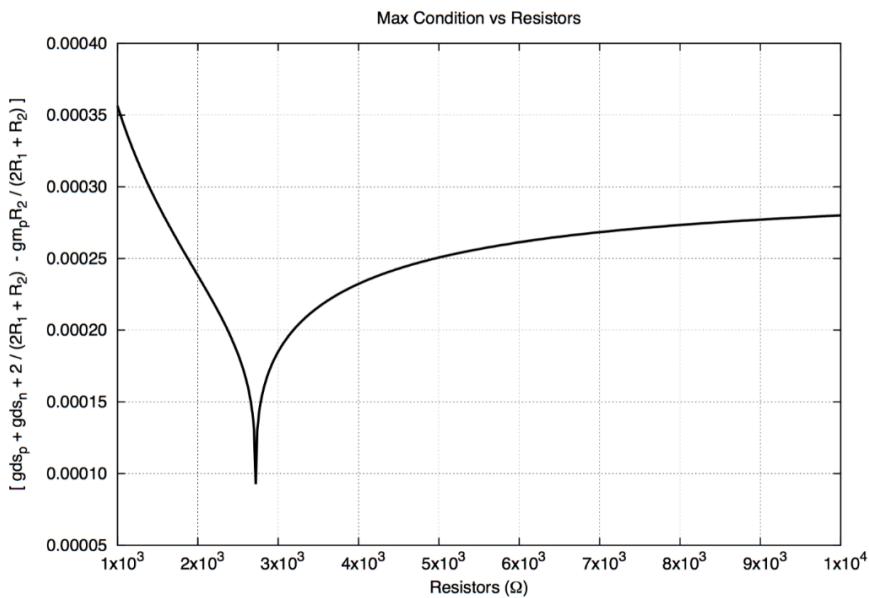
Figure 5.7: Maximum gain condition against varying resistor values

It is seen that (5.10) is minimum with a resistor of 2.7KΩ. With this resistor value, the maximum gain is obtained for a given input transconductance as shown in Figure 5.8.
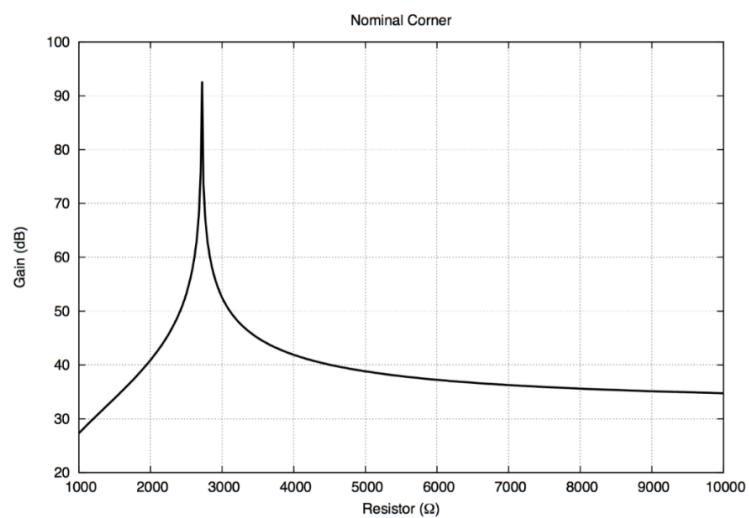

Figure 5.8: Gain variation against varying resistor values.

Due to the dependence of (5.10) on process parameters, the maximum gain in the nominal corner will vary across corners. For this application, a minimum gain of 40 dB is required across all corners. The variation of gain for different resistor values across all corners is shown in Figure *5.9*. For a minimum gain of 40 dB across all corners, a resistor of 2.9KΩ is chosen.
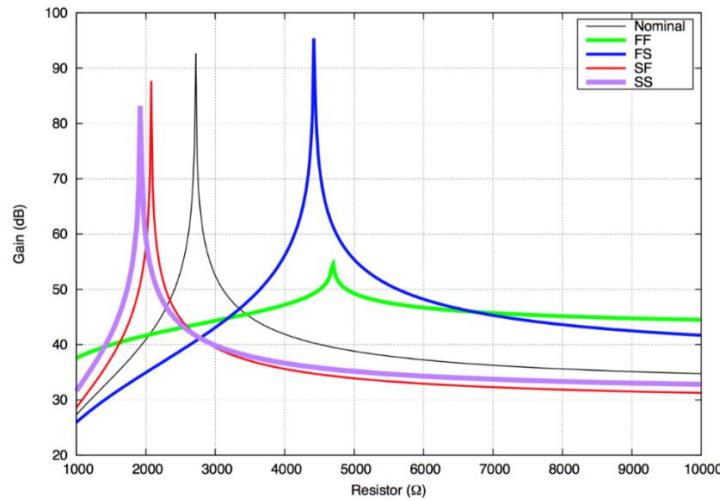

Figure 5.9: Gain variation for varying resistor values across all corners.
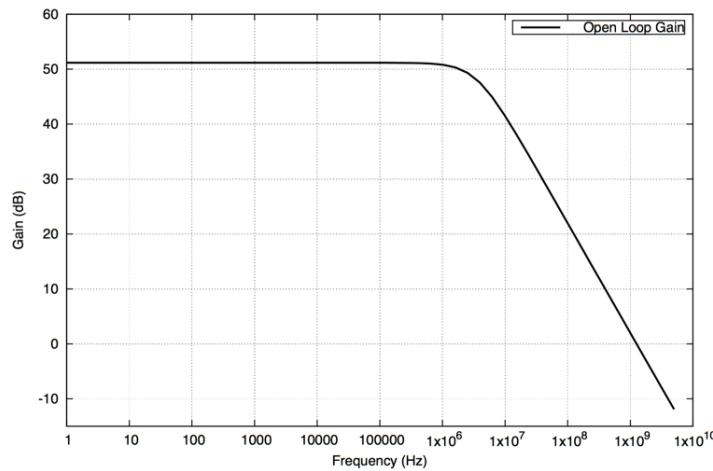

Figure 5.10: AC response of Partial Positive Feedback amplifier.

Figure 5.10 shows the AC response of the designed amplifier. It achieves a gain of 51 dB and a GBW of 1.2GHz while consuming 1.8mA of current.

Table 5.1 shows a comparison between the proposed amplifier and the conventional single stage amplifier with two resistors shown in Figure 5.4. It can be observed that the GBW remains the same across all corners for both amplifiers.

Table 5.1: Proposed amplifier against conventional single stage amplifier

ARCHITECTURE	CORNER.	GAIN (dB)	GBW (GHz)
PARTIAL POSITIVE FEEDBACK AMPLIFIER	NOMINAL	51	1.8
	SS	41.6	1.69
	FF	40.9	1.9
	FS	42.19	1.87
	SF	40.9	1.75
CONVENTIONAL SINGLE STAGE AMPLIFIER WITH 2 RESISTORS	NOMINAL	22.26	1.8
	SS	23.17	1.69
	FF	20.6	1.9
	FS	21.78	1.87
	SF	22.37	1.75

In the conventional single stage amplifier in shown in Figure 5.4, the gate voltage of the PMOS transistors is held at virtual ground and hence is not a function of the output voltage as shown in Figure 5.11.
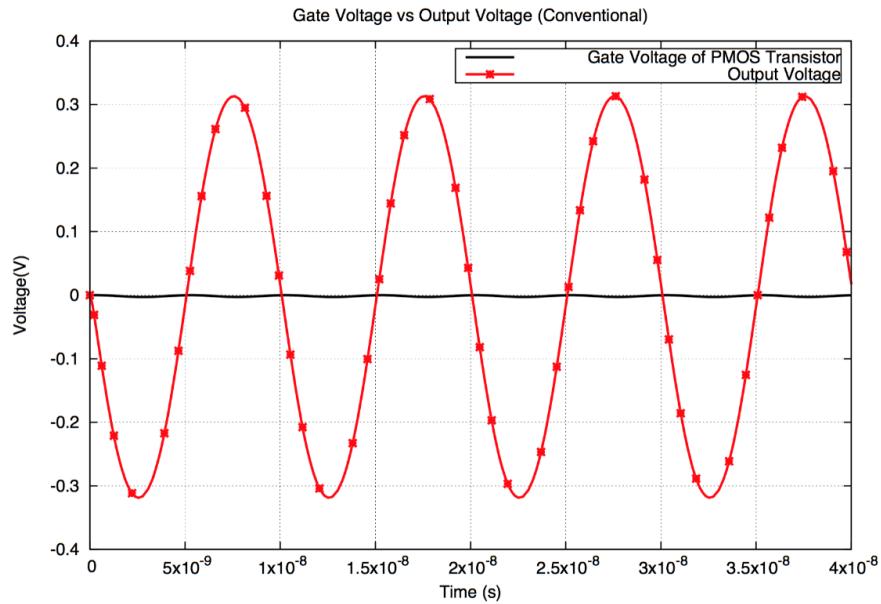
Figure 5.11: Gate voltage not changing as a function of output voltage.

Due to the fixed gate voltage the overdrive voltage of the PMOS transistors is fixed and the linearity of the operational amplifier is not affected by the PMOS transistors. However, with the partial positive feedback amplifier the voltage at the gate of the PMOS transistors varies as a function of the output and the ratio of R_2 to R_1 according to the equation below:

$$V_2 = -\frac{R_2}{R_1 + R_2} \cdot V_{out} \tag{5.11}$$

where V_2 is the gate voltage of transistor Mp1 in Figure 5.5. The negative sign indicates that the swing at the gate of the PMOS transistors is out of phase with the output swing.
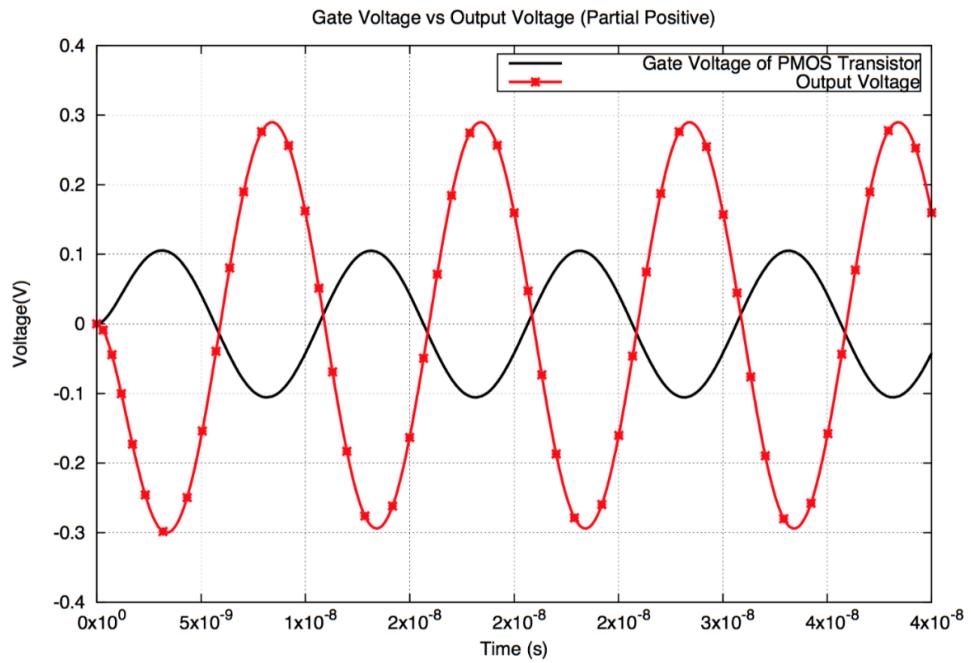
Figure 5.12: Gate voltage changing as a function of output voltage.

As shown in Figure 5.12, the gate voltage decreases as the output voltage increases resulting in an increase in the overdrive voltage of the PMOS transistors as the drain-source voltage decreases. With a large swing at the gate, the overdrive voltage could be larger than the drain-source voltage causing the transistor to go into the linear region. To avoid this, R_2 should always be less than or equal to R_1.

Figure 5.13 shows the layout of the proposed Partial Positive feedback amplifier.
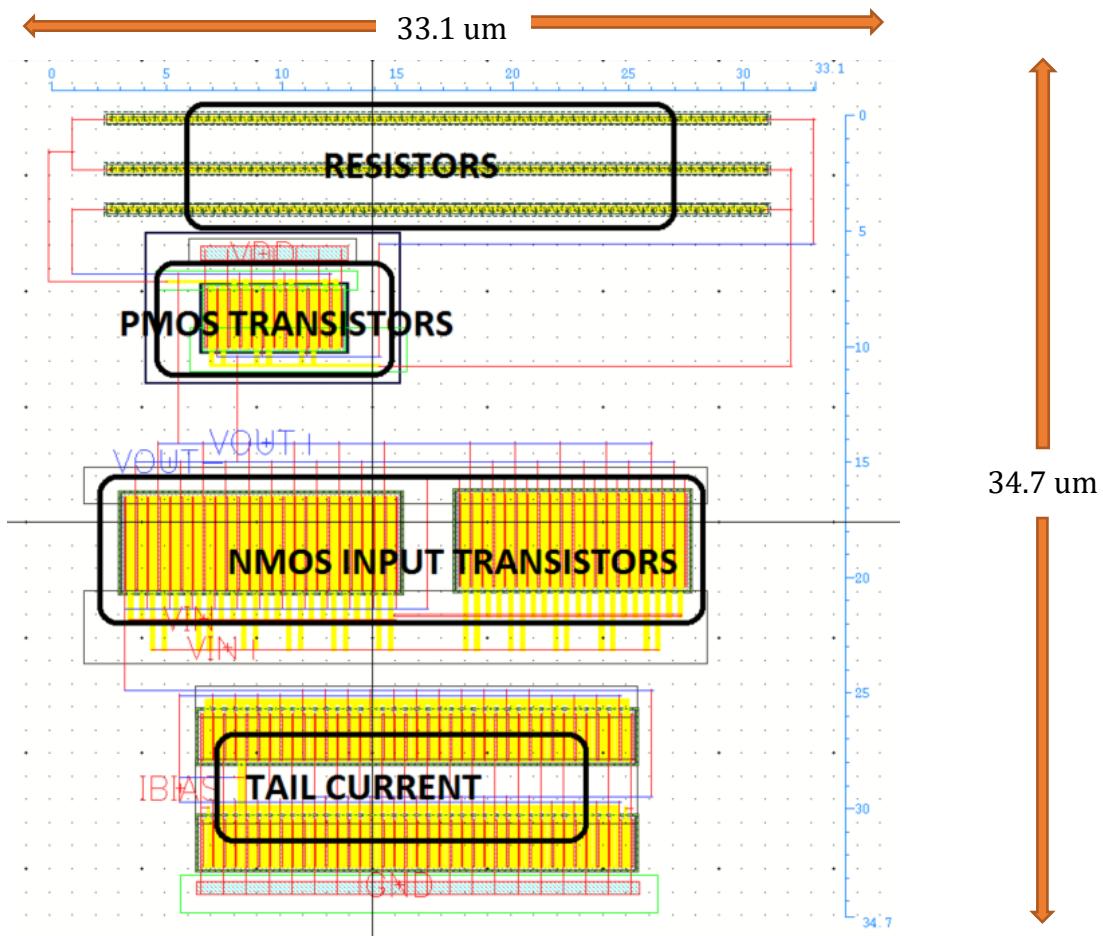
Figure 5.13: Layout of Partial Positive Feedback Amplifier

The post layout AC response of the designed Partial Positive Feedback Amplifier is shown in Figure 5.14 it achieving a DC gain of 49dB.
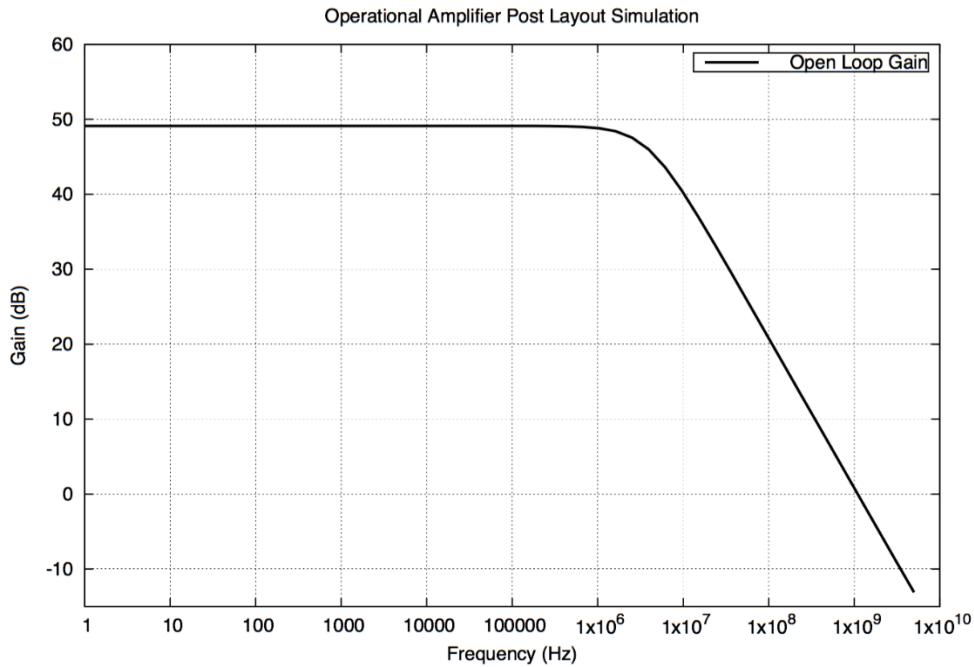
Figure 5.14: Post layout AC response

5.2.4 *Multiplying Digital to Analog Converter*

In the conventional MDAC structure of Figure 3.3, the sampling capacitor is obtained from a summation of several capacitors connected to the input voltage in the first phase of operation. The operation of the conventional MDAC is highly susceptible to capacitor mismatches as all sampling capacitors would have to be matched to obtain the ideal transfer characteristics of the MDAC which is challenging. To reduce the matching requirements, the MDAC structure shown in Figure 5.15 is used. It uses just one sampling capacitor and a multiplexer network to select the appropriate reference voltage to subtract from the input signal before the amplification is done.

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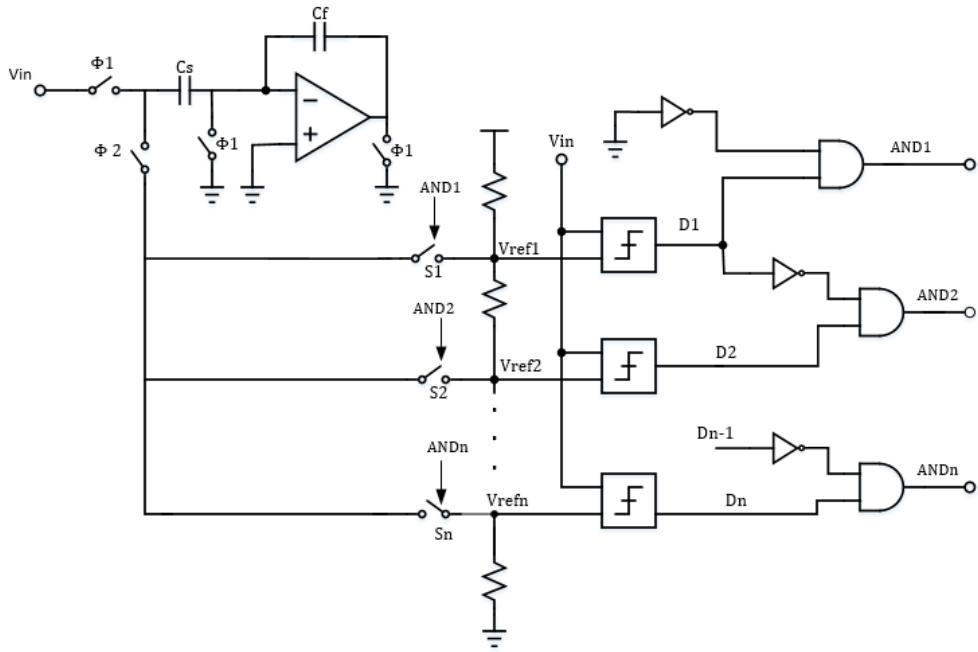
Figure 5.15: Multiplexer based MDAC

In the first phase of operation, the input voltage is sampled unto the sampling capacitor, *Cs*. At the same time, the comparators take decisions with the sampled input voltage and various reference voltages. In the second phase, the reference voltage directly below the input voltage is subtracted from the sampled input and subsequently amplified. The multiplexer consists of a combination of *AND* and Inverter logic gates that enable it to select the correct reference voltage for subtraction. The *AND* and Inverter logic gates are driven by the output of the comparators (*D1-Dn*). The output of each *AND* gate (*AND1 – ANDn*) turns on a particular switch depending on the level of the input voltage to allow a particular reference voltage to be subtracted from the input voltage.

Consider a sampled input voltage greater than *Vref2* but less than *Vref1*. The comparator output *D1* will be 0 while output *D2* will be 1. *AND2* will be held at a logic 1 while all other *AND* outputs are held at logic 0. This will turn on the switch, *S2*, and

subsequently the reference voltage *Vref2*, which is the reference voltage directly lower than the input voltage, is passed to be subtracted from the input voltage.

 It should be noted that only one output of the *AND* logic can be high for a particular input voltage. This allows a unique reference to be selected for every unique input voltage.

The transfer function of the residue curve obtained from the MDAC structure is given below:

$$V_{out} = \frac{C_S}{C_f} (V_{in} - Vref_i) \tag{5.12}$$

where $Vref_i$ refers to the reference voltage immediately below a given input voltage. As can be observed, transfer curve is now dependent only on matching between the single sampling capacitor, C_s , and the feedback capacitor, C_f.

5.2.5   *Bootstrapped Switch*

The design of switches in switched-capacitor circuits could be as simple as an NMOS transistor operating in linear region as shown in Figure 5.16.
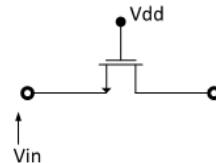

Figure 5.16: NMOS Switch

The resistance of the switch is given by:

$$R_{ON} = \frac{1}{\mu_n Cox \left(\frac{W}{L}\right)(V_{gs} - V_{th})} \tag{5.13}$$

where R_{ON} is the on-resistance of the switch, $V_{gs} = V_{DD} - V_{in}$. Ideally, switches are expected to keep a constant resistance independent of the input signal. A change in the resistance of the switch results in distortion of the output signal.

To achieve constant switch on-resistance, the transmission gate shown in Figure 5.17 was introduced. As input voltage increases, the on-resistance of an NMOS switch increases, while that of a PMOS decreases. By connecting the NMOS and PMOS together, a fairly constant resistance independent of input voltage can be obtained. However, for this to be effective matching between the NMOS and PMOS transistors is required which is practically not possible.
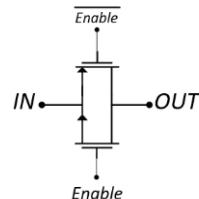

Figure 5.17: Transmission gate

An improved solution is the use of Bootstrapped switches as shown in Figure 5.18 [30].
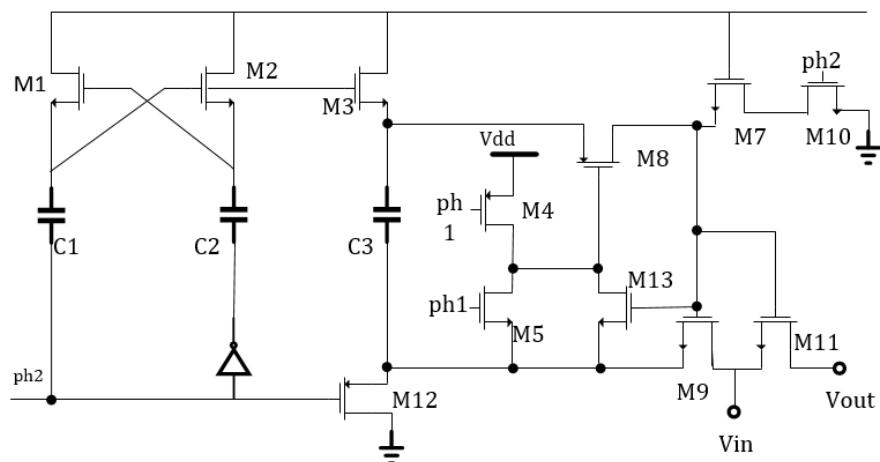
Figure 5.18: Clocked Bootstrap Switch [30]

The basic principle of Figure 5.18 is to keep the gate-source voltage of the switch constant, hence keeping the switch on-resistance constant. The operation of Figure 5.18 is described as follows [30];

When the clock phase is low, the gate of the main switch, *M11*, is discharged to ground through *M7* and *M10*. At the same time, the capacitor *C3* is charged up to *VDD* by *M3* and *M12*. During the on phase, the gate of *M8* is pulled down by *M5* allowing the charge stored on the capacitor *C3* to flow onto the gate of the switch *M11*. Transistor *M9* enables the gate of *M11* to track the input voltage at the source of *M11* shifted by *VDD*. Hence, there is always a constant voltage across the gate and source of *M11*, keeping the on-resistance constant for all values of the input voltage. The capacitor *C3* should be sized to be sufficiently large to mitigate the effect of parasitic capacitances. Since the supply voltage in this design is 2.4V, by charging the capacitor *C3* to *VDD* the gates of transistors *M11* and *M9* are held at a voltage of $2.4V + Vin$, which is quite large. In this design, to prevent the gates of transistors *M11* and *M9* from holding an excessive voltage ($VDD + Vin$), the capacitor *C3* is charged up to a fixed voltage of 1V. Therefore, the maximum voltage across the gate of the transistors is $1V + Vin$.
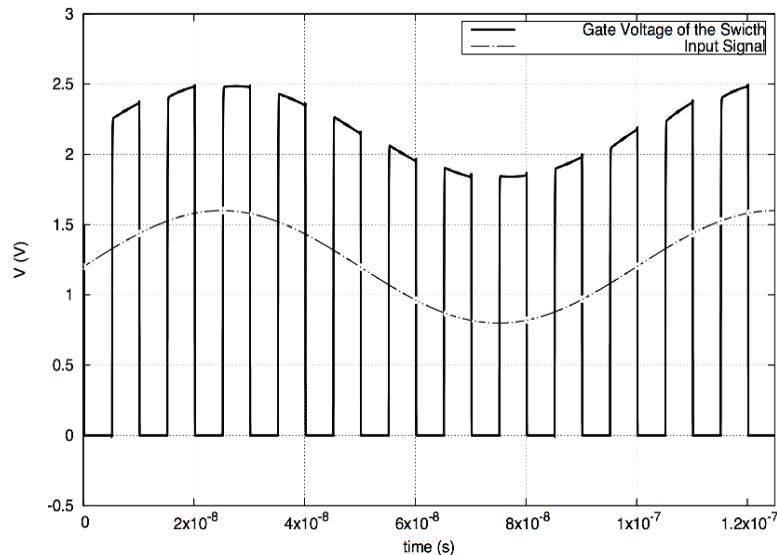
Figure 5.19: Operation of Clocked bootstrap switch

As shown in Figure 5.19, when the switch is on gate voltage is greater than the input signal by a fixed voltage of 1V. Hence the voltage difference between gate and source is always constant and independent of the input voltage making the switch operation highly linear.

5.2.6 *Final Block Level Schematic of Designed ADC*

The block level schematic of the designed ADC is shown in Figure 5.20.
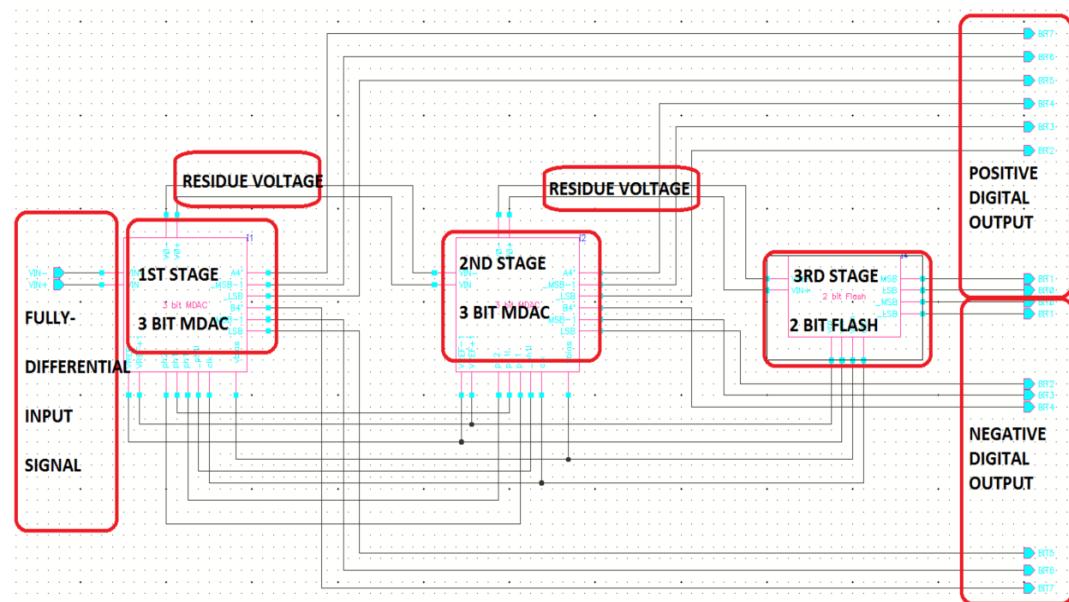
Figure 5.20: Final Block Level Schematic of Designed ADC

5.3   Simulation Results

A comparison of the designed Pipeline ADC with other published work is presented in

. An SNDR of 48.08 dB is achieved at the Nyquist frequency with a total power consumption of 8.2mW.

Table 5.2: Results summary and comparison

Publication	**This Work**	[2]	[20]	[24]	[23]
Sampling rate (MS/s)	100	50	40	75	160
Resolution	8	10	10	12	12
SNDR (dB)	48.2	58.2	59	67	65.6
Power (mW)	**8.2**	**9.9**	**54.9**	**290**	**102.96**
Supply (V)	2.4	1.8	3	3	1.8
Current (mA)	3.4	5.5	18	96	57
FoMp (pJ/ conv. bit)	0.38	0.3	1.86	2	0.41
iFoM (pA/ conv. bit)	0.15	0.165	0.62	0.69	0.22

$$FoMp\ (pJ/conv.bit) = \frac{Power}{2^{\frac{SNDR-1.76}{6.02}} \cdot fs} \tag{5.14}$$

$$iFoM\ (pA/conv.bit) = \frac{Current}{2^{\frac{SNDR-1.76}{6.02}} \cdot fs} \tag{5.15}$$

Equations (5.14) and (5.15) are the two FoMs used in evaluating the performance of the designed ADC. Equation (5.14) takes into consideration the power consumption (power), sampling speed (fs) and the SNDR of the ADC. To normalize (5.14) with respect to supply voltage, (5.15) which takes into consideration the current consumed by the ADC is generated.

Figure 5.21 shows the frequency spectrum of the ADC at 24.9 MHz.
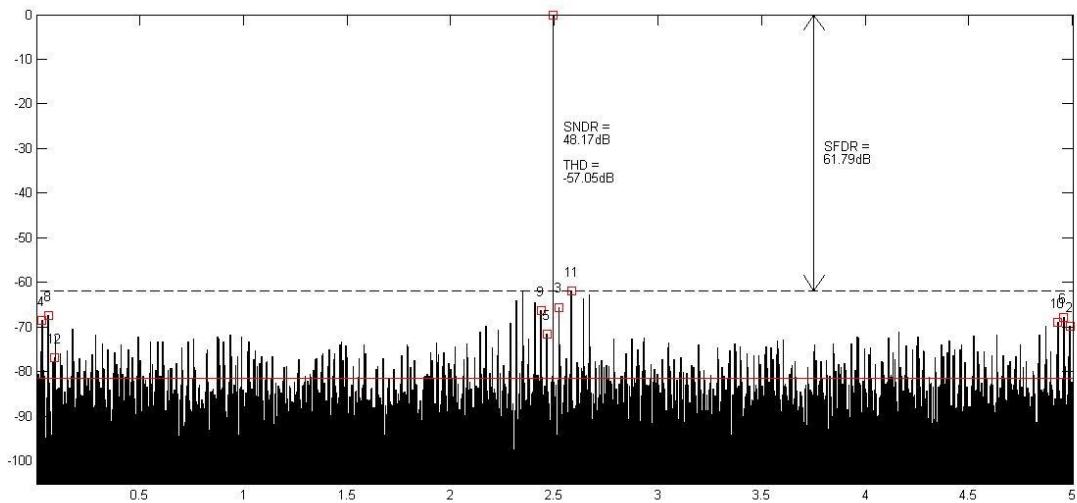
Figure 5.21: Frequency spectrum at 24.9MHz

Figure 5.22 shows the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) of the designed converter at 8 bits. Ideally, the analog voltage difference between two adjacent digital codes in an ADC should correspond to 1 LSB. Practically, there is a deviation from this ideal behavior. The analog voltage

difference between two digital codes may vary from the ideal case of 1 LSB. This variation could result in missing codes (i.e. some analog input voltages will have no corresponding digital codes). The DNL refers to the deviation of the analog voltage difference between two adjacent digital codes from the ideal case of 1 LSB. A DNL within ± 1 of an LSB indicates that there are no missing code in the data converter. As shown below, the designed data converter achieved a DNL within ± 1 of an LSB which means that all the digital codes corresponding to an 8-bit ADC are available. The cumulative sum of DNL is known as the INL.
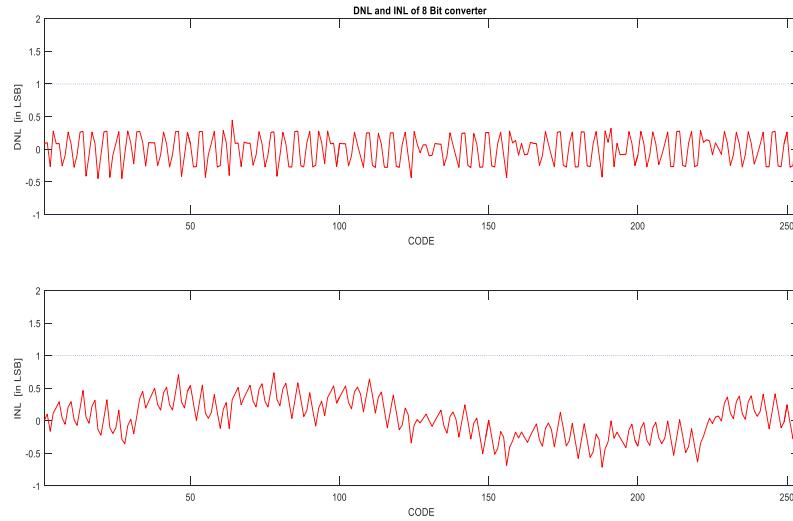

Figure 5.22: DNL and INL at 8 bits

Figure 5.23 shows the variation of the Signal-to-noise and distortion ratio as well as the spurious free dynamic range with varying input frequency. The input frequency is varied from DC to the Nyquist frequency.

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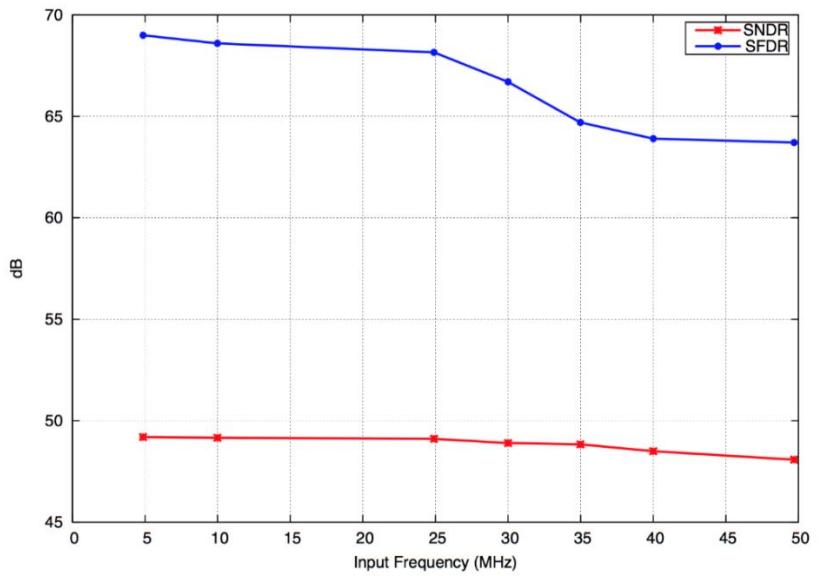
Figure 5.23: SFDR and SNDR across the input frequency range

6   CONCLUSION

In this thesis, a Partial Positive Feedback amplifier is used in the design of an 8-bit, 100MS/s fully differential Pipeline ADC in 40nm CMOS technology.

The proposed amplifier ensured that high gain was obtained with very little power consumption. The designed amplifier achieved an open loop gain of 51 dB while consuming 1.8mA of current. A comparison between this amplifier and a conventional single stage amplifier showed a 20 dB increase in gain with the same power consumption.

Capacitor mismatch errors were mitigated by using a multiplexer based MDAC which uses a single sampling capacitor instead of the combination of capacitors as is the case in the conventional MDAC. Consequently, the challenge of matching sampling capacitors as well as the need for complex calibration techniques for capacitor mismatch is reduced.

The designed ADC achieved an ENOB of 7.69 bits at the Nyquist frequency which corresponds to an SNDR of 48.08 dB.

REFERENCES

[1]   Y. Tawk, J. Costantine, and C. G. Christodoulou, "Cognitive-radio and antenna functionalities," IEEE Antennas Propag. Mag., vol. 56, no. 1, 2014.

[2]   I. Ahmed, "Pipelined ADC design and enhancement techniques," vol. 1542. Dordrecht: Springer Netherlands, 2010.

[3]   G. P. C. Gamauf, A. Nemecek , F.P. Leisenberger, "Design and characterization of a 10 bit pipeline-ADC for 100MS/s in 0.18um CMOS," IEEE, DOI-10.1109/Austrochip.2014.6946311 , October 9th, 2014.

[4]   Gartner, "Data converter chips,"April 13, 2005 http://www.hit.bme.hu/~papay/edu/Conv/pdf/ADC_DAC.

[5]   C. P. Huang, Y. Z. Lin, C. W. Lin, Y. T. Shyu, and S. J. Chang, "A systematic design automation approach for flash ADCs," 2010 Int. Symp. Next-Generation Electron. ISNE 2010 - Conf. Progr., pp. 81–84, 2010.

[6]   R. L. Geiger, N. Strader, and N. R. Strader, VLSI design techniques for analog and design circuits. McGraw-Hill Series, 1990.

[7]   D. Johns and K. Martin, Analog integrated circuit design. John Wiley & Sons, 1997.

[8]   Rudy van de Plassche, CMOS analog-to-digital and digital-to-analog converters, 2nd Edition. Springer International, 2003.

[9]   P. T. F. Kwok and H. C. Luong, "Power optimization for pipeline analog-to-digital converters," IEEE Trans. Circuits Syst. II Analog Digit. Signal Process., vol. 46, no. 5, pp. 549–553, 1999.

[10]   Analog Devices, "Complete 12-Bit, 65 MSPS ADC converter (AD9226-Data Sheet)," November 1st, 2016.

http://www.analog.com/media/en/technical-documentation/data-sheets/AD9226.pdf

[11]   D. Johns, K. Martin, and T. C. Carusone, Analog integrated circuits design 2nd. John Wiley & Sons, 2012.

[12]   M. K. Hati and T. K. Bhattacharyya, "An 8-b 250-Msample/s power optimized pipelined A/D converter in 0.18-um CMOS," 2015 Int. Conf. VLSI Syst. Archit. Technol. Appl. VLSI-SATA 2015.

[13]   M. Geelen and K.Bult, "A fast-settling CMOS op-amp for SC circuits with 90-dB DC gain," IEEE J. Solid-State Circuits, vol. 25, no. 6, pp. 1379–1384, 1990.

[14]   F. You, S.H.K. Embabi, and E.Sanchez-Sinencio, "A multistage amplifier topology with nested Gm-C compensation for low-voltage application," 1997 IEEE Int. Solids-State Circuits Conf. Dig. Tech. Pap., pp. 348–350, 1997.

[15]   Sebastian Hoyos, "Mixed signal interface," in ECEN610 lecture notes, Texas A&M Universtity, Department of Electrical Engineering , 2015.

[16]   B. Razavi, "Design of analog CMOS integrated circuits," Ch.2, Sec. 2.2, pp. 13–23, 2001.

[17]   C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 731–740, 2010.

[18]   S. Thakre and P. Srivastava, "Design and analysis of low-power high-speed clocked digital comparator," Glob. Conf. Commun. Technol. GCCT 2015, pp. 650–654, 2015.

[19]   L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, "CMOS dynamic comparators for pipeline A/D converters," 2002 IEEE Int. Symp. Circuits Syst. Proc. (Cat. No.02CH37353), vol. 5, pp. 157–160, 2002.

[20] I. Mehr and L. Singer, "55-mW, 10-bit, 40-Msample/s nyquist-rate CMOS ADC," IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 318–325, 2000.

[21] D. Y. Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," IEEE Trans. Circuits Syst. I Regul. Pap., vol. 51, no. 11, pp. 2123–2132, 2004.

[22] B. Murmann, "VLSI data conversion circuits," in l6ecture notes, Stanford Universtiy, Department of Electrical Engineering, 2010.

[23] A. A. Vatanjou and A. Dadashi, "A high speed power efficient pipeline ADC in 0.18um," Faibl. Tens. Faibl. Consomm., pp. 8–11, 2013.

[24] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," IEEE J. Solid-State Circuits, vol. 38, no. 12, pp. 2040–2050, 2003.

[25] J. Melorose, R. Perroy, and S. Careas, "Low voltage pipeline A/D converter," Statew. Agric. L. Use Baseline 2015, vol. 1, 2015.

[26] Yun Chiu, "High-performance pipeline A/D converter design in deep-submicron CMOS," University of Carlifornia, Berkley, 2004, Thesis.

[27] T. Sundström and A. Alvandpour, "A kick-back reduced comparator for a 4-6-bit 3-GS/s flash ADC in a 90nm CMOS process," Proc. 14th Int. Conf. "Mixed Des. Integr. Circuits Syst. Mix. 2007, pp. 195–198, 2007.

[28] E. Sail and M. Vesterbacka, "A multiplexer based decoder for flash analog-to-digital converters," 2004 IEEE Reg. 10 Conf. TENCON 2004., vol. D, 2004.

[29] B. D. Sahoo and B. Razavi, "A 10-b 1-GHz 33-mW CMOS ADC," IEEE J. Solid-State Circuits, vol. 48, no. 6, pp. 1442–1452, 2013.

[30] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 599–606,

1999.