EFFICIENT HIGH-PERFORMANCE MILLIMETER-WAVE FRONT-END INTEGRATED CIRCUIT DESIGNS AND TECHNIQUES IN SiGe BiCMOS

A Dissertation

by

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ABSTRACT

This dissertation presents various “efficient” design techniques for mm-wave front-end integrated circuits in regards to dc power, bandwidth, and chip size. The ideas, while suitable for different CMOS/BiCMOS processes, were implemented using a 0.18-μm SiGe BiCMOS process. The proposed techniques are validated through the actual implementations of several building blocks constituting two different front-end sections: a V-band OOK/pulse transceiver front-end and a concurrent K-/V-band receiver front-end, where K-band ranges from 18 to 27 GHz and V-band from 40 to 75 GHz.

As one of the constituent components in the V-band pulse transmitter, a 60-GHz active OOK/pulse modulator has been designed with an emphasis on the enhancement in the ON/OFF isolation. Having a decent gain (higher than 10 dB), the designed modulator can also be used as a driver stage, which can save the chip area and possibly the dc power consumption compared to the combination of a switch-based passive modulator and a drive amplifier. For the receiver front-end, a wideband V-band low-noise amplifier (LNA) has been designed. Employing a wideband gain shaping technique through two *T*-type inter-stage matching networks, the designed LNA features very high gain-bandwidth product compared to the conventional gain-staggered wideband amplifier designs for a given dc power consumption.

For the concurrent K-/V-band receiver front-end, a low-noise and variable gain stages have been designed. As the first component of the receiver chain, a concurrent dual-band LNA has been designed within a similar footprint required for a single-band

amplifier operating either at K- or V-band. The most significant direct intermodulation (IM) product and harmonics are suppressed by a simple rejection network between the input and cascode devices of the 1st stage. This network also plays a crucial role in achieving dual-band input matching through Miller effect. For amplitude control purposes in the RF stage, a variable gain amplifier (VGA) operating concurrently at K- and V-bands has been developed starting from a wideband amplifier design. By replacing the inductors in the wideband design with the transformer-coupled resonators (TCRs), the critical direct IM products can be suppressed without increasing the active chip area. Gain tuning is achieved by conventional current steering, but a new technique is applied to reduce phase variation in the course of gain tuning process, which is one of the most critical concerns, especially in phased array systems.

DEDICATION

To my beloved family…

ACKNOWLEDGEMENTS

I would first like to show my sincere appreciation to my advisor, Professor Cam V. Nguyen. The painful but enjoyable journey to my doctoral degree has finally come to an end with his thoughtful guidance and mentorship. Keeping the balance between macro- and micro-managing, he has led me to stand at this point. Technical discussions with him always gave me intuitions and motivations in seeking for any possible contributions to our field of study. In addition to being a routine academic advisor, he has been a good conversation partner in the subject of Asian history as well. The casual conversation with him blew some of the stresses away and helped me stay focused on the research.

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My respect and appreciation to my family can never be exaggerated. Mom and Dad, you have always been encouraging and trusting me without urging at any points during my entire study. Dad, you are the most diligent and honest person I have ever known and I have been trying to resemble you in every aspect. Also, my thanks go to my younger brother Jaehwan.

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CHAPTER I

INTRODUCTION

1.1 Overview and Objectives

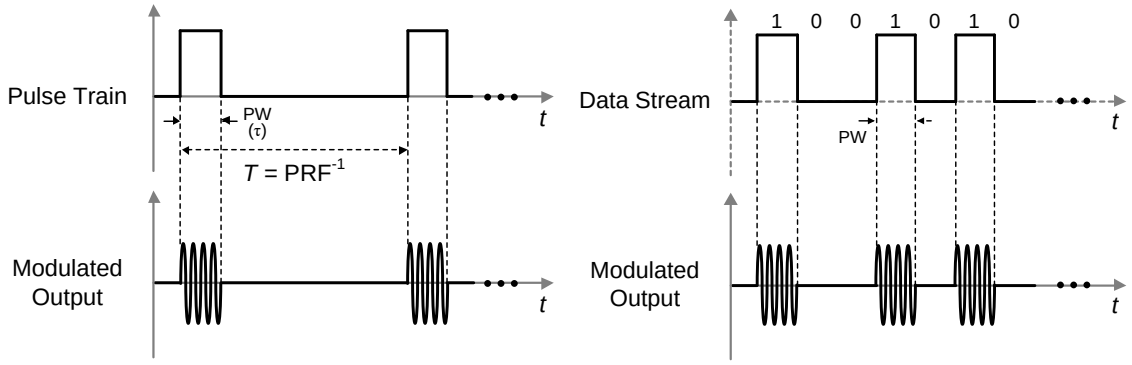
Having relatively unoccupied and inherently wide available frequency spectrum, millimeter-wave (mm-wave) frequencies, defined as the frequencies between 30 GHz to 300 GHz, have been proven to be a suitable candidate for the next generation of communication with high achievable data throughput and high resolution/accuracy sensing applications, etc. As the operating frequency increases and hence the wavelength scales down, passive components such as antennas, on-chip spiral inductors and transmission lines can be realized within much smaller footprint than those at lower microwave frequencies, which produces various advantages such as system integration in a reduced chip area, highly integrated networks of systems, low cost, and increased directivity by employing an array of multiple channel elements in a given chip area.

Given a fixed dc current, however, a maximum available gain (MAG) of an active device decreases as the frequency is increased. It implies that in order to achieve a gain similar to that at lower microwave frequencies, more dc power should be consumed, which makes the mm-wave system difficult to be employed in small and mobile battery powered devices or platforms and in networks of multiple systems with very tight power budget requirements. Another problem of the mm-wave circuits is that the circuit performance is more sensitive to any inaccuracy in the design process such as simulations, device modeling, and fabrication process variation, etc. than circuits operating at lower microwave frequencies due to the high operating frequencies upon which many of the design parameters depend on.

Therefore, for successful development and deployment of mm-wave systems for commercial and defense applications, especially in the consumer market, power-efficient design and size minimization are highly desired.

1.2 Millimeter-Wave OOK/Pulse Transceiver

Millimeter-wave frequencies are more suitable than lower microwave frequencies for applications such as sensing using very short pulses or high data-rate transmission due to the inherently wide available fractional bandwidth. When mm-wave frequencies are used in pulsed radar systems or on-off keying (OOK) system, one can expect better range resolution or higher data rate than the systems using lower frequencies due to narrow pulse widths.



(a) (b)

Fig. 1.1. Transmitted waveforms of (a) pulsed radar and (b) OOK systems.

Fig. 1.1 shows the transmitted waveforms for pulsed radar and OOK systems. In case of a pulsed radar system as shown in Fig. 1.1(a), there are two fundamental parameters defining the specifications of pulsed radar systems [1]: τ and PRF. τ is the

pulse width, which is the primary factor determining the range resolution, dictating the minimum distinguishable range between nearby targets, defined as

$$\Delta R = \frac{1}{2} c_o \tau \tag{1.1}$$

where c_o is the speed of light in free space. PRF (pulse repetition frequency) is the rate at which the pulses are transmitted and is inversely proportional to T, which defines the maximum unambiguous range (such that the reflected signal should be received before the transmission of the next pulse) as

$$r_{\max} = \frac{c_o}{2 \cdot \mathrm{PRF}}. \tag{1.2}$$

For an OOK system as shown in Fig. 1.1(b), the data rate is solely determined by the pulse width, which is regarded as a bit interval, as

$$\text{Data Rate} = \frac{1 \text{ bit}}{\text{Pulse Width [sec]}} \tag{1.3}$$

where the unit of data rate is “bits per second”.

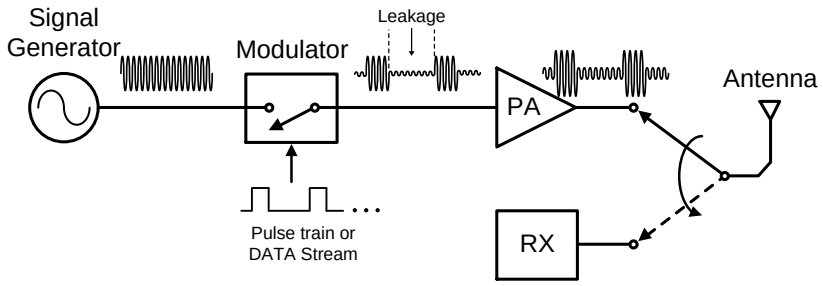


Fig. 1.2. Simplified pulsed radar transceiver front-end.

Fig. 1.2 shows a simplified pulsed radar system with more weight on the transmitter part, where the transmitter can also be used in an OOK system. The

continuous wave (CW) generated by the signal generator is modulated by the pulse train (or data stream), which turns on and off the modulator. Ideally, the modulator allows transmission of the carrier signal only for the duration that the pulses are present.

In an actual system, however, the finite isolation between the input and output of the modulator results in carrier leakage during the off states, which may lead to false target detection, bit errors, etc. The leakage at the modulator output is small compared to the signal for ON state (typically 20 ~ 30 dB lower) and one may think it does not have critical impacts on the system performance. However, its adverse effects become more significant as the leakage signal goes through the chain of the power amplification stages typically having large gain before transmitted through the antenna. One can argue that designing the power amplifier (PA) to be switched on and off by the same pulse train (or data stream) would greatly help reduce the transmission of the leakage signal. While it sounds plausible, the limited turn-on/off characteristics of PA will cause a bottleneck to the minimum achievable pulse width (or maximum achievable data rate) of the overall system. Therefore, it is desirable to improve the off-state isolation of the modulator to suppress the leakage signal as much as possible.

Another concern is to design all the constituent building blocks to have sufficiently wide bandwidth to process the short pulses without any distortion that may cause degradation in the signal fidelity or inter-symbol interference (ISI). Pulse shaping using filters such as Gaussian, raised-cosine, and sinc filters can be used to relax the burden on the minimum required bandwidth for processing short pulses or high data rate stream. While pulse shaping techniques can reduce the bandwidth requirement for the

pulsed radar receiver, they can also cause ISI problems in an OOK system, which significantly worsens the bit error rate (BER) performance of the receiver. Therefore, it is important to design all the b constituent locks with sufficiently wide bandwidth.

1.3 Concurrent Multi-Band Receiver

In the regime of digital and analog integrated circuits, CMOS technology has been dominating due to the low cost and easy integration between analog and digital blocks. For RF and mm-wave frequency ICs, however, III-V compound semiconductor devices such as GaAs, GaN, and InP have traditionally dominated mainly due to the superior power handling capability, lower thermal noise, higher operating frequencies, and lower substrate losses, while they suffer drawbacks such as higher manufacturing cost, limited integration capability with digital baseband ICs, lower production yields, etc. [2]. Therefore, catching up the high frequency and low loss characteristics of the compound semiconductor devices with silicon will allow full system integration on a single silicon substrate and hence lower production cost, which are the ultimate goals of RF / mm-wave ICs. Even though low cost production is possible using Silicon process, the cost is directly related to the system die size on a Silicon wafer. In order for the low cost mass production, the size of integrated system should be minimized as much as possible.

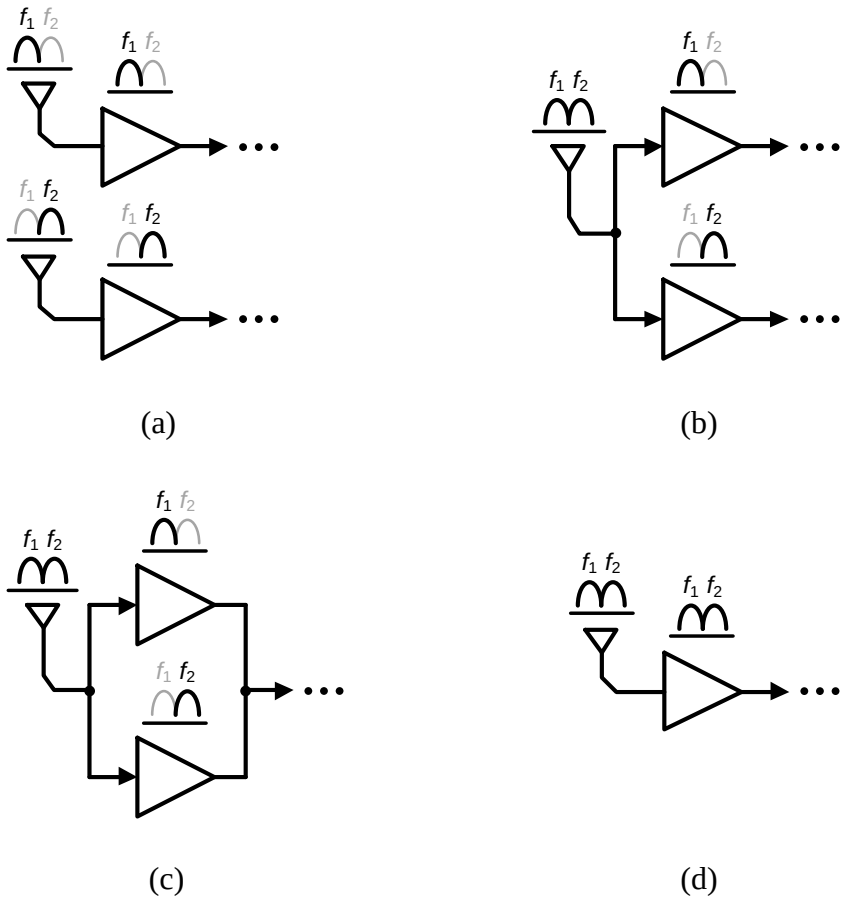


Fig. 1.3. Several possible realizations of concurrent dual-band receiver front-end.

Fig. 1.3 shows several different possible structures for concurrent dual-band receiver front-ends. The most intuitive and conventional way is to employ two separate antennas and receiver chains with each path only processing single frequency (either f_1 or f_2) as shown in Fig. 1.3(a). As the most bulky component in any transceivers even at mm-waves, the antenna can be designed to operate at both frequencies as shown in Figs. 1.3(b) and (c), which can reduce the system sizes. In order to split the received signal containing the two carrier frequencies onto each path, however, an additional building block such as diplexer must be included, which will cause degradation in gain and noise

figure (NF) due to its insertion loss. In order to fully exploit the advantages of the dual-band system, it is desirable to design all the constituent building blocks as shown in Fig. 1.3(d) while the linearity degradation issue compared to the single band circuits should be carefully treated in the design. The details on these issues will be addressed in the later chapters.

1.4 Dissertation Organization

This dissertation provides the thorough analysis and experimental results by designs, simulations, and measurements of several building blocks constituting a single-band (V-band) and concurrent dual-band (K- and V-band) transceiver front-ends. Additionally, the designs of analog baseband circuits such as active filter and baseband VGA for a wideband receiver are included. All the circuits operating at mm-waves are realized using HBT in SiGe BiCMOS process while the baseband circuits are designed using CMOS transistors.

Chapter II presents the design of a 60-GHz active pulse/OOK modulator, featuring the technique to enhance the off-state isolation by inclusion of the switched impedance cell. Based on a single-cascode stage, the modulator achieves improved off-state isolation without degrading the forward gain, resulting in very high on/off isolation. In Chapter III, a wideband V-band LNA is presented with an emphasis on power-efficient wideband design. The design features much higher gain-bandwidth product than a conventional gain-staggered wideband amplifier designs for a given dc power consumption. In other words, the proposed design method will require much less dc

power to achieve a certain gain level over a wide bandwidth than the conventional gain-staggered tuning method.

Chapter IV presents a concurrent K-/V-band LNA as the first constituent building blocks of the dual-band phased array receiver chain. The design features the simultaneous rejection of the critical intermodulation product / harmonics and dual-band input matching through Miller effect, which can save the chip area and possibly reduce the minimum noise figure by obviating at least one additional physical inductor at the input.

Chapter V deals with the design of a concurrent dual-band RF variable gain amplifier (VGA) operating at K- and V-band for the gain control of the dual-band phased array receiver front-end. Starting from a wideband design, the proposed RF VGA achieves the suppression of the two most significant IM products by replacing as many inductors in a wideband design as possible with transformer-coupled resonators. Moreover, a technique to reduce the phase variation in the course of gain tuning process has been applied because it is one of the most critical concerns in phase array systems.

Chapter VI concludes the dissertation and includes possible future works related to the research. Finally, the load-dependent impedance appearing at the input through Miller effect are summarized for several different special load conditions in Appendix A.

CHAPTER II

60-GHZ ACTIVE OOK/PULSE MODULATOR[1]

In this chapter, a 60-GHz active on-off-keying (OOK)/pulse modulator with a switched-impedance cell for enhanced ON/OFF isolation supporting up to 2.5-Gbps data rate (or 400-ps square pulse equivalently) is presented. Based on a single-stage cascode amplifier, the designed active OOK/pulse modulator achieves 36.5-dB OFF-state isolation and 11.5-dB ON-state forward gain, resulting in very high ON/OFF isolation of 48 dB by incorporating the switched-impedance cell. The designed modulator is realized in a 0.18-μ*m* SiGe BiCMOS process. It occupies 0.95 mm × 0.95 mm with all the test pads and 0.4 mm × 0.28 mm without the pads. It only consumes 4.5 mA at 1.8-V supply voltage (P_{DC} = 8.1 mW).

2.1 Introduction and Motivation

Increasing demand for high data rates for growing number of users and applications has pushed the operating frequencies to millimeter-wave region these days. Especially, the 60-GHz band has been getting much attention for its wide unlicensed spectrum (5-GHz in common worldwide), which implies that Gbps communication is possible even with very simple binary signaling. OOK modulation is one of the simplest

[1] Copyright 2015 IEEE. Reprinted, with permission from Sunhwan Jang and Cam Nguyen, "A 60 GHz 2.5 Gbps OOK Modulator with Data-Dependent Impedance Cell for Enhanced ON/OFF Isolation in 0.18 μm BiCMOS Process," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 4, Feb. 2015, pp. 244-246.

form of binary signaling scheme, which transmits a carrier signal only when bit "1" is being sent. While being spectrally inefficient, employing OOK modulation greatly reduces the system complexity and power consumption since no complex phase locking/recovery and frequency conversion circuitries are required. Recently, many works have been reported on the OOK modulators operating at millimeter-wave frequencies, mostly in the 60-GHz frequency band [3-10].

Since an OOK-modulated signal carries information only by means of signal amplitude, any signal transmission during OFF state can significantly degrade the signal-to-noise ratio (SNR) at the receiver side. The SNR can be enhanced by increasing the transmitter's output power [8], which, however, leads to more dc power consumption. Alternatively, the SNR can be increased by minimizing the leakage signal during OFF state while keeping the forward gain intact for the modulator, which effectively maximizes the ON/OFF isolation.

In this chapter, a 60-GHz active OOK/pulse modulator supporting Gbps data rate (or equivalently as narrow pulse width as 400 ps) with the enhanced ON/OFF isolation is presented. The designed modulator implements a data-dependent impedance cell to enhance the isolation ($S_{21,OFF}$) without sacrificing the maximum achievable data rate and the forward gain ($S_{21,ON}$) while consuming no additional dc-power, effectively resulting in enhanced ON/OFF isolation. In the following sections, circuit analysis and measured results are provided to verify the functionality of the proposed OOK/pulse modulator.

2.2 Circuit Design and Analysis

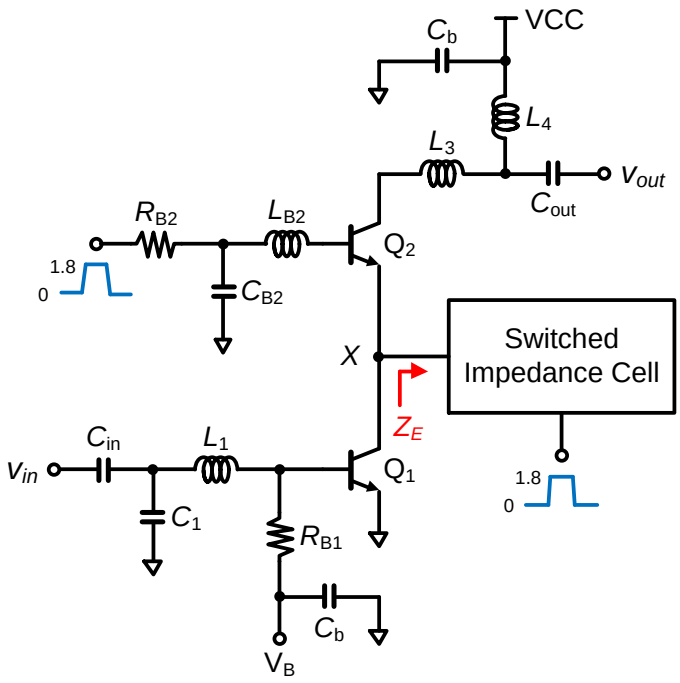


Fig. 2.1. Circuit schematic of the 60-GHz active OOK/pulse modulator.

Fig. 2.1 shows the circuit schematic of the proposed 60-GHz active OOK/pulse modulator, which is based on a single cascode amplifier stage, where the cascode device (Q_2) is turned ON and OFF according to the data sequence (i.e. 0 or 1.8 V). Data signal is applied to the base of Q_2 through R_{B2}, which should be large enough to prevent overshoot in the events of data transition and small enough to have small *RC* time-constant ($\tau = R_{B2}C_{B2}$) for high-speed data signal. Therefore, R_{B2} as well as C_{B2} should be chosen very carefully to supply properly shaped data signal to the base of Q2. A small inductor, L_{B2}, is connected at the base of Q_2 to increase the forward gain through the positive feedback mechanism as well as to provide an ac ground for the 60-GHz carrier signal by forming a series resonance with C_{B2}. The proposed switched-impedance cell is

connected at node *X* and its impedance (Z_E) at 60 GHz is designed to be high and low for ON and OFF states, respectively. The details about the switched-impedance cell will be discussed in the later part of the section.

The small-signal equivalent circuit of the proposed modulator is shown in Fig. 2.2. Note that the base-collector capacitors (C_{bc1} and C_{bc2}) are neglected for simplicity. Also, the base-emitter resistances ($r_{\pi 1}$ and $r_{\pi 2}$) can be neglected as they are much larger than the impedance of C_{be1} and C_{be2} at very high frequencies, and the emitter resistances (r_{e1} and r_{e2}) are excluded as they are irrelevant to the analysis for the proposed method.

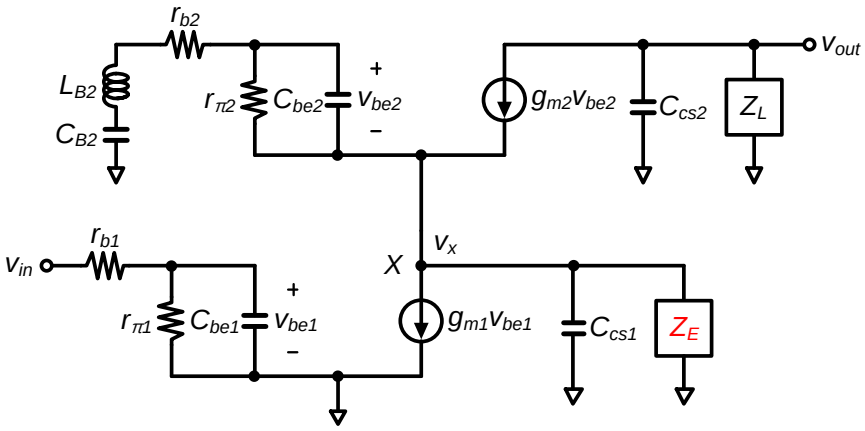


Fig. 2.2. Simplified small-signal equivalent circuit of the proposed modulator.

The overall voltage transfer function can be obtained by multiplying the transfer functions of the common-emitter and common-base stages as

$$\frac{v_{out}}{v_{in}} = \frac{v_x}{v_{in}} \cdot \frac{v_{out}}{v_x}. \tag{2.1}$$

For the common-emitter stage, the relationship between v_{in} and v_x can be found to be

$$\frac{v_x}{v_{in}} = -g_{m1} \cdot \left(\frac{1}{1 + j\omega C_{be1} r_{b1}} \right) \cdot \left(\frac{1}{j\omega C_{cs1}} \| Z_E \right) \tag{2.2}$$

where

$$v_x = -g_{m1} v_{\pi 1} \cdot \left(\frac{1}{j\omega C_{cs1}} \| Z_E \right) \tag{2.3}$$

and

$$v_{\pi 1} = \frac{1}{1 + j\omega C_{be1} r_{b1}} \cdot v_{in}. \tag{2.4}$$

The voltage transfer function for the common-base stage (v_{out}/v_x) can be written as

$$\frac{v_{out}}{v_x} = g_{m2} \cdot \frac{1}{\left(1 + \frac{C_{be2}}{C_{B2}} - \omega^2 L_{B2} C_{be2} + j\omega C_{be2} r_{b1} \right)} \cdot \left(\frac{1}{j\omega C_{cs2}} \| Z_L \right) \tag{2.5}$$

where

$$v_{out} = -g_{m2} v_{be2} \cdot \left(\frac{1}{j\omega C_{cs2}} \| Z_L \right) \tag{2.6}$$

and

$$v_{be2} = -\frac{1}{1 + \frac{C_{be2}}{C_{B2}} - \omega^2 L_{B2} C_{be2} + j\omega C_{be2} r_{b2}} \cdot v_x. \tag{2.7}$$

Then, by substituting (2.2) and (2.5) into (2.1), the overall voltage transfer function between the input and output can be found as

$$\frac{v_{out}}{v_{in}} = -\underbrace{\left(\frac{g_{m1}}{Y_E + j\omega C_{cs1}}\right)}_{Z_E \text{ dependent term}} \cdot \left(\frac{1}{1 + j\omega C_{be1} r_{b1}}\right) \cdot \frac{g_{m2}}{\left(1 + \frac{C_{be2}}{C_{B2}} - \omega^2 L_{B2} C_{be2} + j\omega C_{be2} r_{b2}\right)} \cdot \left(\frac{1}{j\omega C_{cs2}} \| Z_L\right) \tag{2.8}$$

where Y_E is the admittance looking into the switched-impedance cell (i.e. $1/Z_E$).

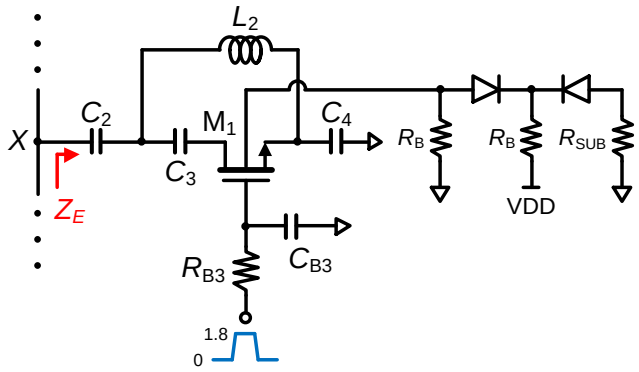
From (2.8), only the first term is dependent on Z_E. If Z_E exhibits relatively high impedance (or equivalently Y_E is close to zero) compared to the impedance of the parasitic capacitance associated at node X at the frequency of interest, it would have little impact on the forward gain. If Z_E becomes very small (i.e., $Y_E \rightarrow \infty$) at the frequency of interest, on the other hand, ideally no signal would appear at the output. That is, the ON/OFF isolation by employing the switched-impedance cell can be improved by finding the optimum solutions to

$$\begin{aligned} &\textit{min} && \left|Y_{E,ON} + j\omega C_{cs1}\right| \\ &\textit{subject to} && Y_{E,OFF} \rightarrow \infty \end{aligned} \tag{2.9}$$

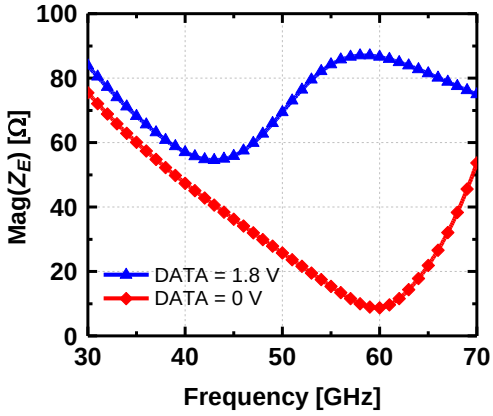
where $Y_{E,ON}$ and $Y_{E,OFF}$ are the admittances of the data-dependent impedance cell for ON and OFF states, respectively.

One of the optimum solutions to (2.9) can be implemented by adding a switched-impedance cell as shown in Fig. 2.3(a). The operation of the proposed impedance cell is explained through qualitative approaches, which are much simpler and more intuitive than complex and lengthy mathematics. When the data is ON (1.8 V), L_2 and C_3 with the series on-resistance of M_1 form a parallel resonance at 60 GHz, which is dominant over other series resonances. On the other hand, when the data is OFF (0 V), a series

resonance occurs at 60 GHz by C_2, L_2, and C_4, while the parallel resonance formed by L_2 and C_3 with the off-capacitor of M_1 is at far higher frequency than 60 GHz. As can be seen in Fig. 3(b), the magnitude of the input impedance of the switched-impedance cell (Z_E) is relatively high and very low at 60 GHz for ON and OFF states, respectively.



(a)



(b)

Fig. 2.3. (a) Switched-impedance cell with deep n-well NMOS transistor and (b) simulated magnitude of Z_E for both ON and OFF states.

These results imply that, by employing the proposed impedance cell, improvement in the ON/OFF isolation can be expected while keeping the degradation in

the forward gain negligible, which is verified by the experimental results in the following section. From the simulations, it has been confirmed that the modulator with the impedance cell achieves more than 10-dB improvement in the ON/OFF isolation with only 0.4-dB reduction in the forward gain as compared to that without the impedance cell, where this simulation results are not included here. The NMOS transistor (M_1) performing the switching function is buried in the deep n-well layer to increase the isolation as shown in Fig. 2.4. The very large resistor (R_B) is connected to the body terminal of the transistor, which makes the body floating. The n-well layer is tied to the most positive voltage in the circuit through a very large resistor (R_B) to prevent the latch-up issue.

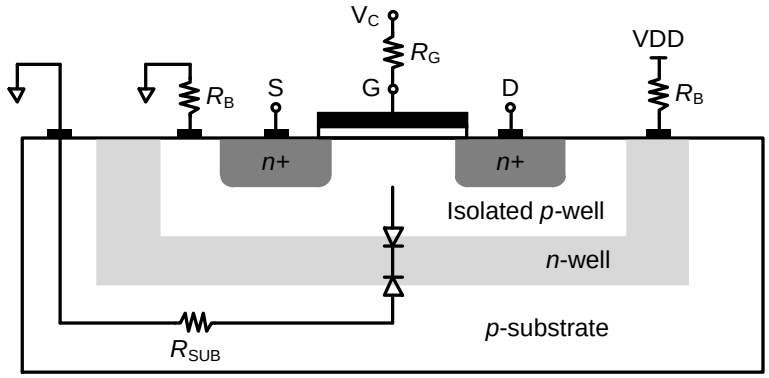


Fig. 2.4. Cross-section of a deep n-well transistor with floating body.

The 60-GHz active OOK/pulse modulator was fabricated in TowerJazz 0.18-μm SiGe BiCMOS process [11] and its die microphotograph is shown in Fig. 2.5. The input and output RF GSG pads are located in the left and right edges of the chip. The dc pad (PGPPGP) at the top supplies the dc bias voltages. The bottom dc pad is designed for supplying the dc voltages (0 or 1.8 V) through the dc pad for the *S*-parameters and P_{1dB}

measurements as well as the data (or pulse) signal for the transient measurements. The chip size measures 0.95 mm × 0.95 mm including all the RF and dc pads and only 0.4 mm × 0.28 mm without the pads.

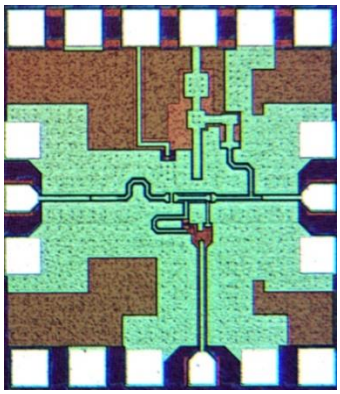


Fig. 2.5. Chip microphotograph of the 60-GHz active OOK/pulse modulator.

2.3 Measured Results and Discussion

All the measurements were performed using the Rhode & Schwarz vector network analyzer (ZVA67) and by on-chip probing. Fig. 2.6 plots the simulated and measured transmissions (S_{21}) both for ON and OFF states. The forward gain ($S_{21,ON}$) is measured to be11.5 dB while the isolation ($S_{21,OFF}$) is 36.5 dB, resulting in 48-dB ON/OFF isolation at 60 GHz. The measured OFF-state isolation is about 10-dB lower than the simulated one, which could be resulted from the fact that the measurable limit of the network analyzer for isolation is less than 50 dB at this frequency range.

Fig. 2.7 plots the simulated and measured input (S_{11}) and output (S_{22}) return losses for ON state. Both the measured $S_{11,ON}$ and $S_{22,ON}$ are well above 10 dB, and show good agreements with the simulated results. The return losses for OFF state are also

plotted in Fig. 2.8. The measured $S_{11,OFF}$ is still the reasonable value of – 9 dB while $S_{22,OFF}$ is still maintained below -10 dB at 60 GHz.

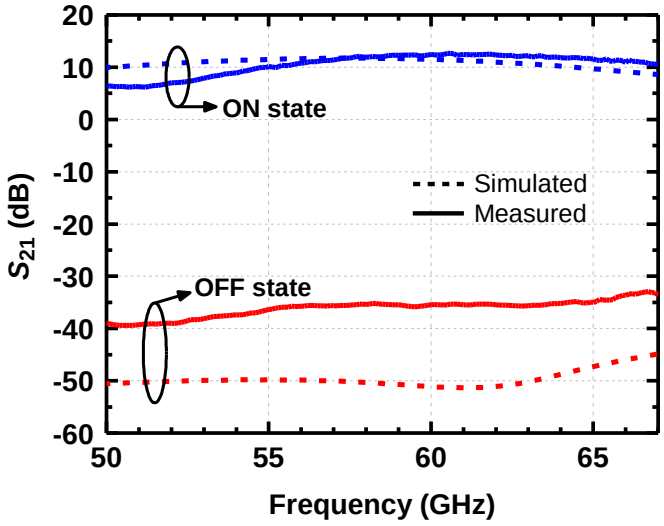
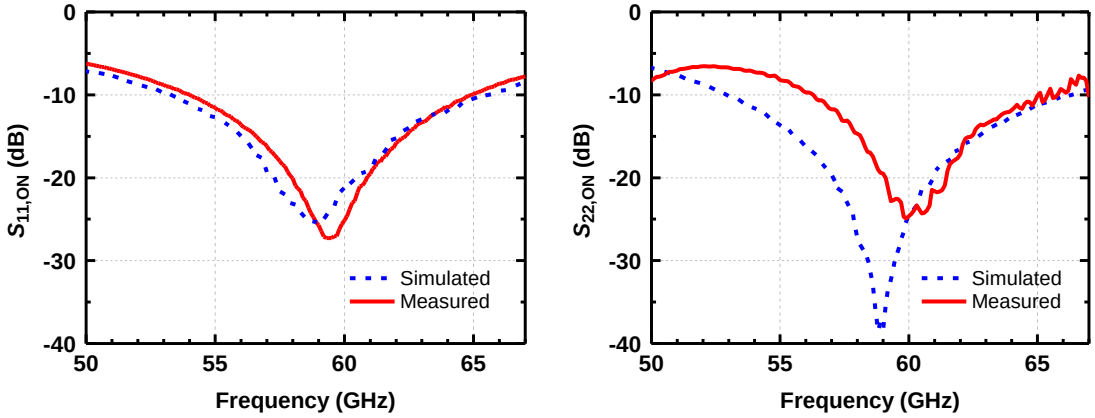
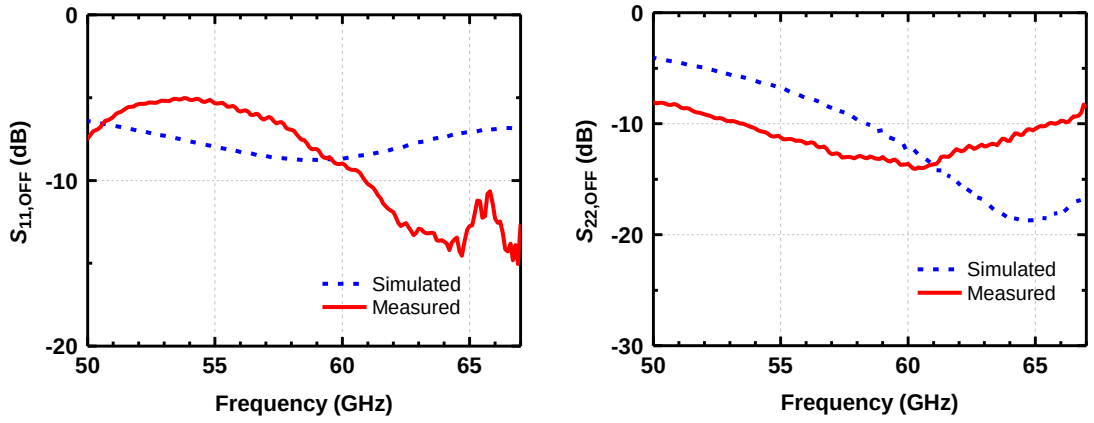


Fig. 2.6. Simulated and measured forward gains ($S_{21,ON}$) and isolations ($S_{21,OFF}$).



(a) (b)

Fig. 2.7. Simulated and measured (a) input (S_{11}) and (b) output (S_{22}) return losses for ON state.



(a) (b)

Fig. 2.8. Simulated and measured (a) input (S_{11}) and (b) output (S_{22}) return losses for OFF state.

Fig. 2.9 shows the measured forward gain and output power versus input power. Consuming only 4.5-mA dc current at 1.8-V supply voltage, the proposed modulator has decent input and output P_{1dB} of -12.5 dBm and -1.5 dBm, respectively. Having over 10-dB gain with decent output P_{1dB}, the designed modulator can serve as a drive amplifier for a power amplifier when it is to be integrated in the transmitter.

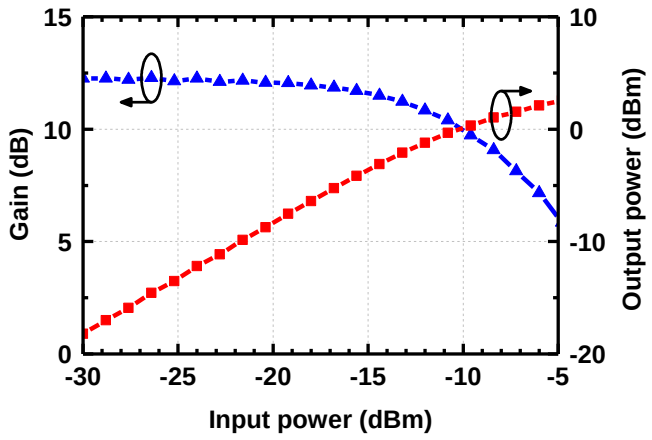


Fig. 2.9. Measured forward gain and output power versus input power.

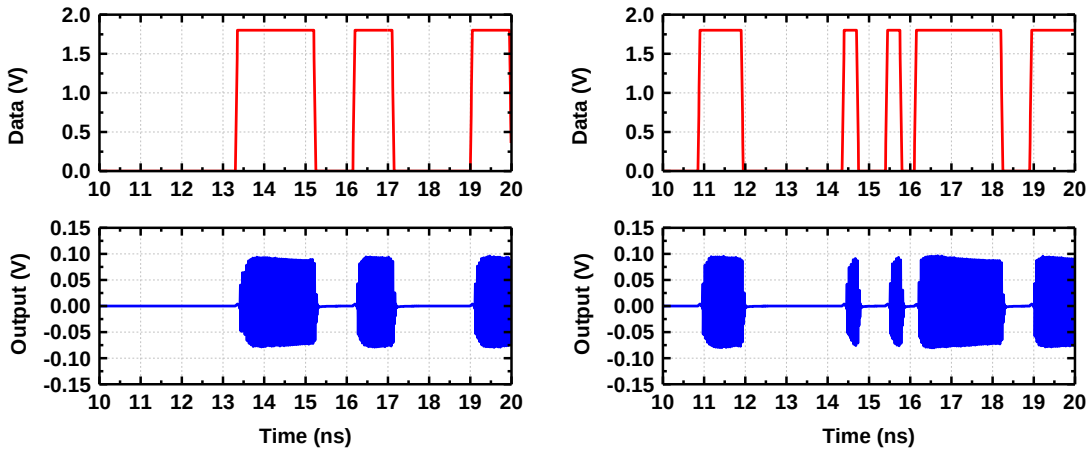


Fig. 2.10. Simulated transient output with random bit sequence input with data rate of (a) 1 Gbps and (b) 2.5 Gbps.

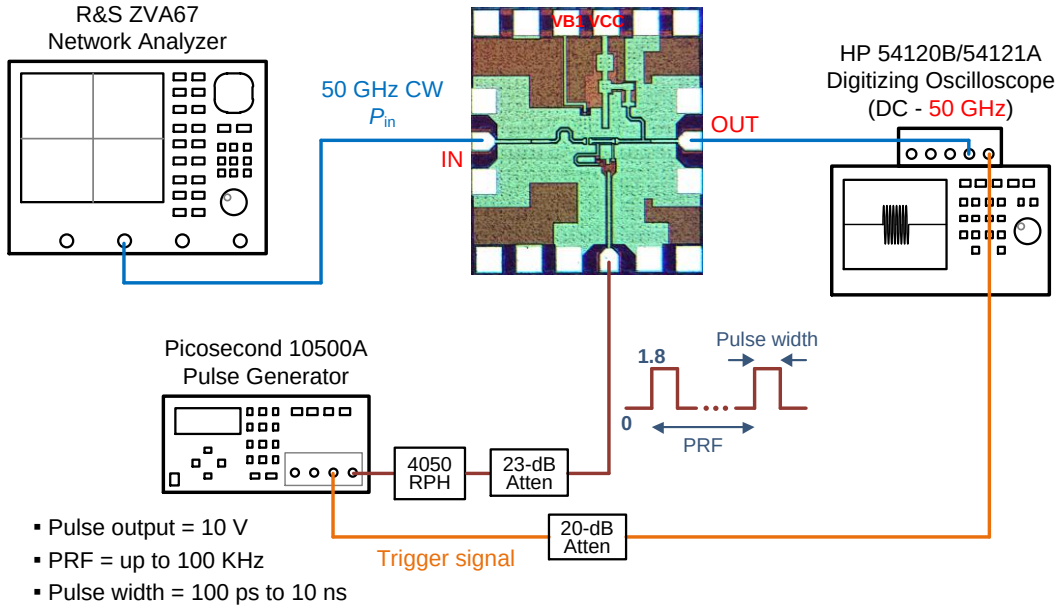
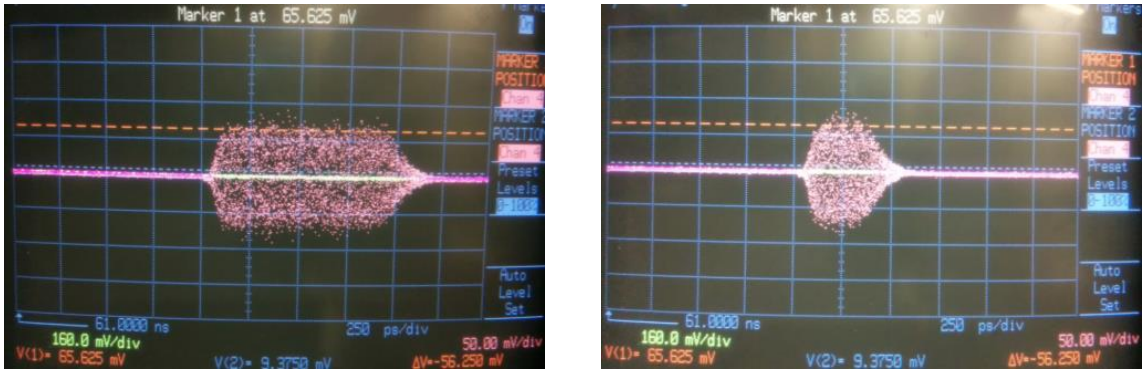


Fig. 2.11. Transient measurement setup.

The transient simulations are performed by applying a random bit sequence as the data input. Both the rise and fall times of the data bits are set to 50 ps, rather than 0

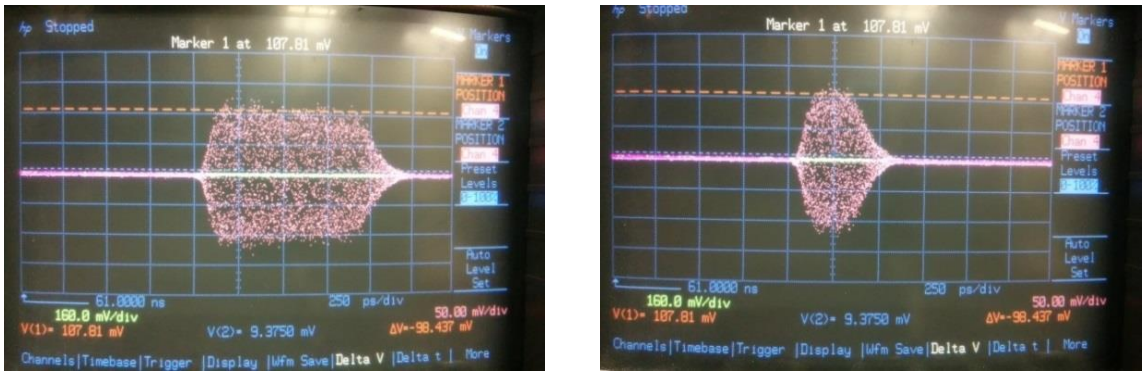
ps, for more realistic simulations. The transient output waveforms with 1-Gbps and 2.5-Gbps data rates are plotted in Figs. 2.10(a) and (b), respectively, which confirm the proper operation of the proposed modulator in the time domain.

Fig. 2.11 shows the setup for the time-domain measurements. The network analyzer (R&S ZVA67) provides the continuous wave (CW) input, of which power calibration is performed in advance. With the data signal supplied by the pulse generator (Picosecond 10500A) applied, the output transient waveforms are captured by the digitizing oscilloscope (HP 54124T). A 50-GHz continuous wave, instead of 60-GHz, is used as an input signal due to the measurable limit of the oscilloscope (only up to 50 GHz). Also, single pulses with the pulse width narrower than 1 ns, instead of periodic pulse trains or random data sequences, were applied as data input due to the limited availability of the equipment for the data signal or pulse generation.



(a) (b)

Fig. 2.12. Transient output waveforms with CW input of -15 dBm at 50 GHz and pulse width of (a) 1-ns and (b) 400-ps.



(a) (b)

Fig. 2.13. Transient output waveforms with CW input of -10 dBm at 50 GHz and pulse width of (a) 1-ns and (b) 400-ps.

Fig. 2.12 shows the measured output waveforms with the 50-GHz CW input of -15 dBm. When a 1-ns square pulse is applied as shown in Fig. 2.12(a), it clearly shows that the peak output level (V_P = 65.6 mV) is well maintained for the pulse duration, from which the rising and falling times can be estimated to be 110 ps and 200 ps, respectively. Fig. 2.12(b) shows the output waveform with a 400-ps square pulse applied. As can be seen, the output waveform reaches the maximum output level before the falling starts, ensuring that the modulator can handle 2.5-Gbps data rate or equivalently 400-ps pulse width. Fig. 2.13 captures the measured output waveforms with the CW input power of -10 dBm. Compared to the results in Fig. 2.12, the transient behaviors are almost identical except for the higher peak output level (V_P = 107.8 mV), which is due to the increased CW input power. From the successful measurements with 50-GHz CW input, it is convincing that the modulator will operate at 60 GHz as well. Table I compares the proposed modulator with the recently reported OOK modulators operating at V-band. To

the best knowledge, the proposed modulator achieves the highest measured ON/OFF isolation and gain among the reported ones.

Table 2.1 Comparison with the reported mm-wave OOK/pulse modulators

Ref.	Technology	Data Rate [Gbps]	Gain [dB]	On/Off Isolation [dB]	P_{DC} [mW]
[3]	0.25-μm BiCMOS	20	-1.1	36	54.6
[4]	90-nm CMOS	2	9.9	28.4	14.4
[5]	90-nm CMOS	1.5	-2.5	19.2	3.6
[6]	90-nm CMOS	8	-6.6	26.6	0
[7]	90-nm CMOS	6	N/A	30	0
[8]	65-nm CMOS	16	1	30.5	5
[9]	90-nm CMOS	5.5	0	50*	6
This	0.18-μm BiCMOS	2.5	11.5	48	8.1

***from simulation**

2.4 Summary

A 60-GHz 2.5-Gbps pulse/OOK modulator supporting up to 2.5-Gbps data rate or as narrow pulse width as 400 ps with enhanced ON/OFF isolation has been designed in a 0.18-μm BiCMOS process. With an aid of the proposed switched-impedance cell,

the designed OOK/pulse modulator allows negligible signal transmission during OFF state ($S_{21,OFF}$ = -36.5 dB) while providing a decent amount of gain during ON state ($S_{21,ON}$ = 11.5 dB), which results in very high ON/OFF isolation of 48 dB, with low dc power consumption of 8.1 mW (4.5 mA at 1.8-V supply). Combining with Gbps data rate / narrow pulse width support, the proposed pulse/OOK modulator can be well-suited for 60-GHz applications such as a low-power Gbps point-to-point link and pulsed radar system within a short range.

CHAPTER III

WIDEBAND V-BAND LOW-NOISE AMPLIFIER[2]

This chapter introduces a design of high-gain power-efficient wideband low noise amplifier (LNA) operating at V-band, realized in 0.18-μm SiGe BiCMOS process. An effective wideband gain shaping method with gain enhancement under low power consumption is employed, where the 1st and 2nd inter-stage matching (ISM) network are designed for better conjugate matching around the lower and upper 3-dB cutoff frequency ends, respectively, without giving up the gains at the opposite frequency ends for each ISM network. The developed LNA achieves the peak measured gain of 32.5 dB at 61 GHz and over 29.5 dB gain across the 3-dB bandwidth from 43 to 67 GHz while consuming only 11.7 mW at 1.8-V supply voltage. The measured average noise figure and group delay variation are 6 dB and less than 28.3 ps over the entire bandwidth, respectively.

3.1 Introduction and Objectives

Millimeter-waves (mm-waves) are very attractive for various applications such as high-data-rate communications and fine-resolution remote sensing. The V-band (40-75 GHz), especially, has received significant attention due to its unique properties of

[2] Copyright 2016 IEEE. Reprinted, with permission from Sunhwan Jang and Cam Nguyen, "A High-Gain Power-Efficient Wideband V-Band LNA in 0.18-μm SiGe BiCMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 4, Apr. 2016, pp. 276-278

strong signal absorption in the atmosphere at 60 GHz, making it ideal for secure satellite crosslinks and short-range communications with frequency-reuse capability, where the unlicensed frequency range of 57-64 GHz is one of the most well-known mm-wave spectrums available for such applications. Various works on 60-GHz low-noise amplifiers (LNAs) have been reported in the past decade. Most of these LNAs were designed for the unlicensed 57-64 GHz spectrum [12-14] and are not suitable for wider bandwidth applications. The most conventional way for wideband amplifier design is the gain-staggered tuning [15-17]. This technique, however, generally requires large dc power in order to achieve sufficiently high gain. The bandpass distributed amplifier in [18] can achieve very wide bandwidth (BW) up to a few tens of GHz but requires a significant amount of power to obtain a gain even less than 10 dB. The transformer-based design reported in [19] can also enlarge the bandwidth with reduced power and chip size, but the design is more complex.

This chapter presents a high-gain power-efficient wideband V-band LNA, which exploits a wideband gain-shaping method different from those employing conventional staggered tuning method. The designed LNA achieves an unprecedented high gain of 29.5 dB over a wide bandwidth from 43 to 67 GHz with only 11.7 mW dc power consumption.

3.2 Circuit Design and Analysis

Fig. 3.1 shows the circuit schematic of the designed three-stage V-band LNA realized in TowerJazz 0.18-μm SiGe BiCMOS process [11]. The input transistor of the

1st stage (Q1) has one emitter finger (w = 0.13μm and l = 4 μm), two base fingers, and two collector fingers (CBEBC) considering the tradeoff between noise characteristic and high frequency gain performance of the transistor [20], while all other transistors (Q2-Q6) have identical size to Q1. Inductive degeneration is employed for simultaneous input and noise matching, where the degeneration inductor is a bit larger (37 pH) than the value for optimum noise figure (29 pH) to broaden the input matching. To complete the input matching, very small shunt capacitance (20 fF) is required, which cannot be realized with the metal-insulator-metal (MIM) capacitor provided in the process design kit (PDK).

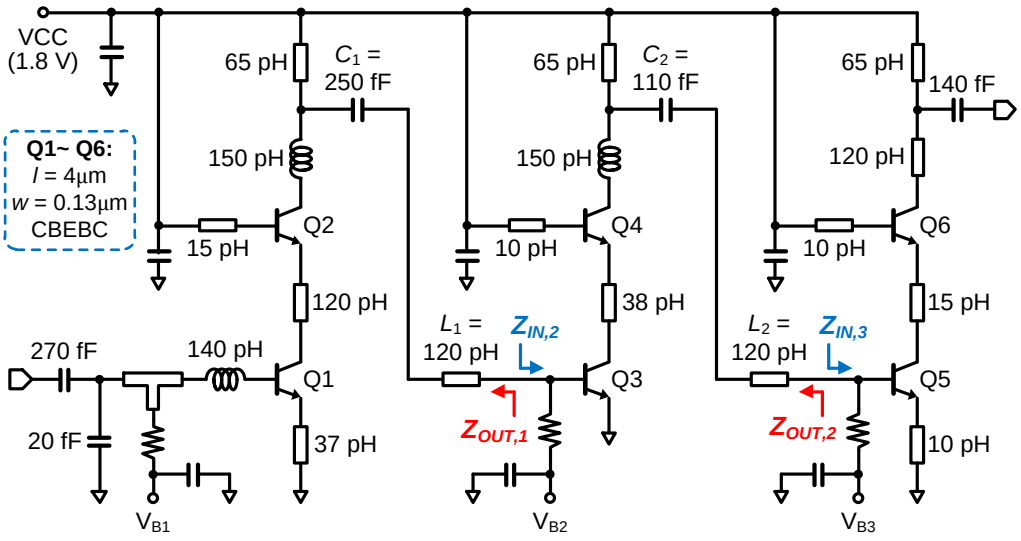


Fig. 3.1. Circuit schematic of the developed wideband V-band LNA.

The required capacitance is realized by an inter-digital capacitor through EM-simulations as shown in Fig. 3.2. By placing the fingers connected to the signal line and the ground plane alternately, the capacitance is formed by the lateral fluxes created between the two adjacent fingers. The capacitance can be increased by increasing the

number of fingers, but at the cost of increased parasitic series inductance and resistance. For each finger, metal 4 to metal 6 (top metal) are stacked, which increases the capacitance density per unit area and hence the overall capacitance for a given area.

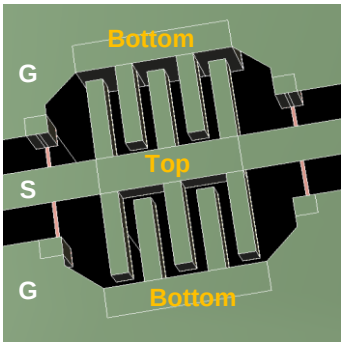


Fig. 3.2. 3-D view of a 20-fF inter-digital shunt capacitor for input matching network.

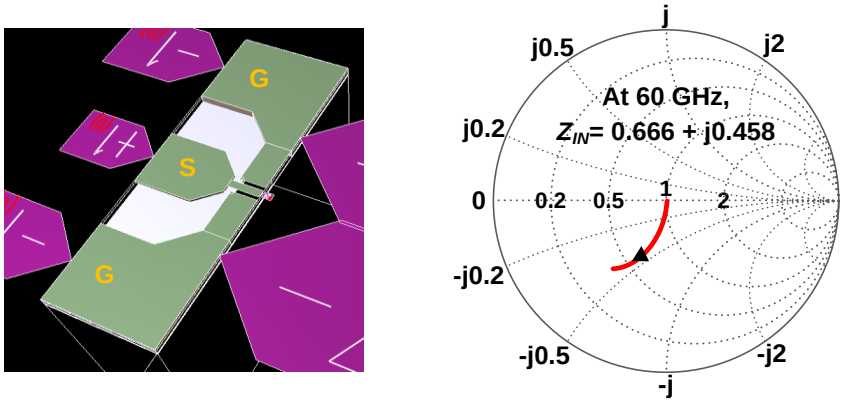
The RF GSG (ground-signal-ground) pad is especially designed to have nearly zero parasitic reactive elements (i.e., inductance and capacitance), which is explained in details as follows. In order to visualize the benefits of the pad structure employed in this LNA design, three different pad structures including the proposed pad design are simulated using Mentor Graphics IE3D 2.5-D EM simulator [21] from dc to 100 GHz as shown in Fig. 3.3.

Generally, the two ground pads are connected using the lowermost metal layer (metal 1) passing under the signal pad (topmost metal layer, metal 6) as shown in Fig. 3.3(a) to keep the potentials of the two ground pads the same. Note that the center-to-center pitch between the signal pad to one of the ground pads is 100 μm. However, this pad structure introduces significant shunt capacitance from the signal pad to ground pad. The input impedance of the RF pad (Z_{IN}) is found to be 33.3 - j22.9 Ω at 60 GHz as

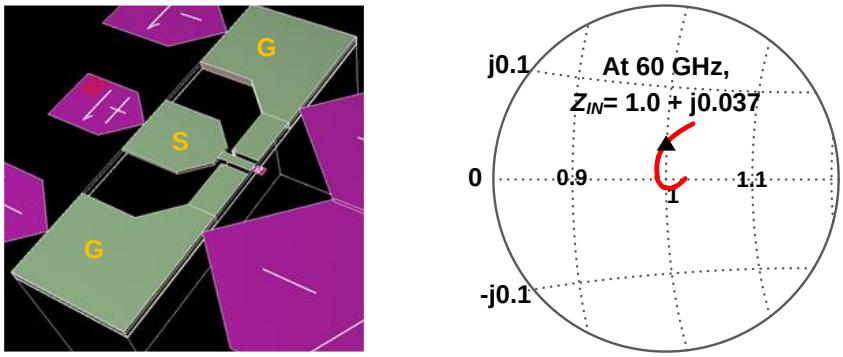
marked on the Smith Chart. Taking the reciprocal of Z_{IN}, the input admittance (Y_{IN}) is $0.02 + j0.014\ \Omega^{-1}$, which can be represented as the parallel combination of 50-Ω resistor and 37-fF capacitor at 60 GHz. Therefore, the input matching network of LNA should be designed by including the large parasitic shunt capacitance (37 fF) of the input pad. In other words, the input matching network must be reconfigured when the input pad is removed and the input of LNA is to be connected to any 50-Ω components or systems.

The parasitic shunt capacitance appearing for the pad structure in Fig. 3.3(a) can be eliminated by removing the connection through the lowermost metal between the two ground pads passing under the signal pad as shown in Fig. 3.3(b). The simulated Z_{IN} is $50 + j1.85\ \Omega$ at 60 GHz, which can be represented as the series connection of 50-Ω resistor and 5-pH inductor at 60 GHz. While no parasitic shunt capacitance appears as expected, the series inductance of 5-pH at 60 GHz can also lead to the shift in the resonant frequency of the input matching.

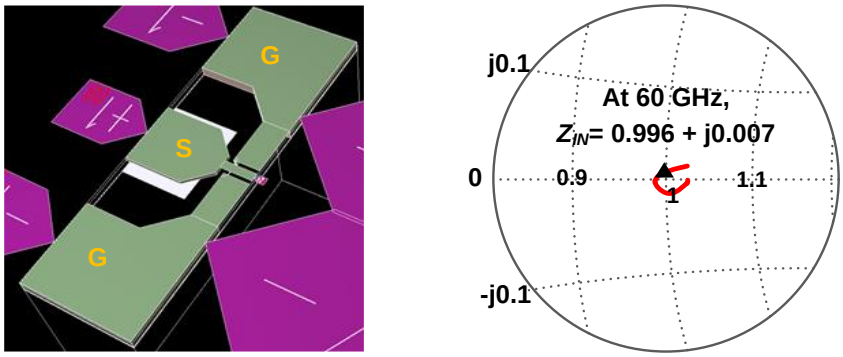
In order to remove the parasitic series inductance as well as the shunt capacitance, the pad structure shown in Fig. 3.3(b) can be modified by placing the lowermost metal piece floating under the signal pad as shown in Fig. 3.3(c). The EM-simulated input impedance of the pad is plotted on Smith Chart. At 60 GHz, $Z_{IN} = 49.8 + j0.35\ \Omega$ at 60 GHz and the corresponding parasitic series inductance is only 0.9 pH while technically no parasitic shunt capacitance is present. The parasitic-free input RF pad is advantageous for on- or off-chip integration with a 50-Ω based antenna or other components such as T/R switches, circulator, etc. because no adjustment in the LNA's input matching is necessary after the removal of the pad.



(a)



(b)



(c)

Fig. 3.3. Three different RF GSG pad structures and their EM-simulated input impedances from dc to 100 GHz on Smith Chart: (a) GSG pad with two ground pads connected using the lowermost metal, (b) GSG pad without connection between two ground pads, and (c) GSG pad with floating the lowermost metal piece under signal pad.

For a power-efficient wideband design, a *T*-type inter-stage matching (ISM) in [22] is adopted. The ISM method, however, selects the series capacitance in the ISM network for the best gain flatness, making the gain response of the LNA sensitive to a variation of the series capacitance, which leads to reduction in the bandwidth. To achieve enhanced and wideband gain response under low power consumption, a wideband gain shaping method based on two ISM networks in a three-stage design is employed, which also alleviates the sensitivity on capacitance variation as will be demonstrated later in this section. This method exploits the combined effect of the gain peaking at lower (f_{low}) and toward upper (f_{high}) 3-dB cutoff frequencies by choosing larger C_1 in the 1st ISM and smaller C_2 in the 2nd ISM than the optimum capacitance for the best gain flatness. The wideband gain shaping method results in very high gain-bandwidth product with very low power consumption for the LNA as will be seen later in this section.

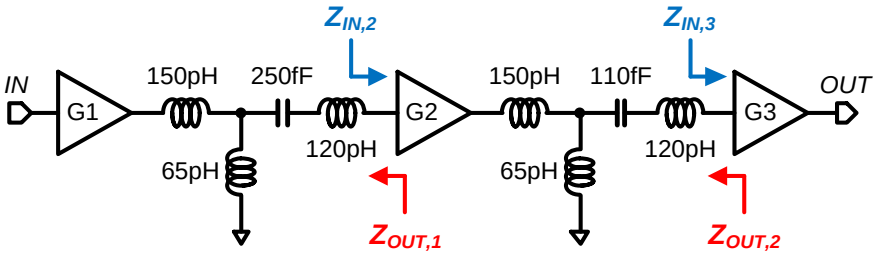


Fig. 3.4. Simplified schematic of the designed LNA for ISM analysis.

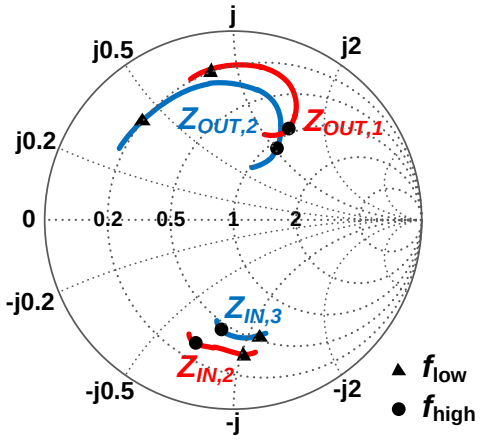
For better illustration, the simplified schematic only including the two ISM networks and the component values is shown in Fig. 3.4. In the 1st ISM network (between G1 and G2), the series connection of large capacitance (C_1 = 250 fF) and large

inductance (L_1 = 120 pH) is employed, which has a series resonance at 29 GHz. It implies that series L_1-C_1 behaves as an inductor over the frequencies of interest (40 to 70 GHz). It makes $Z_{OUT,1}$ to be located much closer to the conjugate of $Z_{IN,2}$ ($Z^*_{IN,2}$) around f_{low} without making the distance between $Z_{OUT,1}$ and $Z^*_{IN,2}$ around f_{high} far away (see Fig. 3.5(a)). Therefore, the 1st ISM gives gain peaking around f_{low} while the matching around f_{high} is still maintained. The matching performance can be illustrated by the mismatch factor for the N^{th} ISM ($M_{ISM,N}$) network defined as [23]

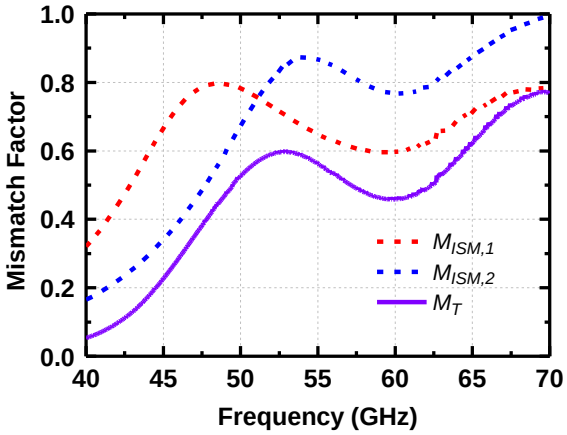
$$M_{ISM,N} = \frac{4R_{OUT,N}R_{IN,N+1}}{\left|Z_{OUT,N} + Z_{IN,N+1}\right|} \tag{3.1}$$

where N = 1 and 2. Note that $M_{ISM,N}$ = 1 for perfect conjugate matching between the N^{th} output and $(N+1)^{th}$ input. As can be seen in Fig. 3.5(b), $M_{ISM,1}$ peaks around f_{low} and is maintained above 0.6 over the bandwidth of interest.

On the other hand, the 2nd ISM network employs the series connection of small capacitance (C_2 = 110 fF) and large inductance (L_2 = 120 pH), which resonates at 44 GHz. It hence behaves as a capacitor below 44 GHz while acting as an inductor above 44 GHz. Therefore, $Z_{OUT,2}$ above 44 GHz tends to move closer toward the conjugate of $Z_{IN,3}$ ($Z^*_{IN,3}$) while $Z_{OUT,2}$ below 44 GHz becomes more distant from $Z^*_{IN,3}$ as can be seen in Fig. 3.5(a). As a result, the 2nd stage gain becomes high toward f_{high} while rolling off slowly toward f_{low}, which is illustrated by $M_{ISM,2}$ in Fig. 3.5(b).



(a)

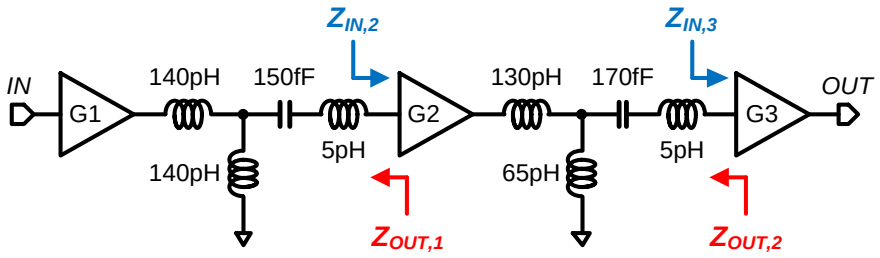


(b)

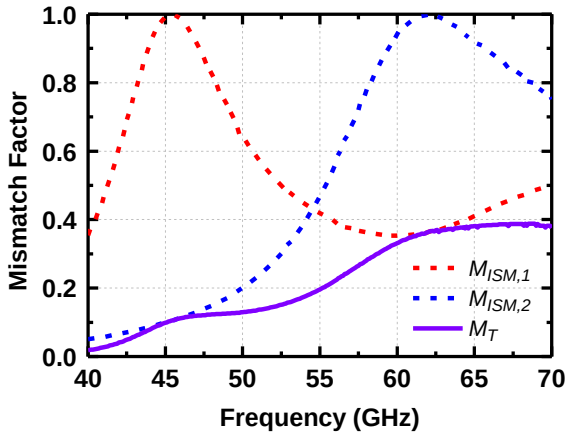
Fig. 3.5. (a) $Z_{OUT,1}$ and $Z_{IN,2}$ for the 1st ISM and $Z_{OUT,2}$ and $Z_{IN,3}$ for the 2nd ISM, and (b) the mismatch factors for each ISM and their product.

The combined effect of the two ISM networks can be visualized by the product of the two mismatch factors ($M_T = M_{ISM,1} \times M_{ISM,2}$) as plotted in Fig. 3.5(b). With the 3rd stage having parallel resonance around 60 GHz, a flat and enhanced gain response can be achieved over a wide bandwidth. To illustrate the gain enhancement over the conventional method, a 3-stage stagger tuned wideband amplifier employing

conventional *T*-type ISM networks is designed based on the same gain cells used in Fig. 3.1, as shown in Fig. 3.6(a), with the 1st and 2nd ISM networks having parallel resonances at 45 and 63 GHz, respectively. The simulated mismatch factors plotted in Fig. 3.6(b) shows M_T is less than 0.4 over the bandwidth of interest, which is significantly smaller than M_T of the proposed design shown in Fig. 3.5(b). Therefore, it can be concluded that the proposed method consumes less dc power for the same gain level or achieves much higher gain for the same dc power.



(a)



(b)

Fig. 3.6. (a) 3-stage wideband amplifier by conventional staggered tuning and (b) mismatch factors of the 1st and 2nd inter-stage matching networks.

Fig. 3.7 plots the gain responses (S_{21}) of the designed LNA when the capacitances (C_1 and C_2) in the two ISM networks are varied. As both C_1 and C_2 are decreased by 20% from the original values, the gain around f_{low} is increased by 0.7 dB while it stays the same around f_{high}, which results in a bandwidth reduction of 1.1-GHz. When the capacitances are increased by 20%, on the other hand, the gain around f_{low} is reduced by 0.5 dB and the bandwidth is increased only by 300-MHz. Therefore, the proposed wideband gain shaping method preserves the gain and bandwidth well over the course of capacitance variations.

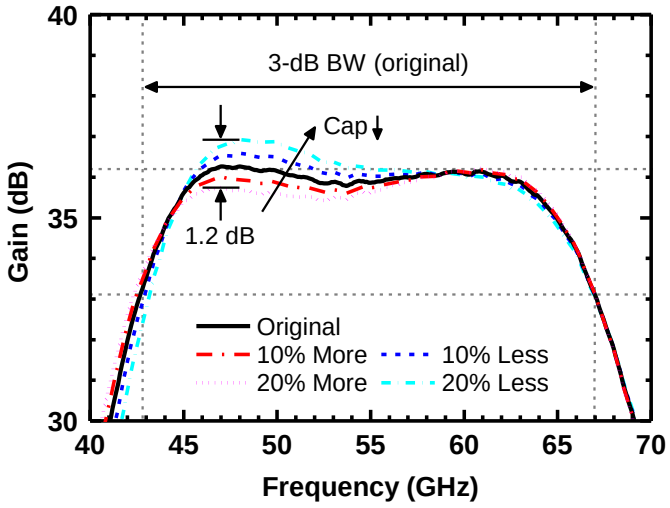


Fig. 3.7. Simulated gain responses according to capacitance variation in the two ISM networks.

All the interconnections and inductors are realized using coplanar waveguide (CPW) transmission line, while the spiral inductors are chosen for inductance larger than 140 pH considering layout size and series loss. All the passive elements including RF pads, except MIM capacitors in the process design kit, are simulated using IE3D EM

simulator [13]. The chip microphotograph of the fabricated V-band LNA is shown in Fig. 3.8. The total chip area is 0.94 mm × 0.94 mm while the core area is 0.65 mm × 0.6 mm. It only consumes 6.5 mA dc current with 1.8-V supply voltage (P_{DC} = 11.7 mW).

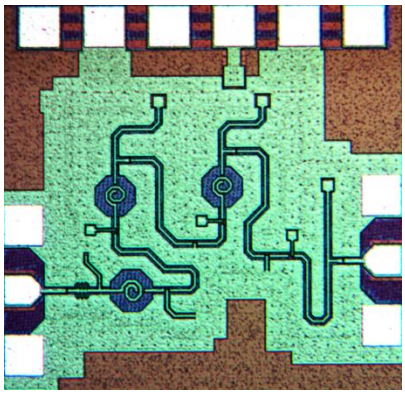


Fig. 3.8. Chip microphotograph of the designed wideband V-band LNA.

3.3 Experimental Results and Discussion

All the measurements including noise figure were performed by on-chip probing using a Rohde & Schwarz ZVA67 network analyzer. Fig. 3.9 shows the simulated and measured forward gain (S_{21}). Over the wide bandwidth from 43 to 67 GHz, the measured S_{21} is maintained above 29.5 dB with the peak measured S_{21} of 32.5 dB at 61 GHz. The average difference between the simulated and measured S_{21} is 4 dB even though all the bias voltages during the measurements are set to the same values used in the simulations, which is likely due to the overly optimistic modeling of the current gain of the HBTs. The input (S_{11}) and output (S_{22}) return losses are plotted in Fig. 3.10 and Fig. 3.11, respectively. With the quite good agreements between the simulations and measurements, the measured S_{11} and S_{22} are kept below -10 dB from 45 to 65 GHz and 52.5 to 61 GHz,

respectively. The measured reverse isolation (S_{12}) is maintained below -42 dB for all the frequencies as shown in Fig. 3.12.

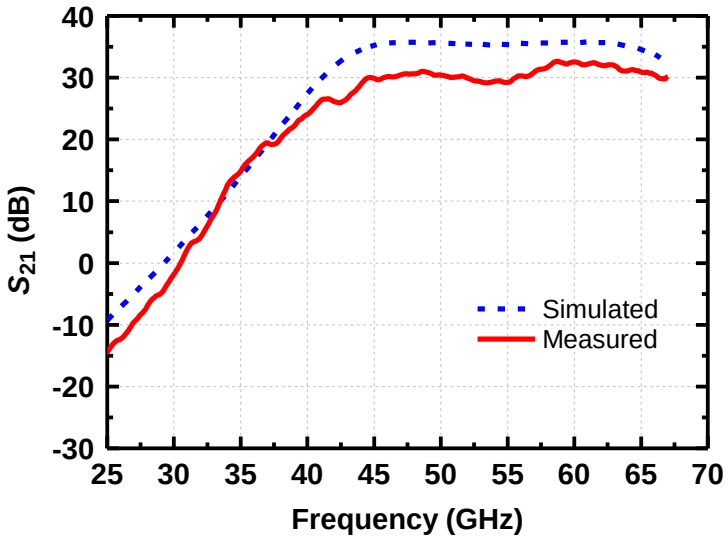


Fig. 3.9. Simulated and measured forward gain (S_{21}).

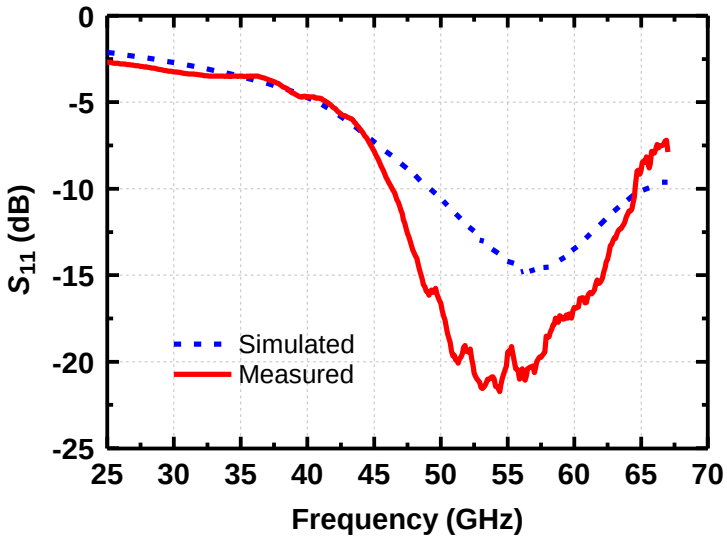


Fig. 3.10. Simulated and measured input return loss (S_{11}).

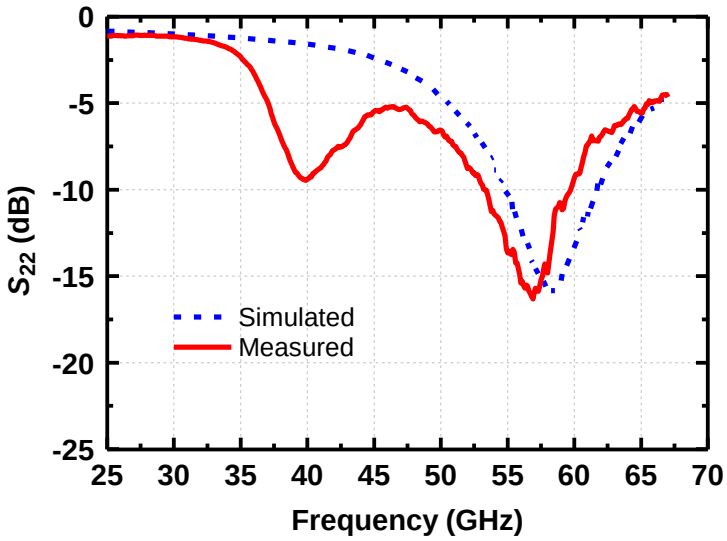


Fig. 3.11. Simulated and measured output return loss (S_{22}).

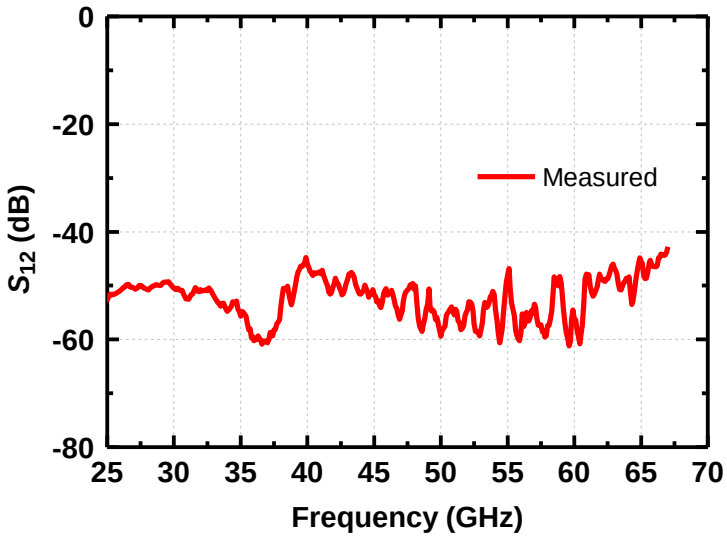


Fig. 3.12. Simulated and measured reverse isolation (S_{12}).

The simulated and measured noise figure (NF) are plotted over the 3-dB bandwidth as shown in Fig. 3.13, where the measurements were performed using the network analyzer having built-in NF measurement capability. The measured NF ranges

between 5.6 and 6.4 dB, showing at most 1-dB difference from the simulated values and giving the average NF of 6 dB. Group-delay variation is another important metric, especially in the wideband or broadband circuits, as a large group-delay variation within the bandwidth can result in poor signal fidelity, inter-symbol interference (ISI), etc. The group delay is defined as the rate of change in the transmission phase with respect to the frequency and expressed as

$$\tau_g = -\frac{\partial \phi\left(S_{21}(\omega)\right)}{\partial \omega} \tag{3.2}$$

where S_{21} represents the transmission between the input port 1 and output port 2. Fig. 3.14 plots the measured group-delay and the measured group-delay variation is kept less than 28.3 ps within the entire bandwidth, which is less than or comparable to those reported in the previously published wideband amplifiers operating at V-band.

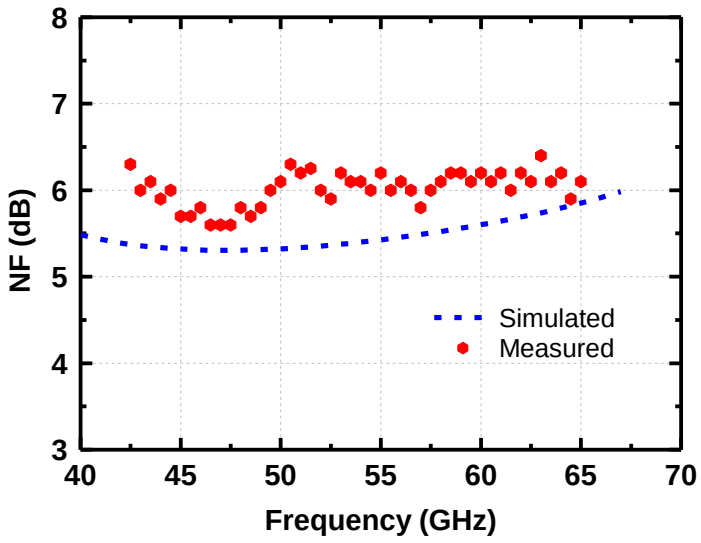


Fig. 3.13. Simulated and measured noise figure within 3-dB bandwidth.

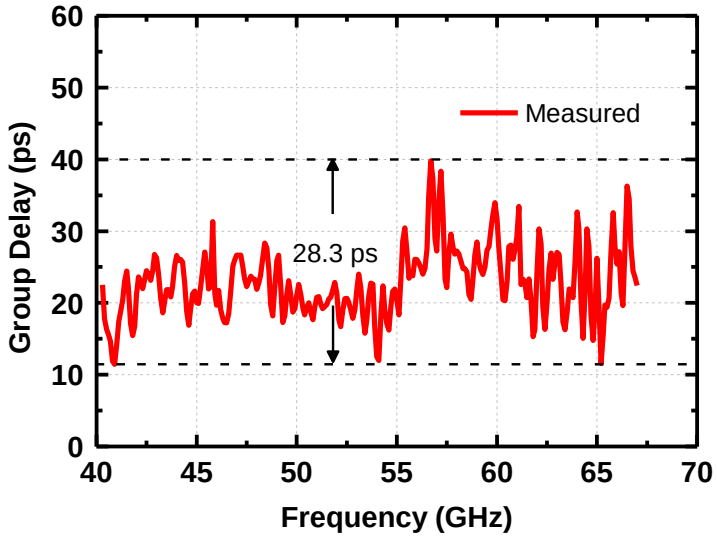


Fig. 3.14. Measured group delay within 3-dB bandwidth.

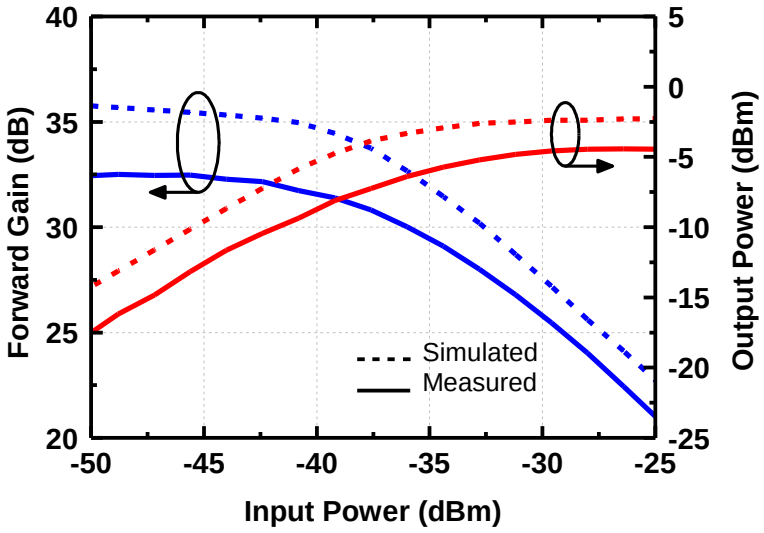


Fig. 3.15. Simulated and measured forward gain and output power versus input power at 61 GHz.

The measured input and output 1-dB compression points (P_{1dB}) at 61 GHz are measured to be -38 and -6.5 dBm, respectively, as shown in Fig. 3.15. The linearity

performance is degraded due to the high gain under very low dc power consumption. Table I provides a comparison with the recently reported silicon-based V-band LNAs having wide bandwidth. Due to the proposed power-efficient wideband gain shaping technique, the developed LNA achieves the highest gain-bandwidth product under the lowest power consumption.

Table 3.1 Comparison with other reported V-band LNAs

Ref.	Technology	BW [GHz]	Gain [dB]	NF* [dB]	IP_{1dB}/OP_{1dB} [dBm]	P_{DC} [mW]
[15]	65-nm CMOS	17 (51-68)	24	5.8	-22.5/0.5**	33.6
[16]	65-nm CMOS	23 (50-73)	17.5	3.7	-19.8/-3.3**	24
[17]	90-nm CMOS	23 (52-75)	14	6	N/A	32
[18]	40-nm CMOS	30 (24-54)	7	5	-5/1	34
[19]	90-nm CMOS	17 (46-63)	17	6.2	-17/-1	19.2
[22]	0.25-μm BiCMOS	30 (47-77)	22.5	6.8	-17/4.5***	52
This	**0.18-μm BiCMOS**	**24 (43-67)**	**32.5**	**6**	**-38/-6.5**	**11.7**

*average noise figure (measured) over BW **estimated ***simulated

3.4 Summary

A low-power-dissipation V-band LNA with high gain over wide BW implemented in 0.18-μm SiGe BiCMOS process is presented in this chapter. Along with the decent NF and small group-delay variation, the developed LNA can be well suited for the first amplification stage in wideband receiver front-ends for V-band applications such as high-speed data transmission, fine-resolution radar sensing, and so on.

CHAPTER IV

CONCURRENT K-/V-BAND LOW-NOISE AMPLIFIER

This chapter presents a concurrent K-/V-band low noise amplifier (LNA) operating around 24-/60-GHz realized in a 0.18-μm SiGe BiCMOS process, featuring the simultaneous achievement of rejection of the most significant side-products stemming from non-linearity and dual-band input matching exploiting Miller effect. The rejection network connected between the input and cascode devices of the first stage is designed to suppress the most significant inter-modulation (IM) product at 36 GHz and harmonic at 48 GHz that appear between the two passbands to avoid degradation of the linearity performance of the LNA, especially in the concurrent dual-band operation. At the same time, the rejection network plays an important role in achieving the dual-band input matching through Miller effect with only one physical inductor at the input instead of at least two physical inductors generally required at the input for matching at two different frequencies. This is advantageous in terms of the chip size and presumably the noise figure by obviating at least one physical inductor at the input, which is explained in details in the remainder of this chapter.

The designed concurrent K-/V-band LNA achieves good gain balance between the two passbands as well as good rejection of the most significant IM product and harmonic at 36 and 48 GHz (larger than 30 dBc), which can be confirmed from the measured results later in this chapter. The LNA occupies 1 mm × 0.7 mm including all the RF and dc pads and 0.7 mm × 0.36 mm without the pads. It only consumes 8-mA dc

current at 1.8-V supply voltage (P_{DC} = 14.4 mW), which confirms that the size and the power consumption are in similar order of the single-band counterparts designed at either K-band or V-band.

4.1 Introduction and Motivation

As myriads of wireless standards and applications operating at different frequency spectrums are prevailing, wireless transceivers capable of handling multiple operating frequencies concurrently can be beneficial in regards to functional versatility, chip size, cost, dc power consumption, etc. Since the late 90's, there have been attempts to develop systems or building bocks concurrently operating at two distinct frequency bands in the lower microwave frequency range [24-27]. Dual-band wireless router supporting both 2.4- and 5-GHz frequency bands is one of the most widely known and commercially available multi-band systems, where the users can choose through which frequency band they want to communicate. Another existing application, which finds the multi-band systems to be useful, is geological sensing. It measures the earth response at multiple frequencies, which is equivalent to measuring the earth response from multiple depths. Both applications employ separate antennas and transceiver chipsets for each operating frequency, which is not viable (or at least very inefficient) especially when it comes to an integration within any small hand-held devices or sensors.

As the most indispensable building block in any transceiver systems, amplifiers employed in multi-band transceivers should be capable of operating concurrently at multiple frequency bands while maintaining other performance metrics (e.g. NF, gain,

linearity, etc. for low noise amplifier (LNA)) in order to exploit the benefits in terms of size, cost and dc power consumption. A multi-band amplifier can be implemented within a similar footprint of a single-band amplifier. Also, the power consumption of a multi-band amplifier can be made smaller than the sum of all single-band amplifiers [27]. However, a multi-band amplifier has an inherent linearity problem mainly caused by the direct inter-modulation (IM) products as well as the harmonics generated by the multiple main carrier signals and their numerous harmonics. Therefore, the significant side-products have to be sufficiently suppressed in order not to degrade the linearity performance of the overall amplifier when multiple tones are concurrently applied.

One of the most intuitive ways to implement a multi-band amplifier is to design all the matching networks for multiple operating frequencies [28-30]. In [28], a concurrent dual-band (25.5-/37-GHz) power amplifier (PA) employing dual-band impedance matching filtering networks shows the detailed analysis and good experimental results, but the needs for having two distinct pass bands is questionable as no significant IM products and harmonics appear between the two passbands, which will be discussed in the following section. Dual-band amplifiers operating at X-/K-band incorporating dual-band matching scheme are presented in [29, 30], showing fairly good dual-band input/output matching performance. However, both amplifiers have large gain imbalance (about 10-dB) between the two passbands and large chip size, which make the design less suitable when it comes to system integration.

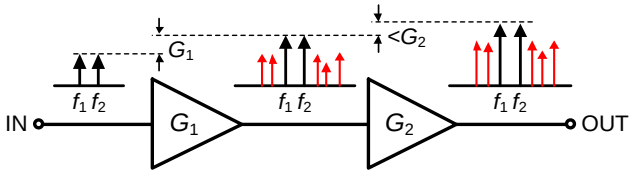
Another method is to embed notch (bandstop) circuits based on a wideband amplifier design [31, 32], which is adopted by this LNA design. [31] reports a

concurrent tri-band (13.5-/24-/35-GHz) LNA utilizing the tri-band feedback notch circuit as a load while the input and output are wideband-matched. Even though it achieves well-balanced passband gains with good stopband rejection characteristics, the power performances are only characterized in single-band modes and the locations of two notch frequencies seem to be arbitrary, making the proper concurrent operation questionable. In [32], a concurrent tri-band (15-/25-/35-GHz) PA based on a distributed amplifier (DA) and active noth filter is presented. While showing good experimental results, DA-based implementation makes the chip size inevitably large and causes high dc power consumption, and the notch performance can be very prone to the negative resistance generation circuits.

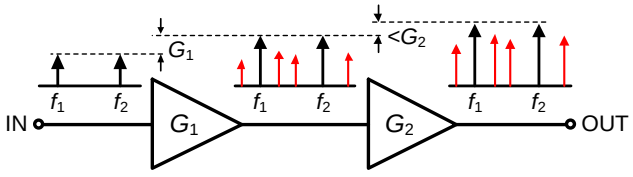
This chapter presents the design of LNA operating concurrently at K-/V-bands. The rejection network employed between the input and cascode devices of the first stage not only rejects the direct IM product (36-GHz) and the most significant harmonic (48-GHz) appearing between the two passbands, but also acts as a part of the dual-band input matching through Miller effect. Therefore, the input matching both at K- and V-band can be achieved by employing only a single physical series inductor at the base terminal of the input device, which may help reduce the overall noise figure as well as the chip size as compared to a dual-band input matching network, which generally requires at least two physical inductors at the input. In the remainder of this chapter, the analysis and experimental results will be presented to validate the proposed design methodology.

4.2 Considerations of Inter-Modulation Products and Harmonics in Concurrent Dual-Band Amplifiers

As discussed in the previous section, a concurrent dual-band amplifier with distinct two passbands can be advantageous over combined two separate single-band amplifiers in parallel in regards to size and dc power consumption, while the linearity performance is inherently inferior due to numerous IM products and harmonics generated, which cannot be perfectly removed. Compared to a wideband amplifier, a dual-band amplifier can have better linearity performance than a wideband amplifier when both of them are subjected to the same two concurrent tones if all the critical IM products and harmonics are sufficiently suppressed. This notion is based on the fact that in general, it is theoretically easier to suppress the IM products and harmonics in a dual-band amplifier than in a single wideband amplifier covering the same dual-band continuously when both of them are injected with the same arbitrary dual-band signals.



(a)



(b)

Fig. 4.1. Conceptual generation of IM products and harmonics with two main tones (f_1 and f_2) applied to a wideband amplifier for cases that (a) $f_1 < f_2 < 2f_1$, and (b) $2f_1 < f_2$.

Fig. 4.1 illustrates the generation of IM products and harmonics when the two fundamental tones (f_1 and f_2) are applied to input of the wideband amplifier formed by two cascaded gain stages (G_1 and G_2). Note that no memory effect is assumed in the following discussion for brevity. Also, note that the levels of IM products and harmonics (represented as "red" arrows) are not to scale. There are two different scenarios for the selection of the two fundamental frequencies regarding to their relative positions.

When the two tones located such that $f_1 < f_2 < 2f_1$ are applied at the input of the amplifier as shown in Fig. 4.1(a), no significant IM products or harmonics appear between f_1 and f_2. Therefore, a wideband amplifier with a bandwidth covering f_1 and f_2 can handle the concurrent dual-band operation as long as the dominant IM products and harmonics residing outside the bandwidth of interest are properly suppressed. If f_1 = 25.5 GHz and f_2 = 37 GHz as in [28], for instance, the dominant side products arising from the non-linearity include 11.5 GHz ($f_2 - f_1$), 62.5 GHz ($f_1 + f_2$), 14 GHz ($2f_1 - f_2$), 48.5 GHz ($2f_2 - f_1$), etc. Therefore, for a given layout footprint, it will be more effective to suppress the dominant side products residing outside the bandwidth but close to the passband rather than to make two distinct passbands in terms of the overall linearity.

On the other hand, if the two tones are placed quite apart from one another such that $f_2 > 2f_1$, some critical IM products and harmonics appear especially between the two fundamental tones as depicted in Fig. 4.1(b). The most problematic ones are the lower-side direct IM product between the two main tones ($f_2 - f_1$) and the second harmonic of the lower main tone ($2f_1$). If not sufficiently suppressed before entering G_2, they will be mixed with the amplified (by G_1) fundamental tones inside G_2 and create another IM

products, which will reside right on top of the two fundamental tones (i.e. (f_2 - f_1) - f_1 and f_2 - (f_2 - f_1). As a result, it will cause the two fundamental tones to experience the gain compression or expansion, which deteriorates the overall linearity of the amplifier. For the case in Fig. 4.1(b), therefore, an amplifier design having two distinct passbands should be selected instead of wideband implementation. Note that the other direct IM product at f_1 + f_2 is also as large as one at f_2 - f_1, but it can be suppressed without any rejection networks due to the bandpass gain response covering between f_1 and f_2 only.

For both cases in Fig. 4.1(a) and (b), it is ideally the best practice to include any types of rejection networks at the output of each active device so that the dominant IM products and harmonics do not deteriorate the linearity performance of the overall amplifier, especially for concurrent dual-band operation. As the number of the rejection networks is increased, however, the size benefit of the dual-band design diminishes, and hence techniques to enhance the rejection level with as fewer number of the rejection networks as possible should be employed so as to maintain the footprint of the overall dual-band amplifier comparable to the single-band counterpart.

The rejection network can be simply implemented by parallel *LC* (in series with the signal path), series *LC* (in shunt to the signal path) networks, or their combination. In order not to degrade the passband gains, the quality factor (*Q*) of the network must be high enough, which results in a narrow rejection bandwidth. In this case, however, any mismatches during fabrication or any inaccuracy in simulations can cause deviation from the desired resonant frequency of the rejection network. As a result, the rejection of the targeted frequencies (e.g. the most significant IM products and harmonics) can be worse,

and this effect becomes much more problematic at millimeter-wave (mm-wave) frequencies. Therefore, the rejection bandwidth should be wide enough to maintain sufficient rejection in case of any variations and mismatches in the passive components, while it needs to be narrow enough to keep the passband gains intact.

4.3 Revisit of Miller Effect: Impact of Load Impedance on Input Impedance

4.3.1 Brief Introduction of Miller Effect

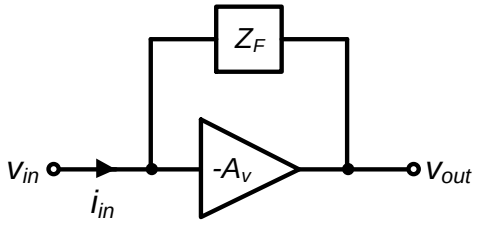


Fig. 4.2. An ideal inverting amplifier with feedback by Z_F.

In 1920, John M. Miller proposed that the impedance of the feedback element connected between input and output of the vacuum tube triode would be seen a number of times smaller than the actual impedance at the input [33], which is known as Miller effect. Fig. 4.2 shows an ideal inverting amplifier having gain of $-A_v$ with the feedback element (Z_F) connected between the input and output. Assuming infinite input impedance of the ideal inverting amplifier, the overall input impedance can be written as

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{\frac{v_{in} - v_{out}}{Z_F}} = \frac{Z_F}{1 - \frac{v_{out}}{v_{in}}} = \frac{Z_F}{1 + A_v} \tag{4.1}$$

which implies that Z_F is seen by $1+A_v$ times smaller at the input. If the feedback

element is a capacitor (i.e. $Z_F = 1/j\omega C_F$), for example, its effective capacitance seen at the input becomes $(1+A_v)C_F$.

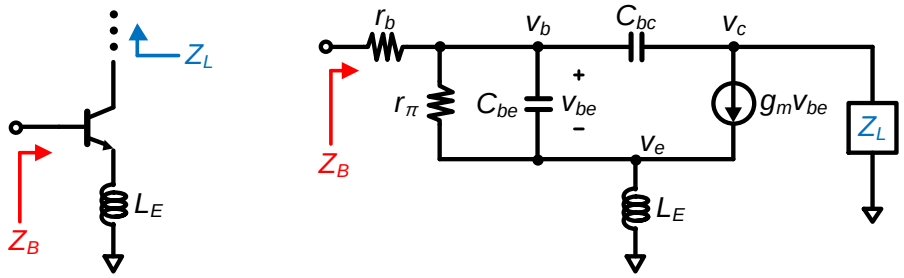
If the inverting amplifier is not ideal (i.e. finite input impedance and non-zero output impedance), however, the overall input impedance obtained by applying Miller approximation in (4.1) is not very accurate. One of the reasons is that the finite input impedance makes a fraction of i_{in} to flow into the input of amplifier, which results in a deviation from (4.1). It becomes even more significant at high operating frequencies such as mm-wave frequencies due to the capacitive input impedance of the actual transistor amplifiers. Another reason is that the non-zero output impedance makes the loading effect non-negligible. In other words, the load connected at the output does affect the input impedance through the feedback element. Therefore, for the actual transistor amplifiers especially at high frequencies, the detailed derivations are required to obtain the accurate overall input impedances for different load conditions while Miller approximation can give rough estimates.

4.3.2 Input Impedance of Common-Emitter Stage with Load Impedance, Z_L

Fig. 4.3 shows the inductive-degenerated common-emitter (CE) stage with a load impedance Z_L and its small-signal equivalent circuit. Note that the impedance (Z) and admittance (Y) are used interchangeably throughout this analysis, where $Z = 1/Y$. Let the impedance looking into the base terminal without the base-collector capacitor (C_{bc}) be Z_{BO}, which can be simply written as

$$Z_{BO} = \frac{g_m L_E}{C_{be}} + j\omega L_E + \frac{1}{j\omega C_{be}} \tag{4.2}$$

which is independent of the load impedance. Note that r_b and r_π are neglected because r_b is not critical in obtaining the input impedance at very high frequencies and r_π defined as β/g_m is much larger than the impedance of C_{be} at the frequencies of interest.



(a) (b)

Fig. 4.3. (a) Inductive-degenerated CE stage with load impedance Z_L, and (b) its small-signal equivalent circuit.

When C_{bc} is included, however, the impedance looking into the base (Z_B) becomes dependent on not only C_{bc} but also Z_L due to the current flowing between the base and collector nodes through C_{bc} and the resultant changes in the collector voltage (v_c). Applying Kirchhoff's current law (KCL) at the base node gives

$$i_b = j\omega C_{be}\left(v_b - v_e\right) + j\omega C_{bc}\left(v_b - v_c\right) \tag{4.3}$$

from which the input admittance can be expressed as

$$Y_B = \frac{i_b}{v_b} = \underbrace{j\omega C_{be}\left(1 - \frac{v_e}{v_b}\right)}_{Y_{BE}} + \underbrace{j\omega C_{bc}\left(1 - \frac{v_c}{v_b}\right)}_{Y_{BC}} \tag{4.4}$$

where $Y_B = 1/Z_B$, and Y_{BE} and Y_{BC} are the admittances seen from base terminal to emitter and collector terminals, respectively.

Applying KCL at the emitter and collector nodes, respectively, the voltage

transfer functions from the base terminal to the emitter and collector terminals can be found as

$$\frac{v_e}{v_b} = \frac{g_m + j\omega C_{be}}{g_m + j\omega C_{be} + \dfrac{1}{j\omega L_E}} \tag{4.5}$$

and

$$\frac{v_c}{v_b} \approx \frac{-g_m}{1 + j\omega g_m L_E} \cdot \left(\frac{1}{j\omega C_{bc} + Y_L} \right) \tag{4.6}$$

where Y_L is the load admittance (i.e. $1/Z_L$) and $g_m \gg j\omega C_{be}$ is assumed at the frequencies of interest. Substituting (4.5) and (4.6) into (4.4), the two admittance terms in (4.4) can be written as

$$Y_{BE} = \frac{j\omega C_{be}}{j\omega g_m L_E - \omega^2 L_E C_{be} + 1} \tag{4.7}$$

and

$$Y_{BC} = j\omega C_{bc} + \underbrace{j\omega C_{bc} \left[\frac{g_m}{1 + j\omega g_m L_E} \cdot \left(\frac{1}{j\omega C_{bc} + Y_L} \right) \right]}_{Y_M}. \tag{4.8}$$

where Y_M represents the load-dependent admittance seen at the base terminal (i.e. $1/Z_M$).

As can be seen in (4.7), Y_{BE} is the input admittance of the inductive-degenerated common-emitter stage without C_{bc} included, which is the reciprocal of Z_{BO} in (4.2). From (4.8), Y_{BC} can be represented as the parallel combination of C_{bc} and the load-dependent impedance, Z_M. Then, the equivalent circuit representing Z_B can be drawn using (4.7) and (4.8) as shown in Fig. 4.4, which is the parallel combination of Z_{BE} and Z_{BC} (or $Y_B = Y_{BE} + Y_{BC}$). Therefore, it is concluded that the input impedance can be

significantly affected by the load impedance as well as the feedback capacitor through Miller effect.

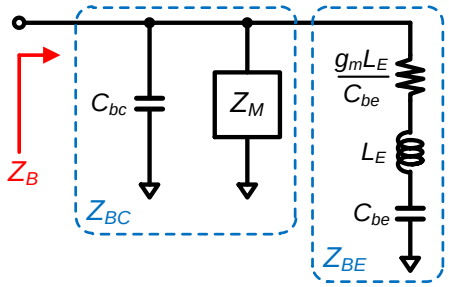


Fig. 4.4. Equivalent circuit representing the impedance looking into the base of the inductive-degenerated CE stage with the load, Z_L.

It is neither intuitive nor simple to predict the exact mechanism how the load impedance is seen at the input through Miller effect. For better intuition, the load-dependent admittances (Y_M) for several different special load conditions are derived and summarized in Appendix A. In the next section, the details on the dual-band input matching exploiting Miller effect is presented by applying the analysis performed in this section.

4.4 Circuit Design and Analysis

4.4.1 Circuit Design Brief

The circuit schematic of the designed concurrent K-/V-band concurrent LNA is shown in Fig. 4.5. Two inductively degenerated cascode stages are cascaded, where L_{E1} is employed for simultaneous noise and input matching near the upper passband and L_{E3} for gain balancing at both passbands and linearity enhancement. The input transistor of

the first stage (Q1) is sized with the emitter width and length of 0.13 μm and 10 μm, respectively, while all other transistors (Q2 - Q4) have the same size as Q1. CBEBC configuration (one emitter, two base, and two collector fingers) is chosen for all the transistors with considerations of the targeted gain, noise figure, etc. [20].

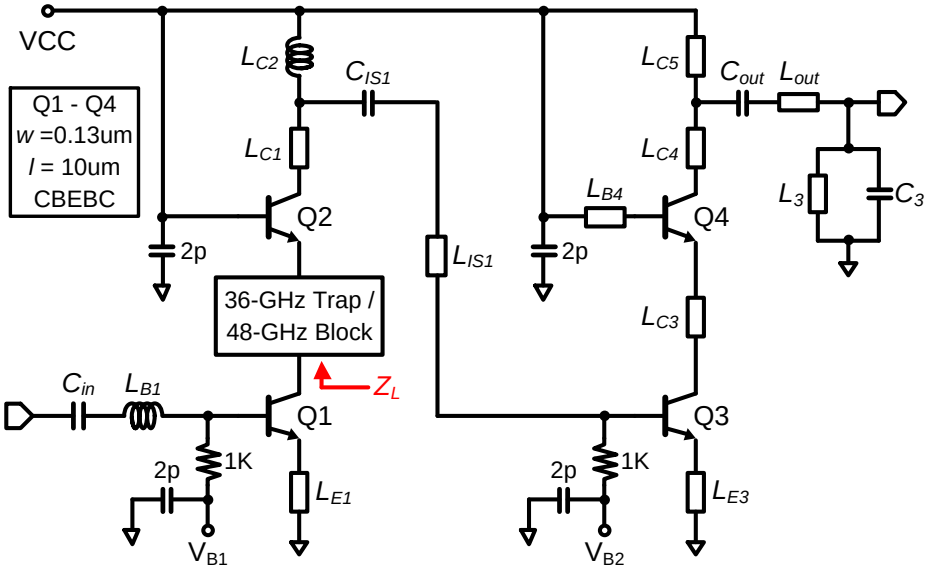


Fig. 4.5. Circuit schematic of the designed concurrent K-/V-band LNA.

Input matching at both K- and V-bands is achieved by employing only a single series inductor (L_{B1}) at the base of Q1, while generally at least two physical inductors are required to achieve the dual-resonance and hence dual-band input matching. It is possible due to the collaboration of the 36-GHz Trap / 48-GHz block network and Miller effect, which is presented in details in the following subsection. Wideband *T*-type matching method in is applied to the inter-stage matching between the first and second stage rather than the conventional narrowband shunt matching scheme. The dual-band output matching is achieved conventionally by employing multiple inductive sections

while each passband is narrowband-matched. Table 4.1 lists all the passive components values used in the LNA design shown in Fig. 4.5, where all the inductance values are extracted from EM-simulated data at 60 GHz using Mentor Graphics IE3D EM-simulator [23].

Table 4.1 Passive component values used in the actual design

C_{IN}	550 fF	L_{B1}	154 pH	L_{C3}	5 pH
C_{ISM}	200 fF	L_{E1}	54 pH	L_{B4}	10 pH
C_{OUT}	240 fF	L_{C1}	73 pH	L_{C4}	70 pH
C_3	100 fF	L_{C2}	125 pH	L_{C5}	50 pH
		L_{IS1}	150 pH	L_{OUT}	50 pH
		L_{E3}	20 pH	L_3	55 pH

4.4.2 36-GHz Trap / 48-GHz Block Network

The rejection (36-GHz trap / 48-GHz block) network consists of the series L_1-C_1 and parallel L_2-C_2 resonators tuned at 36 GHz and 48 GHz, respectively, as shown in Fig. 4.10(a). It is designed to reject the most significant IM product at 36 GHz (between the two main tones at 24 GHz and 60 GHz) and the second harmonic at 48 GHz of the lower main tone (24 GHz) appearing between the two passbands. Fig. 4.10(b) shows the 3-D view layout of the rejection network. L_1 and L_2 are realized by spiral inductors, and MIM capacitors available in the design kit are used for C_1 and C_2, where the reference planes are marked as white dashed lines. Fig. 4.10(c) plots the transmission characteristics (S_{21}) through the simulation using IE3D EM simulator. It shows that the rejection of 36- and

48-GHz signals more than 20 dB with referenced to the insertion losses at the two passbands. Therefore, if the rejection network is connected in series with the signal path, it can be used to block the transmission of the unwanted side products at 36 and 48 GHz.

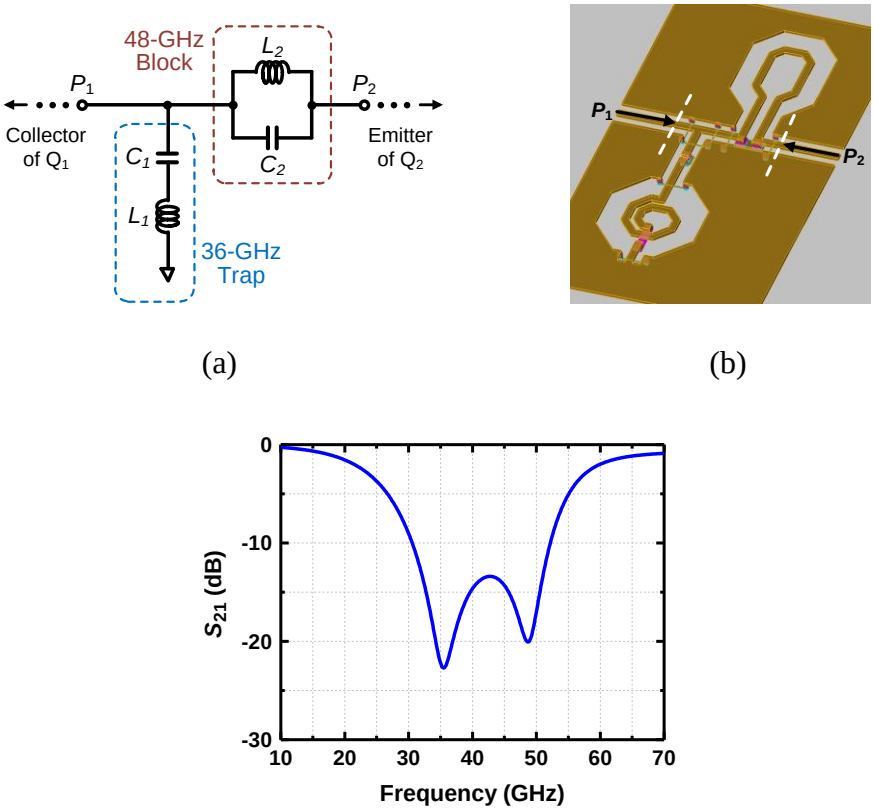
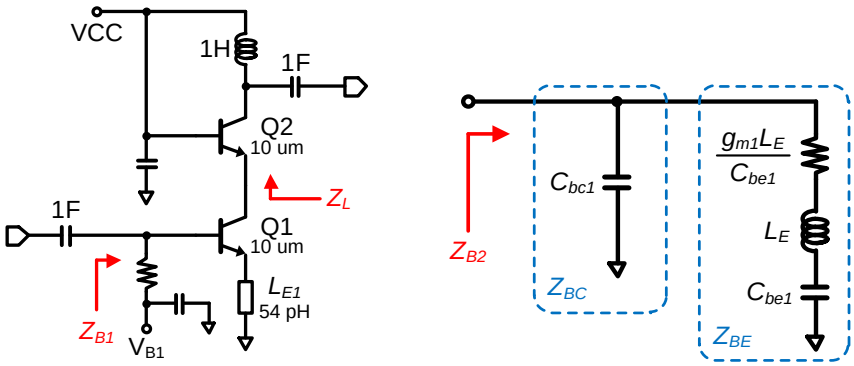


Fig. 4.6. (a) 36-GHz trap / 48-GHz block network schematic, (b) its layout in 3-D view and (c) its transmission characteristic (S_{21}) with 50-Ω port impedance.

4.4.3 Input Impedance of General Cascode Stage

Before delving into the details of the dual-band input matching, the examination on the input impedance of the general cascode stage is preceded. In case of the normal cascode configuration as shown in Fig. 4.7(a), Z_L can be approximated to be $1/g_{m2}$, which is generally much smaller than $1/j\omega C_{cs1}$ at the design frequencies and hence it is

legitimate to assume $Z_L \approx 1/g_{m2}$. Assuming $g_{m1} = g_{m2}$ and using (A.6) in Appendix A, Y_M can be found to be the parallel combination of very small capacitance and very small conductance, which therefore can be ignored. That is, only C_{bc} exists in (4.8) and the equivalent network representing the impedance looking into Q1 (Z_{B2}) can be drawn as shown in Fig. 4.7(b).



(a) (b)

Fig. 4.7. (a) Schematic of general cascode stage for input impedance simulation and (b) equivalent network representing the impedance looking into the base of Q1.

The device model parameters including parasitic capacitances of Q1 are extracted after layout in Cadence circuit simulator, where the extracted parameters are listed in Table 4.2. In order to check the validity of the equivalent circuit shown in Fig. 4.7(b), the input impedance of the equivalent circuit (Z_{B2}) is simulated using the extracted parameters in ADS circuit simulator. Fig. 4.8 plots both Z_{B1} from Cadence circuit simulator (red trace) and Z_{B2} from ADS circuit simulator (blue trace) over the frequency range from 10 GHz to 70 GHz, which shows reasonably similar results. Therefore, the extracted parameters of the input transistor together with the input

impedance expression in (4.8) are legitimate and can be used for the dual-band matching analysis in the next subsection.

Table 4.2 Transistor (Q1) parameters after layout extraction

C_{be1}	C_{bc1}	C_{cs1}	g_{m1}
125 fF	32 fF	24 fF	0.19 mS

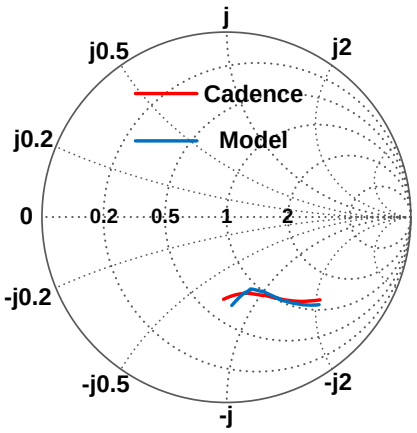


Fig. 4.8. Simulated input impedances of general cascode stage from 10 GHz to 70 GHz using both Cadence circuit simulator and equivalent model.

4.4.4 Dual-Band Input Matching Exploiting Miller Effect

Beside of the IM product and harmonic suppression discussed in the subsection 4.4.2, the rejection network plays another important role as a part of the dual-band input matching through Miller effect. Fig. 4.9 shows the small-signal equivalent circuit of the input stage of the dual-band LNA in Fig. 4.5, where all the parasitic resistances such as r_b, r_π, and r_e are excluded for simplicity. Z_L is the impedance looking into the rejection

network and Z_{LT} is the parallel combination of Z_L and C_{cs1}, where C_{cs1} is the parasitic capacitance at the collector of Q1 with referenced to the substrate.

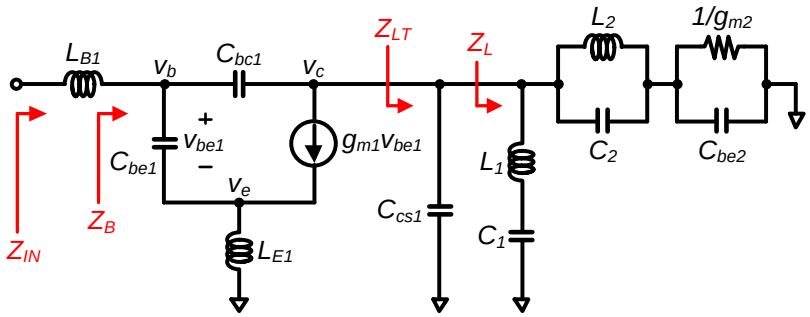
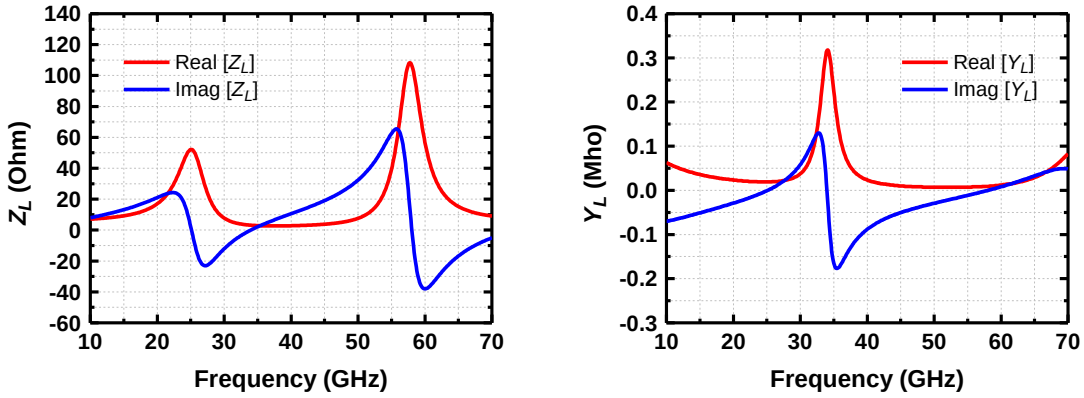


Fig. 4.9. Small-signal equivalent circuit of the input stage of the designed LNA.



(a) (b)

Fig. 4.10. (a) Impedance (Z_L) and (b) admittance (Y_L) looking into the rejection network.

Obviously, Z_L is totally different from that of the general cascode configuration. Then, what happens if Z_L is other than $1/g_m$, which is normally small? Fig. 4.10 plots the impedance and admittance looking into the rejection network. As can be seen from Fig. 4.10(a), Z_L can be roughly modeled as parallel LC with pretty low Q factor around at 25 GHz and 58 GHz. Because the real parts of Z_L are fairly large and comparable to that of

C_{cs1} around 25 GHz and 58 GHz, C_{cs1} cannot be neglected and hence Z_{LT} becomes the parallel combination of Z_L and C_{cs1}, where C_{cs1} is estimated to be 24 fF from the parameter extraction. Consequently, the inclusion C_{cs1} will shift the resonant frequencies in Z_L to slightly lower frequencies. The load admittance (Y_L) is also plotted in Fig. 4.10(b) as it is more convenient for calculating Y_M.

As it is extremely complicated to obtain Y_M with the exact expression of Y_{LT} using low-Q parallel *LC* models in the vicinity of the two passbands, the load-dependent admittances are only examined at the two resonant frequencies of 25 GHz and 58 GHz, where Y_{LT} can be represented as the parallel combination of *G* and *C* at the frequencies. Letting $Y_{LT} = G_L + j\omega C_L$ and substituting it into the load-dependent admittance term in (4.8), it can be written that

$$Y_M = \frac{j\omega g_{m1} C_{bc1}}{1 + j\omega g_{m1} L_{E1}} \cdot \frac{1}{j\omega C_T + G_L} \tag{4.9}$$

where $C_T = C_{bc1} + C_L$. Note that (4.9) is in the identical form to Y_M with the resistive load as in (A.2) and hence it can be expected that Y_M is represented as the parallel combination of *G*, *L*, and *C*. Rearranging (4.9) gives the exact expressions for each equivalent component as

$$G_M = \frac{\omega\left(g_m L_E + C_T/G_L\right)\left(\omega C_{bc} g_m/G_L\right)}{T} \tag{4.10}$$

$$L_M = \left[\frac{\omega\left(\omega C_{bc} g_m/G_L\right)\left(\omega g_m L_E\right)\left(\omega C_T/G_L\right)}{T}\right]^{-1} \tag{4.11}$$

$$C_M = \frac{C_{bc} g_m/G_L}{T} \tag{4.12}$$

where

$$T = \left[1 + \left(\omega g_m L_E\right)^2\right] \cdot \left[1 + \left(\omega C_T / G_L\right)^2\right]. \tag{4.13}$$

The equivalent network representing Z_B around at 25 GHz and 58 GHz in Fig. 4.9 can be drawn as shown in Fig. 4.11. Since Z'_{B1} is the impedance looking into the general cascode stage (Z_{B2}) as shown in Fig. 4.7(b), it is only required to examine that how Y_M is affected by the load impedance both at 25 GHz and 58 GHz. Note that, in order to find the equivalent components constituting Y_M, the extracted parameters of Q1 as listed in Table 4.2 are used.

Starting from Z'_{B1} in Fig. 4.11(the same as Z_{B2} in in Fig. 4.8), there are two main steps to achieve the dual-band matching. One is to position Z_B both at 25 GHz and 58 GHz close to the constant 50-Ω (i.e. r = 1) circle in the lower half of the Smith Chart. Then, the other is to bring Z_B at 25 GHz and 58 GHz close each other in the lower half of the Smith Chart. In doing so, the single series inductor (L_{B1}) can bring Z_B both at 25 GHz and 58 GHz inside the circle of S_{11} = -10 dB, which confirms the input matching both at 25 GHz and 58 GHz.

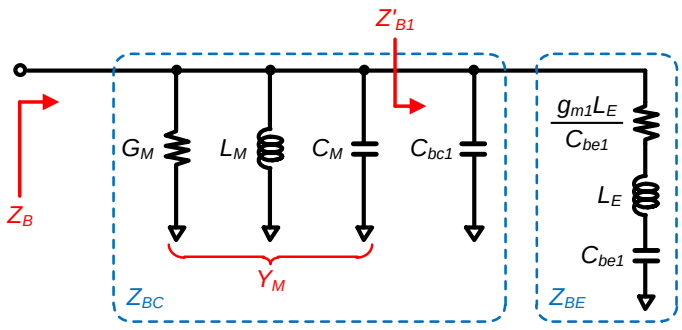


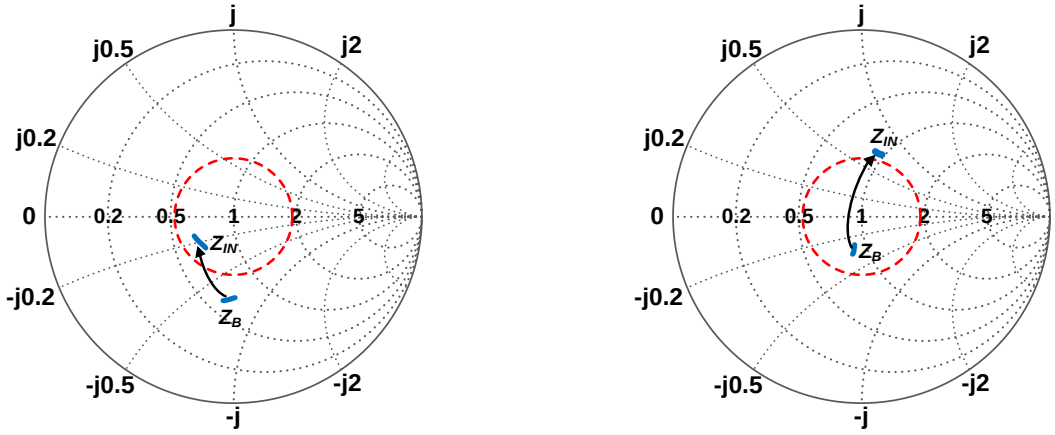
Fig. 4.11. Equivalent network representing the input impedance of the designed LNA only valid in the vicinity of two passbands.

In order to validate the approach, Z_B in Fig. 4.11 is simulated using the extracted parameters in Table 4.1 and Y_L shown in Fig. 4.10(b). Table 4.3 summarized the calculated component values constituting Y_M both at 25 GHz and 58 GHz. Note that Y_M represented by parallel *G*, *L*, and *C* is valid only for the capacitive load or parallel *RC* load as manifested in Appendix A. Fig. 4.12 plots not only Z_B but also Z_{IN} by adding a series inductor to Z_B near at 25 GHz and 58 GHz from the equivalent circuit model in Fig. 4.11. Note that the red-dashed circle on the Smith Chart represents the input impedances resulting in S_{11} = -10 dB and it is added for better visualization of the input matching. While not being perfectly precise, adding a single series inductor (L_{B1} = 154 pH) does bring Z_B inside or at least very near the circle of S_{11} = -10 dB, resulting in the input matching both around at 25 GHz and 58 GHz.

Fig. 4.13 plots Z_B and Z_{IN} of the designed dual-band LNA from the actual circuit simulation in Cadence. As can be seen in Fig. 4.13(a), Z_B near the two passbands are located close each other and near the constant 50-Ω circle. Then, adding an inductor (L_{B1} ≈ 150 pH) in series with the base moves Z_B inside the circle of S_{11} = -10 dB for both passbands as shown in Fig. 4.13(b). Therefore, the rejection network through Miller effect gives dual-band input matching by using only one physical inductor at the input.

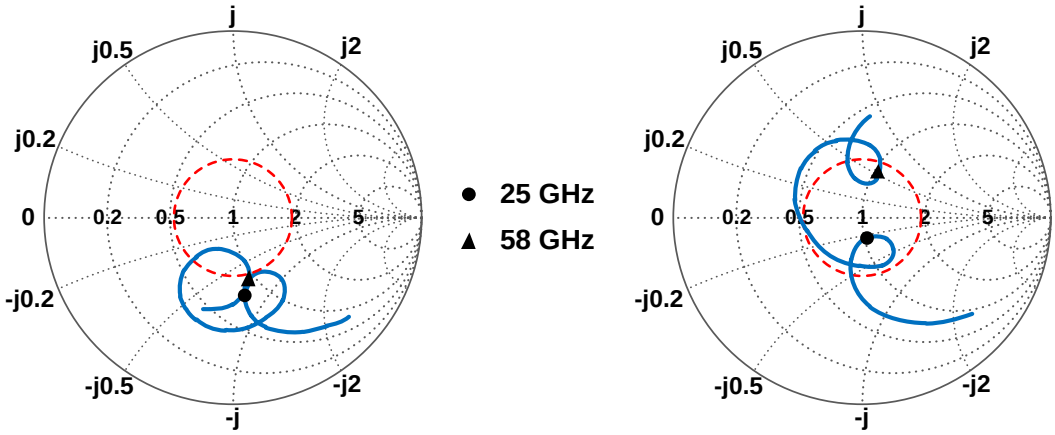
Table 4.3 Calculated component values constituting Y_M at 25 and 58 GHz

Frequency	G_M	L_M	C_M
25 GHz	0.013 Ω^{-1}	1.5 nH	75 fF
58 GHz	0.012 Ω^{-1}	150 pH	14 fF



(a) (b)

Fig. 4.12. Z_B and Z_{IN} near (a) 25 GHz and (b) 58 GHz using the equivalent circuit model. Red dashed-circle represents the input imedances resulting in S_{11} = -10 dB.



(a) (b)

Fig. 4.13. (a) Z_B and (b) Z_{IN} from the actual circuit simulations in Cadence. Red dashed-circle represents the input impedances resulting in S_{11} = -10 dB.

4.5 Experimental Results

The chip microphotograph of the designed concurrent K-/V-band LNA is shown in Fig. 4.14. The whole chip including all the test pads measures 0.98 mm × 0.75 mm while the core size without the pads is 0.68 mm × 0.36 mm. The fabricated concurrent K-/V-band LNA was measured by on-chip probing using Rhode & Schwarz ZVA67 network analyzer having built-in noise figure measurement capability.

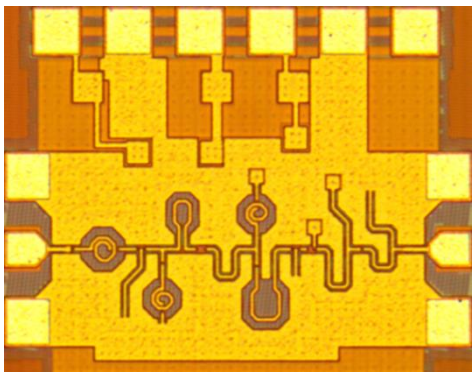


Fig. 4.14. Chip microphotograph of the fabricated concurrent K-/V-band LNA.

The simulated and measured forward gains (S_{21}) are plotted in Fig. 4.15. The measured peak S_{21} for each passband are 20.2 dB at 25.5 GHz and 20.1 dB at 61.5 GHz, while the simulated ones are 20.6 dB at 24.6 GHz and 20.2 dB at 60.2 GHz, showing the peak gain frequencies at both passbands are shifted up by 1.5-GHz. The measured 3-dB bandwidths for each passband are 2.4-GHz (24.7 to 27.1 GHz) and 6.5-GHz (58.8 to 65.3 GHz), showing reduction in the 3-dB bandwidths in both passbands by 1.9-GHz and 1.7-GHz, respectively, compared to the simulated ones. The measured rejection levels at 36 GHz and 48 GHz are -34 dBc and -31 dBc with referenced to the peak gain levels at both passbands, which are about 5-dB larger than the simulated ones, where the

difference might have stemmed from the inaccuracies of the MIM capacitor models in the design kit provided by the foundry.

The simulated and measured input (S_{11}) and output (S_{22}) return losses are plotted in Fig. 4.16. As can be seen from Fig. 4.16(a), the simulated input matching clearly shows dual resonance around at 25 GHz and 61 GHz while the measured result exhibits the resonances at 26.2 GHz and 61.5 GHz. In spite of the slight deviation from the simulated result, the measured result confirms the validity of the proposed dual-band matching strategy presented in the previous sections. The measured output return loss is pretty similar to the simulated one as shown in Fig. 4.16(b).

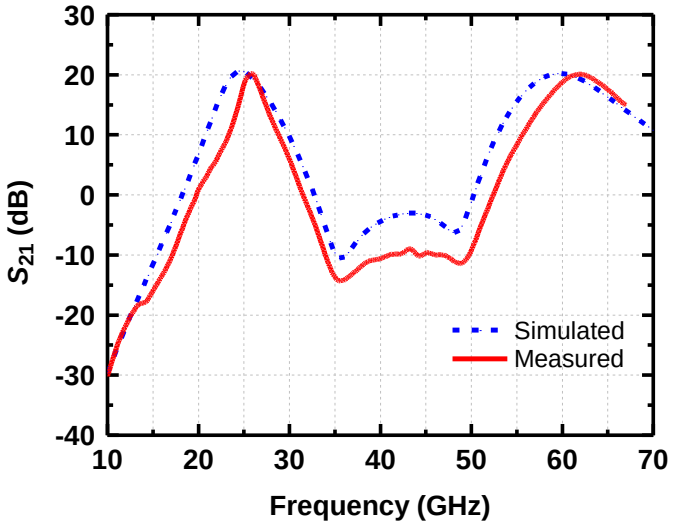
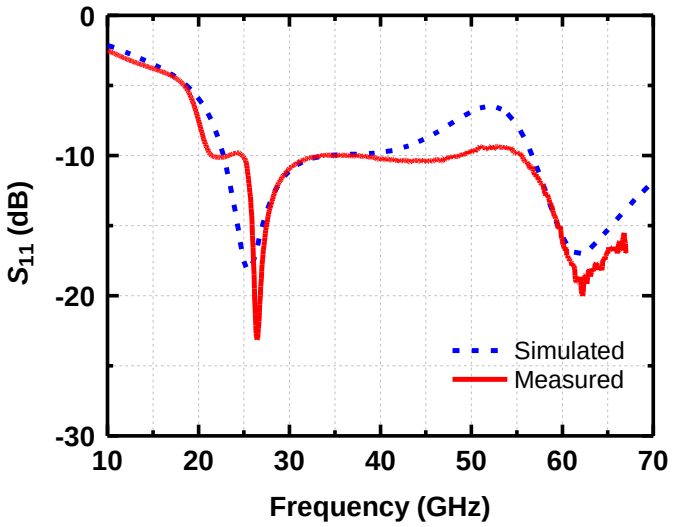
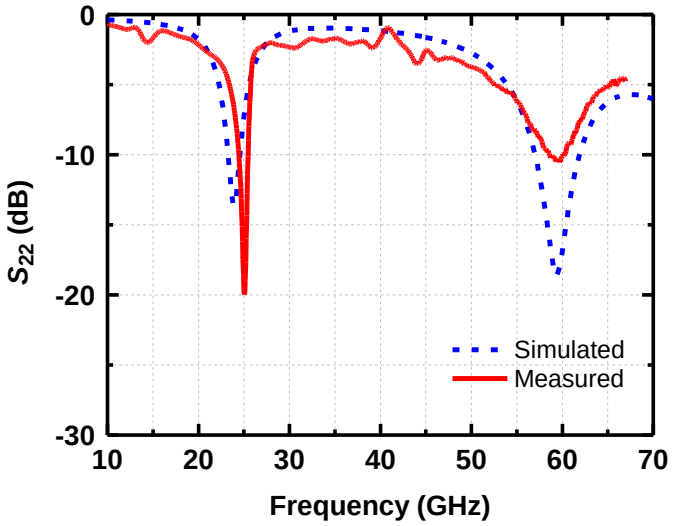


Fig. 4.15. Simulated and measured gain (S_{21}).



(a)



(b)

Fig. 4.16. Simulated and measured (a) input (S_{11}) and (b) output (S_{22}) return losses.

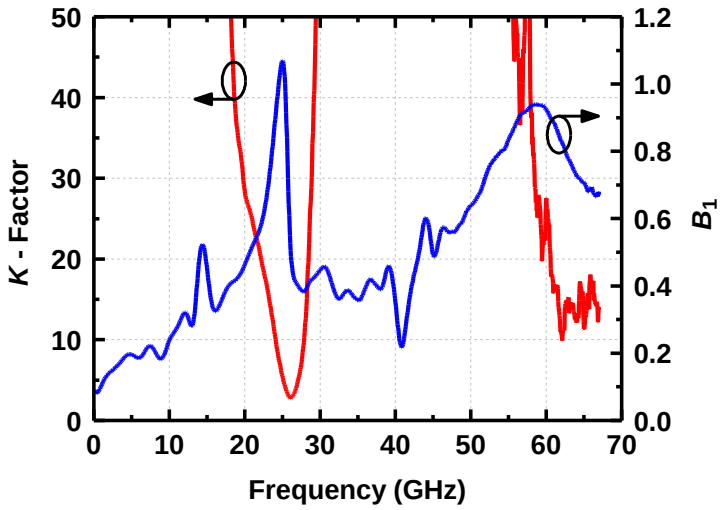


Fig. 4.17. Measured stability factor (K) and stability measure (B_1).

For unconditional stability check, the following necessary and sufficient conditions must be satisfied [22],

$$K > 1 \quad \text{and} \quad B_1 > 0 \tag{4.14}$$

where K and B_1 are the stability factor and stability measure, respectively. They have been measured and plotted in Fig. 4.17, which confirms the unconditional stability of the designed amplifier from dc to 67 GHz.

The simulated and measured noise figures are plotted in Fig. 4.18. Note that the NFs are measured only within the two passbands as the NFs between the two passbands are meaningless. The lowest noise figures in simulations are 3.8 dB and 5.7 dB at 23.5 GHz and 59 GHz, respectively, while the lowest measured noise figures are 4.1 dB and 6.1 dB at 25 GHz and 61 GHz, respectively.

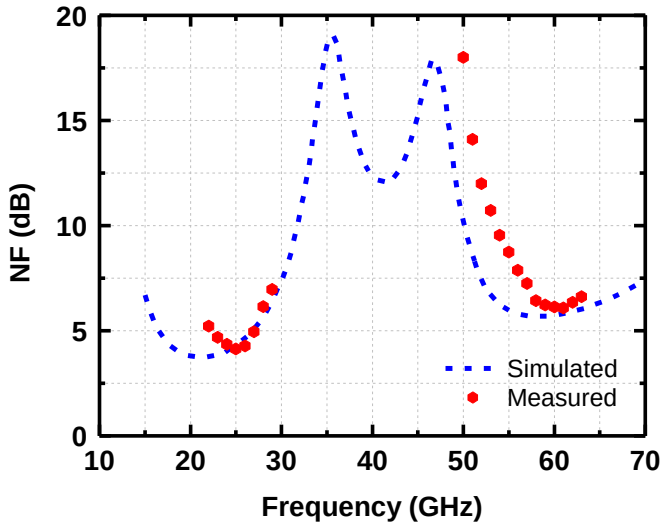
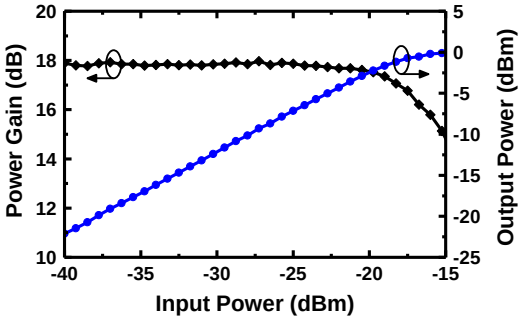
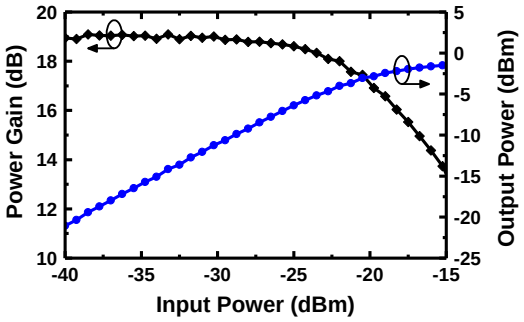


Fig. 4.18. Simulated and measured noise figure versus frequency.

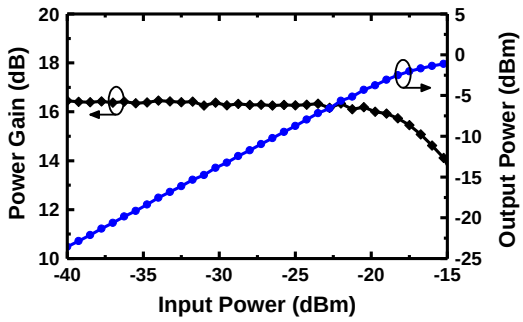
For the linearity test, large signal measurements are performed by applying concurrent dual-tone input as well as single-tone input. Fig. 4.19 plots the measured gain and output power versus the input power when the single tones in the lower passband (K-band) are applied. With the single-tone inputs at 25, 26, and 27 GHz, the measured input P_{1dB}s are -18.5, -22.3, and -17.5 dBm, respectively. The input P_{1dB}s with the single-tone input in the upper passband (V-band) are measured and shown in Fig. 4.20. With the single-tone input at 59, 60, and 61 GHz, the measured input P_{1dB}s are -18.7, -20.6, and -22.3 dBm, respectively. With the single-tone inputs either in the lower or upper passbands, the measured P_{1dB} performances are reasonable for its dc power consumption, and are comparable to the performances of the previously reported low-power single-band LNAs operating at K- [34-36] or V-band [12-14].



(a)

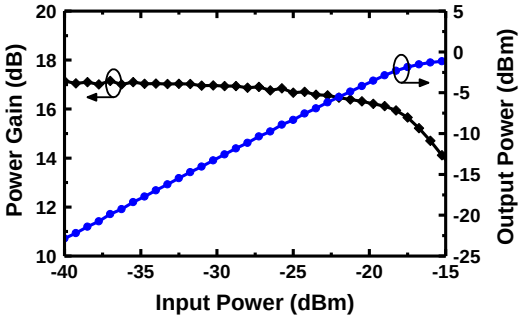


(b)

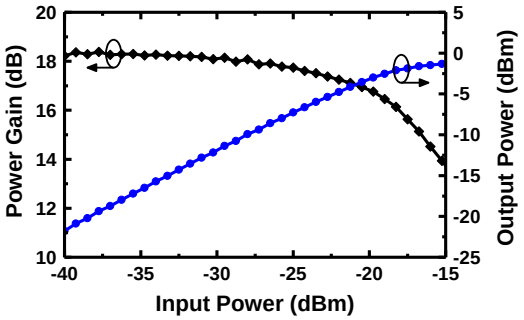


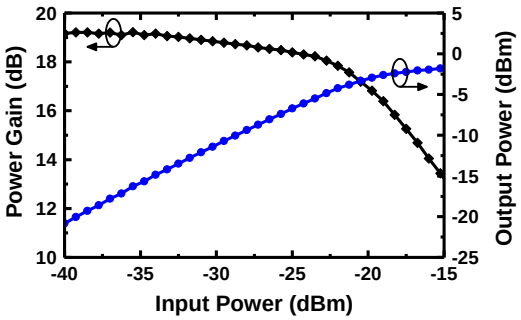
(c)

Fig. 4.19. Measured power gain and output power versus input power with single-tone inputs at (a) 25 GHz, (b) 26 GHz, and (c) 27 GHz.



(a)



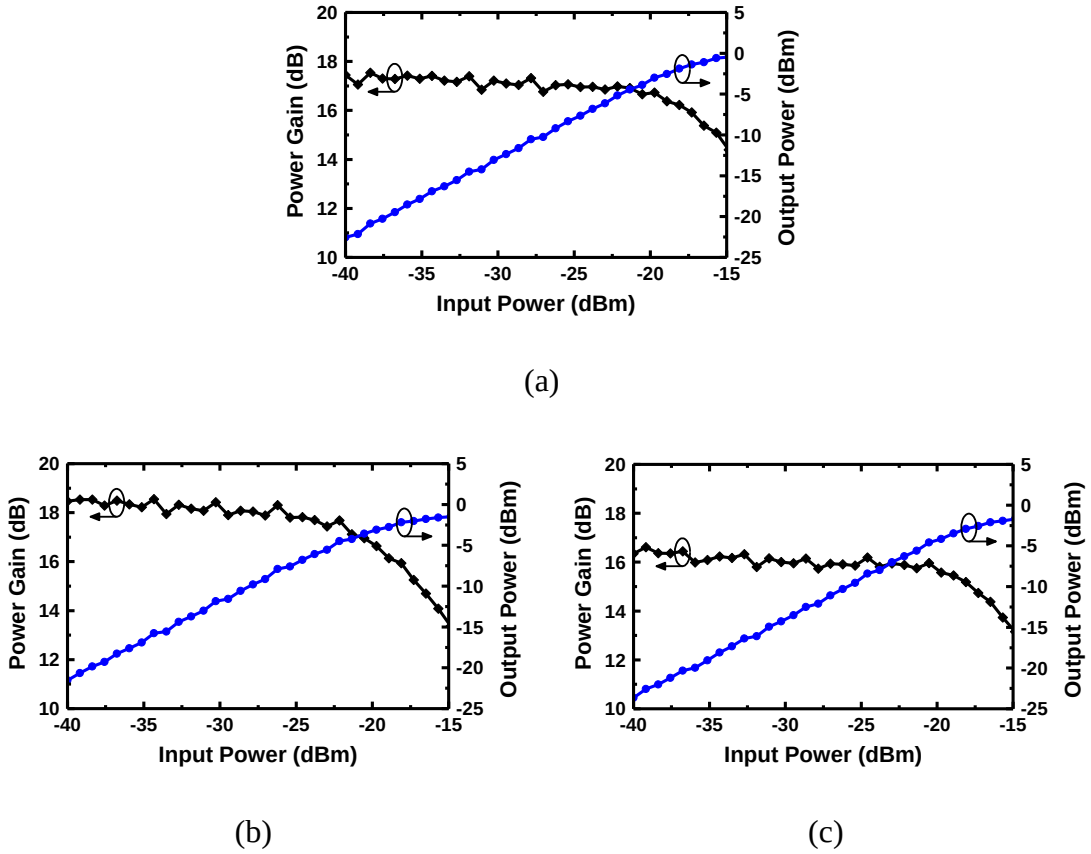


(b) (c)

Fig. 4.20. Measured power gain and output power versus input power with single-tone inputs at (a) 59 GHz, (b) 60 GHz, and (c) 61 GHz.

In order to check the large-signal performance of the dual-band LNA in concurrent dual-band operation, the measurements with simultaneous dual-tone inputs are conducted. Fig. 4.21 plots the results with dual-tone input (60 GHz in the upper passband and 25 GHz, 26 GHz or 27 GHz in the lower passband) measured at each tone in the lower passband. The input powers both at the lower and upper passbands are kept to be the same when swept from -40 dBm to -15 dBm. With the dual-tone inputs, the input P1dBs measured at 25, 26, and 27 GHz are -18.7, -22.2, and -18.2 dBm, respectively. The results in Fig. 4.21 show that the large signal performances in

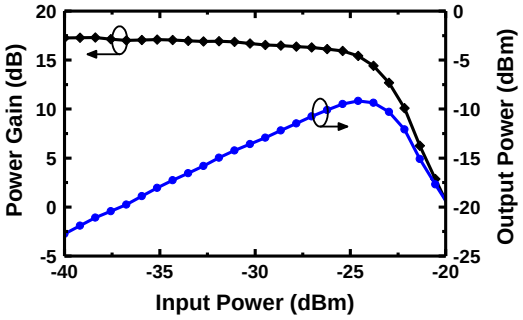
concurrent dual-band mode measured at the tones in lower passband are almost the same as those with single-tone input in the lower passband as plotted in Fig. 4.19. Therefore, it can be concluded that the tones in the upper passband rarely affect the linearity performance of the tones in the lower passband in the concurrent dual-band operation.



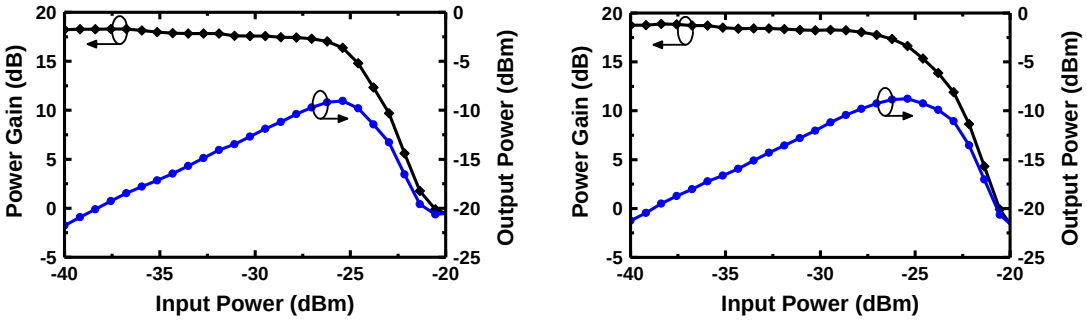
(a)

(b) (c)

Fig. 4.21. Measured power gain and output power versus input power with concurrent dual-tone input: (a) 25 GHz and 60 GHz input and measured at 25 GHz, (b) 26 GHz and 60 GHz input and measured at 26 GHz, and (c) 27 GHz and 60 GHz input and measured at 27 GHz.



(a)



(b) (c)

Fig. 4.22. Measured power gain and output power versus input power with concurrent dual-tone input: (a) 25 GHz and 59 GHz input and measured at 59 GHz, (b) 25 GHz and 60 GHz input and measured at 60 GHz, and (c) 25 GHz and 61 GHz input and measured at 61 GHz.

Fig. 4.22 plots the power gains and output powers with dual-tone input (25 GHz in the lower passband and 59 GHz, 60 GHz or 61 GHz in the lower passband) measured at each tone in the upper passband, where the input powers both at the lower and upper passbands are kept to be the same when swept from -40 dBm to -20 dBm. Unlike the results measured at the tones in the lower passband as shown in Fig. 4.21, the results measured at the upper passband with dual-tone inputs exhibit unexpected behaviors when measured at the tones in the upper passband. The measured output powers show

significant compression for the input power larger than -25 dBm, causing drastic gain roll-off. From the measured results, it can be deduced that the larger input power at the tones in the lower passband affects much more on the linearity. The most probable reason is that the IM products and harmonics generated when the two concurrent tones are applied pose much more severe limitation on the linearity performance at the upper passband frequencies since the power handling capability of the active devices gets worse at higher frequencies. To find out the exact cause, more investigations needs to be entailed. Table 4.4 summarizes the large-signal measurement results both with single-tone and concurrent dual-tone inputs, and Table 4.5 summarizes the measured performance of the designed concurrent K-/V-band LNA.

4.6 Summary and Conclusion

In this chapter, the concurrent K-/V-band LNA realized in 0.18-μm SiGe BiCMOS process is presented. The rejection network named as 36-GHz trap / 48-GHz block network not only suppresses the most significant direct IM product and harmonic appearing between the two passbands, but also act as a critical element of the dual-band input matching through Miller effect. Therefore, the input matching at the two distinct passbands can be achieved by employing only a single physical inductor at the input while at least two physical inductors are required to have dual-resonance. The designed concurrent dual-band LNA achieves 20-dB gain at both passbands, showing good gain balance between the two passbands. While showing some unexpected behavior in the large-signal performances measured at the tones in the upper passband when the two

concurrent tones are applied, the designed concurrent dual-band LNA shows quite competitive performances compared to the single-band counterparts while being packed within the similar layout footprint requires for a single-band amplifier implementation.

Table 4.4 Summary of large-signal measurements with single-tone (f_1 or f_2) and concurrent dual-tone (f_1 and f_2) inputs

f_1 (GHz)	f_2 (GHz)	Measured at (GHz)	$P_{1dB,in}$ (dBm)	$P_{1dB,out}$ (dBm)
25	None	25	-18.5	-1.5
26	None	26	-22.3	-4.3
27	None	27	-17.5	-2.0
None	**59**	59	-18.7	-2.7
None	**60**	60	-20.6	-3.4
None	**61**	61	-22.3	-4.3
25	**60**	25	-18.7	-2.1
26	**60**	26	-22.2	-4.7
27	**60**	27	-18.2	-2.8
25	**59**	59	-24.8	-9.5
25	**60**	60	-25.6	-9.7
25	**61**	61	-26.3	-9.6

Table 4.5 Measured performance summary of concurrent K-/V-band LNA

	24 GHz (K-band)	**60 GHz (V-band)**
S_{21} (dB)	20.2	20.1
S_{11} (dB)	-23.3	-18.8
S_{22} (dB)	-20.0	-10.3
NF (dB)	4.1	6.1
$P_{1dB,in}$ (dBm) (Single-tone)	-18.5	-20.6
$P_{1dB,in}$ (dBm) (Dual-tone)	-18.7	-25.6
DC Power (mW)	14.4 (8 mA at 1.8-V supply)	

CHAPTER V

CONCURRENT K-/V-BAND RF VARIABLE GAIN AMPLIFIER

This chapter presents the design of a concurrent K-/V-band RF variable gain amplifier (VGA) for a dual-band phased-array system realized in a 0.18-μm SiGe BiCMOS process. The dual-band RF VGA is developed starting from a wideband amplifier design covering from 24 GHz (f_1) to 60 GHz (f_2). In concurrent dual-band operation, the direct inter-modulation (IM) products between the two main carrier signals ($f_2 - f_1$ and $f_1 + f_2$) are of the biggest threats for degrading the linearity of the amplifier, which have to be suppressed as much as possible without increasing the chip size and degrading the passband gains. In order to achieve the goals, as many inductors used in the wideband amplifier design as possible are replaced with the transformer-coupled resonators (TCRs), which are designed to resonate at either one of the direct IM products. For the gain control, the conventional current-steering technique is employed but with a technique to reduce the phase variation in the course of gain tuning process, which is one of the most critical concerns in the phase array systems.

The developed K-/V-band RF VGA achieves the maximum gain of 19.8 dB and 20.3 dB at 24 GHz and 60 GHz, respectively. The gain tuning ranges at 24 GHz and 60 GHz are 1.2 to 19.8 dB and -0.8 to 20.3 dB, respectively. Over the entire gain tuning ranges, variations in the phase of S_{21} are only 3.2º and 6º at 24 GHz and 60 GHz, respectively, which are more than enough for phased-array systems employing 4-bit phase control (i.e. 16 phase states). The noise figures for the maximum gain states are

3.2 and 6.1 dB at 24 GHz and 60 GHz, respectively. The size of the layout is 1.3 mm by 0.76 mm with all the test pads while the active core area is only 0.65 mm by 0.35 mm. From a 1.8-V supply, it consumes only 8.4 mA dc current (P_{DC} = 15.1 mW).

5.1 Introduction and Motivation

For a receiver front-end, gain control is generally required to widen the receiver dynamic range. For certain systems such as a phased-array receiver with multiple channels, the gain control should be employed to compensate any gain imbalances among the channels stemming from constituent components such as antenna, phase shifter, etc. While the gain control function can be integrated inside the LNA itself, there could be noise figure issues especially at low gain states of the LNA. Therefore, it is a general practice to employ the low-noise gain stage with sufficiently high gain before the gain control stage so that the overall noise figure of the receiver is less affected by the gain tuning process. One of the biggest concerns, especially in a phased-array receiver, is the phase variation when the gain is tuned. It should be reduced as much as possible because large phase variation leads to recursive adjustments in the phase shifting states of each channel and hence dramatically increase the system complexity [37].

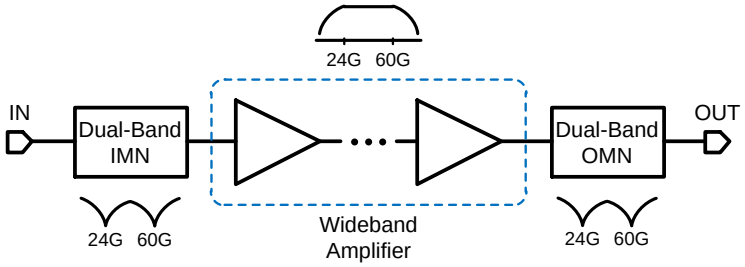


Fig. 5.1. Wideband amplifier with input and output matched both at 24 and 60 GHz.

Before implementing the gain control function, an amplifier operating at the two distinct passbands (center frequencies of each passband are at 24 GHz and 60 GHz) should be designed first. Suppose that a dual-band amplifier is to be designed starting from a wideband design covering from 24 GHz to 60 GHz with the input and output matched at both passbands as shown in Fig. 5.1. In spite of the wideband gain response, the overall transmission gain of the amplifier can be made to have some rejection (denoted as "*R*") near at 36 GHz, one of the direct IM products, due to the dual-band matching at the input and output as shown in Fig. 5.2. However, the rejection level may not be enough and hence it can degrade the linearity performance of the amplifier in concurrent dual-band operation mode compared to its single-band counterparts or dual-band amplifiers in the single-band mode.

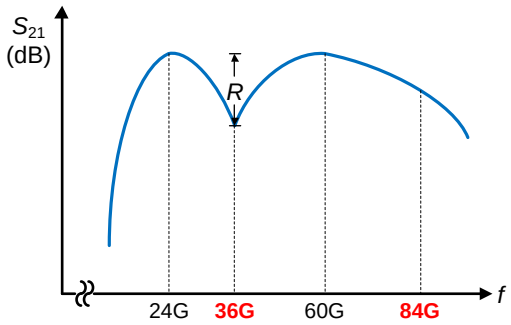


Fig. 5.2. Projected gain response of wideband amplifier with dual-band input and output matching.

To increase the suppression levels of the critical IM products, there are two conventional ways as mentioned in CHAPTER 4. One is to design all the matching networks for both frequency bands, which is very complex and can possibly make the chip size bulky. The other is to include as many bandstop networks as possible, which

obviously increases the chip size and may degrade the passband gains. Therefore, a simple and area-efficient method should be employed for a dual-band amplifier to be competitive with a single-band counterpart.

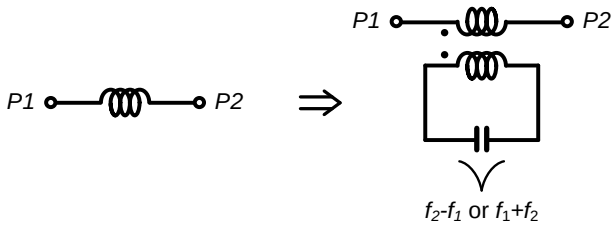


Fig. 5.3. Transformer-coupled resonator (TCR) in place of inductor.

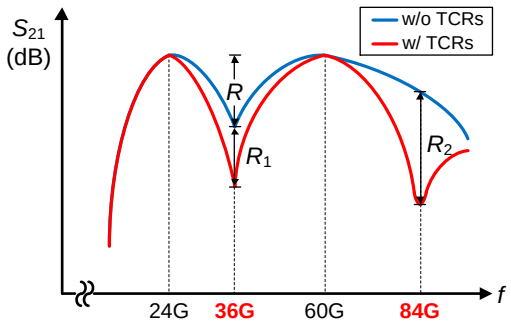


Fig. 5.4. Projected gain response of the wideband amplifier with its inductors replaced with TCRs.

This design proposes the replacement of as many inductors used in the wideband amplifier design as possible with transformer-coupled resonators (TCRs) as shown in Fig. 5.3, which does not increase the chip size as well as the design complexity. The resonant frequency of a TCR is primarily set by the *LC* resonator in the secondary coil side and hence each TCR can be designed to resonate either at 36 GHz ($f_2 - f_1$) or 84 GHz ($f_1 + f_2$), depending on the size of each inductor. Then, the gain response of the wideband amplifier with its inductors replaced with TCRs is expected to be as shown in

Fig. 5.4, from which the suppression of both direct IM products at 36 GHz and 84 GHz can be enhanced by R_1 and R_2, where R_1 and R_2 depends on the number of TCRs.

5.2 Circuit Design and Analysis

5.2.1 Circuit Design Brief

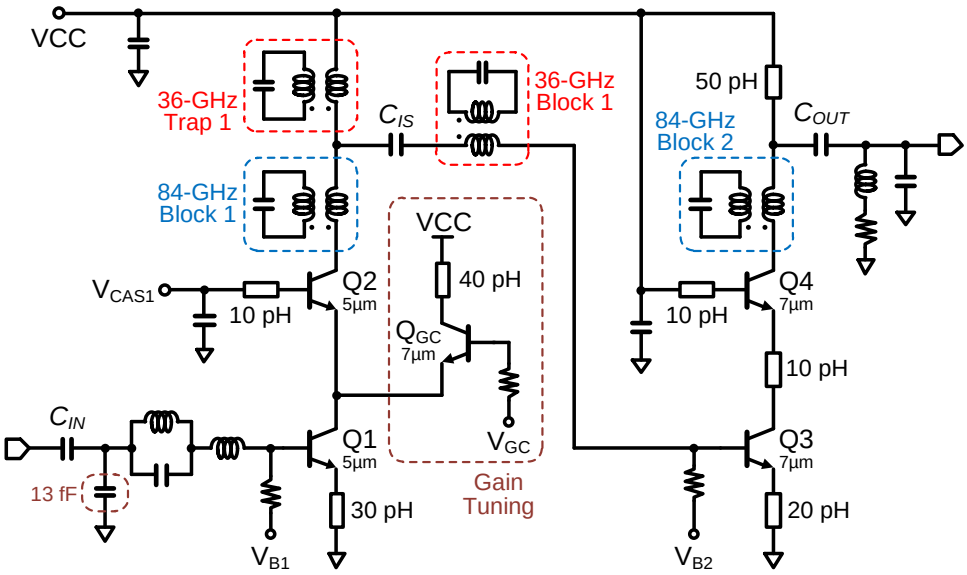


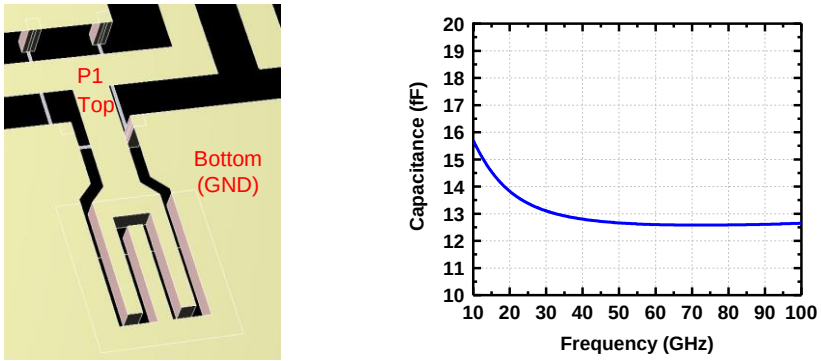
Fig. 5.5. Circuit schematic of the K-/V-band RF VGA.

Fig. 5.5 shows the circuit schematic of the designed K-/V-band RF VGA realized in a 0.18-μm SiGe BiCMOS process [11]. The input transistor of the first stage (Q1) has the emitter width and length of 0.13μm and l = 5 μm, respectively, with the two base fingers and two collector fingers (CBEBC). Conventional dual-band matching at the input is realized by employing two series inductors at the base of Q1 as well as the emitter degeneration inductor. To complete the input matching, the required small shunt

capacitance of 13 fF is realized by inter-digital capacitor as shown in Fig. 5.6(a). The capacitance is extracted from EM-simulated *Y*-parameters by using

$$C = \frac{\mathrm{Im}(Y_{11})}{2\pi f} \tag{5.1}$$

which is plotted versus frequency in Fig. 5.6(b). The input transistor of the second stage (Q3) is sized to have a longer length (l = 7 μm) than those of Q1 and Q2 while the configuration (CBEBC) is chosen to be the same as Q1 and Q2. Inductive degeneration is also employed in the second stage for balancing the gains at the two passbands as well as for linearity consideration.



(a) (b)

Fig. 5.6. Small inter-digital capacitor used for input matching: (a) 3-D view and (b) extracted capacitance versus frequency.

To increase the suppression of the two most critical direct IM products at 36 and 84 GHz, four inductors used in the wideband design are replaced with the TCRs. The resonant frequency of each TCR is determined by the size of the inductor, which is to be replaced. For example, for a fairly large inductor (e.g., larger than 100 pH), the secondary turn is drawn using the metal one layer below the primary turn and the

capacitance is chosen such that the TCR shows resonance at 36 GHz. For a small inductor, on the other hand, capacitance connected to the secondary turn is selected to make the TCR to resonate at 84 GHz. The details about the operation of the TCR and the selection of the resonant frequency are presented in the next subsection.

The gain control is achieved by the conventional current-steering technique through Q_{GC} in Fig. 5.5. By changing the base bias voltage of Q_{GC} (V_{GC}), the dc current flowing through the cascode device (Q2) is varied and hence is the gain of the first stage. Note that the gains at both passbands are controlled by similar amount as V_{GC} is tuned because independent gain control of each passband seems not feasible without the signal paths for each passband being separated. In order to reduce the phase variation over the gain tuning process, a series inductor of 40 pH is added, which is also used to route the dc bias line from the collector of Q_{GC} to the dc pad. The details on the gain control through the current-steering technique and the reduction of phase variation in the course of gain tuning process are provided in the next subsection.

5.2.2 Transformer-Coupled Resonator (TCR) Analysis

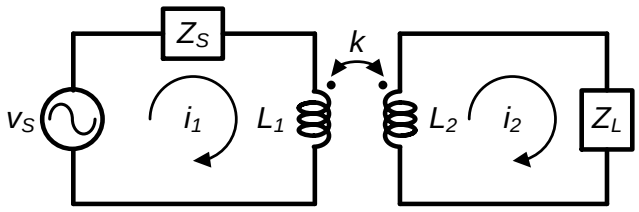


Fig. 5.7. Transformer with source and load impedances connected.

Fig. 5.7 shows the transformer with the source (Z_S) and load (Z_L) impedances connected to the primary (L_1) and secondary (L_2) inductors, respectively, where k denotes the coupling factor between the two inductors. For simplicity, the series resistance associated with each inductor is excluded in this analysis.

In order to find the impedance looking into the primary side, which is the main goal of this analysis, firstly the mesh equations for the primary and secondary sides are written as

$$\begin{aligned} v_S &= \left(Z_S + j\omega L_1\right) i_1 - j\omega M i_2 \\ 0 &= -j\omega M i_1 + \left(Z_L + j\omega L_2\right) i_2 \end{aligned} \tag{5.2}$$

and they can be rearranged in the Z-matrix form as

$$\begin{bmatrix} v_S \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Z_S + j\omega L_1 & -j\omega M \\ -j\omega M & Z_L + j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{5.4}$$

where M is the mutual inductance determined as

$$M = k\sqrt{L_1 L_2}. \tag{5.4}$$

As the current in the secondary mesh can be written as

$$i_2 = \frac{j\omega M}{Z_{22}} i_1 \tag{5.5}$$

the source voltage (v_S) can be found by substituting (5.5) into the mesh 1 equation in (5.2) as

$$v_S = \frac{Z_{11} Z_{22} + \omega^2 M^2}{Z_{22}} i_1 = \left(Z_{11} + \frac{\omega^2 M^2}{Z_{22}} \right) i_1 \tag{5.6}$$

where Z_S is ignored in this calculation for simplicity. From (5.6), the mesh 1 current can be written with respect to v_S as

$$i_1 = \frac{Z_{22}}{Z_{11}Z_{22} + \omega^2 M^2} v_S \tag{5.7}$$

from which the impedance looking into the primary coil can be found to be

$$\begin{aligned} Z_{IN,P} &= \frac{v_S}{i_1} \\ &= Z_{11} + \frac{\omega^2 M^2}{Z_{22}} - Z_S \\ &= j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + Z_L}. \end{aligned} \tag{5.8}$$

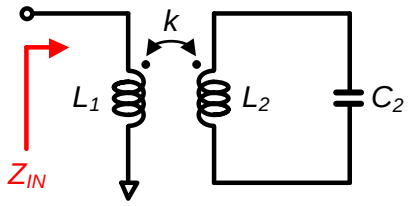


Fig. 5.8. TCR replacing inductor in shunt to signal path.

Fig. 5.8 shows the transformer-coupled resonator with the one end of the primary inductor grounded. The input impedance of TCR (Z_{IN}) can be found by substituting $Z_L = 1/j\omega C_2$ into (5.8) as

$$\begin{aligned} Z_{IN} &= j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + 1/j\omega C_2} \\ &= j\omega L_1 + j\omega \frac{\omega^2 M^2 C_2}{1 - \omega^2 L_2 C_2} \end{aligned} \tag{5.9}$$

which becomes zero when

$$\omega^2 = \frac{L_1}{C_2\left(L_1 L_2 - M^2\right)}. \tag{5.10}$$

Therefore, when connected in shunt to the signal path, the TCR as shown in Fig. 5.8 can

be used to replace the shunt inductor and behave as a frequency trap with the resonant frequency of

$$\begin{aligned} f_r &= \frac{1}{2\pi}\sqrt{\frac{L_1}{C_2\left(1-k^2\right)L_1L_2}} \\ &= \frac{1}{2\pi}\sqrt{\frac{1}{L_2C_2}}\cdot\frac{1}{\sqrt{1-k^2}} \\ &= f_{r2}\cdot\frac{1}{\sqrt{1-k^2}} \end{aligned} \tag{5.11}$$

where f_{r2} is the resonant frequency set by L_2 and C_2. (5.11) implies that the series resonant frequency of the shunt TCR can be set by properly choosing the resonant frequency of the resonator in the secondary side and the coupling factor of the transformer. In this design, the TCR marked as 36-GHz trap 1 in Fig. 5.5 is realized using the configuration shown in Fig. 5.8 having f_r = 36 GHz and replaces a fairly large shunt inductor used for the wideband amplifier design.

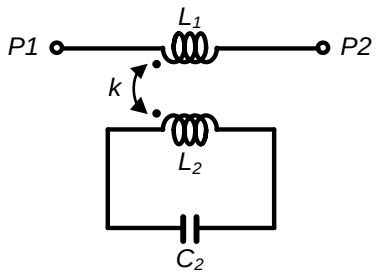


Fig. 5.9. TCR replacing inductor in series with signal path.

On the other hand, if the TCR is in the configuration as in Fig. 5.9, it replaces a series inductor and can be designed to block the transmission of either one of the IM

products at 36 GHz or 84 GHz as explained below. Using the expression of Z_{IN} in (5.9), the *ABCD*-matrix of the TCR in Fig. 5.9 can be written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z_{IN,P} \\ 0 & 1 \end{bmatrix} \tag{5.12}$$

Then, the transmission coefficient (S_{21}) can be found by using the conversion from *ABCD*- to *S*-parameters as [38]

$$S_{21} = \frac{2}{A + \frac{B}{Z_o} + CZ_o + D} \tag{5.13}$$

where Z_o is 50 Ω. Substituting the *ABCD*-parameters in (5.12) into (5.13) gives

$$S_{21} = \frac{100}{100 + j\omega L_1 + j\omega \frac{\omega^2 M^2 C_2}{1 - \omega^2 L_2 C_2}} \tag{5.14}$$

which becomes very small when

$$\omega = 1/\sqrt{L_2 C_2}\,. \tag{5.15}$$

In this dual-band VGA design, three TCRs (36-GHz Block 1, 84-GHz Block 1 and 2 as marked in Fig. 5.5) in the configuration shown in Fig. 5.9 replace the three series inductors used for wideband design.

Several assumptions are made in order to simplify the analysis in this subsection. While not being very precise, the analysis gives an idea how TCRs can be used in place of inductors to suppress the unwanted direct IM products. In real designs, a TCR has fairly low quality factor and hence limited rejection performance. However, the rejection performance can be improved by replacing as many inductors with TCRs as possible.

5.2.3 Minimization of Phase Variation over Gain Tuning Process

RF gain control can generally be achieved by the conventional current-steering method as shown in Fig. 5.10. The gain control transistor (Q_{GC}) steers the dc current of the cascode device (Q_2) by tuning the base bias voltage, V_{GC}. It can be understood by applying KCL at the collector terminal of Q_1 as

$$I_{Q1} = I_{Q2} + I_{QGC}. \tag{5.16}$$

When V_{GC} is very low, then Q_{GC} remains turned off and hence all the dc current of Q_1 flows through Q_2 (i.e. $I_{Q1} = I_{Q2}$), which leads to the maximum gain state. As V_{GC} is increased, however, Q_{GC} starts to draw some fraction of I_{Q1}, which results in a reduction in the gain. When V_{GC} is further increased, Q_{GC} steerss all I_{Q1} and therefore the gain becomes zero or even negative as no current flows in Q_2.

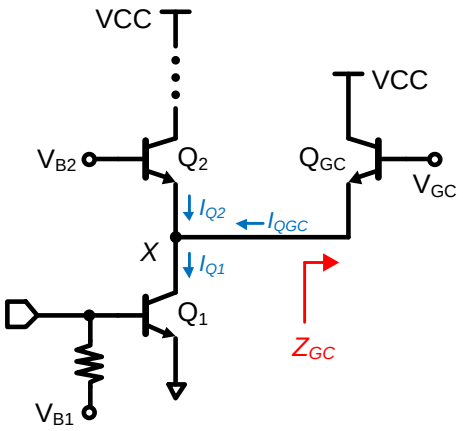
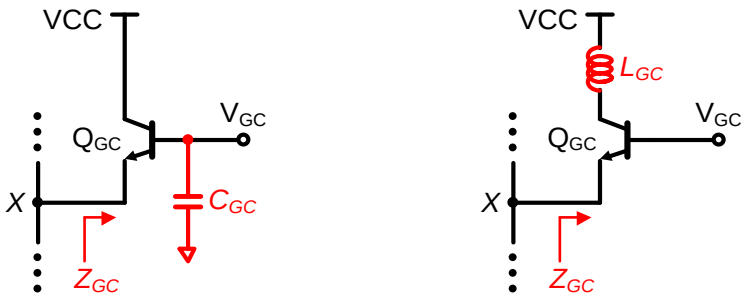


Fig. 5.10. Gain control using current-steering technique.

While seeming quite simple and straightforward, gain tuning through the current-steering technique exhibits fairly large variation in the phase of transmission gain (S_{21}) when the gain is tuned. As the primary source for the large phase variation is the

dependence of the base-emitter capacitance of Q_{GC} (C_{be}) on V_{GC}, the best way to reduce the phase variation is to mitigate the effect of C_{be} on the phase of S_{21} in the course of gain tuning. One way is to add a very small shunt capacitor (C_{GC}) at the base of Q_{GC} as shown in Fig. 5.11(a) [39], which is connected in series with C_{be} in the small-signal equivalent circuit. Then, the total effective capacitance seen from the emitter of Q_{GC} to the ground is dominated by C_{GC}, which is very small. Therefore, the dependence of the phase of S_{21} on C_{be} and hence on V_{GC} is reduced while the implementation of such a small capacitor in shunt with the base terminal of Q_{GC} is quite challenging.



(a) (b)

Fig. 5.11. Techniques to reduce phase variation by (a) adding a small capacitor (C_{GC}) in shunt with base of Q_{GC} and (b) adding an inductor (L_{GC}) in series with collector of Q_{GC}.

As an alternative, adding an inductor (L_{GC}) in series with the collector of Q_{GC} as shown in Fig. 5.11(b) can also reduce the phase variation. If the base-collector capacitor (C_{bc}) is neglected, L_{GC} has no effect on Z_{GC}. At very high frequencies, however, C_{bc} creates a path between the emitter and the collector. Hence, L_{GC} contributes to Z_{GC} by adding the positive imaginary part, which in part cancels the negative imaginary part dominated by C_{be}, and hence soothe the dependence of the phase on C_{be} variation.

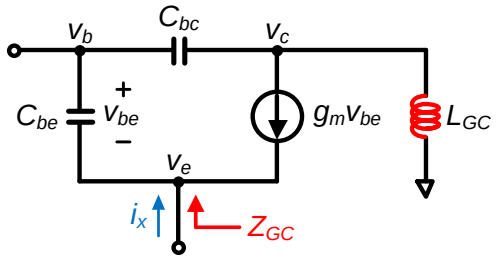


Fig. 5.12. Small-signal equivalent circuit model of the proposed current-steering cell shown in Fig. 5.11(b).

In order to validate how L_{GC} helps reduce the phase variation, Z_{GC} can be obtained from the small-signal equivalent model as shown in Fig. 5.12. Applying KCL at the emitter,

$$\begin{aligned} i_x &= j\omega C_{be}(v_e - v_b) + g_m(v_e - v_b) \\ &= (g_m + j\omega C_{be})v_e - (g_m + j\omega C_{be})v_b \end{aligned} \tag{5.17}$$

The base voltage, v_b, can be obtained by the voltage division by C_{be} and C_{bc} between v_c and v_e as

$$v_b = \frac{C_{bc}}{C_{be} + C_{bc}}(v_c - v_e) \tag{5.18}$$

where v_c can be expressed as

$$v_c = j\omega L_{GC} \cdot i_x. \tag{5.19}$$

Substituting (5.19) into (5.18) and then the resultant (5.18) into (5.17) gives

$$\left[1 + (g_m + j\omega C_{be})\frac{C_{bc}}{C_{be}+C_{bc}} j\omega L_{GC}\right] i_x = (g_m + j\omega C_{be}) \cdot \left(1 + \frac{C_{bc}}{C_{be}+C_{bc}}\right) v_e. \tag{5.20}$$

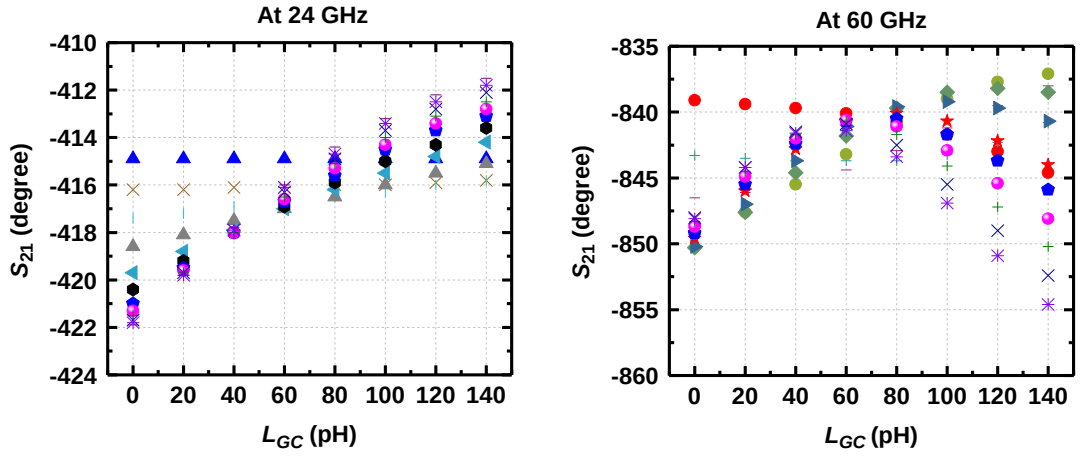
Then, the impedance looking into the current-steering cell (Z_{GC}) can be found to be

$$Z_{GC} = \frac{v_e}{i_x} = \frac{1}{1+\dfrac{C_{bc}}{C_{be}+C_{bc}}} \cdot \left[\frac{1}{g_m + j\omega C_{be}} + \frac{C_{bc}}{C_{be}+C_{bc}}\, j\omega L_{GC} \right]. \qquad (5.21)$$

As can be deduced from (5.21), L_{GC} neutralizes the combined effect of C_{be} and g_m of Q_{GC} (the first term in the bracket) by introducing the positive imaginary part in Z_{GC}, and hence reduces their effect on the phase variationas as the gain is tuned. Note that if L_{GC} is too large, the imaginary part in the bracket becomes excessively positive and the phase variation increases. Therefore, L_{GC} should be chosen a bit smaller than the optimum value for the lowest phase variation. Moreover, it is also advantageous in regards to the layout. The dc pad supplying VCC is normally a few tens or hundreds of micro-meters away from the active circuit area and therefore the collector of Q_{GC} needs to be routed to the dc pad through the metal line anyways. That is, L_{GC} can not only help reduce the phase variation but also be used as the routing to the dc pad for biasing of the collector of Q_{GC}.

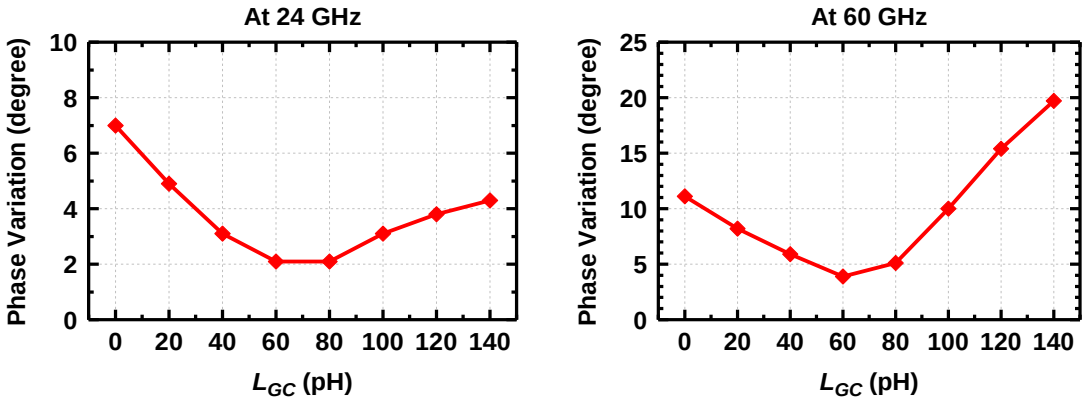
Fig. 5.13 plots the phases of S_{21} for all the gain states over the tuning range versus different L_{GC} values at 24 and 60 GHz. As can be seen from both Figs. 5.13(a) and (b), the phases of S_{21} both at 24 and 60 GHz with L_{GC} between 40 pH to 80 pH tend to show much less variation over the gain tuning process than those with no L_{GC}. At 24 GHz, as shown in Fig. 5.14(a), the minimum phase variation of 2.2º can be achieved when can be achieved L_{GC} = 60 pH. At 60 GHz, the minimum phase variation occurs when L_{GC} = 60 pH, of which value is 4.2º as shown in Fig. 5.14(b). Therefore, for the selected Q_{GC} in this design, it can be concluded that the phase variation of S_{21} over the

entire gain tuning process can be significantly reduced both at 24 and 60 GHz by choosing L_{GC} = 60 pH compared to the case without L_{GC}.



(a) (b)

Fig. 5.13. Phases of S_{21} for all gain states versus L_{GC} at (a) 24 GHz and (b) 60 GHz.



(a) (b)

Fig. 5.14. Phase variation over whole gain tuning range versus L_{GC} at (a) 24 GHz and (b) 60 GHz.

5.3 Simulated Results and Discussion

The final layout of the designed K-/V-band RF VGA is shown in Fig. 5.15. The area including all the test pads is 1.3 mm × 0.76 mm, where the horizontal dimension is set by the size of the DC pad with six power pins, while the active core area is 0.65 mm × 0.35 mm. From 1.8-V supply, it only consumes 8.4 mA DC current (P_{DC} = 15.1 mW).

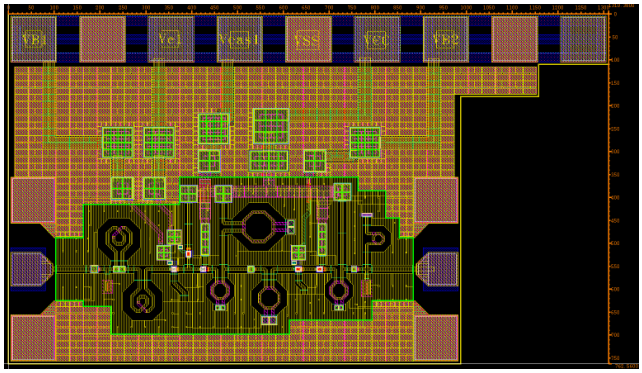
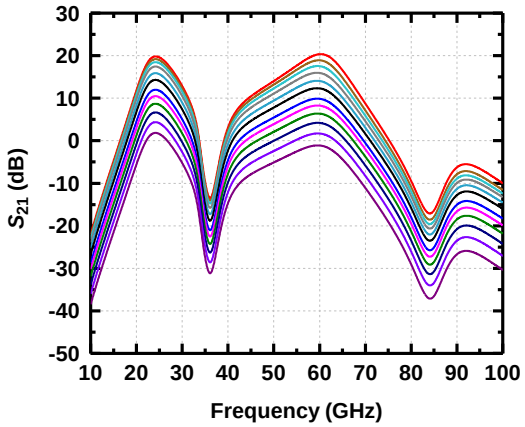
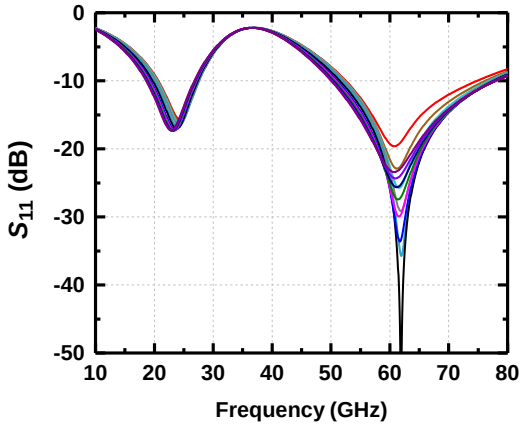


Fig. 5.15. Final layout of the designed K-/V-band RF VGA.

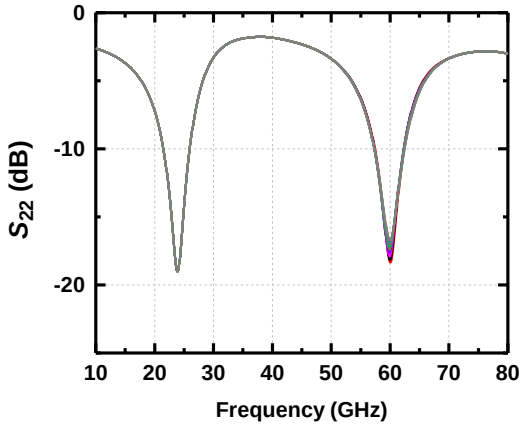
Fig. 5.16 shows the simulated *S*-parameters for all the different gain states. As shown in Fig. 5.16(a), the maximum gains at 24 GHz and 60 GHz are 19.8 dB and 20.2 dB, respectively, while the gain tuning ranges are from 1.2 to 19.8 dB at 24 GHz and from -0.8 to 20.2 dB at 60 GHz. The rejection levels at 36 GHz and 84 GHz are maintained to be lower than 30 dB with referenced to the gain levels at 24 GHz and 60 GHz. Input and output return losses plotted in Fig. 5.16(b) and (c) show good matching performances at both passbands and they are well preserved over the entire gain tuning process.



(a)



(b)

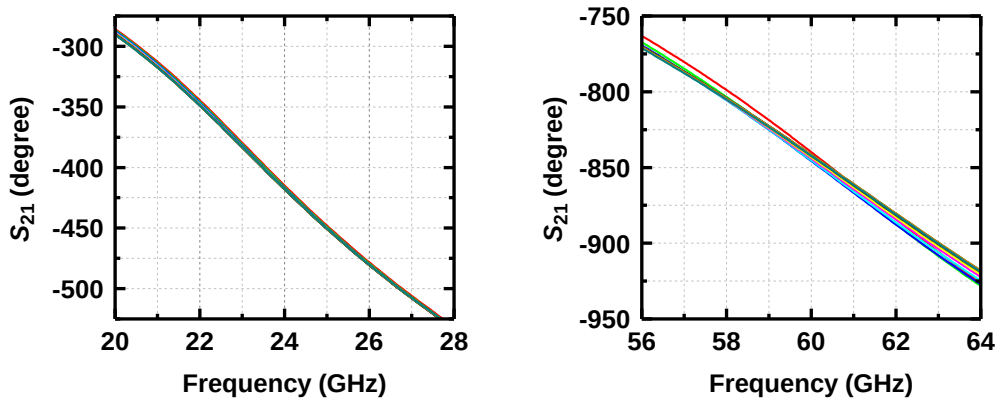


(c)

Fig. 5.16. Simulated *S*-parameters for all different gain states.

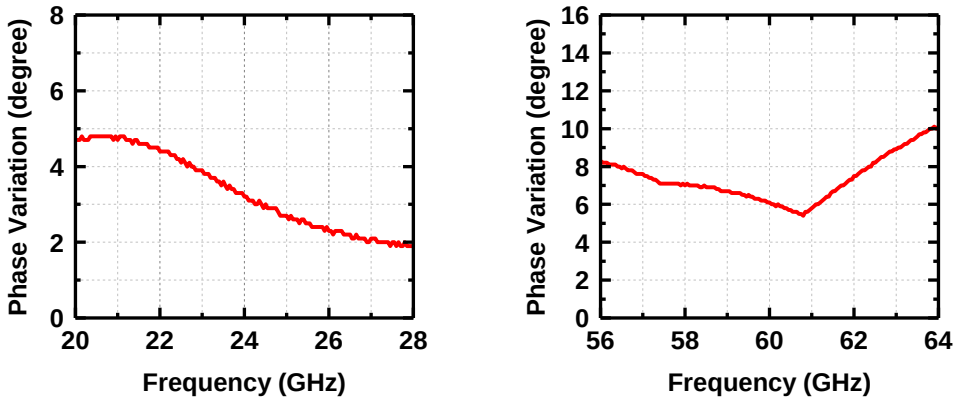
Fig. 5.17 plots the simulated phases of S_{21} for all the gain states in both lower (20 GHz to 28 GHz) and upper (56 GHz to 64 GHz) passbands, which confirms very small phase variations of 3.2° and 6° at 24 GHz and 60 GHz, respectively, over the gain tuning range of about 20-dB. From the plots of the phase variations versus frequency as shown

in Fig. 5.18, the phase variation ranges from 2º to 4.8º in the lower passband while it is from 5.3º to 10º in the upper passband.



(a) (b)

Fig. 5.17. Simulated phases of S_{21} for all gain states in (a) lower and (b) upper passbands.

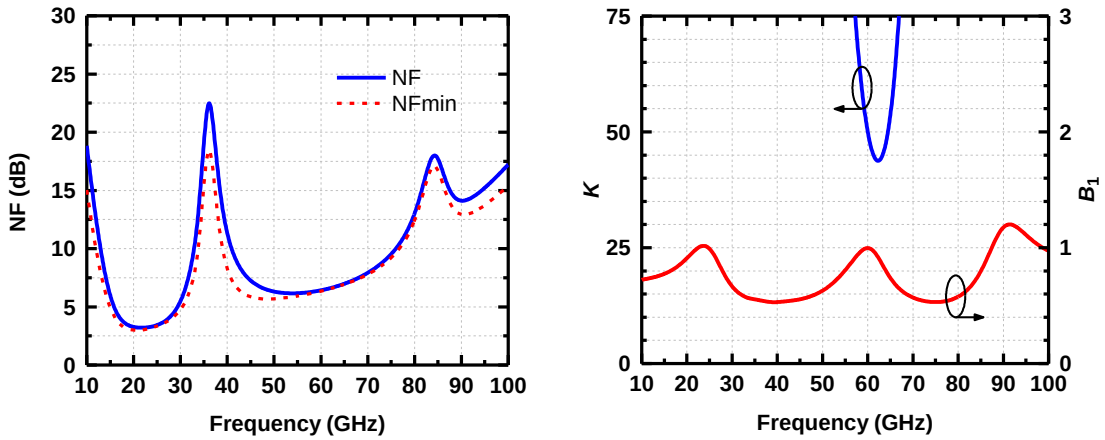


(a) (b)

Fig. 5.18. Phase variation in S_{21} versus frequency in (a) lower and (b) upper passbands.

The simulated noise figures at the maximum gain state are plotted in Fig. 5.19(a). At 24 GHz and 60 GHz, the lowest NFs are obtained to be 3.2 dB and 6.1 dB, respectively, where they are very close to the minimum achievable noise figures

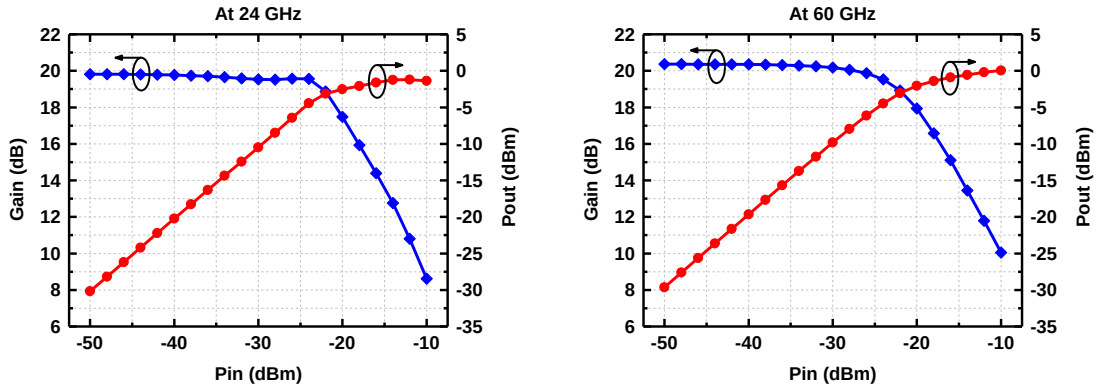
(NFmin). The stability factor (K) and stability measure (B_1) are shown in Fig. 5.19(b), confirming the unconditional stability by satisfying the conditions in (4.14).



(a) (b)

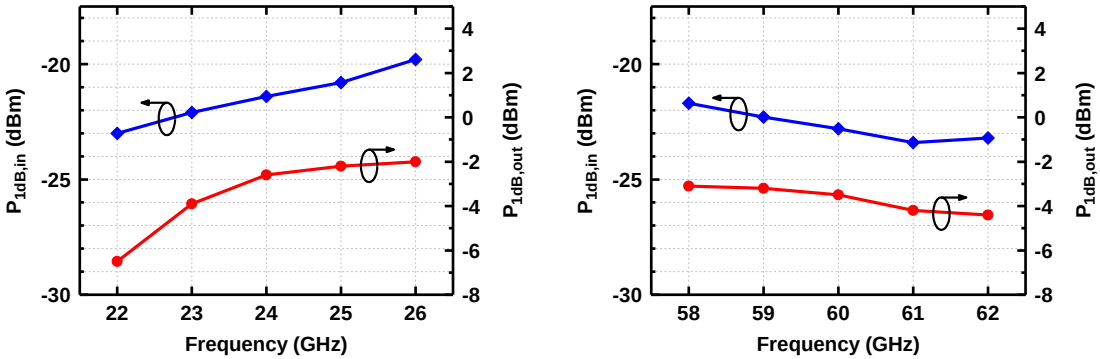
Fig. 5.19. Simulated (a) noise figure and (b) stability factors at maximum gain state.

Large-signal simulations are conducted to check the linearity performances of the dual-band VGA with concurrent dual-tone input (24 GHz and 60 GHz) as well as single-tone input (24 GHz or 60 GHz at a time). Fig. 5.20(a) and (b) plot the power gains and output powers versus input power with the single-tone inputs at 24 GHz and 60 GHz, respectively. With the single-tone input at 24 GHz, the input and output 1-dB compression points ($P_{1dB,in}$ and $P_{1dB,out}$) are -21.5 dBm and -2.5 dBm, respectively, as shown in Fig. 5.19(a). When 60-GHz signal is applied alone, $P_{1dB,in}$ and $P_{1dB,out}$ are read to be -22.8 dBm and -3.5 dBm, respectively, as plotted in Fig. 5.20(b). The large-signal performances of the dual-band amplifier with single-tone input both at 24 GHz and 60 GHz are very similar to those obtainable from the low-power single-band amplifiers for the receiver front-ends operating either at 24 GHz or 60 GHz.



(a) (b)

Fig. 5.20. Simulated forward gain and output power versus input power with single tone input at (a) 24 GHz and (b) 60 GHz.



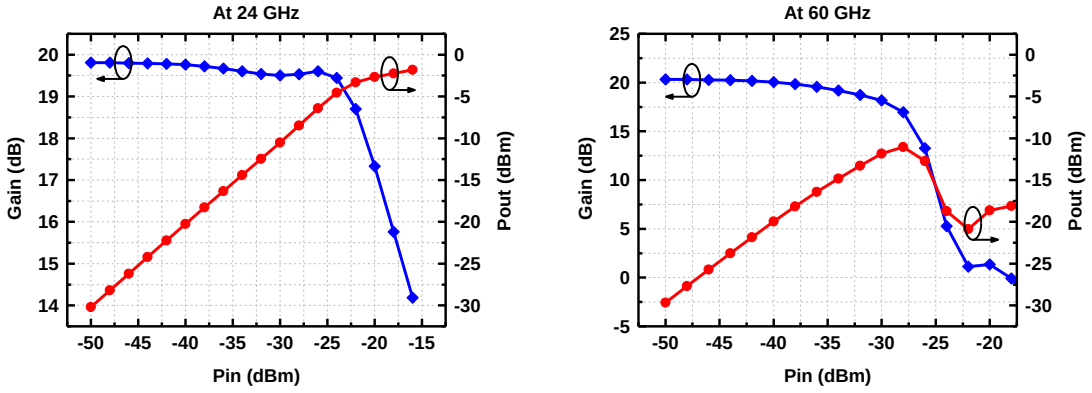
(a) (b)

Fig. 5.21. Simulated input and output P_{1dB} versus frequency at (a) lower passband and (b) upper passband.

The input and output 1-dB compression points (P_{1dB}s) are also plotted versus frequency as shown in Fig. 5.21. Within the frequency range from 22 GHz to 26 GHz, $P_{1dB,in}$ and $P_{1dB,out}$ range from -23 dBm to -20 dBm and from -6.5 dBm to -2 dBm, respectively, showing gentle increase along with the frequency as shown in Fig. 5.21(a). On the other hand, $P_{1dB,in}$ and $P_{1dB,out}$ are plotted versus frequencies between 58 GHz to

62 GHz as shown in Fig. 5.21(b), which range from -21.8 dBm to -23.2 dBm and from -3.2 dBm to -4.4 dbm, respectively, maintaining the relatively constant $P_{1dB,out}$ within the frequency range.

Fig. 5.22 shows the simulated large-signal performance when the concurrent two tones at 24 GHz and 60 GHz are applied. Fig. 5.22(a) plots the gain and the output power measured at 24 GHz versus input power, from which $P_{1dB,in}$ and $P_{1dB,out}$ are read to be -22.6 dBm and -3.8 dBm, respectively. While showing slight degradation, the performance is comparable to the case with 24-GHz single-tone input as shown in Fig. 5.20(a). The gain and the output power measured at 60 GHz versus input power are plotted in Fig. 5.22(b).



(a) (b)

Fig. 5.22. Simulated forward gain and output power versus input power measured at (a) 24 GHz and (b) 60 GHz with concurrent dual-tone input of 24 and 60 GHz.

As can be seen, gain compression starts occurring at low input power and the output power starts decreasing for the input power higher than -27.5 dBm. With the concurrent dual-tone input at 24 GHz and 60 GHz, it seems by inspection that the

existence of 24-GHz signal has much more adverse effects on 60-GHz signal at the output. This bizarre result agrees with the measured results shown in Fig. 4.22 of CHAPTER IV (measured at upper tone with two-tone input) while the exact cause of this symptom needs more thorough investigations.

The simulated performances of the designed concurrent K-/V-band RF VGA are summarized in Table 5.1. Except for the unexpected large-signal performance measured at 60 GHz with the concurrent dual-tone input, all other performances are comparable to those obtainable from low-power single-band amplifiers designed for the receiver front-ends operating at either at 24 GHz or 60 GHz.

5.4 Summary and Conclusion

A concurrent K-/V-band RF VGA implemented in 0.18-μm SiGe BiCMOS process is presented in this chapter. Starting from the wideband design, all the possible inductors are replaced with TCRs in order not only to create the two distinct passbands but also to suppress the direct IM products as much as possible. By doing this, the layout footprint of the dual-band amplifier can be kept within the layout footprint required for the single-band counterparts operating either at K- or V-bands. The designed dual-band RF VGA achieves about 20-dB gain tuning range both at 24 GHz and 60 GHz while the phase variations in the transmission gain are kept very small due to the proposed technique to reduce the phase variation in the course of gain tunings.

Table 5.1 Simulated performance summary of concurrent K-/V-band RF VGA

	24 GHz (K-band)	**60 GHz (V-band)**
$S_{21,max}$ **(dB)**	19.8	20.2
$S_{11,max}$ **(dB)**	-15.5	-19.5
$S_{22,max}$ **(dB)**	-19.2	-18.9
Gain Tuning Range (dB)	1.2 ~ 19.8	-0.8 ~ 20.2
Phase Variation (º)	3.2	6
NF (dB) (at max gain)	3.2	6.1
$P_{1dB,in}$ **(dBm) (Single-tone)**	-21.5	-22.8
$P_{1dB,in}$ **(dBm) (Dual-tone)**	-22.6	-27.5
DC Power (mW)	15.1 (8.4 mA at 1.8-V supply)	

CHAPTER VI

CONCLUSION

While mm-wave frequencies seem to be the most probable candidate for the next generation of communications, they inherently have many drawbacks to be overcome such as maximum achievable gain, dc power, noise figure, output power, substrate loss, etc. when it comes to the realization and integration in Silicon. This dissertation is focused on the efficient design techniques for mm-wave transceiver front-end ICs using SiGe BiCMOS process.

In Chapter II, a 60-GHz active OOK/pulse modulator featuring the high ON/OFF isolation is presented. By incorporating with the switched-impedance cell, the designed modulator achieves 36.5-dB OFF-state isolation and 11.5-dB ON-state forward gain, resulting in very high ON/OFF isolation of 48 dB. As verified from the time domain measurements, the modulator can handle the pulses with the pulse width of as narrow as 400 ps as a pulse modulator or equivalently it can support up to 2.5-Gbps data rate when used as an OOK modulator. Realized in a 0.18-μ*m* SiGe BiCMOS process, the core chip size is measured to be 0.4 mm by 0.28 mm. While consuming only 4.5 mA at 1.8-V supply voltage, the input and output 1-dB compression points are -12.5 dBm and -1.5 dBm, respectively, which can also replace one of the PA driver stages and hence lead to dc power saving.

In Chapter III, a large gain-bandwidth power-efficient LNA operating at V-band is introduced. A wideband gain shaping technique achieved by the collaboration between

the first and second inter-stage matching networks both realized by *T*-type matching is applied for gain enhancement over very wide bandwidth. Realized in a 0.18-μm SiGe BiCMOS process, the core chip size of the LNA is measured to be 0.65 mm and 0.6 mm. The designed LNA achieves the measured gain higher than 29.5 dB across the wide 3-dB bandwidth from 43 to 67 GHz with the peak measured gain of 32.5 dB at 61 GHz while consuming only 6.5 mA at 1.8-V supply voltage (P_{DC} = 11.7 mW). The designed LNA shows the highest gain-bandwidth product per unit dc power consumption among the published wideband LNA operating at mm-wave frequencies.

In Chapter IV, a concurrent K-/V-band LNA is presented. The design features the simultaneous achievement of the direct IM product / harmonic rejection and dual-band input matching through the collaboration between the 36-GHz trap/ 48-GHz block network and Miller effect. Consequently, the dual-band input matching is achieved by employing only one physical inductor at the input while at least two physical inductors are necessary for dual-resonance. The designed dual-band LNA achieves good gain balance between the two passbands while the rejections at 36 GHz and 48 GHz are higher than 30 dB with referenced to the peak gain levels of the two passbands. Fabricated in a 0.18-μm SiGe BiCMOS process, the designed dual-band LNA occupies 0.7 mm by 0.36 mm without the test pads while it consumes only 8-mA dc current at 1.8-V supply voltage (P_{DC} = 14.4 mW), which confirms the comparable size and dc power consumption to the single-band counterparts designed to operate either at K- or V-band.

In Chapter V, the development of a concurrent K-/V-band RF VGA starting from a wideband amplifier design is presented. One of the two main objectives is to suppress the two most critical direct IM products between the two fundamental tones at 24 GHz and 60 GHz as much as possible without increasing the chip size, which was achieved by replacing as many inductors used in the wideband design as possible with TCRs. In the proposed design, four inductors are replaced with TCRs, where each TCR is to resonate at one of frequencies of the direct IM products (either 36 GHz or 84 GHz) depending on the original spiral inductor's footprint size. By doing so, the suppression level higher than 35 dBc is achieved both at 36 GHz and 84 GHz for the maximum gain state. The other main objective is to reduce the phase variation in the course of gain tuning. While the gain tuning by the conventional current-steering shows large phase variation, the designed VGA achieved very small phase variations of 3.2º and 6º over 20-dB gain control range at 24 GHz and 60 GHz, respectively.

REFERENCES

[1] Christian Wolff, *Radar Basics*, Available: www.radartutorial.eu

[2] C. Hyunh, "Millmeter-wave concurrent dual-band BiCMOS RFIC transmitter for radar and communication systems," Ph.D. Dissertation, Texas A&M University, College Station, TX, USA, Dec. 2012.

[3] U. Yodprasit, C. Carta, and F. Ellinger, "20-Gbps 60-GHz OOK modulator in SiGe BiCMOS technology," in *Int. Symp. Signals, Systs, and Electron.,* Oct. 2012, pp. 1-5.

[4] J. J. Lee and C. S. Park, "60-GHz gigabits-per-second OOK modulator with high output power in 90-nm CMOS," *IEEE Trans. Circuits Syst. II: Expr. Briefs,* vol. 58, no. 5, pp. 249-253, May 2011.

[5] W. Shin, M. Uzunkol, R. A. Alhalabi, and G. M. Rebeiz, "60 GHz low power 1.5 Gb/s ASK transmitter in 90 nm CMOS with on-board Yagi-Uda antenna," in *European Microwave Conf.*, Sep. 2010, pp. 272-275.

[6] A. Oncu, K. Takano, and M. Fujishima, "8Gbps CMOS ASK modulator for 60GHz wireless communication," in *IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 125-128.

[7] A. Hamidian, A. Malignaggi, R. Shu, A. M. Kamal, and G. Boeck, "Multi-gigabit 60 GHz OOK front-end in 90 nm CMOS," in *IEEE Top. Meeting Silicon Monolithic Integr. Circuits in RF Systems (SiRF)*, Jan. 2013, pp. 96-98.

[8] X. Yu, S. P. Sah, H. Rashtian, S. Mirabbasi, P. P. Pande, and D. Heo, "A 1.2-pJ/bit 16-Gb/s 60-GHz OOK transmitter in 65-nm CMOS for wireless network-on-chip," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2357-2369, Oct. 2014.

[9] F. Zhu, W. Hong, W. F. Liang, J. X. Chen, X. Jiang, P. P. Yan, *et al.*, "A low-power low-cost 45-GHz OOK transceiver system in 90-nm CMOS for multi-Gb/s transmission," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2105-2117, Aug. 2014.

[10] Z. He, T. Swahn, Y. Li, and H. Zirath, "A 14 Gbps On-/Off- keying modulator in GaAs HBT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 5, pp. 272-274, May 2012.

[11] E. Preisler, G. Talor, D. Howard, Z. Yan, R. Booth, J. Zheng, *et al.*, "A millimeter-wave capable SiGe BiCMOS process with 270GHz f_{max} HBTs designed for high volume manufacturing," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2011, pp. 74-78.

[12] H. H. Hsieh, P. Y. Wu, C. P. Jou, F. L. Hsueh, and G. W. Huang, "60GHz high-gain low-noise amplifiers with a common-gate inductive feedback in 65nm CMOS," in *IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, Jun. 2011, pp. 1-4.

[13] C. C. Huang, H. C. Kuo, T. H. Huang, and H. R. Chuang, "Low-power, high-gain V-band CMOS low noise amplifier for microwave radiometer applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 2, pp. 104-106, Feb. 2011.

[14] F. Vecchi, S. Bozzola, E. Temporiti, D. Guermandi, M. Pozzoni, M. Repossi, *et al.*, "A wideband receiver for multi-Gbit/s communications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 551-561, Mar. 2011.

[15] N. Li, K. Bunsen, N. Takayama, Q. Bu, T. Suzuki, M. Sato, *et al.*, "A 24 dB gain 51-68 GHz CMOS low noise amplifier using asymmetric-layout transistors," in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2010, pp. 342-345.

[16] Q. Bu, N. Li, K. Okada, and A. Matsuzawa, "A wideband LNA with an excellent gain flatness for 60 GHz 16QAM modulation in 65 nm CMOS," in *Asia-Pacific Microw. Conf.*, Dec. 2011, pp. 359-362.

[17] R. Sananes and E. Socher, "52-75 GHz wideband low-noise amplifier in 90 nm CMOS technology," *Electron. Lett.*, vol. 48, no. 2, pp. 71-72, Jan. 2012.

[18] V. Bhagavatula, M. Taghivand, and J. C. Rudell, "A compact 24-54 GHz CMOS band-pass distributed amplifier for high fractional bandwidth signal amplification," in *IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, Jun. 2014, pp. 71-74.

[19] H. C. Yeh, C. C. Chiong, S. Aloui, and H. Wang, "Analysis and design of millimeter-wave low-voltage CMOS cascode LNA with magnetic coupled technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4066-4079, Dec. 2012.

[20] A. Y. K. Chen, Y. Baeyens, Y. K. Chen, and J. Lin, "A low-power linear SiGe BiCMOS low-noise amplifier for millimeter-wave active imaging," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 103-105, Feb. 2010.

[21] *IE3D, HyperLynx 3-D EM. Mentor Graphics.* Available: http://www.mentor.com/pcb/hyperlynx/3d-em/

[22] G. Liu and H. Schumacher, "Broadband millimeter-wave LNAs (47-77 GHz and 70-140 GHz) using a T-type matching topology," *IEEE J. Solid-State Circuits,* vol. 48, no. 9, pp. 2022-2029, Sep. 2013.

[23] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1997.

[24] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits,* vol. 33, no. 12, pp. 2178-2185, Dec. 1998.

[25] F. Ken Leong, "Dual-band high-linearity variable-gain low-noise amplifiers for wireless applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* Feb. 1999, pp. 224-225.

[26] J. Ryynanen, K. Kivekas, J. Jussila, A. Parssinen, and K. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," in *IEEE Custom Integr. Circuits Conf. (CICC),* May. 2000, pp. 175-178.

[27] H. Hashemi and A. Hajimiri, "Concurrent dual-band CMOS low noise amplifiers and receiver architectures," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2001, pp. 247-250.

[28] C. Huynh and C. Nguyen, "New technique for synthesizing concurrent dual-band impedance-matching filtering networks and 0.18-μm SiGe BiCMOS 25.5/37-

GHz concurrent dual-band power amplifier," *IEEE Trans. Microw. Theory Techn.,* vol. 61, no. 11, pp. 3927-3939, Sep. 2013.

[29] K. A. Hsieh, H. S. Wu, K. H. Tsai, and C. K. C. Tzuang, "A dual-band 10/24-GHz amplifier design incorporating dual-frequency complex load matching," *IEEE Trans. Microw. Theory Techn.,* vol. 60, no. 6, pp. 1649-1657, 2012.

[30] S. Wang and C. Y. Xiao, "Concurrent 10.5/25 GHz CMOS power amplifier with harmonics and inter-modulation products suppression," *Electron. Lett.,* vol. 51, no. 14, pp. 1058-1059, Jul. 2015.

[31] J. Lee and C. Nguyen, "A concurrent tri-band low-noise amplifier with a novel tri-band load resonator employing feedback notches," *IEEE Trans. Microw. Theory Techn.,* vol. 61, no. 12, pp. 4195-4208, Nov. 2013.

[32] K. Kim and C. Nguyen, "A concurrent Ku/K/Ka tri-band distributed power amplifier with negative-resistance active notch using SiGe BiCMOS process," *IEEE Trans. Microw. Theory Techn.,* vol. 62, no. 1, pp. 125-136, Dec. 2014.

[33] J. M. Miller, "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit," *Sci. Pap. Bur. Stand,* vol. 15, no. 351, pp. 367-385, 1920.

[34] W. H. Cho and S. S. H. Hsu, "An ultra-low-power 24 GHz low-noise amplifier using 0.13 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.,* vol. 20, pp. 681-683, 2010.

[35] Y. L. Wei, S. S. H. Hsu, and J. D. Jin, "A low-power low-noise amplifier for K-band applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, pp. 116-118, 2009.

[36] J. H. Lee, C. C. Chen, and Y. S. Lin, "3.7 mW 24 GHz LNA with 10.1 dB gain and 4.5 dB NF in 0.18 μm CMOS technology," *Electron. Lett.*, vol. 46, pp. 1310-1312, 2010.

[37] C. W. Byeon, I. S. Song, S. J. Cho, H. Y. Kim, C. Lee, and C. S. Park, "A 60 GHz variable gain amplifier with a low phase imbalance in 0.18 μm SiGe BiCMOS technology," in *IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2012, pp. 1-4.

[38] D. M. Pozar, *Microwave Engineering, 4th ed.* . Hoboken, NJ, USA: John Wiley & Sons, Inc. , 2011.

[39] H. Chia-Yu, K. Jui-Chih, J. J. Kuo, and K. Y. Lin, "A 57-64 GHz low-phase-variation variable-gain amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1-3.

APPENDIX A

INPUT IMPEDANCE OF COMMON-EMITTER STAGE WITH DIFFERENT Z_L

Here, the expressions of the input impedance with four different special cases of Z_L (resistive, capacitive, inductive, and cascode loads) are examined and summarized in order to better illustrate the effect of the load condition on the input impedance through Miller effect. Note that only the load-dependent admittance (Y_M) in (4.8) is analyzed as Z_{BE} and C_{bc} in Z_{BC} are not dependent on the load, where it is rewritten from (4.8) as

$$Y_M = j\omega C_{bc}\left[\frac{g_m}{1+j\omega g_m L_E}\cdot\left(\frac{1}{j\omega C_{bc}+Y_L}\right)\right]. \tag{A.1}$$

A.1 Resistive Load

First of all, the load-dependent admittance (denoted as $Y_{M,R}$) for resistive load can be found by substituting $Z_L = R_L$ into (A.1) as

$$\begin{aligned} Y_{M,R} &= j\omega C_{bc}\left[\frac{g_m}{1+j\omega g_m L_E}\cdot\left(\frac{1}{j\omega C_{bc}+1/R_L}\right)\right] \\ &= \frac{j\omega C_{bc} g_m}{\left(1+j\omega g_m L_E\right)}\cdot\frac{R_L}{\left(1+j\omega C_{bc}R_L\right)} \\ &= j\omega C_{bc} g_m R_L \frac{\left(1-j\omega g_m L_E\right)\left(1-j\omega C_{bc}R_L\right)}{\left[1+\left(\omega g_m L_E\right)^2\right]\left[1+\left(\omega C_{bc}R_L\right)^2\right]} \end{aligned}$$

$$= \underbrace{\frac{\left(\omega C_{bc} g_m\right) R_L \left[\omega g_m L_E + \omega C_{bc} R_L\right]}{\left[1 + \left(\omega g_m L_E\right)^2\right]\left[1 + \left(\omega C_{bc} R_L\right)^2\right]}}_{Shunt\ G}$$

$$+ \underbrace{\frac{j\left(\omega C_{bc} g_m\right) R_L}{\left[1 + \left(\omega g_m L_E\right)^2\right]\left[1 + \left(\omega C_{bc} R_L\right)^2\right]}}_{Shunt\ C}$$

$$+ \underbrace{\frac{-j\left(\omega C_{bc} g_m\right)\left(\omega g_m L_E\right)\left(\omega C_{bc} R_L\right) R_L}{\left[1 + \left(\omega g_m L_E\right)^2\right]\left[1 + \left(\omega C_{bc} R_L\right)^2\right]}}_{Shunt\ L} \tag{A.2}$$

While complicated, it can be seen from (A.2) that the load-dependent admittance seen at the input is clearly the parallel combination of *G* (conductance), *L*, and *C* as shown in Fig. A.1(a).

A.2 Capacitive Load

When the load is capacitive (i.e. $Z_L = 1/j\omega C_L$), the load-dependent admittance ($Y_{M,C}$) can be found as

$$Y_{M,C} = j\omega C_{bc}\left[\frac{g_m}{1 + j\omega g_m L_E} \cdot \left(\frac{1}{j\omega C_{bc} + j\omega C_L}\right)\right]$$

$$= \frac{g_m\left(1 - j\omega g_m L_E\right)}{1 + \left(\omega g_m L_E\right)^2} \cdot \left(\frac{C_{bc}}{C_{bc} + C_L}\right)$$

$$= \underbrace{\frac{g_m}{1 + \left(\omega g_m L_E\right)^2} \cdot \left(\frac{C_{bc}}{C_{bc} + C_L}\right)}_{Shunt\ G}$$

$$+\underbrace{\frac{-j\omega g_m L_E}{1+\left(\omega g_m L_E\right)^2}\cdot\left(\frac{C_{bc}}{C_{bc}+C_L}\right)}_{Shunt\ L} \tag{A.3}$$

From (4.10), the load-dependent admittance with the capacitive load appears at the input as the parallel connection of *L* and *G* as shown in Fig. A.1(b).

A.3 Inductive Load

For the inductive load (i.e. $Z_L = j\omega L_L$), the load-dependent admittance denoted as $Y_{M,L}$ can be found to be

$$Y_{\mathrm{M},L} = j\omega C_{bc}\left[\frac{g_m}{1+j\omega g_m L_E}\cdot\left(\frac{1}{j\omega C_{bc}+1/j\omega L_L}\right)\right]$$

$$= \frac{j\omega C_{bc} g_m}{\left(1+j\omega g_m L_E\right)}\cdot\frac{j\omega L_L}{\left(1-\omega^2 C_{bc} L_L\right)}$$

$$= \frac{1-j\omega g_m L_E}{1+\left(\omega g_m L_E\right)^2}\cdot\left(\frac{\omega^2 C_{bc} g_m L_L}{\omega^2 C_{bc} L_L - 1}\right)$$

$$= \underbrace{\frac{-1}{1+\left(\omega g_m L_E\right)^2}\cdot\left(\frac{\omega^2 C_{bc} g_m L_L}{1-\omega^2 C_{bc} L_L}\right)}_{Negative\ Shunt\ G}$$

$$+\underbrace{\frac{j\omega g_m L_E}{1+\left(\omega g_m L_E\right)^2}\cdot\left(\frac{\omega^2 C_{bc} g_m L_L}{1-\omega^2 C_{bc} L_L}\right)}_{Shunt\ C} \tag{A.4}$$

from which the admittance seen at the input due to the inductive load is the parallel combination of G and C as shown in Fig. A.3. Note that the conductance is negative when $\omega < 1/\sqrt{L_L C_{bc}}$, which is normally the case.

A.4 Cascode Load

It is also worthwhile to examine the input impedance of cascode stage including Miller effect as it is one of the most widely used topologies for building amplifiers. For a general cascode stage with inductive degeneration, Z_L is the input impedance of the cascode device, which can be approximated to be $1/g_m$, assuming that the cascode device have the same transconductance as the input device. Then, the load-dependent admittance with the cascode load ($Y_{M,CAS}$) can be written as

$$Y_{M,CAS} = j\omega C_{bc}\left[\frac{g_m}{1 + j\omega g_m L_E}\cdot\left(\frac{1}{j\omega C_{bc} + g_m}\right)\right]. \tag{A.5}$$

As g_m can be generally assumed to be much larger than $j\omega C_{bc}$ at the design frequencies, (A.5) can be reduced to

$$\begin{aligned} Y_{M,CAS} &\approx \frac{j\omega C_{bc}}{1 + j\omega g_m L_E} \\ &= \underbrace{\frac{j\omega C_{bc}}{1 + \left(\omega g_m L_E\right)^2}}_{Shunt\ C} + \underbrace{\frac{\omega C_{bc}\cdot\left(\omega g_m L_E\right)}{1 + \left(\omega g_m L_E\right)^2}}_{Shunt\ G} \end{aligned} \tag{A.6}$$

which can be represented as the parallel combination of C and G as shown in Fig. A.1(d). For very large $\omega g_m L_E$, $Y_{M,CAS}$ approaches zero and its effect to the input

impedance can be ignored. For very small value of $\omega g_m L_E$, $Y_{M,CAS}$ becomes close to $j\omega C_{bc}$.

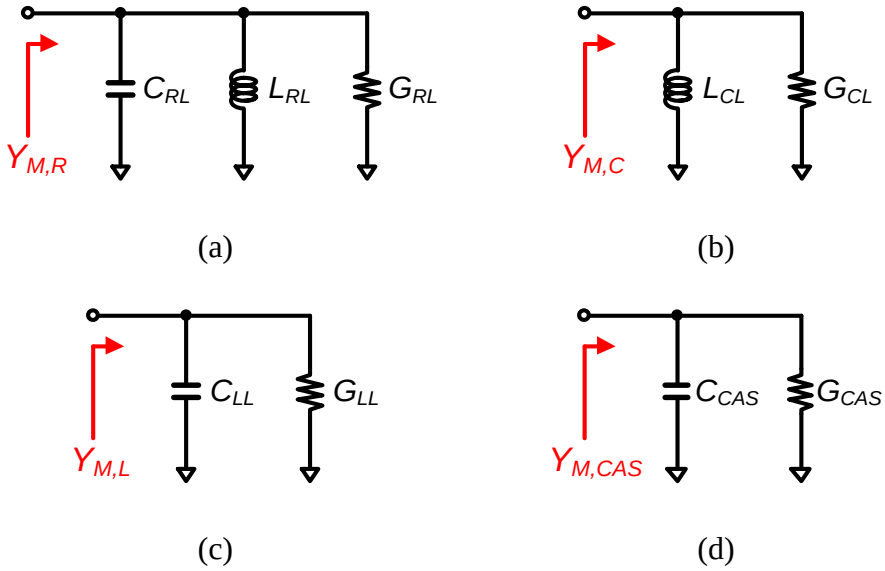


Fig. A.1. Equivalent networks representing Y_M with (a) resistive, (b) capacitive, (c) inductive, and (d) cascode loads.