A SUB-CENTIMETER RANGING PRECISION LIDAR SENSOR PROTOTYPE BASED ON ILO-TDC

A Thesis

by

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ABSTRACT

This thesis introduces a high-resolution light detection and ranging (LIDAR) sensor system-on-a-chip (SoC) that performs sub-centimeter ranging precision and maximally 124-meter ranging distance. With off-chip connected avalanche photo-diodes (APDs), the time-of-flight (ToF) are resolved through 31×1 time-correlated single photon counting (TCSPC) channels. Embedded time-to-digital converters (TDCs) support 52-ps time resolution and 14-bit dynamic range. A novel injection-locked oscillator (ILO) based TDC are proposed to minimize the power of fine TDC clock distribution, and improve time precision. The global PVT variation among ILO clock distribution is calibrated by an on-chip phase-looked-loop (PLL) that assures a reliable counting performance over wide operating range. The proposed LIDAR sensor is designed, fabricated, and tested in the 65nm CMOS technology. Whole SoC consumes 37mW and each TDC channel consumes 788μW at nominal operation. The proposed TDC design achieved single-shot precision of 38.5 ps, channel uniformity of 14 ps, and DNL/INL of 0.56/1.56 LSB, respectively. The performance of proposed ILO-TDC makes it an excellent candidate for global counting TCSPC in automotive LIDAR.

DEDICATION

To my beloved family

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NOMENCLATURE

ADC	Analog-to-Digital Converter
CML	Current-Mode Logic
CTDC	Coarse Time-to-Digital Converter
DFF	D Flip-Flop
DLL	Delay-Locked-Loop
DR	Dynamic Range
FLIM	Fluorescence Lifetime Imaging
FIR	finite impulse response
FTDC	Fine Phase Time-to-Digital Converter
GBW	Gain-Bandwidth Product
ILO	Injection-Looked Oscillator
JKFF	J-K Flip Flop
LIDAR	Light Detection and Ranging
PCB	Printed Circuit Board
PET	Positron-Emission Tomography
PLL	Phase-Looked-Loop
PMT	Photomultiplier Tube
PVT	Process Voltage and Temperature
RADAR	Radio Detection and Ranging
TCSPC	Time-Correlated Single Photon Counting
TDC	Time-to-Digital Converter
RO	Ring Oscillator

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1. INTRODUCTION

With the emerging growth of three-dimensional (3-D) enhanced computer vision, high-resolution 3-D image sensing technology has gained increasing interest recently. This sensing technology, capable of mapping the geometric information within the surrounding environment and collecting the data for the background analysis, is applied in several applications, including automotive, industrial, health-care and entertainment. In this context, light detection and ranging (LIDAR) with imaging capability or so-called time-of-flight (ToF) technology is one of the fast-growing classes in this field. Comparing with other 3-D imaging techniques such as millimeter-wave (MMW) radars [1], ultrasonic sensors [2], and stereo-vision cameras [3], LIDAR offers fast detection, high spacial resolution and reliable 3-D mapping in uncontrolled illuminance environment.

1.1 Applications: Automotive

With the force of national regulation, safety issue has become as important as fuel economy and engine performance in automotive market. A particular class of safety systems that are proposed among several tier-one car manufactures are so-called advanced driver assistance system (ADAS). This system is aimed at not only preventing traffic accidents in the first place, but also provides adaptive cruise control (ACC). Many features such as forward collision warning (FCW), autonomous emergency breaking (AEB), pedestrian detection, etc. are counted in this system. In the near future, ADAS will be incorporated into not only high-end car market, but the mid- and low-end.

Among several 3-D imaging techniques, MMW-radar remains the sensor of choice for now. MMW-radar has been widely used in conventional driving assistance to monitor vehicle driving environment. However, due to the limit of radar wavelength the angular resolution ($\theta = 1.22\lambda/D$ rad, where λ is the wavelength and D is the diameter of antenna) of MMW-radar is typically in the angle of 2° to 5° that is insufficient for some applications that need detail feature to identify remote sensing objects. To achieve desirable function, many automotive radars are usually combined with stereo-vision cameras in which the 3-D information is constructed from multiple 2-D image frames that were taken simultaneously from different viewing angles. Such technology usually utilizes low-cost CMOS imaging sensors (CISs) but demands intensive computing resources, process time, and power to reconstruct the 3-D information. Also, as stereo-vision camera is passive-mode sensor, it is sensitive to the ambient light condition and work poorly in low illuminance environment.

LIDAR, on the other hand, can offer higher spatial resolution due to the shorter optical wavelength. This characteristic allows LIDAR to detect smaller threaten objects in the environment such as wires, pillar, and defect on the road land. Also, the active optical source embedded in LIDAR provides reliable ranging detection under low background illuminance. The main challenge of automotive LIDAR sensor is the cost. To increase the signal-to-noise ratio (SNR), laser scanning approach is mostly utilized. This approach requires sophisticated mechanical and optical design so the cost is much higher than radar module. The challenges of reducing module complexity and driving down the cost will be the first priority in advanced LIDAR sensor. Undoubtedly, LIDAR will be prevalent in automotive industry in the near future. For example, LIDAR was applied in pseudo-cruise control and pedestrian detection in Texas Instrument's ADAS solutions guide in 2015 [4]. Meanwhile, many

car manufacturers such as Toyota and Nisson have started investigating LIDAR technique in their vehicles.

Autonomous driving, a more advanced driving system, is another fact that boosts the development of LIDAR in automotive industry. Comparing with ADAS, the autonomous driving system demands for higher resolution 3-D mapping and more sophisticated computer vision technique to identify different kinds of obstacles and navigate the car safely in the traffic environments. The high demand for the imaging quality makes LIDAR as a major sensor in autonomous vehicles. For instance, the Google's driverless car has a 64-beam laser scanning LIDAR mounted on the top. This LIDAR module provides central navigator a 360-degree 3-D vision.

1.2 Range Technique

As known as the optical radar, LIDAR measures the distance by timing how long a light to make a round trip between the senor and the object. The system usually contents two major components: 1) transmitter: an array of light-emitting diodes (LEDs) or laser diodes (LDs), and 2) receiver: a time-correlated single-photon counting (TCSPC). There are many variants of LIDAR systems. According to the modulation of light sources, these systems can be generally classified into two categories: pulse-based LIDAR [5, 6, 7, 8, 9] and modulation-based LIDAR [10, 11].

1.2.1 Pulse-based LIDAR

In pulse-based LIDAR sensors (Fig. 1.1), the transmitter emits single light pulse in a rapid frequency. As the light pulse hits remote objects (car, tree, or human being), it gets reflected. The travel time between the pulse being emitted

and then returning to the optical sensor is measured by the receiver, and so-called as time-of-flight (ToF). ToF time, along with the speed of light can be used to calculate the distance from the LIDAR module to objects:

$$d = \frac{c \cdot t_{TOF}}{2} \tag{1.1}$$

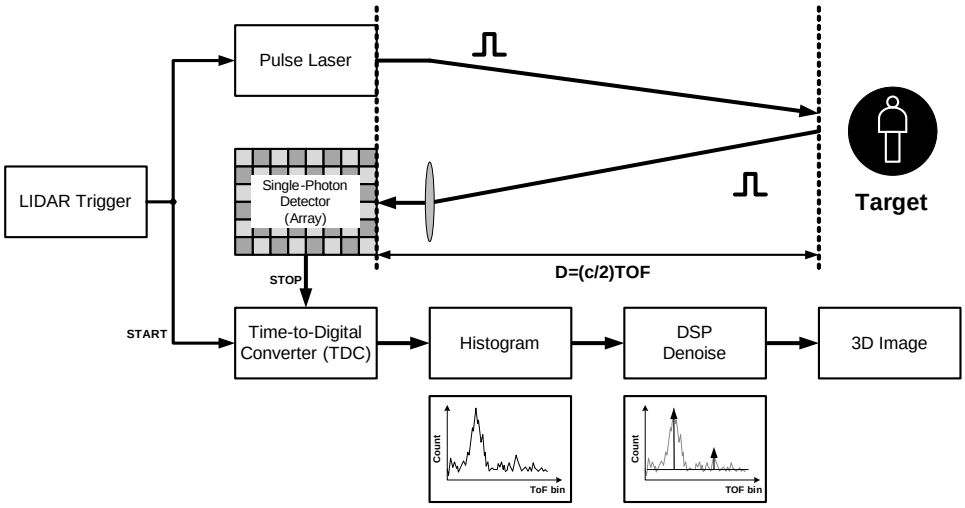

Figure 1.1: Pulse-based LIDAR sensor.

where c is the speed of light in air and the t_{TOF} is the round trip travel time. This approach seems straight-forward and the complexity of related optical design is low. However, the pixels in the sensor array have to be very sensitive to capture the low intensity of the returned pulse. Usually, single-photon-level sensitivity is needed in long-range application. Photomultiplier-tubes (PMTs) are traditional devices that are used as single-photon detector. However, PMTs require kilo-volt operating voltage, and device is so bulky that makes it hard to integrated as array-based sensor in a lite module size. This is also the reason why LIDAR is hard to be commercial-

ized in early ages. This bottleneck, fortunately, was been broken in the last decade with the progress in CMOS technology. Semiconductor photodiodes (PDs) such as avalanche photodiodes (APDs) and single-photon avalanche photodiodes (SPADs) are the alternative to PMTs in quantum optics. These solid-state devices, which are typically biased at tens-volt operating voltage, offer better optical responsivity and higher bandwidth. With the improvement in device fabrication, these micro-meter-scale PDs are available in conventional CMOS chip-level integration, meaning a lower power, lower cost, and higher resolution LIDAR sensor system-on-a-chip (SoC).

Time-to-digital converter (TDC) is the main component to measure travel time of light in pulse-based LIDAR. Since the depth information is directly converted from TDC results, the specifications of TDC is essential to LIDAR sensors. According to the size of pixel array, multiple TDC channels are usually utilized to increase the conversion rate. Therefore, the TDC block will consume a considerable power as the resolution gets higher and the pixel array becomes larger. In this context, power budget of TDC channels is a critical for the whole systems.

In out-door environment, due to the low intensity of returned pulse, pulse-based LIDAR usually suffers from the background light (i.e. sun-light). Higher signal-to-noise (SNR) can be achieved by increasing the measuring cycles and build a histogram to filer the white noise in the ambient. More advanced LIDAR systems leverage digital-signal-processing to refine histogram and extract accurate ToF value.

Pulse-based LIDAR sensors have several advantages. From the circuit-level perspective, it leverages the benefits of deeply scaled CMOS technology since most of signal processing are in digital-domain. For example, the digital TDCs achieves better resolution and higher precision in advanced technology node since transistor fre-

quency (f_T) gets higher in short channel devices. From the system-level perspective, pulse-based LIDAR has the advantages of high dynamic range, fast measurement time and capability to deal with multiple echoes in uncontrolled environment. Actually, the multiple-echo capturing is an important feature in pulsed LIDAR and useful in many application. For instance, geometry features beneath the ocean or forest canopy can be mapped through multiple-echo reflection. In driving assistance systems and driverless car, multiple-echo is prevalent in most practical traffic scenarios.

1.2.2 Modulation-based LIDAR

In modulation-based LIDARs, the laser power is modulated with a sinusoidal or square-wave signal. The light travel time is measured through phase delay between the received and the transmitted signals:

$$t_{TOF} = \frac{\phi \cdot T}{2\pi} = \frac{\phi}{2\pi f} \tag{1.2}$$

where ϕ is phase delay between the received and the transmitted signals, T and f is the period and frequency of modulation signal. The phase delay can be detected through a demodulation pixel. As shown in Fig. 1.2, the demodulation pixel has two transfer gates (TX_1 and TX_2) that controls the charging time of two integration capacitors (C_1 and C_2) [11]. With a certain amount of repeating cycle, the phase difference can be calculated through the amount of charges integrated on C_1 and C_2:

$$\phi = \frac{Q(\pi)}{Q(0) + Q(\pi)} \tag{1.3}$$

The amount of integrated charges can be converted into voltage-domain through

front-end amplifier such as capacitive transimpedance amplifier (CTIA), and then digitized by analog-to-digital converter (ADC). Since the depth information is acquired through analog manner, dynamic range of conversion is limited by the ADC input range versus electronic noise in the circuit. A trade-off presents between ranging precision and ranging distance: we can improve ranging precision by increasing modulation frequency but that also reduces ranging distance.

Unlike pulse-based LIDAR sensor where PDs has to be very sensitive to cope with optical pulse signals, the sensitivity requirement for the PDs in modulation-based LIDAR is moderate since the ToF signal is continuous-wave power. A conventional photodiodes such as pin-photodiodes (PPDs) can work properly as Demodulation pixel with a certain amount of integration time. Comparing with SPADs and

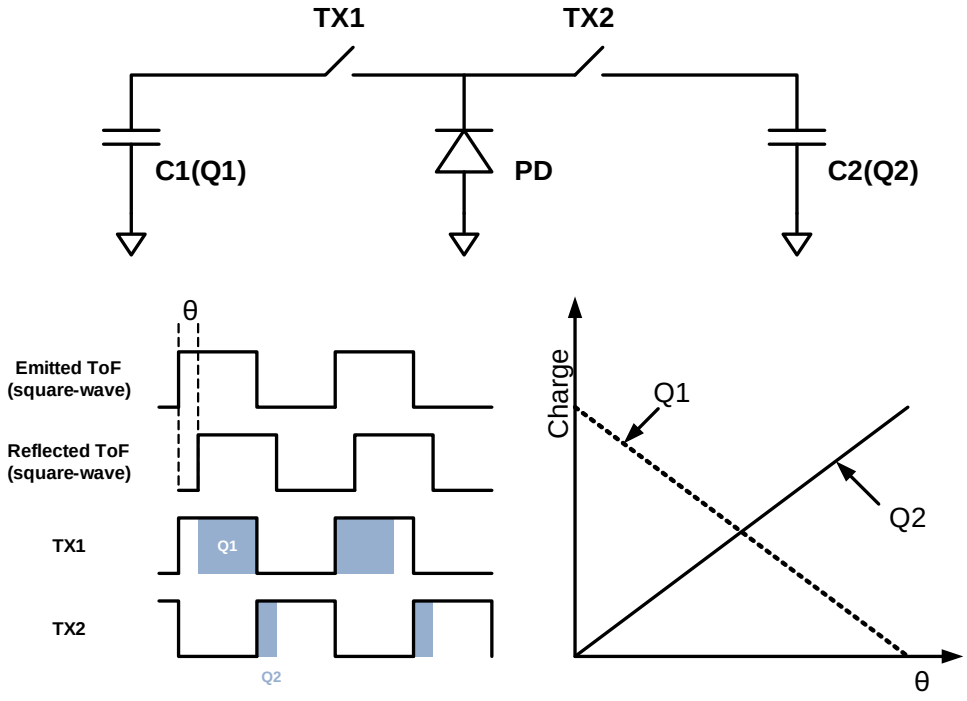

Figure 1.2: Demodulation pixel to demodulate phase delay between the emitted and reflected ToF signals into electronic charges [11].

APDs, PPDs are relatively mature and low-cost device that were used in mega-pixel CMOS image sensors for many years. Therefore, modulation-based LIDAR usually has potential for achieving larger pixel array and lowering complexity of fabrication.

The advantage of analog conversions in modulation-based LIDAR is that resolution can be enhanced by increasing voltage-gain in front-end amplifiers, which is hard to implement in time-domain signal processing. Time-domain amplifier usually relies on the device matching and consumes longer process time [12, 13, 14]. This difference makes the sub-centimeter resolution is easily achieved in modulation-based LIDAR but burns a lot of power in pulsed-based LIDAR for boosting high frequency of TDC reference clock.

As we described previously, the downside of modulation-based LIDAR is the limited dynamic range. On the other hand, TDC-based conversion has extensible dynamic range. Moreover, the modulated signals are more vulnerable to the multi-echo reflections, which limit the applications of this technology . In summary, modulation-based LIDARs are typically used in short range-finding that demands high resolution 3-D imaging such as 3-D scanner, 3-D copier, gesturing, and gaming, while the pulse-based LIDARs are used in the long range-finding such as geometric mapping, driving assistance, autonomous vehicle, and out-door surveillance.

1.3 Thesis Organization

In this thesis, we demonstrate a pulse-based LIDAR sensor prototype that are targeting at the long-range application such as driving assistance system and autonomous car. The object of this work is to minimize the power consumption of TDC meanwhile achieve sub-centimeter ranging precision. A TDC topology based

on injection-locked oscillators (ILOs) is utilized in the prototype to achieve a low-power clock distribution, which is the novelty in TDC design as well as LIDAR sensor SoC.

In Section 2, an overview of LIDAR sensor is presented. The overview commences with the optical transmitter design. It contents LIDAR power equation, the characteristics of transmitter sources, and scanning technique. We then discuss the properties of two conventional single-photon photodiodes, i.e. APDs and SPADs, and their respective front-end receivers. This will be followed by a general discussions of high-level TDC design. The concept of multi-stage conversion will be illustrated in circuitry level. A literature survey of the current state-or-art TDC designs implemented in LIDAR sensors is presented, commenting on each topology and highlighting the strengths and drawbacks with each architecture. The section concludes with the introduction of advanced back-end rejection technique, which is important for improving signal-to-noise ratio (SNR) and the quality of imaging. The technique was implemented in digital-side or analog-side.

In Section 3, it starts with a statement of the major challenges and con-siderations involved in LIDAR-TDC. A new TDC architecture based on ILO clock distribution is proposed to address the trade-off between the power and timing accu-racy in previous works. We then discuss the theory of injection locking and derived the the locking equation for characterizing the circuitry behavior. This is followed by circuitry level design of ILO-based TDC (ILO-TDC), with single channel and multiple channels. The section is concluded with a comparison of power budget be-tween the ILO-based TDC and the other types of clock distribution. The comparison results show the advantage of ILO-TDC in terms of power budget, time resolution, and time precision.

In Section 4, the proposed LIDAR sensor prototype is presented. The proto-type SoC supports 31×2 pixel array channels. The estimated distance resolution is 0.78-cm and the maximum detection range is 124-m. The consideration from system-level to circuitry-level will be describe thoroughly. The main core in the SoC is a 14-bit two-stage flash TDC. The Coarse-TDC (CTDC) is implemented by a global 10-bit Gray code counter, and the Fine-TDC (FTDC) is based on the 4-bit ILO-TDC in Section 4. The TDC supports 31 input channels, 52-ps time resolution, and 852-ns measurement range.

In Section 5, SoC electrical measurement results are presented, including power breakdown, single-shot precision (SSP), channel uniformity, and linearity performance. Finally, a table summarizes the performance of the proposed SoC and compares this work against recent state-of-the-art works.

In Section 6, a summary of the work is given, conclusions are made and the nature and scope of future work in this thesis is discussed.

2. OVERVIEW OF LIDAR SENSOR

Applications such as driving assistance and autonomous car demand hundreds of meters of ranging distance within uncontrolled luminance environment. Signal-to-noise ratio (SNR) degrades severely in this condition due to the strong intensity of solar background illuminance. Also, in complicated traffic situations such as that in the urban cities, the effect of multi-echos could be serious due to the surroundings, i.e., buildings, traffic signs, vehicles, and pedestrians. In this context, pulse-based LIDAR is typically preferred due to its high dynamic range, fast measurement time and capability to deal with multi-echos. In this section, we will discuss several considerations in pulse-based LIDAR sensor from the optical design to electrical circuitry.

Fig. 2.1 shows the block diagram of pulse-based LIDAR sensor. In the transceiver, a pulse laser emits optical pulses at a repetition frequency. Laser beam is collimated through a focal lens in front of laser head to enhance the power efficiency and SNR. The return pulse, reflected by remote targets, is collected through a receiver lens, and focused on the sensor array in receiver. Single-photon photodiodes (PDs) such as APDs or SPADs are usually utilized here to capture the low intensity of returned pulse. A time-correlated single-photon counting (TCSPC) is cooperated to measure the travel time of light. To get accurate counting results, the transmitter and receiver are synchronized with a global LDIAR trigger clock. This global clock triggers pulse laser emission as well as the start time of time-to-digital converter (TDC). Therefore, TDC counts the time starting from pulse emitted by transceiver. As return pulses are detected by PDs, the optical signal is converter into photocurrent signal that is

sensed and amplified by front-end receiver (RX). The output of front-end RX is used as the STOP signal for TDC. The resolved TDC output is:

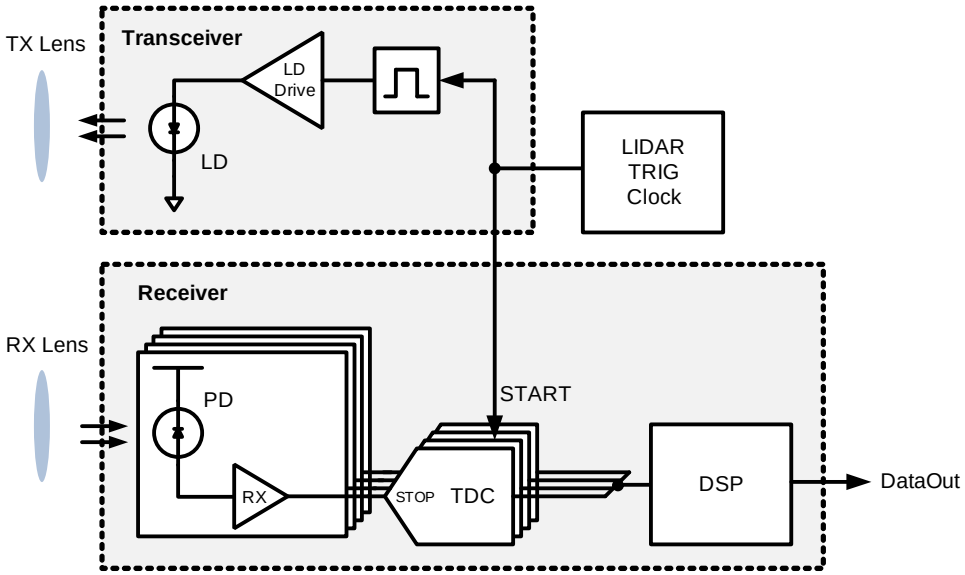

Figure 2.1: Block diagram of pulse-based LIDAR.

$$\begin{aligned} t_{TDC} &= t_{STOP} - t_{START} \\ &= t_{detection} - t_{emission} \end{aligned} \tag{2.1}$$

Multiple TDC channels are designed to support the input of time events from sensor array so that a faster conversion rate can be achieved. Several state-of-art TDC architectures were proposed based on the requirement of power, area and conversion rate in applications. According to those specifications, TDC design can be pixel-shared, column-shared, or global.

Finally, DSP is designed to filter out the noise in ambient illuminance, photodiodes, and electrical circuits. Typical filtering technique includes temporal correlation

filtering (histogram average, finite-impulse-response) and spatial correlation filtering that will discuss further in the later paragraph.

2.1 Optical Design

2.1.1 Surface Reflection Model

LIDAR ranging distance is typically limited by the minimum light intensity of returned pulse that can be captured by sensor pixels. The intensity reflected from an object is dependent on the distance, reflection coefficient, and surface roughness of the object. Fig. 2.2 shows three typical reflection models that are used to describe the surface reflection in the nature. The first type is Specular reflection, in which the light from a single incoming direction is reflected into a single outgoing direction. The angle of light reflection follows the Snells law: the angle of reflection is equal to angle of incidence:

$$\theta_i = \theta_o \tag{2.2}$$

Specular model describe the reflection of ideal mirror surface. If surface has a slight roughness, the reflection power tends to spread out along the ideal reflected direction.

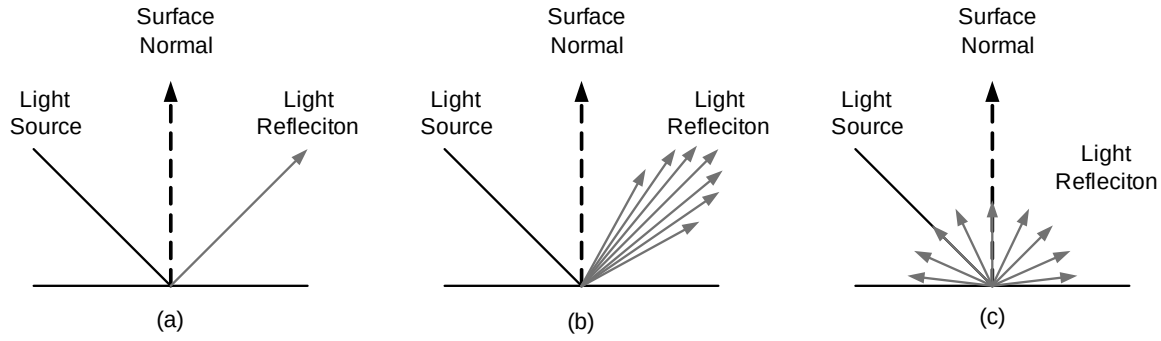

Figure 2.2: Surface reflection model: (a) specular, (b) spread, (c) lambertian.

The illuminance of outgoing light detected by viewer can be approximated by Phong equation [15]

$$\begin{aligned} I(\theta) &= k_S \cdot I_{in}(\vec{V} \cdot \vec{R})^n \\ &= k_S \cdot I_{in} \cos^n \theta \end{aligned} \tag{2.3}$$

where k_S and n are specular reflection constant and shininess constant of surface, I_{in} is the incident illuminance, $\vec{V}$ is the vector to viewer, $\vec{R}$ is the vector of ideal specular reflection, and θ is the angle between $\vec{V}$ and $\vec{R}$. Phong equation reflection presents the light reflection of most mirror-like surfaces in the nature, i.e., glass and water.

As the roughness increases, the surface reflection will be more divergent. This diffusely reflecting surface is described as Lambertian surface. In Lambertian reflectance, light from a single incoming direction is reflected isotropically: the same radiance would be detected by viewer from any angle. For example, a white paper has the same brightness no matter the viewer is on perpendicular direction and tilt direction. It is interesting to note that even the reflection radiance is isotropic in Lambertian reflectance, the luminance intensity is not. This is because the solid-angle detected by viewer from a tilt direction (θ) is actually smaller than that from the perpendicular direction by $cos(\theta)$. To maintain the same radiance, the intensity needs to decrease by $cos(\theta)$. This phenomenon is well-known as Lambert's Cosine Law:

$$I(\theta) = I(0^\circ)cos(\theta) \tag{2.4}$$

Lambertian reflectance represents most nature surfaces in the world such as woods, stones, and sands. It is also the most adoptive model used in LIDAR equation.

In the following, we derive LIDAR equation with the assumption of Lambertian reflectance.

2.1.2 LIDAR Equation

LIDAR equation describes the fundamental relation between the emitted power and received power in LIDAR system. In the transmitter, a pulse laser transmits a narrow beam toward a reflector. The footprint area of the beam at reflector is:

$$A_{laser} = \frac{\pi R^2 {\Omega_t}^2}{4cos(\theta)} = \frac{A_{laser,0}}{cos(\theta)} \tag{2.5}$$

where R is the distance to the reflector, Ω_t is the laser beamwidth, and θ is the incident angle respective to surface normal. Dividing the power by the footprint area, the incident power density S_t of laser beam at the reflector is:

$$S_t = \frac{P_t}{A_{laser}} = \frac{P_t}{A_{laser,0}} cos(\theta) \tag{2.6}$$

where P_t is total transmitted power. The reflection power P_r can be calculated as:

$$P_r = \rho S_t A_s \tag{2.7}$$

where ρ is the reflection constant of material, and A_s is the optical receiving area of the reflector. The reflection pattern is quite complex, but for simplicity we assume that the radiance is reflected uniformly into a cone of solid angle. The reflected power density S_r is:

$$S_r = \frac{P_r}{\Omega_r R^2} \tag{2.8}$$

where Ω_r is the solid angle of reflected beam that is π in Lambertian reflectance. Thus, the reflected power collected by receiver lens is:

$$P_{Lidar} = S_r A_{lens} \tag{2.9}$$

where A_{lens} is the effective area of the receiver lens. Combining (2.5)-(2.9), we can rewrite (2.9) as:

$$P_{Lidar} = \frac{\rho}{\pi R^2} \frac{P_t}{A_{laser,0}} cos(\theta) A_s A_{lens} \tag{2.10}$$

(2.10) can be further simplified by assuming that A_s is equal to $A_{laser,0}$. This is a valid assumption since sensor should cover the over all footprint area at reflector to acquire the maximum power efficiency. In long range detection, we also need to consider the optical absorption in atmosphere which is expressed as $\exp(-2\alpha R)$ where the α is the extension rate. Thus, the final LIDAR equation is:

$$P_{Lidar} = \frac{\rho}{\pi R^2} P_T A_s cos(\theta) e^{-2\alpha R} \tag{2.11}$$

Fig. 2.3 shows the simulation results of (2.11). In this simulation, the laser peak power P_t is 40W, reflection constant ρ is 50%, lens area is $0.00785m^2$ (10-cm diameter focal lens), and extinction rate is $0.227/km$. Simulation results shows that the distance R is the dominating factor in this equation, while the incident angle θ is minor factor: power degrades 1.5dB as incident angle changing from 0° to 45°.

2.2 Transmitter

The transmitter in LIDAR could an array or a single point. The array source utilizes an array of light-emitting diodes (LEDs) or laser diodes (LDs) to diffusely

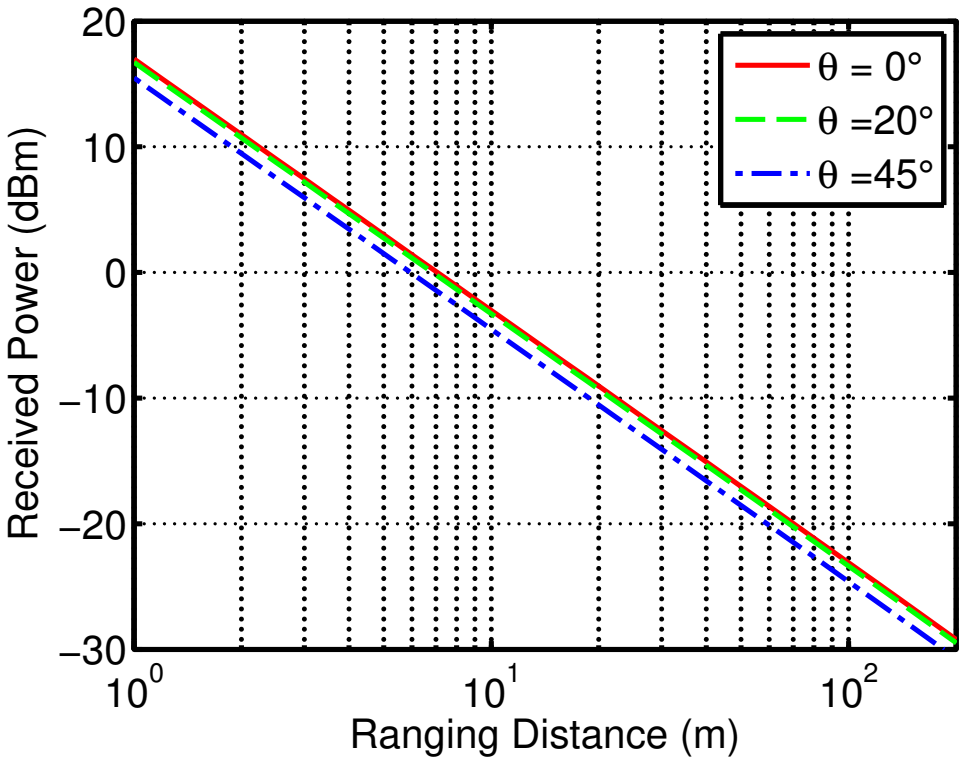

Figure 2.3: LIDAR equation: received power vs. ranging distance.

illuminate targets. The advantage of array source is the simple optical design and fast measurement speed. However, it usually requires higher power to illuminate multiple targets simultaneously that might induce eye safety issue. This is especially important in consumer and automotive application where the optical power is confined by strict regulation: Class-I eye safety in typical case. In this context, single source with scanning approach can achieve higher SNR but consumes less optical power.

2.2.1 Laser Scanning Technique

To date, three major types of laser scanning are proposed in state-of-art LIDAR module. The first type of scanning is by spinning the entire LIDAR module. For

example in Ref. [16], the entire module spins at 900 rpm around its vertical axis to generate 360° horizontal field-of-view (H-FoV). The 28.6° vertical field-of-view (V-FoV) is achieved through the well-aligned 64 laser channels. The second type of scanning is based on a fixed laser source and a rotated mirror. In Ref. [5], the laser beam is coaxially targeting at a rotated six-faced polygonal mirror where each facet has a slightly different tilt angle, resulting in a 170° H-FoV and 4.5° V-FoV. The last type of scanning is based on Micro-electro-mechanical systems (MEMS) scanner. In Ref. [17], the laser beam is aimed at a 2-axis MEMS mirror. By electrically driving the facet angle of the MEMS mirror, the laser beam can be aligned with the any desired angle. Although this scanning technique only achieves 15° H-FoV and 11° V-FoV, it demonstrates a possibility for all-in-one LIDAR SoC, manufacturing the transmitter and receiver on a shingle chip. Due to avoiding the mechanical part in module level, this technique has great potential to simplify module design and reduce the cost.

2.2.2 Laser Wavelength

The wavelength region utilized in LIDAR is related to the processing technology, fabrication cost, and application. To reduce the possibility of eye damage, almost all LIDAR systems are operated at infrared (IR) region. Typically, two different wavelength regions are considered: 850nm-950nm (near IR) and 1550nm (IR).

NIR (850-950nm): The most common range utilized in LIDAR system since the correlated optical components, i.e., lasers and photodiodes, are easily acquired in conventional CMOS process within this wavelength region. However, because the wavelength region is close to the visible region of human eyes. High power emission is sitll harmful. Therefore, the maximum power at this region is strictly confined

for the safety. According to international standard IEC60825-1, the emission limit for Class 1 laser at wavelength 700nm to 1050nm and pulse duration 1-ns to 100-ns is $2 \times 10^{-7} J$. Besides, since NIR is the most common used wavelength region, the cross-talk and uncorrelated signal could impact the operation in this region.

IR (∼1550nm): a rather common wavelength region because it is out of optical window of silicon. Typical materials that are used to detect this range are InP/InGaAs or germanium (Ge). While InP/InGaAs has higher quantum efficiency, it is very hard to integrated in CMOS technology. On the other side, Ge is compatible with conventional CMOS. However, the optical responsivity of Ge is lower due to its indirect bandgap. Thus, most high-sensitivity PD is InP/InGaAs-based. Since the power at this wavelength is seldom detected by human eye, higher emission power is allowed in Class 1 laser. Also, the atmosphere extinction rate at 1550nm is lower than that at NIR region, which leads the longer detection range.

2.3 Photodiodes

Due to the Lambertian reflectance in the nature, intensity of returned pulse is very weak in long-range detection. As depicted in (2.11), with a 40W peak transmitted power, LIDAR can only receives -25dBm return power reflected from object at 100-m distance. To cope with the low intensity power, avalanche photodiodes (APDs) or single-photon avalanche photodiodes (SPADs) are usually utilized as the sensor in receiver.

2.3.1 Avalanche Photodiodes (APDs)

The structure of avalanche photodiodes (APDs) is a conventional p-n junction or p-i-n junction. Through biasing the junction close to breakdown voltage, the avalanche detection can triggered once photon detection. The avalanche process in p-i-n APDs is illustrated in Fig. 2.4. As the photon energy is absorbed, the energy excited electrons from valence to conduction band, creating an electron-hole pair (EHP) in intrinsic region. The electron is accelerated by the high electric field in intrinsic layer, until it gains sufficient energy to excite the second EHP (first impact ionization). The hole generated from first impact ionization is accelerated by electrical field and creates the third EHP (second impact ionization). This positive feedback process amplifies the number of EHPs and generates the optical gain M in the intrinsic layer. The linear relationship between APD's photocurrent and incident optical power is:

$$I_{APD} = M \cdot \eta \frac{q}{h\nu} P_{in} \tag{2.12}$$

where η is quantum efficiency of APDs, $h\nu$ is photon energy, and P_{in} is the incident power. Optical gain is proportional to the biasing voltage of APDs. Depending on the device process, the biasing voltage of APD is from 10V to 30V to achieve acceptable optical gain. Operating in such high biasing voltage, a good junction quality is the essential in APD because any non-uniform profile or defects at junction surface would potentially cause diode breakdown and trigger the avalanche mechanism spontaneously.

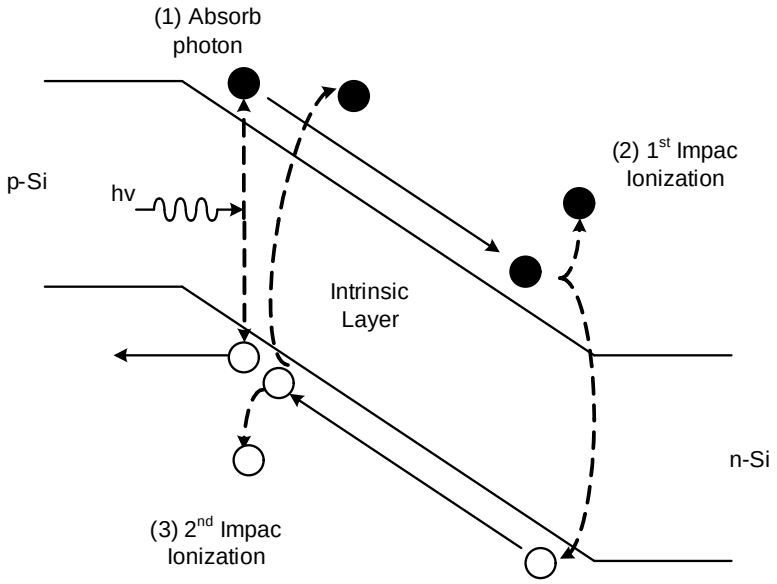

Figure 2.4: Avalanche process in APD.

2.3.2 Single-Photon Avalanche-Photodiodes (SPADs)

Recently, one fast-growing class of APDs, single-photon avalanche-photodiodes (SPADs), are gain increasing interest. Similar to APDs, SPADs amplifier the electrical signal through the avalanche detection in the intrinsic layer. However, since SPADs are biased at Geiger-mode: reverse bias is higher than diode breakdown voltage (V_{BD}), this device performs a bi-stable output. Only few photons can give rise to a very high number of carriers and induced irreversible avalanche current. Since the gain is very high, the output signal is easily saturated and the intensity information is not preserved at output. Thus, SPAD is a logic photodiodes where its output only records time events of incident photons. The intensity information can be obtained by counting the number of incoming photons during a period of time. Since photocurrent in SPADs is irreversible unless the leakage path is broken, devices need to be quenched every time before the next detection. During this time, SPADs cannot

operate in detection mode. Thus, the time is also called the deadtime of SPADs. Typical length for deadtime is from 10-ns to 100-ns [5, 18] depending on the design of photodiode and quenching circuits.

2.4 Front-End Receiver

The purpose of front-end receiver (RX) is to bias photodiodes at proper operating voltage, and convert photocurrent and into a full swing voltage signal. Different PDs need for different RX design. In the following, we will discuss two main RX design: 1) transimpedance amplifier (TIA) that is used in APD-based sensor, and 2) quenching circuit that is used in SPAD-based sensor.

2.4.1 Transimpedance Amplifier (TIA)

In APD-based sensor, transimpedance amplifier (TIA) is usually utilized for the current-to-voltage conversion through a linear transimpedance gain. Fig. 2.5 shows

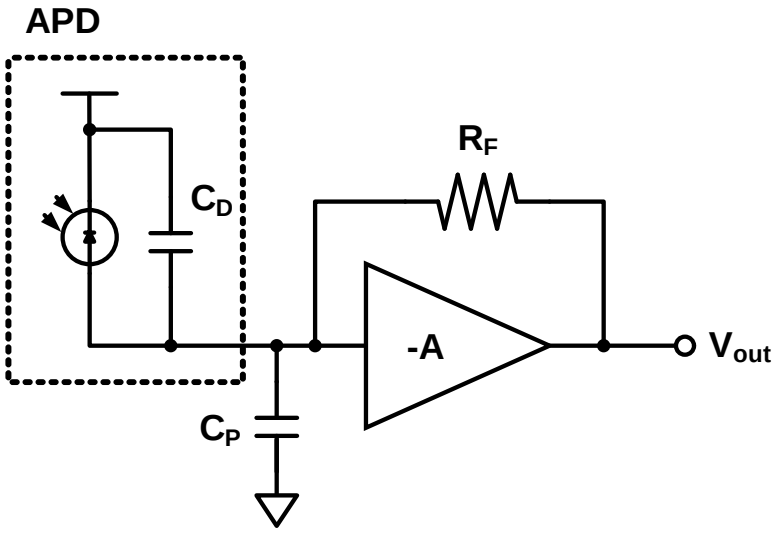

Figure 2.5: Schematic of transimpedance amplifier.

one of the most popular TIA: resistor feedback TIA. It contents an operational amplifier (OPAMP) with voltage gain of $-A$ and a feedback resistor R_F. Assuming an ideal amplifier with unlimited bandwidth, the input impedance R_{in} of TIA is:

$$R_{in} = \frac{R_F}{A+1} \tag{2.13}$$

and the frequency response of transimpedance Z_T is:

$$Z_T = -\frac{A}{A+1} R_F \frac{1}{1+sR_{in}C_T} \tag{2.14}$$

where C_T is total input capacitance that is the sum of the junction capacitance of APD (C_D) and parasitic capacitance at TIA input (C_P). Notice that as A increases, R_T will approach to R_F and R_{in} will approach to zero. It is desirable since the bandwidth of TIA is usually dominated by the input pole ($1/R_{in}C_T$). Thus, a higher bandwidth can be achieved with higher amplifier gain. In the real implementation, the gain-bandwidth (GBW) in OPAMP is limited by power consumption and device technology. A trade-off needs to consider between gain and ω_{3dB} bandwidth in amplifier. With considering the ω_{3dB} of OPAMP, the frequency response of Z_T is:

$$Z_T(s) = -\left(\frac{A}{A+1}R_F\right)\left(\frac{1}{1+s/(\omega_0 Q)+s^2/\omega_0^2}\right) \tag{2.15a}$$

$$\omega_0 = \sqrt{\frac{A+1}{R_F C_T T_A}} \tag{2.15b}$$

$$Q = \frac{\sqrt{(A+1)R_F C_T T_A}}{R_F C_T + T_A} \tag{2.15c}$$

where T_A is the time constant of amplifier ($1/\omega_{3dB}$), ω_0 is the resonant frequency, and Q is the quality factor. (2.15) shows that TIA response is a conventional second-order low-pass response. The maximum flat frequency response is characterized as

Butterworth response ($Q = 1/\sqrt{2}$). Thus, the optimized ω_{3dB} for amplifier is:

$$\omega_{3dB} = 2A/R_F C_T \tag{2.16}$$

The bandwidth requirement for TIA is dependent on the time resolution of time-correlated single-photon counting (TCSPC). In order to confine power-supply-noise jitter at TIA output within time resolution of TDC channel, the time constant of TIA need to be roughly closed to two significant-bit (LSB). For instance, the TIA bandwidth should be higher than 1.6GHz for a 50-ps time resolution.

Noise performance is another important characteristic in TIA design since it determines the sensitivity of LIDAR sensor. Assuming an ideal photodiode (i.e. noiseless), the optical sensitivity of LIDAR is:

$$\overline{P_{sen}} = \frac{\alpha I_{rms}}{2\rho} \tag{2.17}$$

where α is random noise margin, ρ is the responsivity of APD, and I_{rms} is input-referred noise of TIA. Generally, I_{rms} is dominated by resistor thermal noise ($4kT/R_F$) over TIA bandwidth. As we recalled the transimpedance response in (2.14), the Z_T is roughly equal to R_F as the gain A is much larger than 1. Thus, we can use higher R_F to increase Z_T and suppress I_{rms} in the same time. However, it also reduces the TIA bandwidth. A trade-off among gain, noise, and bandwidth needs to consider in design.

In general RX design, a limiting amplifier (LA) is cascaded after TIA to amplify TIA output signal to a reliable signal level. Bandwidth of LA is larger than the TIA for maintaining the overall bandwidth. Noise performance, however, is not critical

since the effective input-refer noise from LA is divided by Z_T. The overall I_{rms} of RX is dominated by TIA.

2.4.2 Quenching Circuit

In SPAD-based sensor, output of SPADs is inherently a rail-to-rail signal, which can be directly processed with digital circuit. A simple CMOS inverter is cascaded after SPAD for isolating the input noise and parasitic loading. However, due to the bi-stable characteristics (once the photocurrent is trigger by photons, it cannot be terminated), a queching circuit (QC) is applied to disconnect photocurrent path (quench) and reset SPAD each time before next detection.

The simplest QC is shown in Fig. 2.6 where a quenching resistor (R_Q) is in series with SPAD. In dark light condition, SPAD is biased at Geiger-mode: the sensing node (V_s) is pulled to ground by R_Q, and SPAD operation voltage V_{SPAD} is higher than junction breakdown voltage V_{BD} by an excessive bias voltage V_E. As a photon is captured, avalanche photocurrent will be triggered, flow through R_Q and pulls V_s up until V_s reaches V_E and quenches the avalanche current. After SPAD enters quenching mode, RQ start to discharge the excessive carriers in the junction of PD and pull the V_s back to ground. The discharge rate is dependent on the value of R_Q that needs to be customized according to the different SPAD design. A fast discharge rate may trigger an unwanted avalanche process or so-called "afterpulse" in SPAD [19]. To prevent afterpulse, PD has to be held-off at a low biasing point (lower than V_{BD}) for a sufficient time for releasing carriers trapped in deep level before recharging. After the junction carriers are completely depleted, SPAD is recharged and back to Geiger-mode. During this process (hold-off time and recharging time), SPAD cannot work for detection. So it is also called dead time for

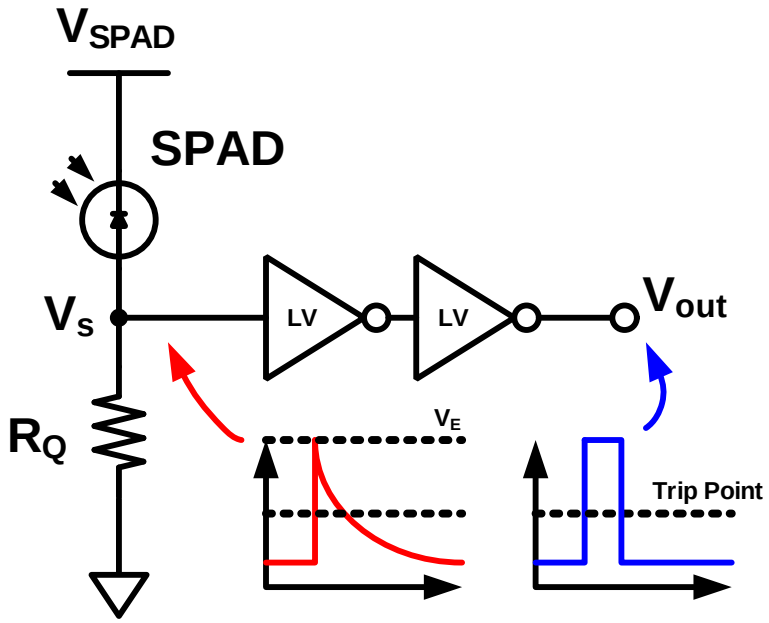

Figure 2.6: Schematic of typical passive quenching circuit (PQC).

SPADs. The passive quenching circuit (PQC) described above usually require long quenching time since it needs a large R_Q to sustain enough hold-off time. The large R_Q makes a large time constant in recharging process. Thus, deadtime takes around 40-ns to 100-ns.

The long quenching time can be improved in active quenching circuits (AQC). In ref [19], an AQC is proposed to shorten the quenching time through two-step charge rate (Fig. 2.7). In this design, the charge rate is different between hold-off time and recharge time. Upon photon detection, the V_s node is pulled-up by SPAD current, making SPAD quenched. Since the NOR gate does not switch at this moment, V_s is discharged slowly through M_1 to prevent afterpulse effect. During this time, the discharging current I_{QCH} is set to be smaller than so-called SPAD latching current, it would eliminate the probability of afterpulse and gives time to extract deep-level

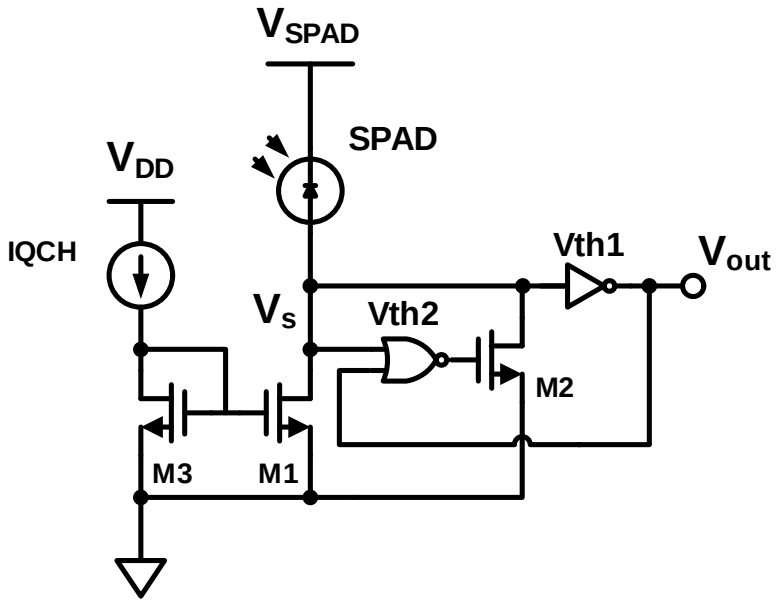

Figure 2.7: Schematic of two-step discharging rate active quenching circuit (AQC) [19].

carriers. As V_s is lower than V_{TH2}, it would switch the NOR gate and turn on M_2. A faster discharge rate is presented in recharging time. The proposed active quenching circuit shrinks dead time to 6-ns.

2.5 Time-to-Digital Converter (TDC)

Time-to-digital converter refers to a data interface where the input is a timing event and the output is a digital word corresponding to the magnitude of the timing event with quantization error:

$$T_{TDC} = B_{out} \cdot T_{LSB} + \epsilon \tag{2.18}$$

where B_{out} is the digital output word, T_{LSB} is the time interval of least significant bit or time resolution, and ϵ represents the quantization error. There are many

approaches for converting/quantizing a time-event into its digital equivalent. However, in this work we will focus on the digital approach since it typically supports higher dynamic range (DR). In addition, digital TDC leverages the benefits of deeply scaled CMOS technology. Higher TDC resolution can be achieved due to the higher transistor frequency and shorter gate delay in short channel devices.

DR is an important specifications in LIDAR, especially in automotive application. For high performance driving assistance LIDAR, the detection range is up to 100-m distance with the resolution of few centimeters. It is corresponding to 0.667-us maximum counting range and 100-ps time resolution in time-domain ($DR > 76dB$). In order to reach high DR but also maintain good power efficiency, the multi-stage conversion is typically utilized: front stages are responsible for DR extension while the later stages provide high resolution for TDC. Time resolution of each stage varies with the different specifications and applications. However, a general rule of three-stage conversion can be applied:

Coarse TDC (CTDC): CTDC is responsible for the highest-level time conversion where its DR represents the DR of whole TDC. Since the fine conversion will be resolved in the later stages, the resolution of CTDC is equal to the dynamic range of the next stage. Counter-based TDCs are the most common CTDC architectures where the counting rate is triggered by an external clock. The resolution of general CTDCs is few nanosecond or more. The simplest and also most prevalent counter-based TDC is ripple counter due to the simple design complexity and high DR (this will be discussed further). In ripple counter, 1-bit DR extension can be simply achieved by adding one additional logic register.

Fine TDC (FTDC): FTDC is responsible for the second-stage conversion. DR

is confined by the LSB of CTDC. Delay-line TDC (DL-TDC) is the most popular FTDC architecture where the time event is measured according to the number of stage of propagation delay. Resolution of FTDC is limited by the gate delay of the delay cell. To compensate variation of delay time due to PVT, the delay line are usually controlled by a feedback loop control such as DLL or PLL.

Sub-Fine TDC (S-FTDC): S-FTDC provides time resolution shorter than the gate delay of technology (sub-ps). Several state-of-art has been proposed in previous literature, including Vernier delay-line TDC [20], Successive Approximation (SAR) TDC [21], and pipelined TDC [22, 23]. The accuracy of resolution in S-FTDC mainly relies on device matching and sizing ratio. Approaching of Feedback-loop control cannot be applied here since the resolution is too high. Thus, S-FTDC demands higher process control and the operation range of the circuit is limited . In addition, sub gate-delay resolution usually achieved through iteration of conversions that takes longer conversion time and consumes higher power than CTDC and FTDC. S-FTDC is mainly used in high-resolution TCSPC such as that used in positron emission tomography (PET) and fluorescence lifetime (FLIM), while the performance and power is not suitable for conventional LIDAR application.

2.5.1 Coarse TDC (CTDC) Counting Scheme

As we described in previous section, the simplest CTDC is a ripple counter. In this design, a N-bit ripple counter contents N cascade logic registers where the clock trigger of each register is connected to the output Q of previous one. The advantage of ripple counter is small layout size and low power consumption. Therefore, it is popular in pixel-based CTDC design. The problem of ripple counter is that the counting signals are not synchronous. It causes ambiguous edges at counting tran-

sition and jeopardize time accuracy of counter. A synchronous version is proposed to solve this issue (Fig. 2.8). In the design, the toggle flip-flops (TFFs) are used to generate counting bits. All TFFs are triggered by one clock source. Generally, coarse counter signals (Q_0 - Q_3) are sent into a time memory. Once STOP signal rise up, counter signals are latched in time memory as CTDC output $CTDC[3:0]$.

In LIDAR sensor, since the STOP signal comes from the front-end RX, it can be trigger asynchronously once photon detection. Therefore, the design in Fig. 2.8 encounters a serious problem with the asynchronous trigger in time memory. The asynchronous trigger induces inevitable time violation in time memory and causes the probability of missing code at TDC output. For example, if STOP is triggered while counter value transits from $4'b0001$ to $4'b0010$, time memory could latches counting value as $4'b0000$ (if bit[0] transits earlier than bit[1]) or $4'b0011$ (if bit[1] transits earlier than bit[0]). The either cases can cause DNL larger than ±2-LSB .

An alternative binary coding approach, the reflected binary code counting, which is also well-known as Gray code counting, is utilized to solve this problem. In Gray code counting, the two successive values differ in only one bit. For example, three and four in decimal is represented as $4'b0001$ and $4'b0011$ in Gray code. As STOP is triggered during the transition between these two values, there is a 50% probability to latch $4'b0001$ and $4'b0011$, respectively, and DNL is always smaller than ±0.5-LSB.

In binary system, Gray code and binary code are transferable through a simple logic process. The converting from N-bit binary code to Gray code is:

$$\begin{aligned} G[N-1] &= B[N-1] \\ G[i] &= B[i+1] \oplus B[i] \ (i < N-1) \end{aligned} \tag{2.19}$$

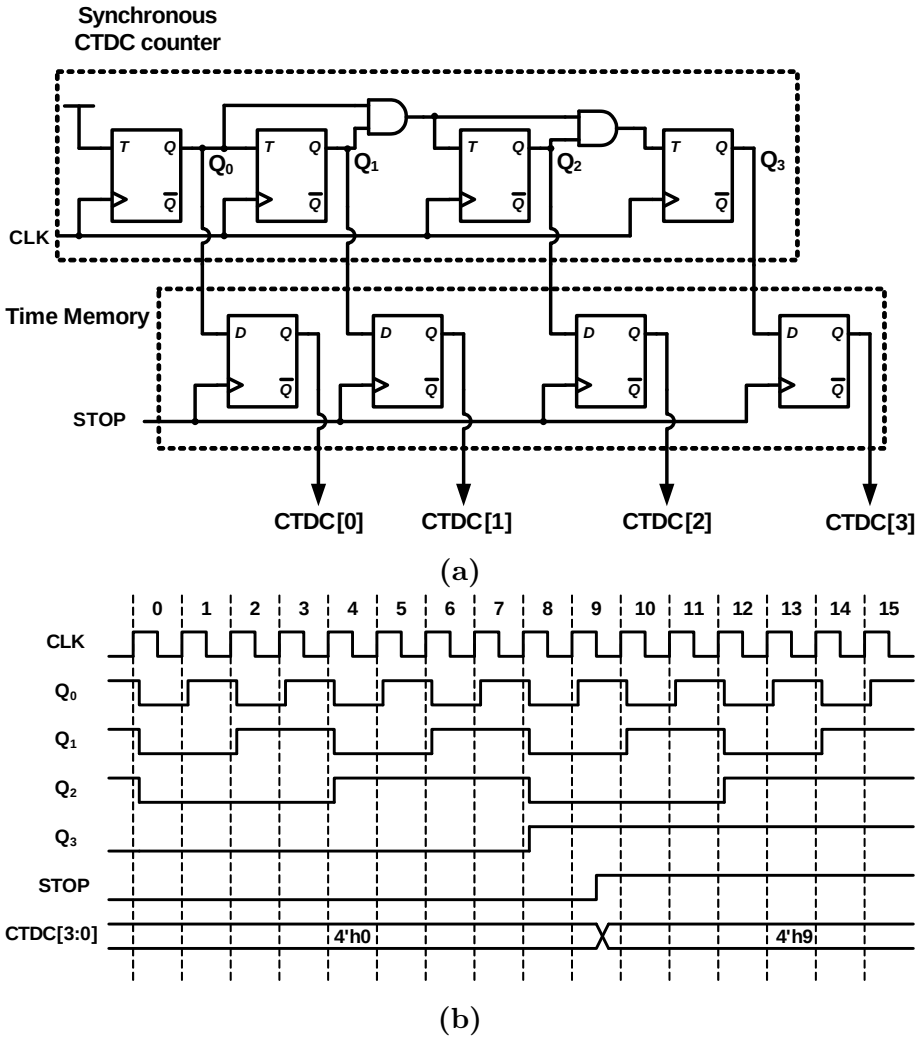

Figure 2.8: A 4-bit synchornous up-counter using T (toggle) flip-flops with a 4-bit time memory: (a) schematic, (b) counting waveform.

And the converting from N-bit Gray to binary code is:

$$\begin{aligned} B[N-1] &= G[N-1] \\ B[i] &= B[i+1] \oplus G[i] \ (i < N-1) \end{aligned} \tag{2.20}$$

Thus, we can use Gray code counter to void missing code in asynchronous time memory and convert it back to binary code in synchronous readout data circuit.

2.5.2 Fine TDC (FTDC) Counting Scheme

In two-stage TDC architecture, FTDC is responsible for the least significant bit in TDC. To achieve centimeter-level depth resolution in LIDAR, the TDC needs to support time resolution smaller 100-ps. In this context, delay-line based TDCs (DL-TDCs) are generally preferred. In the following, we will discussed several state-of-art DL-TDCs:

a. Tapped DL-TDC

Fig. 2.9 shows the schematic of Tapped Delay Line TDC [24]. In the design, a rising edge signal is injected into a delay chain through the START pin that defines the start time of TDC. Assuming the gate delay of each delay cell is Δt_D, the time spends for the START rising edge propagating from the START pin to N-th delay cell output is:

$$T_{TDC} = \Delta t_D \cdot N \tag{2.21}$$

The transition of each node in DL is sensed by digital flip-flops. Once the STOP triggers, state of propagation delay will be latched. Since the signal propagation is from the left to the right, the latched data is a thermometer-code and interpret the time difference between START and STOP.

To avoid PVT variation in delay line, the delay cell is biased with a self-calibrating scheme. In Fig. 2.9, the calibration is implemented by a delay-looked-loop (DLL). By comparing the phase difference between START and START', the delay time can be adapted trough an periodic START clock. Calibration can be also implemented in digital manner. Fig. 2.10 shows the another state-of-art Tapped DL-TDC, which is applied in am all-digital-PLL (ADPLL) circuit[25]. In this design, a known

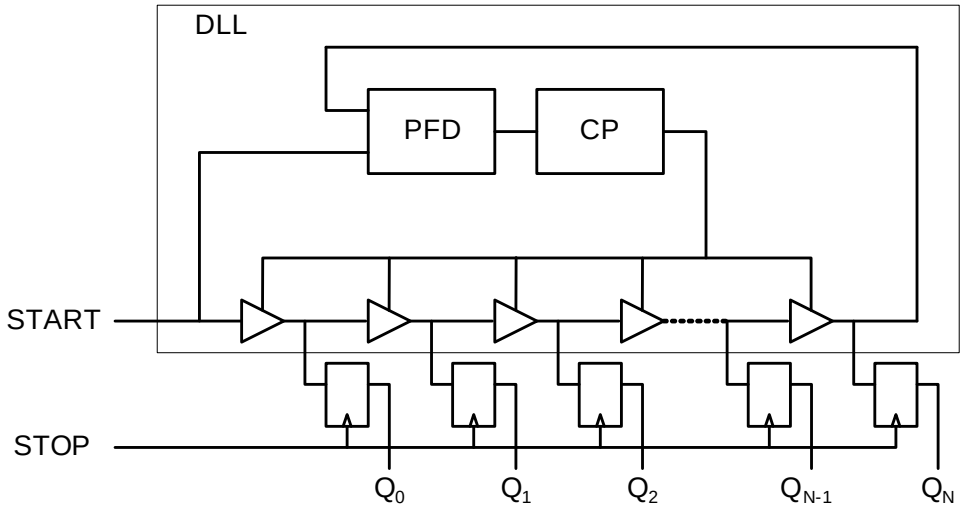

Figure 2.9: Schematic of delay-line TDC (DL-TDC) embedded in DLL.

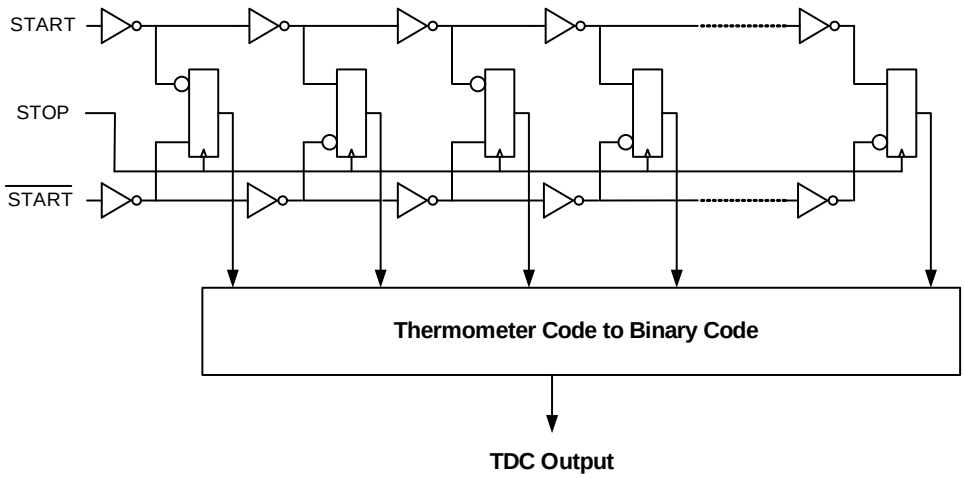

Figure 2.10: Tapped delay-line TDC with self-calibrating circuit [25].

time interval is resolved by TDC. Based on the averaged TDC output (averaging to remove random jitter), the delay time of unit delay cell can be acquired. Notice that differential DLs are utilized here to subtract out common-mode noise. A strongarm sense-amplifier (SA) is used to sense the falling and rising on each node in DLs. Since inverter gates are used as unit delay cell, the polarization of sensing input

of flip-flops is also inverted stage-by-stage. This design achieves 20-ps resolution in 90nm technology.

b. Gated Delay-Line TDC (GDL-TDC)

Fig. 2.11 shows a 4-bit GDL-TDC which is implemented in a pixel-based TDC design [26]. Unlike Tapped delay-line, the GDL latches the propagation delay by gating the signal propagation in DL (disconnecting delay cells). Since no flip-flop is required in the circuit, the smaller layout size is achievable. It is a great appeal to those designs which have stringent area budget,i.e., pixel-based TDC. However, the gating operation might induce metastable nodes in delay line and cause missing code results. This TDC achieves 111-ps time resolution in CMOS 130nm Technology.

This design also introduces a well-known configuration, "reverse start-stop scheme" where the START signal is triggered by photon detection event and the STOP signal

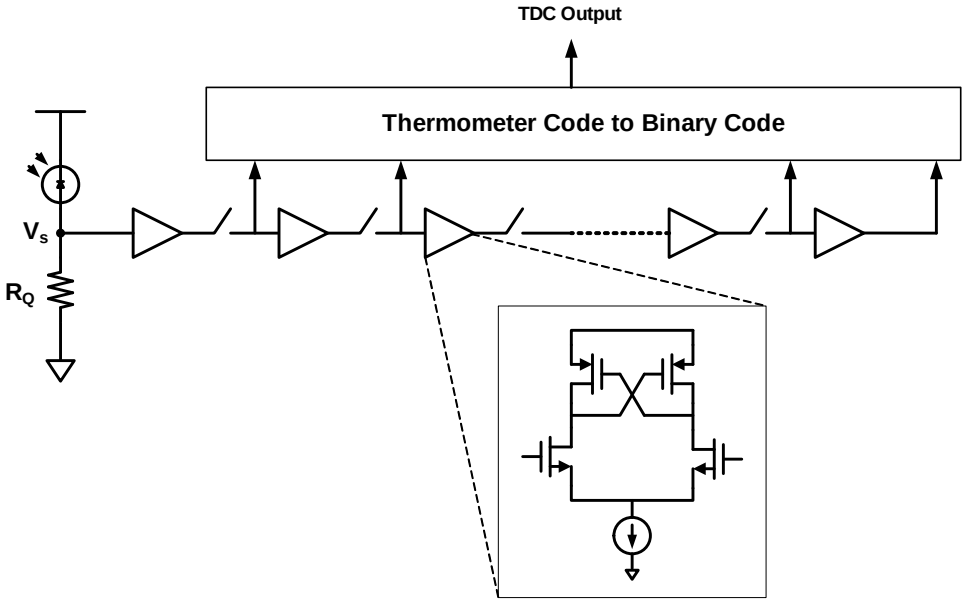

Figure 2.11: Gated delay-line TDC [26].

is triggered by a successive edge of coarse reference clock. The main advantage of the scheme is low power consumption. Since FTDCs are only initiated upon photon detection and stopped by a successive reference clock edge, the power consumption could be minimized. The time is counted from photon detection to the end of one measurement cycle. The TDC output in reverse start-stop scheme is:

$$T_{TDC} = T_0 - (T_{CDTC} + T_{FTDC}) \tag{2.22}$$

where T_0 is the period of one measurement cycle.

c. Gated Ring Oscillator TDC (GRO-TDC)

GRO-TDC utilized a gated-ring-oscillator (GRO) as the timing counter. Fig. 2.12 shows a 3-bit four-stage GRO-TDC [9]. The TDC supports reverse start-stop scheme. The four-stage GRO is gated/frozen at the beginning of the operation. Once the photon is detected, it starts the oscillating until the next rising edge of global

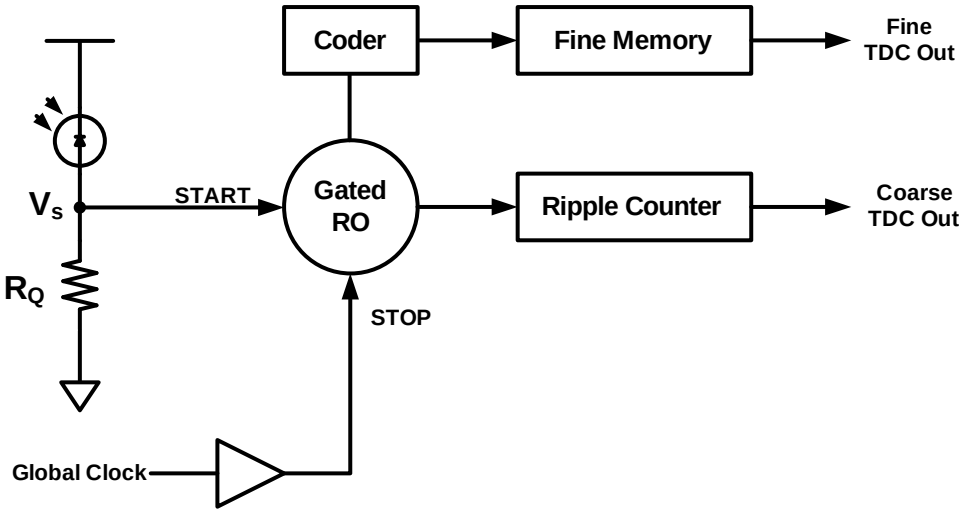

Figure 2.12: Gated-ring-oscillator (GRO) TDC [9].

clock arrives. The number of the oscillating cycle is counted by a 7-bit ripple counter, and the GRO itself provides 3-bit fine resolution. The advantage of GRO is that its dynamic range can be doubled by adding an additional bit number in ripple counter, while it needs two times of area for DL-TDC. This TDC achieves 55-ps resolution in 130nm CMOS Technology. The TDC average power is 38uW and the peak power is 275uA.

2.5.3 Sliding Scale Technique

Sliding scale technique is first proposed by E. Gatti [27] to improve the linearity performance in ADC systems. This technique is mainly to minimize the DNL that is caused by the unequal quantization through the averaging results. In this design, a random but known analog noise is continuously added to the ADC input signal and subtracted from the digital output. As the same quantity is added and subtracted, the overall results do not change. However, since the conversion of the same input signal is performed in different regions of converter range, depending on the random noise value, the linearity of the averaged output is improved.

In TDC, sliding scale technique is inherently provided if START and STOP signals are asynchronous to the reference clock [20]. As shown in Fig. 2.13, the time events of START and STOP are converted in different interpolator ranges, respectively. The time interval, i.e. gate delay, between START and reference clock results in a random noise, which is added to STOP conversion, but it will be eliminated in

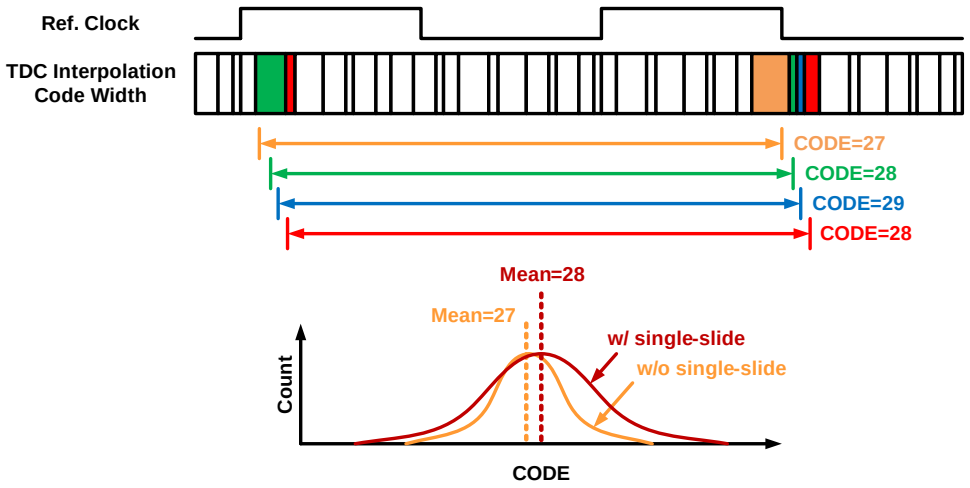

Figure 2.13: Sliding scale technique in TDC.

the final conversion:

$$\begin{aligned} T_{START,1} &= T_{START} + T_{noise} \\ T_{STOP,1} &= T_{STOP} + T_{noise} \\ T_{TDC} &= T_{STOP,1} - T_{START,1} \\ &= T_{STOP} - T_{START} \end{aligned} \tag{2.23}$$

Since the conversion range is random, the effective DNL is improve due to the averaging effect. The improvement of linearity is paid in terms of higher quantization noise and lower single-shoot precision. In fact, the sliding scale transforms the nonlinearity into measured timing jitter. As we utilize two interpolators to convert START and STOP, the quantization noise is:

$$\rho_q = \sqrt{\frac{LSB_{START}^2}{12} + \frac{LSB_{STOP}^2}{12}} = \frac{LSB}{6} \tag{2.24}$$

2.6 Sensor Integration

Imaging-based LIDAR receiver comtents an array sensor and multiple TDC channels. The consideration of sensor integration involves the pixel array and TDC channels, which is dependent on the requirement of specifications (time resolution, pixel array size, power budget, accuracy, etc.) and applications (automotive, IoT, or indoor gaming). There are many kinds of implementation in LIDAR SoC. But for simplicity, they can be classified into two main architectures: global-based counting [5, 6, 7] and pixel-based counting [8, 9].

In the global-based counting, TDC reference clocks are generated from a global source that is usually implemented by a PLL or DLL to calibrate on-chip PVT variation (Fig. 2.14). Since the reference clocks among TDC array are all synchronous and well controlled, the global-based architecture has uniform and high PVT-tolerance. The downside of global-based counting is the high power that is consumed by the embedded clock distribution circuits. Global-based architecture usually requires a sort of clock distribution circuitry to distribute reference clocks from global source into TDC array. The length of distribution traces are propotional to the size of pixel array which could be several millimeters long, inducing picofarads parasitic capacitance loading. Therefore, a strong buffer is required to drive the distribution traces that consumes large power. The power cosummed by driveer could be higher than the power of TDC itself if adoptive reference frequency is very high. Moreover, the large parasitic lamp-RC loading also limits the signal transition time and the frequency of reference clock. Typically, reference clock frequency in global-counting architecture is lower than 1-GHz. For instance, the reference clock is 560MHz in Ref. [26] and 600MHz in Ref. [6]. Although higher counting rate can be achieved through

multi-stage buffers or current-mode logics (CMLs), they burn more power and cost more layout area.

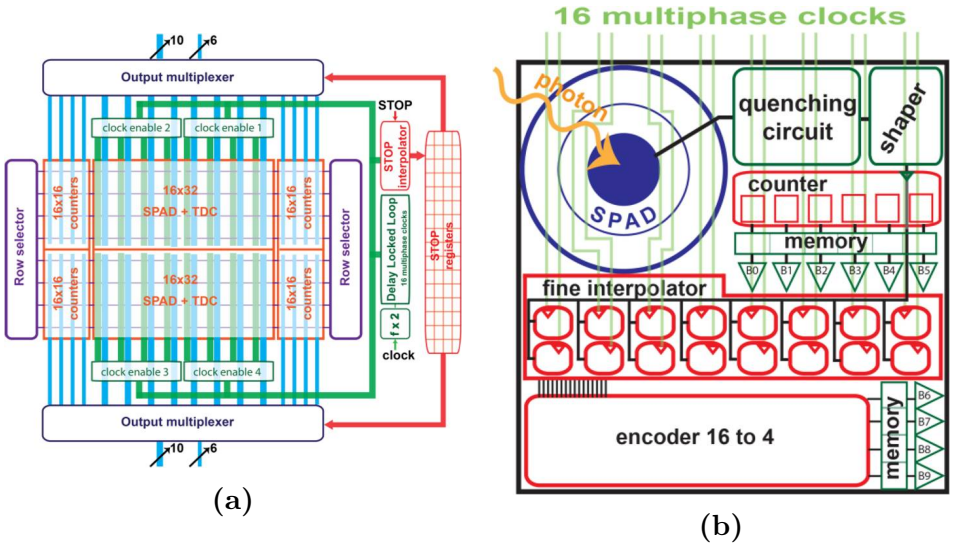

Figure 2.14: Global-based couting architecture: (a) 32×32 imager floorplan, (b) pixel block diagram [7].

On the other side, pixel-based counting have a local oscillator inside a pixel to perform a pixel-level counting (Fig. 2.15). Since the reference clocks are generated inside pixel, it does not require a long clock distribution traces so that consumes less power. In pixel-based counting, power can be further minimized by reverse start-stop scheme where the local oscillator is activated only when photodiodes detect photon flux. In Ref. [8], an ultra-low power TDC which consumes average 38uW per-TDC was demonstrated. It is a candidate technique for mega-pixel array imaging and IoT application.

Although pixel-based counting has a great advantage in the power, the free running oscillation in those pixel-level oscillators is very sensitive to PVT variation,

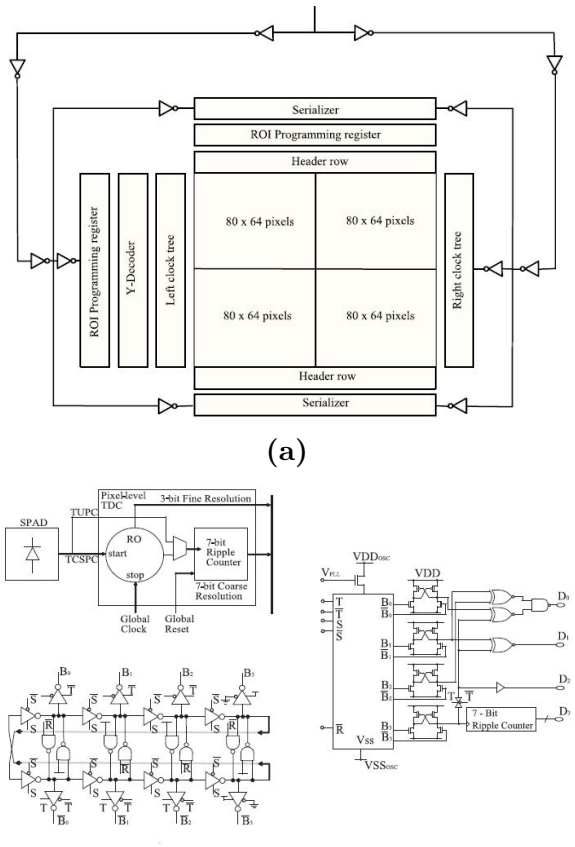

Figure 2.15: Pixel-based counting architecture: (a) 160×128 imager architecture, (b) pixel block diagram [9].

causing the non-uniform counting among TDC array. In order to compensate process mismatch, most pixel-level oscillator is biased with a global-controlled voltage (or current) that is generated from an on-chip PLL or DLL. However, local process variation (channel-to-channel) is hard to be eliminated through this manner. Imaging-dependent power consumption is another issue for pixel-based TDCs. Since the local oscillators are activated only when photon is detected, the power consumption of pixel/TDC array varies with the sensing image. For instance, the TDC design in Ref. [8] consumes peak power $275\mu A$ in active mode and almost none in gated

mode. Such imaging-dependent power could induce variable IR-drop on the power trace which can impact the biasing point and oscillation frequency in oscillators. This in turn has the potential disadvantage of introducing an imaging-dependent time resolution.

2.7 Advanced Background Light Rejection Technique

As we described previously, the returned optical pulse in LIDAR system is so weak that could be suppressed by strong background light. In order to achieve a reliable sensing in the environment within strong ambient light, background light rejection techniques need to be considered in LIDAR sensors. The first level of background rejection is implemented by the optical IR filter in front of sensor array that rejects background light out of the filter window. However, IR filter is insufficient in moderate daylight conditions due to the overwhelming disparity in power between solar ambient light and the LIDAR signal. Therefore, there are many auxiliary background light rejection techniques proposed in front-end circuitry and back-end digital signal processing (DSP).

2.7.1 Back-end Rejection Technique

The most general noise rejection technique in back-end DSP is the integration of a temporal histogram [28]. Assuming a periodic laser pulses were emitted, the ToF data resolved from the time events of return pulses can build up a histogram plot. The histogram contents two parts: 1) a single peak at a time corresponding to the target ToF and 2) a uniformly distributed noise component due to uncorrelated background light. As the measurement cycle increases the amplitude of ToF peak is getting significant from ambient noise floor. Moreover, since the relative fluctuation

in a histogram bin with an expected value N decreases with respect to its mean value in proportion to the $\sqrt{N}$, the accuracy of ToF is also improved by the number of measurement cycles. However, in laser scanning approaches such long temporal-histogramming-process cannot satisfy the frame rate requirement unless sacrificing image resolution. Therefore, a histogram-based finite impulse response (FIR) filter is proposed to improve the accuracy of ToF signal within a specified measurement cycles. The FIR filter demonstrated in Ref. [6] contents a low-pass filter with 15-word kernel. The filter output is performed by convolving the histogram with the filter kernel K_{FIR}:

$$h(m) = \sum_{i=0}^{i<15} h_{RAW}(m-i) \cdot K_{FIR}(i) \tag{2.25}$$

where $h(m)$ is the m-th filter histogram bin and h_{RAW} denotes the unprocessed bin values.

2.7.2 Front-end Rejection Technique

The integration of histogram applied in back-end process needs for certain amount of measurement cycles to acquire enough ToF accuracy. This process degrate the response time of images. To minimize the measurement cycles, an alternative background rejection is proposed at the front-end circuitry-level. In Ref. [5], the spatiotemporal-correlated photon counting technique is applied in front of TDC to filter out the non-correlated time events.

In this design, the 6×2-macro SPAD unit is utilize to detect multiple returned photons simultaneously. Since the ToF returned photons (photons that are returned from targets) are usually spatiotemporal-correlated, more than one sub-SPADs will be fired simultaneously in a single micro SPAD. On the other side, lower than one

sub-SPAD is fired by sparse noise photons from background illumination. Therefore, the noise background photons can be filtered by applying a threshold value for the number of correlated photons. For example, if more than two sub-SPADs are fired in one time event, we pass this coincident event to TDC. Oppositely, if only one sub-SPAD is fired in one time event, we hold this time event and waiting for the next pulse. The coincident events are detected by a coincident detection circuit (CDC) in front of TDC. CDC can filter out the uncorrelated events, i.e., ambient background light, in a fast response. However, the cost of this technique is larger pixel size (macro-Pixel) and an additional supporting circuit involved in signal chain.

3. INJECTION-LOCKED OSCILLATOR (ILO) AND TDC DESIGN

3.1 Problem Statement of Existing TDC Architectures

As we discussed in Section 2, global-based counting usually perform higher PVT tolerance, higher linearity, and better channel uniformity. Also, the counting performance is independent of imaging condition. Due to the outstanding performance, global-based counting is a candidate architecture in automotive LIDAR sensors [5, 6] that are usually operated at stringent environment and claims for a wider operation range.

The high power consumption, however, is downside of global counting. With the large capacitance loading on global clock distribution traces, gloabl counting usually consumes few mW per TDC channel, and the power is linearly increased with the sensor array size. It excludes LIDAR from some IoT applications (drones, or mirco robotics). On the other side, pixel-based counting avoid this by generating the reference clocks locally. Moreover, the power can be further reduced through reverse start-stop scheme in which the high frequency oscillator is only active once photon detection. Nevertheless, resolution and uniformity of pixel-based counting relies on the device matching and more sensitive to PVT variation. Also, the imaging dependent time resolution is another issue.

Targeting at automotive and IoT applications, we will propose a low-power solution for global-based counting. The low-power design is mainly focused on the improvement of the global clock distribution scheme. Instead of the conventional global distribution, the reference clocks are generated inside TDC arrays through

several local injection-locked oscillators (ILOs). Although this design takes advantage from pixel-based counting, ILOs can provide a better uniformity and linearity since the oscillation frequency can be locked by an external injected clock.

In the following section, we are going to overview the injection locking technique, including the concept and locking equation. Then, we will describe the detail design of ILO-based TDC. Finally, the power budget is compared between ILO-based TDC and its counterpart architectures.

3.2 Introduction of Injection-Locked Oscillator (ILO)

Injection-locked oscillator (ILO) is a regenerative oscillator in which the oscillation frequency can be influenced and locked by an external clock driving. Historically, injection locking has been widely used as a low-power approach in high-speed circuits such as frequency division [29], quadrature generation [30], and jitter filtering/clock deskew on high-speed SerDes [31]. For example, in quadrature sampling transceiver, injection locking is a low power solution for the multiple phases clock distribution.

Comparing to conventional clock distribution technique such as CMOS or CML buffers, ILO provides several advantages: 1) multiple clock phases can be generated from single injected clock while multiple distribution traces are needed in conventional architecture, thus saving the routing area and power; 2) ILOs can operate with small injected amplitude due to its high sensitivity, thus the reference clock can be distributed with lower power; 3) ILO rejects high frequency jitter and is less susceptible to power supply noise since its inherent first-order PLL behavior.

Injection locking can be applied to both LC oscillators (LCOs) and ring oscillators (ROs). Typically, LCOs have better phase noise and jitter performance than

ROs. The band-pass nature of LC tank resonators that preserves the monolithic sine-wave behavior makes theoretical analysis easier. But from the perspective of system-level, ROs have the advantage of smaller layout area, larger tuning range, multiple-phase generation and scaling with CMOS technology. Thus, Injection-locked ROs (ILROs) are more suitable for the local counting architecture.

Several methods have been proposed in previous works to model the behavior of injection locking, including: phasor-based Adlers equation [32], perturbation-based projection vector (PPV) [33], and waveform-based time-domain derivation [34]. Since Adlers equation is quite simple and is proven to be useful for modeling the locking behavior in frequency and time domains, we will describe Adlers equation in the this analysis.

Fig. 3.1(a) shows the model of ILO that will be used to obtain the locking equation. In the model, H_{vco} represents the small-signal open-loop frequency response of VCO. The behavior of H_{vco} is dependent on the VCO architectures. In LCOs, H_{vco} is a response of LC tank. In ROs, H_{vco} is a low-pass response that is composition of multiple delay cells. The nonlinear block represents the nonlinearities associated with the VCOs, such as the square wave behavior in ROs. I_{inj} is the injected locking current and I_{osc} is the oscillator feedback current. The I_{inj} is injected into oscillator through a summing point that sums up the I_{inj} and I_{osc} and get I_L at the output. Now, we assume that the frequency of I_{inj} (w_{inj}) is not located at the resonant frequency ω_0 of VCO. In order to maintain loop gain equal to unity with zero phase shift in oscillator, I_L and I_{osc} must have a proper phase shift to compensate the phase deviation due to the oscillation frequency offset from ω_0. As a results, we will see different phases among I_{inj}, I_L, and I_{osc} as shown in Fig. 3.1(b). The three types of current can be expressed as:

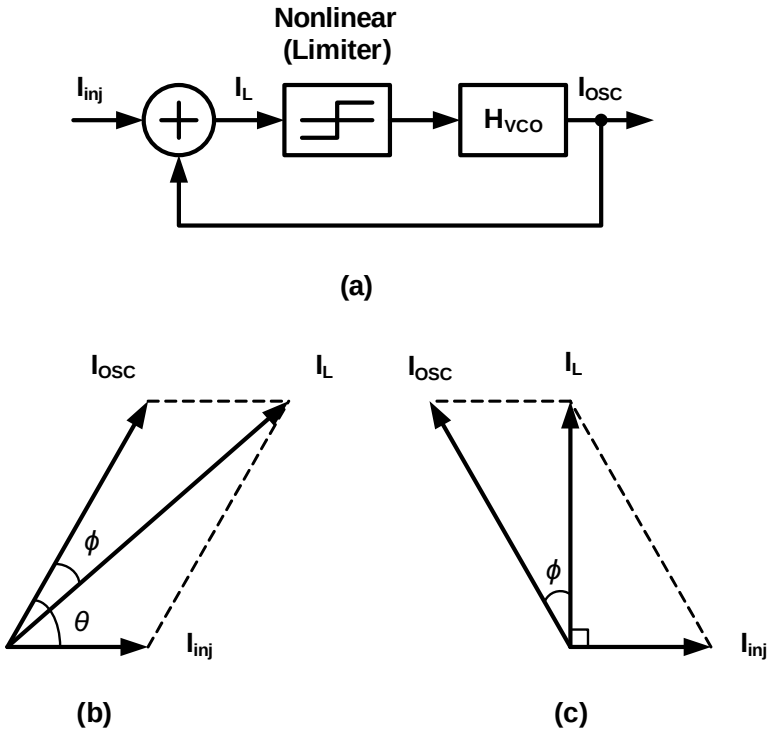

Figure 3.1: Injection Locking: (a) oscillator model, (b) phase shift diagram, and (c) phase shift diagram on the boundary of locking range.

$$I_{inj} = |I_{inj}|e^{j\omega_{inj}t} \tag{3.1a}$$

$$I_{osc} = |I_{osc}|e^{j\omega_{inj}t+\theta} \tag{3.1b}$$

$$I_L = I_{inj} + I_{osc} \tag{3.1c}$$

where θ is the phase shift between I_{inj} and I_{osc}. Let ϕ the phase shift between I_L and I_{osc}, we can conduct geometric analysis and get:

$$\tan\phi = \frac{|I_{inj}|\sin\theta}{|I_{osc}| + |I_{inj}|\cos\theta} = \frac{K\sin\theta}{1 + K\cos\theta} \tag{3.2}$$

where K is the injection ratio $|I_{inj}|/|I_{osc}|$. We can further define:

$$A \equiv \frac{\tan\phi}{\omega_0 - \omega_{osc}} \tag{3.3}$$

Then, 3.2 can be rewritten as:

$$A\left[(\omega_{osc} - \omega_{inj}) - (\omega_0 - \omega_{inj})\right] = \frac{K\sin\theta}{1 + K\cos\theta} \tag{3.4}$$

In (3.4), $(\omega_{osc} - \omega_{inj})$ is the instantaneous frequency difference $\partial\theta/\partial t$, and the $(\omega_0 - \omega_{inj})$ is the inherent frequency difference $\Delta\omega_0$. We rewrite (3.4) as:

$$\frac{\partial\theta}{\partial t} = -\frac{1}{A}\frac{K\sin\theta}{1 + K\cos\theta} + \Delta\omega_0 \tag{3.5}$$

In locking state, ω_{osc} is equal to ω_{inj}. $\partial\theta/\partial t$ is zero. The locking equation can be obtained:

$$\Delta\omega_0 = \frac{1}{A}\frac{K\sin\theta}{1 + K\cos\theta} \tag{3.6}$$

(3.6) illustrates the relationship between frequency deviation $\Delta\omega_0$ and angular phase shift θ in ILO. The maximum $\Delta\omega_0$ is occurs when $\cos\theta$ is equal to $-K$:

$$\Delta\omega_{0,max} = \frac{1}{A}\frac{K}{\sqrt{1 - K^2}} \tag{3.7}$$

(3.7) defines the locking range of ILO. With a low injection ratio K, we can assume $K\cos\theta << 1$. The angular phase shift θ versus $\Delta\omega_0$ can be acquired from (3.6):

$$\theta \approx \sin^{-1}\left(\frac{A}{K}\Delta\omega_0\right) \tag{3.8}$$

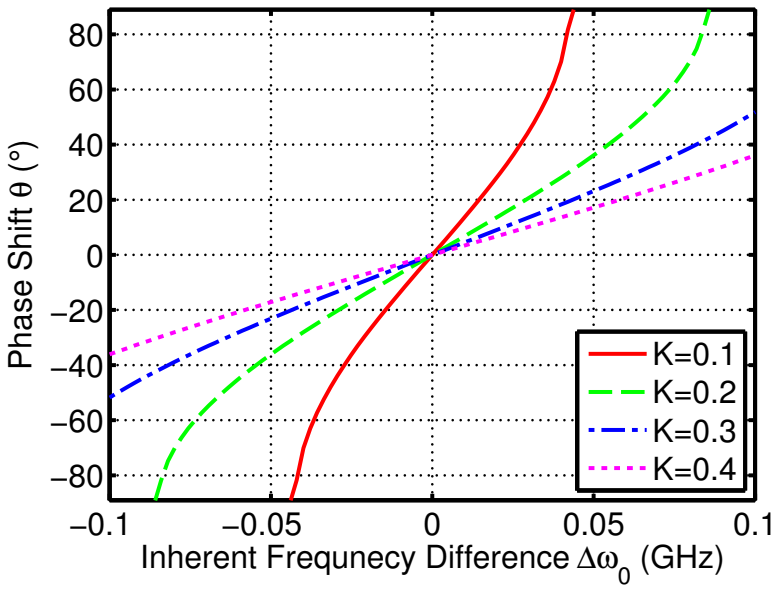

Figure 3.2: ILO phase shift versus inherent frequency difference ($\Delta\omega_0$).

Fig. 3.2 shows the curve of angular phase shift versus the VCOs resonant frequency. Notice that although the nonlinear relationship occurs at large $\Delta\omega$, the curve is quite linear when injected frequency ω_{inj} is closed to resonant frequency ω_0. (3.3) can be rearranged:

$$A \cong -\frac{d\tan\phi}{d\omega}|_{\omega-\omega_0} \tag{3.9}$$

where ϕ is the phase shift of H_{vco} to compensate the inherent frequency difference $\Delta\omega_0$. Therefore, A is dependent on the VCO architectures. In the case of LCOs, A is expressed as [32]:

$$A_{LCO} = \frac{2Q}{\omega_0} \tag{3.10}$$

where Q is quality factor of LC tank circuit. In the case of ROs, A is expressed as [35]:

$$A_{RO} \cong \frac{n}{2\omega_0}\sin\left(\frac{2\pi}{n}\right) \tag{3.11}$$

where N is the number of delay cells in RO. Since the nominal Q in CMOS technology is around 4 to 5, A_{LCO} is larger than A_{RO} in general. Thus, as shown in (3.7), IL-RO would have larger locking range than that in IL-LCO.

3.3 ILO-Based Time to Digital Converter (ILO-TDC)

Fig. 3.3 shows a single channel of proposed ILO-TDC. It contents a CTDC counter, a FTDC counter (ILO), and two 14-bit time registers. The CTDC counter is a 10-bit gray code counter, CTDC[9:0], that is triggered by a 1.2GHz reference clock (f_{REF}). The FTDC counter is a eight-stage injection-locked ring oscillator (ILRO) that generate 16-phase reference clocks for FTDC (f_{ILO}[15:0]). The oscil-lation frequency of f_{ILO}[15:0] is locked at 1.2GHz by f_{REF}. Sliding-scale technique is applied in the design. Time information is recorded by 14-bit START and STOP registers, respectively. In FTDC, time information is resolved by a phase-edge detec-tor (PED) that convert f_{ILO}[15:0] into a 4-bit binary code (FTDC-START[3:0] and FTDC-STOP[3:0]) where the PED is composed of eight SA and a 16-to-4 priority encoder as shown in Fig. 3.3(b). The operation waveform of ILO-TDC are shown in Fig. 3.4. The resolution of ILO-TDC is defined as the time difference between two neighbor f_{ILO} phases that is 52.1-ps in this design. A more detail discussion about the physical design of ILO will be presented in Section 4. Fig. 3.5 shows the simplified schematic of eight-stage ILRO. Although the phase noise of RO is worse than LC oscillator, RO has several advantages: multiple phase output, smaller layout area, and wider locking range. The current-starved delay cells are used for improving power noise rejection and increase the tolerance to the variant IR-drop. In injection locking design, a pseudo-differential buffer converted the single-ended f_{REF} into differential which are injected into two complementary oscillator nodes (f_{ILO}[0]

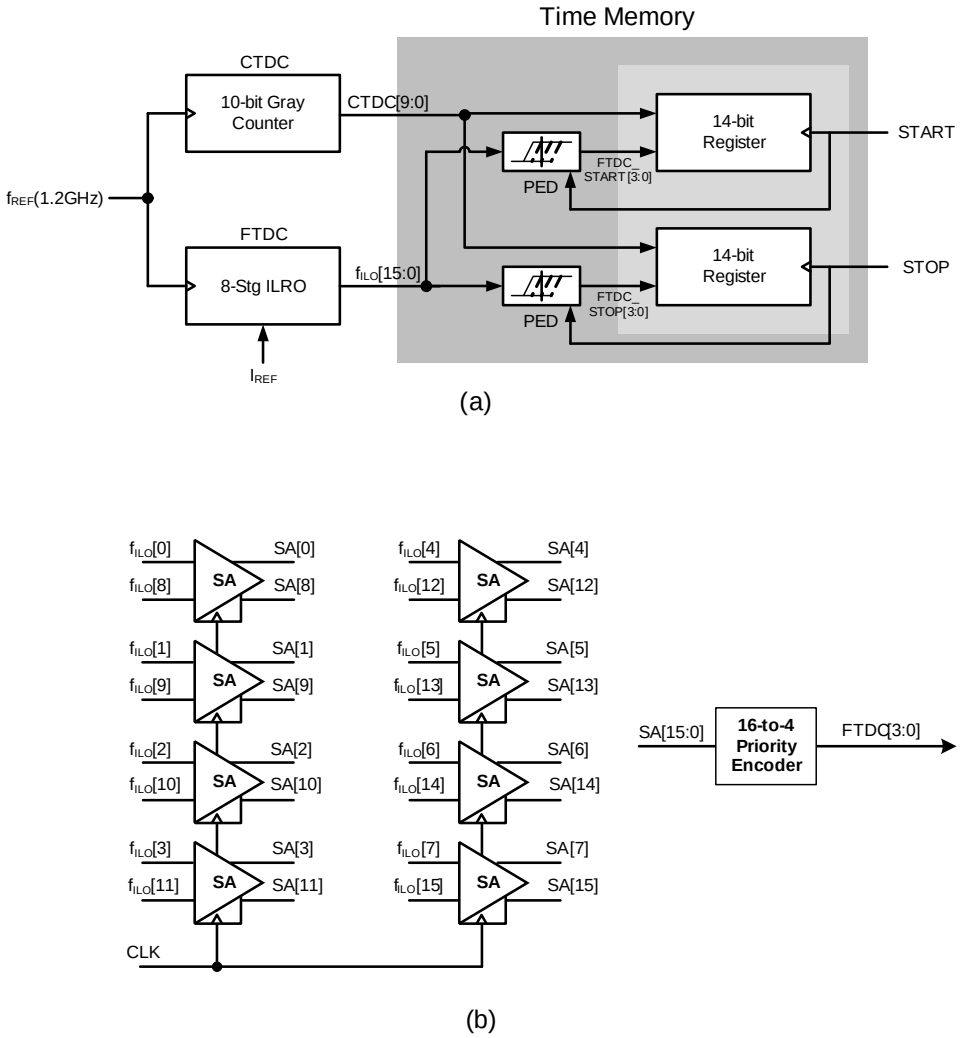

Figure 3.3: Single channel ILO-based TDC: (a) block diagram, (b) schematic of phase-edge detector.

and $f_{ILO}[8]$) through ac-coupling. AC-coupled injection results more uniform output phase spacing, comparing to DC-coupled injection [36].

The extended array of ILO-TDC topology with 32 input channels are shown in Fig. 3.6. In the extended version, it contents 1) 32-TDC registers that support 32 input channels, 2) a global CTDC gray code counter (CTDC[9:0]), 3) eight ILOs

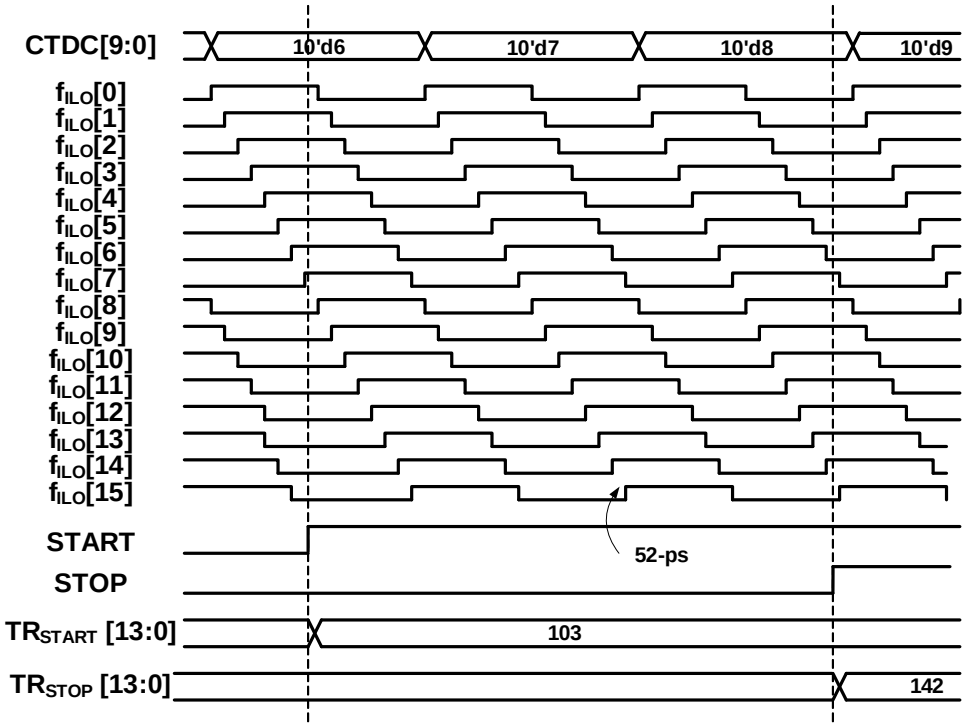

Figure 3.4: Operation waveform of ILO-TDC.

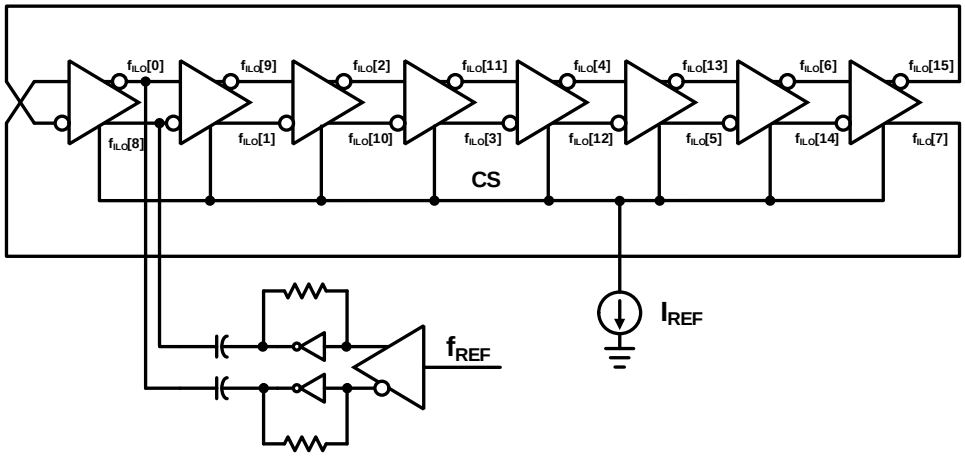

Figure 3.5: Schematic of eight-stage ILRO.

that generates local 16-phase reference clocks (f_{ILO}[15:0]) for FTDC, 4) a global distribution circuit that distributes CTDC counter value and ILOs injection locked

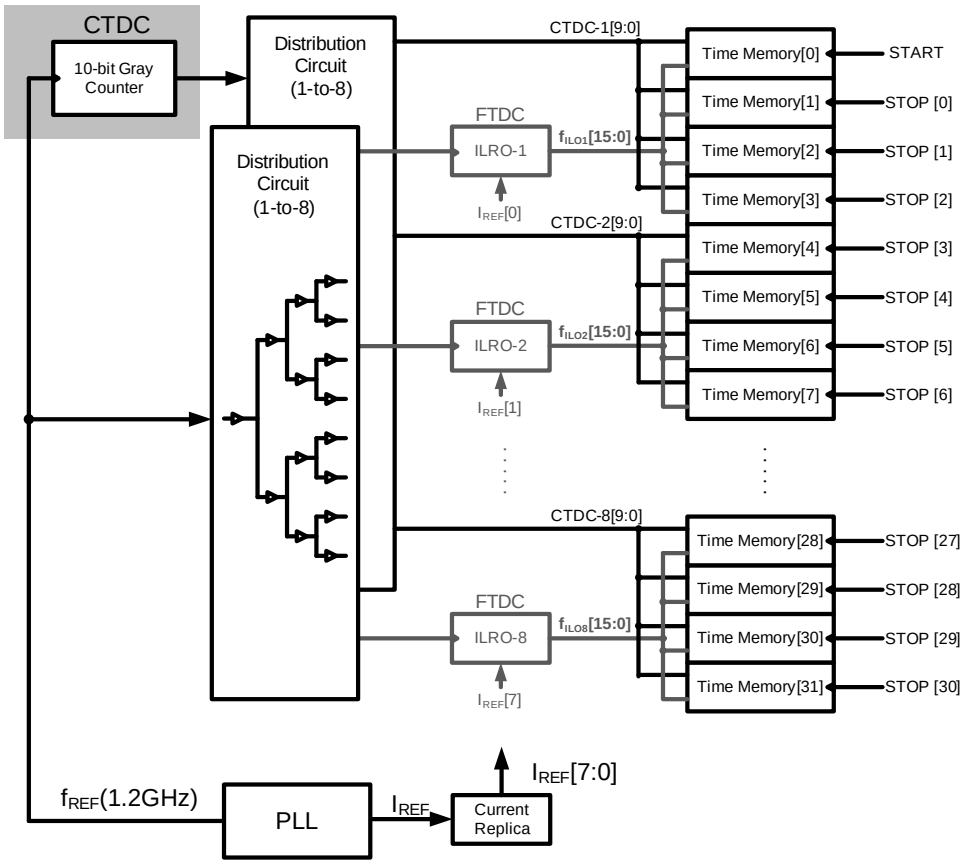

Figure 3.6: 32-channel ILO-TDC array.

clock (f_{REF}), and 5) 32-to-1 multiplexer readout circuit.

Unlike most topology where the CTDC ripple-counter is designed in the TDC array [26, 37], CTDC[9:0] is generated from a global Gray-code counter and shared by whole TDC array. This design reduces the power consumption of CTDC counting. Reference clock f_{REF} is generated from an on-chip 1.2GHz PLL that triggers the Gray-code counter and locks the eight ILOs. CTDC[9:0] as well as f_{REF} are distributed through a global distribution circuit which is a 4-stage 1-to-8 clock tree buffers. Each ILO is shared by 4-TDC channels. The number of sharing is optimized based on power and the driving capability of ILOs.

In order to calibrate the global PVT variation and IR-drop variation that could induce the deviation of f_{ILO} and impact LSB of FTDC time conversion, the ILO is implemented by a current controlled oscillator (ICO), instead of voltage controlled oscillator (VCO). The bias current I_{ref} of each ILO is generated by the PLL. The ICO design provides better immunity to the IR-drop variation than VCO. In array-based design, since some ILOs are physically far away from each other, a significant power and ground IR-drop can be induced between these two locations. In current control, the bias condition in ILOs would not change with the IR-drop if an identical amount of bias current is used. However, in voltage control, since the controlled voltage (V_C) is respect to the potential of local ground, the biasing condition will be different in ILOs if a serious IR-drop variation presents. The cost of ICO topology is the extra dc power consumption in the biasing circuit.

3.4 FTDC Power Analysis

In order to quantify the power improvement in FTDC clock distribution, we compare the power of ILO-TDC with the other competitor architectures at the same specifications. The FTDC specifications support 32-TDC channels, 52-ps time resolution, and 4-bit dynamic range at 1-V supply. Power estimation of each architecture is calculated based on the parasitic parameters in 65nm CMOS technology and confirmed with circuitry simulation. Four architectures were compared in this analysis (Fig. 3.7):

Type-I. Global Counting driven by Single-Stage Buffer [5, 6]: It is the simplest distribution technique among the four architectures. The 16-phase reference clocks (f_{REF}[15:0]) are distributed through single stage buffering. Since the physical distance of distribution traces is quite huge (800-μm in the case of 25-μm TDC

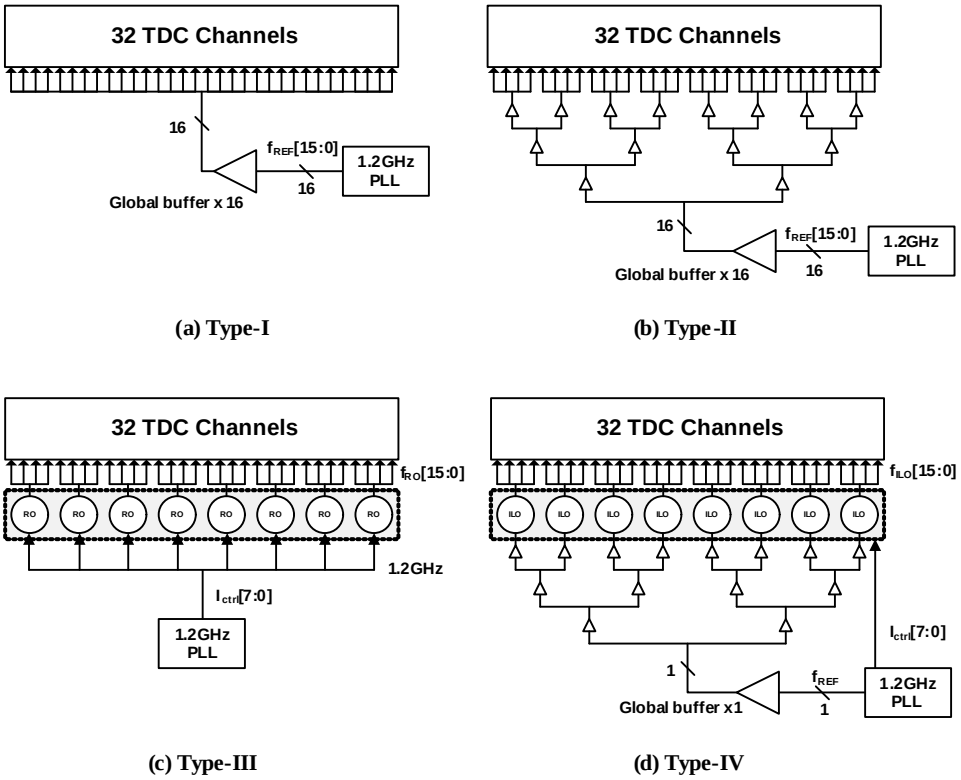

Figure 3.7: Four clock distribution architectures: (a) Type-I: global counting driven by single-stage buffer, (b) Type-II: global counting driven by multi-stage buffers, (c) Type-III: local counting driven by ring oscillators (ROs), (d) Type-IV: local counting driven by injection locked ring oscillator (ILROs).

column pitch), the parasitic loading on the trace is considerable. According to the 65nm parasitic parameters, a total capacitance of 700fF and resistance of 220 Ω are observed on the global trace. Each global buffer also induces a 100fF parasitic capacitance at output. To achieve 52-ps time resolution, the frequency of f_{REF} should be as high as 1.2GHz which will consumes dynamic power (CV^2f) 1080μW per f_{REF}, and 17.28mW for the 16 phases (f_{REF}[15:0]). Although this power level seems acceptable, the single-stage buffering has several disadvantages. First, according to lumped RC equation ($t_{10\%-90\%} = 2.2RC$), the signal transient time on the trace is close to 339-ps that will cause considerable amount of random jitter on f_{REF} and

affect the single-shot precision of TDC. Second, signal propagation time from the buffer to the end of trace is larger than one LSB (52-ps) that causes a process-dependent offset among TDC array. Third, single-stage buffering is hardly used in large sensor array. This is because the effect of transmission-line will be serious as the trace length increases. In summary, single-stage buffer limits TDC array size and the pixel array size in LIDAR sensor.

Type-II. Global Counting driven by Multi-Stage Buffers: In order to solve the problem encounter in the Type-I, we can use multi-stage buffers to distribute f_{REF}[15:0]. For example, the buffer in Fig. 3.7 (b) is a 4-stage 1-to-8 clock-tree buffers that can assure the same propagation delay to each TDC column. Since the distribution path is separated into several stages, the loading of each stage decreases at least by 2^N times where N is the Nth-stage buffer. Thus, it preserves better signal integrity. However, this architecture consumes significant power since the total parasitic loading of four-stage buffer is higher and the number of buffers is increased. The simulated power consumption of the four-stage buffers in Fig. 3.7 (b) is 48-mW that is approximately three times higher than the Type-I.

Type-III. Local Counting driven by Ring Oscillators (ROs): Instead of distribute f_{REF}[15:0] globally, there are eight ROs utilized in TDC array to generate local reference clocks (f_{RO}[15:0]) and avoid the long-trace distribution. Design of RO is similar to that in Fig. 3.5, except the absence of injection lock buffer. Eight delay cells are implemented in RO to achieve 16-phase f_{RO} output where the oscillation frequency is 1.2GHz. Each RO is shared by four TDC columns, the number of sharing is dependent on the driving capability and power budget of RO. The eight RO reference current bias (I_{ref}[7:0]) are generated from PLL to calibrate the PVT variation. Simulated power of each RO is 1.3mW. Thus, the total power consump-

tion for 8-ROs is 10.4mW. It is much improved comparing to the global counting architectures (Type-I/II). The problem of RO-based counting is that the oscillation of the eight ROs are not synchronous so that the f_{REF}[15:0] are not in phase among different ROs that induces an column fix pattern noise (CFPN) in TDC channels.

Type-IV. Local Counting by Injection Locked Ring Oscillator (IL-ROs): Our proposed ILRO-based TDC solves the phase asynchronous issue in the Type-III. The frequency and phase of ILROs can be locked and synchronized by an injection locked clock. In Fig. 3.7 (d), the local oscillator in Type-III are replaced by eight ILROs in Type-IV. The oscillation frequency of ILROs is locked by f_{REF}. The total power of the Type-IV can be broken-up into 1) eight ILROs (each consumes 1.5mW, including an the 200μW consumption in injection locked buffer), and 2) f_{REF} distribution buffer 3mW. The total power consumption is 15mW.

Fig. 3.8 summarize the power consumption per channel of the four architectures. Notice that the Type-III consumes the least power but it has several issue such as

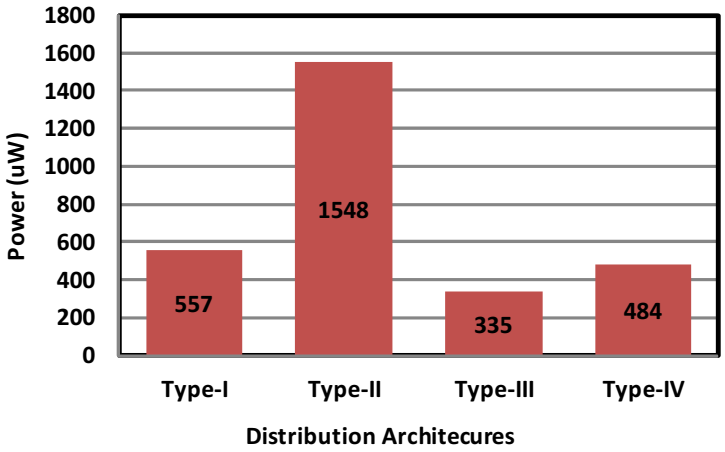

Figure 3.8: The simulated power/channel of the four clock distribution architectures.

poor channel uniformity and fix pattern noise that we mentioned above. Type-I is acceptable but the signal integrity on the global clock trace is poor and the architecture is hardly used in large sensor array. The four-stage buffers in the Type-II divides the parasitic capacitance into several segments and minimize the loading at each stage. However, the cost is the significant power consumption since the total parasitic is increased. Finally, ILO-TDC (Type-IV) consumes power 1.44× higher than the Type-III. However, it provides a injection-locked reference frequency locally. Also, the ILO-TDC saves the power by 70%, comparing with Type-II.

The Monte-Carlo simulated oscillation waveform of free-running RO (f_{RO}) and IL-RO (f_{ILO}) locked by an 1.2GHz injection-locked clock are shown in Fig. 3.9. We can notice that the oscillation phases are asynchronous in free-running RO, while well-synchronous in IL-RO. Fig. 3.10 shows the statistic distribution of f_{RO} and

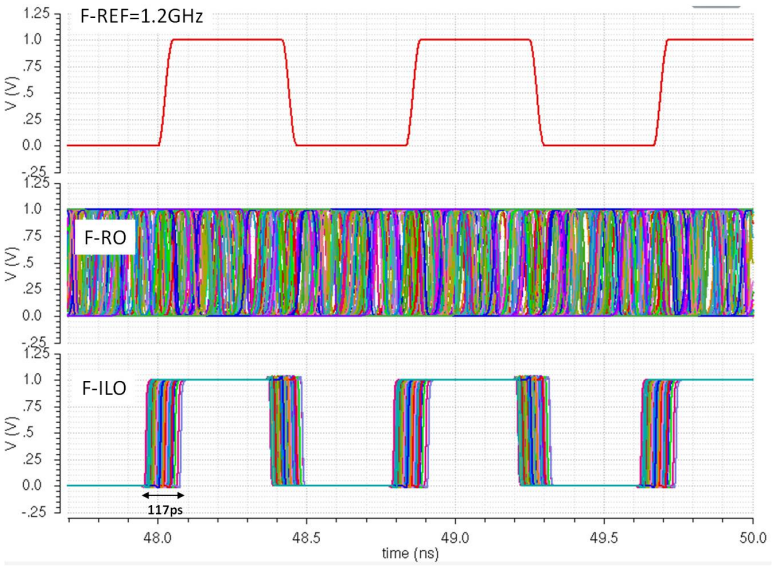

Figure 3.9: Oscillation waveform of free-running RO (f_{RO}) and IL-RO (f_{ILO}) locked by an 1.2GHz injection-locked clock in Monte-carlo simulation (number of sample=200).

f_{ILO}. In RO, a 5% variation in the oscillation frequency (f_{RO}) is observed. In ILROs, a very small f_{ILO} variation ($< 0.001\%$) is achieved. The comparison shows the advantage of ILO-TDC in terms of power budget, time resolution, and timing accuracy.

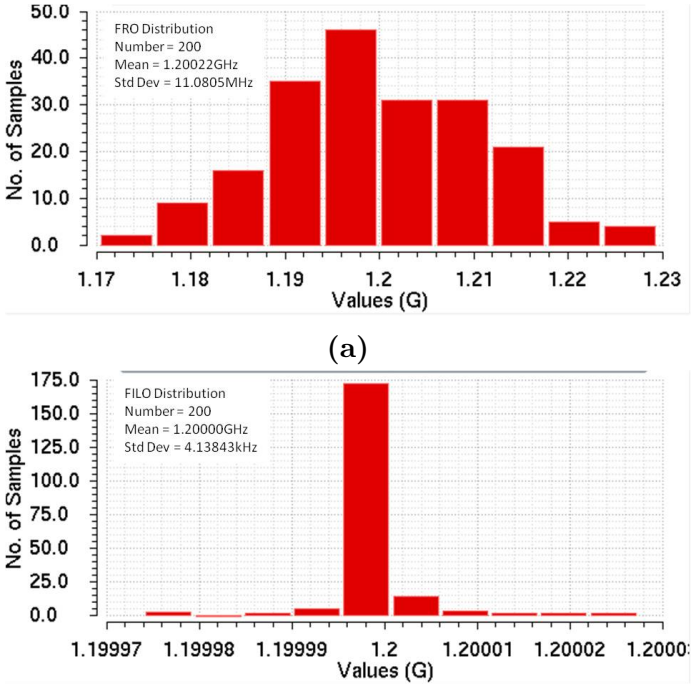

Figure 3.10: Statistic distribution of (a) free running RO and (b) ILO with injection locked by an 1.2GHz external clock in Monte-carlo simulation (number of sample = 200).

4. PROPOSED LIDAR SENSOR

The goal of this work is to design and demonstrate a long-range LIDAR sensor system-on-chip (SoC) that supports sub-centimeter ranging precision. The target applications of the proposed LIDAR sensor are in the automotive, providing the depth-imaging for the systems like advanced driver assistance system (ADASs) or driverless system. Sub-centimeter ranging precision offers higher resolution for featuring the sensing objects in environment that allows the background algorithm to make accurate decision when risks are detected. The pulse-based architecture is adopted, instead of the modulation-based, since it has high dynamic range, higher conversion speed and better capability to deal with multiple echos.

Fig. 4.1 shows the block diagram of the proposed pulse-based LIDAR sensor prototype. It contents a 31×2 pixel channel array, a TDC-Core, and a Digital-Core. The pixel channel array is the input of LIDAR sensor. Each pixel channel has one front-end receiver (RX) that is responsible for sensing the photocurrent pulse and amplifying it to a full-swing signal in order to trigger TDC-STOP time. The pulse signal from RX is regenerated through a bit-line (BL) buffer that generates a well-defined pulse width at output at every pulse input to improve signal integrity.

In TDC core, there are 32-channels of TDCs that support 32 time events at once. Each TDC channel offer 14-bit dynamic range (DR). Sliding scale technique is utilized to improve linearity of time conversion. The first TDC column (TDC-START) records the START time and the other 31 TDC columns (TDC-STOP) record the 31 time events from pixel array. TDC design follows two-stage conversion (CTDC and FTDC) for pursuing both high resolution and DR. As the architecture

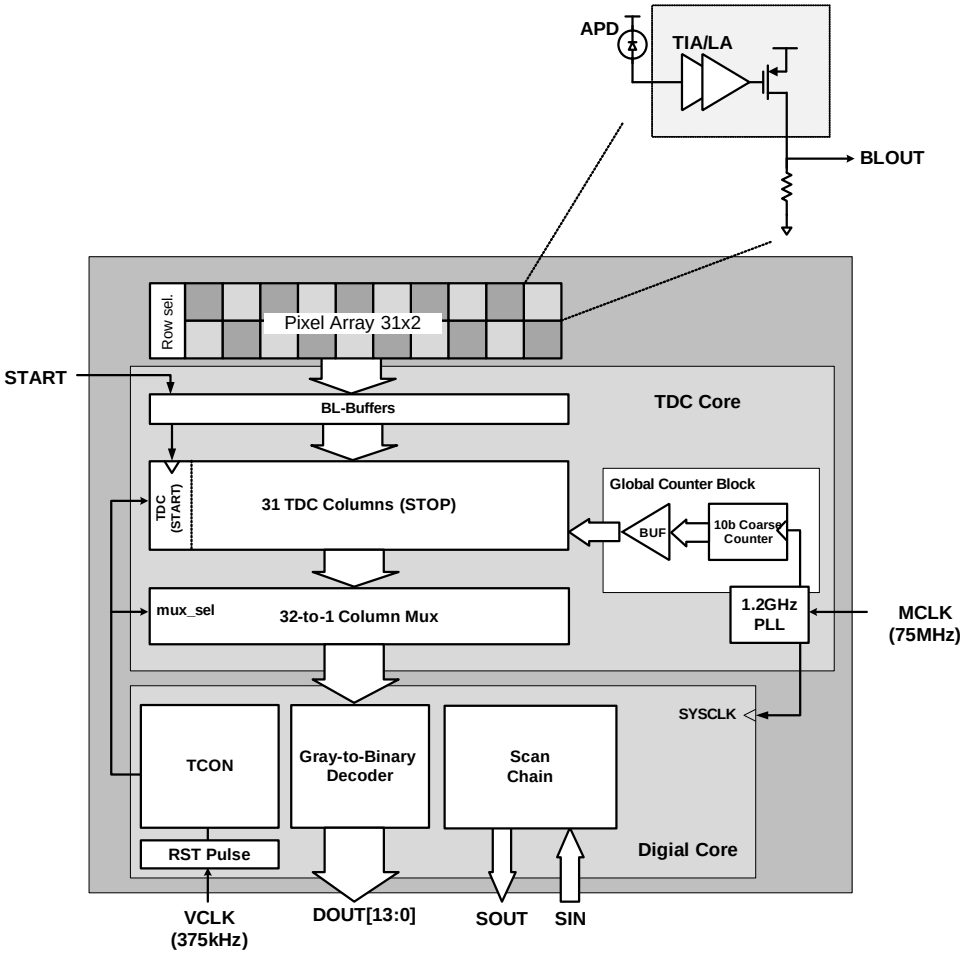

Figure 4.1: Block diagram of proposed pulse-based LIDAR sensor prototype.

we described in Section 3, CTDC is implemented by a global 10-bit gray-code counting and FTDC design is based on ILO-based TDC. TDC reference clock is generated from an on-chip 1.2-GHz PLL. This clock is used as the synchronous clock for the global gray code counter and the injected clock of ILOs. After conversion is finished, the 32 TDC output are read out through a 32-to-1 Column multiplexer.

In the Digital Core, timing controller block (TCON) generates timing signals for the whole LIDAR operation. Gray-to-binary decoder converts CTDC gray code to binary code output. A scan-chain block allows for setting chip register value

from background computer. The maximum TDC conversion rate of each row is 375kHz,which is synchronous with VCLK. In a 31x32 pixel array, the conversion rate is able to support 10000 frame per second (fps).

4.1 Pixel Channel Array

Pixel channel array size in this prototype is 31x2. Although this array size is small, a higher resolution of depth image can be achieved through laser scanning approach. In each pixel channel, a front-end receiver is utilized to convert DP photocurrent into a full-swing voltage signal. Fig. 4.2 shows the floor-plan for the 31x2 array. The pixel channels in first row are connected to off-chip APDs, while the second row are connected to the photodiode emulators (PDEM) for testing. Since the purpose of this work is to demonstrated a LIDAR sensor prototype, the photodiodes are not integrated on chip. Alternatively, a commercial 4×2 InP APD array photonic chip is off-chip bonded to the eight pixel channels in the first row, while the remaining 24-pixel channels are left idle. The APD pixel diameter is 32um with the pixel pitch of 250um. The APDs are reversed biased at 24V for the multiplication gain (M) of 10. The PDEMs in the second row generate a 5-ns current pulse current

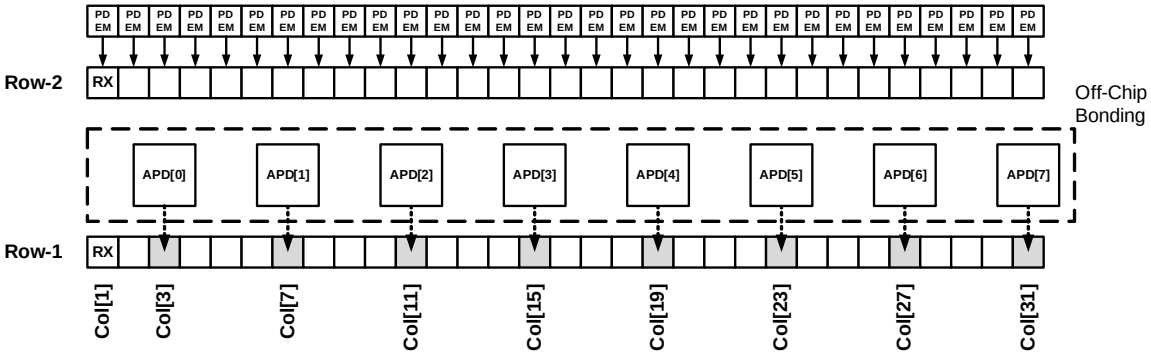

Figure 4.2: Floor-plan of the 31×2 pxiel channel array.

as triggered by a testing circuit to emulate transient behavior of on-chip APD. The emulated dark current and photocurrent are programmable so that we are able to characterize the sensitivity of front-end receiver.

4.2 Front-end Receiver

The single-ended CMOS inverter TIA/LA receiver (RX) is shown in Fig. 4.3. Although the single-ended RX is vulnerable to power supply noise, it consumes less chip area (25μm$\times 21\mu$m per channel) and lower power consumption [38] which is especially important in array-based design. In order to reduce power noise coupled from other circuits, RX power PVDD is separated from the other blocks of the chip. TIA is implemented by an inverter (I_1) and a feedback resistor (R_{F1}). The simulated TIA gain is 2.6kΩ and 3dB-bandwidth (3dB-BW) is 1.5GHz at 120fF input capacitance loading. LA is implemented with 2-stage inverters (I_2 and I_3) with a resistor feedback (R_{F3}) around I_3 to boost the BW. The simulated LA gain is 10dB and 3dB-BW is 14GHz. The offset cancellation is done by the common-mode feedback (CMFB) circuit that generates the common-mode level for TIA input. A 5.3MHz cut-off frequency is implemented by a RC low-pass filter (LPF) with miller-boosted capacitor by I_4. The output of LA is amplified by another 2-stage inverters (I_6 and I_7) and converted into a full-swing signal to control the output stage.

The output stage is a PMOS open-drain buffer that allows for the bit-line (BL) sharing among the pixels on the same column. CMFB, which is well defined through the aspect ratio of NMOS and PMOS in I_6, can assure that PMOS open-drain buffer is off as no photon flux is detected. The CMOS inverter RX has a full-swing output signal at 50uA photocurrent input (This is equivalent to -20dBm optical power at APD M=10, R=0.8), 1.5GHz BW, and 1uArms input-referred noise in simulation.

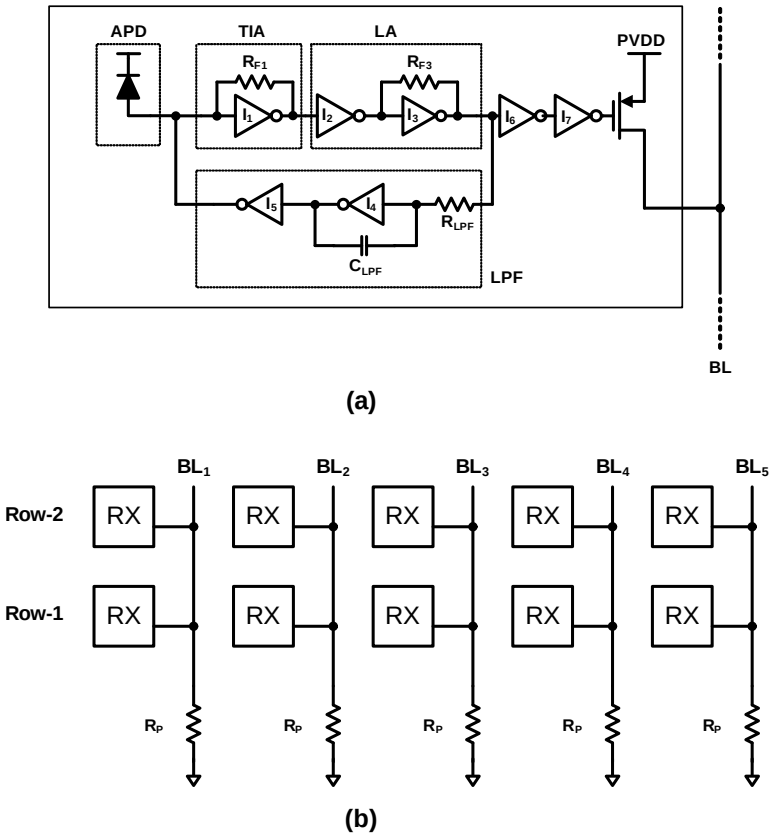

Figure 4.3: APD front-end receiver: (a) schematic of single-channel receiver, (b) receiver output with bit-line sharing.

The RX active power is 300μA. A powerdown function is implemented in row-base to turn-off RXs at idle mode.

4.3 Bit-line Buffer

In pulse LIDAR sensor, the returned power varies with the travel distance and return angle of light beam. For instance, the pulse that returns from a near relfector has higher power than that returns from a far relfector. This variable optical power could induce the variant electrical pulse-width in APD response and cause reliability issue in circuitry. Assuming a return pulse that has power of the sensitivity level

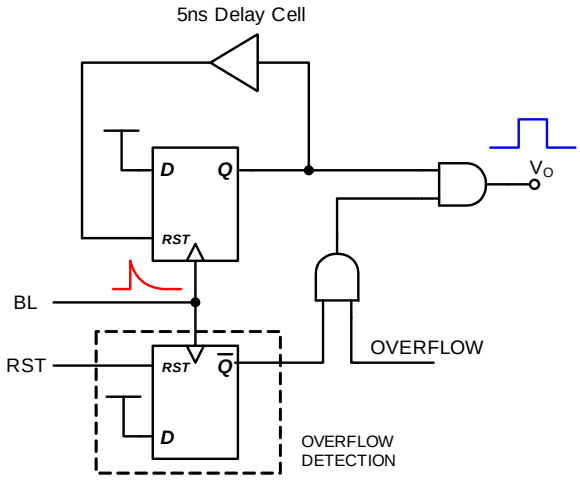

Figure 4.4: Schematic of bit-line (BL) buffer.

of front-end RX, the responsible electrical pulse at RX output would not be a full-swing signal. After propagating through multiple inverter buffers, the pulse can be trimmed into a short pulse width. Thus, time violation could happen in TDC if the signal pulse at RX output is directly used as the STOP signal. To avoid the short pulse width, a bit-line (BL) buffer is added before TDC STOP input. The purpose of BL-buffer is to detect the positive-edge transition from BL signal and regenerate a well-defined pulse width (and pulse edge) to trigger STOP input in TDC.

Fig. 4.4 shows the schematic of BL-buffer. As the BL pulse triggers, DFF passes one from input D to output Q and holds this state until RST is triggered by a 5-ns delay buffer. In this design, the pulse width at the output of BL buffer is independent from the input. Fig. 4.5 shows the co-simulation of front-end RX and BL-buffer. The input photocurrent of RX is swept around the detection threshold of front-end RX from 14μA to 15.5μA. Since the photocurrent smaller than 15μA is lower than detection threshold, the related RX output is not a full-swing signal. BL-buffer senses the output of RX. As the amplitude of pulse is large a threshold

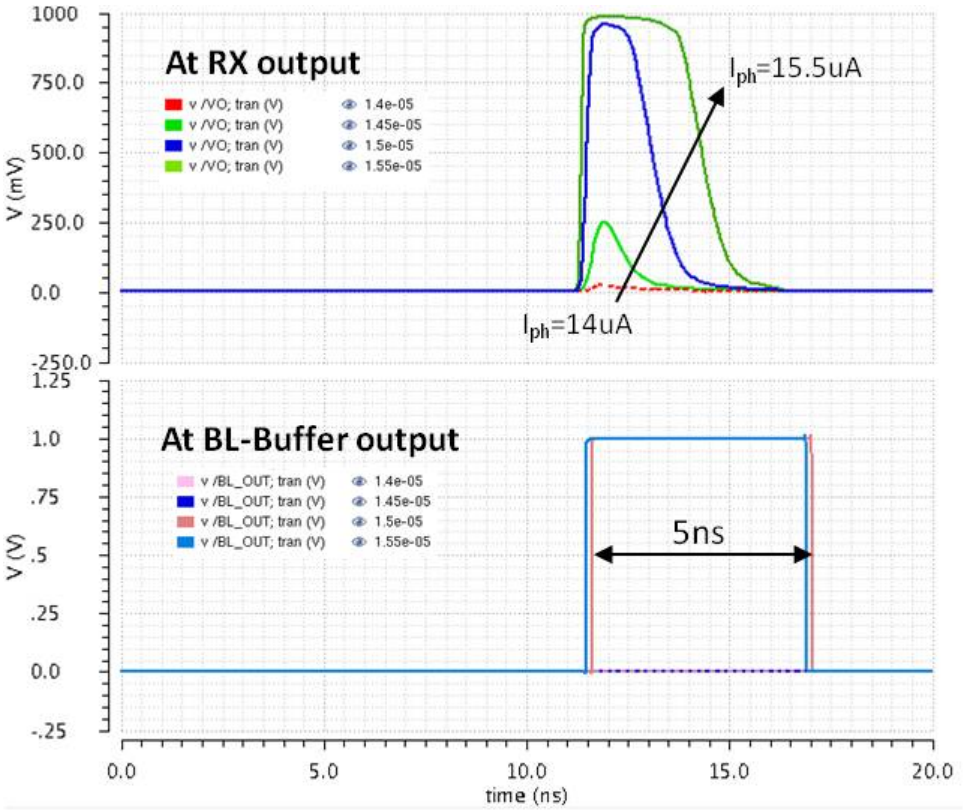

Figure 4.5: Pulse regeneration though BL-buffer. The simulated photocurrent is swept around the detection threshold of front-end RX from 14μA to 15.5μA. BL-buffer senses the RX output and regenerates a 5ns pulse when I_{ph} is larger than 15μA and filters out the I_{ph} lower than it.

at the input of BL buffer, the BL buffer is triggered and regenerated a 5ns pulse at output. However, if if the pulse is smaller than the threshold, BL-buffer filters out the pulse and no pulse regeneration at output.

4.4 Time-to-Digital Converter

Fig. 4.6 shows the block diagram of 32-TDC columns. Sliding scale technique is utilized to improve linearity of time conversion. Thus, the input of first TDC column (TDC-0) is START time event and the rest TDC columns record the STOP

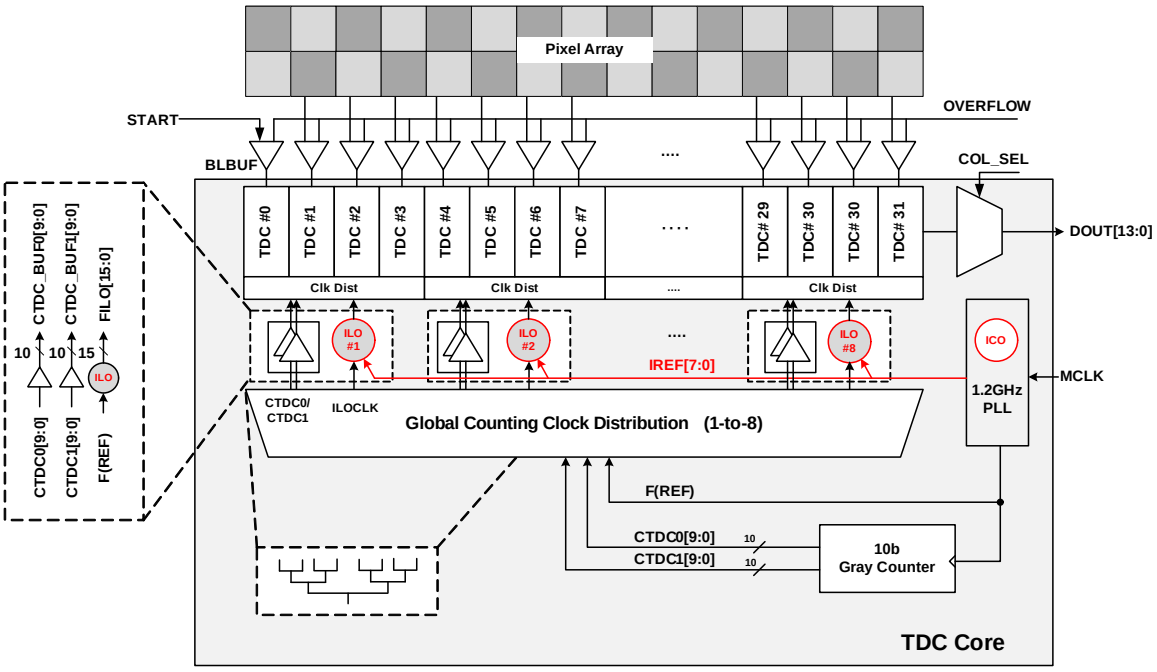

Figure 4.6: The block diagram of 32-TDC columns design.

time event triggered from the pixel channel array. TDC design is based on the two-stage conversion topology we discussed in Section 3, including 10-bit CTDC and 4-bit FTDC to enlarge dynamic range (DR). Each TDC supports 52-ps time resolution and 852-ns dynamic range. CTDC is implemented through a 10-bit global gray-code counter that is driven by a 1.2GHz PLL clock (f_{REF}). It is equivalent to 833-ps counting period (coarse LSB). A four-stage 1-to-8 global distribution circuit is utilized to distribute coarse counting signals into 32 TDC columns. FTDC reference clocks are distributed by eight local 1.2GHz ILOs in TDCs where each ILO is shared by 4-TDC columns. The adapted replica reference current (I_{REF}[7:0]) is generated from PLL to calibrate the global PVT variation among ILOs. ILO-based TDC supports 52-ps fine LSB.

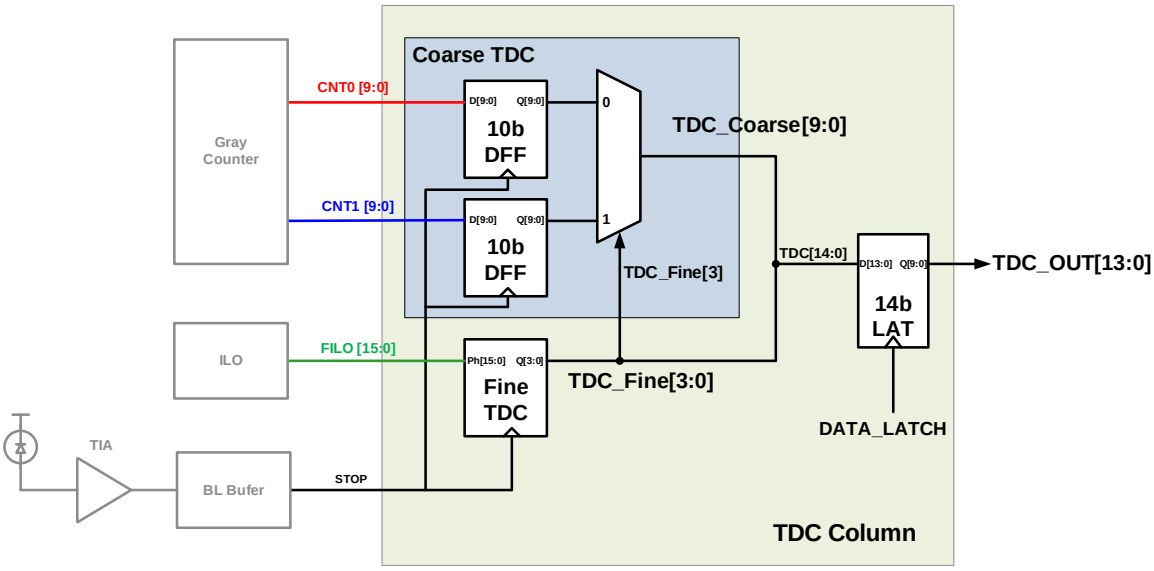

Figure 4.7: Schematic of single TDC column circuit.

4.4.1 TDC Column

The schematic of single TDC column is shown in Fig. 4.7, which contents two 10-bit CTDC registers and one 4-bit FTDC edge detector. In CTDC, the double counting scheme is applied to improve the linearity of TDC, which will be discussed later in Section-4.4.2. Two coarse counter values (CNT0 and CNT1) are latched by two correlated 10-bit DFFs when STOP triggers. Final coarse output (CTDC [9:0]) will be selected by the MSB of FTDC (TDC-Fine [3]). In FTDC, the input are 16-phase 1.2GHz reference clocks from ILO (f_{ILO} [15:0]). An edge detection is utilized to convert the phase information into 4-bit binary code. After the time conversion is done, 14-bit TDC output (TDC [13:0]) will be read into the second-level (L2) register. Serial 14-bit TDC output is read out by a column multiplexer circuitry at 18.75MHz (not shown). The L2 register allows the pipelined process, where time conversion and data read-out can be operated at the same time.

4.4.2 CTDC Counter

CTDC counter is implemented by a synchronous digital counter due to its high DR. As described in Section 2, DR of digital counter can be extended easily: two-time of DR can be achieved by adding one additional register. The counting rate is dependent on the clock triggering. In this work, a 1.2GHz PLL clock is used to trigger the CTDC counter that is equivalent to 833-ps counting period (LSB). To reduce chip size, the global-based CTDC counter is shared by whole TDC columns. Counter value are distributed into TDCs through a four-stage 1-to-8 distribution circuit.

Gray-code counting is applied here to eliminates the missing code issue in TDC and reduce the power of the distribution circuit. Fig. 4.8 shows the schematic of 10-bit CTDC ripple counter. Basically, the design follows the logic formula in Eq. 2.19. However, instead of converting binary code into gray code, the synchronous counter generates gray code directly. The first level (L1) registers are added between the two XOR gates to leverage the pipeline operation and extend maximum operating frequency, while the second level (L2) is to eliminate the signal glitch at counter output and improve signal integrity.

In asynchronous TDC design, a special attention was paid on the missing code issue caused by the phase misalignment between CTDC and FTDC counting signals. Since the TDC-STOP signal can be triggered at any time, the missing code issue can easily happens if counter signals are not aligned perfectly. An example to illustrate this issue is shown in Fig. 4.9. In Case-I, the CTDC and FTDC are perfectly aligned, the transition between two neighbor CTDC counting values will be linear. However, the perfect timing alignment is never exiting in the real circuit.

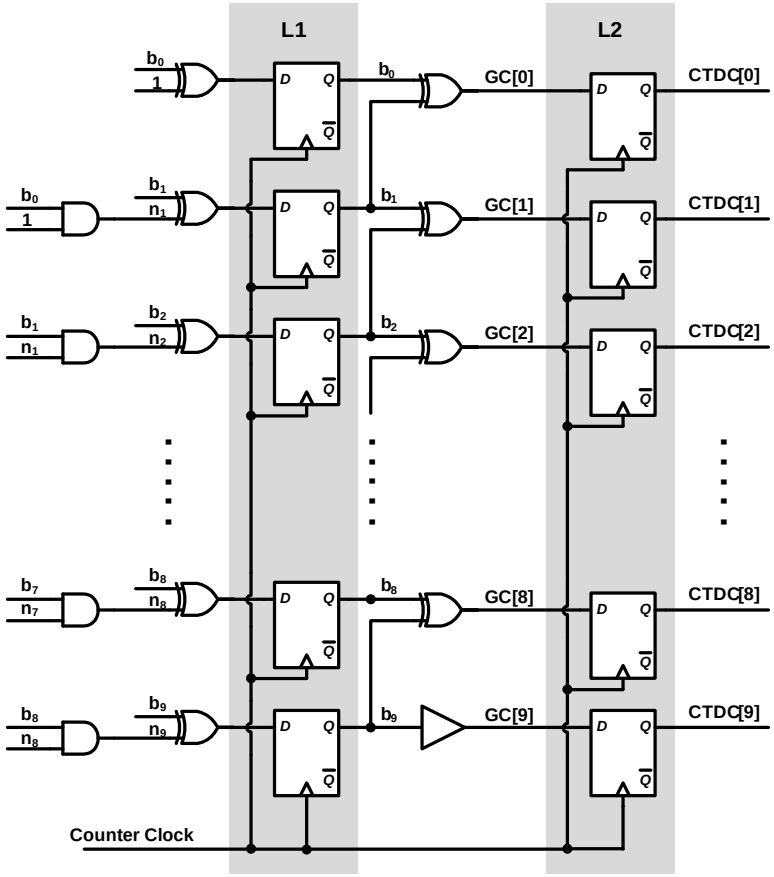

Figure 4.8: Schematic of CTDC Gray-code counter.

An inevitable phase shifting between CTDC and FTDC could induce missing code and nonlinearity behavior in two-stage TDC architecture (Case-II).

In order to prevent the missing code issue, a double counter scheme is applied here [5]. As shown in Fig. 4.10, two CTDC counters (CTDC0 and CTDC1) that have 180° phase shift with each other are generated globally. The purpose of this design is to allow TDC column record both present counter value (CTDC0) and previous counter value (CTDC1) while STOP triggers. The selection of these two counter values is according to FTDC results. If STOP triggers during T1 period, CTDC0 will be selected as final CTDC output. If STOP triggers during T2 pe-

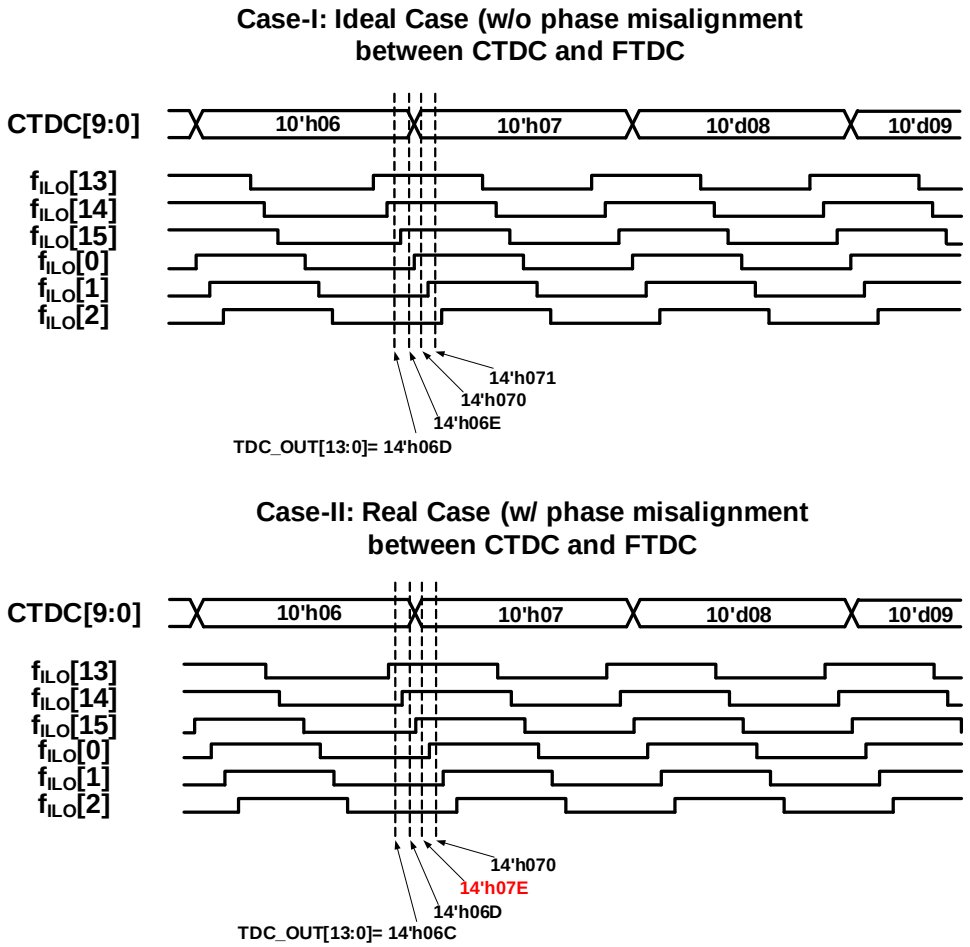

Figure 4.9: The example of nonlinear missing code induced by misalignment between CTDC and FTDC.

riod, CTDC1 will be selected as final CTDC output. Notice that since there is no transition for CTDC0 (CTDC1) during the T1 (T2) period, missing code issue can be eliminated if the phase misalignment between CTDC and FTDC is smaller than ±4LSB (±208ps). Although double counting technique requires an additional counting signals (CTDC1) and doubles the CTDC power, it greatly improves the linearity of TDC.

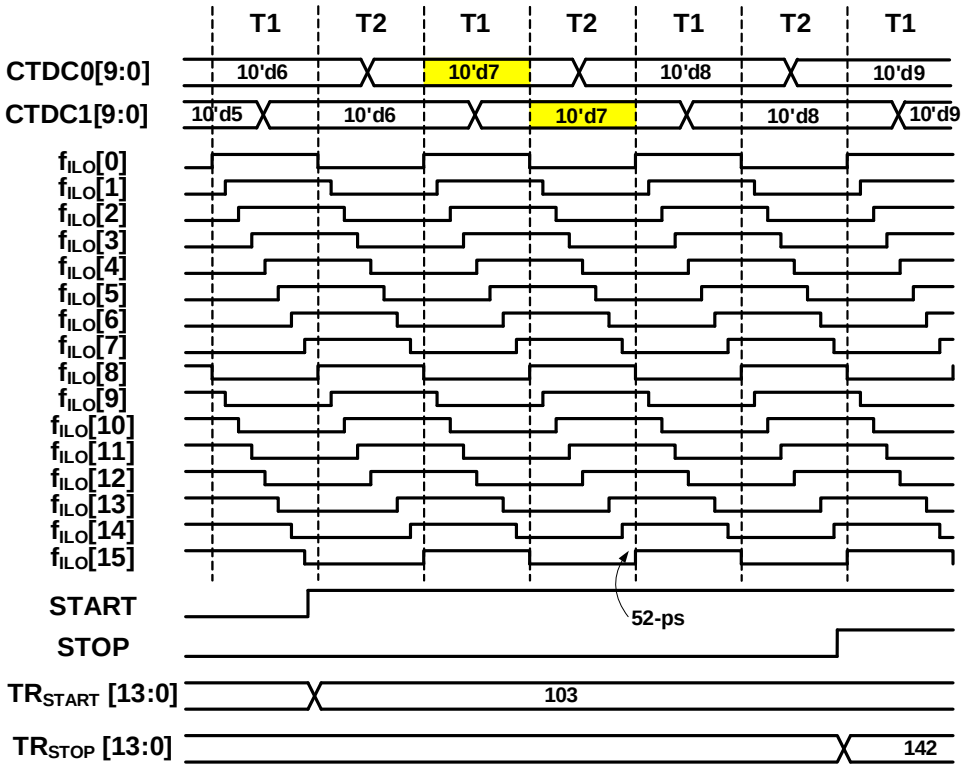

Figure 4.10: The timing diagram of CTDC and FTDC. The double counter scheme (CTDC0 and CTDC1) is implemented to solve misalignment issue between coarse and fine counters. If TDC STOP signal triggers at the time during T1 period, CTDC0 [9:0] will be selected as CTDC output. If TDC STOP signal triggers at time during T2 period, CTDC1 [9:0] will be selected as coarse-TDC output.

4.4.3 FTDC Edge Detector

As shown in Fig. 3.3 (a), The 16-phase FTDC ILO clocks f_{ILO} are fed into the eight strong-arm sense amplifiers (SAs) with one cascaded SR latch [39]. XOR-based edge detector is then used to detect the edge from high to low in SAs output. A embedded 2-bit bubble filter can filter out the bubble effect at SAs' output. Finally, the filtered edge detector output is converter into a 4-bit binary code by a 16b-to-4b priority encoder.

4.5 Injection-locked Oscillator (ILO)

Injection-locked oscillator provides the FTDC reference clocks. As mentioned in Section 3, ILO has the advantage in power, area, and timing jitter. The power of ILOs is much lower than the global driving since it performs clock distribution locally. Without the need for feedback loop control, ILO size is very competitive. Finally, since the embedded oscillator in ILO performs 1st-order jitter filtering, it rejects high frequency jitter and is less susceptible to power supply noise. Thus, time precision performance would be better than that from the global-driving buffers.

As shown in Fig. 4.7, eight ILOs are utilized to generate 16-phase FTDC reference clocks for 32 TDC columns: each ILO is shared by four TDC columns. The number of sharing is optimized based on power and the driving capability of ILOs. All ILOs are injection-locked by an 1.2GHz PLL clock (f_{REF}) that is distribute by 4-stage 1-to-8 clock tree buffer.

Fig. 4.11 shows the complete schematic of ILO. Oscillator is an eight-stage ring oscillator (RO). The single-ended injection locked clock F_{ref} is converted into pseudo-differential clock signal, and injected into two complementary oscillator stages through ac-coupling. In RO design, the current-starved delay cells are designed for improving power noise rejection and tolerance to the variant IR-drop. Each ILO consumes 1.5mW power where most of power is consumed by the level shifters at output. The could be much shrunk if removing the level shifters. However, by that it will requires higher sensitivity in the SAs at FTDC. The biasing current of ILO (I_{ref}) is adapted by on-chip PLL to calibrate PVT variation among ILOs.

Fig. 4.12 shows operating of PVT calibration in ILO clock distribution. It

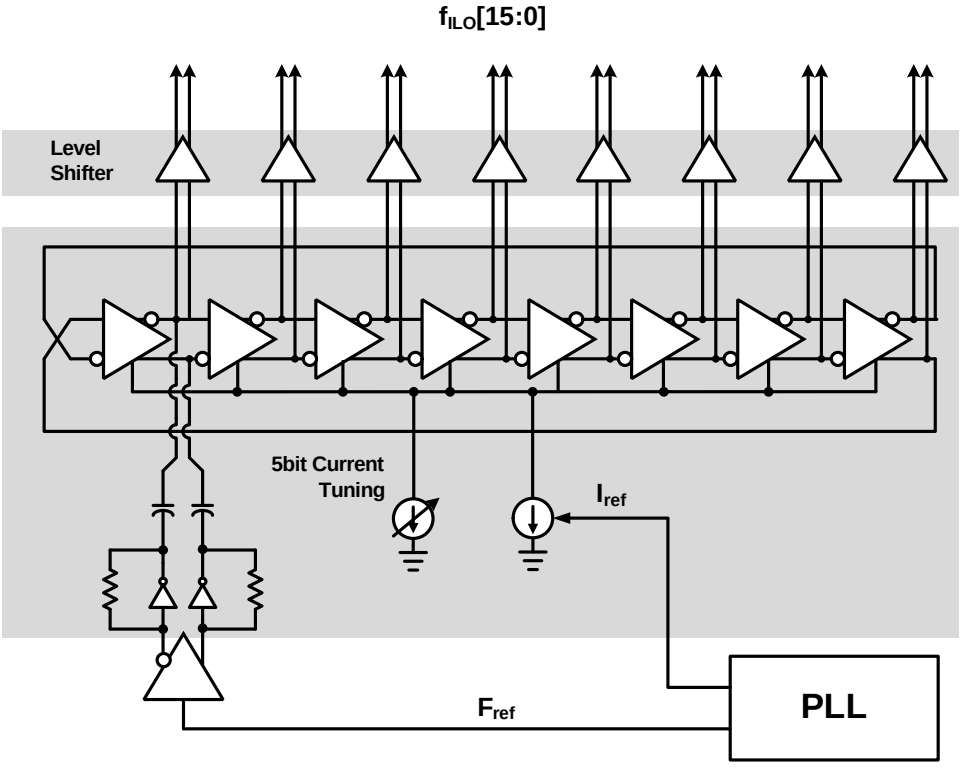

Figure 4.11: Schematic of injection locked oscillator (ILO).

contents 8 ILOs in TDC channels and a on-chip PLL. In PLL, a voltage-to-current converter (VIC) is used to convert voltage control to current control. Output of VIC is 9-bit adaptive current where $I_{ref}[0]$ is bias of the RO in PLL, and I_{ref}[8:1] are the current replica of $I_{ref}[0]$, biasing the ROs in ILOs. Since the ROs share the same design in the PLL and ILOs and they all suffer the same PVT variation on chip, the oscillation frequency will be the identical with the same current bias. Thus, the overall PVT variation can be sensed in PLL and calibrated through adjusting I_{ref}[9:0]. To calibrate minor mismatch, a 5-bit fine current tuning is applied in each ILO.

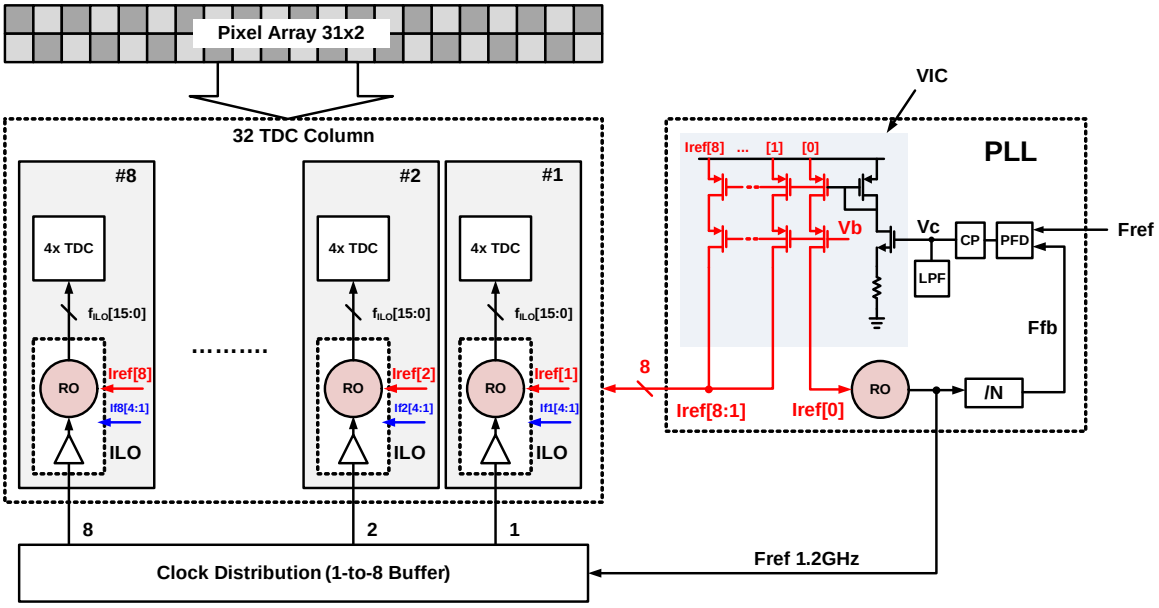

Figure 4.12: PVT-calibration in ILO clock distribution.

5. EXPERIMENTAL RESULTS

5.1 Sensor SoC

A chip photomicrograph of the LIDAR sensor prototype is depicted in Fig. 5.1. The chip size consumes 1.43×1.6 mm^2 area. The chip floor plan was mostly defined by the TDC columns and CTDC/FTDC clock distribution circuitry. An 1.2-GHz on-chip PLL is to generate a well-controlled reference frequency for whole SoC and also provide adaptive ILO biasing to calibrate PVT variation. The 31x2 pixel channel array is located at the center of the chip that is the input of the sensor. Also, a testing circuitry was embedded in sensor array to characterize TDC performance. The area of each pixel channel is 25×30 μm^2. Sensor operation is dominated by a digital synthesis circuit timing control (TCON). It controls the operation of TDC conversion and data readout sequence. The sensor chip was thoroughly tested and confirmed to be fully functional at 1-V nominal voltage supply and normal operating frequency. The power breakdown table was shown in Table 5.1. The whole chip consumes 39mW, and the power per TDC channel is 788μW, including CTDC and FTDC.

Multi-chip-module (MCM) bonding will be applied to connect this prototype CMOS chip with an InP-based 4×2 APD sensor array photonic chip. The APD sensor array can be operated as the high-sensitive LIDAR receiver at 1550nm optical wavelength. To demonstrate range-finding operation, a pulse-based fiber laser is used as an optical transmitter at 1550nm. The laser repetition rate was 375kHz and the duration of light pulse was 5ns (FWHM) with 40W peak power. In order to

accurately determine ToF, the pulse trigger signal is synchronous with the sensor SoC.

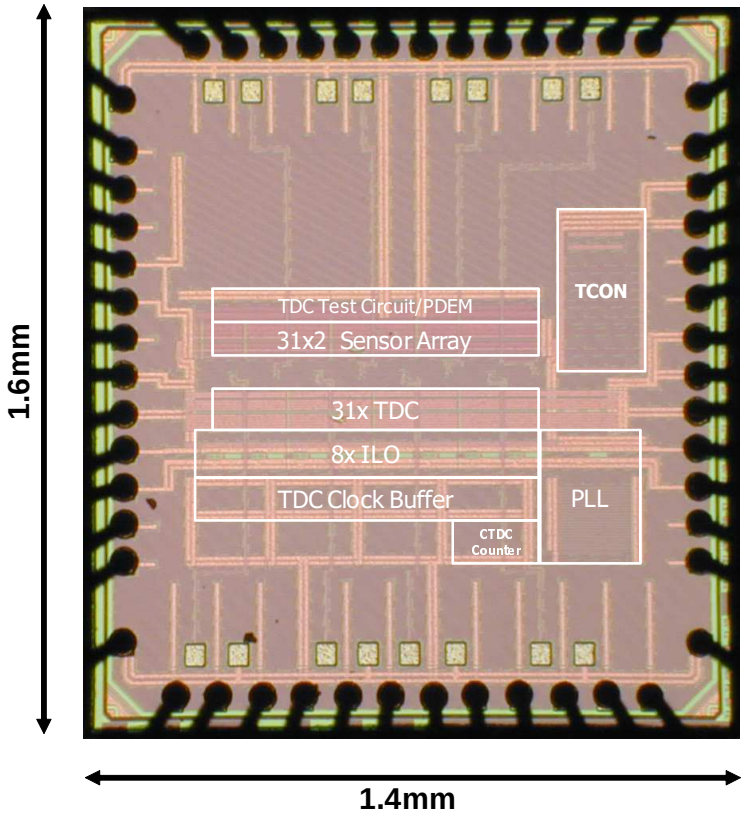

Figure 5.1: Photomicrograph of prototype LIDAR SoC in 65nm CMOS.

To characterize electrical performance of the TCSPC channels, an on-chip testing circuit is adopted. TDC-START and TDC-STOP signals are triggered externally. The STOP signal is distributed though an 1-to-8 clock tree buffer that provides universal time input for 31 TDC-STOP columns. The parallel 14-bit TDC output data was read out sequentially by columns and captured by FPGA. The scan chain signals are applied to the chip through a data-acquisition (DAQ) card, interfacing with

Table 5.1: Power breakdown of main SoC blocks operating at 52-ps time resolution

Circuit Block	Power	Units	Note
Front-end Receivers	**9.41**	**mW**	**31 Channels.**
PLL	**3.21**	**mW**	**1.2GHz PLL Frequency.**
TDC	**24.42**	**mW**	**1xTDC-START, 31xTDC-STOPs.**
8-ILOs	15.20	mW	
1-to-8 Clock Buffers	8.39	mW	CTDC0[9:0], CTDC1[9:0], Ref clock (f_{ref}).
CTDC global counter	0.83	mW	
Biasing, TCON, Digital I/O	**1**	**mW**	
Total Power	**38.04**	**mW**	
Power per TDC ch.	**788**	**μW**	

computer.

5.2 Single-Shot Precision (SSP)

Single-shot precision (SSP) represents the noise performance of TDC in time-domain, i.e. jitter. It is performed for time-resolved channel by taking several measurements of a time input over the DR of TDC. To characterize the actual SSP of TCSPC channel in LIDAR sensor, both the jitter contributed from front-end RX and TDC were considered. In the measurement, a 43μApp 5ns-pulsed photocurrent is emulated by an on-chip photodiode emulator (PDEM) that triggers front-end RX in each pixel channel. Fig. 5.2 shows the SSP measurement results for single TDC column. Three different time input (151ns, 502ns, and 703ns) are used in this work to verify SSP performance at difference input range. As seen from Fig. 5.2, the worst standard deviation of histograms among the three time input is 35.97ps at 703ns input that is smaller than one-LSB (52ps).

Fig. 5.3 shows the SSP across 31-TDC columns. The rms accuracy is distributed from around 31ps at 151-ps time input to around 36ps at 703ps time input. Although

the rms value gets slightly higher as input time increases, the performance can still satisfied with in one-LSB requirement. The demonstration of SSP results shows the great time jitter performance on localized ILO as well as the FTDC multi-phases.

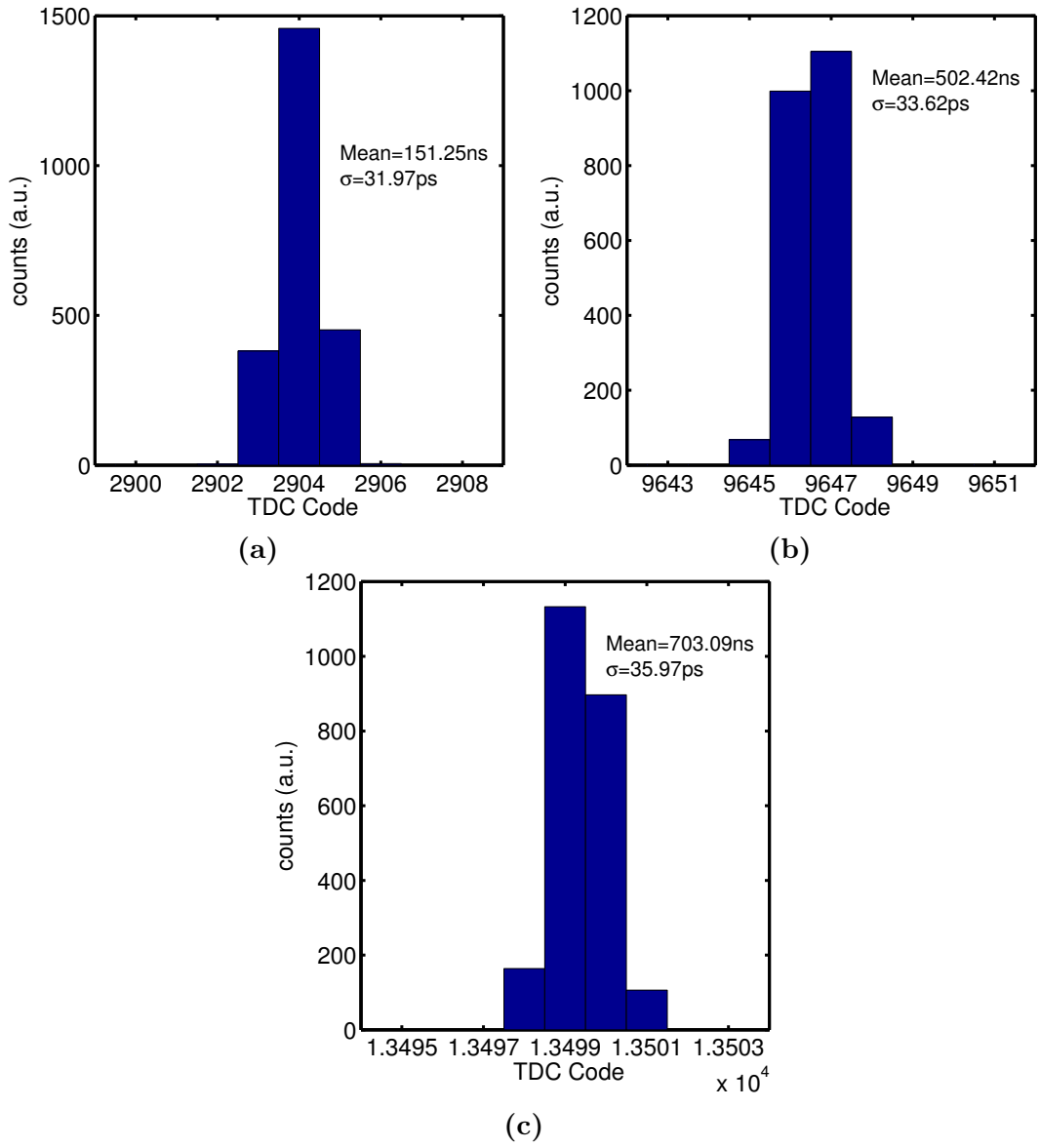

Figure 5.2: Single-shot precision of TCSPC channel (front-end RX and TDC) with time input: (a) 151ns, (b) 502ns, and (c) 703ns, corresponding to rms precision of 31.97ps, 33.62ps, and 35.97ps, respectively.

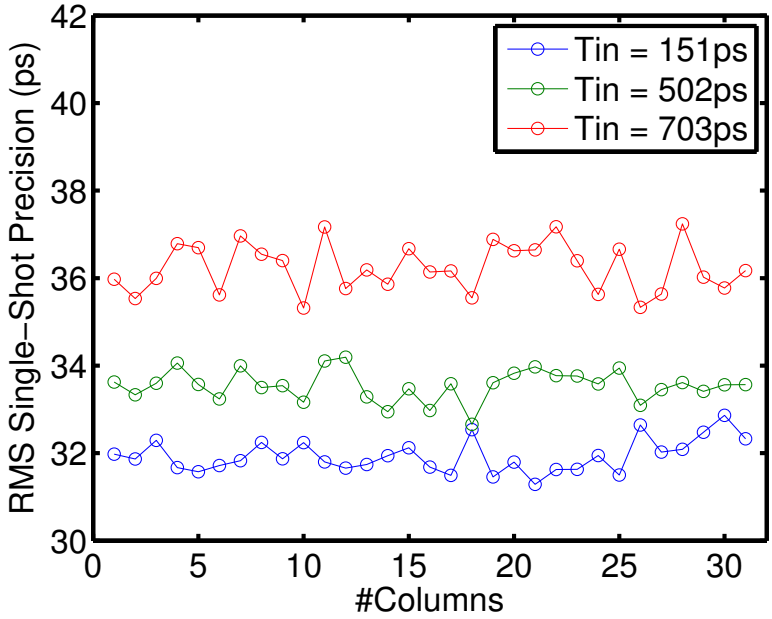

Figure 5.3: RMS single-shot precision of 31 TCSPC channels (front-end RX and TDC) with time input at 151ns, 502ns, and 703ns.

5.3 Channel Uniformity

TDC channel uniformity is measured by buffering a global STOP signal through a 1-to-8 clock tree buffer into 31 TDC channels. To minimize the jitter effect, TDC output value is obtain by averaging 2000 measurements of an time input. Fig. 5.4 depicts the channel uniformity of 31 TDC channel with time input at 151ns, 502ns, and 703ns. At three difference input range, the rms accuracy are smaller than 7.5ps (0.15-LSB). The uniformity is significantly better than conventional pixel-counting TDC, although the FTDC reference phases are generated from the local ILOs. The rms accuracy gets slightly higher by 3ps as we considered the front-end RX in the channel (Fig. 5.5). It is because the single-ended RX architecture is more vulnerable to the process variation that induces determined cell delay mismatch among the channels. However, the rms accuracy is less than one-LSB and would not impact the

14-bit time resolution.

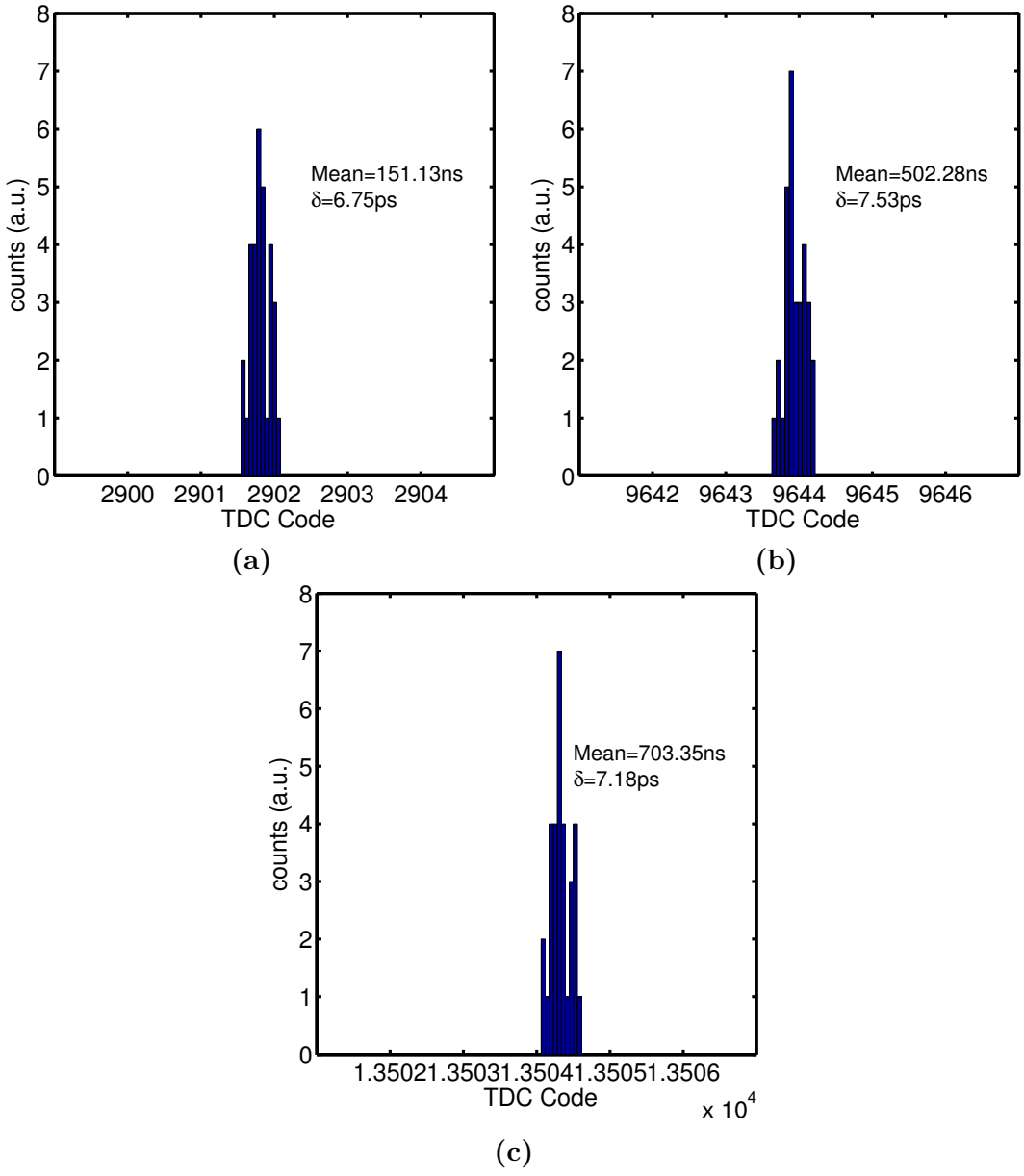

Figure 5.4: TDC channel uniformity with time input: (a) 151ns, (b) 502ns, and (c) 703ns, corresponding to rms precision of 6.75ps, 7.53ps, and 7.18ps, respectively.

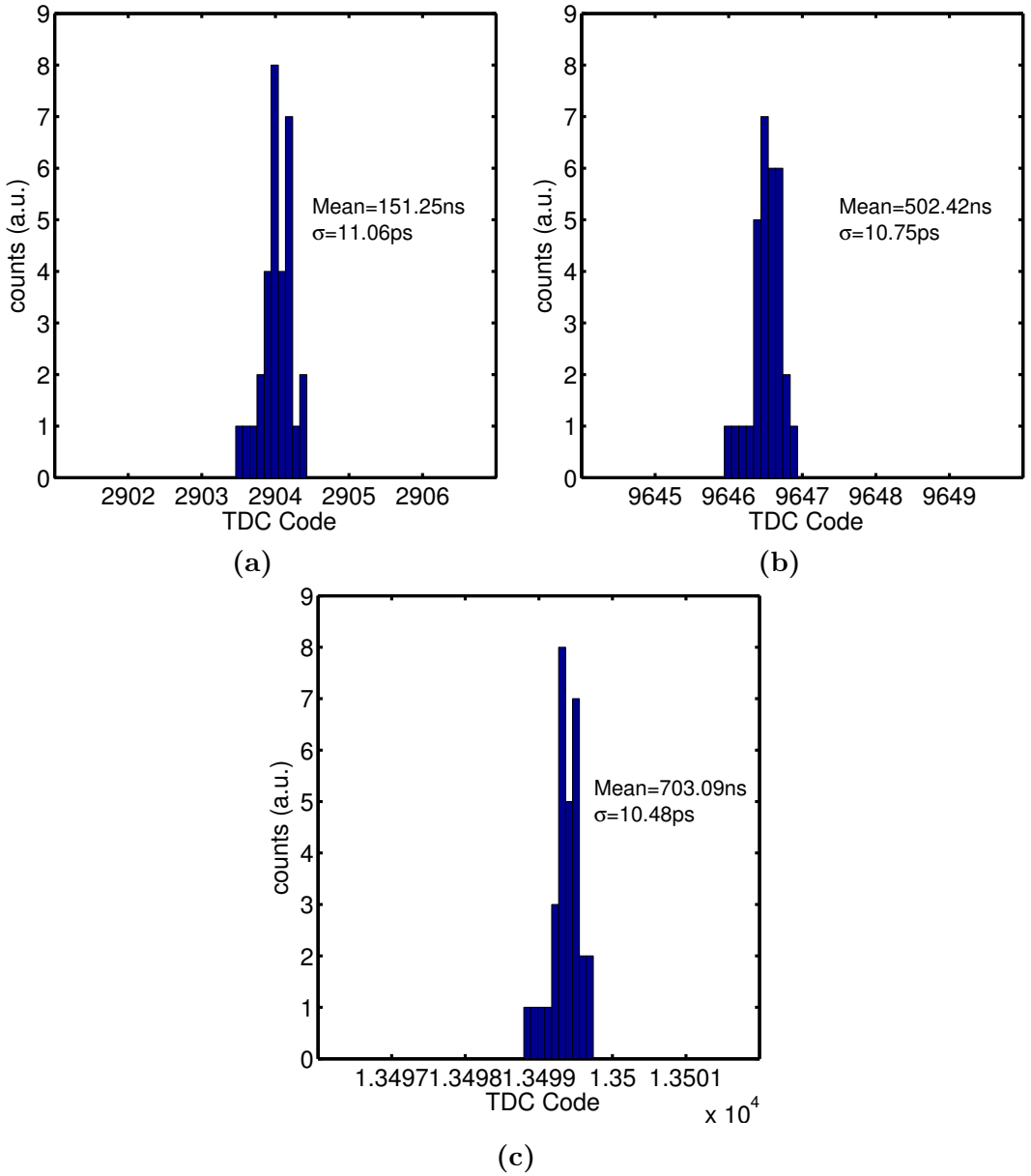

Figure 5.5: TCSPC channel uniformity with time input: (a) 151ns, (b) 502ns, and (c) 703ns, corresponding to rms precision of 11.06ps, 10.75ps, and 10.48ps, respectively.

5.4 Linearity

Linearity of TDC has been characterized in terms of differential non-linearity (DNL) and integral non-linearity (INL). Histogram approach is adopted to eliminate any jitter and noise effect in the testing. During the test, two clock domains, 375kHz and (375kHz-10Hz), are applied to the TDC, generating a time ramp input with a ramp step of 71.1ps. The corresponding histogram of the resolved digital codes is used to calculate the DNL and INL errors. Fig. 5.6 shows the measured DNL of 0.56 LSB and INL of 1.56 LSB, throughout a range of 830 ns. It results in 124 m maximum detection range in distance. The measured results claims for no missing code in the digital conversion.

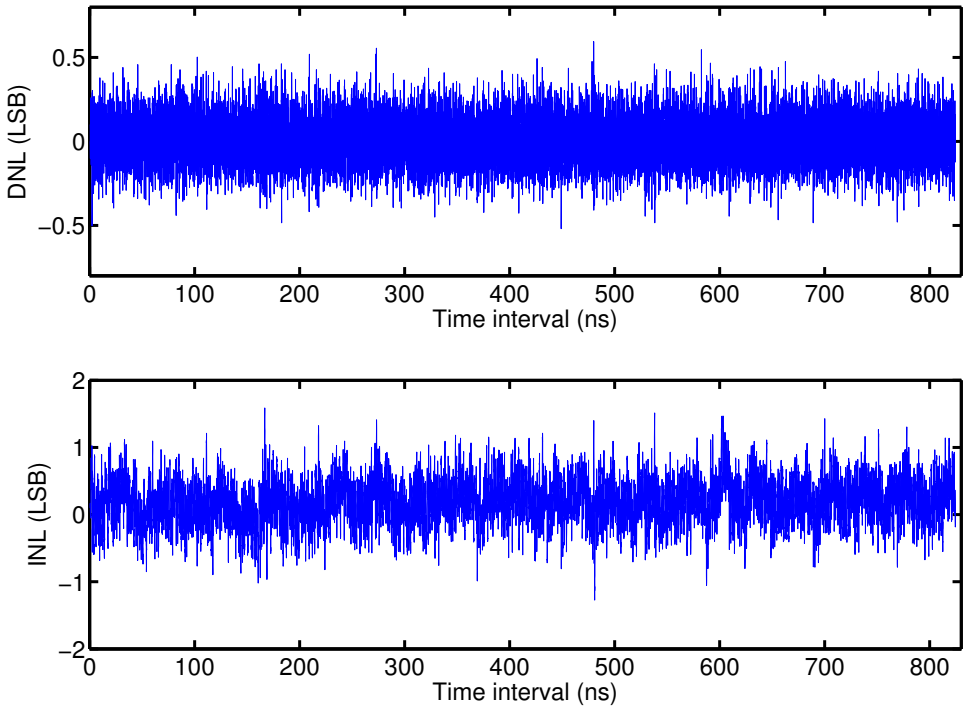

Figure 5.6: Measured DNL and INL of TDC over dynamic range.

Table 5.2 summarizes the performance of the proposed SoC and compares this work against recent state-of-the-art works. Evidently, the proposed SoC achieves high time resolution and large dynamic range. Also, a good channel uniformity (0.21-LSB) and single-shot precision (0.72-LSB) is performed by ILO clock distribution. Meanwhile, to the best of author's knowledge, the proposed design achieves the lowest power consumption in global-based counting architecture.

Table 5.2: Comparison table of recently published state-of-the-art devices

	Parameters	Unit	[6]	[37]	[7]	[8]	This Work
Sensor	**Process**	**-**	180nm	350nm	350nm	130nm	65nm
	Array Size	**pix.**	1x16	128x128	32x32	32x32	31x2
	Pixel Size	**μm^2**	30x10 (Macro-Pixel)	25x25	30x30	50x50 (SPAD+TDC)	35x35
	Pixel Type	**-**	SPAD	SPAD	SPAD	SPAD	APD
TDC	**Architecture**	**-**	Global-Counting Column-TDC	Mixed-Counting Column-TDC	Global-Counting Pixel-TDC	Pixel-Counting GRO-TDC	Global-Counting ILO-TDC
	Channel Size	**-**	16x4	32x1	32x32	32x32	31x1
	Resolution (LSB)	**ps**	208	97.66	312	52	52
	No. of Bits	**bit**	12	10	10	10	14
	Measurement Range	**ns**	852	100	319	53	830
	Nonlinearity (DNL/INL)	**ps**	35/116	7.8/185	6.4/ 31.9	20.8/ 72.8	29.1/81.1
	Uniformity (1σ)	**ps**	NA	NA	42	416	14
	Single-Shot Precision (1σ)	**ps**	NA	NA	254	31.2	38.5
	Power per Channel	**uW**	NA	NA	2400[1]	38	788
System	**Illumination Wavelength**	**nm**	870	635	750	NA	1550
	Illumination Repetition Rate	**MHz**	0.133	40	NA	NA	0.375
	Illumination Power (Average)	**mW**	21	250	90	NA	40
	Ranging Resolution	**cm**	3.12	1.46	4.68	NA	0.78[2]
	Unambiguous Distance Range	**m**	128	15	48	NA	124[2]
	Relative Precision[3]	**%**	0.14	0.13	0.18	NA	TBD

[1] Power measured at 50-gate per frame.

[2] Calculated from TDC specifications.

[3] Relative Precision = Single-shot precision (1σ)/ Measuring distance.

6. SUMMARY AND CONCLUSIONS

With the emerging need for high resolution LIDAR sensor in automotive and IoT application, we have introduced prototype LIDAR sensor SoC which supports a range precision of 0.78 cm and a distance range of 124 m. At the core of SoC, the front-end receivers are 31×2 pixel channel array. The time-of-flight (ToF) is resolved by 31×1 14-b 52-ps resolution time-correlated single-photon counting (TCSPC) channels. The CTDC is implemented with a 10-b global Gray code counter while the FTDC is implemented by eight localized injection-locked oscillators (ILOs). The sensor SoC has been fabricated and tested in a 65nm CMOS technology and has been confirmed to be fully functional. The proposed TCSPC channels perform single shoot precision (SSP) and channel uniformity less than 38ps and 11ps across entire DR, respectively.

New ILO-based clock distribution is proposed in this work to minimized the power consumption in global driving architecture. Comparing with conventional clock distribution technique, ILOs have the advantage in power, area, channel uniformity, and time precision. The simulated FTDC consumes 484μW that is 70% lower than the power of muli-stage clock driving. The injection locking technique preforms the phase synchronous among ILOs and preserve good channel uniformity. Also, the ILO perform 1st-order jitter filtering, improving the time precision.

Future work may involve the demonstration of LIDAR system. A high power 1550nm pulse laser will be used as the transmitter in system. Receiver is the proposed SoC integrated with a APD photonic chip. Multi-chip-module (MCM) process is applied to attach a 4×2 APD photonic chip on top of proposed SoC, and connected through chip-to-chip bonding. A complete test of LIDAR operation will be conducted

to evaluate the performance of range finding.

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