2.4 GHZ PHASE LOCKED LOOP WITH DLL BASED SPUR SUPPRESSION TECHNIQUE IN 40NM CMOS

A Thesis

by

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ABSTRACT

Phase locked loops (PLLs) are widely used as frequency synthesizers in modern communication systems because of the frequency accuracy and programmability of output frequency.

Reference spur is an issue of concern in the PLL design as it merges the interference into the desired signal band. This study focuses on the design of PLLs with low reference spurs level. A PLL with 2.4 GHz output frequency is implemented in TSMC 40nm CMOS technology using a 1.1V supply. A delay locked loop (DLL) is inserted in the phase locked loop as a multiple phase generator, in order to move the fundamental spur to higher frequency. The influence of errors inside the DLL due to CMOS process on the performance of spur suppression is also analyzed in this work. Two independent calibration systems, continuous time calibration and switch capacitor integrator based calibration for DLL's errors are presented, to reduce the delay errors.

A spur reduction of 35 dB compared to a conventional structure is verified by the schematic simulation in Cadence.

DEDICATION

To my parents

ACKNOWLEDGEMENTS

I would like to thank my advisor, Dr. Jose Silva-Martinez, for his patient guidance and support on my research. And I would also like to thank my committee members, Dr. Entesari, Dr. Hu and Dr. Jo.

Also, thanks to my mother and father for their encouragement.

NOMENCLATURE

CP	Charge Pump
DLL	Delay Locked Loop
LO	Local Oscillation Signal
PLL	Phase Locked Loop
PFD	Phase and Frequency Detector
RF	Radio Frequency
TX/RX	Transmitter/Receiver
VCO	Voltage Control Oscillator
VC	Control Voltage

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1. INTRODUCTION

1.1 Introduction of PLL

Frequency synthesizers are important building blocks in today's wireless communication systems. Band and channel selection in the RF transceiver circuits requires accurate, programmable, low noise local oscillator (LO) signals. The quality of LO signal plays a critical role in overall performance of the communication systems, determining how closely channels can be placed to each other to achieve a given signal to noise ratio (SNR) or bit error rate (BER). In other words, high quality of LO signal improves the use efficiency of communication bandwidth.

Phase locked loop (PLL) is widely used as the structure of frequency synthesizers in modern communication systems. Frequency synthesis techniques mainly consist of the direct analog synthesis, the direct digital synthesis and the indirect synthesis (usually refers to PLL). The direct analog synthesis and the direct digital synthesis are both hardware intensive techniques to achieve fine frequency resolution and fast switching. However, both of these method are not suited for high frequency and low phase noise frequency systems. The PLL based indirect synthesis technique has the capability to generate high frequency with low phase noise [1]. Therefore, PLL based frequency synthesizers are used in most wireless application for local oscillator signal generation.

Programmability of the output frequency is also another important factor letting PLL popular, which enables RF system to be compatible to multiple communication standard. Specifically, PLL is able to output different value of frequency by simply

changing the ratio of the divider (a building block in PLL) which enables PLL to perform channel selecting as shown as Figure 1.

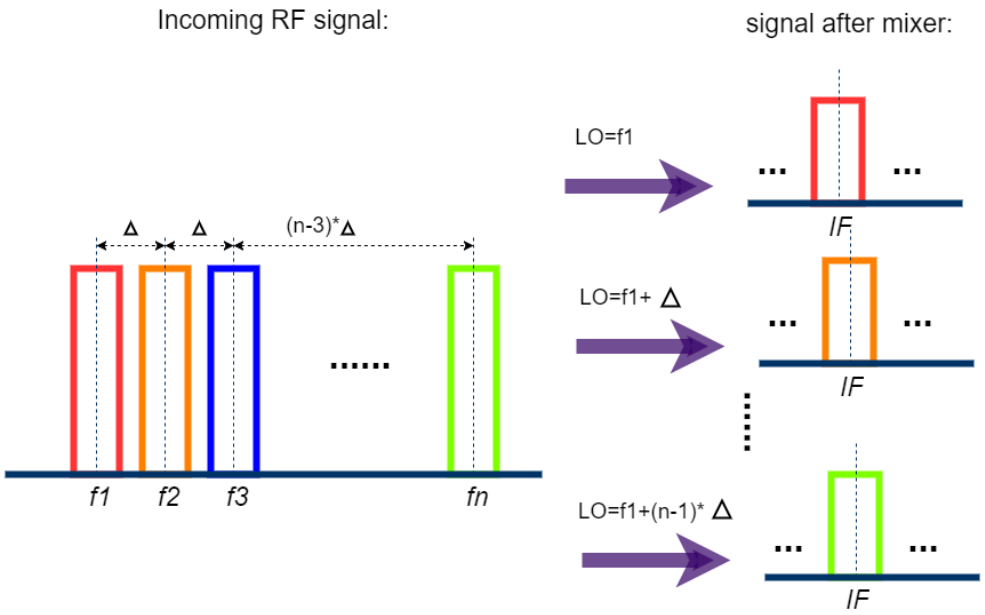

Figure 1 Channel Selecting Using Different LO Frequency

1.2 Application

Majority of PLL designs are used for frequency generation in RF and digital systems. As the functions of today's electronic systems become diverse, PLLs are also used in a wide range of application, such as Clock and Data recovery (CDR), phase-locked modulation and demodulation and compensation of timing skew in digital systems [2].

2. STRUCTURE

PLLs used for frequency synthesizers include 2 types of structure: integer N PLL and fractional N PLL. In an integer-N PLL, the divider ratio N is an integer, so the output frequencies have an interval of the reference frequency. In a fractional N structure, the divider ratio N can be a fractional number.

This project will focus on integer-N PLL since it is widely used in today's RF communication circuits. Figure 2 is block diagram of a simple type II PLL where type of PLL refers to the number of integrators within the loop.

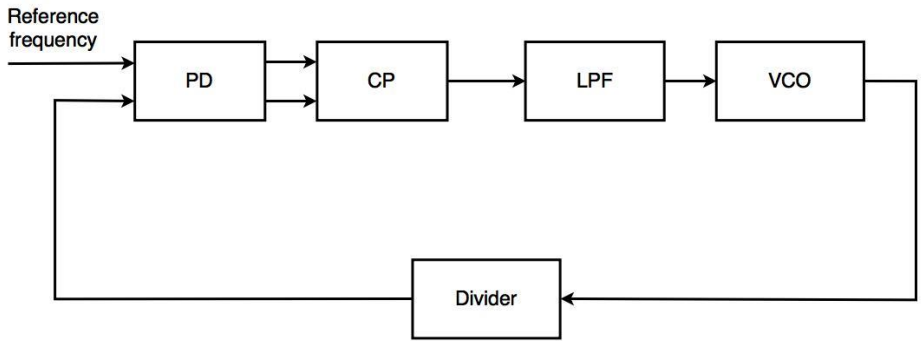

Figure 2 Structure of a Type II PLL

2.1 Phase Detector and Charge Pump

Phase detectors in common uses include analog mixer phase detector, XOR phase detector, JK flip-flop phase detector and tri-states phase and frequency detector (PFD). Tri-states PFD is used dominantly in type II PLL, shown in Figure 3.

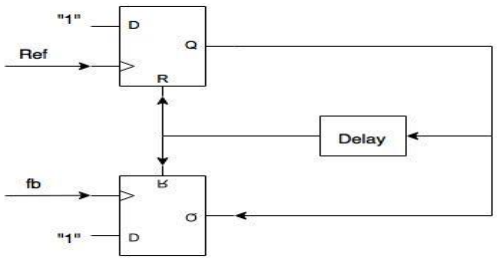

Figure 3 Tri-States Phase Detector

Charge pump in a PLL acts as an electronic switch that dispenses charge into the loop filter under control of the phase detector.

2.2 Oscillator

An oscillator with controllable frequency is another essential element of a phase-locked loop. There are voltage control oscillators (VCOs) and current control oscillators (ICOs). A good designed oscillator should have a series properties including low phase noise, wide tuning range, fast modulation capability, low power consumption and capability to integration on a chip. In CMOS circuit design, oscillator with LC resonant tank and ring oscillator is the two dominate types of oscillator in PLLs. LC – tank is advanced in low phase noise while ring oscillator has the advantage in low power dissipation and small size.

2.3 Divider

Frequency divider convert a high-frequency signal to a low-frequency signal, by a factor of N which is usually programmable. Digital counters based divider is more

versatile and widely used. Analog divider including injection locked divider and Miller divider are capable to operate at higher frequencies than digital counter, but realizing the programmability of the dividing ratio of an analog divider is difficult.

3. MODEL

3.1 Linear Approximation

PLLs are inherently nonlinear circuits, though, its operation in phase domain can be approximated well by linear models. A linear model will be applicable if phase error is small, a condition normally attain when the loop is locked. Most analysis and design of PLLs can be based on the linear approximations.

Most of the PLLs are simply approximated using a second order model with non-dominant poles in higher frequencies. A second order type II PLL has the open loop transfer function as equation (1), where I_{CP} and K_{VCO} refers the current value of charge pump and the gain of VCO, respectively. And N is the dividing ratio of the frequency divider.

$$G(s) = \frac{\frac{I_{CP}}{2\pi N} K_{VCO} R \left(s + \frac{1}{RC}\right)}{s^2} \quad \textbf{(1)}$$

A second order type II PLL has the transfer function and error transfer function as equation (2) and equation (3), respectively.

$$H(s) = \frac{\frac{I_{CP}}{2\pi} K_{VCO} R \left(s + \frac{1}{RC}\right)}{s^2 + \frac{I_{CP} K_{VCO} R}{2\pi N} s + \frac{I_{CP} K_{VCO}}{2\pi NC}} \quad \textbf{(2)}$$

$$E(s) = \frac{s^2}{s^2 + \frac{I_{CP} K_{VCO} R}{2\pi N} s + \frac{I_{CP} K_{VCO}}{2\pi NC}} \quad \textbf{(3)}$$

A best known set of parameters for a second order consists of the natural frequency ω_n and damping factor ζ. These two parameters determine the settling behavior of a

second order system. In a second order type II PLL, nature frequency ω_n and damping factor ζ are given by equation (4) (5), respectively.

$$\omega_n = \sqrt{\frac{I_{cp}K_{vco}}{2\pi NC}} \tag{4}$$

$$\zeta = \frac{\omega_n}{2} R_1 C \tag{5}$$

The normalized transfer function and error transfer function plot with different ζ value is in Figure 4, where the loop gain $K = 2\zeta\omega_n$.

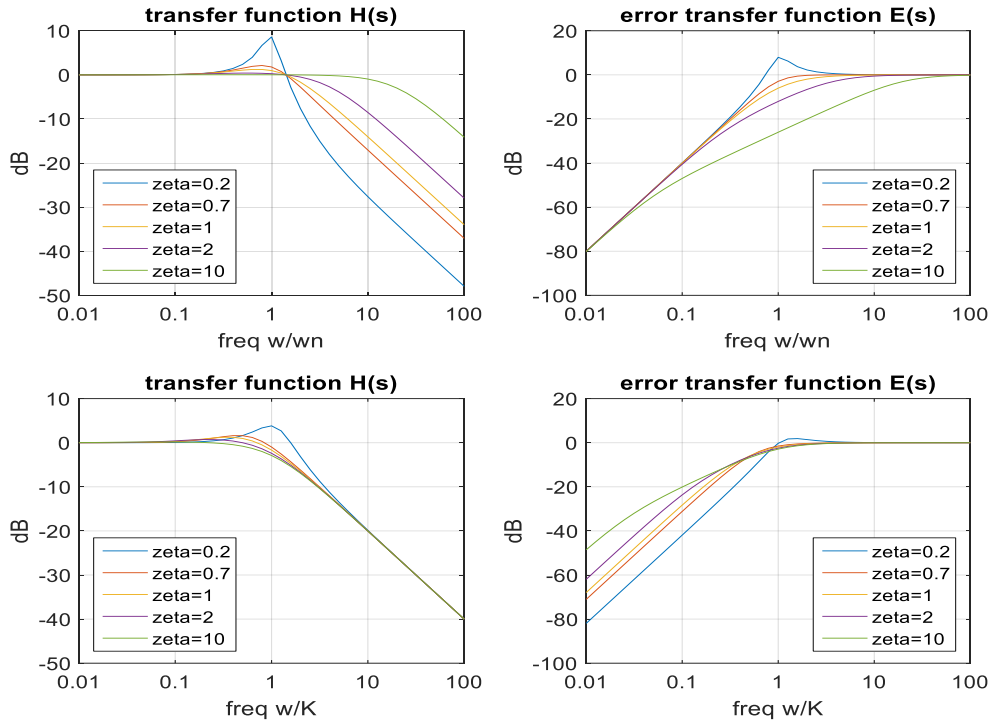

Figure 4 Nomalized Transfer Funtion of PLL

The unity gain frequency of the open loop transfer function is shown by equation (6) which is useful when determining the phase margin of PLL.

$$\omega_u^2 = \left(2\zeta^2 + \sqrt{4\zeta^4 + 1}\right)\omega_n^2 \quad \textbf{(6)}$$

3.2 Specs

3.2.1 Settling

Transient error response to a phase step with different cases of the value of ζ is given by Table 1 [2].

Table 1 Transient Error Response to Phase Step.

Phase step Δθ	
ζ	Transient phase error $\theta_e(t)$
$\zeta < 1$	$\Delta\theta\left(cos\sqrt{1-\zeta^2}\omega_n t - \frac{\zeta}{\sqrt{1-\zeta^2}} sin\sqrt{1-\zeta^2}\omega_n t\right) e^{-\zeta\omega_n t}$
$\zeta = 1$	$\Delta\theta(1-\omega_n t)e^{-\omega_n t}$
$\zeta > 1$	$\Delta\theta\left(cosh\sqrt{\zeta^2-1}\omega_n t - \frac{\zeta}{\sqrt{\zeta^2-1}} sinh\sqrt{\zeta^2-1}\omega_n t\right) e^{-\zeta\omega_n t}$

Transient error response to a frequency step with different cases of the value of ζ is given by Table 2.

Table 2 Transient Error Response to Frequency Step

Frequency step $\Delta\omega$	
ζ	Transient phase error $\theta_e(t)$
$\zeta < 1$	$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{1-\zeta^2}} sin\sqrt{1-\zeta^2}\omega_n t\right) e^{-\zeta\omega_n t}$
$\zeta = 1$	$\frac{\Delta\omega}{\omega_n}(\omega_n t) e^{-\omega_n t}$
$\zeta > 1$	$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{\zeta^2-1}} sinh\sqrt{\zeta^2-1}\omega_n t\right) e^{-\zeta\omega_n t}$

Transient error response to a frequency ramp with different cases of the value of ζ is given by Table 3.

Table 3 Transient Error Response to Frequency Ramp

Frequency step Λ	
ζ	Transient phase error $\theta_e(t)$
$\zeta < 1$	$\frac{\Lambda}{\omega_n^2} - \frac{\Lambda}{\omega_n^2}\left(cos\sqrt{1-\zeta^2}\omega_n t + \frac{\zeta}{\sqrt{1-\zeta^2}} sin\sqrt{1-\zeta^2}\omega_n t\right) e^{-\zeta\omega_n t}$
$\zeta = 1$	$\frac{\Lambda}{\omega_n^2} - \frac{\Lambda}{\omega_n^2}(1+\omega_n t) e^{-\omega_n t}$
$\zeta > 1$	$\frac{\Lambda}{\omega_n^2} - \frac{\Lambda}{\omega_n^2}\left(cosh\sqrt{\zeta^2-1}\omega_n t + \frac{\zeta}{\sqrt{\zeta^2-1}} sinh\sqrt{\zeta^2-1}\omega_n t\right) e^{-\zeta\omega_n t}$

Among the all cases of input error, the settling speed is determine by the loop gain K which is given by equation (7).

$$K = 2\zeta\omega_n = \frac{I_{CP}K_{VCO}R}{2\pi N} \quad \textbf{(7)}$$

Among the all cases of input error, the settling speed is determine by the loop gain K which is given by equation (8). Under the condition of $\zeta > 1$, $K \cong \omega_u$. So we can say the unity gain frequency of the open loop decides the settling speed.

3.2.2 3-dB Bandwidth

3-dB Bandwidth of a second order type II PLL could also be specified by equation (8).

$$\omega_{3dB} = K\left(\frac{1}{2} + \frac{1}{4\zeta^2} + \frac{1}{2}\sqrt{1 + \frac{1}{\zeta^2} + \frac{1}{2\zeta^4}}\right) \quad \textbf{(8)}$$

3.2.3 Stability

Stability of an ideal second order type II PLL is ensured unconditionally. For an ideal second order type II PLL, the phase margin (PM) is given by equation (9).

$$PM = tan^{-1}\left(2\zeta\sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}\right) \quad \textbf{(9)}$$

But, in fact a PLL is inevitably a third order system at least since there is a parasite capacitor in the output node of the charge pump, denoted by C_1 here. In that case, a pole is introduced in the open loop transfer function, given by equation (10).

$$pole = \frac{C + C_1}{RC_1C} \quad \textbf{(10)}$$

This additional pole degrades the stability of PLL. In the most cases of practical designs, $32\zeta \gg 1$ and the phase margin is given by equation (11) under this condition. If the C_1 is large compared to C, the phase margin approximates zero degrees.

$$PM = tan^{-1}(4\zeta^2) - tan^{-1}(\frac{4\zeta^2 C_1}{C + C_1}) \quad \textbf{(11)}$$

3.2.4 Noise Filtering

There are multiple noise sources in a PLL system, while the most dominant two is the input noise from the reference source and the phase noise from the VCO. The PLL loop can filter out a part of these two kinds of noise.

For the noise from the input reference source, the noise transfer function is given by equation (12), which has low pass property.

$$H_{nIN}(s) = \frac{2\zeta\omega_n\left(s + \frac{\omega_n}{2\zeta}\right)}{s^2 + 2\zeta\omega_n + \omega_n^2} \quad \textbf{(12)}$$

For the noise from the VCO, the noise transfer function is given by equation (13), which has high pass property.

$$H_{nVCO}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textbf{(13)}$$

3.3 Design Tradeoffs

3.3.1 Bandwidth, Noise and Stability

There are multiple definition of the bandwidth of PLLs, but they are close to each other in a log scale. Here, for convenience, the bandwidth BW refers the unity gain frequency ω_u of the open loop transfer function.

To boost the settling speed, the loop bandwidth should be set as large as possible. The loop is low-pass for the input noise from source while it is high-pass for phase noise generated by VCO. To optimize the noise performance, the loop bandwidth should be chosen at the intersection point of the input noise spectrum and the VCO phase noise spectrum. In PLLs in CMOS technology using in RF communication, this intersection point is relative high. Thus, the bandwidth of PLL is set to as high as possible to filter out more VCO noise and to get fast settling property.

However, the bandwidth of PLLs used as frequency synthesizer in RF transceiver cannot arbitrary high. Frequencies resolution refers to the smallest frequencies interval of the output of a PLL in different mode which is equal to the reference frequency f_{ref}. For a PLL used in frequency synthesizer in RF communication, frequencies resolution is equal to or even less than the interval of adjacent channels, which is thus specified by the communication standard applied. $f_{ref} \gg BW$ is the pre-requisite of the linear approximation. This condition should attain in PLLs' design, otherwise the linear model fails to describe the system's behavior and the actual behavior of the system may be unstable.

In actual design, to suppress noise on the control voltage node of the PLL and the periodic disturbances also known as frequency spurs, higher order loop filter is desirable. But high frequencies poles are potential to degrade the stability of the system. To achieve a robust stability, the bandwidth is also restricted.

4. NOISE

4.1 Effects of Phase Noise

Phase noise is one of the most important specs of PLL. A low phase noise means high spectral purity which is essential for applications like mixer. For instance, when using the output of PLL as LO clock for mixer, the converted IF signals will be polluted by the phase noise of LO clock, resulting in a low SNR system as shown in Figure 5. In the case of transmitting, the output signal up-converted by noisy LO clock will also degrade other adjacent signals.

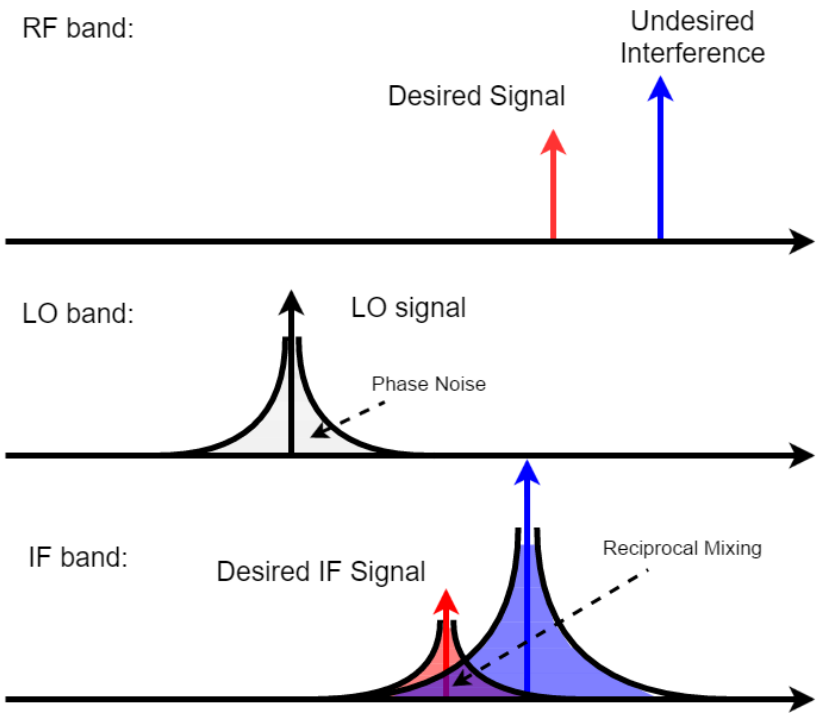

Figure 5 Effect of Phase Noise in a PLL

4.2 Linear Model

The source of phase noise inside PLL can be everywhere. All blocks including PFD, CP, filter, VCO and divider generate their own noise. However, these noise sources can have different transfer function to the output. The noise from PFD/CP and divider can actually be equivalent to input noise, thus sharing the same transfer function as input reference phase. Phase noise from VCO, on the other hand, have a high-pass transfer function which will be shown in the following analysis.

The linear model for phase noise analysis is shown in Figure 6. The phase noise from each block can be model by adding noise at the output of that block. Obviously, the noise from divider can be equivalent to input noise, while the noise from PFD/CP can also be referred back to input by dividing certain gain. Phase noise from VCO as shown is actually directly added to the output. Thus it has the entire low pass loop gain at its feedback path, which makes its transfer function high-pass. For convenience, all transfer functions have been translated to standard 2nd order system type.

$$\frac{\phi_{out}}{\phi_{in}} = \frac{N2\zeta\omega_n(s + \frac{\omega_n}{2\zeta})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textbf{(14)}$$

$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \textbf{(15)}$$

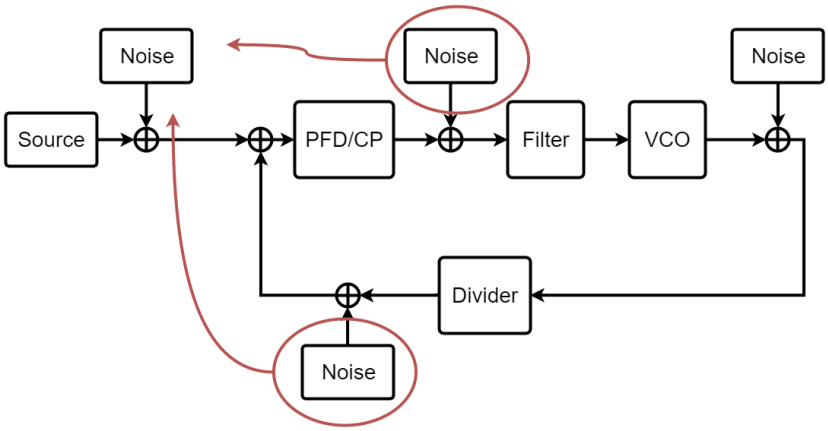

Figure 6 Noise Sources in a PLL

Since the PLL shapes its input noise by low-pass filter, while VCO noise by high-pass filter. A kind of trade-off for noise exists when designing bandwidth. For input noise, one of the interesting things to notice is that a high divide ratio N will result in noise power at output increased by N^2.

For VCO noise, different theories all indicate that it has a $\frac{1}{\omega^3}$ part contributed by flicker noise and a $\frac{1}{\omega^2}$ part contributed white noise. Thus, their influence can be studied separately [3], as shown as Figure 7. According the transfer function for $\frac{1}{\omega^3}$, when ω is sufficient small, the phase noise power rises linearly with frequency and reaches its maximum point at $\frac{\omega_n}{\sqrt{3}}$ which is 12dB less than a free running VCO. Beyond corner frequency, the white noise begins to dominate. Its analysis shows that it reaches maximum point at ω_n, suggesting a 6 dB reduction compared to a free running VCO. The overall noise is the combination of these two results.

$$\phi_{out}^2 = \frac{\omega^4}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega^2}\left(\frac{\alpha}{\omega^3} + \frac{\beta}{\omega^2}\right) \quad \textbf{(16)}$$

$$\phi_{out,flicker}^2 \sim \frac{\alpha\omega}{\omega_n^4} \quad \textbf{(17)}$$

$$\phi_{out,white}^2 = \frac{\beta\omega^2}{(\omega^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega^2} \quad \textbf{(18)}$$

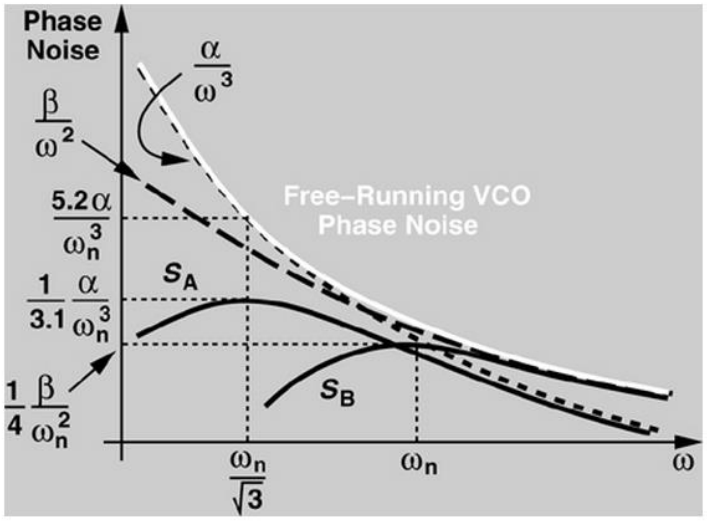

Figure 7 VCO Noise Sharping in the PLL (Reprinted from [3])

4.3 Jitter Model

An interesting topic about noise analysis of PLL is its modeling for simulation. Simulating a PLL in transistor level with transient noise is a super time-consuming task. To solve this problem, Ken Kundert [4] introduced a hands-on modeling technique on Cadence. Before using this technique, another important concept for noise should be presented. Jitter is basically the same thing as phase noise on spectrum. It is a form of

phase noise in time domain. Different kinds of jitter can be defined for different applications, while here in PLL two kinds of them are utterly important.

The first type of jitter is synchronous jitter. This jitter can be used to model phase noise of driven circuit. It is an undesired fluctuation in the delay between the input and output events. This jitter appears as a modulation of phase of the output, which is why it is sometimes referred to as phase modulated or PM jitter. The simplest metric is edge-to-edge jitter, J_{ee}. This definition can be used to model jitter of divider and PFD/CP since they are all driven blocks.

$$v_n(t) = v(t + j_{sync}(t)) \quad \textbf{(19)}$$

$$J_{ee}(i) = \sqrt{var(j_{sync}(t_i))} \quad \textbf{(20)}$$

Another type of jitter is accumulating jitter. Unlike synchronous jitter, accumulating jitter happens in autonomous system, like VCO. It is undesired variation in the time since the previous output transition, thus uncertainty of when a transition occurs accumulates with every transition. The accumulating jitter can be modeled by using period jitter J_{cc} which is the standard deviation of variation in one period [4].

$$J = \sqrt{var(j_{acc}(t + T) - j_{acc}(t))} \quad \textbf{(21)}$$

$$J_{cc} = \sqrt{2}J \quad \textbf{(22)}$$

In terms of extraction, different methods can be used for different blocks. In the divider, jitter happens during transition time when threshold crossing time varies. To extract the crossing time, PSS and strobed PNOSIE can be used. The spectrum density

$S_{n_v}(f, t_c)$ calculated can be integrated to get the total noise power $var\left(n_v(t_c)\right)$. Taking advantage of slew rate near crossing time, the RMS jitter of the divider can be calculated.

$$var\left(n_v(t_c)\right) = \int_0^{f_o/2} S_{n_v}(f, t_c)df \tag{23}$$

$$J_{ee,divider} = \frac{\sqrt{var\left(n_v(t_c)\right)}}{dv(t_c)/dt} \tag{24}$$

PFD/CP, on the other hand, generates jitter in a totally different way. Since this block injects noise all the time to loop filter, not only at transition time, the total output noise of PFD/CP should be calculated. Thus, in this case conventional PNOISE instead of strobed PNOISE should be used to compute the output noise over the total bandwidth. To equivalent this noise to PFD jitter, the output noise standard deviation should divided by the gain K of PFD/CP then times the period time T. The factor of square two is due to the total twice output transitions per period by PFD/CP.

$$var(n) = \int_0^{\infty} S_n(f)df \tag{25}$$

$$J_{ee_{PFD/CP}} = \frac{T}{K}\sqrt{\frac{var(n)}{2}} \tag{26}$$

The extraction of accumulating jitter of VCO can be a little bit complicated. According to [4], using PSS and PNOISE, the phase noise at an offset frequency can be get. Using the following equation (27) (28) [4], the RMS jitter J of VCO can be calculated.

$$c = \frac{L(\Delta f)\Delta f^2}{f^2} \tag{27}$$

$$J = \sqrt{cT} \tag{28}$$

Up until now, all jitters have been quantized by their RMS value. Since theoretically the random jitter is unbounded, to get the peak-to-peak value, certain bit-error-rate (BER) should be chosen first. A factor α corresponding to the specified bit-error-BER then can be used to calculate the peak-to-peak value of jitter according to equation (29).

$$J_{PP} = \alpha J_{RMS} \tag{29}$$

Figure 8 shows the resulted BER under different values of factor α.

Error Rate	α
10^{-3}	6.180
10^{-4}	7.438
10^{-5}	8.530
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996
10^{-10}	12.723
10^{-11}	13.412
10^{-12}	14.069

Figure 8 Error Rate vs. α (Reprinted from [4])

5. REFERENCE SPURS

5.1 Definition

Charge pump in a PLL acts as an electronic switch which converts the difference time durations of the two output of PFD to a current charge. In equilibrium, the amount of charge and discharge output by the charge pump are the same, keeping the control voltage of the PLL as a constant, as shown as Figure 9.

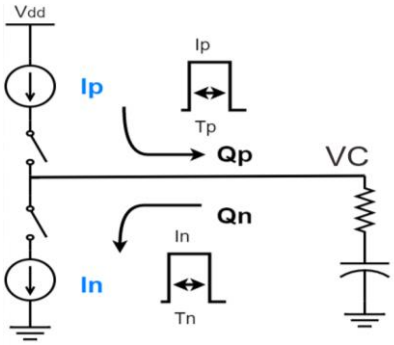

Figure 9 Operation of Charge Pump

Ideally, in static (locked) condition, the outputs of PFD arrive and turn on the charge pump simultaneously and generate two current pulses identical in shape with opposite polarities. Thus, the total charge is zero and the charge pump can be seen as open circuit by the control voltage node.

Unfortunately, because of non-idealities in circuit design, two current pulses generated by charge pump cannot be identical. As assumption, there is a height mismatch

between the two current pulses, and the charge from PMOS transistor is larger than the discharge to NMOS transistor, as shown as Figure 10. To keep the charge equilibrium, the PLL is finally is locked with a phase difference between input and feedback signals.

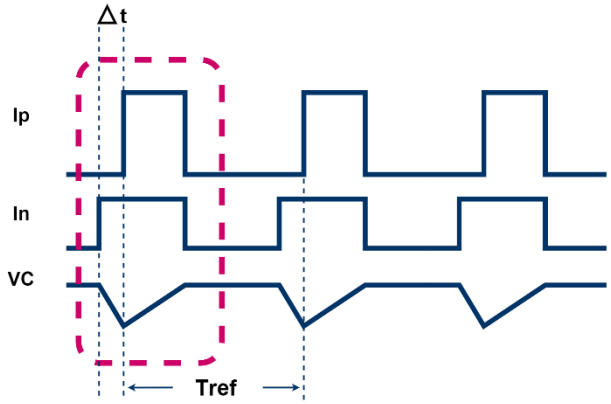

Figure 10 Charge Pump Mismatch and Ripples on VC

It turns to be periodic disturbances appearing on the control voltage node of the VCO in a frequency equal to the reference frequency.

These disturbances modulate the oscillation frequency in the oscillator, so there will be a large energy at one reference frequency offset from the center frequency in the output spectrum of the PLL, which is called as reference spur. Also, due to the nonlinearity of the voltage tuning in the oscillator, multiple spurs occur at the offset frequencies equal to harmonics of reference frequency as shown as Figure 11.

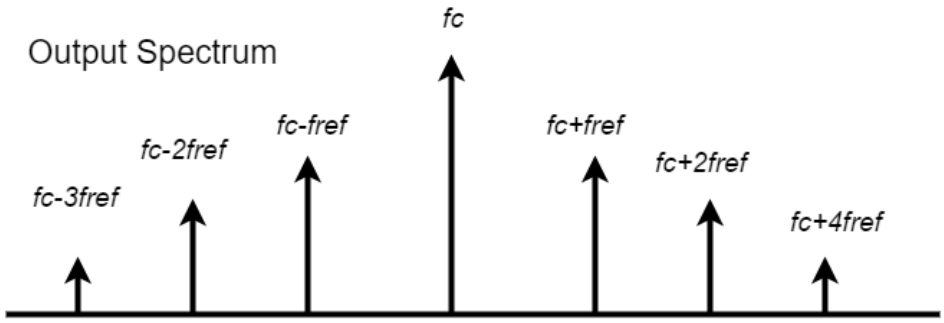

Figure 11 Output Spetrum with Reference Spurs

5.2 Effects of Reference Spurs

In PLLs used in frequency synthesizer in communication system, the reference frequency often equal to the frequency interval of the adjacent channel. These spurs are undesired as they move energy from interference probably from other channel in the same band to the IF band, corrupting the quality of communication. It can be exampled by the case shown in Figure 12. In received RF signals in a receiver, the power of interference is much higher than the desired signal, and there is a reference spur in the LO band. After mixed in the mixer, two signals overlap at the IF frequency, one is desired from the correct channel while another from the interference can be seen as noise. The SNR of the receiver is degraded and crosstalk occurs.

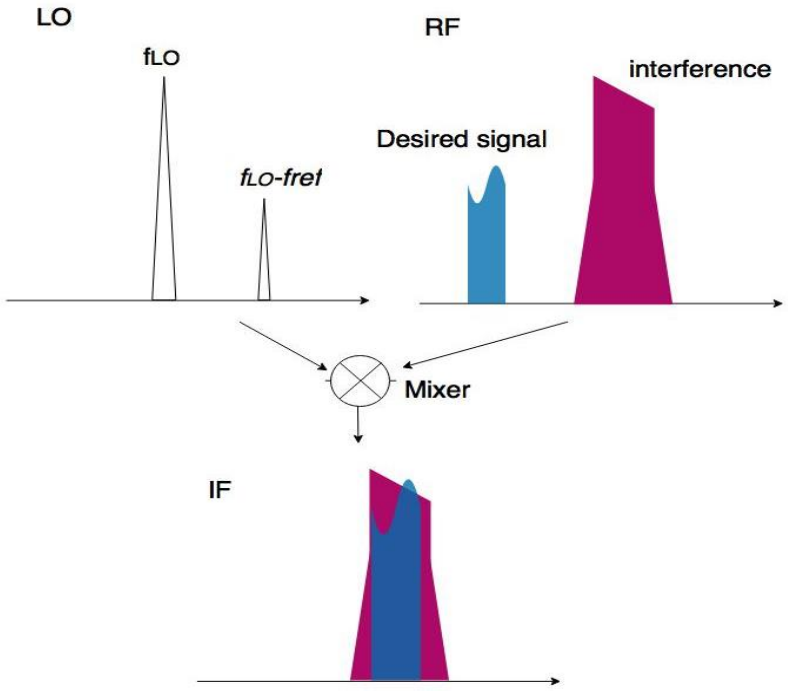

Figure 12 Effects of Reference Spur

5.3 Origins of Reference Spurs

There are several mechanism of the generation of reference spurs in PLLs. They are Up and Down Skew and Width Mismatch, charge injection and clock feedthrough in the charge pump, charge sharing and channel length modulation.

5.3.1 Up and Down Skew and Width Mismatch

Due to design difference between paths of UP and DOWN signals and random mismatches in CMOS process, the UP and DOWN signals experience different propagation delays to turn on the switches in the charge pump even though the inputs of PFD are perfectly in phase. As explained in Figure 13, a difference of arrival time of T1

translates to two current pulses of width T1 and opposite polarities that are injected by the charge pump at each phase comparison instant.

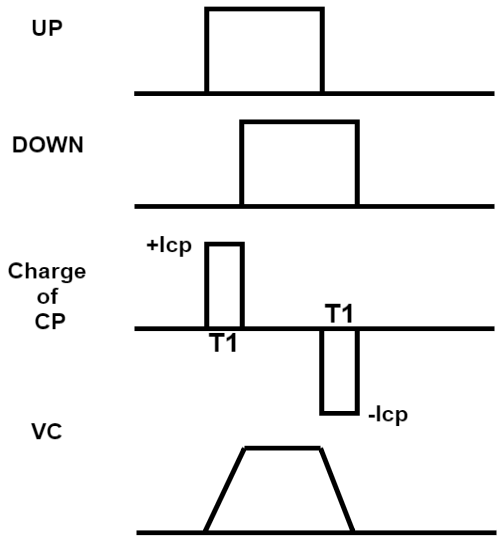

Figure 13 Waveform of UN and DN Skewing

Even though UP and DOWN signals arrive the charge pump at exactly the same, the currents produced by PMOS and NMOS sections of the charge pump may still suffer from skews.

5.3.2 Charge Injection and Clock Feedthrough

The switching transistors in the charge pump, carry a certain amount of mobile charge in their inversion layers when they are on. This charge amount is express as equation (30).

$$|Q_{ch}| = WLC_{ox}|V_{GS} - V_{TH}| \quad \textbf{(30)}$$

At the moment switches are turning on, the charge of carries is absorbed from the source and drain terminals, and the charge of carries is dispel to the source and drain terminals at the moment switches are turning off. Since the PMOS switch and NMOS switch generally have different design dimensions and overdrive voltage, the two current charges are unable to neutralize each other, thereby disturbing the control voltage of PLL.

Another effect from the switching transistors is the clock feedthrough which is relate to the gate-drain parasitic capacitance C_{GD}. The switches signals UP and DOWN couple through the $C_{GD,P}$ and $C_{GD,N}$, respectively.

Equation (31) and equation (32) give the voltage error created by clock feedthrough when the charge pump is on and when charge pump is off, respectively, where C_1 is the shunt capacitor in the loop filter.

$$\Delta V = \frac{C_{GD,P} - C_{GD,N}}{C_{GD,P} + C_{GD,N} + C_1} V_{DD} \quad \textbf{(31)}$$

$$\Delta V' = \frac{C_{GD,P} - C_{GD,N}}{C_{GD,P} + C_{GD,N} + C_2 + C_1} V_{DD} \quad \textbf{(32)}$$

5.3.3 Channel-Length Modulation

The up and down current in the charge pump also experience mismatch due to channel-length modulation of the current sources. Moreover, the change of output voltages leads to opposite changes in the drain-source voltages of the current sources, creating a larger mismatch. With short-channel devices, the current mismatches from channel-length modulation may reach 30% of the total charge pump current.

5.4 Techniques of Spur Suppression

5.4.1 Improved Charge Pump Design

Improved designs of charge pump have been proposed aiming to spurs due to different mechanism.

In order to alleviate the effect of charge injection and clock feedthrough, source switched topologies and adding dummy switches are adopted.

To reduce the channel length modulation, gain boosting structure is used to raise the output impedance. For the current mismatch of the up and down current sources, servo loop with an amplifier is used [5]. However, large extra power consumption is introduced by the amplifiers.

5.4.2 Spur Suppress PLLs

The first method to reduce the spur is using a "sample loop filter" [6] [7]. As explain in the previous part, the reference spurs comes from the instant disturbance when the charge pump operating. The concept in this method is that the disturbance on VCO's control voltage disappears if the control voltage node is isolated in the time period that the charge pump is operating. The circuit arrangement is shown in Figure 14. The switch turns off just before the charge pump begins to operate and turns on slightly after the disturbance on C1 is finished. As a result, C2 only sense the settled value at charge pump output and holds this value when the switch is off.

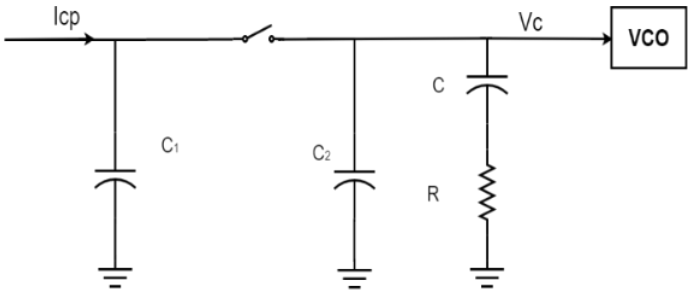

Figure 14 Sample Loop Filter

Other spur suppression techniques are also proposed, for example, Zolfaghari proposed a new structure with zero in VCO rather than in the loop filter like the conventional structure [8]. This is realizing by adding a variable delay stage in VCO. The benefit is that by avoiding the resistor in series with capacitor C, C is able to absorb the PFD/CP mismatches.

5.4.3 Spur Frequency Boosting

Another solution for the issue reference spurs is boosting it to higher frequency instead of eliminating it. Similar idea is used in works in [9] [10].

In [9], frequency boosting is realized by TVC and TVC based frequency booster shown in Figure 15. Another clock signal in higher frequency needs to be generate by extra blocks.

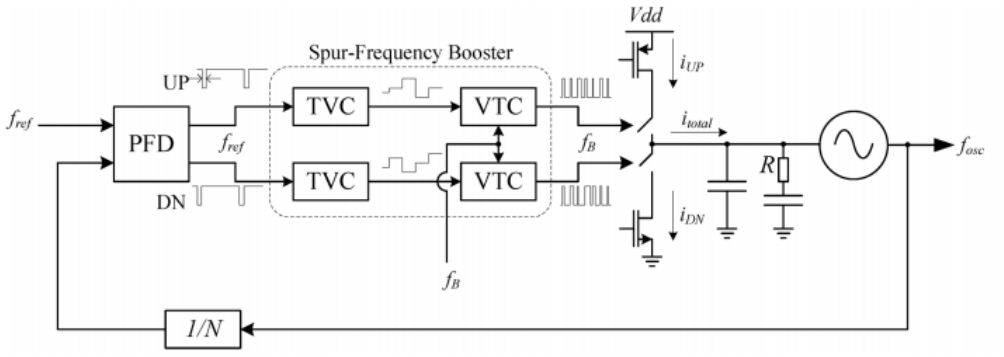

Figure 15 Frequency Boosting Realized by TVC (Reprinted from [9])

In [10], Choi proposed an architecture to refresh control voltage to the VCO eight times frequently by using a DLL based edge interpolator, shown in Figure 16.

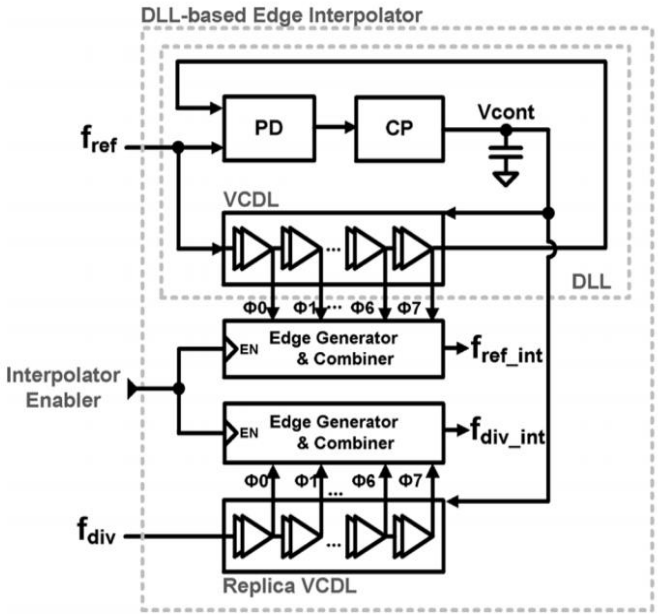

Figure 16 DLL-Based Edge Interpolator (Reprint from [10])

Table 4 shows test results of structures using different techniques of spur suppression.

Table 4 Comparison of Previous Techniques of Spur Suppression

	[9]	[10]	[11]	[12]
Output Frequency(GHz)	3.6	0.7-1.05	0.64	2.21
Reference Frequency (MHz)	6	13	40	55.25
Loop Bandwidth (kHz)	300	300	-	2712
Spur (dBc)	-74	-66	-68.5	-80
Spur Reduction (dB)	-	16	10	-
Technology	90nm	0.18µm	65nm	0.18µm

6. SYSTEM LEVEL DESIGN

6.1 Concept

As other works to boost the reference spur frequency, the charge pump in this system is designed to work in higher frequency than the regular reference frequency as usual. The disturbance on control voltage thereby appears multiple times every reference period, and then modulate the frequency of VCO, generating spurs located at higher offset frequencies.

Compare to other spur suppression techniques, spur frequency boosted PLL can reject multiple interferences, as shown as Figure 17.

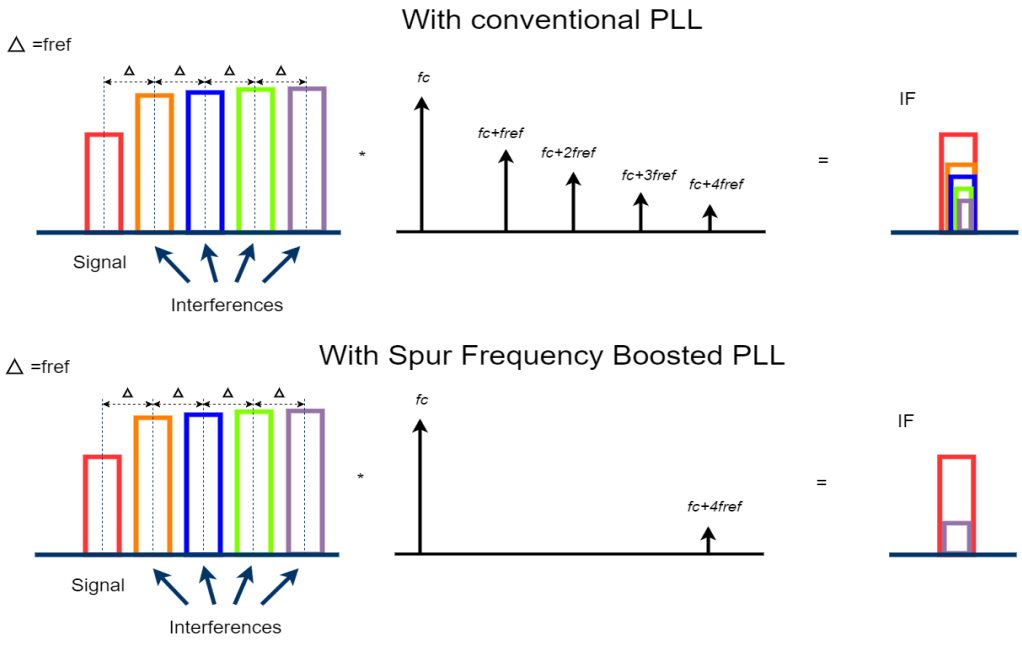

Figure 17 Output IF Signals with Conventional and Spur Frequency Boosted PLL

6.2 Proposed System

The entire system is shown in Figure 18 which is made up of 3 main sub-system: the phase lock loop (PLL), the delay lock loop and the delay calibration loop. The main loop PLL performs as a frequency synthesizer, generating a 2.4 GHz clock using a 32MHz reference clock. The delay locked loop generates 4 phase outputs of the 32MHz reference signal and the 32MHz feedback signal. Calibration block calibrates the phase errors between the 4 phases of the UP or DN signal at the charge pump input node.

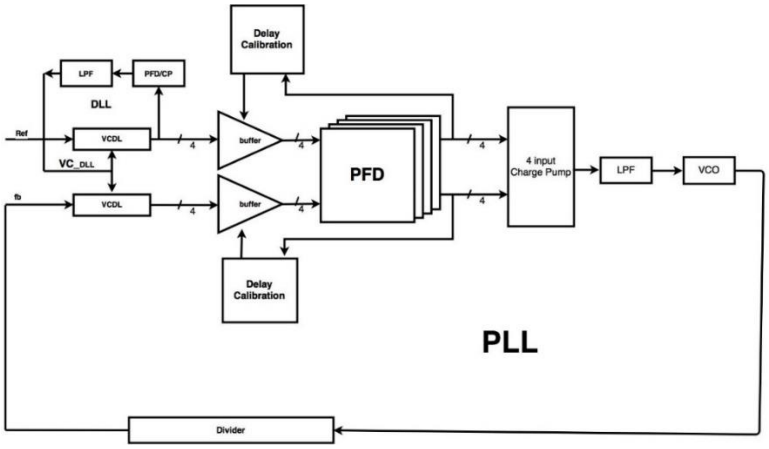

Figure 18 Proposed System

6.3 PLL Design

The main loop is type II phase lock loop (PLL) with a charge pump driving the loop filter as shown as Figure 19.

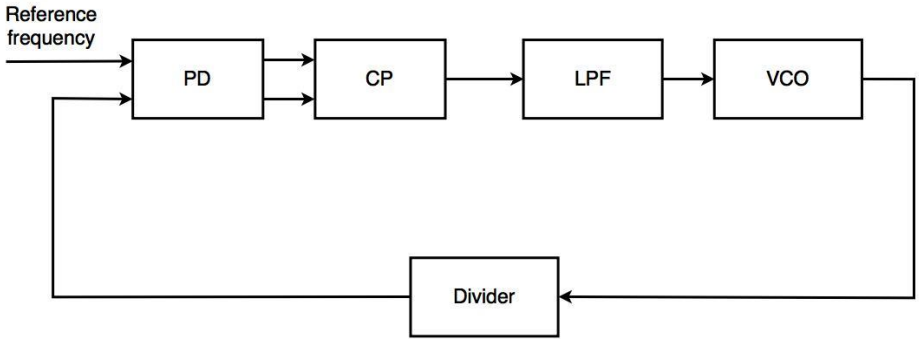

Figure 19 Main Phase Locked Loop

The advantage of this type of PLL is that it can achieve zero phase error even with a frequency offset. The loop can be considered as a second order loop, when ignoring the higher order poles in the loop filter and the delay of the delay lock loop. In design of second order loop, the parameters nature frequency ω_n and damping factor ζ must be carefully chose for settling performance and stability. Nature frequency ω_n and damping factor ζ are given by equation (33) and (34) below, respectively, where I_{cp} is the charge pump current value and K_{vco} is the frequency gain of the VCO. In the PLL with DLL, I_{cp} is referred to the total summation of current driven by multiple phases.

$$\omega_n = \sqrt{\frac{I_{cp}K_{vco}}{NC}} \tag{33}$$

$$\zeta = \frac{\omega_n}{2} R_1 C \tag{34}$$

The loop filter is a second order passive filter, shown in Figure 20. And its poles and zeros location is given by Table 5.

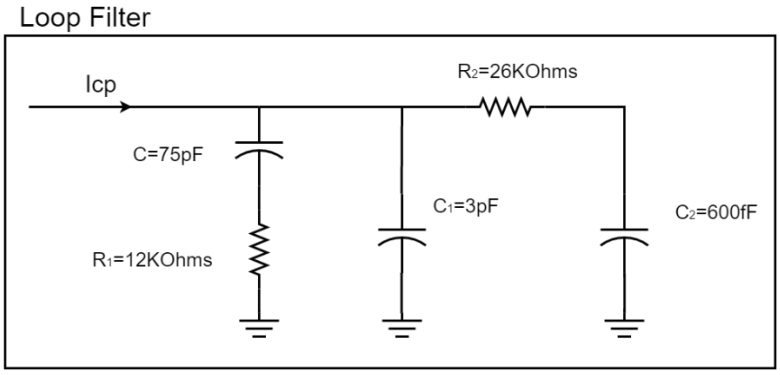

Figure 20 Passive Low-Pass Filter

Table 5 Configuration of the Loop Filter

	Expression	Value
Zero	$\frac{1}{R_1 C}$	$177KHz$
Pole1	$\frac{1}{R_1 \frac{C C_1}{C + C_1}}$	$4.6MHz$
Pole2	$\frac{1}{R_2 C_2}$	$10MHz$

This PLL is designed with $I_{cp} = 0.7mA$ and $K_{vco} = 90MHz/V$. And the reference frequency is 32*MHz* and output frequency is 2.4*GHz*, so the divider factor is *N*=75. Therefore according to equation 33 and 34, the nature frequency ω_n is approximately 530 *kHz* and damping factor ζ is about 1.5.

The open loop bode diagram with consider the entire loop filter in Figure 20 is shown in Figure 21. We can see the phase margin of the main phase lock loop is about 55

deg. Also, the closed loop transfer function is shown in Figure 22, where we can get the closed loop bandwidth BW is 2.26 *MHz*, a moderate value for settling time and stability.

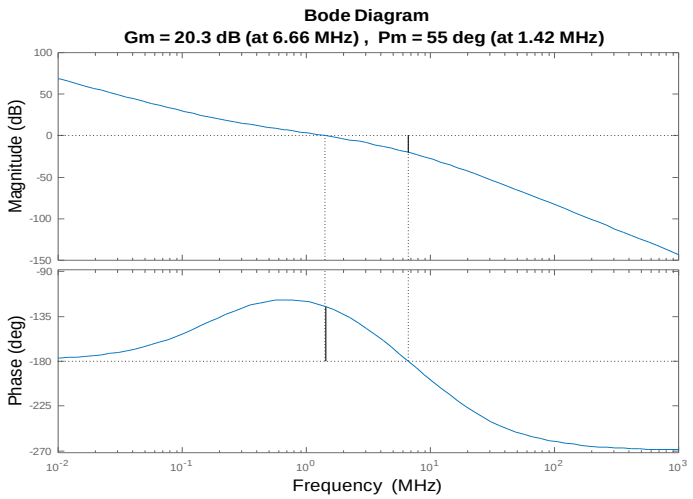

Figure 21 Open Loop Transfer Function

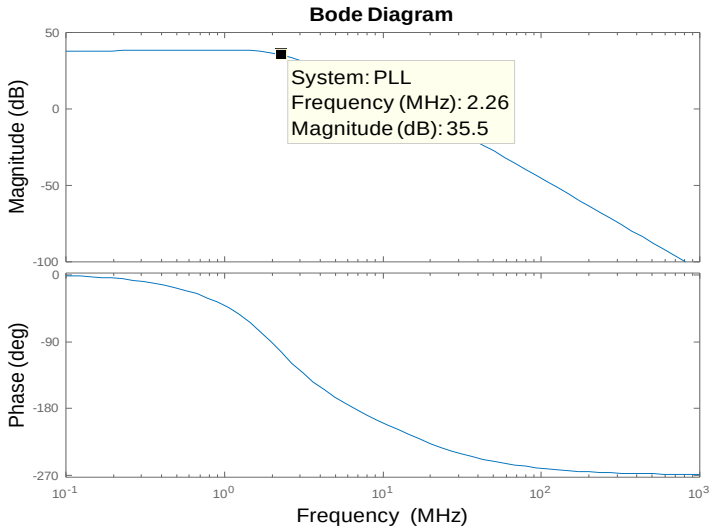

Figure 22 Closed Loop Transfer Function

6.4 DLL Design

The delay lock loop is a first order system without low frequency pole and the closed loop transfer function is given by equation (35) and the closed loop bandwidth is given by equation (36), according reference [13]. This first order system is unconditionally stable as long as continuous-time approximation ($\omega_n \ll \omega_{REF}$) holds.

$$\frac{D_O}{D_I} = \frac{1}{1 + \frac{s}{\omega_n}} \tag{35}$$

$$\omega_n = I_{CP} K_{DL} F_{REF} / C \tag{36}$$

In this work, the bandwidth of the DLL approximately equals to 7*MHz*. The bandwidth is 3 times wider than the basic PLL, so it does not introduce much extra settling time. The block diagram is shown in Figure 23.

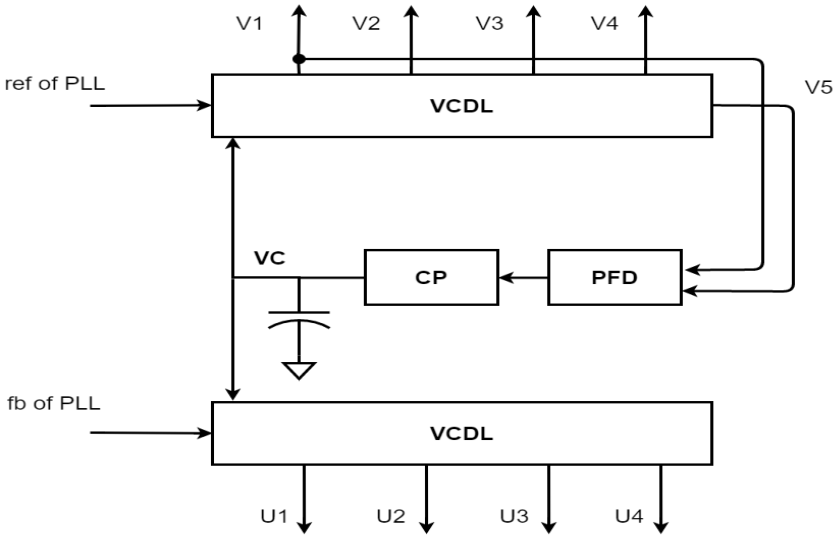

Figure 23 4-Phases Generator Using DLL

6.5 Delay Calibration

6.5.1 Delay Mismatches

DLL locks phase difference between the feedback signal (V5) and the first output (V1) as 360°. So the subsequent outputs has 90° phase difference as long as each stages are identical. However, these stages are different because there are errors in the manufacture period. In CMOS process, there are usually up to 5% mismatches in the capacitance. In terms of active devices, mainly refer to transistors, the mismatches are much serious.

The effects of delay mismatches can be shown in Figure 24. Suppose the PLL settled with a static phase error, DN signals precedes due to charge pump up and down current mismatch. The ideal case is shown in Figure 24 a), the ripples appear at a frequency of 4 times of reference frequency. When Up and Down signals has errors in Φ2 and Φ3 and the polarities of errors are the same between Up and Down as shown as Figure 24 b), the shape of ripples remains the same but time intervals are different between Φ1 and Φ2 and between Φ2 and Φ3. And these different intervals repeat every reference period, causing reference spurs in the PLL's output. Suppose the errors process opposite polarities between Up and Down, as shown as Figure 24 c). Disturbance with one reference period occurs, so the PLL's outputs reference spurs.

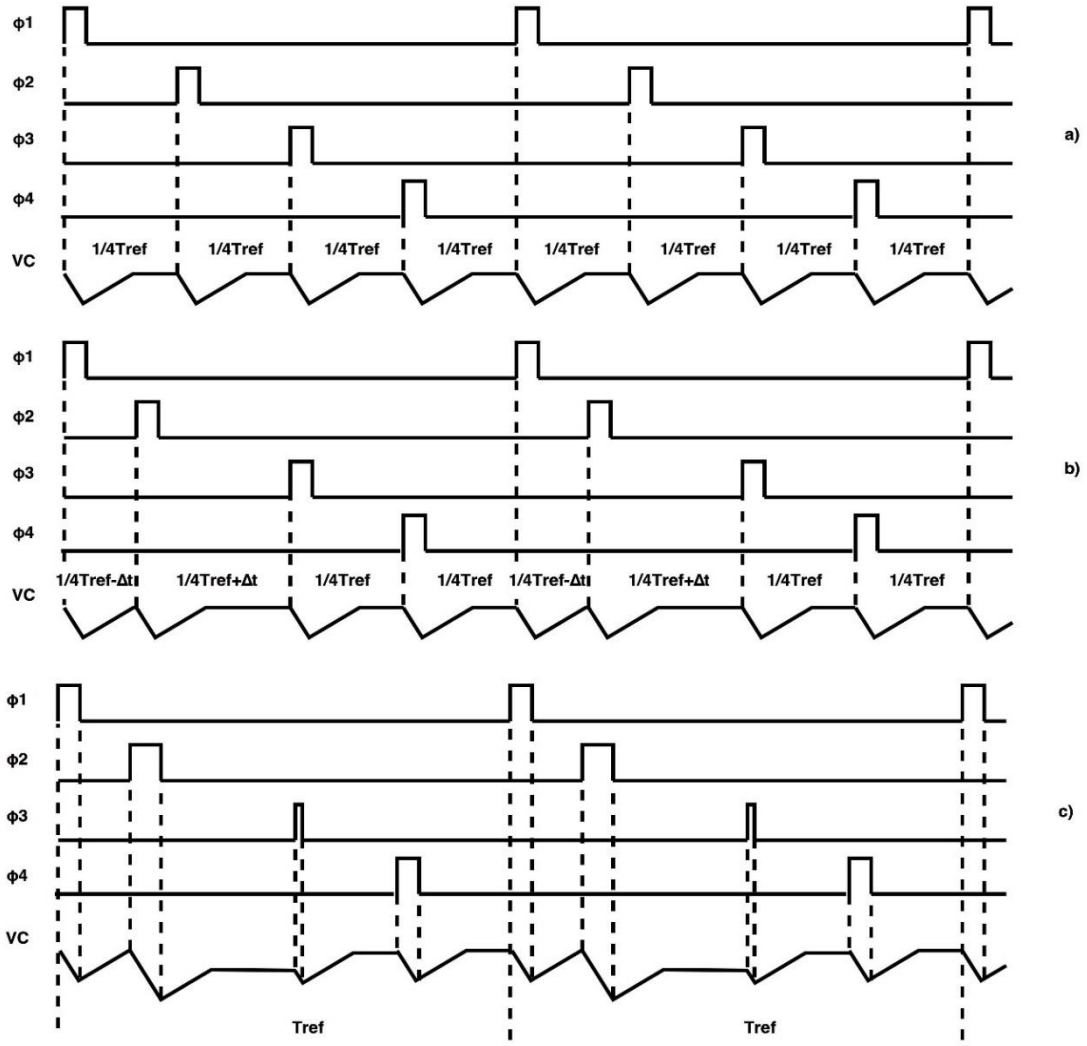

Figure 24 Voltage Ripples with Delay Mismatches

6.5.2 Calibration Design

The delay calibration is necessitated by the fact that mismatches in VCDL always exist and the system performance on reference spur suppression is sensitive by delay error because of mismatches shown in Section 6.4.1. The basic calibration loop is shown in Figure 25.

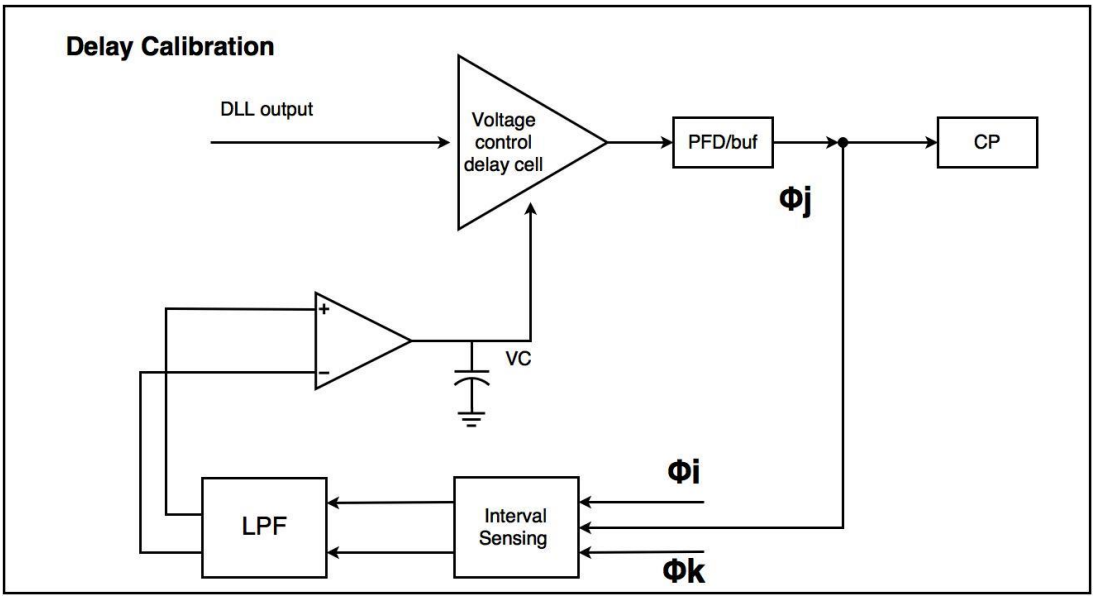

Figure 25 Delay Calibration Block

The calibration feedback path includes an interval sensing block, a low pass filter and an Opamp. The interval sensing block compares the rising edges of 3 phases at the input of the charge pump and outputs the phase difference between the first input Φi and the second input Φj and the phase difference between the second input Φj and the third input Φk, as shown as Figure 26.

In the ideal case, Φj is at the middle of Φi and Φk, and so the two outputs have the same width. After through the low-pass filter and the Opamp, the total charge and discharge during one period are the same causing no voltage changes on the control voltage (VC) after a period.

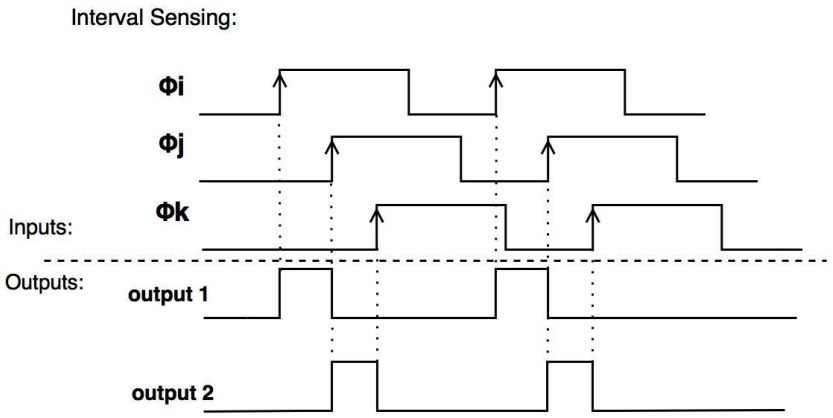

Figure 26 Inputs and Outputs of the Interval Sense Block

There are four parallel calibration loop, and the whole calibration scheme is shown in Table 6. Specifically, interval from φ1 to φ3 and the interval from φ3 to next φ1 are compared to generate control voltage for φ3. Interval from φ1 to φ2 and the interval from φ2 to φ3 are compared to generate control voltage for φ2; interval from φ3 to φ4 and the interval from φ4 to next φ1 are compared to generate control voltage for φ4.

Table 6 Calibration Schemes

	loop 1			loop 2			loop 3			loop 4		
sense phases	Φi	Φj	Φk	Φi	Φj	Φk	Φi	Φj	Φk	Φi	Φj	Φk
	φ3	φ1	φ3	φ1	φ3	φ1	φ1	φ2	φ3	φ3	φ4	φ1
control phase	φ1			φ3			φ2			φ4		

Passive low pass filter is added before the Opamp, in order to suppress the input swing of the Opamp. While the low pass filter placing a high frequency pole, the calibration loop becomes second order loop. The product of nature frequency ω_n and damping factor ζ are around several MHz, for a moderate settling speed. The calibration bandwidth for φ3 is lower than the other two loops because the nominal width of outputs of interval sensing block are larger and so lower bandwidth is needed to suppress the swing.

7. CIRCUIT DESIGN

7.1 Circuits in PLL

7.1.1 Charge Pump

In the charge pump design of PLL, there is always a challenge of minimizing the mismatch in charge pump. While the PFD translates the phase difference into the widths of UP and DOWN signal in the output, charge pump translates the widths into charge or discharge and causes the change in control voltage (VC) of VCO. Any differences between charge and discharge current will introduce phase offset in PLL. There are several mechanisms of the occurrence of charge and discharge mismatch, including UP/DN skew and width mismatch, charge injection and clock feedthrough of the switching transistor, charge sharing and channel-length modulation. The first three cause dynamic mismatch and the last on cause static mismatch. The static phase error after PLL settled will causes ripple in VC and the reference spurs in the frequency domain.

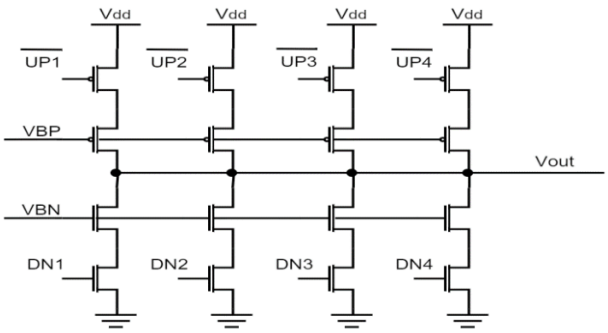

Figure 27 4-Inputs Charge Pump Design

As shown as Figure 27, the four phases input charge pump is tied together by four branches of simple single ended charge pump. Switch in source structure is adopted in the charge pump design which means the switching transistor are placed in the supply side (VDD or ground). In the conventional switch in drain charge pump, at the beginning of switches turning on, the voltage level of source node of pmos switch is still close to the supply VDD, it causes a peak charge on the output node. The nmos switching experience the same situation, causing a peak dis charge on the output node. The matching of this peak current from nmos and pmos is difficult since it is not generate by the current mirror and it is dependent to the output voltage. Unlike the conventional switch in drain charge pump, switch in source charge pump in this project avoids this transition period so the speed of switching is faster.

7.1.2 VCO

The VCO design uses simple NMOS cross couple VCO shown in Figure 28, with the advantage of easy startup. And the quality factor Q of the inductor is 6. The VCO can output 8 bands by means of switch capacitors. Varactor is capacitive coupling to the VCO tank, maximizing the tuning range.

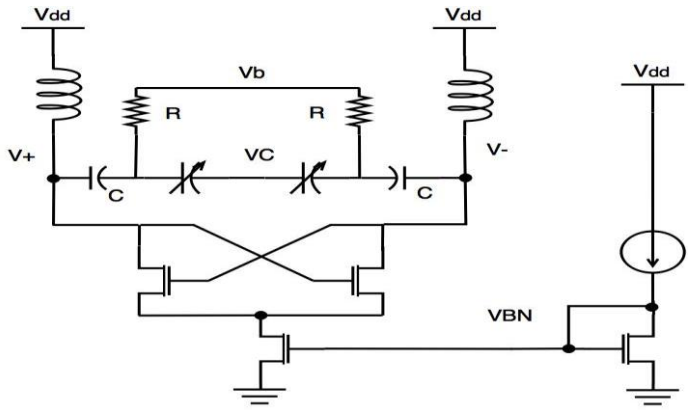

Figure 28 Cross Couple VCO

The output frequency ranges from 2.38 to 2.66 GHz, as in Figure 29. Figure 30 shows the phase noise at 1 MHz offset in the first band (around 2.4GHz).

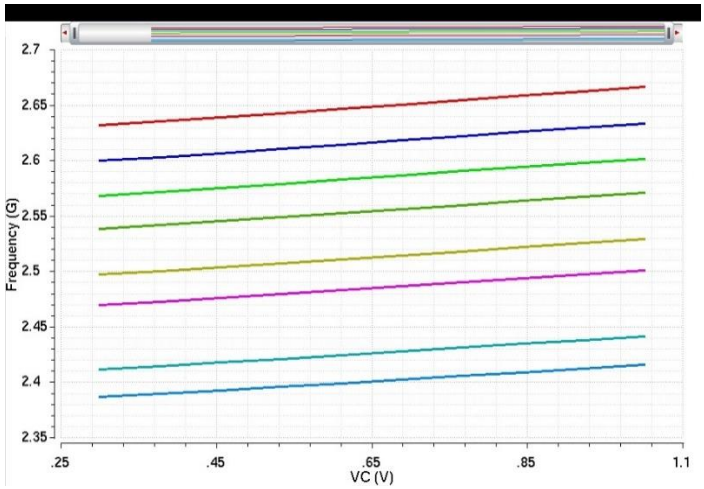

Figure 29 Output Frequency vs Control Voltage

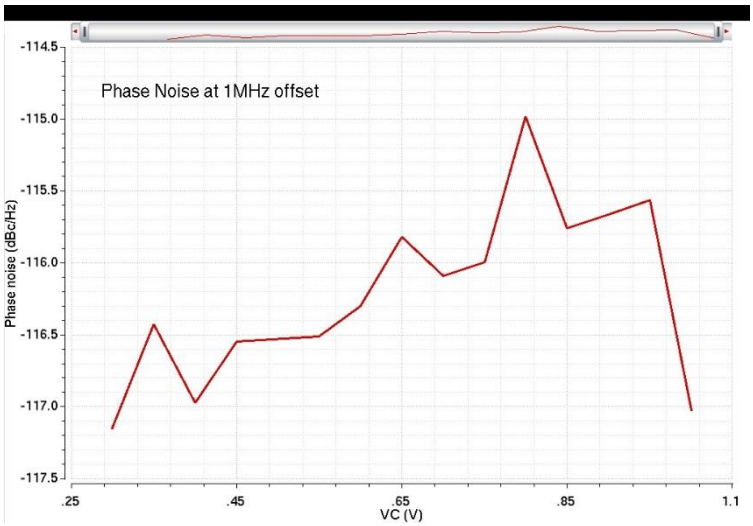

Figure 30 Phase Noise at 1MHz Frequency Offset

7.1.3 PFD

A high speed design of tri-states phase and frequency detector is used in this system as shown as Figure 31.

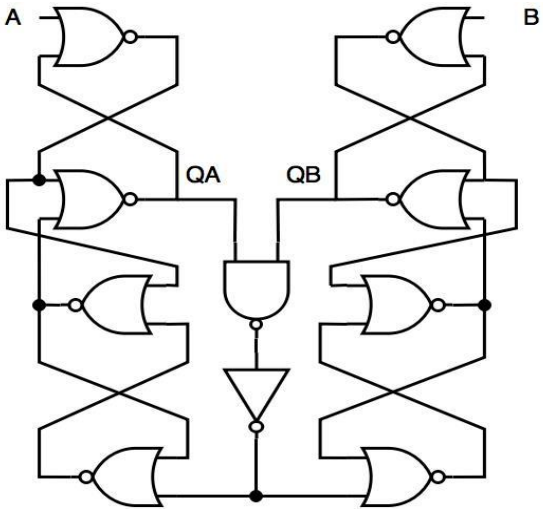

Figure 31 High-Speed PFD Design

7.2 DLL Design

7.2.1 VCDL

In the designed system, there are two identical voltage control delay line. One delay line is in the delay locked loop (DLL) while another one is controlled by the control voltage in the DLL. If the two delay line are ideally identical, the outputs of the delay line have same delays. The voltage control delay line is shown in Figure 32.

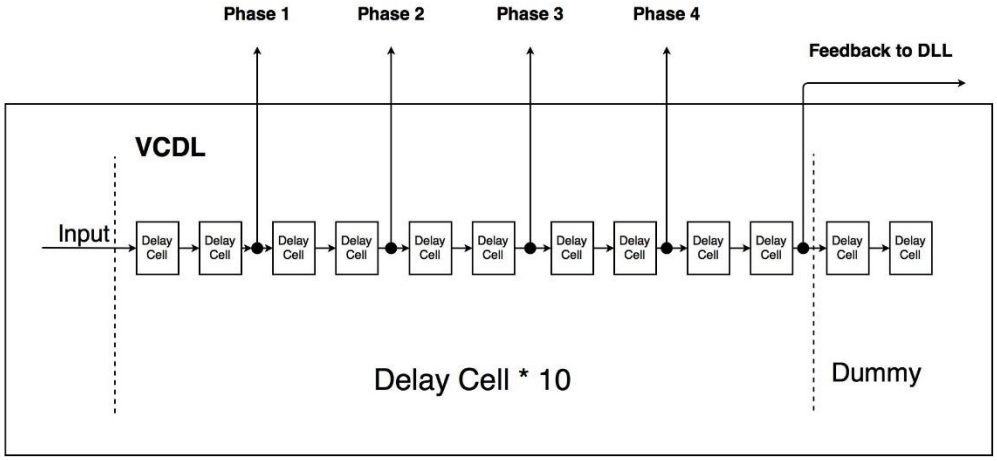

Figure 32 Delay Line

There are four identical stages and 2 inverter based delay cells in each stage. Current starved structure is used in the delay cell design where the control voltage determine the maximum charge and discharge the inverter draws, as shown as Figure 33. The delay of single delay cell is the total time T for the capacitor C is charged or discharged to Vth which is the threshold voltage of next delay cell as equation (7). Thus, the delay of each delay cell is monotonic decided by the control voltage, shown as Figure 34.

$$\int_0^T i(t)dt = CV_{th} \ \ or \ \int_0^T i(t)dt = C(V_{dd} - V_{th}) \tag{37}$$

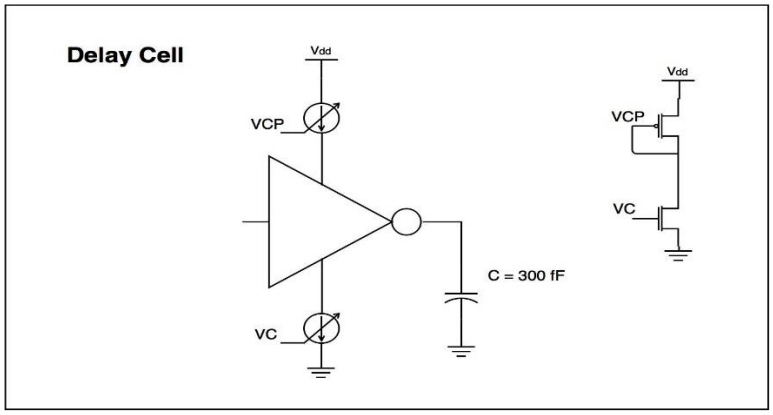

Figure 33 Delay Cell Realization in a Delay Line

From Figure 34, we can expect the locked control voltage of the DLL is around 700mV. The gain of the delay line is given by equation (38).

$$K_{DL} = -\frac{4}{360°} * \frac{530.6}{f_{ref}} = 184\ n/V \tag{38}$$

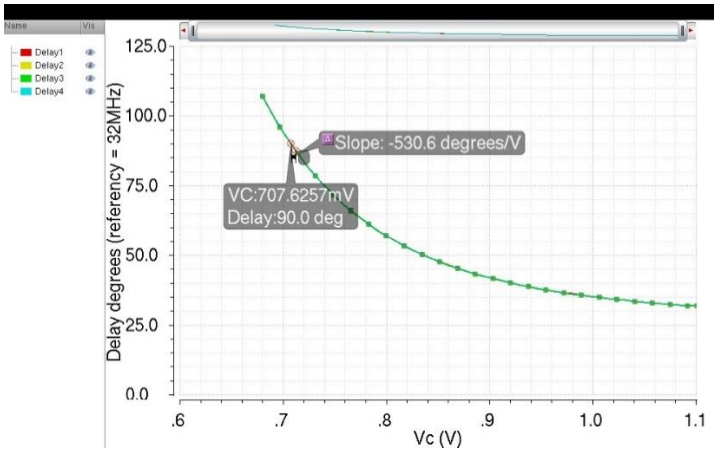

Figure 34 Delay of Single Stage vs. Control Voltage

7.2.2 Simulation Results

Figure 35 is the control voltage settling and lock status signal to enable the delay calibration blocks. Figure 36 shows the four phases outputs of the two delay lines.

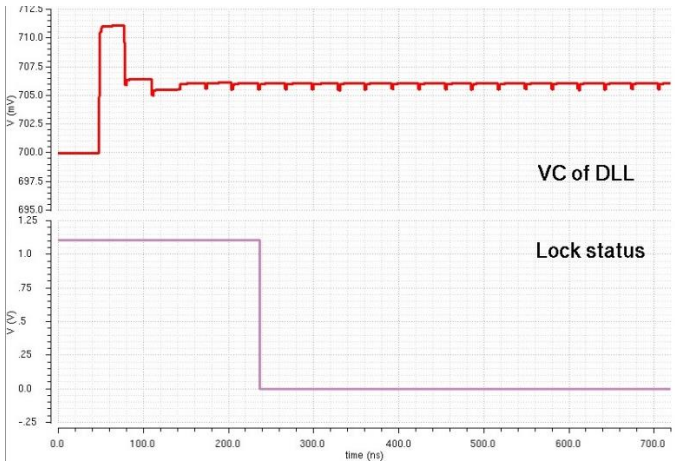

Figure 35 Transient Control Voltage

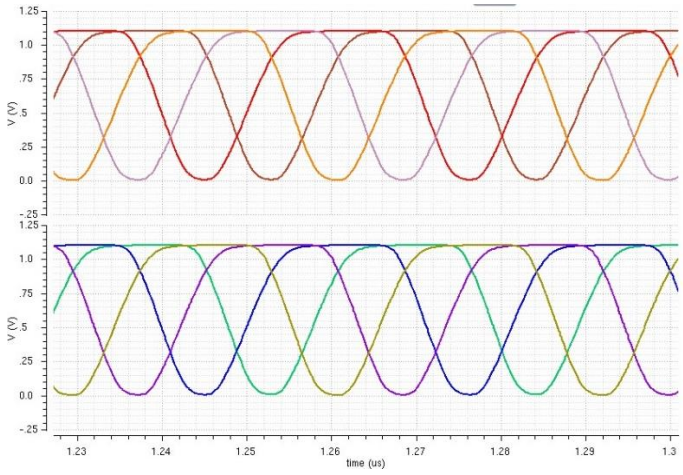

Figure 36 Four Phases Output

7.3 Delay Calibration

The calibration scheme is shown in Figure 37. UP and Down paths are calibrated independently.

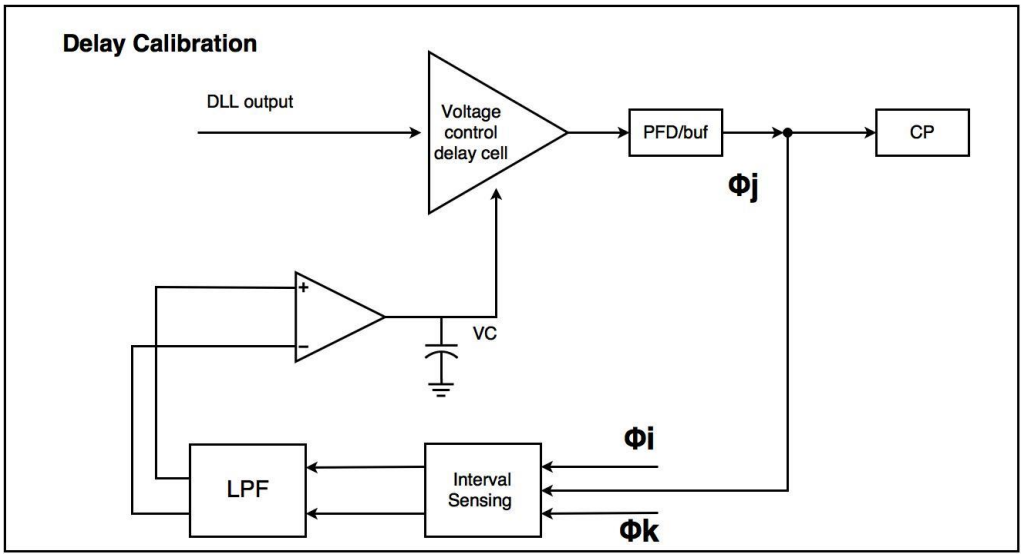

Figure 37 Delay Calibration Block

7.3.1 Delay Cell

To calibrate the delay of each phase, buffers for each phase are placed after the DLL output and before the PFDs, whose delays are voltage tuning. These buffers are realized by current starved delay cell shown as Figure 38. M1-M4 are two cascaded inverters, as the core of this buffer. The maximum current driving the inverters are control by VC and VCP, where VCP is generated by a current mirror. If VC is below the threshold voltage, Mc1-Mc4 outputs no currents. To avoid the situation the delay is infinite, Mb1-Mb4 are added to generating minimum current value and thus the buffer has maximum delay. To stabilize the PLL, the delay should be well less than one reference period, which is 31ns in this system.

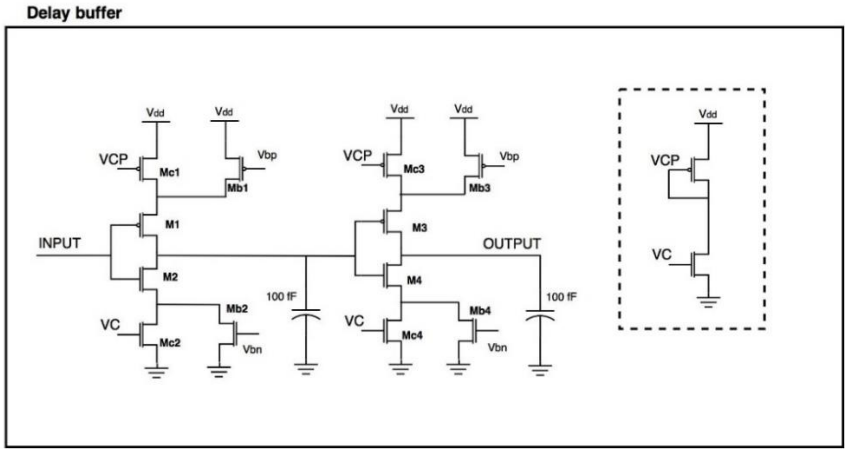

Figure 38 Delay Cell in Calibration

The delay curve vs control voltage of the buffer is shown in Figure 39, in which we can see the delay ranges from 1ns to 4.8ns, and the delay gain at VC=600m is 7.49n/V.

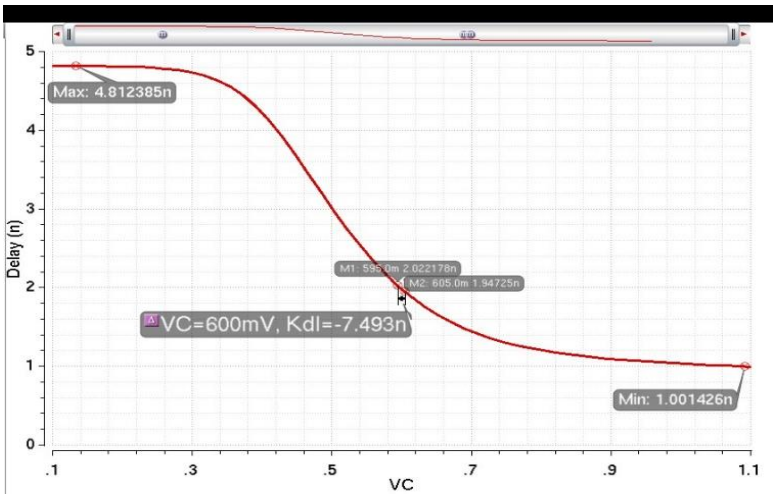

Figure 39 Delay vs Control Voltage

7.3.2 Interval Sensing Circuit

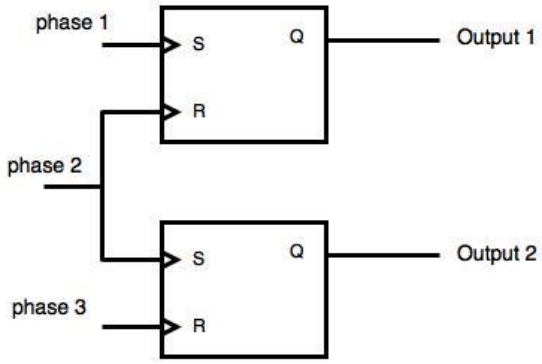

Figure 40 Interval Sense Block

The interval sensing circuit is made up of 2 RS flip-flops shown as Figure 40, trigging by rising edge of three input phases. And the schematic of the RS flip-flop is shown by Figure 41, which is used in the Down path. As in the UP path, low level voltage

‘0’ turns on the charge pump, as shown as Figure 42. Therefore, complementary logic is used in the interval sensing circuit for the UP path calibration which is triggering by falling edges.

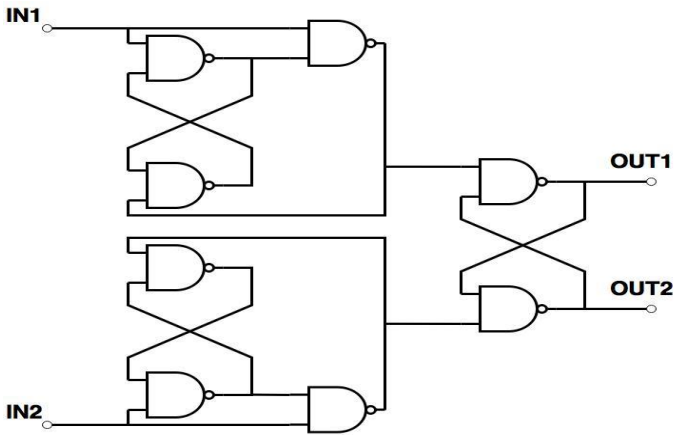

Figure 41 Logic Implement of Interval Sense Block (DN)

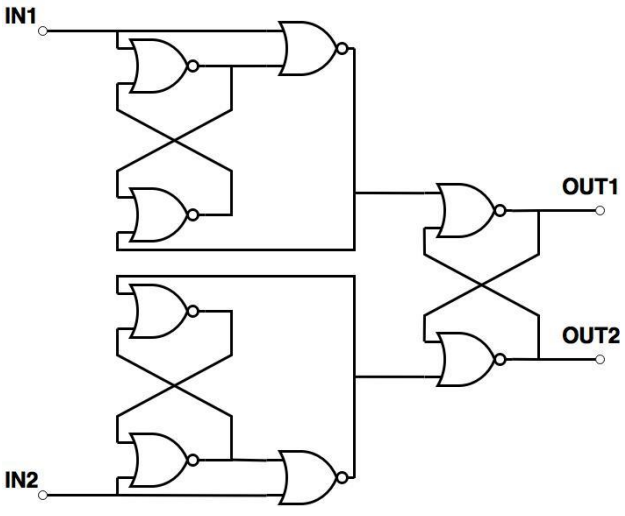

Figure 42 Logic Implement of Interval Sense Block (UP)

7.3.3 Low Pass Filter

Passive RC low pass filter is using to suppress the input swing of the Opamp. In the loop of φ1 and φ3, R is 150KΩ and C is 1pF. The accuracy of these RC value affects the settling speed but does not affect the accuracy of calibration.

7.3.4 Opamps

As introducing in the system design part, there are 4 parallel calibration loops for 4 phases calibration, φ3 is calibrated using φ1 and φ3 while φ1 is calibrated using φ3, φ1 and φ3. Then φ2 is calibrated using φ1, φ2 and φ3 while φ4 is calibrated using φ3, φ4 and φ1.

The output duty cycle of interval sensing block in the loop of φ1 and φ3 is around 50% and the output duty cycle of interval sensing block in the loop of φ2 and that in the loop of φ4 are 25%. After passing low pass filter, the input level of opamp in the loop of φ3 is 550mV the input level of opamps in the loop of φ2 and φ4 is 275mV in the DN and 875mV in the UP path. This difference in the input and the high gain needed requires separate design different opamps otherwise the power is traded off.

7.3.4.1 OPAMP1

Opamp 1 is used in the calibration loops to calibrate φ1 and φ3 in the UP path and DN path. This design uses a cascode structure with PMOS input transistor, as shown as Figure 43.

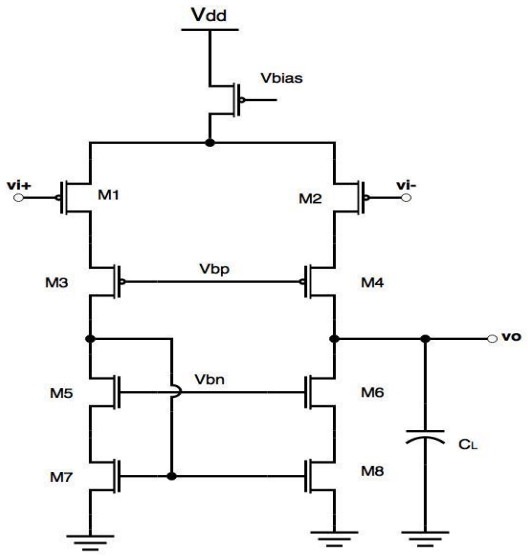

Figure 43 Opamp Used in φ1 and φ3 Calibration

From Figure 44, we can get the DC gain of this opamp is 40.2dB, unit gain frequency is 88.35MHz and the phase margin is 89 degrees.

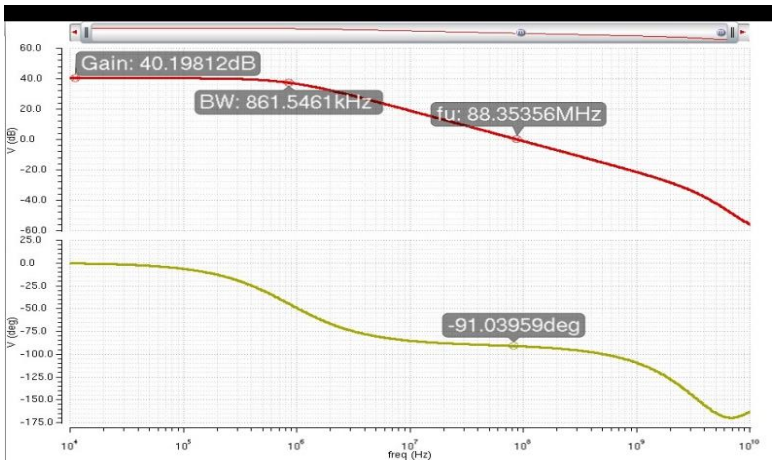

Figure 44 AC Response of Opamp 1

7.3.4.2 OPAMP2

The realization of opamp in the loop of φ2 and the loop of φ4 in the DN path is a folded cascode structure as shown as Figure 45. From Figure 46, we can get the DC gain of this opamp is 38.9dB, unit gain frequency is 41.75MHz and the phase margin is 88.8 degrees.

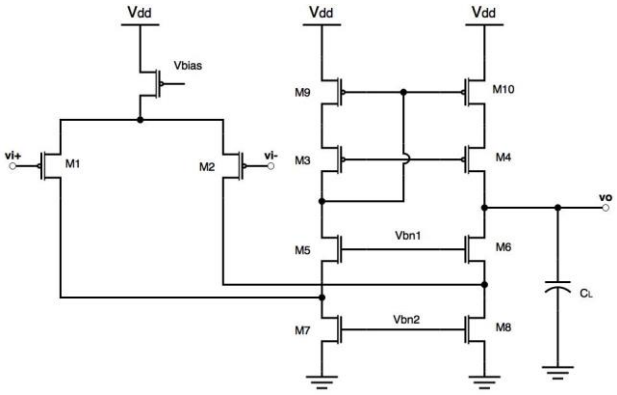

Figure 45 Opamp Used in φ2 and φ4 Calibration

Figure 46 AC Response of Opamp 2

7.3.5 Simulation Results

Figure 47 to Figure 50 shows the simulation with of the calibration of phase 1 and phase 3 with and input error of 5% of the nominal delay. The calibration block is enable at t = 50ns.

A period of 0.5µs of open loop operation is added mainly for the common mode settling as the initial state is uncontrollable. In the initial state, the gain of the loop may be small and the loop needs long time to settle both in common mode and differential mode. A reference voltage source controls the delay of phase 1 and phase 3. The input phase error is integrated in this period, with VC1 and VC3 locating different sides of the dc operating point, until the opamps are saturated. If the initial phase error is negligible, both VC1 and VC3 change slowly to around the dc operating point of the opamp output.

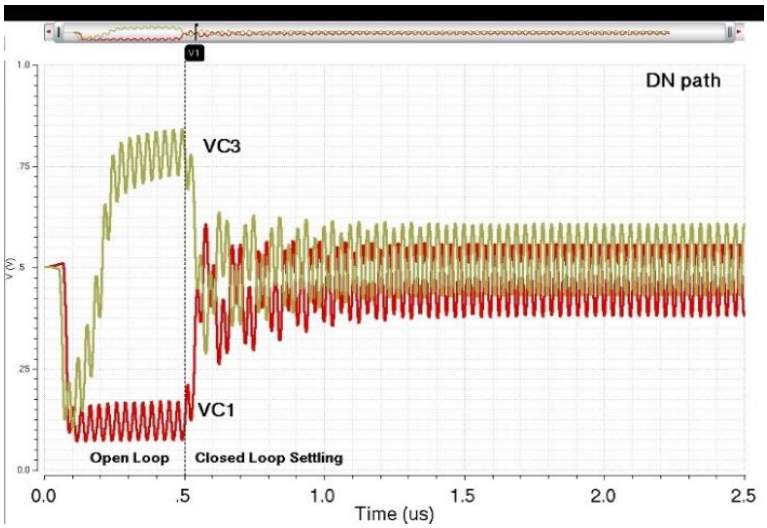

Figure 47 Settling of VC of φ1 and φ3 (DN)

Figure 47 and Figure 49 show the transient voltage settling of the calibration system. Figure 48 and Figure 50 are the phase difference between phase 1 and phase 3 in degrees, in the DN and UP, respectively. The ideal case with no error is 180.

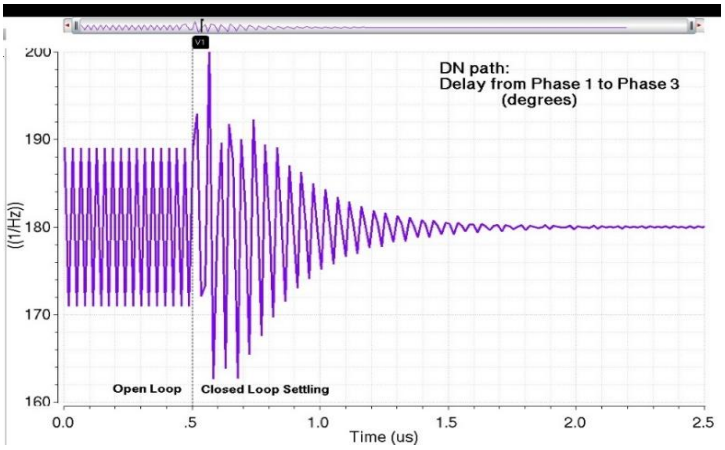

Figure 48 Transient Phase Error of φ3 (DN)

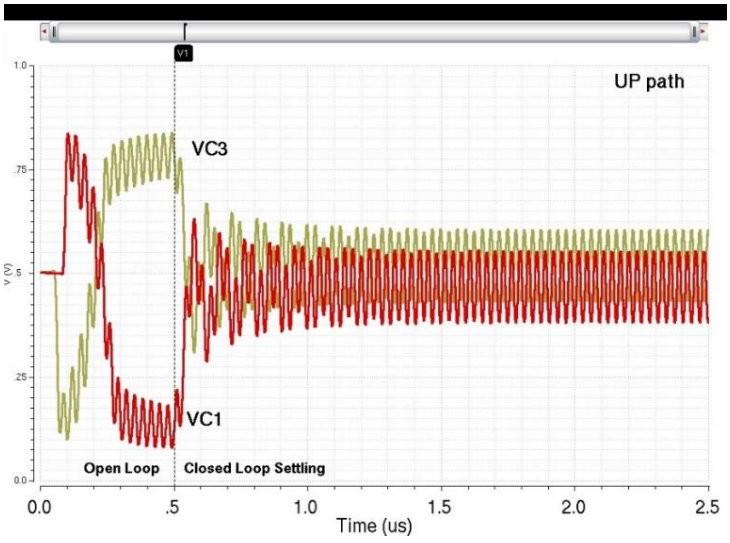

Figure 49 Settling of VC of φ1 and φ3 (UP)

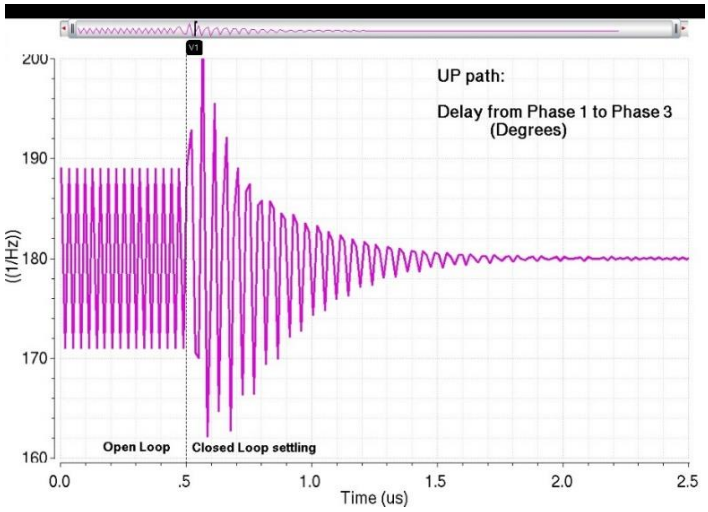

Figure 50 Transient Phase Error of φ3 (UP)

7.4 Calibration (Sample Capacitor)

7.4.1 Introduction

7.4.1.1 Motivation

In the calibration loop, the interval sense blocks output signals with 50% or 25% duty cycle. The wide pulses cause large swing in the opamp input and output. However, only the value of VC in a small time period before the buffers' rising and falling edges determines the delay of the buffer, letting the high swing is unnecessary. Also the high swing may make the opamp enter saturation, constraining the calibration performance.

To suppress the high swing, low pass filters are used in the design proposed in 7.3. But the calibration speed is lower by the low pass filter. There is a tradeoff between the calibration speed and the static error after calibration. Also, the passive low pass filter occupies large area in the chip.

7.4.1.2 General Design

An improved calibration design using sampling capacitor based integrator is proposed in this section, as shown as Figure 51. The function of the interval sense circuit remains the same. The low-pass filter and amplifier in 7.3 are replaced by a switch capacitor integrator. The phase error is sampled in the integrator and then VC is changed according the sampled phase error.

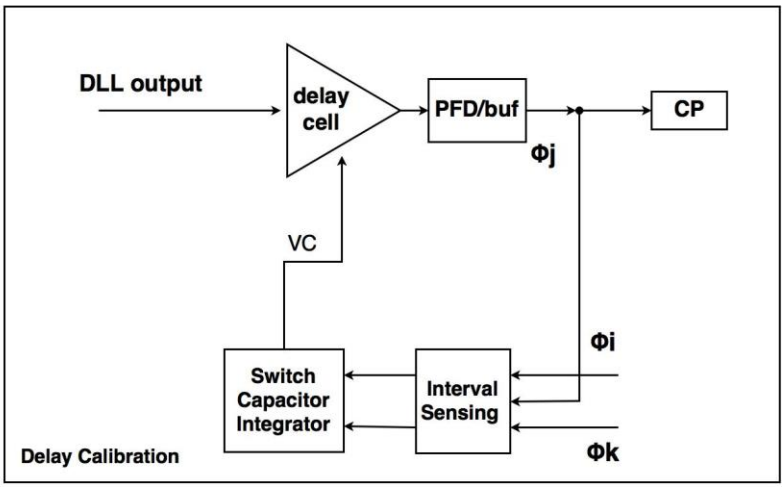

Figure 51 Delay Calibration Using Switch Capacitor Integrator

There are three parallel calibration loop, and the whole calibration scheme is shown in Table 7. Specifically, the delay of φ1 is controlled by a reference dc voltage. Interval from φ1 to φ3 and the interval from φ3 to next φ1 are compared to generate control voltage for φ3. Interval from φ1 to φ2 and the interval from φ2 to φ3 are compared to generate control voltage for φ2; interval from φ3 to φ4 and the interval from φ4 to next φ1 are compared to generate control voltage for φ4.

Table 7 Calibration Schemes of Switch Capacitor Calibration

	loop 1			loop 2			loop 3		
sense phases	Φi	Φj	Φk	Φi	Φj	Φk	Φi	Φj	Φk
	φ1	φ3	φ1	φ1	φ2	φ3	φ3	φ4	φ1
control phase	φ3			φ2			φ4		

7.4.2 Integrator

The design of switch capacitor based integrator is shown in Figure 52, which consists of two differential paths and an output stage (Opamp 2) that converts differential signal to single-ended signal. In each path, there are one charge pump, two sampling capacitors (Ci) and differential amplifier (Opamp 1) with feedback capacitor (Cf).

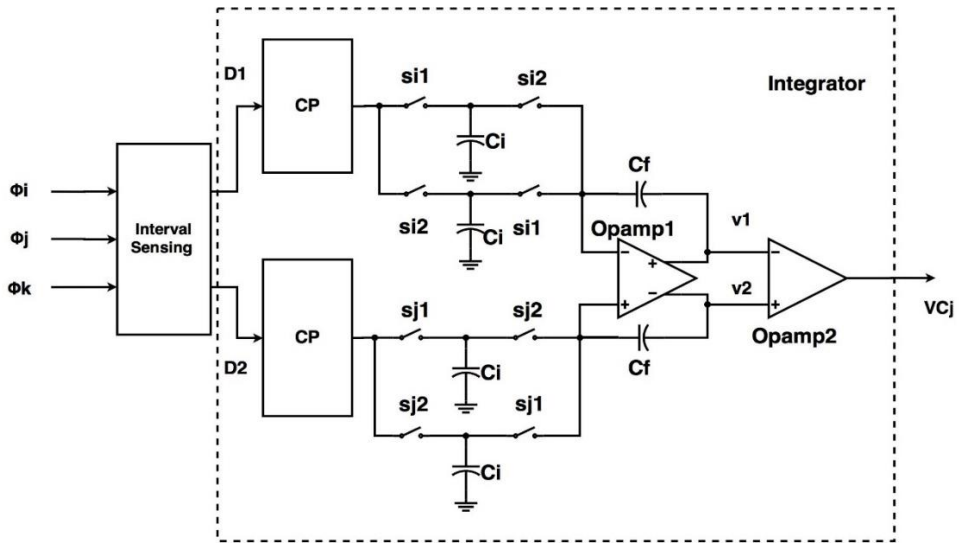

Figure 52 Switch Capacitor Integrator

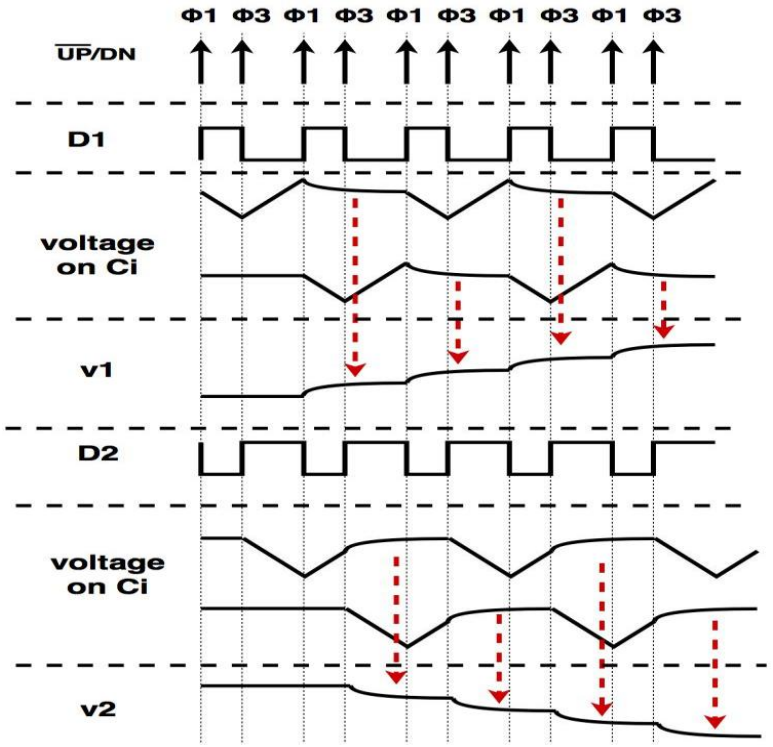

Figure 53 Waveforms in Integrator Used to Calibrate φ3

The waveforms in the integrator to calibrate φ3 is shown in Figure 53. In the first period, the charge pump in one of the differential paths driven by the output of the interval sensing block generates about half period of discharge and then half period of charge on one of the sampling capacitors (Ci). Assuming the delay sensing block has same delay of rising edge and of falling edge and the charge pumps have no current mismatch, the phase error is translated to difference between charge and discharge, changing the voltage value at the end of the sampling phase. In the next period, the charge on Ci is transferred to Cf, causing the change of output voltage of Opamp1. At the end of this phase, the voltage value on Ci returns to the common mode voltage same as the initial condition. And in the

same period, the other sampling capacitor samples the charge of the charge pump. So the output of Opamp 1 is charged alternately by the two sampling capacitors. In the other path, the circuit experiences the same sampling and charging process, but the starting point of each periods is charge to another phase.

For instance, the φ3 is faster than the ideal case like Figure 53. One of the output of Opamp 1 (v1) rises up while the other goes down. After propagated through the output stage (Opamp 2) VC3 goes down, making the delay φ3 larger.

There sampling capacitor is charged in a half of period and discharged in the other half of period, so there is a large swing which is equal to $I_{cp}T/C_i$ (156.25mV in this design). But the voltage change at the input of Opamp1 only equals to $2I_{cp}\Phi_e/C_i$ where Φ_e is the input phase error in this period and is much smaller than the period ($\Phi_e \ll T$). Therefore the swing of the signal in the amplifier is small and the operating range is maximized and so is the calibration range.

As both of outputs of the two differential paths reflect the phase error, the calibration can be realized by a single-ended system with only one path. However, the differential system has great advantage on calibration performance.

In fact, there is mismatch in the interval sensing block between the pulling up current and pulling down current, causing delay error in the output. It is meant that even though φ3 is exactly at the middle between consecutive φ1 at the input, the circuit outputs square wave with duty cycle unequal to 50%. Also the charge always suffers from current mismatch between the PMOS current and NMOS current, though various improving techniques were proposed, just like the charge pump in PLL. In this two case, the phase

error is sampling with an inherent error. In a single ended system, this sampling error finally introducing an offset in the calibration performance. In the differential system, the two path experience sampling errors with same value and polarity. Therefore the system has a common mode error before the opamp 1 and so they are not reflected on the differential mode output of opamp 1. That is the differential system is preferable, compare to a single-ended system.

The gain of the integrator is given by equation (39), where $Z = e^{j\omega/16M}$. I_n and I_p is the absolute current value of the NMOS current and PMOS current in the charge pump, while A_{v2} is the DC gain of Opamp 2. Here is assuming Opamp 1 has infinite DC gain and infinite settling speed, which will be revised in next part. In ideal case, the DC gain of the integrator is infinite, the performance of amplifiers limits the DC gain and so limits the calibration performance.

$$G = -\frac{Z^{-1}}{1-Z^{-1}}\frac{2}{C_f}(I_n + I_p)\,A_{v2} \quad \textbf{(39)}$$

The design parameters are given by Table 8.

Table 8 Design Parameters in SC Integrator

parameter	value	parameter	value
C_i	$1pF$	I_n	$10\mu A$
C_f	$1pF$	I_p	$10\mu A$
A_{v2}	$2dB$		

7.4.3 Circuit Design

7.4.3.1 Charge Pump

Although the current mismatch in the charge pump introduce common mode errors, it is undesired in the calibration system and needs to be suppressed. Large common mode fluctuation in the input influence the gain of opamp1. Once the gain of opamp1 falls below specific level, the integrator is dysfunctional, failing to suppress the phase error or even amplifying it. Also, as the two path in the integrator has 180° phase difference, common mode signal will cause transient differential output as shown as Figure 54.

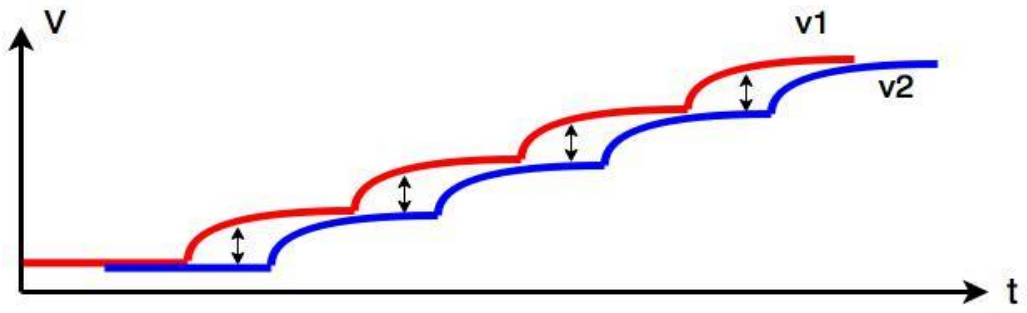

Figure 54 Effect of Common Mode Error

The charge pump design used in the switch capacitor calibration loops is shown in Figure 55. Switch in source structure is adopted in the charge pump design so as to boost the switching speed. The gates of NMOS and PMOS switches are tied together, so there is only one side turned on. The charge pump outputs PMOS current when input equals “0” and outputs NMOS current when input equals “1”.

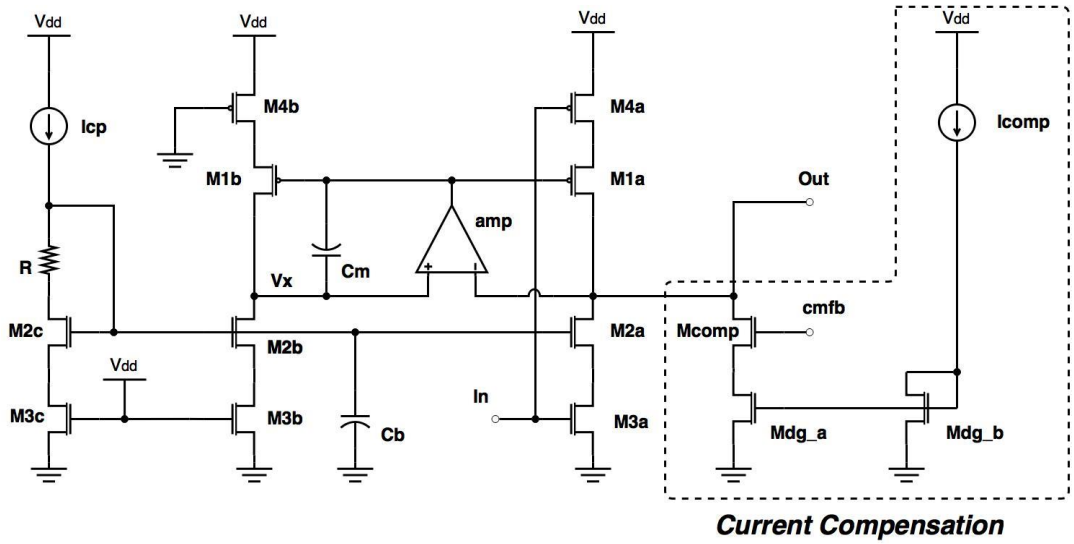

Figure 55 Charge Pump Used to Calibrate φ3

Servo loop in the biasing circuit is used shown as Figure 55. Ideally, by using an amplifier, the voltage at node Vx tracks the value of the output node. Specifically, in first half period the NMOS current let the output node voltage drop from VCM to (VCM-In*T/Ci) and the transient NMOS current varies due to channel length modulation. In the next half period, the PMOS switch on, the PMOS current copies the NMOS current in the replica branch exhibiting the same channel length modulation like the first half period.

The amplifier used in this charge pump design is shown in Figure 56. Cascode topology is used to guarantee the gain at 32MHz. Small capacitor that connects the Vx node and the output of this amplifier provides Miller compensation, improving the stability.

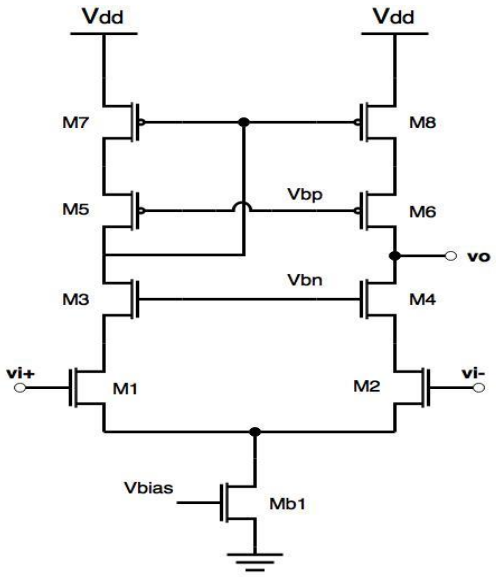

Figure 56 Amplifier Used in the Charge Pump

By using this configuration, the mismatch total PMOS current and NMOS current is under 1%. Small current control by the common mode in the next stage is added to the output to compensate this 1% mismatch.

7.4.3.2 Switch Signal Generation

As every sampling capacitor (Ci) samples the charge in one input period and charges the feedback capacitor in another period, switch signal with double period needs to be generated. The switch signal generation is shown in Figure 57. The input clock is the same as the signal control the charge pump. And this clock frequency is divided by 2 through the frequency divider using true single phase logic (TSPC). And the configuration next to the divider ensures that 2 non-overlapped phases are generated.

The waveforms of input clock and outputs are shown in Figure 58.

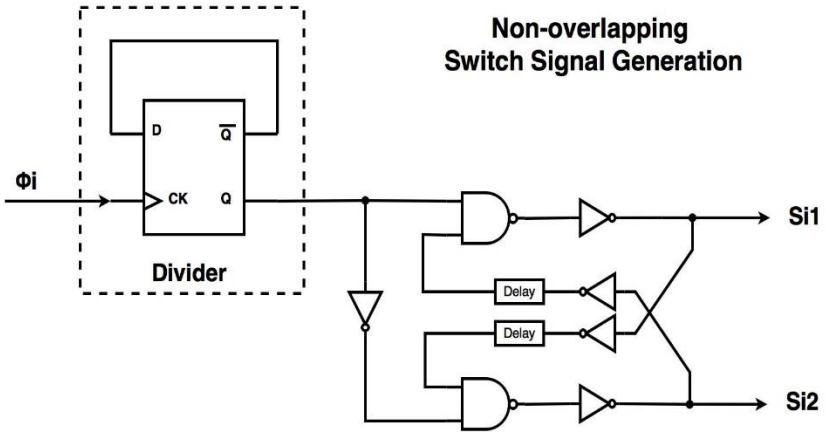

Figure 57 Non-Overlapping Switch Signal Generation

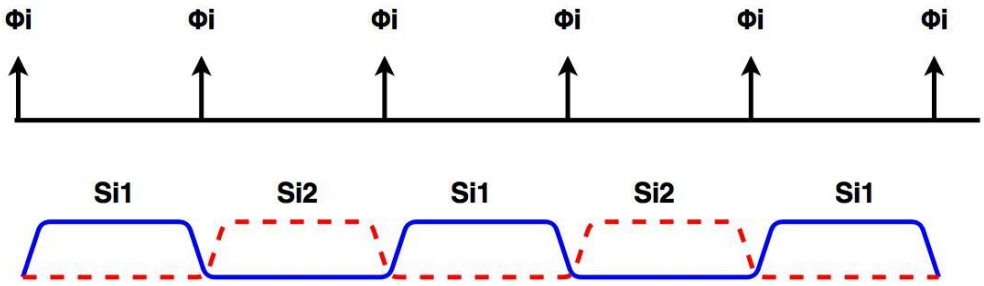

Figure 58 Input Clock and the Output Switch Signals

7.4.3.3 Opamp 1

7.4.3.3.1 Analysis

The ideal gain of the integrator is given by equation (40) under the assumption that Opamp 1 has infinite DC gain and infinite fast response.

$$G_{ideal} = -\frac{Z^{-1}}{1-Z^{-1}}\frac{2}{C_f}(I_n + I_p)\,A_{v2} \qquad \textbf{(40)}$$

However, in practice the DC gain of the opamp is finite especially in the low power application, which introduces static error even if the settling time is unlimited. The actual gain of the integrator is given by equation (41).

$$G_{actual} = -\frac{Z^{-1}}{1-Z^{-1}}\frac{2}{C_f + \frac{C_f + C_i}{A_{v1}}}(I_n + I_p)\,A_{v2} \quad \textbf{(41)}$$

So the error in percentage due to finite DC gain is given by equation (42).

$$E_{static} \approx -\frac{1+\frac{Ci}{Cf}}{A_{v1}} * 100\% \quad \textbf{(42)}$$

Also, the maximum operation speed of the Opamp is also finite due the parasitic capacitance in input and output nodes as shown as Figure 59. So dynamic error is introduced due to uncompleted settling.

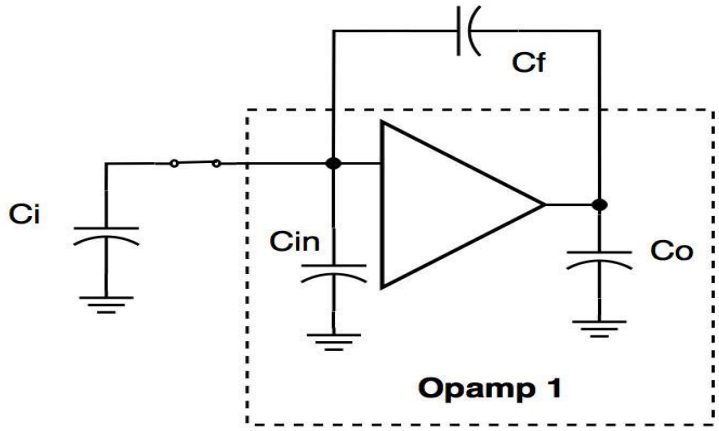

Figure 59 Opamp Model

Assuming there are no other dominant pole inside the opamp, the settling response is determined by the input and output parasitic capacitance. The pole introduced is given by equation (43).

$$\omega_p = \frac{g_m}{C_i + C_{in} + C_o + \frac{C_o}{C_f}(C_i + C_{in})} \quad \textbf{(43)}$$

The dynamic error is given by equation (44) where t is the settling time equal to $1/f_{ref}$ in this design.

$$E_{dynamic} = e^{-\omega_p t} \quad \textbf{(44)}$$

Therefore, to suppress both the static error and dynamic error, the Opamp needs to have large DC gain and trans-conductance as possible, but power is the trade-off.

7.4.3.3.2 Design

The differential amplifier used in the integrator adopts a full input range pseudo cascode amplifier with common mode feedforward as shown as Figure 60.

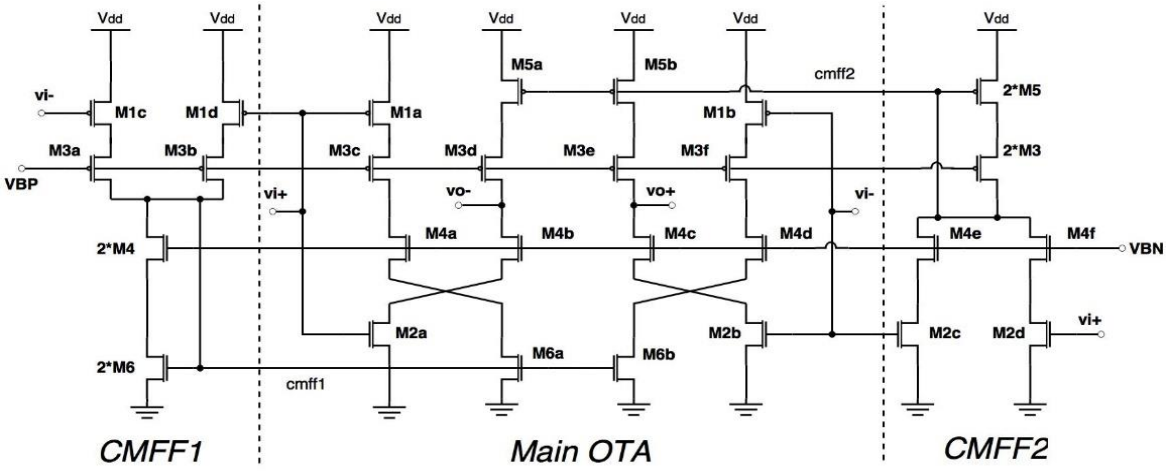

Figure 60 Pseudo Differential Opamp Design

As low power design dominate in modern CMOS applications, the supply voltage in the new generations of CMOS technologies comes to lower and lower, and becomes one of bottlenecks of the design of CMOS amplifiers especially for amplifiers with both high DC gain and wide output range. In a cascode stage with tail current source, the achievable output swing is given by ($V_{DD} - \sum Vov$). To get reasonable response speed, the overdrive voltage Vov of input transistors needs to be large as around 150mV to 200mV. And the cascode transistors can have smaller Vov as about 100mV. So the left voltage room is about 400mV to 500mV which is not enough for the proposed calibration system. Moreover, the input range is also limited by the low voltage headroom and relative high threshold voltage Vth.

Pseudo differential amplifiers have advantage in low power supply operation. Unlike conventional differential amplifiers, tail current source is removed in pseudo differential structure and so the voltage headroom is saved both in the input and output.

But common mode signal in the input is also amplified as same as the differential signal, which is not desire. Common mode feedforward branches are added to suppress the common amplification.

To get a larger input range, full swing topology is used in this design. Basically, two pseudo amplifiers with common mode feedforward are design with pmos and nmos input transistors, respectively. And they are tied parallel together, to make up of a single amplifier. The trans-conductance of the tied-up opamp is doubled, while the DC gain remain the same as single amplifier.

7.4.3.4 Output Stage (Opamp2)

To convert the differential signal to single-ended signal to control the delay of the delay cell. The circuit realization is shown in Figure 61.

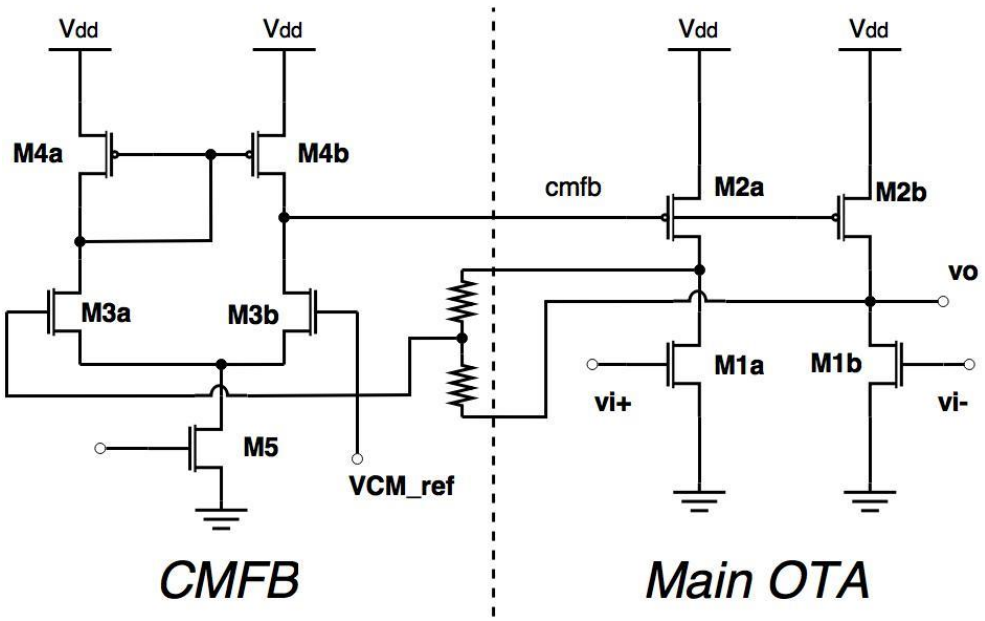

Figure 61 Output Stage

7.4.3.5 Common Mode Feedback

As analysis in the design of charge pump, the common errors are proved to problematic. Even though improved charge pump design is used, there is still small portion of mismatch between PMOS and NMOS current. This current mismatch will make the common mode voltage rise up or fall down continuously. After a long period of operation, the system will break down because of the accumulated commode error.

Therefore, a feedback path as show in Figure 62 is design to provide small piece of compensation current added to the charge pump.

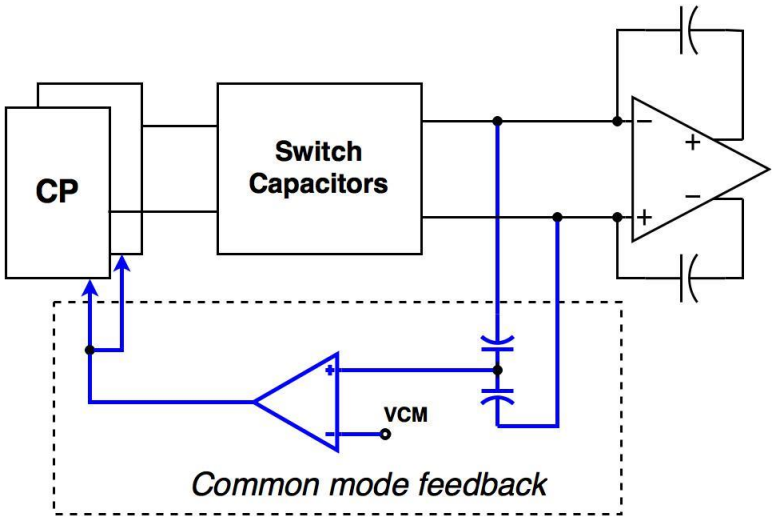

Figure 62 Common Mode Feedback

The circuit implement is shown in Figure 63. Specifically, two small capacitor sample the common mode level at the input of Opamp 1. A telescopic differential pair compares this common mode level to a reference common mode voltage source. In the next stage, source degenerated transistor (Mcomp) transform this common voltage signal to current. As the settled value of common feedback voltage (cmfb) is about one threshold voltage (Vth), the source node of Mcomp is about zero and so Mdg_a operates in linear region like a resistor. Mdg_a is biased as a current source with current Icomp equal to 2% of the charge pump current. In the common mode feedback settling, the transient cmfb

may well exceed threshold voltage, though, the output current of the compensation will not exceed Icomp and so will not influence the normal operation of the charge pump.

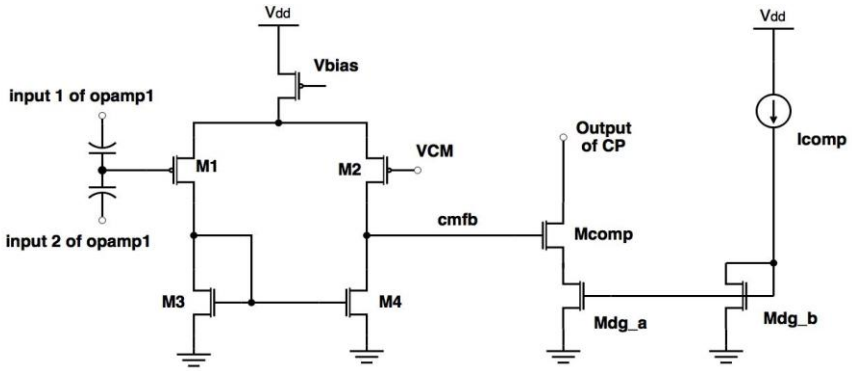

Figure 63 Circuit Implement of Common Mode Feedback

7.4.3.6 Integrators in Loop 2 and Loop 3

The design of integrators used to calibrate φ2 and φ4 has slight difference from that of integrator to calibrate φ3. Since the input duty cycle of the integrators is around 25%, the charge pump is designed to have triple current in the NMOS as the PMOS, in order to keep stable common mode level. Specifically, the PMOS transistor in replica branch is 3 times wider than the PMOS in the main branch as shown in Figure 64, so the PMOS output current can only copy one third of the NMOS current.

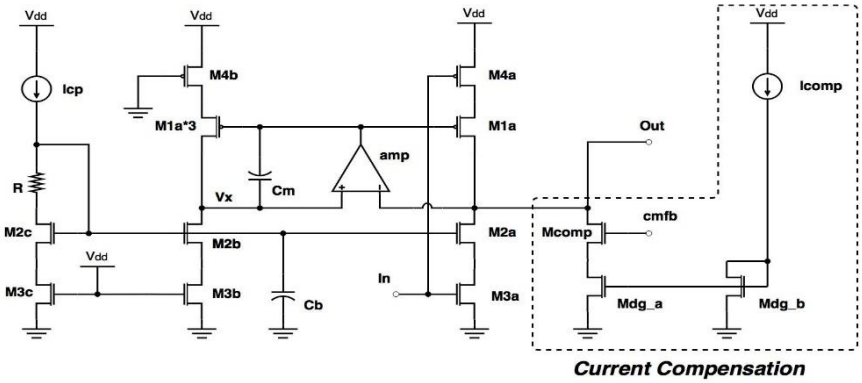

Figure 64 Charge Pump Used to Calibrate φ2 and φ4

The waveforms in the integrator are shown in Figure 65. We can see the voltage on the sampling capacitor has triple times falling slope than the rising slope.

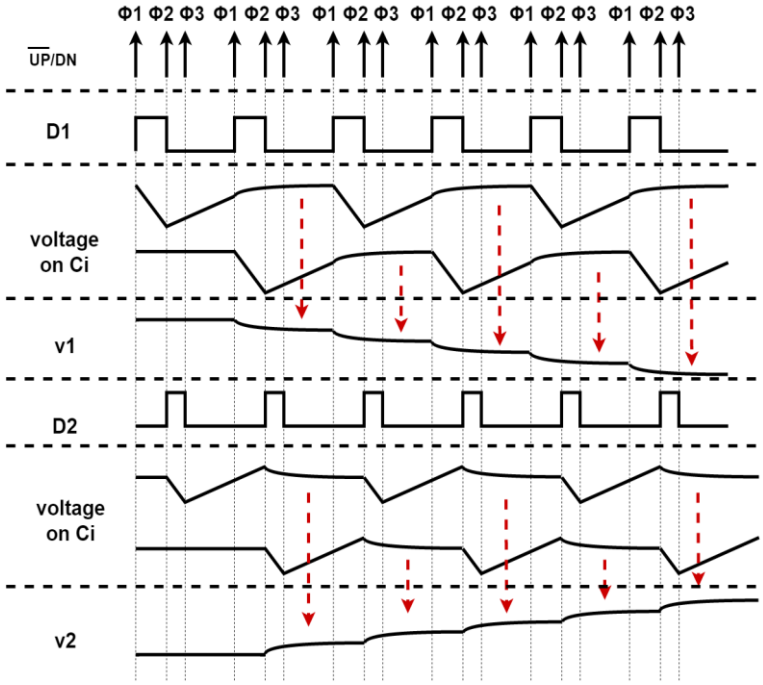

Figure 65 Waveforms in Integrator Used to Calibrate φ2 and φ4

7.4.4 Simulation Results

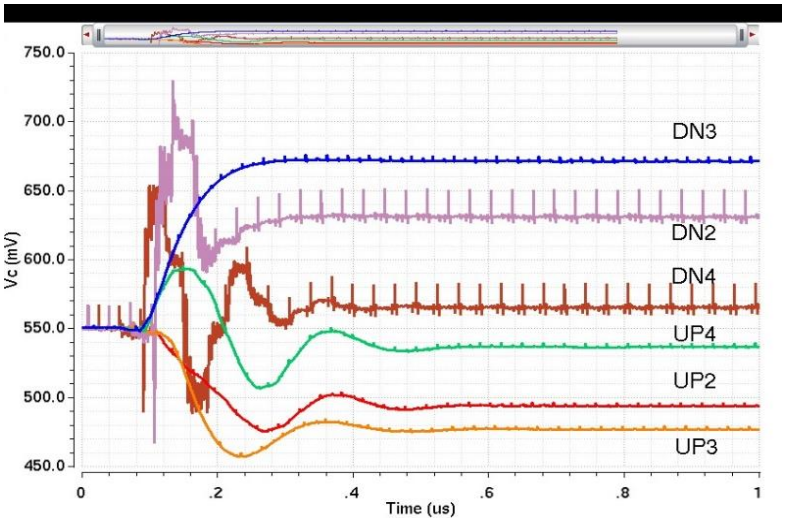

Figure 66 Transient Control Voltages of the Calibration System

The transient control voltages of the Calibration system are shown in Figure 66. And transient phase errors are shown in Figure 67 and Figure 68. After calibration, the phase error drops to around 0.1° from the initial phase error of +/- 10°.

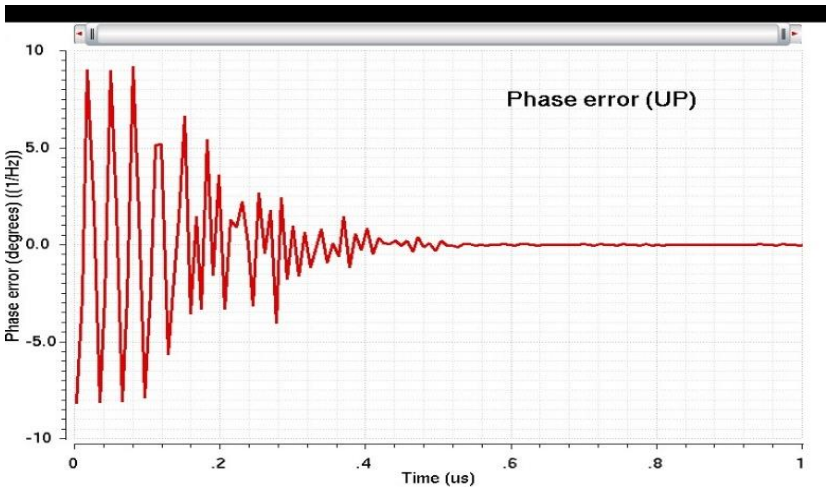

Figure 67 Transient Phase Error (UP)

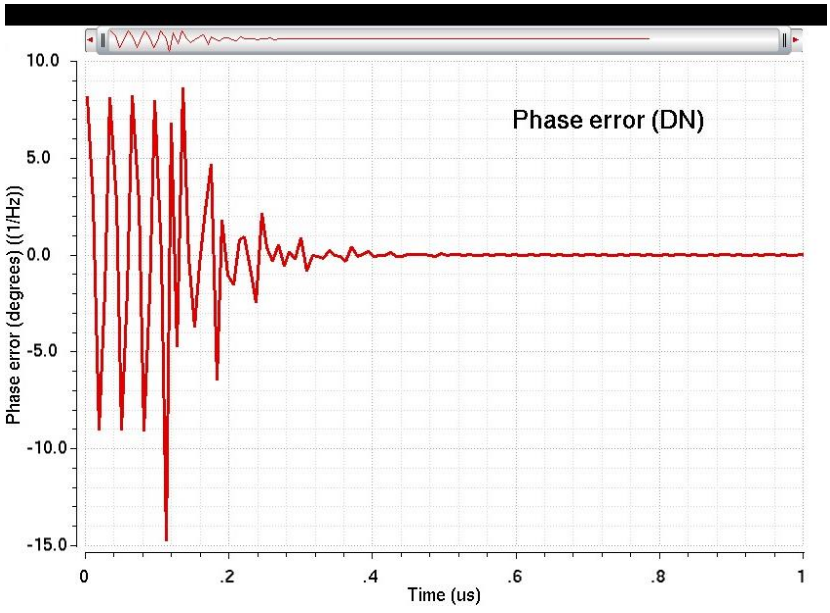

Figure 68 Transient Phase Error (DN)

8. SIMULATION RESULTS

In this section, system performance in Cadence simulation is presented.

8.1 Simple PLL

Firstly, the original PLL only system performance is shown. In the simple PLL, the CP is driven by signals with one reference period of 32MHz. Figure 69 is the transient settling of control voltage. The peaking in control voltage is about 200mV, this value is translated to reference spur of -50.21dBc in the output spectrum as shown as Figure 70.

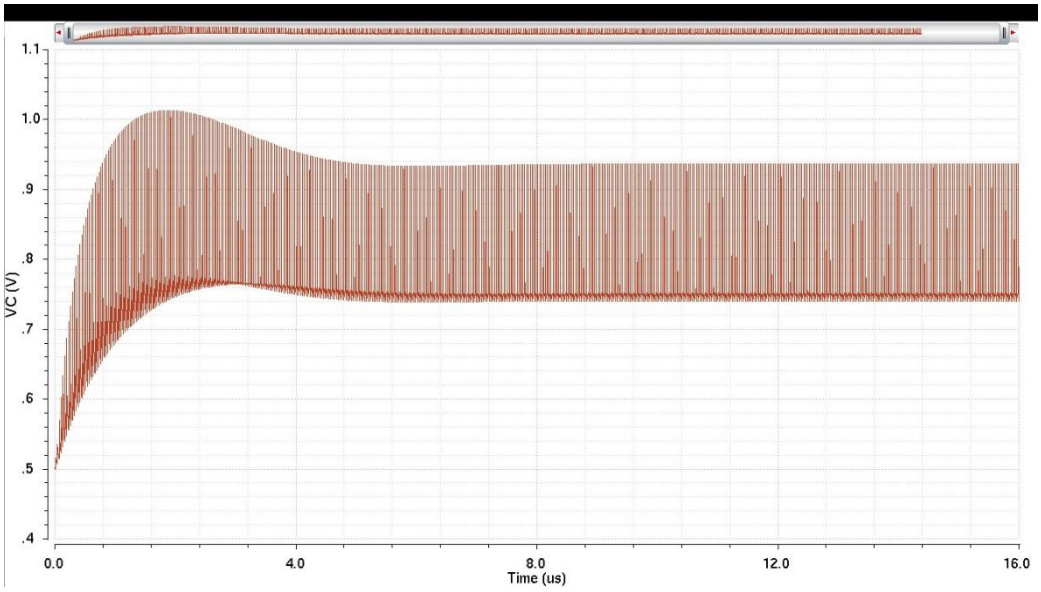

Figure 69 Control Voltage in Simple PLL System

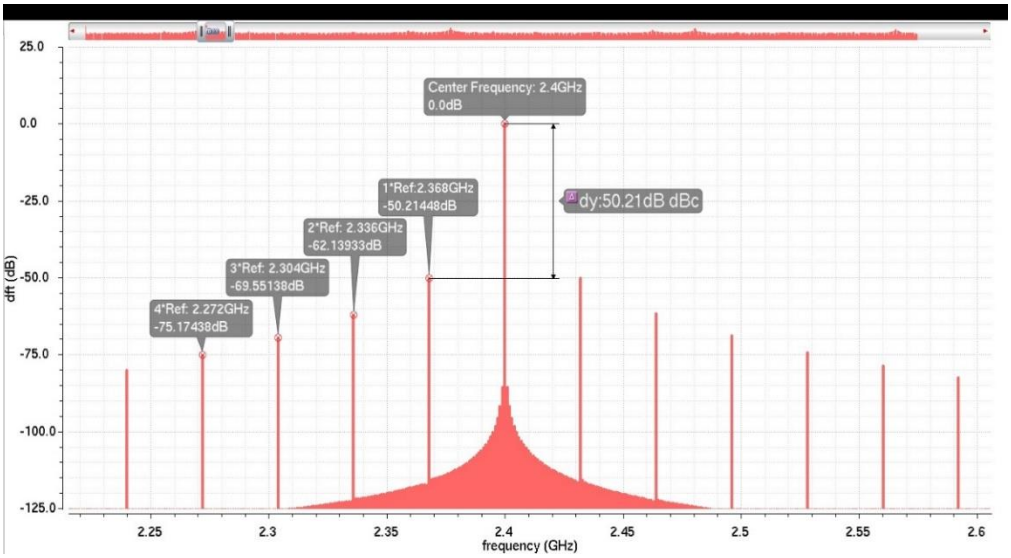

Figure 70 Output Spectrum of Simple PLL (Normalized to Center Frequency)

8.2 PLL with DLL without Mismatch

In the PLL with DLL embedded, the charge pump has 4 phases inputs, with the total charge current remaining the same. Thus, the transient behavior is not affected as shown in Figure 71. The value of glitches on the control voltage is around 40mV at a frequency of 4 times reference frequency which is 128MHz. The value of glitches is smaller than that of simple PLL because the loop is low pass for these glitches. The dft result of the output in the PLL with DLL embedded is shown in Figure 72. We can see the reference spur is -85.8dBc, which is improved about 35dB than the simple PLL structure.

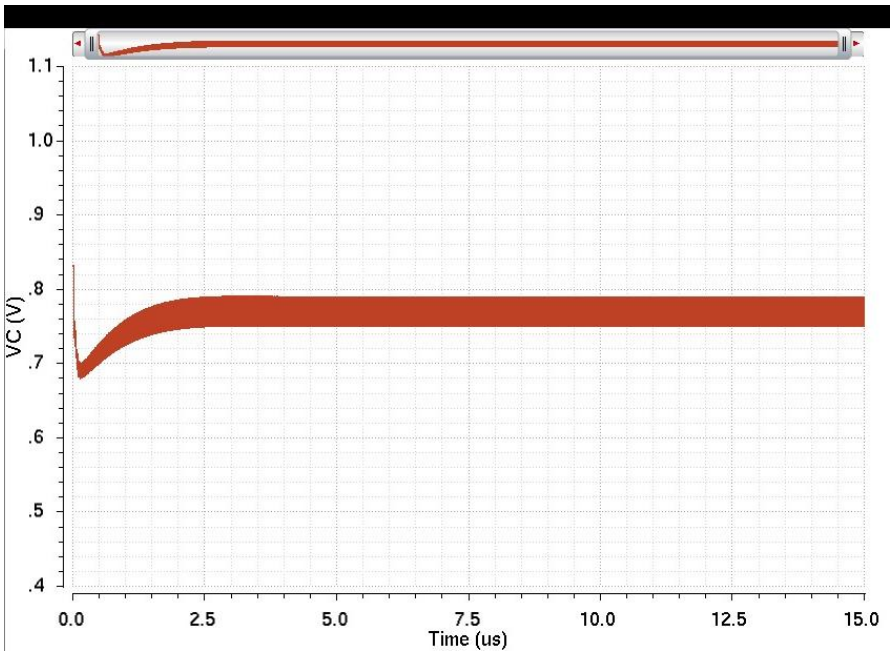

Figure 71 Control Voltage in PLL System with DLL (No Mismatch)

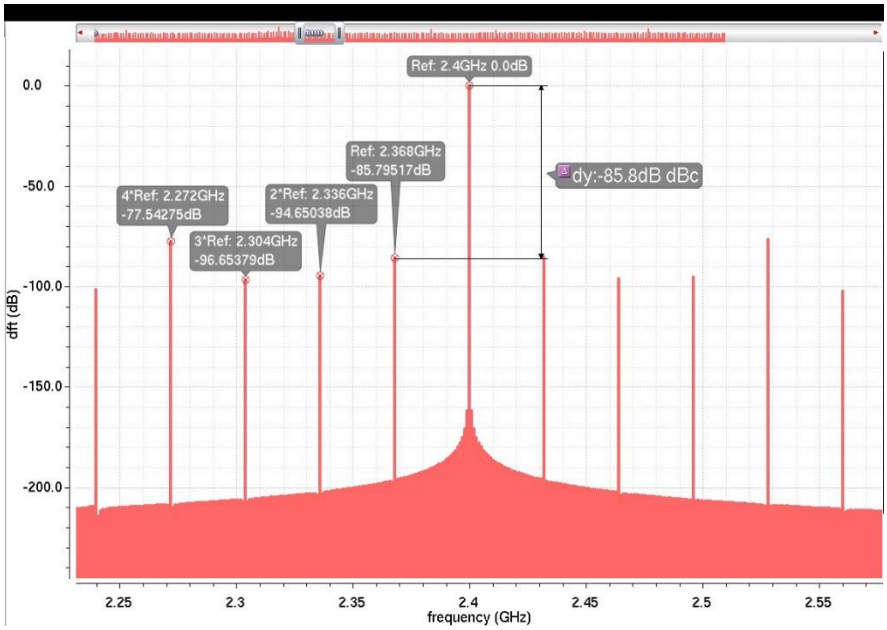

Figure 72 Output Spectrum of PLL System with DLL (No Mismatch) (Normalized to Center Frequency)

8.3 PLL and DLL with Delay Mismatch

As mentioned in previous parts, the VCDL in modern CMOS process suffers from mismatched between stages. In this part of simulation, mismatch patterns will be added in the 2 of VCDLs shown in Figure 73 and the corresponding simulation results will be shown in Table 9.

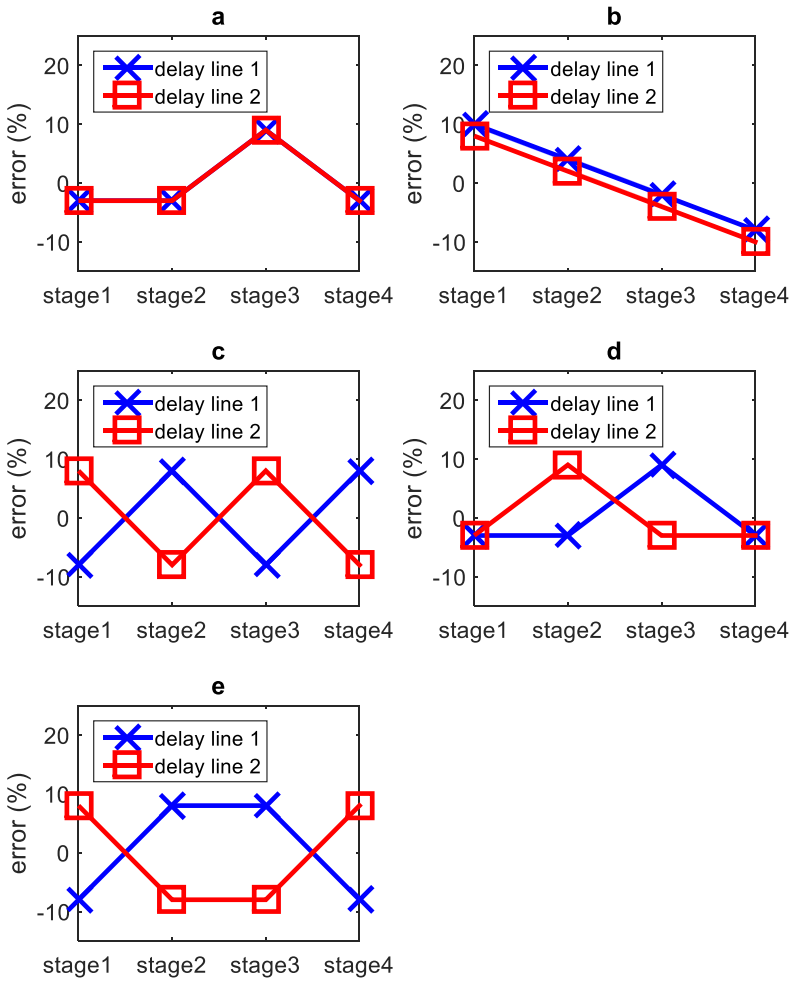

Figure 73 Mismatch Patterns inside DLL

Table 9 Spur Level on Output Spectrum Corresponding to Different Distribution Mismatches

	spurs (dBc)			
	1*Ref	2*Ref	3*Ref	4*Ref
no mismatch	-85.80	-94.65	-96.65	-77.54
a	-82.34	-87.07	-91.10	-76.42
b	-61.83	-83.16	-85.00	-76.45
c	-73.96	-62.57	-87.84	-76.93
d	-53.71	-72.32	-79.04	-76.59
e	-45.23	-82.74	-72.51	-75.75

It is reasonable that the worst case is that the two delay line has mismatches with opposite polarities: one is faster and faster to the backend and the other one is slower and slower. Simulation is conducted under assumption the maximum mismatch of one stage is 9%, as shown in Figure 74.

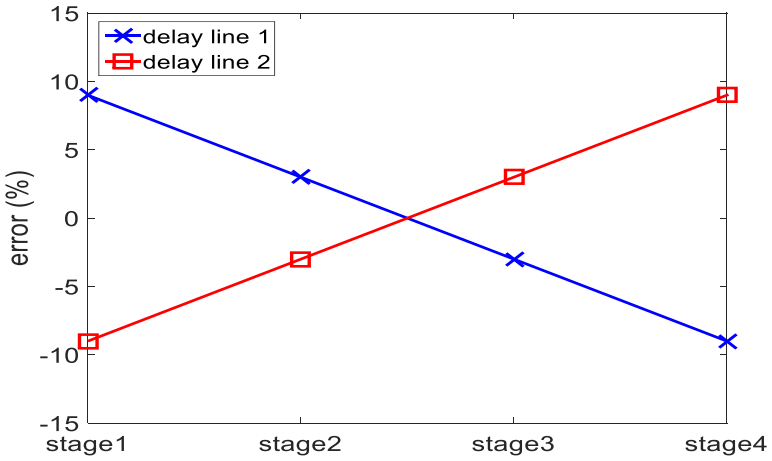

Figure 74 Delay Lines with Opposite Delay Distribution

Figure 75 is the transient control voltage (VC) on the charge pump output after the PLL settled. From Figure, we can see the peak to peak level of reference glitches on the charge pump output is 89.59mV. The output spectrum is shown in Figure 76.

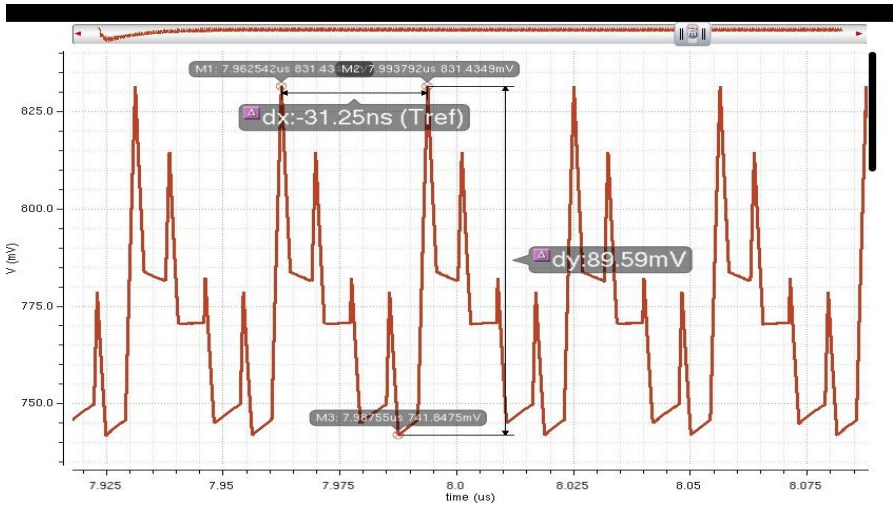

Figure 75 Control Voltage in PLL System with DLL (+/- 9% Mismatch)

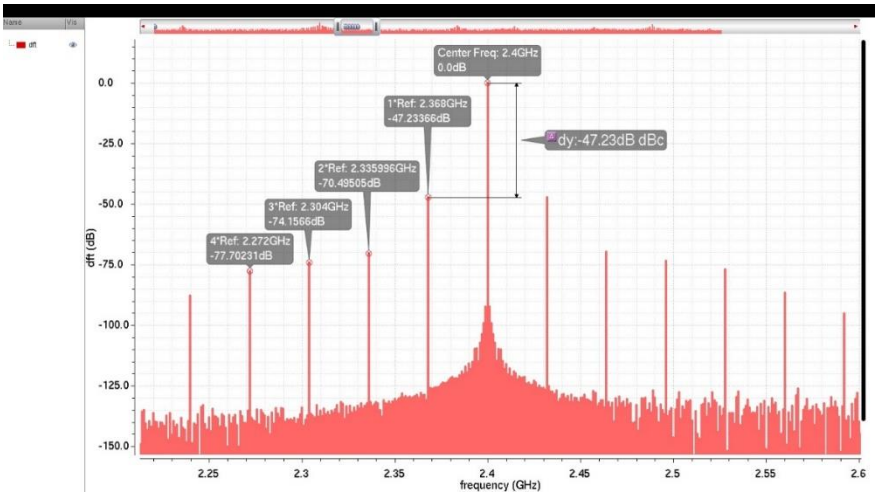

Figure 76 Normalized Output Spectrum of PLL System with DLL (+/- 9% Mismatch)

8.4 System with Continuous Time Delay Calibration

Figure 77 is the transient control voltage (VC) on the charge pump output. In the system, the calibration is enabled after receiving the DLL locked signal, as mentioned. Figure 78 shows the calibration introduces extra settling time in the PLL. But compare to the total PLL's settling period, this extra settling time is acceptable. Figure 76 shows that after calibration, the phase errors at the inputs of the charge pump are reduced to around 0.1°. But the pattern of error repeats with one reference frequency.

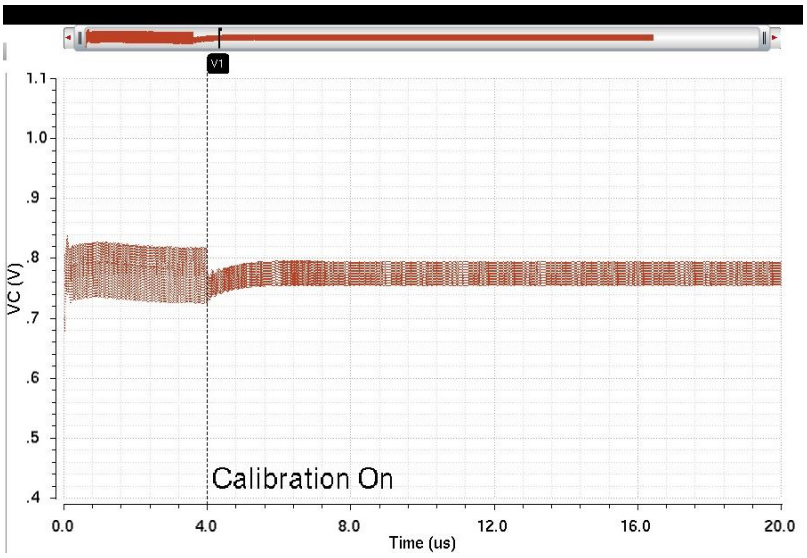

Figure 77 Control Voltage in PLL System with DLL (+/- 9% Mismatch) (with Continuous Time Calibration)

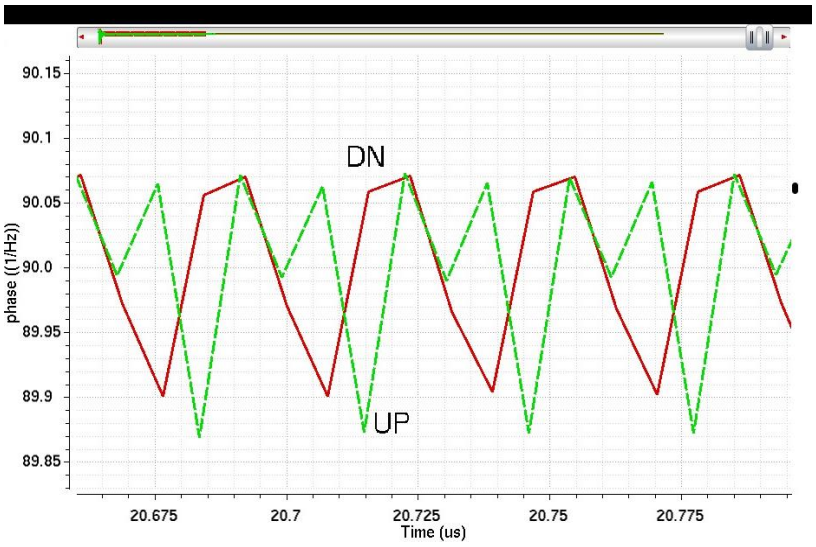

Figure 78 Phase of UP and DN (with Continuous Time Calibration)

According to Figure 79, the output reference spur is reduced to -85.86dBc.

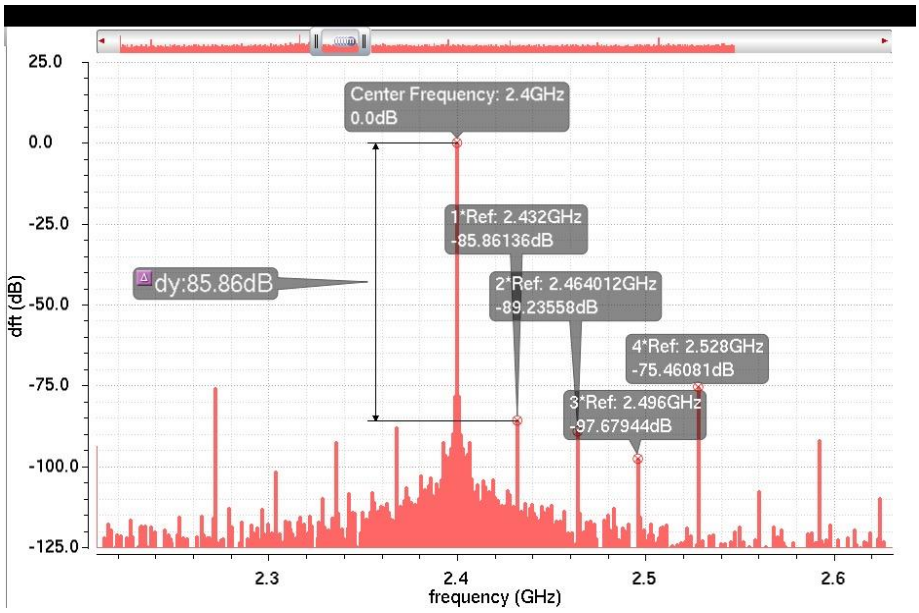

Figure 79 Normalized Output Spectrum of PLL System with DLL (+/- 9% Mismatch) (with Continuous Time Calibration)

8.5 System with Discrete Time Delay Calibration (SC)

The performance of final system as frequency synthesizer with DLL embedded and switch capacitor integrator based delay calibration is presented in this part.

Figure 80 is the transient control voltage (VC) on the charge pump output. In the system, the calibration is enabled after receiving the DLL locked signal.

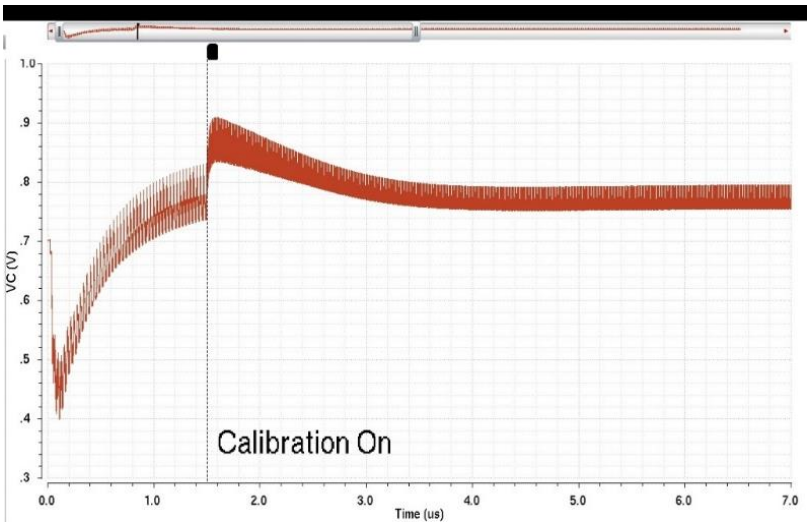

Figure 80 Control Voltage in PLL System with DLL (+/- 9% Mismatch) (with Discrete Time Calibration)

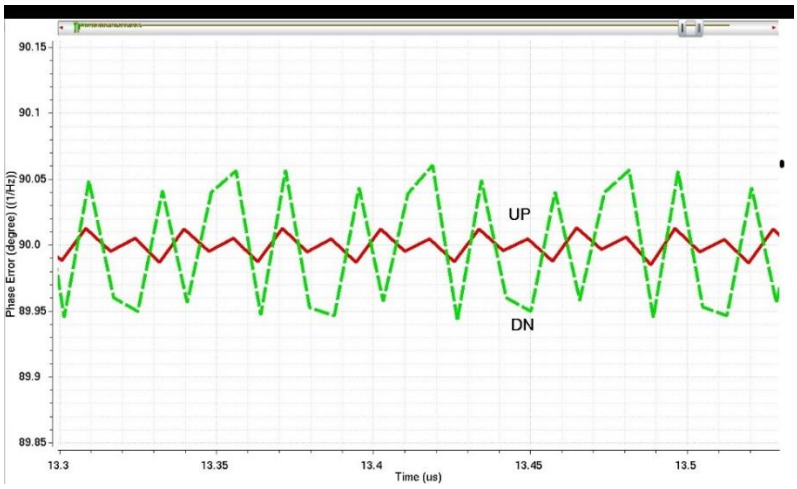

Figure 81 Phase of UP and DN

Figure 81 is the transient phases of the four UP signals and DN signals. From Figure 81, we can see the phase errors achieve under 0.05 degree after calibration.

Quantitive results can be shown in frequency domain. Figure 82 is the dft results of the system output. From Figure 82, we can see the level of reference spur is about -83.7 dBc. Therefore, the system achieves spur suppression of 33dB at a reference offset. Also, at double reference offset and at triple reference offset, the system achieves 26dB and 19dB spur suppression.

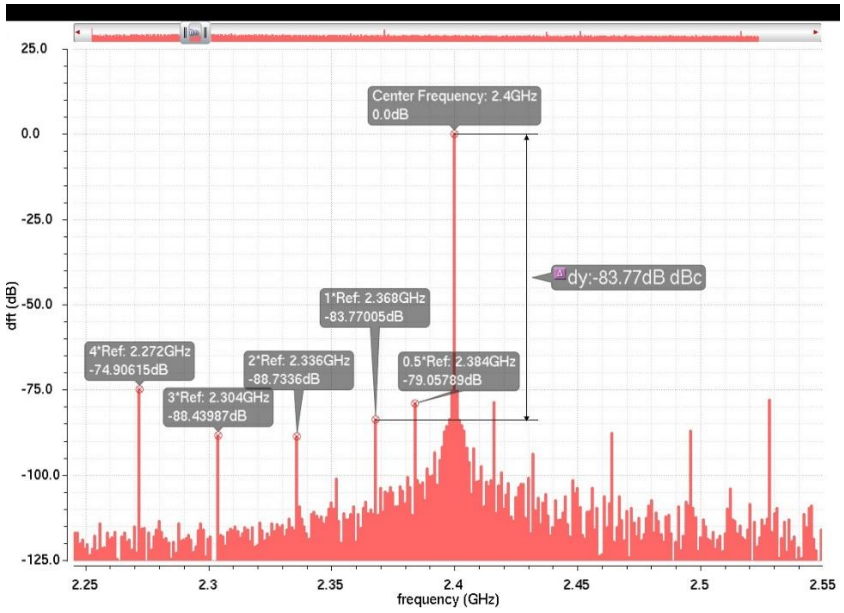

Figure 82 Normalized Output Spectrum of PLL System with DLL (+/- 9% Mismatch) (with Discrete Time Calibration)

But, the calibration system has bring some penalties. From Figure 70, we can see extra spurs appear at +/- half reference frequency offset, equal to -79.06dBc, which is undesired as they locate at lower frequency offset. Also, the level of out of band noise floor increase than the systems without calibration.

8.6 Comparison

The systems mentioned in the previous part are design to have same main loop with same charge pump and same loop filter. The simulation results are compared in Table 10.

Table 10 Comparison of Spurs

	spurs (dBc)			
	1*Ref	2*Ref	3*Ref	4*Ref
simple PLL	-50.21	-62.14	-69.56	-75.17
PLL with DLL (with no mismatch)	-85.80	-94.65	-96.65	-77.54
PLL with DLL (with +/- 9% maximum mismatch)	-47.23	-70.49	-74.16	-77.70
PLL with DLL (with +/- 9% maximum mismatch) (with continuous delay calibration)	-85.86	-89.24	-97.68	-75.46
PLL with DLL (with +/- 9% maximum mismatch) (with discrete delay calibration)	-83.77	-88.73	-88.44	-74.90

9. SUMMARY

In this project, a 2.4 GHz phase locked loop with a bandwidth of 2.2MHz is presented with reference spur frequency boosting realized by embedding a DLL. In the ideal case that no phase mismatches in DLL, the reference spur is reduced to -85.80dBc from -50.21dBc. The influence on the reference spur from different mismatch patterns is discussed. Two independent design of calibration systems including continuous time calibration system and switch capacitor based integrator calibration system are introduced in order to alleviate these effects. With calibration, the system achieves -83.77dBc of reference spur, with approximate 33dB, 26dB and 19dB rejection, in first, second and third reference spurs compared to the convention PLL structure.

Also, issues in this design exist and are valuable for potential further research. In the continuous time calibration system, the settling is slow and the calibration range is small due to the large signal swing in the system. In terms of the discrete time calibration system, extra spurs are introduced by the clock frequency in the calibration which are highly undesired.

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